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Pulse Ratings and Thermal Characteristics of Power Transistors

Christopher Jako

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PULSE RATINGS AND THERMAL CHARACTERISTICS - JAKO

PULSE RATINGS AND THERMAL CHARACTERISTICS
OF POWER TRANSISTORS

By

Christopher Jako

A Thesis

Submitted in Partial Fulfillment of the

Requirements for the Degree of

Master of Science in Electrical Engineering

The University of New Mexico

1957

This thesis, directed and approved by the candidate's committee, has been accepted by the Graduate Committee of the University of New Mexico in partial fulfillment of the requirements for the degree of

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DATE August 14, 1949

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WW Grannemann
CHAIRMAN

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Date

Thesis committee

ACKNOWLEDGEMENT

This study was carried out under the supervision of Dr. W. W. Grannemann. Other persons whose suggestions and advice were also appreciated are: Dr. Abraham Rosenzweig, Dr. Morris S. Hendrickson, and John M. Usry. Special thanks are due to Dr. Victor J. Skoglund for his encouragement and his help in solving the heat flow problem. The transistor protection device described in section 3.4 was developed and built by James R. Durant.

ACKNOWLEDGMENT

This study was planned and [illegible] under the supervision of [illegible] Grannemann. Other persons whose suggestions and encouragement were appreciated are Dr. Abraham [illegible], Dr. Robert [illegible], and John M. Berry. Special thanks are due to Dr. Victor [illegible] for his encouragement and his help [illegible]. The [illegible] transistor production device described in [illegible] was developed and built by James [illegible].

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CHAPTER I

INTRODUCTION

The dissipation of power is closely related to the generation of heat. A source of power, a battery for example, does not only have power dissipated in its load, but there is a power dissipation internally to the source. In the case of the battery, this can be represented by the expression $P = I^2 R$, where R represents the internal resistance of the battery. This indicates that by increasing the load on the battery, the internal power dissipation will also be increased.

In the case of transistors and vacuum tubes, the available power output is often limited by the amount of power that these devices can dissipate internally. Since power generates heat, an increased power dissipation increases the temperature of the components of these devices. In vacuum tubes excessive temperature melts the plate or other elements; in transistors it permanently damages the crystal. Our purpose here is to investigate the nature of this damage; i.e., to find out at what temperature the damage occurs and what amount of power will cause excessive heating. In particular, failure under pulsed conditions will be investigated.

1.1 <u>The Major Purpose of the Study</u>. Power transistors are used in switching circuits of various types. Their operation in these circuits can be considered as an essentially on-off operation. Designers working with these circuits found that the ratio of the

CHAPTER I

INTRODUCTION

The dissipation of power in [illegible]

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resistance of the battery. [illegible]

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power output is often limited [illegible]

vices can dissipate internally. [illegible]

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of these devices. In vacuum [illegible]

plate or other elements; in [illegible]

crystal. Our purpose here is [illegible]

i.e., to find out at what [illegible]

amount of power will cause excessive [illegible]

under pulsed conditions will be [illegible]

1.1 The Major Purpose of the Study. [illegible]

used in switching circuits of [illegible]

these circuits can be considered [illegible]

Designers working with these [illegible] on-time to the off-time[1] is a critical factor in determining the average power that the transistor can dissipate without exceeding its inherent temperature limits. Also it was apparent that the peak power, applied only for a short duration, may exceed several times the rated average power dissipation without damage to the transistor. This study establishes experimentally how the failure point depends on the duty factor. The analytical section makes an attempt to explain the results of the experimental work. Thus by experiment and analysis, the power rating of transistors in pulsed operation is established.

1.2 Scope of the Study. All of the experimental work was performed on the Clevite type CTP-1003 alloyed junction power transistor. The analytical work was first carried out for the general case using the alloyed junction geometry, after which the results were applied to the CTP-1003. This portion of the study and the procedure for finding the maximum peak pulse power, presented in section 6.2, can be applied to any transistor with similar geometry.

1.3 Transistors and Temperature. Transistor action is inherently temperature sensitive, and is described as such by its in-

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[1] This ratio will subsequently be referred to as duty factor, and may be expressed as a fraction or as a percentage.

$$\text{Duty factor (d.f.)} = \frac{\text{on-time}}{\text{off-time + on time}} = \frac{\text{pulse width}}{\text{period}}$$

on-time to the off-time[1] is [illegible] the average power that the transistor [illegible] its inherent temperature limit [illegible] power, applied only for a short [illegible] the rated average power dissipation [illegible] This study establishes experimentally [illegible] on the duty factor. The analytical [illegible] explain the results of the experimental [illegible] and analysis, the power rating [illegible] established.

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1.3 Transistors and [illegible] herently temperature sensitive. [illegible]

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[1] This ratio will [illegible] and may be expressed as [illegible] Duty factor (d.f.) = [illegible]

ventors.[2,3] It was recognized that the designer of transistor circuits had to take into account the variation of electrical properties with temperature.[4,5,6] The change in transistor parameters with temperature has been analyzed and described by several investigators.[7,8] Heat flow and heat dissipation in transistors, however, did not become a major design problem until the advent of the power transistor. Manufacturers were striving to improve the heat flow characteristics of their product in order to raise its power dissipating ability.[9] This brought about the development of a use-

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[2] J. Bardeen and W. H. Brattain, "Physical Principles Involved in Transistor Action," The Bell System Technical Journal, XXVIII, (April, 1949), p. 239.

[3] W. Shockley, Electrons and Holes in Semiconductors, (New York: D. Van Nostrand Company, Inc., 1950), p. 115.

[4] R. F. Shea, Principles of Transistor Circuits, (New York: John Wiley & Sons, Inc., 1953), pp.16-19 and 44-49.

[5]. A. W. Lo, et al., Transistor Electronics, (Englewood Cliffs, New Jersey: Prentice Hall, Inc., 1955), pp. 302-305.

[6] A. Coblenz and H. L. Owens, Transistors: Theory and Application, (New York: McGraw-Hill Book Company, Inc., 1955), pp. 58-59.

[7] A. Coblenz and H. L. Owens, "Variation of Transistor Parameters with Temperature," Proceedings of the Institute of Radio Engineers, XL, (November, 1952), p. 1472.

[8] W. W. Gartner, "Temperature Dependence of Junction Transistor Parameters," Proc. IRE, XLV, (May, 1957), p. 662.

[9] L. A. Griffith, "Power Transistor Temperature Rating," Paper presented to the Aircraft Electrical Society, (Minneapolis-Honeywell Regulator Company, 1955).

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[2] J. Bardeen [illegible] "Physical Principles Invol-ved in Transistor Action," The Bell System Technical Journal, XXVIII (April, 1949), p. 239.

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[4] R. F. Shea, Principles of Transistor Circuits, (New York: John Wiley & Sons, [illegible]

[5] A. W. Lo, and others, [illegible] New Jersey: Prentice-Hall, [illegible]

[6] A. Coblenz and [illegible] ation, (New York: McGraw-Hill [illegible]

[7] A. Coblenz and [illegible] meters with Temperature," [illegible] Engineers, XL, (November, [illegible]

[8] W. W. Gartner, "Temperature Dependence of Junction Transis-tor Parameters," Proc. IRE, [illegible]

[9] L. A. [illegible] Paper presented at [illegible] Honeywell Regulator [illegible]

ful method of junction temperature measurement.[10,11] With the help of this method, Mortenson investigated the junction temperature of grown bar junction transistors in pulsed operation.[12] He also applied the criteria of thermally stable operation, developed by Shea[13], to pulse circuits.[14] In the literature examined, no reference could be found to any work devoted to investigating the temperature at which catastrophic failure of the transistor occurs.

This work was preceded by an experimental study with the same purpose in mind,[15] the results of which were, however, considerably different from those to be presented here. The preceding work obtained experimentally the power levels at which the transistor reaches thermal runaway, and considered them as failure points. The approach of the present study, however, has been to isolate the effects of thermal runaway and to obtain the power level at which real failure occurs.

---

[10] K. E. Loofbourrow and J. Ollendorf, "Equipment for Measuring Junction Temperature of an Operating Transistor," Transistors I, (Princeton, N. J.: RCA Laboratories, March, 1956), p. 353.

[11] Bernard Reich, "Transistor Thermal Resistance Measurement," Electronic Design, IV, (December 1, 1956), p. 20.

[12] K. E. Mortenson, "Transistor Junction Temperature as a Function of Time," Proc. IRE, XLV, (April, 1957), p. 504.

[13] Shea, op. cit., pp. 125-130.

[14] Mortenson, op. cit., p. 511.

[15] R. L. Mann, "The Ratings of a Power Type Transistor," (Technical Report EE-2, Engineering Experiment Station, University of New Mexico, 1956).

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of this method, Mortenson [illegible]

grown bar junction [illegible]

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to pulse circuits. [illegible]

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10 K. E. Mortenson [illegible] ing Junction Temperature [illegible] (Princeton, N. J.: [illegible]

11 Bernard Reich, [illegible] Electronic Design, [illegible]

12 K. E. Mortenson, [illegible] Function of Time," [illegible]

13 Shea, op. cit., [illegible]

14 Mortenson, [illegible]

15 [illegible] (Technical Report [illegible] of New Mexico, 1956)

1.4 Organization of the Report. In order to present a complete account of this study, we will first describe and analyze the phenomena associated with the thermal failure of the transistor. Next we will give a description of the experimental method used to obtain failure data of the transistor, together with the results of the experiments. Chapter IV makes an attempt to calculate junction temperature by analytical methods. Following this, thermal resistance and its measurement are discussed. Finally, the results of the tests and the analysis are applied in developing a procedure to calculate the allowable peak power dissipation.

CHAPTER II

THERMAL FAILURE OF THE TRANSISTOR

A detailed description will be given of the transistor used in the experiments. The different types of failures in general, and thermal failure in particular, will be discussed.

2.1 The Transistor and Its Construction. The transistor used in the experiments was the Clevite type CTP-1003 alloyed junction power transistor. Fig. 1, page 7, illustrates its mechanical construction and its dimensions. The crystal and its geometry are shown in Fig. 2, page 8. Typical V_c - I_c characteristics and β are given in Fig. 3, page 9. The manufacturer's specifications of the transistor are given below.

Absolute Maximum Ratings

Instantaneous collector to base voltage	-60 V
Collector supply voltage	-30 V
Junction temperature	85°C
Instantaneous total peak power	25 W
Average total power with infinite heat sink at 25°C	25 W
Average total power (no heat sink) in free air at 25°C	2.25 W

Characteristics @ 25° C

Test	Conditions	Test Requirements
Collector cut-off current	V_{cb} - -60 V I_e - 0	I_{co} = 2.0 mA, max.
Emitter cut-off current	V_{eb} - -6 V I_c - 0	I_{eo} = .20 mA, max.
Power gain, common emitter, transformer coupled	V_{cc} - 14.2 V I_c - .37 A R_L - 30 ohms R_g - 10 ohms	P_g = 23.0 db, min.
Power gain cut-off frequency	Same as for power gain	f_{p_g} = 4 Kc, min.

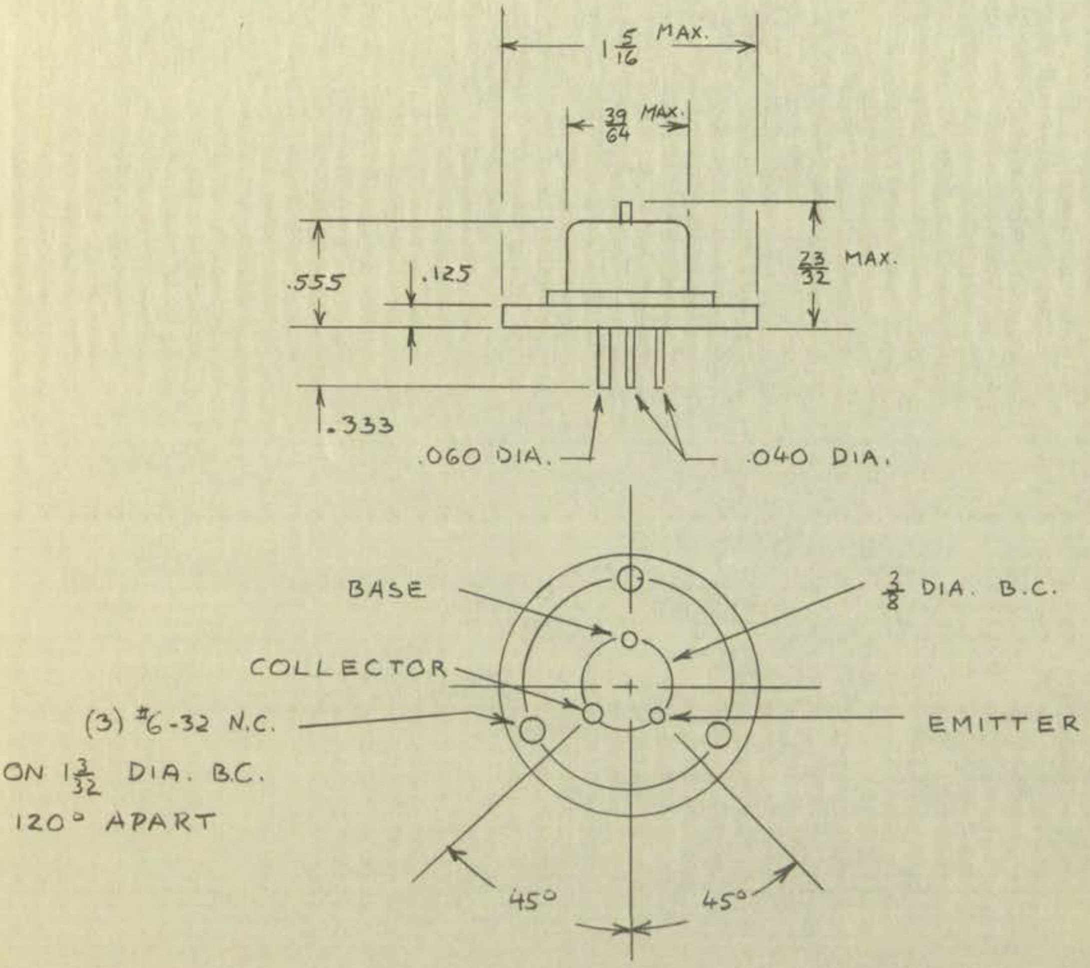
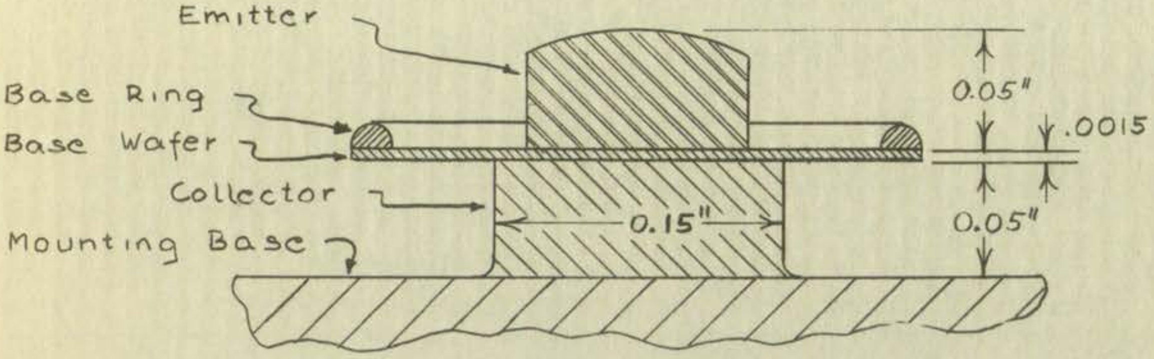
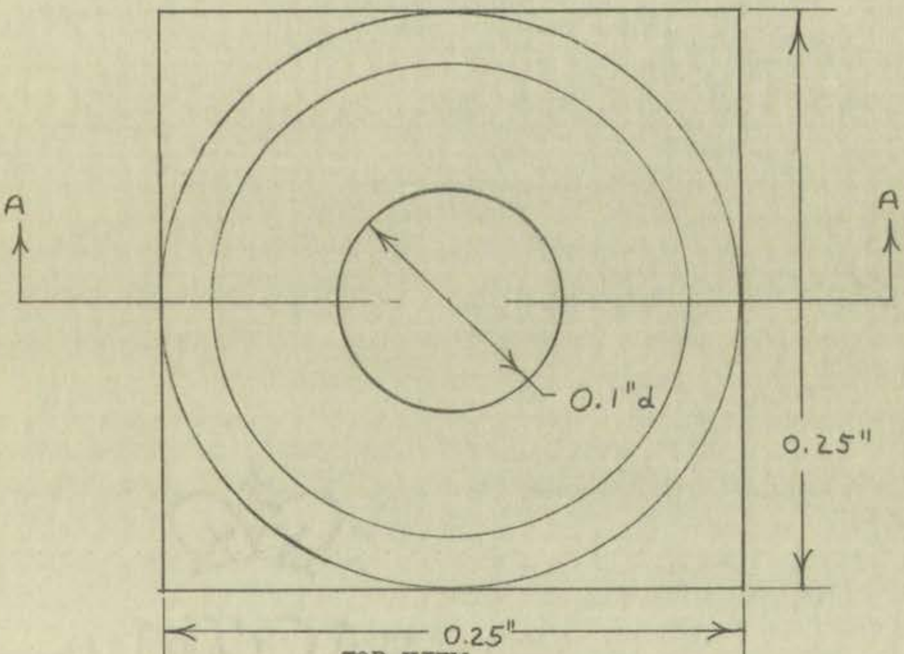


Figure 1

Transistor Dimensions
Clevite CTP 1003
No Scale



SECTION A - A



TOP VIEW

Figure 2

Construction of the Transistor Crystal
Clevite CTP-1003
No Scale

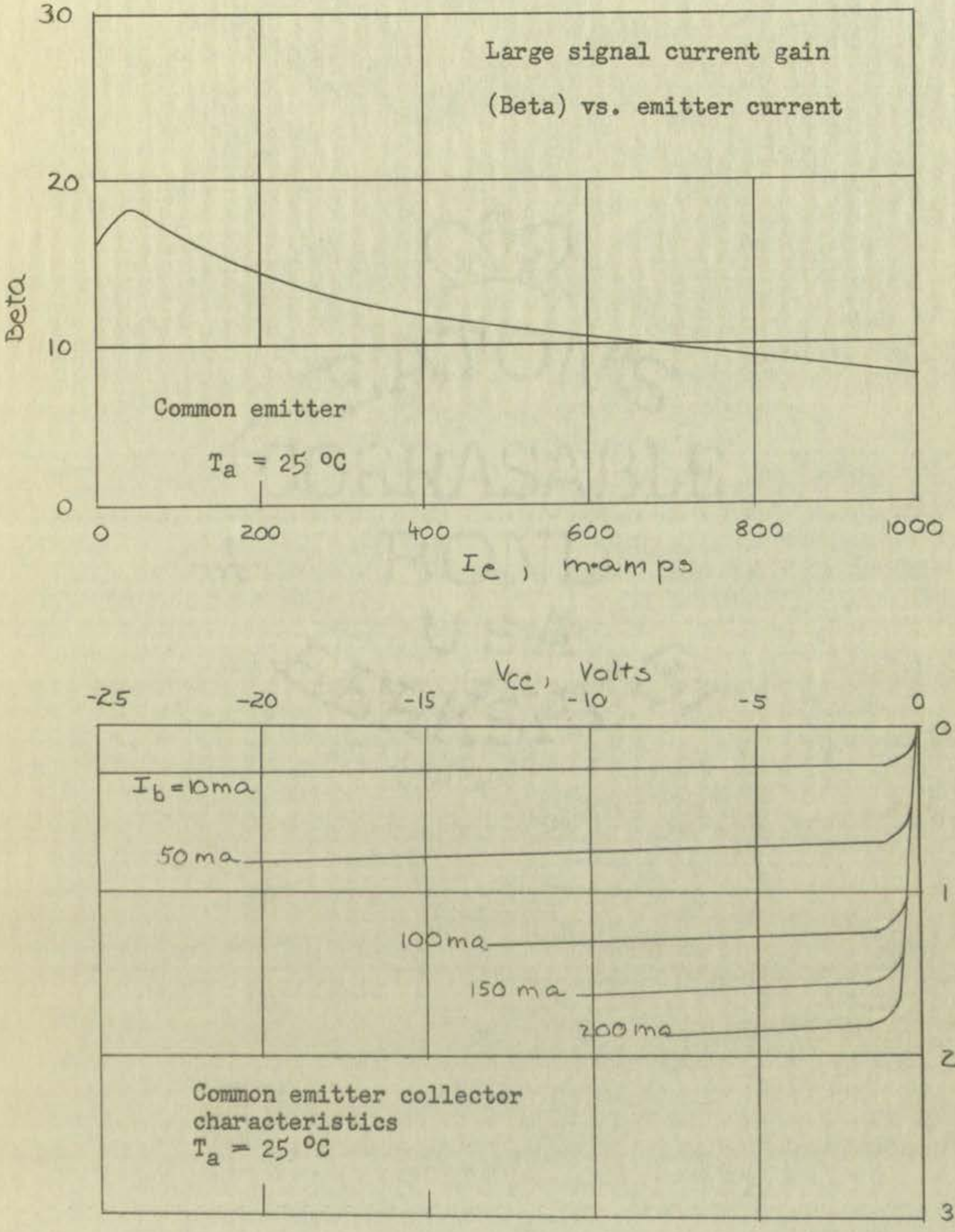


Figure 3

Typical Transistor Characteristics
Clevite CTP 1003

2.2 Failures. Like all man-made devices, transistors are subject to failure. Three common types of failure are: (1) voltage breakdown, (2) surface contamination and (3) thermal damage.

The first of these results from an excessive potential across the collector-emitter; and the damage thus caused is not necessarily permanent. The second, surface contamination, may be caused by moisture at the junction and can be eliminated by proper manufacturing methods.[1]

2.3 Thermal Failure. If the junction temperature reaches a certain level, the transistor circuit may become thermally unstable. A cumulative process, often referred to as thermal runaway, will result and eventually the high temperatures developed in the crystal will permanently damage the junction.

2.3(a) Leakage Current. Thermal instability is caused primarily by the temperature sensitive reverse current of the collector junction.

Considering Fig. 4 on the following page, the current flowing in the circuit is the reverse current of a diode, formed by the collector-base junction. This current is approximately equal to the

---

[1] A. Coblenz and H. L. Owens, Transistors: Theory and Application, (New York: McGraw-Hill Book Company, Inc., 1955), p. 215.

saturation current of the junction and can be written as follows:[2,3]

$$I_{co} \approx I_s = A\ e^{-qV/KT} \qquad (2\text{-}1)$$

where A = constant, determined by geometry and material used,

q = electron charge,

V = energy gap of the semiconductor in volts,

I_s = saturation current,

T = absolute temperature,

K = Boltzmann's constant.

Due to the variation in A, the leakage current will differ considerably between different transistors. The typical variation of I_{co} with temperature is given in Fig. 5, page 12, for the CTP-1003 transistor.

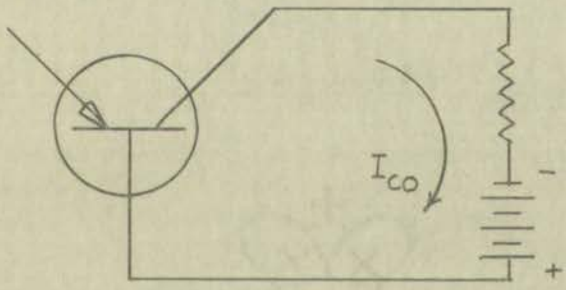


Figure 4

Collector Leakage Current

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[2] W. Shockley, Electrons and Holes in Semiconductors, (New York: D. Van Nostrand Company, Inc., 1950), p. 314.

[3] J. Bardeen and W. H. Brattain, "Physical Principles Involved in Transistor Action," The Bell System Technical Journal, XXVIII, (April, 1949), p. 268.

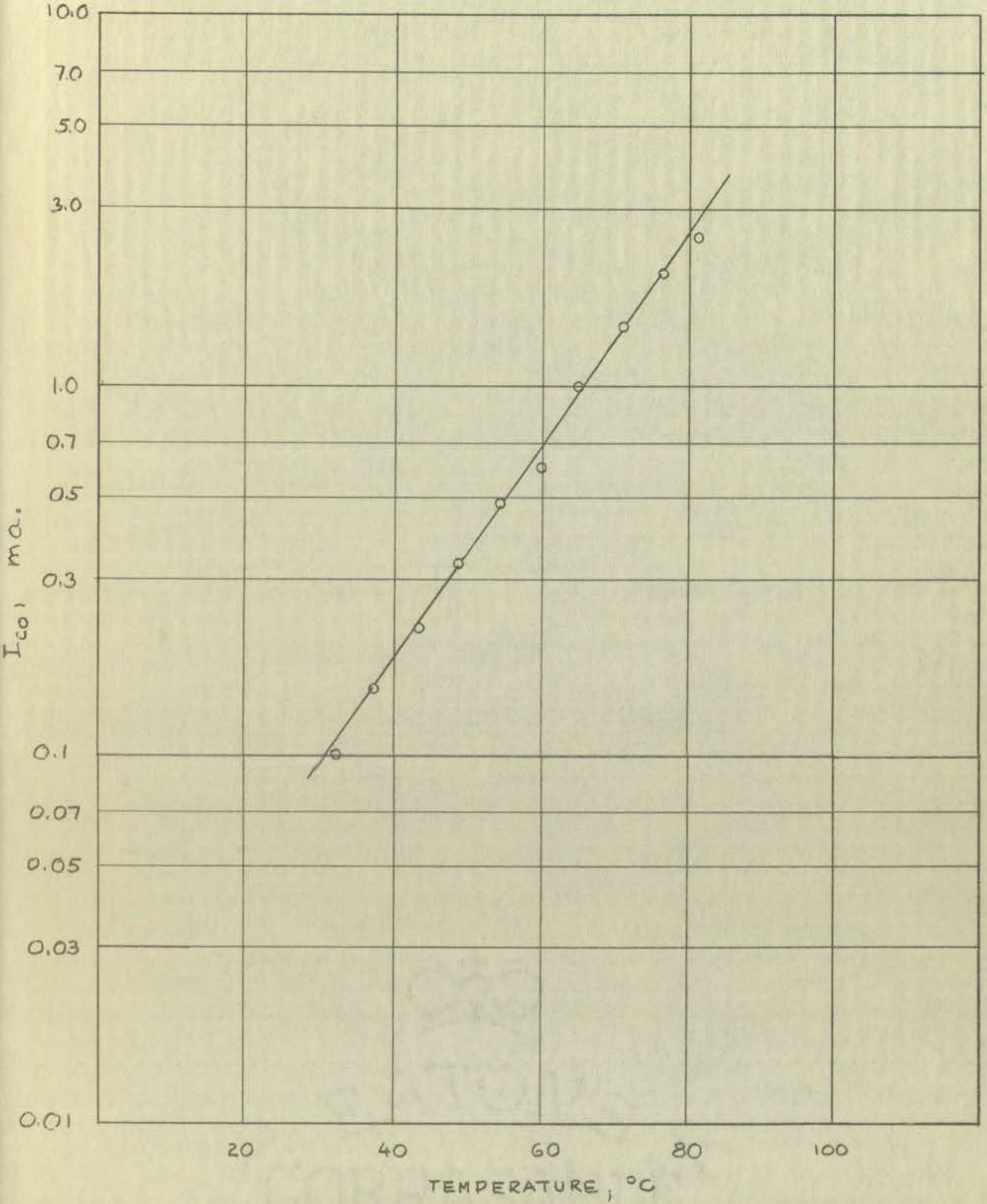

Figure 5

Typical Collector Leakage Current vs.
Temperature Curve

2.3(b) Thermal Instability. If the collector current of a common-base connection is given as

$$I_c = I_{co} + \alpha I_e \tag{2-2}$$

then at low temperatures $I_{co} \ll I_c$, or the leakage current is a small fraction of the total collector current. If, however, the temperature is greatly increased, I_{co} will become a larger percentage of I_c. This is due to the increase of I_{co} in accordance with equation (2-1) and also to the decrease of α with temperature in equation (2-2). Thermal instability occurs if I_{co} reaches a critical value (at temperature above 100 °C in most transistors).

If the cause and its effect are indicated by an arrow, then the process of thermal instability can be expressed as follows:

$$T_1 \rightarrow I_{co} \rightarrow P \rightarrow T_2$$

If $T_2 > T_1$, then thermal instability will result.[4] Unless limited by the external circuit, the collector current and junction temperature will rapidly climb to higher and higher values until the crystal is destroyed. This process may take from a fraction of a second to several seconds, depending on the power dissipating ability of the transistor.

2.3(c) Nature of the Failure. A test of the failed or burned out crystal will normally reveal a short circuit between the collector

---

[4] K. E. Mortenson, "Transistor Junction Temperature as a Function of Time," Proc. IRE, XLV, (April, 1957), p. 504.

and the emitter. The diode action of the junctions, however, remains undisturbed. This might indicate that a high junction temperature would cause the Indium to melt in spots and diffuse farther into the base region until contact is established with the opposite junction.[5]

To substantiate this theory, the crossection of a good and a failed crystal were microscopically examined.[6] The photomicrographs on page 15 bear out the above assumption. The junctions of the good crystal appear fairly evenly spaced, whereas the emitter junction of the burned out transistor shows rough irregularities. The base width between the two junctions appears to be greatly reduced in some spots. By repeated grinding and polishing of the sample, a point could, in all probability, be located where the emitter material would extend into the collector region.

Another interesting observation was made on the damaged transistor. The microscope revealed several small pieces of Germanium embedded in the Indium region of the emitter. This would also indicate that the Indium was in a molten state at the junction when failure occurred.

---

[5] Melting point of Indium is 155 Centigrade.

[6] The procedure used for the preparation of samples is described in Appendix B, page 75.

and the emitter [illegible] undisturbed. This [illegible] would cause the [illegible] base region until [illegible]

To substantiate [illegible] failed crystal was [illegible] on page 15 [illegible] crystal appear [illegible] the burned out [illegible] between the two [illegible] By repeated [illegible] all probability, [illegible] into the collector region.

Another interesting case [illegible] sistor. The [illegible] embedded in the Indium region [illegible] cate that the Indium [illegible] occurred.

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5 Melting point of [illegible]

6 The [illegible] cribed in Appendix [illegible]

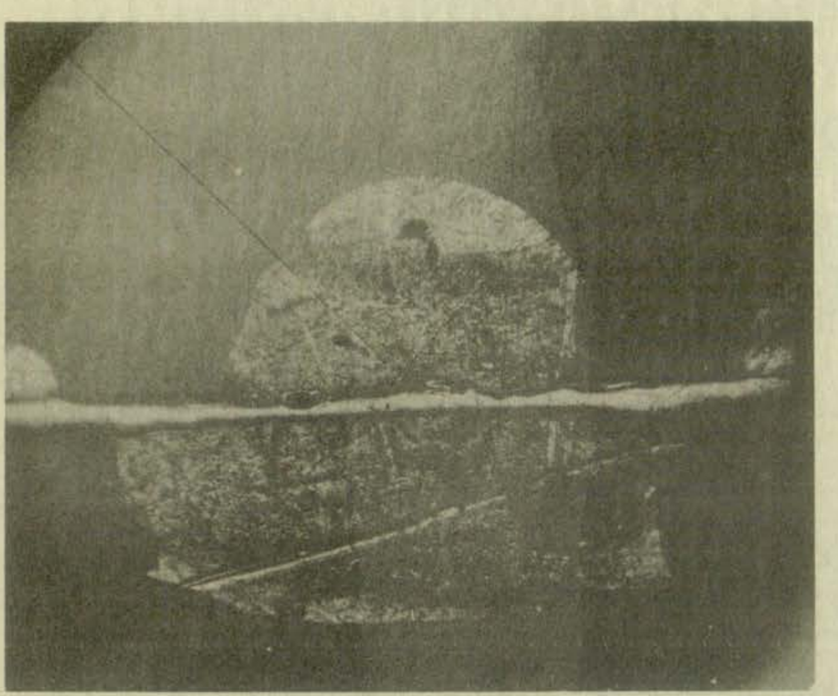

Figure 6

Crossection of Transistor after Thermal Failure

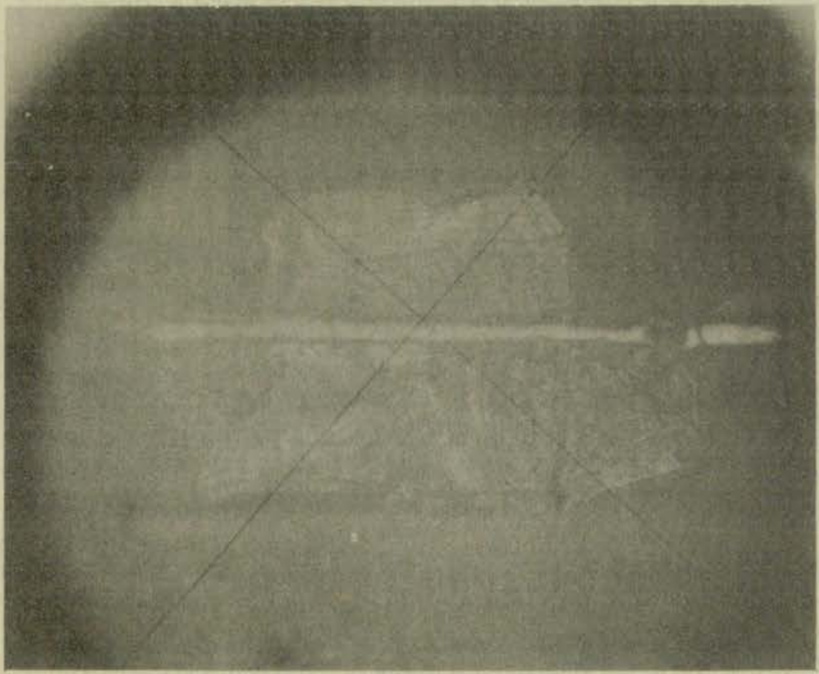

Figure 7

Crossection of Good Transistor

CHAPTER III

THE FAILURE TESTS AND THEIR RESULTS

Our purpose is to determine the amount of power necessary to produce a damaging amount of heat in the transistor crystal under pulsed conditions. To achieve this, an experimental method has been devised whereby the effects of thermal instability may be eliminated An analysis of the problems and variables will be given here, followed by a description of the experimental apparatus and procedure. Finally, the results of the tests will be stated in the conclusion of the chapter.

3.1 Pulse Input at the Base. If the power dissipation in the transistor is not continuous because of the power applied being in the form of periodic rectangular pulses, the maximum power rating[1] depends greatly on the duty factor of the pulsed input. Our prime purpose is to establish experimentally how the failure point of the transistor depends on this variable.

First we consider the common-emitter connection of Fig. 8 on the next page. By raising the input level of the pulse source, the power dissipation in the transistor may be increased to the point at which thermal instability will be caused by the process described in Section 2.3(c). This approach was used in a preliminary investi-

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[1] Maximum average power is meant.

Our purpose [illegible]
produce a [illegible]
poised conditions [illegible]
devised means [illegible]
An analysis of [illegible]
by a description [illegible]
the results of the [illegible]
chapter.

3.1 [illegible]
the translator [illegible]
in the form of [illegible]
depends greatly on [illegible]
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translator depends [illegible]

First we [illegible]
on the next page [illegible]
the power [illegible]
at which [illegible]
in Section [illegible]

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[1] [illegible]

gation preceding the present work.[2]

The above method has two shortcomings: (1) The maximum power level obtained represents the point at which thermal instability and not failure occurs: and (2) in addition to the pulse power, there is a large amount of steady power dissipated due to the high leakage current at higher temperatures.

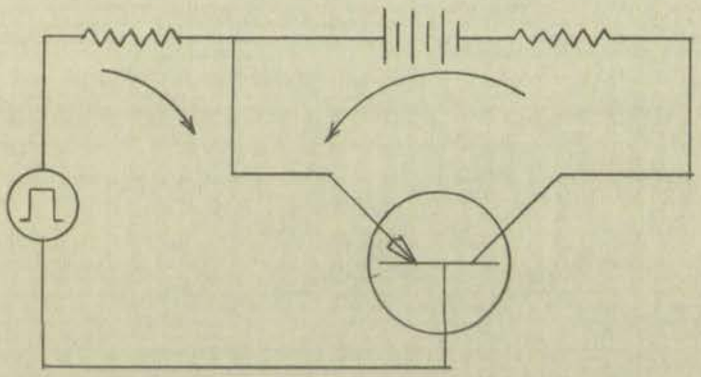

Figure 8

Test Circuit - Base Input

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[2] R. L. Mann, "The Ratings of a Power Type Transistor," (Technical Report EE -2, Engineering Experiment Station, University of New Mexico, 1956).

gation preceding the [illegible]

The [illegible] level obtained [illegible] not failure [illegible][2] [illegible] a large amount of [illegible] current at higher temperatures.

Fig. [illegible]

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[2] R. L. [illegible], "The [illegible] of [illegible]," (Technical Report 32 [illegible] of New Mexico, 19[illegible]).

3.2 Pulse Input at the Collector. To eliminate the undesirable effects of the connection of Fig. 8, a different circuit had to be devised. Fig. 9 represents a common-emitter connection with a pulse source in the collector circuit. If the pulse source is represented by a battery and a switch connected in series, it is evident that no leakage current can flow between pulses. Thermal runaway is also prevented, since the pulse duration is short as compared to the thermal time constant of the whole transistor. The power added due to the current flow in the emitter-base loop, is very small compared to the power dissipated in the collector circuit.

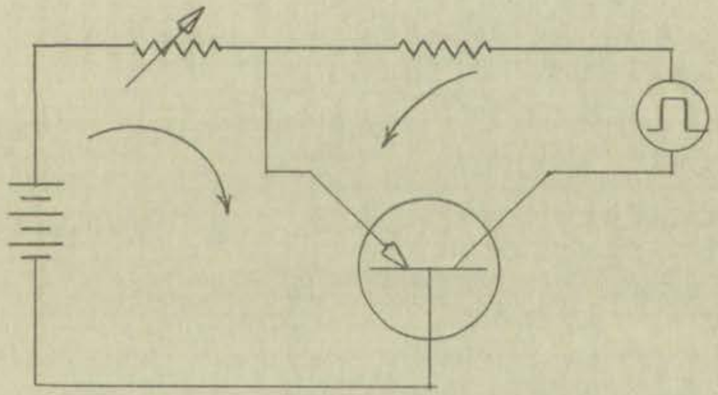

Figure 9

Test Circuit - Collector Input

3.2 Pulse Input [illegible]

able effects of the [illegible] be devised. Fig. 9 [illegible] source in the collector [illegible] by a battery and a [illegible] leakage current can [illegible] prevented, since the [illegible] time constant of the [illegible] current flow in the [illegible] power dissipated in the [illegible]

Fig. [illegible]

Test Circuit [illegible]

3.3 The Pulse Source. Two factors control the design of the pulse source. These are: (1) the peak voltage desired and (2) the impedance of the load.

Since the transistor is rated at maximum 60 volts, the pulse amplitude need not be any higher. The impedance of the collector-emitter circuit may be of the order of several K-ohms at room temperature.[3] At high junction temperatures, however, this impedance may drop as low as one ohm.[4] To be able to transfer power to the load, the source must have an equally low internal impedance. This was accomplished by the use of a pulse amplifier with a transformer output. The schematic diagram for the pulse source is given in Fig. 10, page 21.

3.4 Transistor Protection Device. Since the information desired is the failure point of the transistor, it seems that a large number of them would be required. In order to cut expenses, a device was developed by means of which an indication of failure could be obtained without actually destroying the crystal. This was done by utilizihg the increase in current pulses, which occurs just before transistor failure.

The functioning of the device is shown in the block diagram on

---

[3] This is assuming that the collector junction is biased in the reverse direction or conventional current flow from emitter to collector for the PNP transistor.

[4] R. F. Shea, Principles of Transistor Circuits, (New York: John Wiley & Sons, Inc., 1953), pp. 46-47.

page 22. The pulse generator determines the frequency and the width of the pulses. The power pulse amplifier acts as an impedance matching device as well as greatly increasing the power in the pulses. The current pulses are monitored with a one ohm resistor in the collector circuit of the transistor. The voltage pulses, which are proportional to the current, are amplified and applied to the diode integrator circuit. The diode integrator circuit produces output voltage pulses only when the current pulses are increasing in the transistor circuit. The pulses from the diode integrator circuit are amplified, differentiated, clipped, amplified again, and applied to the Eccles-Jordan circuit. The Eccles-Jordan circuit triggers on these pulses and turns off the pulse generator. Thus when the current pulses in the transistor circuit increase rapidly enough, the pulse generator is turned off.

3.5 The Test Set-Up and Its Components. The operation of the test set-up is illustrated by the block diagram of Fig. 12, page 23. The pulse generator drives an amplifier; the output of the amplifier is fed into the collector circuit of the transistor through a monitoring device. A clipping circuit improves the wave shape of the pulses. The monitor serves two purposes: with the scope it gives an indication of the current; and it also provides the signal for the protection device when failure is imminent. If the protection device is triggered, it will interrupt the operation of the pulse generator.

Variation of the bias source and also variation of the pulse amplitude provide control of the power dissipation. The power is page 22. The pulse [illegible] in [illegible] the [illegible] of the pulses. The [illegible] a [illegible] ing device as well as [illegible] in [illegible] current pulses are [illegible] circuit of the transistor. The [illegible] to the current, are [illegible] cuit. The diode integrating circuit [illegible] when the current [illegible] pulses from the diode integrating circuit [illegible] clipped, amplified [illegible] are applied [illegible] The Eccles-Jordan circuit [illegible] pulses [illegible] pulse generator. [illegible] current pulses [illegible] cuit increase rapidly [illegible] the pulse generator [illegible].

3.5 The [illegible]. The [illegible] test set-up is illustrated [illegible] The pulse generator [illegible] is fed into the collector circuit of the transistor through a [illegible] ing device. A [illegible] The monitor [illegible] of the current [illegible] device when failure is [illegible] it will [illegible] of the pulse generator.

Variation [illegible] amplitude [illegible]

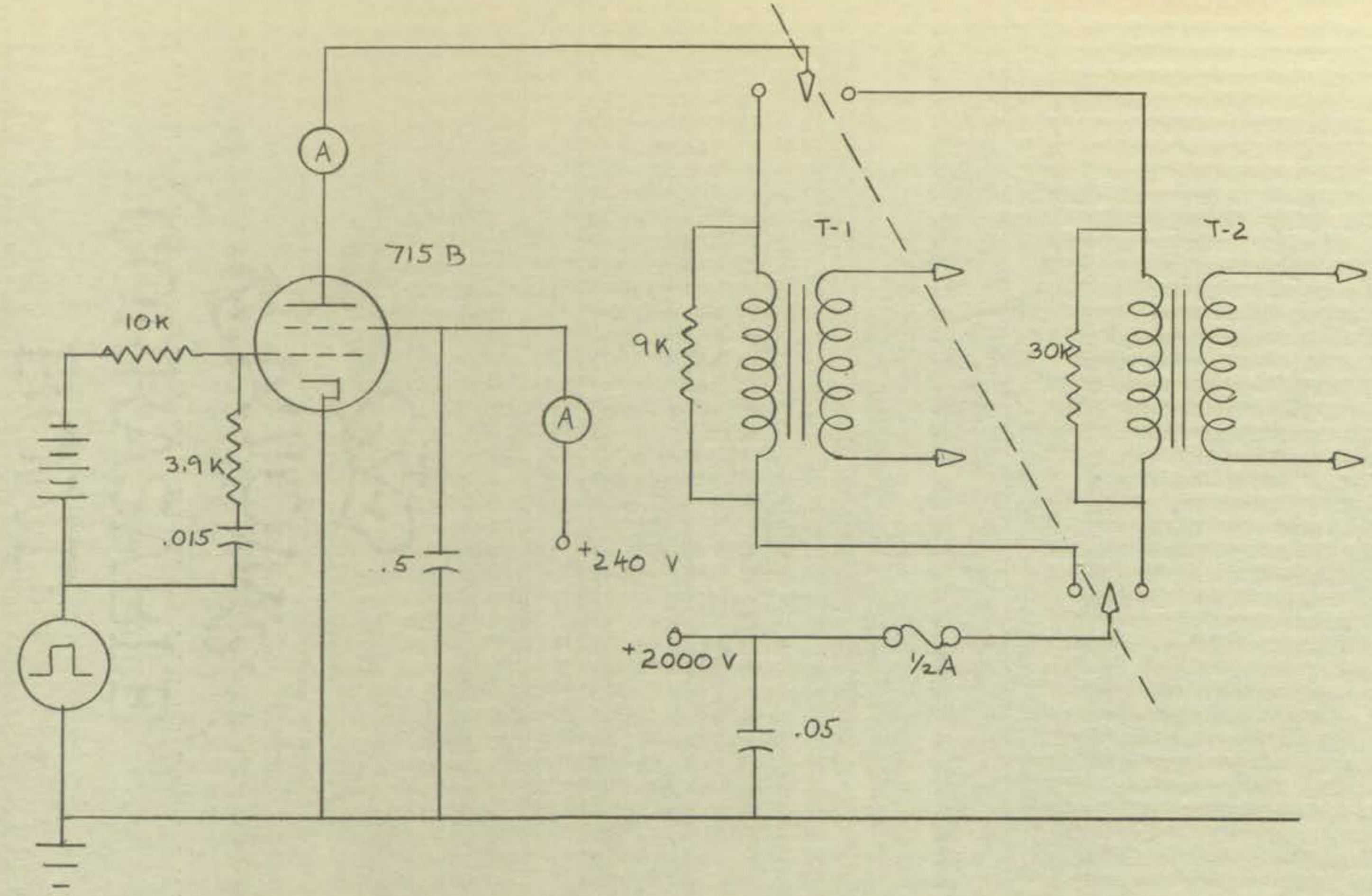

Figure 10

Circuit Diagram of the Pulse Amplifier

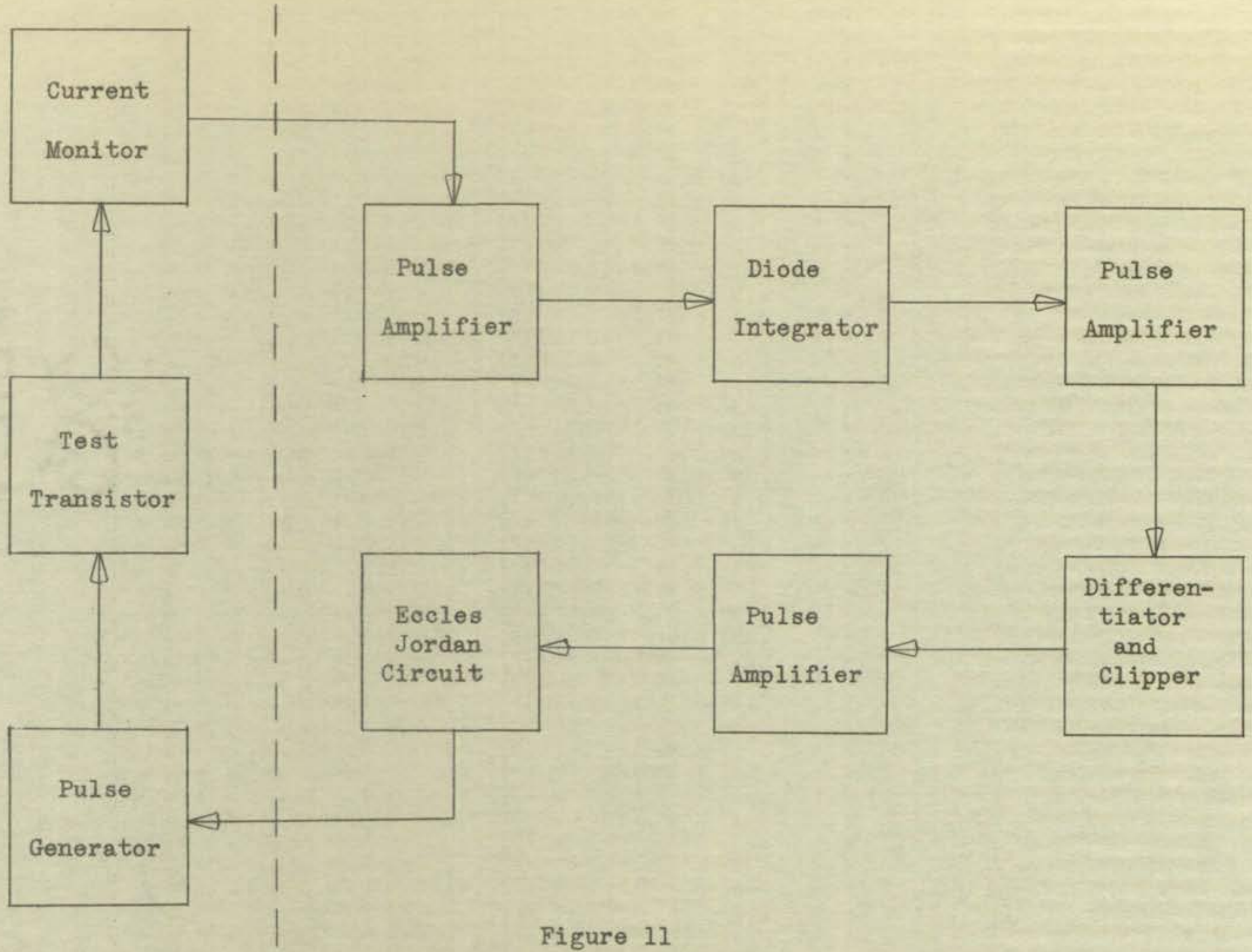

Figure 11

Block Diagram of the Transistor Protection Device

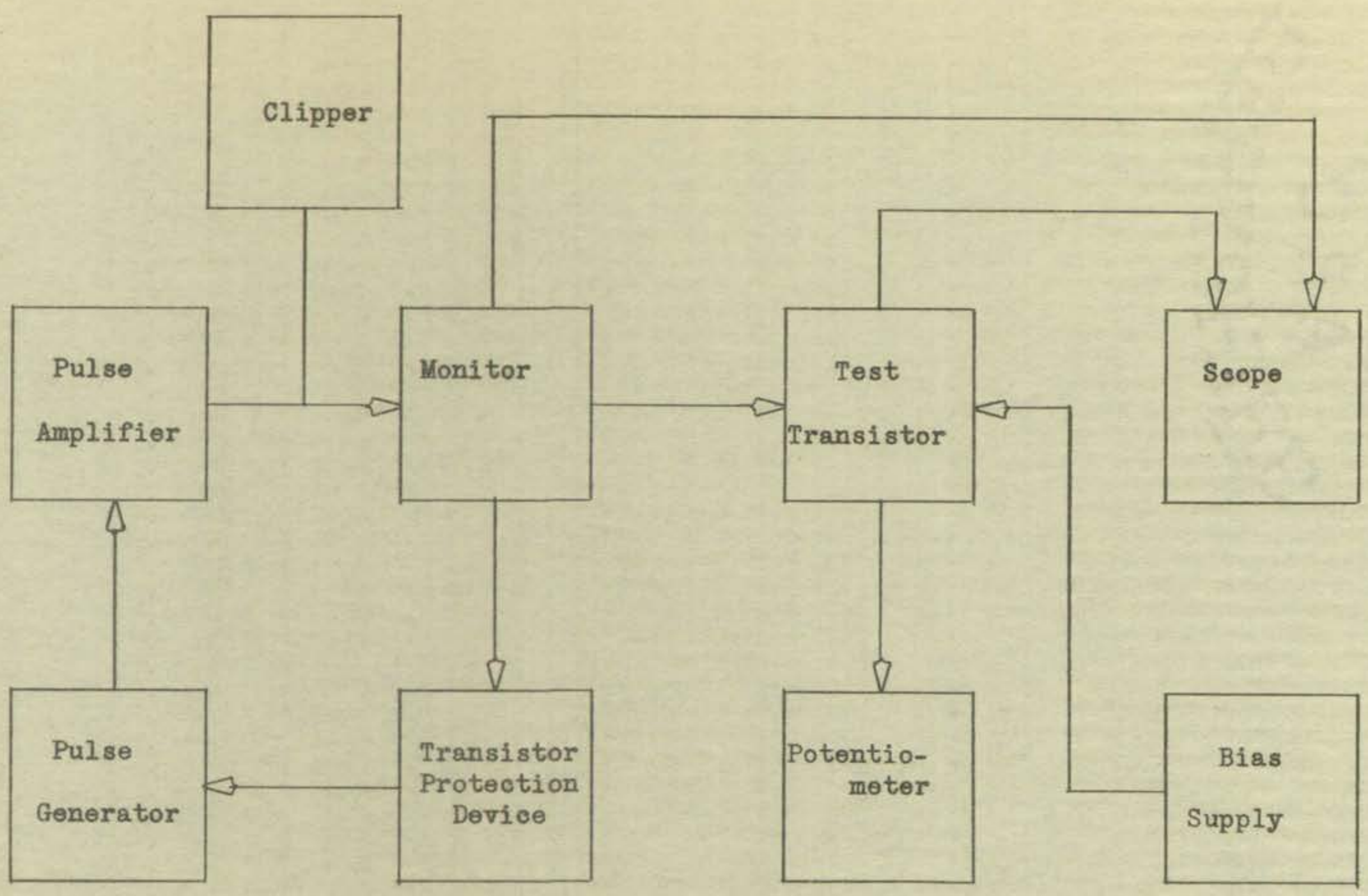

Figure 12

Block Diagram of the Test Set-Up

measured by voltage and current readings on the oscilloscope.

The commercial components of this set-up are described as follows:

Pulse generator: Electro-Pulse, Inc. Model 2120 A.

Oscilloscope: Tektronix, Model 545. Dual trace plug-in unit, Model 53/54C.

The mounting base temperature is measured by means of a thermocouple and a Brown Potentiometer, Model 126 W 2.

3.6 The Variables. For valid results in any experiment, the variables must first be considered carefully. The variables present in our tests are given in Table I below.

TABLE I

VARIABLES PRESENT IN THE FAILURE TESTS

1	T_a	Ambient temperature.
2	T_b	Mounting base temperature.
3	I_c	Collector current
4	V_c	Collector-emitter voltage
5	τ	Period
6	δ	Pulse width
7	I_b	Base current
8	V_b	Base-emitter voltage

It is apparent that some simplifications are needed to reduce the number of variables, or the problem becomes practically impossible.

measured by [illegible]

The [illegible]

follows:

Pulse generator: [illegible]

Oscilloscope: [illegible]

The mounting base [illegible] a Brown Potentiometer, Model [illegible]

3.5 The Variables. [illegible] variables must first [illegible] in our tests are [illegible] in Table [illegible]

TABLE [illegible]

VARIABLES [illegible]

[illegible]

Mounting base temperature [illegible]

[illegible]

It is [illegible]

the number of [illegible]

Therefore, by considering each of them separately, they will be reduced to a reasonable number:

1. Ambient temperature.

   All tests were performed at room temperature (25° Centigrade) and no attempt was made to extend the results experimentally to cover other ambient temperatures.

2. Mounting base temperature.

   This variable was measured and recorded along with other measurements made.

3. and 4. Collector current and collector-emitter voltage.

   These two quantities were lumped together into one and regarded as collector power.

5. Period.

   This is treated as an independent variable.

6. Pulse width.

   This also is an independent variable.

7. and 8. Base current and base-emitter voltage.

   These quantities were recorded, but were later neglected since they contribute very little to the total power dissipation of the transistor.

By using several combinations of values for the independent variables, the power level at failure can be obtained as a function of frequency, pulse width, or duty factor. Table II shows the values and combinations of values used for the independent variables.

TABLE II

THE TEST POINTS

Frequency cps	60	200	600	2000
Pulse	10	10	10	10
width	100	100	100	100
μ sec	1000	1000	1000	

3.7 Test Procedure. The transistor was connected in the circuit shown in Fig. 13, page 28, without a heat sink. The emitter current was adjusted to a fixed value, and the pulse amplitude was then increased in steps until either failure occurred or the peak output of the pulse source was reached. If the latter occurred, the procedure was repeated with a higher value of emitter current. Measurements of all variables were taken at each step, after the mounting base temperature was allowed to stabilize.

Activation of the protection device, described in 3.4, was taken as an indication of failure. To ascertain that the transistor did not suffer any damage in the process of heating, the V_C- I_c characteristics were recorded photographically after each "failure". It was found that the continued operation at high temperatures changes the characteristics and the transistor usually becomes useless after yielding three or four failure points. The method used to obtain the characteristics is described in Appendix A, page 72.

Several failures were recorded at each of the test points of Table II.

[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]

3.7 Test Procedure. [illegible] cult shown in Fig. [illegible] rent was adjusted to a fixed value and the [illegible] increased in [illegible] of the pulp [illegible] grades. [illegible] dure was repeated [illegible] of all variables were [illegible] perature was allowed to stabilize.

Activation of the [illegible] as an indication [illegible] suffer any damage [illegible] were recorded [illegible] the continued [illegible] and the graduation [illegible] failure points. [illegible] cribed in [illegible]

Several [illegible]

Table II.

3.8 The Results. The failure points obtained are indicated on Fig. 14, page 29. It is evident from this figure that there is little variation in average power at failure when the pulse width is varied. The large differences in average power seem to occur when the duty factor is varied. If the average power at failure is plotted as a function of duty factor, the curve of Fig. 15, page 30, is obtained. This curve represents the average value of several failures at each operating point. It is interesting to note that the same curve will be a straight line when plotted on log-log paper. A heat sink added to the mounting base would shift this curve higher, and an increased ambient temperature would shift it lower.

The curve of Fig. 15, page 30, indicates that the failure of the crystal occurs at a certain instantaneous peak temperature and is less dependent on the average temperature. This can be reasoned from the decrease in maximum average power with decreasing duty cycle, because to produce the same average power as at some higher duty cycle, the peak power must be larger, resulting in a higher peak temperature. How this instantaneous temperature varies with time will be shown by analytical methods in the next chapter.

3.8 The Factor [illegible]

on Fig. 14, [illegible]
variation in average [illegible]
The large difference [illegible]
bar is varied, if the average [illegible]
tion of duty [illegible]
curve represents [illegible]
ting point. It is interesting [illegible]
straight line [illegible]
mounting [illegible]
temperature would [illegible]

The dependence of the [illegible]
the crystal [illegible]
less dependent on the average [illegible]
the decrease in [illegible]
because to produce the peak [illegible]
the peak power [illegible]
How this [illegible]
analytical [illegible]

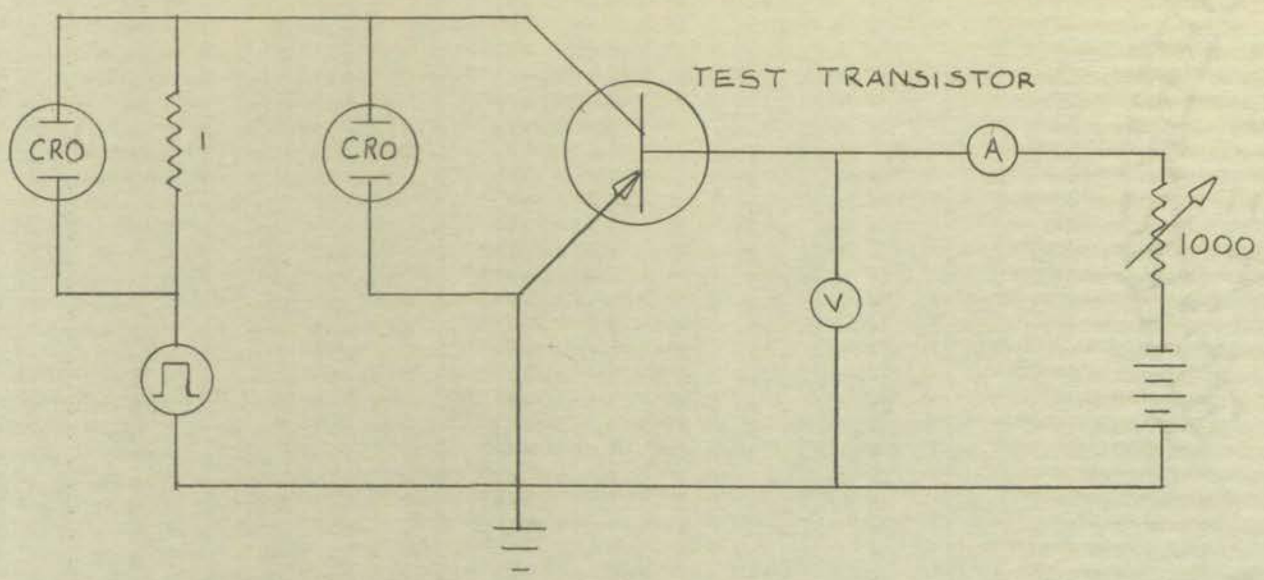

Figure 13

Test Circuit

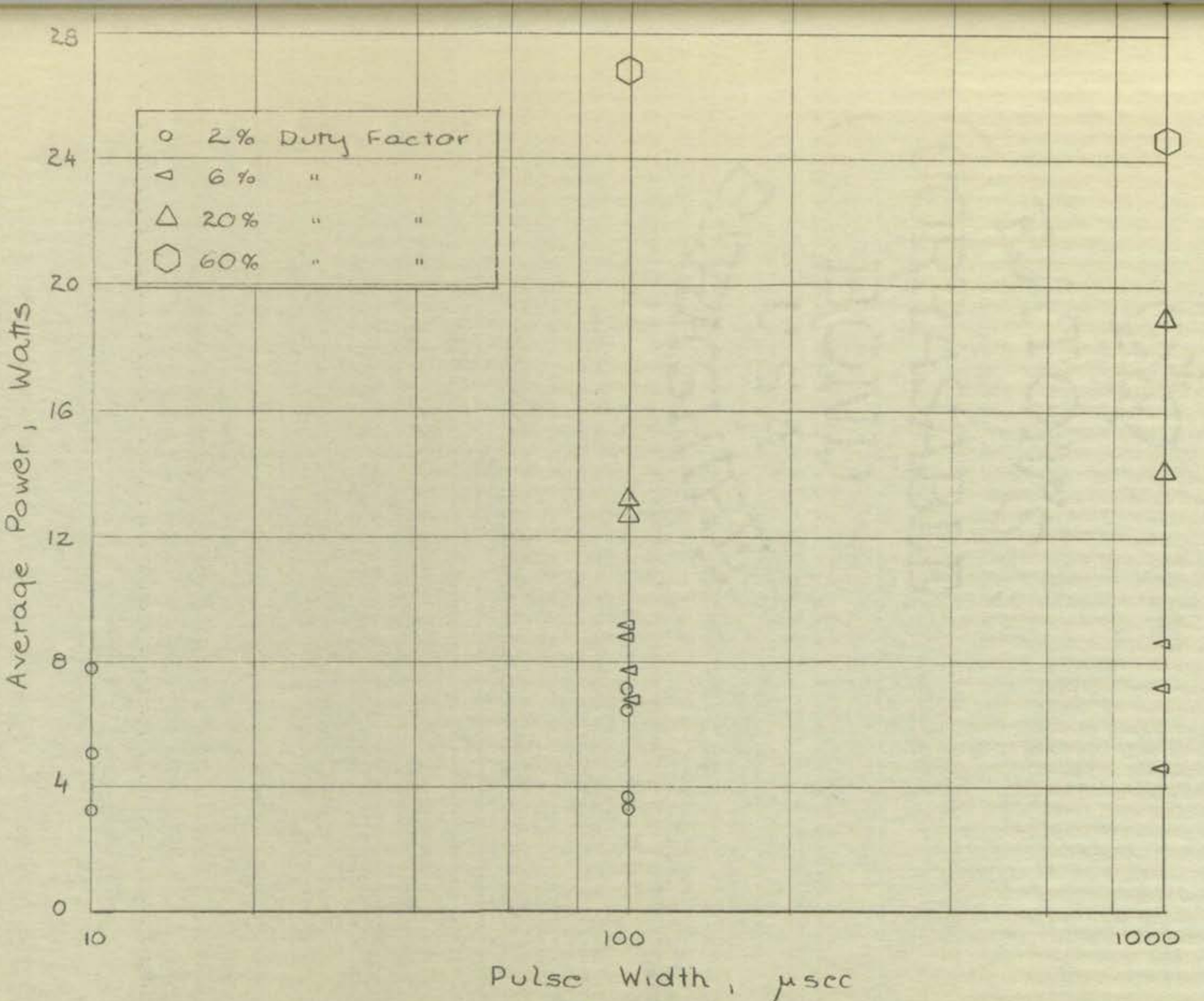

Figure 14

Failure Points

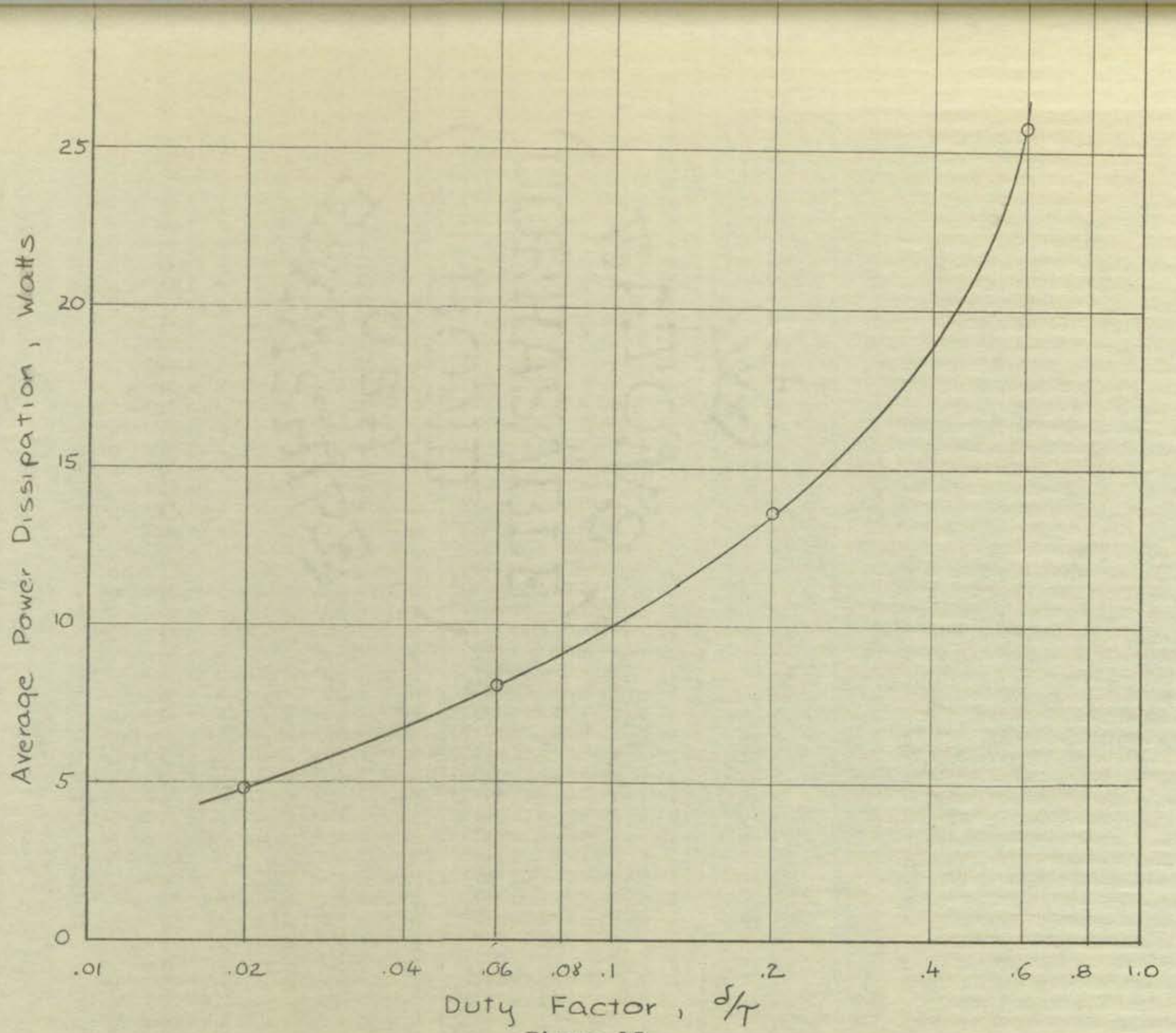

Figure 15

Maximum Average Power vs. Duty Factor

CHAPTER IV

JUNCTION TEMPERATURE CALCULATION

A glance at Fig. 1 on page 7 and Fig. 2 on page 8, showing the crystal crossection and the transistor construction, will reveal that the heat flow picture is not a simple one. The first step, therefore, was to create a thermal model by means of which the heat flow problem can be reduced. The temperatures calculated from this model will be only approximations. Even so, such an analysis may prove valuable if it provides insight into the heat flow characteristics, and it can often reveal ways of improving the device analyzed.

By making several assumptions, the transistor will first be reduced to a thermal model. Then, by means of Fourier analysis, we will develop a method of calculating junction temperature in the crystal for pulsed operation. Finally, the results of the computations will be stated.

4.1 The Thermal Model. To reduce the complex heat flow problem to one which can be more readily solved, the following assumptions are made:

1. Heat transfer occurs by means of conduction only. Considering the crystal alone, it can be said that the heat transfer due to radiation and convection is negligible in comparison to the conduction heat flow into the mounting base.
2. Heat flow is one dimensional. (This follows from the preceeding assumption.)

[illegible]

A glance at [illegible]
crystal preparation and the [illegible]
the heat flow [illegible]
was to create [illegible]
can be reduced. [illegible]
only approximate. [illegible]
it provides insight into the heat flow [illegible]
reveal ways of [illegible]

By making [illegible]
reduced to a [illegible]
develop a method of [illegible]
pulsed operation. Finally, the results [illegible]
stated.

4.1 The Thermal [illegible]
lem to one which [illegible]
are made:

1. Heat transfer [illegible] crystal alone. [illegible] than [illegible] heat flow [illegible]
2. Heat flow [illegible] conditions.

3. The heat is generated uhiformly at a plane between the collector and the emitter. This plane would be represented physically by the base area.
4. The base (Germanium wafer) does not effect heat flow because of its thinness. Actually, the crystal wafer would act as a cooling fin but would not appreciably influence the steady state or average temperatures.
5. No power is dissipated in the emitter and collector regions.

Consequently, our thermal model will consist of a small cylindrical body on top of a larger one, and the heat input occurs uniformly on a plane between the two. This is illustrated in Fig. 16 below.

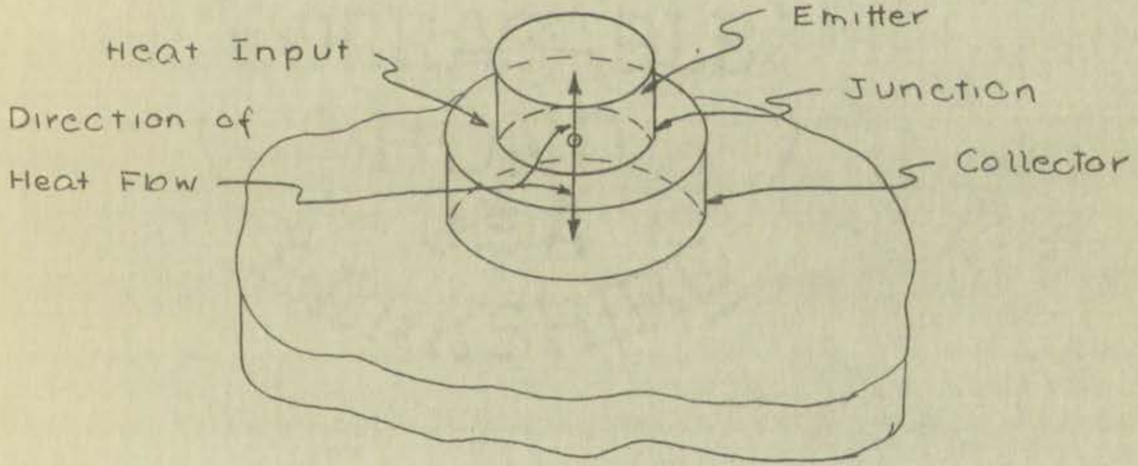

Figure 16

The Thermal Model

4.2 The Steady State Heat Transfer Problem. The steady state one dimensional heat conduction through a solid can be represented by:[1]

$$q = \frac{T_1 - T_2}{\Theta} \qquad (4\text{-}1)$$

where q = heat input in $\frac{cal}{sec}$,

T = temperature, °C, and

Θ = thermal resistance of the path $\frac{^{\circ}C}{cal/sec}$.

When applied to the transistor thermal model, this equation would adequately represent the steady state heat flow if

T_1= junction temperature,

T_2= temperature at the base of the large cylinder,

Θ = thermal resistance of path from junction to base of large cylinder

$q = \frac{\text{input power in watts}}{4.18}$

The emitter region can be neglected from the standpoint of steady state heat flow, since, according to the assumptions of section 4.1, there would be no heat transfer from the emitter region to the surrounding medium. Consequently, the whole cylinder would assume a uniform average temperature equal to the junction temperature.

The heat flowing into the collector cylinder will be dissipated, however, by means of the copper mounting base on which the crystal is resting. Furthermore, heat from the mounting base is rapidly dissi-

---

[1] A. I. Brown and S. M. Marco, Introduction to Heat Transfer, (New York: McGraw-Hill Book Co., Inc., 1951), p. 26.

4.2 The [illegible] Body Carrying Current. The steady state one dimensional heat conduction (Fourier) equation may be represented by:[1]

$$q = \frac{\Delta T}{\Theta} \qquad 4\text{-}1$$

where q = heat input (Btu/hr)

T = temperature, °F, and

Θ = thermal resistance of a body, [illegible]

When applied to the [illegible] the [illegible] adequately represent the [illegible] heat flow and

T_1 = junction temperature

T_2 = temperature at the [illegible]

Θ = thermal resistance of the [illegible] cylinder

q = [illegible]

The [illegible] steady state heat flow [illegible] 4.1, there would be no heat transfer from the [illegible] to the surrounding medium. Consequently, the [illegible] would assume a uniform average temperature equal to the junction temperature.

The heat flowing into the [illegible] cylinder [illegible] however, by means of the [illegible] resting. Furthermore, heat [illegible]

---

[1] A. I. Brown and S. M. Marco, Introduction to Heat Transfer (New York: McGraw-Hill Book Co., Inc., [illegible]

pated into any heat sink, or chassis and ultimately to the surrounding air. This part of the heat flow process is quite complex, however, and our analysis will be limited to the crystal proper.

The above reasoning of the steady state (or d.c.) operation can be carried one step further and applied to the average value of a steady-state periodic operation. This would be the case if the power input (q) would be in the form of a sine function or a recurrent rectangular pulse, applied for sufficient length of time to eliminate transient effects. From this, we can express the average junction temperature for pulsed input as

$$\bar{T}_j = \theta \frac{\bar{P}}{4.18} + T_2 \qquad (4\text{-}2)$$

where $\bar{P}$ is the average power input in watts and T_2 is again the temperature at the base of the collector cylinder. Here the assumption is made that the thermal resistance does not change with the temperature (which will be discussed in detail later).

4.3 <u>The Transient Heat Transfer Problem</u>. In section 3.8 the conclusion was reached that the peak temperature, rather than the average, is responsible for failure in pulsed operation. Consequently, the instantaneous junction temperature is of prime interest.

To derive an expression for this, we need to apply the Fourier heat conduction equation:[2]

---

[2] L. R. Ingersoll, O. J. Zobell and A. C. Ingersoll, Heat Conduction, (Madison: The University of Wisconsin Press, 1954), p. 12.

pated into any instrument [illegible] air. This was a further [illegible] and our analysis [illegible].

The above reasoning of the steady state [illegible] can be carried one step further [illegible] applying to the pulsed [illegible] state periodic operation [illegible] (q) would be in the form of [illegible] pulse, applied for sufficient length of time to [illegible] effects. From [illegible] the average [illegible] for pulsed input as

$$T_0 = \frac{\bar{P}}{\text{[illegible]}} + T$$

where P is the average power [illegible] the temperature at the base of the cylindrical [illegible]. Here the assumption is made that the thermal [illegible] does not change with the temperature (which will be discussed in detail later).

4.3 The Transient and [illegible]. [illegible] conclusion was reached that the heat [illegible], rather than the voltage, is responsible for [illegible] operation. Consequently, the instantaneous junction temperature is of prime interest.

To derive an expression for [illegible] the heat conduction equation[2]

---

[2] [illegible] Conduction [illegible]

$$\frac{\partial T}{\partial t} = \alpha \left[\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2} \right] \tag{4-3}$$

where T = temperature, °C, and

t = time, seconds.

The coefficient α in the above expression represents thermal diffusity in $\frac{\text{cm}^2}{\text{sec}}$ and may be evaluated from:

$$\alpha = \frac{K}{c\rho} \tag{4-4}$$

where k = thermal conductivity, $\frac{\text{cal}}{\text{sec}\ (^\circ\text{C})\ \text{cm}}$,

c = specific heat, $\frac{\text{cal}}{^\circ\text{C gm}}$

ρ = density, $\frac{\text{gm}}{\text{cm}^3}$.

Since we have assumed one dimensional heat flow, equation (4-3) may be written as

$$\frac{\partial T}{\partial t} = \alpha \frac{\partial^2 T}{\partial x^2} \tag{4-5}$$

where x represents the distance from the junction in the direction of heat flow.

4.4 Solution of the Differential Equation for a Sinusoidal Input. If one assumes a semi-infinite slab and applies to its surface a sinusoidal heat source, then the solution of the differential equation (4-5) takes the form:[3,4]

---

[3] P. J. Schneider, Conduction Heat Transfer, (Cambridge, Mass: Adison-Wesley Publishing Company, 1955), p. 277.

[4] The solution to the differential equation is derived in Appendix C page 77.

$$T = T_o e^{-\lambda x} \cos(\omega t - \lambda x) \tag{4-6}$$

where

$$\lambda = \sqrt{\frac{\omega}{2\alpha}} \tag{4-7}$$

This solution presumes that the heat has been applied for a sufficient length of time for the temperatures to reach their steady state periodic values.

To evaluate the coefficient T_o in (4-6) we make use of the conduction equation

$$q = KA \frac{\partial T}{\partial x} \tag{4-8}$$

and the original assumption:

$$q(0, t) = C \cos \omega t \tag{4-9}$$

From (4-6) we get

$$\frac{\partial T}{\partial x} = T_o e^{-\lambda x} \lambda \left[\sin(\omega t - \lambda x) - \cos(\omega t - \lambda x) \right] \tag{4-10}$$

If we let x go to zero:

$$\left.\frac{\partial T}{\partial x}\right|_{x=0} = T_o \lambda \left[\sin \omega t - \cos \omega t \right] \tag{4-11}$$

With the use of the identity

$$\sin \omega t - \cos \omega t = -\sqrt{2} \cos(\omega t + \frac{\pi}{4}) \tag{4-12}$$

(4-11) takes the form

$$\left.\frac{\partial T}{\partial x}\right|_{x=0} = -T_o \lambda \sqrt{2} \cos(\omega t + \frac{\pi}{4}) \tag{4-13}$$

[illegible]

where

[illegible]

This solution [illegible] length of time for the [illegible] periodic values.

To evaluate the coefficients [illegible] conduction equation

[illegible]

and the original [illegible]

[illegible]

From [illegible] we get

[illegible]

If we let x go to zero

[illegible]

With the use of this identity

[illegible]

[illegible] takes the form

[illegible]

From this, a 45 degree phase shift is apparent. Then, if this phase shift is introduced in the solution (4-6), the evaluation of T_o will be more convenient.

Rewriting (4-6):

$$T = T_o e^{-\lambda x} \cos\left(\omega t - \lambda x - \frac{\pi}{4}\right) \qquad (4\text{-}14)$$

This expression still satisfies the differential equation (4-5).

Then

$$\frac{\partial T}{\partial x} = T_o \lambda e^{-\lambda x}\left[\sin\left(\omega t - \lambda x - \frac{\pi}{4}\right) - \cos\left(\omega t - \lambda x - \frac{\pi}{4}\right)\right. \qquad (4\text{-}15)$$

Let x go to zero again:

$$\left.\frac{\partial T}{\partial x}\right|_{x=0} = T_o \lambda \left[\sin\left(\omega t - \frac{\pi}{4}\right) - \cos\left(\omega t - \frac{\pi}{4}\right)\right] \qquad (4\text{-}16)$$

Substituting $\omega t - \frac{\pi}{4} = \beta t$

$$\left.\frac{\partial T}{\partial x}\right|_{x=0} = T_o \lambda \left[\sin \beta t - \cos \beta t\right] \qquad (4\text{-}17)$$

$$\sin \beta t - \cos \beta t = -\sqrt{2}\cos\left(\beta t + \frac{\pi}{4}\right)$$

$$\left.\frac{\partial T}{\partial x}\right|_{x=0} = -\sqrt{2}\, T_o \lambda \cos \omega t \qquad (4\text{-}18)$$

Now from (4-8) and (4-9) we can write:

$$\frac{\partial T}{\partial x} = -\frac{C}{KA}\cos \omega t \qquad (4\text{-}19)$$

Equating coefficients

$$-\sqrt{2}\, T_o \lambda = -\frac{C}{KA} \qquad (4\text{-}20)$$

From this, [illegible]

shaft is introduced [illegible]

be more convenient.

[illegible]

$$T = [illegible]$$

This expression [illegible]

Then

$$\frac{\partial T}{\partial x} = [illegible]$$

Let x go to zero again

$$\left.\frac{\partial T}{\partial x}\right|_{x=0} = [illegible]$$

Substituting [illegible]

$$\left.\frac{\partial T}{\partial x}\right|_{x=0} = [illegible]$$

[illegible]

$$\left.\frac{\partial T}{\partial x}\right|_{x=0} = [illegible]$$

Now from [illegible] and [illegible] we can write

$$\frac{\partial T}{\partial x} = [illegible]$$

Equating coefficients

[illegible]

and

$$T_o = \frac{C}{KA\sqrt{2}\,\lambda} \qquad (4\text{-}21)$$

which is the desired coefficient in (4-14).

To sum it up, for a sinusoidal heat input $q = C \cos\omega t$, the surface temperature of a semi-infinite slab is

$$T(0,t) = \frac{C}{KA\sqrt{2}\,\lambda} \cos\left(\omega t - \frac{\pi}{4}\right) \qquad (4\text{-}22)$$

where C = amplitide of the sinusoidal input, cal/sec,

k = thermal conductivity, $\dfrac{\text{cal}}{\text{sec } ^{o}\text{C cm}}$,

A = surface area, cm^2, and

$\lambda = \sqrt{\dfrac{\omega}{2\alpha}}$

From (4-22) it is also evident that the variation in surface temperature lags 45° behind the input function.

4.5 Derivation of the Instantaneous Junction Temperature.

Any wave shape may be separated into an infinite number of sine and cosine terms by means of a Fourier analysis.[6] If we represent the pulse heat input function by a Fourier series, then (4-22) provides the solution for each of the terms of the series. For the time being, it is assumed that the idea of a semi-infinite slab may be applied to the two Indium cylinders of the transistor. This will be discussed in detail in 4.6.

---

[6] M. E. Van Valkenburg, Network Analysis, (Englewood Cliffs, New Jersey: Prentice-Hall, Inc., 1955), p. 171.

and

[illegible]

which is the [illegible]

To [illegible]

face temperature [illegible]

$T(0,t) = $ [illegible]

where C = [illegible]

K = thermal conductivity [illegible]

A = surface area, and

λ = [illegible]

From (4-22) it is quite evident [illegible] surface temperature lags 45° behind the [illegible]

4.5 [illegible]

Any wave shape may be [illegible] sine terms [illegible] heat input [illegible] Fourier [illegible] tion for each of the [illegible] assumed that [illegible] inline cylinders [illegible] in 4.6.

[illegible] New Jersey: Prentice-Hall [illegible]

Assume the power input of Fig. 17.

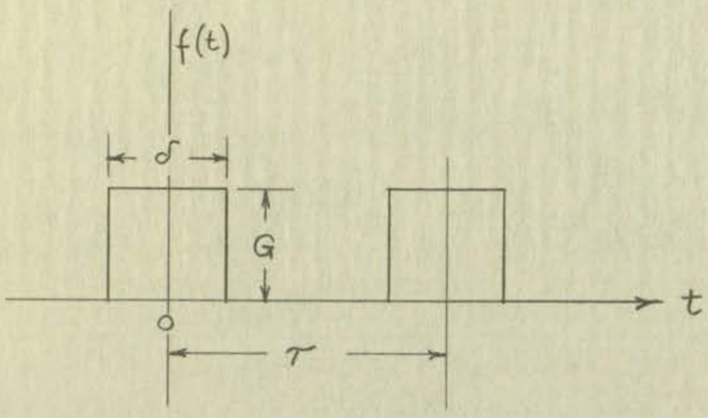

Figure 17

Input Waveshape

$$\begin{aligned} f(t) &= G \quad , \quad \text{for } \left(n\tau - \tfrac{\delta}{2}\right) < t < \left(n\tau + \tfrac{\delta}{2}\right) \\ &= 0 \quad , \quad \text{for } \left(n\tau + \tfrac{\delta}{2}\right) < t < \left[(n+1)\tau - \tfrac{\delta}{2}\right] \\ & \qquad n = 0, 1, 2, \ldots \end{aligned} \qquad (4\text{-}23)$$

By expanding f(t) into a Fourier series, it will be represented as

$$f(t) = A_0 + \sum_{n=1}^{\infty} \left[a_n \cos \omega_n t + c_n \sin \omega_n t\right] \qquad (4\text{-}24)$$

Since f(t) is an even function, no sine terms will be present, consequently

$$f(t) = A_0 + \sum_{n=1}^{\infty} a_n \cos \omega_n t \qquad (4\text{-}25)$$

where $A_0 = \frac{G\delta}{\tau}$, the time average of f(t), and

$$\begin{aligned} a_n &= \frac{4}{\tau} \int_0^{\delta/2} f(t) \cos \omega_n t \, dt \\ &= \frac{4G}{\tau\omega} \sin \omega_n \delta/2 \end{aligned} \qquad (4\text{-}26)$$

Since $\omega = \frac{2\pi n}{\tau}$, this can be written as

$$a_n = \frac{2G}{\pi n} \sin \pi n \frac{\delta}{\tau}$$

Rewriting (4-25) we get

$$f(t) = A_o + \sum_{n=1}^{\infty} \frac{2G}{\pi n} \sin \frac{\pi n \delta}{\tau} \cos \frac{2\pi n t}{\tau} \qquad (4\text{-}27)$$

For the temperature at x = 0, we have

$$h(t) = B_o + \sum_{n=1}^{\infty} b_n \cos\left(\omega_n t - \frac{\pi}{4}\right) \qquad (4\text{-}28)$$

where B_o is the average junction temperature of the transistor. This is evaluated by the use of (4-2)

$$\bar{T}_j = \frac{\hat{P}}{4.18} \cdot \frac{\delta}{\tau} \, \theta + T_2$$

b_n is the amplitude of the cosine function of (4-22), or

$$b_n = \frac{C}{\sqrt{2}\, K A \lambda}$$

C is the amplitude of the heat input function in (4-9), or simply a_n in (4-25), and we can write:

$$b_n = \frac{a_n}{\sqrt{2}\, K A \lambda}$$

$$= \frac{2G}{\pi n} \sin \frac{\pi n \delta}{\tau} \cdot \frac{1}{\sqrt{2}\, K A \lambda} \qquad (4\text{-}29)$$

Using

$$\lambda = \sqrt{\frac{\omega_n}{2\alpha}} \qquad \text{and} \qquad \omega_n = \frac{2\pi n}{\tau}$$

we write

$$b_n = \frac{G}{n^{3/2}} \frac{\sqrt{2\alpha\tau}}{K A \pi^{3/2}} \sin \pi n \frac{\delta}{\tau} \qquad (4\text{-}30)$$

Since [illegible], there can be written as

$Q_n =$ [illegible]

Rewriting [illegible] we get

$f(s) =$ [illegible]

For the temperature at [illegible] we have

$h(t) =$ [illegible]

where h_0 is the [illegible] temperature [illegible]

is evaluated by the [illegible]

$T_1 =$ [illegible]

b_n is the [illegible]

$b_n =$ [illegible]

C is the [illegible] coefficient [illegible]

a_n in (4-35), and [illegible]

$b_n =$ [illegible]

Using

$\lambda =$ [illegible]

we write

$b_n =$ [illegible]

The instantaneous junction temperature is then completely represented by:

$$h(t) = B_0 + \sum \frac{G}{n^{3/2}} \frac{\sqrt{2\alpha T}}{KA\,\pi^{3/2}} \sin \pi n \frac{\delta}{T} \cos\left(\frac{2\pi n t}{T} - \frac{\pi}{4}\right) \qquad (4\text{-}31)$$

The area A in the above expression is the sum of the collector and emitter junction areas.

4.6 Justification of the Semi-Infinite Slab Approach. If heat is applied to the surface of a body for a short period of time, the heat will produce temperature changes only a short distance beyond the surface. Making use of a method described by McAdams[7] we will calculate this distance for the transistor and show that temperature changes at the junction will not influence the temperatures at the opposite ends of the emitter or collector cylinder.

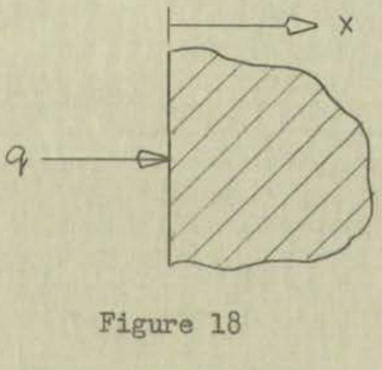

Figure 18

Semi-Infinite Slab

Assuming the semi-infinite slab of Fig. 18, we define the following quantities:

---

[7] W. H. McAdams, Heat Transmission, (New York: McGraw-Hill Book Co., Inc., 1954), p. 39.

$$Y = \frac{T_A - T_x}{T_A - T_B}$$

where T_A = temperature applied at the surface, °C,

T_B = original uniform temperature of the slab, °C,

T_x = temperature at x, °C.

$$Z = \frac{x}{2\sqrt{\alpha \Delta t}}$$

where x = distance, cm,

α = thermal diffusivity of material, $\frac{cm^2}{sec}$,

Δt = time of temperature change, sec.

$$m = \frac{k}{hx} ,$$

where h = coefficient of heat transfer between surroundings and surface. For a value of $h = \infty$ or $m = 0$, the relation between Y and Z is given by the error integral

$$Y = \frac{2}{\sqrt{\pi}} \int_0^Z e^{-Z^2} dZ \qquad (4\text{-}32)$$

Now let us assume certain conditions and for a given temperature change evaluate the distance x from the junction of the transistor into the Indium region.

If $T_A = 100$ °C, $T_B = 0$, $T_x = 10$ °C

$$Y = \frac{100 - 10}{100} = 0.9$$

$Z = 1.2$, from (4-32).

For Indium $\alpha = 0.137 \frac{cm^2}{sec}$. If the heat is applied for a period of 8.35 msec, (as in 60 cps. 50% d.f. operation), then x = 0.0811 cm. The collector and the emitter cylinders are each approximately 0.127 cm. high, which is approximately 50% more than the value computed for x.

where T_A = [illegible]

T_S = [illegible] temperature of the [illegible], °C

T_x = temperature [illegible]

where x = distance, cm

α = thermal diffusivity, [illegible], cm²/sec

Δt = time of [illegible], sec

where h = coefficient of heat transfer, [illegible]

For a value of h [illegible], the [illegible]

the error integral.

Now let us [illegible] conditions [illegible] temperature

change evaluate the [illegible] time [illegible]

the Indium region:

If T_x = 150 °C, T_S = [illegible]

[illegible]

[illegible]

For Indium α = 0.37 [illegible]. If the heat [illegible]

8.35 msec, [illegible]

The collector [illegible]

high, which is approximately [illegible]

Evidently, the cycling of the junction temperature will not be felt at the extreme ends of the emitter and collector regions, and they can therefore be considered as semi-infinite slabs. This will not hold true, of course, if the heat is applied at a frequency much lower than the 60 cycles used in the computation above.

It is interesting to note that the temperature variation will gradually become a sinusoid of decreasing amplitude as it is observed at an increasing distance from the surface, moving into the slab.[8] The reason for this is the faster attenuation with distance of higher frequency harmonics.

4.7 Calculation of Junction Temperature. If one considers the infinite series part of equation (4-31) alone,

$$h'(t) = \sum_{n=1}^{\infty} \frac{G}{n^{3/2}} \sqrt{T} \frac{\sqrt{2\alpha}}{KA\pi^{3/2}} \sin \pi n \frac{\bar{\sigma}}{T} \cos\left(\frac{2\pi n t}{T} - \frac{\pi}{4}\right) \qquad (4\text{-}33)$$

valuable insight may be gained into how the instantaneous junction temperature depends on the variables involved. It is interesting to note that it varies directly proportional with the area and $\sqrt{T}$ if $\frac{\bar{\sigma}}{T}$ is constant, but inversely proportional with $\sqrt{K}$. It is also directly proportional to the amplitude of the applied pulse, as would be expected.

Let us adopt the following notation

$$h'(t) = H D \sqrt{T} \qquad (4\text{-}34)$$

$$D = \frac{\sqrt{2}\,\alpha}{KA\ \pi^{3/2}} \qquad (4\text{-}35)$$

---

[8] H. S. Carslaw and J. C. Jaeger, Conduction of Heat in Solids, (Oxford: Oxford University Press, 1947), p. 50.

Evidently, the results of the [illegible] at the surface ends of the [illegible] can therefore be considered [illegible] 4.7, [illegible] true, of course, [illegible] the 60 cycle [illegible] in the [illegible].

It is [illegible] gradually [illegible] as an increasing distance from [illegible] reason for this [illegible] quency [illegible].

4.4 [illegible] Random [illegible]

Infinite series [illegible]

[illegible]

valuable [illegible] perature [illegible] that [illegible] constant, but [illegible] particular [illegible]

Let us [illegible]

[illegible]

[illegible] (Oxford: [illegible])

$$H = \sum_{n=1}^{\infty} \frac{U}{n^{3/2}} \cancel{\left(\sqrt{T} \quad \frac{\sqrt{2\alpha}}{KA\,\pi^{3/2}} \right)} \sin \pi n \frac{\delta}{T} \cos\left(\frac{2\pi n t}{T} - \frac{\pi}{4} \right) \qquad (4\text{-}36)$$

where we let $G = U = 1$.

A good comparison of the relative junction temperatures under different pulsed conditions may be obtained from Fig. 19, page 45, which contains several plots of H, all curves representing a unit average power input, $\left(U\frac{\delta}{T} = 1\right)$, but different duty factors. The term B_o in equation (4-31) is dependent upon the resistance of thermal path alone, and should be considered independently. It should be mentioned here that the series of (4-33) converges quite slowly for small values of $\frac{\delta}{T}$ and more than 30 harmonics were needed to evaluate some of the curves of Fig. 19.

It can be seen from Fig. 19 that the peak temperature increases rapidly with decreasing duty factor $\frac{\delta}{T}$. A plot of the variation of H_{max} against duty factor for a unit average power input, is given in Fig. 20, page 46.

To find the junction temperature of a transistor, the constants of D need to be evaluated first. Indium has the following properties:

$H = \sum_{n=1} \frac{2\pi}{\ldots}$ [illegible]

where we let [illegible]

A good [illegible] several

different points [illegible]

which contains [illegible]

power [illegible]

equation [illegible] are dependent [illegible] of the [illegible]

and should be considered [illegible]

that the [illegible]

[illegible] and more than [illegible] were [illegible]

curves of Fig. 19.

It can be seen that [illegible] increases

rapidly with decreasing [illegible]

of H_{max} against duty factor [illegible]

Fig. 20, page 85.

To find the [illegible]

of D need to be [illegible]

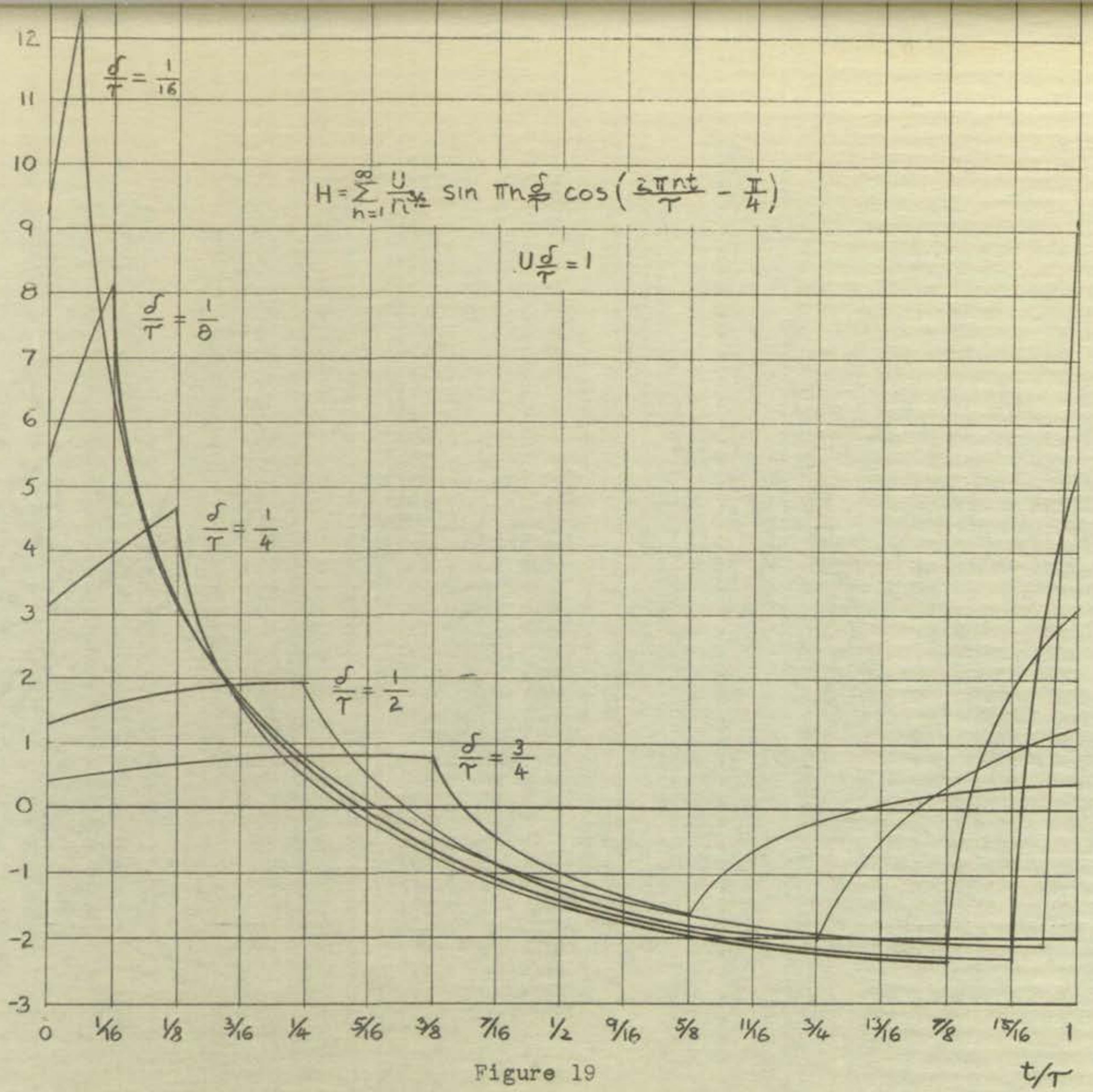

Figure 19

Relative Junction Temperature Variation Under Pulsed Excitation

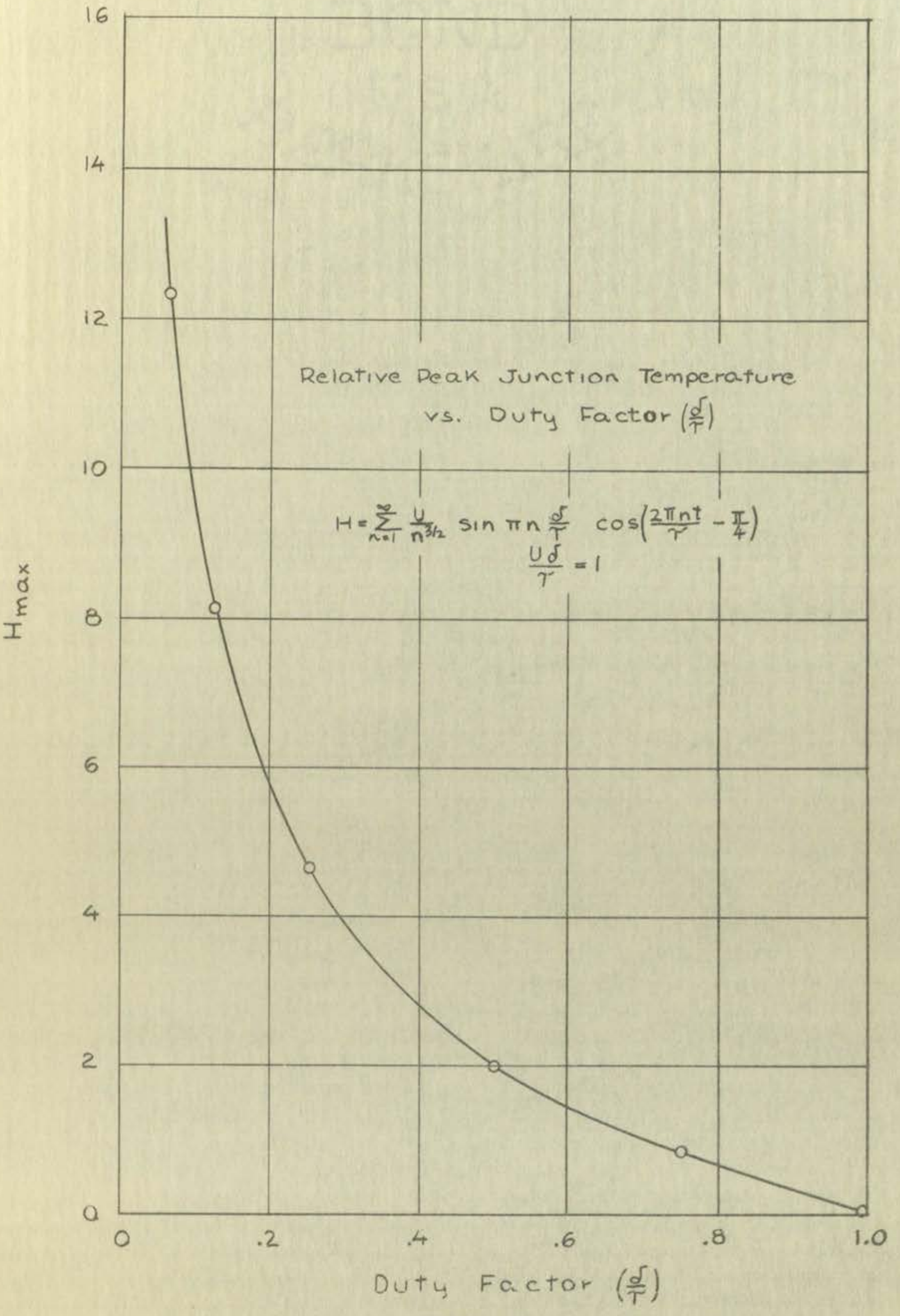
16
14
12
10
8
6
4
2
0
Hmax
Relative Peak Junction Temperature
vs. Duty Factor $(\frac{\delta}{\tau})$
$H = \sum_{n=1}^{\infty} \frac{U}{n^{3/2}} \sin \pi n \frac{\delta}{\tau} \cos\left(\frac{2\pi n t}{\tau} - \frac{\pi}{4}\right)$
$\frac{U\delta}{\tau} = 1$
0
.2
.4
.6
.8
1.0
Duty Factor $(\frac{\delta}{\tau})$

Figure 20

TABLE III

PROPERTIES OF INDIUM

Symbol	Name	Value	Unit
k	thermal conductivity[9]	0.057	$\frac{cal}{^{\circ}C\ sec\ cm}$
ρ	density[10]	7.28	$\frac{gm}{cm^3}$
c	specific heat[11]	0.057	$\frac{cal}{^{\circ}C\ gm}$
α	thermal diffusivity[12]	0.1373	$\frac{cm^2}{sec}$

Knowing these values and the total junction area (emitter and collector), the coefficient D is readily available. The use of the above value for thermal conductivity of pure Indium at room temperature may be a source of error, because k is known to vary with temperature and impurity in the metal. No data are available on the amount of variation, however. Considering that several other assumptions were made on the thermal model, the error due to variation in k is, in all probability, small in comparison.

To compute the actual peak junction temperature of a transistor, for a peak power input P_1 watts, pulse width δ_1 seconds, and period T_1 seconds, one would first consider:

---

[9] M. T. Ludwick, Indium, (New York: The Indium Corporation of America, 1950), p. 14.

[10] Handbook of Chemistry and Physics, 26th Edition, (Cleveland: Chemical Rubber Publishing Company, 1942), p. 1601.

[11] Ibid., p. 1672.

[12] $\alpha = \frac{k}{c\rho}$

TABLE [illegible]

[illegible] PROPERTIES [illegible]

Symbol	Name	[illegible]	[illegible]
k	thermal conductivity	[illegible]	[illegible]
ρ	density[10]	[illegible]	[illegible]
c	specific heat	[illegible]	[illegible]
τ	thermal [illegible]	[illegible]	[illegible]

Knowing these values and [illegible] (see [illegible] tor), the coefficient [illegible] value for thermal conductivity [illegible] a source of error, [illegible] purity in the metal. [illegible] however. Considering [illegible] thermal model, [illegible] small in comparison.

To compute the [illegible] for a peak power [illegible] seconds, one [illegible]

---

9 [illegible] America, 195[illegible], p. [illegible]

10 Handbook of [illegible] Land: [illegible]

11 [illegible]

12 [illegible]

$$T_{j_{max}} = \overline{T}_j + \Delta T_{max} \tag{4-37}$$

where $\overline{T}_j = \overline{P}_1\theta_a + T_a$, (4-38)

$\overline{P}_1 = \widehat{P}_1 \frac{\delta}{\tau}$, (4-39)

θ_a = thermal resistance from junction to ambient,

T_a = ambient temperature,

$\overline{T}_j$ = is actually the term B in (4-31)

ΔT_{max} is the peak temperature difference between $T_{j_{max}}$ and T_j, and may be found from the plot of H_{max} in Fig. 20, page 46, by reading H_{max} for $\frac{\delta_1}{\tau_1}$ and then

$$\Delta T_{max} = H_{max}\, D\, \frac{\overline{P}_1}{4.18}\, \sqrt{\tau_1} \tag{4-40}$$

The input power in watts is converted to $\frac{\text{calories}}{\text{sec}}$ by means of the $\frac{1}{4.18}$ conversion factor, and is multiplied by the value found for H_{max} since the latter represents unity power input.

Sometimes it is necessary to use (4-34) in a different form, depending on the value of thermal resistance given. If, for example, the resistance of the path from the junction to the mounting base, θ_b, is being considered, then

$$\overline{T}_j = \overline{P}_1\theta_b + T_b \tag{4-41}$$

where T_b is now the mounting base temperature. Several examples of junction temperature computations will be given in Chapter VI.

where T_j = [illegible]

T_i = [illegible]

θ_a = thermal resistance [illegible]

T_a = ambient temperature [illegible]

T_j = is actually the [illegible]

ΔT_{max} is the [illegible] T_{max} [illegible]

may be found from the [illegible]

for [illegible] and then

$$\Delta T_{max}$$ [illegible]

The input power in watts [illegible]

[illegible] conversion factor, [illegible]

since the latter [illegible]

Sometimes it is [illegible]

depending on the [illegible]

the resistance of the [illegible]

is being considered, then

[illegible]

where T_j is now the [illegible]

junction temperature [illegible]

CHAPTER V

THERMAL RESISTANCE AND ITS MEASUREMENT

The heat generated at the junction of the transistor is ultimately dissipated into whatever medium surrounds the transistor - usually air. The thermal circuit offers a resistance to the heat flow very much like the resistance to current in an electrical circuit. This resistance is an important factor in the determination of the average junction temperature.

Because of its importance, the thermal resistance will be discussed here in detail. Methods for its calculation and experimental evaluation will be given. Most of this work applies to the geometry and construction of the Clevite CTP-1003 transistor only. However, the experimental evaluation of thermal resistance may be applied to most transistors.

5.1 The Thermal Path and Its Elements.

Heat flows normally from a point of high temperature to a point of low temperature. In the case of the transistor, this may be stated as heat flow from the junction to the surrounding air. The resistance of the heat flow path determines the total difference in temperature between these two points which will be present for a given amount of heat input. This may be stated as:

$$q = \frac{\Delta T}{\theta} \qquad (5\text{-}1)$$

where q = rate of heat flow, $\frac{\text{cal}}{\text{sec}}$, and

Θ = thermal resistance, $\frac{^{o}\text{C}}{\text{cal/sec}}$.

[illegible]

The [illegible] mately [illegible] air. The [illegible] like the [illegible] tance is an [illegible] temperature.

Because [illegible] evaluation [illegible] construction [illegible] permanent [illegible] transistors.

5.1 The [illegible] a [illegible] of the [illegible] the [illegible] the total [illegible] be present [illegible]

where q [illegible]

Since $\Delta T = T_j - T_a$

T_j = junction temperature, and

T_a = ambient temperature,

the value of Θ determines T_j in steady state operation.

To analyze the thermal path, it is convenient to use an electric circuit analogy.[1] The thermal path and its components are illustrated in Fig. 21, page 51, and the equivalent electric circuit in Fig. 22. From these figures it is evident that resistances represent the following parts of the thermal circuit:

R_1 - the path from junction through collector disc,

R_2 - from collector disc to lower surface of mounting base,

R_3 - from the connection between mounting base and heat sink to surface of heat sink

R_4 - from surface of heat sink to ambient,

R_5 - small heat losses from the transistor case.

To complete the analogy, I represents the heat flow and V the thermal drop across the path.

The circuit of Fig. 22 may be simplified by the following reasoning: R_2 is much smaller than R_1, and will therefore be neglected. R_5 is much larger than $R_2 + R_3 + R_4$, its parallel path and may also be

---

[1] L.A. Griffith, "Power Transistor Temperature Rating," Paper presented to the Aircraft Electrical Society, (Minneapolis-Honeywell Regulator Company, 1955).

Since $\Delta T = T_j - T_a$,

T_j - junction temperature [illegible]

T_a - ambient temperature [illegible]

the value of θ [illegible]

To analyze the [illegible]

tric circuit analog [illegible]

trated in Figs. [illegible]

Fig. 22. From [illegible]

the following [illegible]

R_1 - the [illegible]

R_2 - from collector [illegible]

R_3 - from the [illegible]

to surface of heat sink

R_4 - from surface of [illegible]

R_5 - [illegible]

To complete the analogy, [illegible]

drop across the path.

The circuit of Fig. 22 can be simplified [illegible]

ing: R_5 is much smaller than [illegible]

is much larger than [illegible]

---

[1] J.R. Griffith, [illegible] presented to the [illegible] Regulator Company, [illegible]

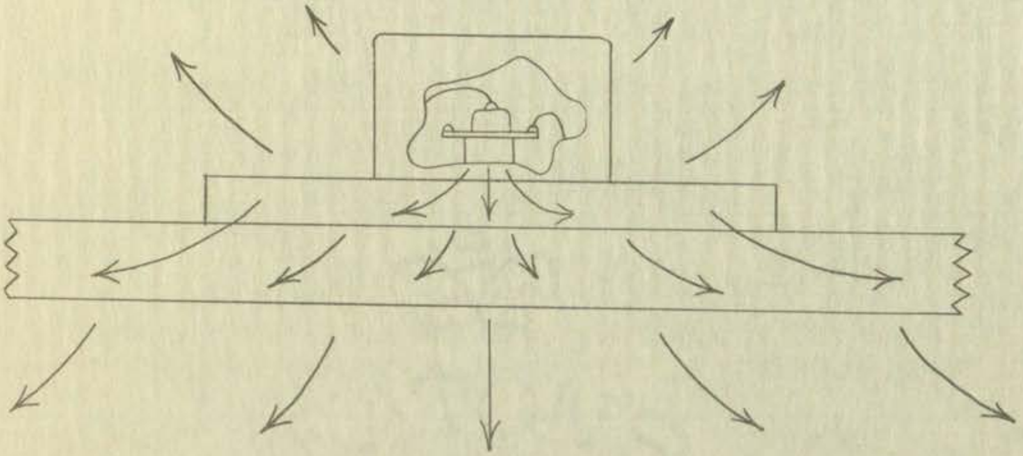

Figure 21

Heat Flow Path of the Transistor

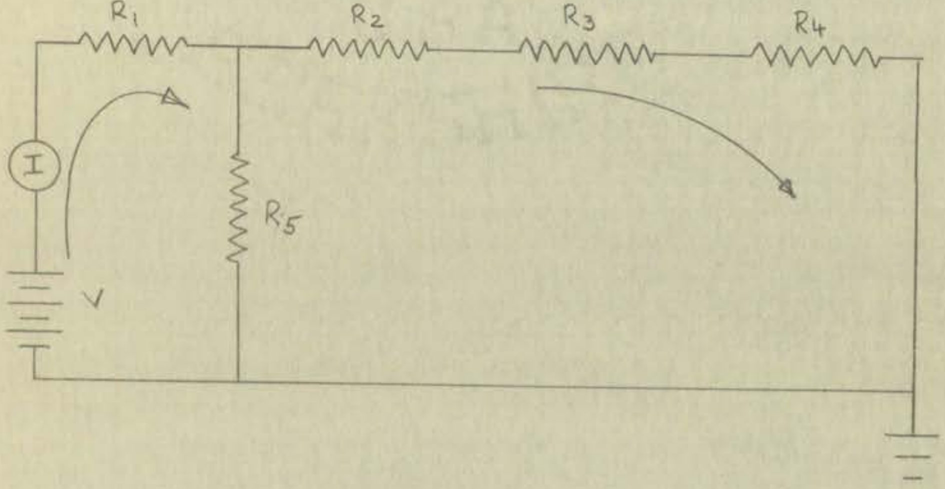

Figure 22

Electric Circuit Representing Heat Flow in the Transistor

neglected. R_3 is again very small compared to R_4 and may be neglected.[2] Thus the only resistances left in the circuit are R_1 and R_4, as shown in Fig. 23, and their approximate values may be calculated.

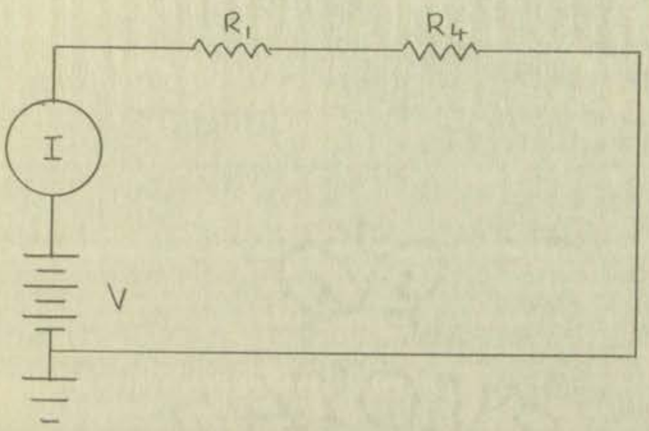

Figure 23

Simplified Circuit Representing Heat Flow

5.2 Calculation of Thermal Resistance. The two main components of the total thermal resistance can be calculated if the physical dimensions of the transistor crystal are available.

5.2(a) R_1 - Resistance of the Collector Disc. The heat flows from the junction to the mounting base through a small Indium disc. The resistance offered by this disc to conduction heat transfer may be determined from its dimensions and its thermal conductivity.

Using the dimensions of Fig. 2, page 8:

$$R_1 = \frac{\text{height}}{\text{k x Area}} = 19.7 \frac{^{o}\text{C}}{\text{cal/sec}} = 4.71\ ^{o}\text{C/watt}$$

---

[2] R_2 and R_3 will be neglected for the purposes of thermal resistance calculations. They are actually lumped together with R_1 and R_4 respectively in the experimental evaluation of the latter two.

5.2(b) R_4 - *Resistance of the Heat Sink Surface*. The heat transfer from the heat sink to the air is accomplished in all three possible ways: conduction, convection and radiation. It is evidently a much more complex process than that described in the preceding section. The heat transfer can still be represented by the expression of (5-1). However, $1/\Theta$ in this case stands for an overall coefficient of heat transfer, and it is no longer a constant value.

If the heat transfer due to radiation is neglected, the value of the surface coefficient may be approximated by the use of formulas found in the literature of heat transfer. According to Brown and Marco[3], for a plane surface

$$\frac{1}{\Theta'} = C\,\frac{k}{L}\,(aL^3\ T)^{\frac{1}{4}} \qquad \frac{BTU}{ft^2\ hr\ (^\circ F)} \tag{5-2}$$

where $\frac{1}{\Theta'}$ = surface coefficient of heat transfer, free convection,

C = tabulated constants,

k = conductivity of surrounding air,

L = height of plane surface, and

a = tabulated constant for air.

All variables in the above expression must be expressed in engineering units.

Using the above equation and converting to the CGS system of units, the value of Θ' is found to be $6.6\ \frac{^\circ C}{Watt}$ for a vertical plate

---

[3] A. I. Brown and S. M. Marco, *Introduction to Heat Transfer*, (New York: McGraw-Hill Book, Company, Inc., 1951), p. 135.

[illegible] Calculation of the Horizontal Surface. The heat

transfer from the [illegible] plate [illegible] coefficient [illegible] possible [illegible] a much more complex [illegible] than that [illegible] tion. The heat transfer [illegible] of (5-41). However, [illegible] heat transfer [illegible] value.

If the heat transfer [illegible] of the surface coefficients [illegible] found in the literature [illegible] heat [illegible] for a plane surface

[illegible]

Where $\frac{1}{GF}$ = [illegible]

C = [illegible]

k = conductivity of [illegible]

L = height of [illegible]

a = [illegible]

All variations of the [illegible] units.

Using the above [illegible] units, the value of [illegible] vertical [illegible]

---

1 [illegible] (New York: [illegible] Book Company, [illegible]

6" x 6", at 100 °C in air at 25 °C.

5.3 Measurement of Thermal Resistance. The total resistance of the thermal path may be measured by experimental methods. For convenience it may also be separated into two parts which can be measured independently.

5.3(a) Resistance from Junction to Mounting Base. To find R_1 of Fig. 22, an indirect method must be used to measure the temperature at the junction, since it is not directly accessible. In section 2.2 it was brought out that the saturation current of the junction is a logarithmic function of temperature. By measuring the collector leakage current of the transistor, with emitter open, the temperature of the junction may be established. The leakage current may be calibrated by first placing the transistor in an oven and varying its temperature. Then if the junction temperature of the operating transistor is desired for a given power input, the emitter current is interrupted for a short time and the collector current can be measured during this period. The circuit of Fig. 24, page 57 is only slightly modified from the one used by Reich[4] and Hood[5].

To find thermal resistance between the junction and the mounting base, it is only necessary to measure the difference in temperature between the two points for a given power input. Results of such measure-

---

[4] B. Reich, "Transistor Thermal Resistance Measurement," Electronic Design, IV (December 1, 1956), p. 20.

[5] J. A. Hood, "Thermal Paths of Power Transistors," Unpublished Report, (Sandia Corporation, Albuquerque, August, 1956).

δ^n or 0^n, [illegible]

5.3 Measurement [illegible] total resistance of the channel [illegible] it may [illegible] independently.

5.4 [illegible]

of Fig. 22, an inductance method may be used to measure the [illegible] at the junction, [illegible] it was [illegible] particular [illegible] current of the [illegible] junction may be calculated. [illegible] first [illegible] if the junction [illegible] given power input, the [illegible] current [illegible] and the [illegible] cuts of Fig. [illegible] Welch and [illegible]

[illegible] base, it is only necessary [illegible] tween the two points [illegible]

[illegible] Electronic [illegible]

Report, [illegible]

ments using the circuit of Fig. 24, are given in Fig. 25, page 8. The temperature of the mounting base was measured with a thermocouple.

The slope of the line of Fig. 25, indicates a thermal resistance of 2.7 °C/Watt for the CTP-1003, as compared to 2.4 °C/Watt given by the manufacturer. The fact that these values are much smaller than the value computed in section 5.2(a) leads us to believe that the value used for thermal conductivity is too low.

5.3(b) Resistance from Mounting Base to Surrounding Air. The computation of this thermal resistance as outlined in section 5.2(b) does not yield very satisfactory results. The shape of the heat sink may be irregular; forced convection may be present. Because of these and other factors which might be present, it is thought that this type of resistance should be measured directly rather than calculated if needed for design purposes. The circuit of Fig. 26, page 59, indicates the simplicity of making such measurements.

Temperature difference vs. power curves for heat sinks of various sizes are given in Fig. 27, page 60. The thermal resistances are determined by the slopes of these curves and are tabulated below.

TABLE IV

HEAT SINK THERMAL RESISTANCES

Heat Sink Inches	Thermal Resistance °C/Watt
None	13.8
3 x 3	6.25
$4\frac{1}{4}$ x $4\frac{1}{4}$	4.2
6 x 6	3.2

mathe using [illegible] of [illegible] surface [illegible]

temperature of [illegible] by [illegible]

[illegible]

of 3.7 °C/watt for the [illegible]

the [illegible] value [illegible]

value computed [illegible] therefore [illegible] that [illegible]

for thermal [illegible]

[illegible]

The computation of this thermal resistance [illegible]

does not give very satisfactory results [illegible]

may be [illegible]

other factors [illegible]

resistance should be [illegible]

for design [illegible]

simplicity of [illegible]

Temperature [illegible]

sizes are given in [illegible] thermal resistance [illegible]

determined [illegible]

TABLE [illegible]

[illegible]

The material used for the heat sinks was smooth, polished aluminum plate, .064 inches thick. The temperature was measured with a thermocouple clamped between the mounting base and the heat sink.

Using a 6" x 6" plate, a comparison of the measured thermal resistance with the computed value in 5.2(b) reveals that the computed value is much higher than the actual measurement. Consequently, the method of section 5.2(b) is not recommended unless only approximate values are desired for rough calculations.

The material used for the determination [illegible]

.064 inches thick. [illegible]

clamped between the [illegible]

Using [illegible]

resistance with [illegible]

value is much higher than [illegible]

method of Section [illegible]

values are [illegible]

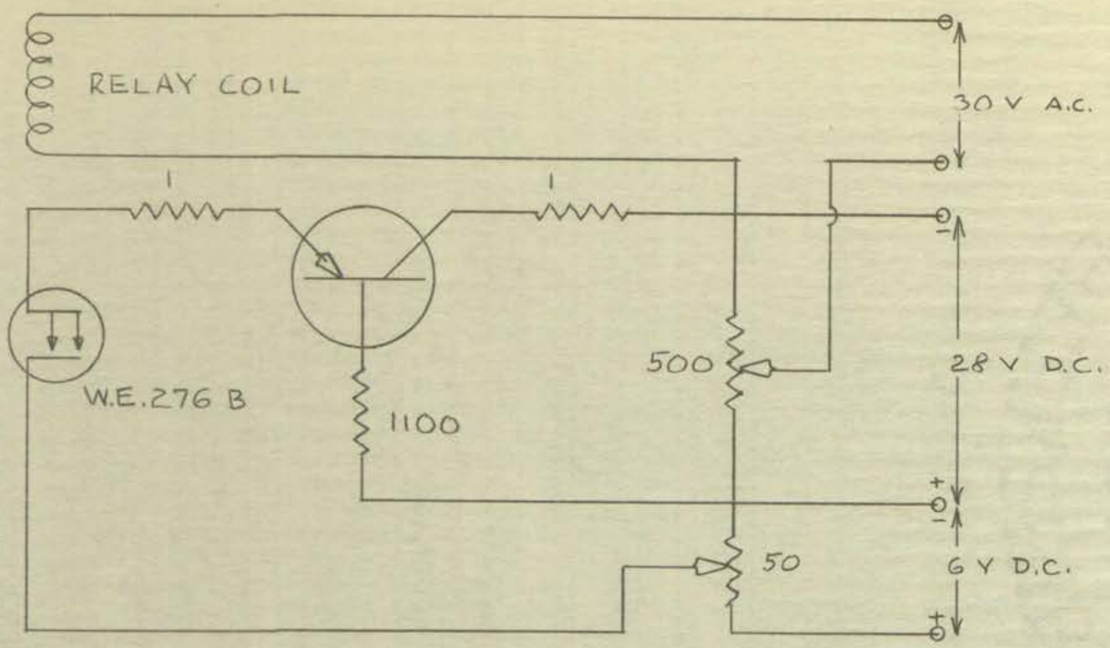

Figure 24

Circuit for Junction Temperature Measurement

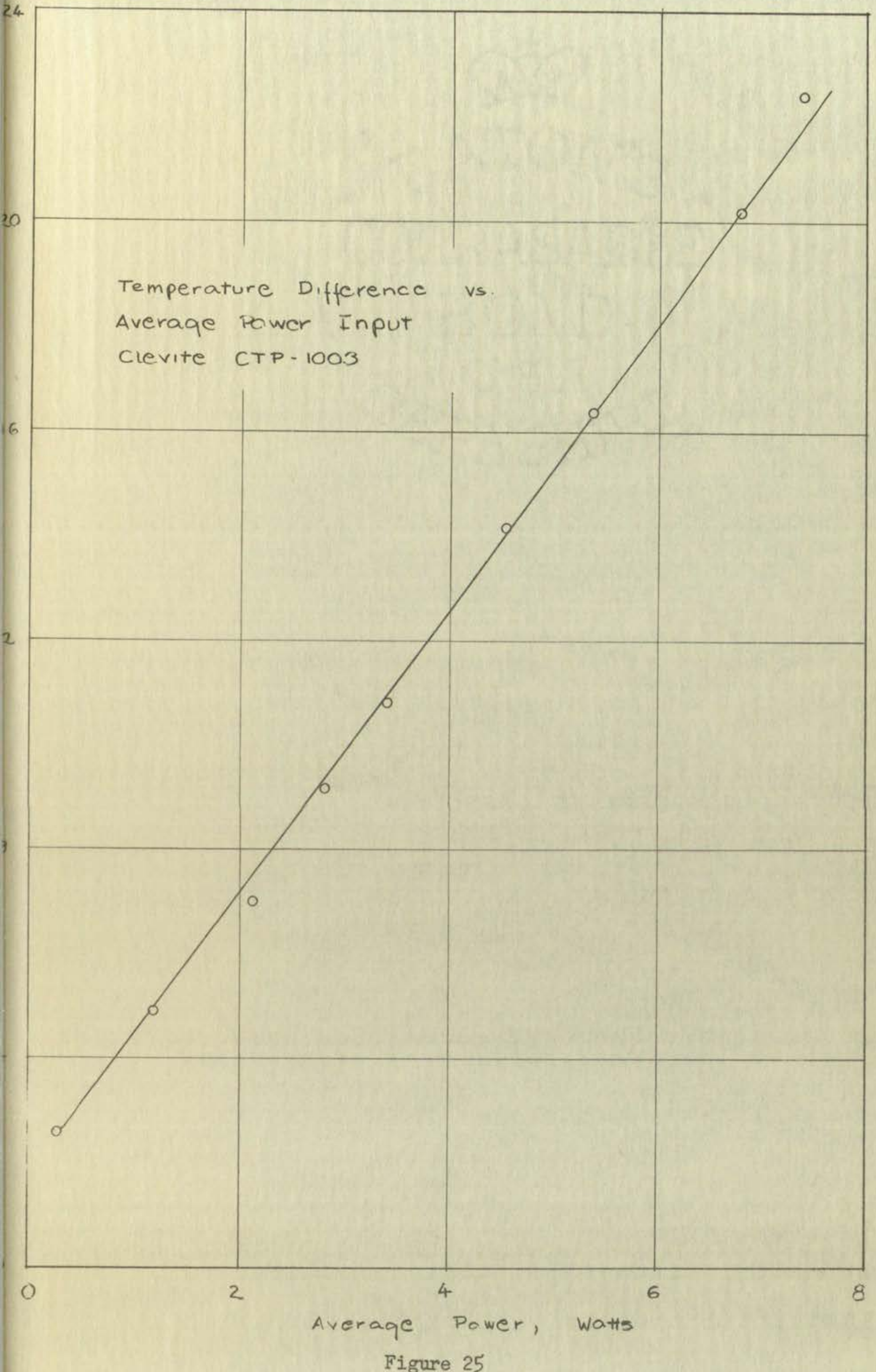
Temperature Difference vs.
Average Power Input
Clevite CTP-1003
24
20
16
0
2
4
6
8
Average Power, Watts

Figure 25

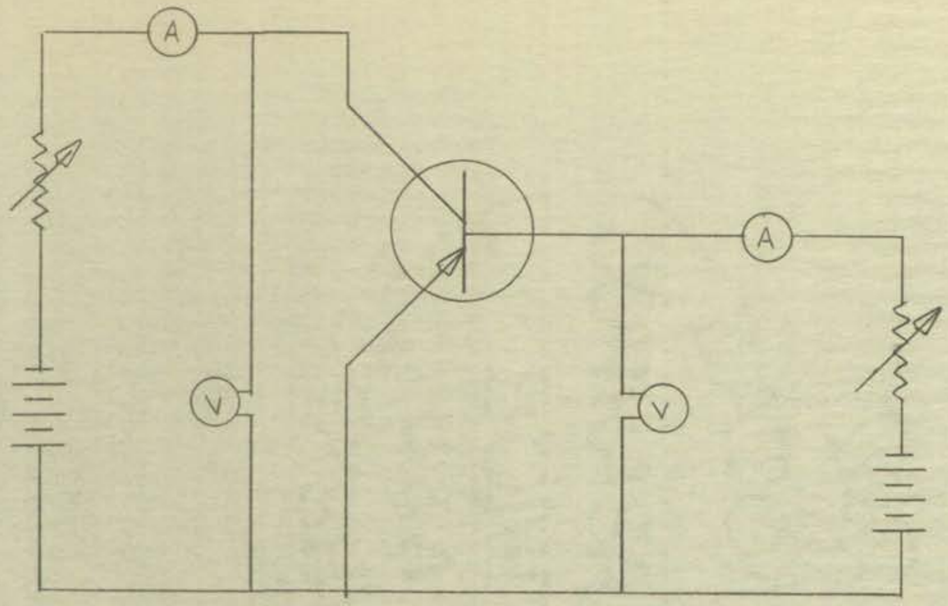

Figure 26

Circuit for Heat Sink Thermal Resistance Measurement

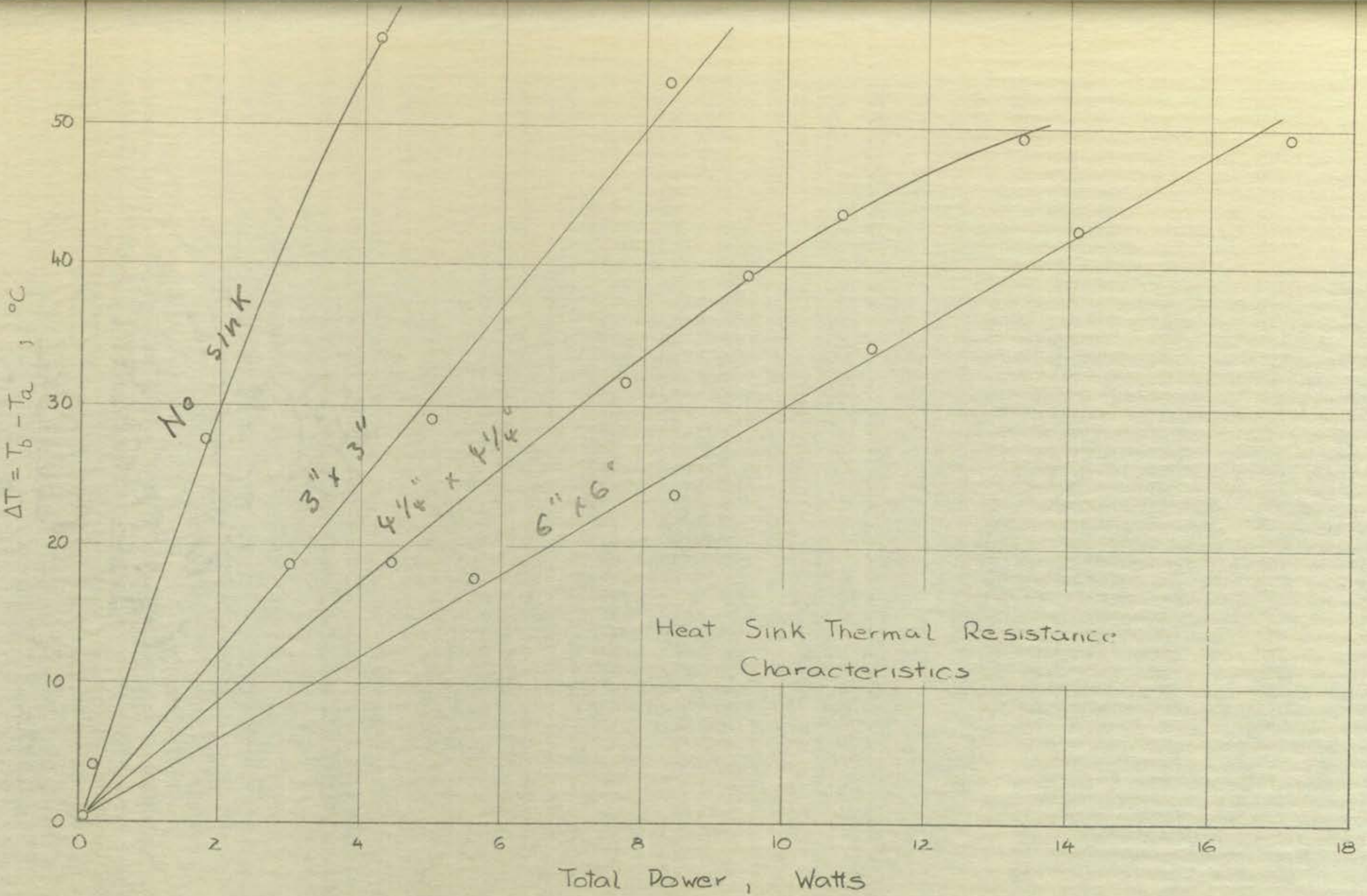
Heat Sink Thermal Resistance Characteristics
No sink
3" x 3"
4¼" x 4¼"
6" x 6"
ΔT = T_b - T_a , °C
0
10
20
30
40
50
0
2
4
6
8
10
12
14
16
18
Total Power , Watts

Figure 27

CHAPTER VI

APPLICATIONS OF JUNCTION TEMPERATURE CALCULATIONS

In Chapter III the power level at failure was determined by experimental methods. Here, the results of Chapter IV and V will be applied to evaluate the peak junction temperature at the failure points obtained in Chapter III. This will be carried out for the various pulsed conditions applied in the tests. Following this, a method will be presented for the calculation of maximum safe power dissipation of the transistor.

6.1 Junction Temperatures at Failure. To find the peak junction temperature at failure, the procedure presented in section 4.7 will be applied to the failure points obtained in section 3.8.

Using the dimensions of Fig. 2, page 8, the total junction area of the CTP-1003 is computed as 0.165 cm^2. This value and the constants of Table III, page 44, are used in computing D of (4-35):

$$D = \frac{\sqrt{2\alpha}}{K A \pi^{3/2}} = 10$$

For the purpose of calculating P_1 in (4-41), one must consider the circuit used in the tests. From Fig. 13, page 28, it is evident that there is a d.c. power dissipation in the emitter-base circuit. Then to compute the average junction temperature we should use the sum of the d.c. power and the average pulse power in the collector circuit.

$$\bar{T}_j = (P_c + P_{dc})\,\Theta_b + T_b$$

The value for Θ_b is given by the manufacturer as 2.4 °C/Watt. From

[illegible]

In [illegible] experimental [illegible] applied [illegible] obtained [illegible] pulsed [illegible] present [illegible] transition.

[illegible] tion temperature [illegible] will be [illegible]

[illegible] area of the [illegible] constants [illegible]

For the [illegible] cm. used [illegible] is a d.c. power [illegible] upon the [illegible] at a power [illegible]

The value for [illegible]

this the average junction temperatures are calculated for the failure points of Fig. 14, page 29. Then, making use of the graph on page 46 and equation (4-40), the difference between peak and average temperatures is computed.

The junction temperatures thus obtained vary considerably. Their average is shown in Fig. 28, page 63. Assuming that the theory behind the calculations is correct, this graph would indicate that the temperature limit of the junction increases with the duty cycle. This is contrary to what one would expect. The only conclusion one could draw from it is that some other factor influenced the failures recorded in section 3.8.

In light of the knowledge gained from the analysis of Chapter IV, another discrepancy appears. According to equation (4-31), the peak junction temperature varies as $\sqrt{\tau}$ if $\frac{\delta}{\tau}$ is kept constant. However, the location of the failure points shown in Fig. 14, page 29 does not seem to be greatly affected by a change in the period.

Even so the graphs of Fig. 28 bring out one valuable point. This is the increasing difference between peak and average junction temperatures with decreasing duty cycle. This point should be carefully considered in predicting the maximum power rating of the transistor for a specified operation.

6.2 Calculation of Maximum Power Rating for Pulsed Operation.

Because of the wide range of the computed junction temperatures at failure, the only conclusion that may be drawn from the graph of Fig. 28 is that the transistor will operate safely at junction temperatures below

that the [illegible] [illegible] [illegible] [illegible] for [illegible] [illegible]
points on the [illegible] [illegible], [illegible] of the [illegible]
equation (3.[illegible]), the [illegible] [illegible] [illegible] [illegible]
is [illegible].

The [illegible] [illegible] [illegible] [illegible] [illegible]
[illegible] in [illegible] [illegible] [illegible] elements [illegible] [illegible]
the calculations [illegible] [illegible] [illegible] [illegible]
pressure limit of [illegible] [illegible] [illegible] [illegible]
[illegible] to the [illegible] [illegible] [illegible] [illegible]
from it [illegible] [illegible] [illegible] [illegible]
section [illegible].

[illegible] of the [illegible] [illegible] [illegible] [illegible]
[illegible]; another [illegible] [illegible] [illegible] [illegible]
[illegible] [illegible] [illegible] [illegible]
the location of the [illegible] [illegible] [illegible]
to be [illegible] [illegible] [illegible] [illegible]

[illegible] of the [illegible] [illegible] [illegible] [illegible]
in the [illegible] [illegible] [illegible] [illegible]
[illegible] with [illegible] [illegible] [illegible]
considered [illegible] [illegible] [illegible] [illegible]
for a [illegible].

[illegible] [illegible] [illegible] [illegible]
because of the [illegible] [illegible] [illegible]
failure, the [illegible] [illegible] [illegible]
[illegible] [illegible] [illegible]

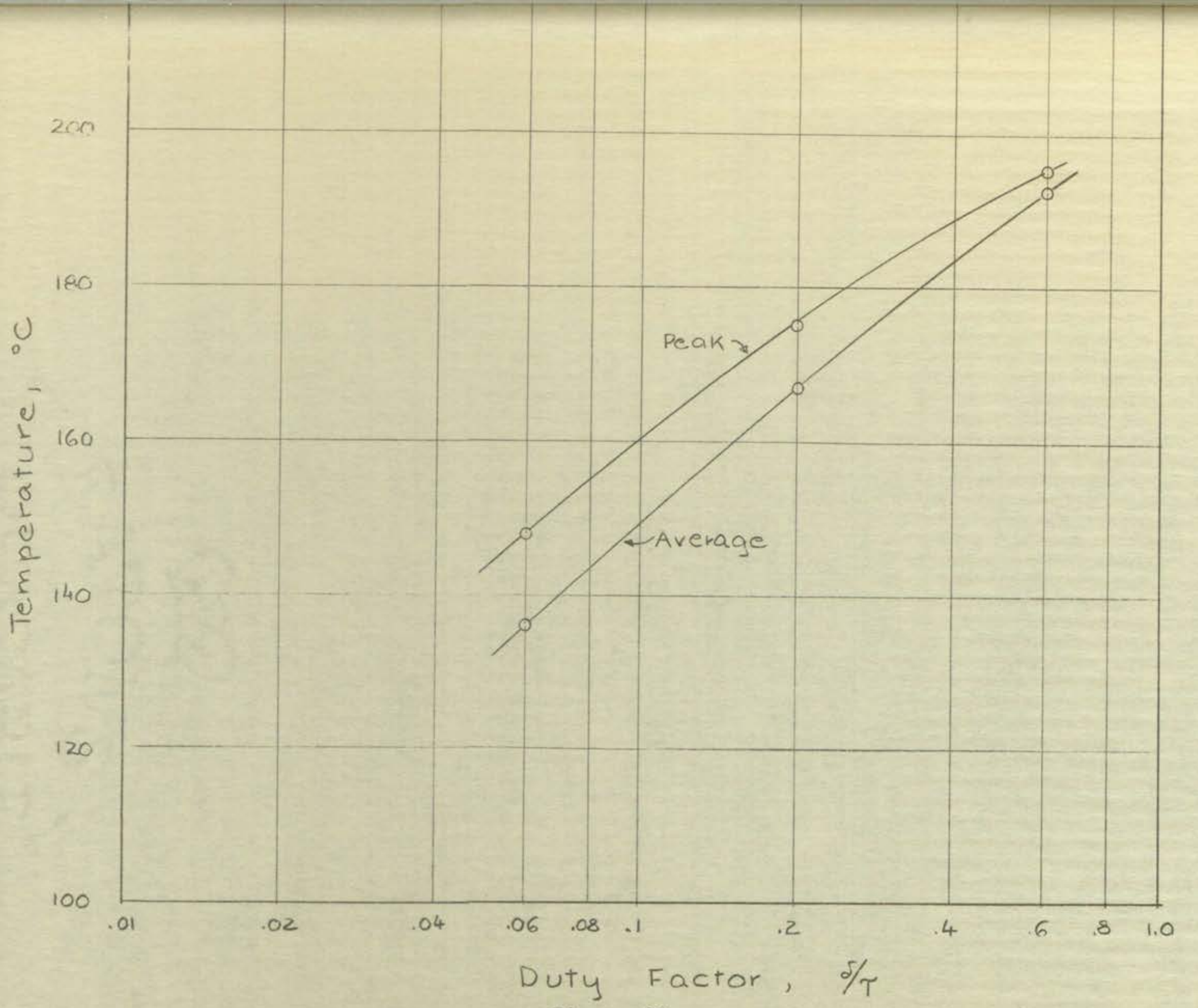

Figure 28

Junction Temperature at Failure vs. Duty Factor

100 °C. Then, making use of the work in section 4.7 again, we can write:

$$T_{j\max} = \bar{T}_j + \Delta T_{\max} \qquad (6\text{-}1)$$

$$= 100\ ^\circ\mathrm{C}$$

$$T_j = \bar{P}\theta_a + T_a \qquad (6\text{-}2)$$

$$\Delta T_{\max} = H_{\max}\, D\, \frac{P}{4.18} \sqrt{\tau} \qquad (6\text{-}3)$$

where θ_a now stands for total thermal resistance from junction to air. Substituting

$$100 = \bar{P}\theta_a + T_a + H_{\max} \frac{D\,P}{4.18} \sqrt{\tau} \qquad (6\text{-}4)$$

Then the maximum average power is given by

$$\bar{P} = \frac{100 - T_a}{\theta_a + \frac{H_{\max}\, D}{4.18} \sqrt{\tau}} \qquad (6\text{-}5)$$

where T_a = ambient temperature

θ_a = sum of thermal resistance from junction to base and from base to ambient

D = constant, evaluated according to section 4.7

τ = period

$H_{\max}$ is available from Fig. 20, page 46, for any given duty factor.

As an example, let us assume the Clevite CTP-1003 transistor operating under the following conditions:

$\frac{\delta}{\tau}$ = 10%

Frequency = 50 cps

6" x 6" heat sink

T_a = 25 °C

100 °C. [illegible]

water.

[illegible]

where [illegible]

Substituting

[illegible]

Then the [illegible]

[illegible]

where [illegible]

[illegible]

to [illegible]

[illegible]

[illegible]

[illegible]

As an example, [illegible]

operating [illegible]

[illegible]

$D = 10$, according to section 6.1.

$$\tau = \frac{1}{50} = 0.02$$

$$\sqrt{\tau} = 0.1414$$

$\theta_a = \theta_1 + \theta_2 = 2.4 + 3 = 5.4$, making use of the value given in Table IV for the 6" x 6" heat sink.

$H_{max} = 9.3$ for $\frac{\delta}{\tau} = 10\%$

Then, according to (6-5)

$$\overline{P} = \frac{100 - 25}{5.4 + \frac{9.3 \times 10 \times 0.1414}{4.18}} = 8.77 \text{ Watts}$$

The peak pulse power that may be safely dissipated is found as

$$\hat{P} = \overline{P}\,\frac{\tau}{\delta} = 87.7 \text{ Watts}$$

It should be noted that if a graph is used similar to those of Fig. 27, page 60, expressing thermal resistance of the heat sink as a function of temperature difference, it may be necessary to resort to the method of successive approximations in computing $\overline{P}$ if the graph is not a straight line. After $\overline{P}$ is found, it is a simple calculation to obtain the mounting base temperature if desired.

D = 12, according [illegible]

$T = \frac{1}{2\pi}$ [illegible]

$\sqrt{F}$ = 0.[illegible]

$\theta_x = \theta_1 + \theta_2$ = [illegible]

for the 0° K of [illegible]

R_{max} = [illegible]

Then, according [illegible]

$F = \frac{100 - 25}{2.1 + [illegible]}$

The peak value [illegible]

$\hat{F} = F$ [illegible]

It should be [illegible]

Fig. [illegible] [illegible] function of [illegible] method of [illegible] a straight line [illegible] the mounting [illegible]

CHAPTER VII

CONCLUSION

The main purpose of this study was to establish experimentally and theoretically a method of determining the power ratings of alloy junction power transistors in pulsed operation. This was accomplished within certain limitations. Here the accomplishments will be summarized and the limitations stated. Also, a few ideas will be presented on how the results of this work could be extended and improved upon.

7.1 Summary. The transistor was subjected to destructive tests and a relationship was established experimentally between the duty cycle of the pulsed input and the average power at failure.

An expression for instantaneous junction temperature in pulsed operation was derived for a thermal model. With this and the results of the tests, it was established that the transistor will safely operate at peak junction temperatures not exceeding 100 °C. A complete procedure was given for determining the maximum power dissipation for a transistor in pulsed operation.

The study provides a partial explanation of the heat flow phenomena present in the transistor, and of the nature of the junction temperature variation under pulsed excitation. This information should enable the designer of transistor pulse circuits to predict the maximum safe power dissipation of the transistor.

7.2 Limitations. The calculation of junction temperature is

CHAPTER VI

SUMMARY

Recent progress in [illegible] and theoretical [illegible] junction power [illegible] within certain limitations. [illegible] and the limitations [illegible] the results of this work [illegible]

1.1 [illegible] and [illegible] of the [illegible]

An [illegible] operation [illegible] the [illegible] at peak junction [illegible] dure [illegible] above [illegible]

The [illegible] nomena [illegible] perature [illegible] able the [illegible] safe power dissipation [illegible]

2. [illegible]

based on a thermal model incorporating several assumptions. Sizeable errors may have been introduced by neglecting the Germanium wafer which constitutes the base and extends beyond the Indium cylinders. The calculations were based on crystal dimensions which might well vary considerably among transistors of the same type. The value of thermal conductivity for pure Indium was used, but the actual thermal conductivity of the emitter and collector material may be a somewhat different value.

The graph of Fig. 20, page 46, used in all maximum junction temperature calculations, does not extend to values of $\frac{\delta}{\tau}$ less than .05. The computations necessary to extend this curve would be laborious.

This study indicates that the transistor will not be damaged by a peak junction temperature of 100 °C. No information is provided, however, whether the life of the transistor would be effected by continued operation at such high temperature.

7.3 *Suggestions for Improvements of the Results*. Although the power ratings established by the procedure of section 6.2 are on the conservative side, more confidence could be placed in the results if the calculated junction temperatures were experimentally supported. A circuit similar to the one described in section 5.3 could be used to measure instantaneous junction temperatures and thus justify the calculations and the thermal model. A similar method might be used to evaluate experimentally the coefficient D in equation (6-5), thus eliminating the need for such constants as junction area and thermal conductivity. This would, of course, also take care of variations in

based on a method [illegible]
errors may have [illegible]
constituents [illegible]
calculations were [illegible]
siderably [illegible]
[illegible]
of the [illegible]

The graph [illegible]
[illegible]
The conservative [illegible]

This study [illegible]
by a [illegible]
however, [illegible]
tinued operation [illegible]

7.2 [illegible]

the power [illegible]
conservative [illegible]
the calculated [illegible]
A circuit similar [illegible]
measure [illegible]
culation and the [illegible]
evaluate [illegible]
eliminating the [illegible]
conducti[illegible]

transistor dimensions discussed in the preceding section.

Using a computer, the graph of Fig. 20, representing maximum temperature variation, may be extended to small values of $\frac{\delta}{\tau}$.

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McAdams, W. H., [illegible] pany, Inc. 19[illegible].

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APPENDIX A

APPENDIX A

MEASUREMENT OF V_c - I_c CHARACTERISTICS OF TRANSISTORS

In section 3.3 the necessity of measuring the V_c - I_c characteristics was indicated. The circuit of Fig. 30, page 71, makes it possible to observe the V_c - I_c curve on the oscilloscope for one value of I_b at a time. A Fairchild F-286 Polaroid camera was attached to the oscilloscope and V_c - I_c curves for $I_b = 0, 20, 40, 60, 80,$ ma were consecutively recorded on the same photograph by means of multiple exposures. A comparison of photographs would indicate changes in α or I_{co}. Typical characteristics obtained by this method are illustrated in Fig. 29.

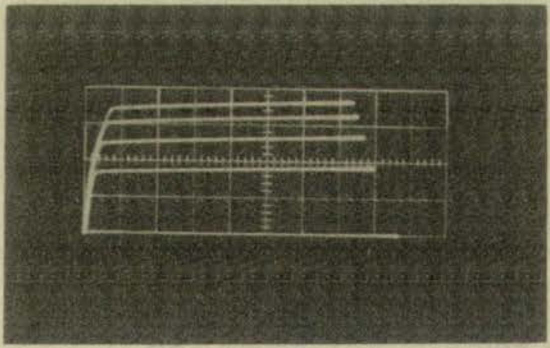

Figure 29

Typical V_c - I_c Curves

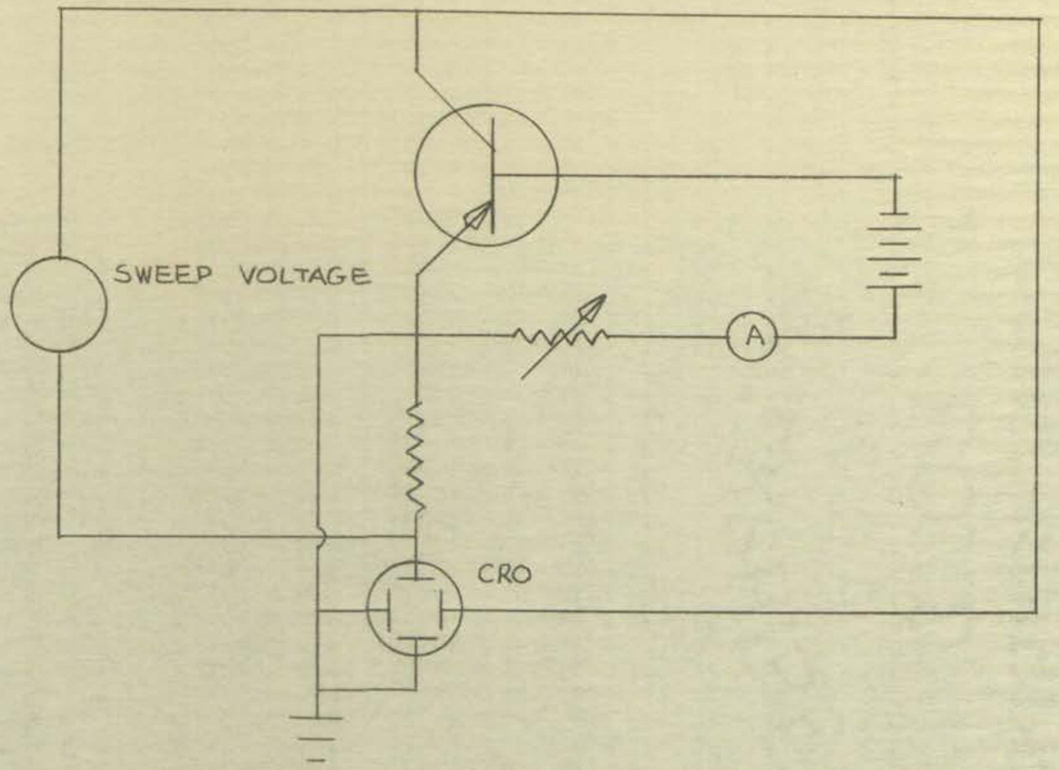

Figure 30

V_c- I_c Curve Tracer Circuit

APPENDIX B

APPENDIX B

PREPARATION OF SAMPLES FOR MICROSCOPIC EXAMINATION OF THE JUNCTION

In section 2.3 photomicrographs of the crossection of a good and a failed transistor crystal are presented. The small size of the crystal made it necessary to devise a special method which would enable one to slice it and polish the surface of the crossection for a microscopic examination. The following procedure was used to prepare this sample:

1. The metal cap of the transistor is removed with a hacksaw.
2. The exposed crystal is cut off the mounting base with a sharp knife, and the leads are clipped.
3. The crystal is then embedded in "Plasticast" (manufactured by Plasticast Company, Chicago, Illinois). A mold of approximately 2" x 2" x 2" will produce a sample of convenient size. A special catalyst which allows low drying temperatures must be used with the "Plasticast" in order to prevent the Indium of the transistor from diffusing into the plastic as it dries.
4. After the plastic has hardened, a slice is cut from it so that one face of it crossects the embedded crystal.
5. The sample is polished first on sandpapers of gradually decreasing courseness, then with emerycloth and crocuscloth. The final polish is acquired on a metallurgical table, using first jewelers rouge and then silicon carbide as abrasives.

After polishing, the sample is ready to be placed on the microscope. No etching is necessary.

PREPARATION OF [illegible]

In order to [illegible] a [illegible]

a failed transistor, [illegible] the crys-

tal made it necessary [illegible] of [illegible]

to allow it and [illegible] for a microscopic

examination. The following procedure was used to [illegible] this [illegible]

1. The metal cap of the transistor is [illegible] hacksaw.
2. The exposed crystal is cut [illegible] and the leads are clipped.
3. The crystal is then mounted in [illegible] quick [illegible] 2" will produce a [illegible] of convenient size. [illegible] which allows [illegible] cast" in order to prevent [illegible] sing into the [illegible]
4. After the plastic has [illegible] face of it [illegible]
5. The sample is polished [illegible] counter[illegible] with [illegible] The [illegible] is mounted on a [illegible] and then [illegible]

After polishing the sample [illegible] microscope, the [illegible]

APPENDIX C

APPENDIX C

SOLUTION OF THE FOURIER HEAT CONDUCTION EQUATION

In section 4.3 the one dimensional heat flow was represented as:

$$\frac{\partial T}{\partial t} = \alpha \frac{\partial^2 T}{\partial x^2} \qquad (1)$$

The solution to this equation, according to section 4.4, is

$$T = T_0 \, e^{-\sqrt{\frac{\omega}{2\alpha}}} \cos\left(\omega t - \sqrt{\frac{\omega}{2\alpha}}\right) \qquad (2)$$

This solution will now be derived by the separation of variables method.

The problem states that the solution is desired for a semi-infinite slab with a harmonic heat input at its surface. This statement yields the necessary boundary conditions which are as follows:

$$T(0,t) = T_0 \cos \omega t \qquad \text{(condition 1)}$$

$$T(\infty, t) = 0 \qquad \text{(condition 2)}$$

First, we assume that the variables are separable, i.e.,

$$T = u(x) \, . \, v(t) \qquad (3)$$

Then

$$\frac{\partial^2 T}{\partial x^2} = u''(x) \, v(t) \qquad (4)$$

$$\frac{\partial T}{\partial t} = u(x) \, . \, v'(t) \qquad (5)$$

Equation (1) becomes

$$u''(x) \cdot v(t) = \frac{1}{\alpha} u(x) \; v'(t) \tag{6}$$

$$\frac{u''}{u} = \frac{1}{\alpha} \frac{v'}{V} \tag{7}$$

Since u is a function of x alone, and V a function of t alone, the relation of (7) is possible only if both sides are constant. Hence

$$\frac{u''}{u} = K \qquad \text{and} \qquad \frac{1}{\alpha} \frac{V'}{V} = K \tag{8}$$

Solutions to these are:

$$u = C_1 e^{-\sqrt{K}x} + C_2 e^{\sqrt{K}x} \tag{9}$$

$$V = C_3 e^{\alpha K t} \tag{10}$$

Then substituting in (3)

$$T = c_3 e^{\alpha K t}\left(c_1 e^{-\sqrt{K}x} + c_2 e^{\sqrt{K} \cdot x}\right) = e^{\alpha K t}\left(c_1' e^{-\sqrt{K}x} + c_2' e^{\sqrt{K}x}\right) \tag{11}$$

Applying the first boundary condition, we get

$$T(0,t) = C'' e^{\alpha K t} = T_o \cos \omega t \tag{12}$$

$$C'' = C_1' + C_2' \tag{13}$$

To make this possible, αK has to be a pure imaginary number, and since α is real and larger than zero, $K = j\lambda$, where λ is real. Then

$$T(0,t) = C'' e^{j\alpha\lambda t} = C''\left[\cos \alpha\lambda t + j \sin \alpha\lambda t\right] \tag{14}$$

Equation (1) becomes

[illegible]

Since u is a function of x alone, the [illegible] solution of [illegible]
lation of (1) is possible [illegible]

[illegible]

Solutions to these are:

[illegible]

Then substituting in [illegible]

[illegible]

Applying the first boundary condition, we get:

[illegible]

To make this [illegible]
be real and [illegible]

[illegible]

$$T(x,t) = e^{j\alpha\lambda t}\left(C_1 e^{-\sqrt{j\alpha}\,x} + C_2 e^{\sqrt{j\alpha}\,x}\right) \tag{15}$$

Since

$$j = \frac{1}{2}\left(1+j\right)^2 \tag{16}$$

$$T(x,t) = C_1 e^{-\sqrt{\frac{\lambda}{2}}\,x + j\left(\alpha\lambda t - \sqrt{\frac{\lambda}{2}}\,x\right)} + C_2 e^{\sqrt{\frac{\lambda}{2}}\,x + j\left(\alpha\lambda t + \sqrt{\frac{\lambda}{2}}\,x\right)} \tag{17}$$

If $\lambda > 0$, then $C_2 = 0$, considering the second boundary condition. Similarly, if $\lambda < 0$, then $C_1 = 0$. Assuming $\lambda > 0$, and $C_2 = 0$, we have:

$$T(x,t) = C\, e^{-\sqrt{\frac{\lambda}{2}}\,x + j\left(\alpha\lambda t - \sqrt{\frac{\lambda}{2}}\,x\right)} = C\, e^{-\sqrt{\frac{\lambda}{2}}\,x}\left[\cos\left(\alpha\lambda t - \sqrt{\frac{\lambda}{2}}\,x\right) + j\sin\left(\alpha\lambda t - \sqrt{\frac{\lambda}{2}}\,x\right)\right. \tag{18}$$

Now since the equation is linear and homogeneous, both the linear and imaginary parts of this solution separately provide solutions. Also, since the first boundary condition involves a cosine but no sine, we take the real part

$$T(x,t) = C\, e^{-\sqrt{\frac{\lambda}{2}}\,x}\cos\left(\alpha\lambda t - \sqrt{\frac{\lambda}{2}}\,x\right) \tag{19}$$

Again with the use of condition one, we get

$$T(0,t) = C\cos\alpha\lambda t = T_0\cos\omega t \tag{20}$$

Since [illegible]

If [illegible]

Similarly, if [illegible]

Now since the [illegible]
imaginary parts [illegible]
since the first [illegible]
take the real part [illegible]

Again with the use of [illegible]

Hence

$$C = T_0 \qquad \text{and} \qquad \alpha \lambda = \omega \tag{21}$$

The solution may then be written as

$$T(x,t) = T_0 \, e^{-\sqrt{\frac{\omega}{2\alpha}}\, x} \cos\left(\omega t - \sqrt{\frac{\omega}{2\alpha}}\, x\right) \tag{22}$$

Hence

[illegible] and [illegible]

The solution may then be written as

[illegible]