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Fault Resilient and Reconfigurable Power Management

Using Photovoltaic Integrated with CMOS Switches

by

Rakeshkumar V Mahto

B.E, South Gujarat University, 2005

M.S, Electrical Engineering, California State University, Fullerton, 2009

DISSERTATION

Submitted in Partial Fulfillment of the Requirements for the Degree of

Doctor of Philosophy Engineering

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Dedication

This dissertation is dedicated to my family, for all the moral support, and encouragement.

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ABSTRACT

A Photovoltaic (PV) cell is a device which converts light incident upon it to electric current. The push for green energy due to global warming and diminution of fossil fuels opens up a huge market for PV cells. Hence, a lot of interest is being garnered for using PV cells for various applications. However, a PV module's performance degrades due to many anomalies such as failure of individual PV cell within a module, the opening of interconnection, a short circuit in the connection, failure of bypass diode, failure in voltage regulator or partial shading. To some extent all of these issues can be addressed by introducing a transistor as a switch in a PV module. This kind of architecture also enables the PV module to switch between high voltage with low current or high current with low voltage. Moreover, such architecture is handy when PV modules are deployed at remote locations where manual intervention in the case of fault or power management becomes too expensive or impossible. With advancements in semiconductor processing, the

MOSFET switches can now be integrated with a PV cell for improved reliability. In this research project, we introduced addressable switches for PV cell that enable the creation of real-time reconfigurable power buses or power island.

Moreover, for PV module deployed at a remote location, we have installed an architecture that let the PV module self-detect faulty PV cells or partial shading condition. Such algorithms detect faulty PV cells or PV cells under partial shading within the module such that the performance of the PV module does not become degraded. The algorithms actively use an embedded computing device to predict the output power based on a number of PV cells connected in series and parallel; then the computed power is compared with the measured power for faulty condition detection.

Typically, for achieving such kind of computing architecture a single-diode based PV module modeling technique is used. However, all of these modeling techniques have an exponential term due to the presence of a diode, the computing of output power and performance of PV module becomes power intensive and it is difficult to implement on an embedded system. Also, due to the presence of the exponential term, there is no closed form solution for I_{PV} versus V_{PV} (output current of PV cell versus output voltage of a PV cell). We have introduced a PV module modeling using an N-channel MOSFET transistor that doesn't have an exponential term. Moreover, a quadratic equation based solution is obtained that can be solved for calculating the load current. Using the same technique PV module can be also be modeled for various configuration. Additionally, with MOSFET based PV cells modeling enables the modeling CMOS-with-PV which is also presented in this work.

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1. Introduction

Recently solar cells have attracted a lot of attention due to its usage in the renewable energy for a clean and green environment. According to an estimate by the International Energy Agency (IEA), the cumulative capacity of the PV based power generation will touch 210 GW by 2020 [1]. Newer, more efficient and cheaper [2]–[4] ways to fabricate PV cells also have greatly contributed to the rise in demand. Additionally, the emergence of the global PV market also contributed heavily to the lowering the prices of the PV modules [1]. According to IEA, the prices of cells and module fell from USD 4/W in 2008 to USD 0.8/W. It is being estimated in [1] that the by 2035 the prices of the PV module will fall to USD 0.4/W. The rising US dollar against other currencies may further reduce these costs. Currently, PV cells are widely used to power residential and commercial buildings, small satellites, motor vehicles, electronics devices and in many other applications.

1.1 Photovoltaic (PV) System

Photovoltaic (PV) modules are made of solar cells by connecting them in series and parallel together to meet the load requirement [5]. To achieving higher voltage at the load terminal more PV cells are connected in series as shown in Figure 1. Alternatively, when two PV cells are connected in parallel, the total current is doubled keeping the terminal voltage constant. For building a PV module, initially all the PV cells are connected in series to achieve the desired

terminal voltage; after that configurations with similar numbers more same number of series PV cells are connected in parallel to meet the load current requirement.



Fig 1-1 PV cells output current vs output voltage characteristics under various configuration such that Ns (Number of PV cells in series) x Np (Number of PV cells in parallel)

However, a physical Photovoltaic (PV) module may suffer from many faults or defects, such as: short/open of a connection, physical damage to the cells, bypass diode failure, and others malicious [6]. Compared to bypass diode, it is shown that use of MOSFET as a switch with PV cells in the module can address most of these issues [7]–[9]. Moreover, for application such as powering of drones and CubeSat using photovoltaic module having an autonomous fault detection and mitigation is a necessity. Operations at a remote location or within hostile environment make human intervention to rectify the faulty condition almost impossible. Additionally, change in the lighting condition will also seriously hamper the performance of the load (i.e., under power the load). The ultimate goal of this work is to make PV module based power source resilient by making them reconfigurable. To make PV module reconfigurable, a CMOS was integrated within the PV cells in the module. Similar work is done in the past, however, that work ignored certain key opportunites such as the presence of the MOSFET transistor with the PV cells while modelling.

1.2 Resilient and Reconfigurable PV Module

The building of an effective resilient PV module requires three important features:

(1) an architecture by which the PV module can be reconfigured based on the load requirement, lighting environment and faulty condition; (2) an efficient algorithm that can enable the user to detect faulty the PV cells in the array in real-time without degrading the performance of load. But only detecting faulty PV cell is not enough since the presence of a faulty cell in the module can lead to damaging whole power source. Therefore, the algorithm should not only detect faulty PV cells but also remove them from the module in real time.

Since the fault detection and mitigation algorithm presented in this work does a comparative analysis between measured and computed power. Hence, an efficient way of modeling the PV module becomes very important. Therefore, the configuration of the PV module will be changing in the field depending on the load requirement, and lighting condition.

1.2.1 Contributed towards improving the previous proposed reconfigurable PV module.

The previously proposed MOSFET based reconfigurable photovoltaic (PV) based module's performance deteriorate due to the body connection of MOSFET switches was not connected properly. Consequently, the PV cells in a module will never turns-OFF and which leads to lowering of the performance of PV module. Moreover, for turning-OFF N-channel MOSFET transistor in the PV module, a new kind of switching architecture was required, which we will be presenting in this report. In addition, the newly proposed SerDes architecture can reconfigure whole PV cell array three times faster. Only one MOSFET switch can be turned on/off at a time in the previous

architecture, whereas with the new architecture the three different kinds of switches can be turn on/off simultaneously. Hence, the whole reconfigurable PV module can be reconfigured three times faster than the previously presented reconfigurable PV module.

1.2.2 Contribution in building autonomous fault and partial shading detection algorithms

An FPGA-based feedback enables self-fault detection and mitigation is presented in this report. For usage of such architecture at remote locations, a fault detection and mitigation algorithm is being presented. The algorithm performs a comparative analysis between the measured power and the expected result for fault detection and accordingly initiate a fault mitigation algorithm.

1.2.3 Contribution in developing MOSFET based Photovoltaic (PV) modelling and characterization

Currently, the easiet and most popular technique used to model PV cells is single diode based model. Compared to other PV cell modelling techniques such as single-diode, double-diode or three-diode based PV cell, that are widely being used by researchers, the technique described in this report gives a closed-form solution. Unlike diode based PV-cell modelling, where an iteration technique is used for the I_{PV} versus V_{PV} characterization, the technique presented in this paper gives I_{PV} = f(V_{PV} , T, G, Ns, Np). Additionally, due to quadratic nature of the mathematical model presented in this work, the model can be easily implemented on an embedded system for a fault detection and mitigation system. Furthermore, with recent advancements in PV manufacturing, where a monolithic MOSFET is embedded with a PV cell, such a modelling technique is very useful for characterization.

1.3 Organization of Dissertation

The rest of this dissertation is organized as follows. Chapter 2 describes the related work such as different kind of fault that occurs in the PV modules and techniques used to mitigate them. Chapter 3 talks about the different PV cells and module modelling techniques. Chapter 4 addresses the issues in the previously proposed CMOS with PV module. Since the older technique is slow in reconfiguring whole PV module and has a major flaw in the way MOSFET switches were connected. In addition, Chapter 4 discusses the partial shading detection and mitigation algorithm. In the end Chapter 5, summarized the work so far and suggestions for future work.

2. Background

The output power of the PV module depends on many factors but the two most important of these is solar irradiance and temperature. However, there are some other factors also which may reduce the power output of the PV modules or reduce the module's life expectancy. These are a) losses due to mismatch/partial shading between solar cells in the modules, b) temperature of the PV cells in modules and c) failure in the PV modules [10].

2.1 Different Kinds of Faults PV Modules

2.1.1 Effects of mismatch and shading

If all the PV cells in the modules are operating at the same temperature with identical electrical characteristics and all of them receive the same solar irradiance, then all the cells should operate at the exactly same voltage and current.

The equation for the module is given by

$$I_T = P \cdot I_L - P \cdot I_0 \cdot \left[e^{\left(\frac{q \cdot T_T}{S}\right)} - 1 \right]$$
(2.1)

where:

S is the number of cells in series

P is the number of cells in parallel

- I_T is the total current from the circuit
- V_T is the total voltage from the circuit
- I_0 is the saturation current from a single solar cell

 I_L is the short-circuit current from a single solar cell

N is the ideality factor from a single solar cell

T is the temperature

q is the charge

In ideal condition, the I-V curve of identical PV cells for the total short circuit current and open load voltage is given by

$$I_{SCtotal} = P.I_{SC} \tag{2.2}$$

$$V_{OC \ total} = S.V_{OC} \tag{2.3}$$



Fig 2-1 A PV Module of 36 PV cells connected in series

The above equation states the total short circuit current across the PV module is given by the short circuit current of individual PV cells times the number of cells connected in parallel. Similarly, for the open load voltage at the terminal of the PV module will be equal to the number of PV cells connected in series times the open load voltage of individual PV cell.

But in reality, due to mismatches caused by the interconnection of PV cells or modules not having same electrical characteristics or facing different operating condition (such as shading) might result in power loss or irreversible damage to the cells due to hot spot.

2.1.1.1 Effect of series mismatch

In a series mismatch, one of the PV cells in the array is either operating under the shade or electrical parameters of one or more cells doesn't match with the rest of the cells in series. Under such condition, the total current flowing through the series PV cells will be equal to the current of the shaded or damaged cells as shown in Fig 2-2. As per Fig 2-3, the short circuit current is driven by the current of the damaged PV cell which is I_{SC2}. The rest of the current from the "good" PV cell will be forced to flow through the diode which leads to forward biasing of the diode.



Fig 2-2 Equivalent circuit for mismatched PV cells operating under short circuit condition As shown in Fig 2-3, the open circuit voltage is slightly affected due to mismatch due to logarithmic relationship between open circuit voltage with respect to the short circuit current as can be seen in Fig 2-3. This kind of the mismatch is very common and considered to be most critical as it can lead to lowering of load current. The forward biasing across all the damaged or shaded PV cells in series cause a large power dissipation within the damaged cells. This power

dissipation over small area results in local overheating or "hot-spots". This hotspot may lead to unrepairable damage to the PV cells. In the plot shown in Fig 2-3, a reduction in short circuit current density across the damaged cell by 20% resulted in the reduction of the short circuit current across the series by 20%.



Fig 2-3 Effect of current mismatch in series

2.1.1.2 Effect of Parallel mismatch

For increasing the current through the load more PV cells are connected in parallel. Even though current coming from each PV cell in parallel are different due to mismatch but then also the short circuit current will be equal to summation of the short circuit current of all the PV cells in parallel. But mismatch will affect the open circuit voltage across the positive and negative terminal of PV module as shown in Fig 2-5.



Fig 2-4 Mismatched cells due to shading are connected in parallel



Fig 2-5 Effect of mismatch in the PV cells connected in parallel

2.1.2 Effect of temperature

Enclosing of the PV cells in the PV module leads to the reduction of heat flow out of the module. These results in a gradual increase in the temperature across the PV cells within the module. The increase in the junction temperature across in PV cells results in a reduction of the voltage across PV module. Reduction in the voltage across PV module results in lowering the output power. The general equation for estimating the voltage of a given material at a given temperature is given by

$$V_{OC,ambient} = Temperature Coefficient \cdot (T_{STC} - T_{ambient}) + V_{OC rated}$$
(4)

where,

 $V_{OC,ambient}$ = open circuit voltage at module temperature, V T_{STC} = temperature at standard test condition (STC) , 25 °C $T_{ambient}$ = module temperature

 $V_{OC \ rated}$ = open circuit voltage at STC

2.1.3 Failure in a PV module

For various applications of the PV cell module failure in the module can create hindrance to the power availability from the module. These faults in the PV modules might result in a reduction in power generation, availability, and reliability of the overall system. For some application like CubeSat or satellite, replacing of PV cells in case of failure becomes almost impossible. So it is important to identify the faulty or failure conditions in PV modules (and perhaps remotely repair them). These failures can happen due to: i) individual PV cell failure, ii) opening of interconnection, iii) short circuit in the connection and iv) failure in the voltage regulator.

2.1.3.1 Individual Cell failure

Due to hostile environmental factors such as snowfall, rain, wind and other factors (i.e., vandalism) might result in breaking of PV cells which can seriously damage the performance of PV cells. These conditions can also lead to failure of the entire panel. The breaking of the top glass surface also to some extent can also lead to lowering of the power generation. Glass cracking can also

happen as a result of hot spot creating due to the presence of one of more mismatched PV cells in series with "good" one.

2.1.3.2 Opening of Interconnection

Even such as aging and corrosion of conductor, melting of solder due to hot spots, poor connection, and accidental disconnection of current carrying conductors, can lead to the opening of current carrying path in series with the load. Opening interconnection of parallel PV cell can lead to the lowering in load current. The opening of interconnection can also lead to total failure of PV panel!

2.1.3.3 Short circuit in the connection

Short circuit of the connection can result from insulation degradation due to weather which can lead to delamination, cracking or electrochemical corrosion [10].

2.1.3.4 Failure in the voltage regulator

A block diagram a simple PV module based power generation and distribution is shown in Fig 2-6. Failure of the voltage regulator as a consequence of electrical and/or mechanical abnormalities can lead to failure of whole PV panel. Also, voltage regulator performance or settings are predetermined at the time of circuit design so efforts to make the PV panel operate at Maximum power point (MPP) after the fact is almost impossible.



Fig 2-6 A basic block diagram of a photovoltaic cell array based power generation system

2.1.3.5 Failure in the bypass diode

Bypass diode plays a very important role in safeguarding PV cells connected in parallel to them. In case of partial shading or faulty condition in PV cells the reversed biased diode becomes forward biased. Therefore, the bypass diode now bypasses the current through them. Moreover, a bypass diode gives protection to PV cells in case of series arc generation in a PV module [11]. However, a bypass diode can result in a significantly reduction in the performance of a PV module. The bypass diode failure can be described in two separate modes: short circuit or open circuit of bypass diode [12]. A short circuit failure of bypass diode can result in bypassing of healthy PV cells in the module. This can result in seriously affecting the performance of PV module, such that a failure of one bypass diode in a module that consists of 60 cells module can result in almost a 1/3rd loss in power [12].

2.2 Previously Used Fault Mitigation Techniques in PV modules

Among all the faulty situation discussed in the previous section, the mismatch in the series connection and partial shading are the most severe. As these can lead to permanent damage of the module and also may result in a fire hazard. The effect of the hotspot can be reduced by employing bypass diodes. Recently, instead of using a static technique for bypassing the faulty PV cells using bypass diode, a MOSFET transistor is used [7]. Higher scalability of MOSFET results in these MOSFETS being more easily be integrated with PV cells. Moreover, unlike bypass diode, MOSFET with PV cells provides a dynamic solution to faulty conditions since they provide direct access to each PV cells in the array.

2.2.1 Bypass Diode with PV

It was first shown in [13] that using a bypass diode across a group of four PV cells connected in series will improve the efficiency of the overall PV module as shown in Fig 2-7. The bypass diodes (most of the time) are reversed biased until the PV cells connected across them are operating normally. Once one or more PV cells connected across the bypass diode are not performing up to the mark due to a fault or partial shading this leads to lowering of the voltage across the four PV cells connected across the bypass diode will become forward biased which leads to the bypassing of current through the bypass diode and opening of the PV cells connected across the bypass diode.



Fig 2-7 Bypass diode connected in parallel across four PV cells

Later, in [14]– [17] it was shown the effect of using bypass diode in reducing the effect of partial shading on PV module which, if ignored, then results in the reversed biasing of PV cell in a module. Many studies have shown the effectiveness of pass diode in successfully mitigating the hot-spot in PV module[12]–[15].

2.2.3 MOSFET Transistor with PV

Though the bypass diode does a good job in rectifying the series mismatch, partial shading, and hotspot conditions, many times with faulty PV cells, healthy PV cells also get bypassed. Additionally, the bypass diode in a PV module can also fail. The bypass diode in the module can

either become shorted or open circuited [12], [16]. A short circuit of the bypass diode will lead to four PV cells in the PV module being removed permanently. Whereas, an open circuited bypass diode can lead to hot spot creation. A more efficient way of dealing with partial shading is by using MOSFET switches as shown in [7], [9], [17]–[19].

The MOSFET based PV module presented in [7], [19] is shown in Fig 2-8. As can be seen in Fig 2-8, each of the PV cells are connected with MOSFET switches except the last one. Each of the PV cells is connected with two kinds of switches, P-switch and S-switch. The top of the PV cell is integrated with S_{PT,i} P-switch, and the bottom is integrated with S_{PB,i} P- switch and S-switch, S_{S,i}.



Fig 2-8 The reconfigurable MOSFET based PV module.

The PV module can be switched to different configurations by controlling the gate voltage at a given switch. The MOSFET switch circuit is shown in Fig 2-9. At a given time the P-switch and S-switch should be operating in different states otherwise; it might result in uncertainty in the number of PV cells connected in series or parallel.



Fig 2-9 The switch circuit

An example, is shown in Fig 2-10, shows that the two separate groups of PV cells can be connected together by using the P-switch and S-switch.



Fig 2-10 An example to elaborate the reconfigurable PV module

In the PV group 1, four PV cells are connected in parallel, whereas, in PV group 2, three of them are connected in parallel. Later by the S-switch the PV group 1 and PV group 2 are connected in series.

The use of MOSFET switches with the PV module also facilitates in creation reconfigurable power buses or power island as presented in [9], [17]. Additionally, this kind of technique is very handy for applications such as satellite and drones where power distribution and management needs to be resilient due to remoteness, thereby being non-serviceability.

The concept of using MOSFET transistor with PV module to address the partial shading is presented in [20].

2.3 Summary

In this chapter, we discussed the different issues or faulty condition faced by the photovoltaics modules in the field. Later, the techniques were described which can help in mitigating some of the issues. A bypass diode with PV and MOSFET integrated PV were explained. The benefit and shortcoming of each of them were argued.

3. Photovoltaics (PV) Module Modeling and

Characterization

3.1 Background

For furthering the research in PV modules it is very important to have an approximate method to model them. In this manner pros and cons of the design can be tested before deploying the PV module based system in the field. In last decade, many mathematical models for PV cells simulation and modeling techniques is being proposed [21]–[31]. The primary aim of an accurate mathematical model of a PV panel, module, or cell is to optimize the design and dimensioning of PV to maximize their power generation capability. Existing PV cell models can mainly can be classified into three categories mainly, single diode, double diode, and three diodes. However, due to the presence of the diode in the modelling technique, for calculating the current across the diode, an exponential function of the voltage across the diode comes in picture. Therefore, finding a closed-form solution of the current through of a PV module, IPV, becomes very difficult. To address this issue, either curve fitting, iterative method or approximation technique is being used. Instead, in this chapter, we are modelling the PV module by having N-channel MOSFET (NMOS) based modeled PV cells. Using of NMOS based modelled gives a closed form of I_{PV} as a function of V_{PV} , operating temperature T, and irradiation G. Moreover, this approach results in the output current of a PV module in terms of Vpv, Ns number of PV cells connected in series, Np numbers of PV cells in parallel operating temperature T, and irradiation G.

3.1.1 Single diode based PV cells modeling

The simplest method used to model a PV cell is by using single diode method as shown in Fig 3-2. The current across the load, I_{PV} is given by Eqn. (5),

(5)

$$I_{PV} = I_{Ph} - I_D - \left(\frac{V_{PV} + I_{PV} \times R_S}{R_P}\right)$$

$$I_D = I_S \left(e^{\frac{V_{PV} + I_{PV} \times R_S}{A \times V_t}} - 1 \right)$$
(6)

$$I_{ph} = \frac{G}{G_{STC}} \cdot I_d \tag{7}$$

The symbols used in Eqns. (6), (5), and (7) are summarized as follows: I_{ph} is the photon current; I_D is current across the diode and is given by (6); Vpv voltage across the load; Rs is the internal series resistance of PV cell; Rp is the internal shunt resistance of a PV cell; Is is the diode saturation current; V_t is the thermal voltage which is equal to 26mV, A is diode quality factor, G is solar irradiation; G_{STC} is solar irradiation at standard testing condition which is equal to 1000 W/m², I_d is the dark current.



Fig 3-1Single diode based PV model
3.1.2 Double diode based PV cell modeling

To obtain better accuracy and better curve fitting between measured data with the simulation data for modelling the PV cells two diodes based PV cells was proposed in [26]. Subsequently, it was developed further in [22], [32].



Fig 3-2Two-diode based PV cells modeling

$$I_{PV} = I_{Ph} - Id_1 - Id_2 - I_P$$
(8)

$$I_{PV} = I_{Ph} - I_{d1} - I_{d2} - \left(\frac{V_{PV} + I_{PV} \cdot R_S}{R_P}\right)$$
(9)

$$I_{d1} = I_{S1} \left(e^{\left(\frac{V_{PV} + I_{PV} \cdot R_S}{V_t}\right)} - 1 \right)$$
(10)

$$I_{d2} = I_{S2} \left(e^{\left(\frac{V_{PV} + I_{PV} \cdot R_S}{A \cdot V_t}\right)} - 1 \right)$$
(11)

3.1.3 Three diodes based PV cell modeling

For modelling mutlicrystalline silicon (Mc-Si) solar cells a 3-diode based equivalent circuit model was proposed in [33]. The equivalent PV cell model is shown in Fig 3-3.



Fig 3-3 Equivalent PV cell modeling using 3-diode

$$I_{PV} = I_{Ph} - I_{d1} - I_{d2} - I_{d3} - I_P$$
(12)

The equation can be solved further to get the output current, IPV.

3.1.4 PV Array modeling from single PV cells

The entire PV module can be modelled with a single PV cell such the output power depends on the number of the PV cells connected in series and parallel in the module [26]. To use this technique for construction of the mathematical model, it is assumed all the PV cells in the array are the same and there is no process variation. Additionally, it is also assumed that all the PV cells are receiving same the irradiation and are operating at the same temperature. To explain the array decomposition, consider an array consist of 3×2 PV cells as shown in Fig 3-4. The final output current and voltage of the PV module can be modelled similar to the done for the single diode



Fig 3-4 PV array decomposition to form a composite model

$$I_{PV} = 2 \left[I_{Ph} - I_S \left(e^{\frac{\left[\frac{V_{PV}}{3} + \frac{I_{PV}}{2} R_S \right]}{A \cdot V_t}} - 1 \right) - \frac{\left[\frac{V_{PV}}{3} + \frac{I_{PV}}{2} R_S \right]}{R_P} \right]$$
(13)

To make a generalized equation, the 2 can be replaced with N_P , the number of PV cells in parallel. Likewise, 3 can be replaced with N_S , the number of PV cells in series.

3.1.5 Iterative technique for modeling PV module

Due to the presence of the exponential term in the output current and voltage across the PV module modeling becomes more difficult. Therefore, in past decade many SPICE based PV module modeling technique are being presented [34]–[40]. However, employing a numerical modeling technique to model PV module is much better approach since it doesn't require a specialized SPICE simulator.

To model PV module, an iterative technique is presented in [25]. This PV array's model circuit is shown in Fig 3-5



Fig 3-5 PV array model circuit with a controlled current source and equation computation block In this technique for calculating the output current value, previously calculated output current value is substituted in the present output current equation. The technique is presented is much easier to solve and implement. However, if the step size of the V_{PV} iteration is not small enough then incorrect results can be produced.

3.1.6 Approximation technique for PV module modeling

Besides using the iterative technique, other easier approximation technique for modelling the PV module are presented in [41]–[43]. The models [41]–[43] utilizes the Taylor series expansion to eliminate quadratic and higher order term from the current-voltage (I-V) modeling. The equation for the current through the diode in the single diode based PV module modeling technique has an exponential term. This exponential term is simplified by using the Taylor series expansion to linear term only.



Fig 3-6 1-diode PV cell modeling

As its presented in previous topic output current equation is given as

$$I_{PV} = I_{Ph} - I_S \left(e^{\frac{V_{PV} + I_{PV} \times R_S}{A \times V_t}} - 1 \right) - \left(\frac{V_{PV} + I_{PV} \times R_S}{R_P} \right)$$
(14)

The diode current I_D can be approximated by Taylor series expansion

$$I_{D} = I_{S} \left(e^{\frac{V_{PV} + I_{PV} \times R_{S}}{A \times V_{t}}} - 1 \right)$$
(15)

$$e^{z} \approx 1 + z + \frac{1}{2!}z^{2} + \frac{1}{3!}z^{2}$$
 (16)

Using Taylor expansion series an easily solvable output current I_{PV} equation in terms of V_{PV} can be obtained.

3.2 MOSFET based PV cell modeling

As discussed in the previous section, the presence of the exponential term makes it essentially impossible to obtained a closed form solution. A MOSFET based PV module modeling technique is presented in [44]. A similar modelling technique is presented in [29], [45]. But, this kind of modelling is not suitable when the configuration of the PV module is changing in the field application[7], [9], [17], [18], [46], [47]. Therefore, the building of a PV module model from a single NMOS based PV cell model is desirable.

3.2.1 PV cell modeling

For building the new N-channel MOSFET (NMOS) based PV cell model, the diode in Fig 3-6 **Error! Reference source not found.**can be replaced with a MOSFET in "diode configuration" [48] as shown in Fig 3-7. In this work we will be using ON-Semi 0.5 um technology node, though, other semiconductor manufacturing technology node can also be used. However, in the ON-Semi 0.5um technology node, the threshold voltage, V_{tho} of NMOS transistor is equal to 0.7V. This means just having an NMOS with drain and gate shorted alone will not be sufficient for modeling a PV cell since the open load voltage, V_{OP} of a single PV cell is between 0.5 to 0.55V, whereas the threshold voltage of NMOS is 0.7V. Therefore, the current across a load of PV cells, going from the I_{ph} to the zero will not happen since the NMOS transistor will never turn-ON for any given voltage less than the threshold voltage. To address this issue, a negative voltage, Vn, should be applied between source and body/substrate terminal of NMOS.



Fig 3-7 N-Channel MOSFET based PV cell model

The effect of applying negative voltage on threshold voltage, Vth is best explained by equation below:

$$V_{th} = V_{thO} + \gamma \left(\sqrt{\left| 2\Phi_F \right| + V_n} - \sqrt{\left| 2\Phi_F \right|} \right)$$
(17)

where, Vtho is the threshold voltage when source and body are at the same potential, γ is the body effect coefficient parameter that is dependent on the technology, ΦF is the Fermi potential and Vn is the voltage between the source and body terminal.

Once the diode is replaced by an N-channel MOSFET operating in the saturation region, the current across the load is given by:

$$I_{PV} = I_{Ph} - I_M - \left(\frac{V_{PV} + I_{PV} \times R_S}{R_P}\right)$$
(18)

where,

$$I_M = \frac{K_n}{2} \frac{W}{L} \left(V_{DS} - V_{th} \right)^2 \left(1 + \lambda V_{DS} \right)$$
(19)

$$V_{DS} = V_{PV} + I_{PV} \times R_S + V_n \tag{20}$$

In Eqns. (18), (19) and (20), I_M is the current through the N-channel MOSFET; K_n is the process transconductance parameter, W is the width of the channel in μ m; L is the length of the channel in μ m, Vds is voltage between drain and source terminal of N-channel MOSFET; V_{th} is the threshold voltage of the N-channel MOSFET, λ is channel length modulation effect, Vn is the voltage source connected to source terminal to lowering the V_{th} of N-channel MOSFET. For characteristics of the PV cell model shown in Fig 3-1, and Fig 3-7 to be equal, the Eqns. (6) and (19) have to be equal. Equating and solving for the W/L term we get,

$$\frac{W}{L} = \frac{2 \cdot K_n \cdot I_s \cdot \left(e^{\frac{V_{PV} + I_{PV} \times R_s}{A \times V_t}} - 1\right)}{\left(V_{DS} - V_{th}\right)^2 (1 + \lambda V_{DS})}$$
(21)

For obtaining IPV vs VPV curve, all the known values have to be substituted in Eqn. 4

$$I_{pv} = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} \tag{22}$$

Where,
$$a = \frac{K_n}{2} \left(\frac{W}{L}\right) R_s^2$$
 (23)

$$b = 1 + K_n \left(\frac{W}{L}\right) R_S (V_{PV} + V_n - V_{th}) + \frac{R_S}{R_P}$$
(24)

$$c = -I_{ph} + \frac{K_n}{2} \left(\frac{W}{L}\right) \left(V_{PV} + V_n - V_{th}\right)^2 + \frac{V_p}{R_p} \quad (25)$$

Eqn. 9 is only valid if $V_{ds} > V_{th}$, otherwise, output current , I_{PV} , can be calculated by considering current $I_M = 0$ in equation (18) which is given below

$$I_{PV} = \frac{I_{Ph}R_P - V_{PV}}{R_P + R_S}$$
(26)

3.2.2 MOSFET based PV module modeling

The scheme for building the module level characteristics from a single N-channel MOSFET based PV cell is shown in Fig 3-8. A PV cell model is such that if they are connected in an array then mathematically they can be treated as a single PV cell as shown in Fig 3-8 for N_S(number of cells in series) x N_P (number of cells in parallel). To illustrate the cell decomposition we are assuming N_S x N_P = 3 x 2 cells. Firstly, in row decomposition the series PV cells are converted into equivalent PV cells. Later, using column decomposition, parallel PV cells can be translated into the equivalent circuit. The current I_{PV} across the N_S x N_P PV cell module is given by,

Column Decomposition



Fig 3-8 Cell decomposition to form a simple model to predict output voltage and current of a PV module of configuration Ns x Np = 3 x 2

$$I_{PV} = N_P \left(I_{Ph} - I_M - \frac{\left(\frac{V_{PV}}{N_S} + \frac{I_{PV} \cdot \mathbf{R}_S}{N_P}\right)}{R_P} \right)$$
(27)

$$I_{M} = \frac{K_{n}}{2} \frac{W}{L} \left(\frac{V_{PV}}{N_{S}} + \frac{I_{PV}R_{S}}{N_{P}} + V_{n} - V_{th} \right)^{2}$$
(28)

The channel length modulation effect, λ is ignored in Eqn. 24. In Eqns. 23, 25 it is assumed that all PV cells are identical in the module and are operating at the same temperature and receiving the same intensity of light.

3.2.3 Comparison between SPICE model with hand calculation

We compared the SPICE simulation of the PV module containing 1-diode based PV cells, Nchannel MOSFET based PV cells, with the mathematical model presented in this paper for different Ns x Np as shown in Fig. 3. In the I_{PV} vs V_{PV} characteristic curve, the solar irradiance, G is assumed to be of 1000 W/m² when the temperature, T= 25 °C.



Fig 3-9I-V curve comparison between spice simulations with N-Channel MOSFET vs single diode PV module vs hand calculation

3.3 Summary

In this chapter, a various technique for modeling PV cells and the modules is presented. Each of them was discussed briefly. Later, an N-channel MOSFET based PV module modelling using cell decomposition technique from individual PV cells was described. It was also shown that the MOSFET based PV module modeling technique yield a more simply calculated closed form solution for the I_{PV} vs V_{PV} curve which was not possible with the single, double or three diode PV cell models. The comparative analysis between SPICE simulation and a mathematical model was also presented.

4. Autonomous Fault Detection Architecture and Algorithms

4.1 Background

For space applications, the power distribution, and management of a Cubesat or Smallsat need sto be resilient considering non-serviceability and hostile environment in space. A battery based power system will have lower power to weight ratio whereas chemical/nuclear power will be very unstable, unsuitable, and dangerous. It was shown that, for a micro autonomous aerial system, InAs DWELL QD-based thin film photovoltaic cells are more efficient in powering Cubesat or Smallsat due to their better power to weight ratio[49]. Generally, most of the photovoltaic cell based power generation and distribution system are predetermined at the time of design. A failure due to overexposure to radiations in space will be a hindrance in functionality and lifespan of the device. At remote locations such as space, manual intervention in the case of fault or power management becomes too expensive or impossible. All of these issues can be addressed by introducing a transistor as a switch in a PV module[7], [9], [17], [18]. This kind of architecture also enables the PV module to switch between high voltage with low current or high current with low voltage. With advancements in semiconductor processing, the MOSFET switches can now be integrated into a PV cell for enhanced reliability[50].

However, while characterizing CMOS with PV cells, we found out that when a single MOSFET is connected with multiple PV cells in series, then the body connection, as well as the voltage

across the gate terminal with respect to the source terminal of the MOSFET, becomes very important. If proper care is not taken, then the transistor continues to stay ON even when the user wishes it to be OFF, resulting in degradation in performance of the PV module. In this chapter, we are proposing a new architecture that addresses this issue and also present our findings.

4.1 MOSFET based embedded PV modules

A switching system based PV matrix enables PV cells in the panel to be connect in series and/or parallel that creates real-time reconfigurable power buses or a power island. This series and parallel connection enables the PV panel to power the load under varying lighting condition by connecting more cells in series to maintain the load current without reducing the load voltage further. Whereas in the case of failure in 1 or 2 PV cells in the array, those cells can be removed in real time by reconfiguring the PV cells without degrading the performance of the system.



Fig 4-1 Reconfigurable solar cells using MOSFET switches

To illustrate the use of the MOSFET transistor for making the solar cell reconfigurable, let us take a simple example as shown in Fig 4-2. In this structure, the N-switches are Nchannel MOSFETs, which connects the PV cells to the ground, whereas the P-switches are P-channel MOSFETs that connect the PV cells to the positive terminal of the bus or with the load. The T-switch shown in Fig 4-2 is a transmission gate which lets two or more PV cells connect in series if it turns ON.



Fig 4-2 A set of PV cells connected to MOSFET switches

These three switches can be active by applying an appropriate voltage to the gate terminal which is presented in Table I.

Switch	ON	OFF
N-Switch	High	Low
P-Switch	Low	High
T-Switch	High	Low

Table I Condition for turning-ON or turning -OFF switches

Now consider a scenario such that the gate voltage V1 in Fig 4-2 is high. This will result in turning-ON of the N-Switch and P-Switch as per the Table I. Since T-Switch is OFF, the two PV cells will be connected in parallel. Now let's assume the gate voltage V1 is low;

this make the T-Switch to turn-ON but, at the same time, N-Switch and P-Switch will be OFF. This configuration will make the two PV cells connected in series.

4.1.1 Addressable switches for PV module by using SerDes

Each of the P-switches, N-switches, and T-switches are controlled by an Addressable Power Switch (APS) that includes a deseralizer, address decoder, and a control circuit. All of the APS are connected to a common clock, reset, and serial data. The PV panel structure with the APS is shown in Fig 4-3. The data packet consists of an address of the selected switch and 1-bit on/off signal for the N-switch, P-switch, and T-switch. The width of the address field is dependent on the number of PV cell in a module. Having common data signal connecting to each of the PV cells makes it easier to integrate CMOS-on-PV with a PV module.



Fig 4-3 Addressable Power Switch with SERDES

4.1.2 Hardware implementation of MOSFET switches and SerDes

4.1.2.1 Layout

To test the concept of the MOSFET based PV cells shown in Fig 4-4 a) a prototype IC was built in ON-Semi 0.5um technology node using L-edit tools by Tanner Tools. The IC had an Addressable power Switch (APS), N-type MOSFET, P-type MOSFET, and a transmission gate.



Fig 4-4 Prototype chip a) die photograph b) layout

4.4.2.2 Simulation result



Fig 4-5 Input voltages at the different switches



Fig 4-6 Output voltage and current at various switching states

4.1.3 Test setup and experiment result

4.1.3.1 Experiment result of testing SerDes circuit

The test results of the SerDes circuit is shown in Fig 4-7. To test the SerDes circuit, the control signals such as clock, bit sequence, and reset are generated from an FPGA board. Once the digital address of the switch matches the bit sequence received by the SerDes circuit a pulse is generated as can be seen in Fig 4-7 on probe no 1. This pulse then let the input signal at node D_4 in Fig 4-3 passed to the transmission gate that either turns it ON or OFF. The probe no 2 and 3 shown in the Fig 4-7**Error! Reference source not found.** are the input signal at node D_5 and D_0 respectively.



Fig 4-7 SerDes circuit test result

4.1.3.2 Reconfigurable PV module Test setup

In order to evaluate the influence of switches with solar cells at three 3 different voltages, 4.5V, 3.0V and 1.5V we measured the three set of 1.5V PV cells with and without the switches by connecting a variable resistor as load. For the load to operate at various voltages the input at the gate terminal of all the switches is shown in Table II. Table III shows which switches are turned-on or off the PV cells to connect in series or parallel. The "ON" or "1" in Table III means the transistor is operating in the linear/triode region whereas "OFF" or "0" means in cut-off region.

Table II Input signal at gate signal of the transistor

Voltage	S1N	S1P	S2	S3N	S3P	S4
4.5V	0	0	1	0	0	1
3.0V	0	1	1	1	1	1
1.5V	1	1	0	1	1	0

Voltage	S1N	S1P	S2	S3N	S3P	S4
4.5V	Off	On	Off	Off	On	Off
3.0V	Off	On	Off	On	Off	On
1.5V	On	Off	On	On	Off	On

Table III Control Table

We measured open load and short current of 3 sets 1.5V PV connected in series with and without the switches. For 4.5V measurements with switches first of all the S1N, S2, S3N, S4 are turned OFF whereas the S1P, S3P have turned ON then the switch SW was turned so that the load can be connected with PV cells. The load resistor is varied then accordingly current and the voltage across the load is measured which is shown in Fig 4-8 a).



a)



Fig 4-8 The reconfigurable PV cells a) block diagram b) switches S1 and S2 c) complementary switches S1N/S1P and S3N/S3P

4.1.3.3 Current vs Voltage characterization of PV cells with and without switches

As can be seen in Fig 4-9 the maximum current obtained with the switch is 0.42A. Because of the space constraints, the W/L of the P-Channel and N-Channel MOSFET's were made to support a small current.



Fig 4-9 I-V characteristics with switches a) Three PV cells in series b) three PV cells in parallel

4.2 Effect of the body current

In our previous work [17], we proposed a reconfigurable photovoltaic module for micro autonomous drones using addressable CMOS transistor, Addressable Programmable Switch (APS) is shown in Fig 4-10.



Fig 4-10 MOSFET based reconfigurable PV cells

As seen in Fig 4-10, the body of N-channel MOSFET (NMOS) based switch is connected to ground, whereas the body of the P-channel based MOSFET (PMOS) is connected to the load terminal. When the MOSFET is connected to an individual PV cell, then the system is able to create the desired power island since the voltage of the PV cell is less than the forward bias voltage of the diode. However, when more than one PV cell is connected in series to an individual NMOS or PMOS, the transistor does not turn-OFF even after applying an appropriate voltage to the gate terminal, as shown in Fig 4-11b). In a MOSFET, the current usually flows through the channel created under the gate terminal, once the appropriate voltage is applied to the gate terminal. In the case of an N-channel transistor, no current flows when the voltage at the gate terminal is low or is connected to the ground terminal. However, as can be seen in Fig 4-11, even when the gate terminal is connected to the ground, the current is still flowing through the body and source terminal due to the

forward biasing of the P and N+ substrates diode. Hence, it is very important to take into account the body connection when more than one PV cell are connected in series to an individual MOSFET. To resolve this issue, the cathode terminal of PV cell connected with body of NMOS whereas the body of PMOS should be connected to the anode terminal of the PV cell.



Fig 4-11 a) NMOS transistor when gate voltage is high or Vdd b) N-channel MOSFET when gate voltage is low or ground

4.3 Autonomous fault detection and mitigation architecture

The overall architecture for partial shading and complete shading detection and mitigation is shown in Fig 4-12. The PV module given in Fig 4-12 is the same reconfigurable PV module which was shown in Fig 4-10. For simplicity, we are using a resistive load, R_{load} . Additional resistors of $R_{Sh}=0.2 \Omega$ are connected in series with the load, resistance and acts as a current sensor to track the load current. The R_{sh} is also connected to the differential input of an operational amplifier based buffer. The output of the buffer is fed to an analog-to-digital converter. The analog-to-digital converter converts the voltage across the Rsh to a 14-bit digital value, V_{AD} , which is later compared with the expected voltage value by using (3) and based on the Np×Ns configuration of the PV module. If 14-bit signal V_{AD} is less than expected value of, Vpv, then the corrective data packet is sent serially to the PV module, along with the clock and reset signals.

$$V_o = I_{pv} \cdot R_{sh} \tag{29}$$

 $Power = P_{pv} = I_{pv} \cdot V_{pv} = I_{pv}^2 \cdot \left(R_{sh} + R_{load}\right) \quad (30)$



Fig 4-12 FPGA based feedback enable reconfigurable PV module for fault detection

4.4 Modified CMOS-on-PV based switches

However, switching the body connection to stop unwanted current flowing through the body creates an issue with NMOS of the PV cell. Even when the gate terminal of NMOS is connected to ground potential, the transistor continues to stay in the ON state. To illustrate this behavior, let's us consider an example as shown in Fig 4-13a).



Fig 4-13 a) N-Channel MOSFET connected in series with PV cell b) Spice simulation

Suppose, the PV cell has an open load voltage of 1.5V. Further, the threshold voltage, Vth of the NMOS is 0.9 V. The gate terminal of the NMOS is grounded. The voltage between the gate and the source terminal of the NMOS is given by:

Vgs = Vg - Vs = 0V - (-1.5V) = 1.5V

Since Vgs > Vth (0.9 V), the transistor will continue to stay ON even though the gate terminal is grounded. This can also be verified using SPICE simulation as shown in Fig 4-13 b). To turn OFF the transistor, a negative voltage must be applied to the gate terminal.

Now, let us assume a voltage of -1.5V is applied to the gate terminal; under this condition, Vgs is given by:

Vgs = Vg - Vs = -1.5V - (-1.5V) = 0V

Now, since $Vgs < V_t$, the transistor is turned OFF.

Taking into account the aforementioned phenomenon, to turn ON/OFF a PMOS, gate voltages of ground/ V_{DD} should be applied at the gate terminal respectively. Similarly, for an NMOS, a gate voltage of V_{DD} or ground/- V_{SS} should be applied to turn it ON/OFF respectively. The PV module

is controlled by an FPGA that emits a digital signal, data sequence, clock and reset as shown in Fig 4-12. Hence, the architecture presented in Fig 4-10 will not work with the feedback architecture presented in [9], [18], since the NMOS can be turned OFF only when a negative voltage is applied to the gate terminal. Hence, the n-channel MOSFET will always be ON. The P-channel MOSFET, however, can be turned ON/OFF by the digital signal "0" (0 V) or "1" (V_{dd}).

To resolve the above issue with NMOS, a modified PV module is proposed [51], as shown in Fig 4-14. The new architecture uses three different kinds of switches: P-switch or PMOS, N-switch or NMOS, and T-switch or transmission gate. A group of N-switches, P-switches, and T-switches have their own digital address which can only be activated by a SerDes circuit as shown in Fig 4-14 d). Compared to older schemes, this new SerDes circuit lets the user control all the three switches, T-Switch, N-Switch and P-Switch simultaneously. Further, the user can reconfigure the entire PV module three times faster. In the new scheme, the FPGA will send the data sequence, clock, reset, Vdd, and -Vss signals to the reconfigurable PV module.



Fig 4-14 a) Reconfigurable PV cells b) N-Switch and P-Switch c) T-Switch d) SerDes Circuit



Fig 4-15 Reconfigurable addressable CMOS-on-PV based PV module

4.5 Partial and complete shading detection algorithm

The important part of the algorithm is to distinguish between the faulty condition and partial or complete shading; the faulty PV cells can then be removed from the module permanently and the cells that are under partial lighting condition can be either removed or the entire module will be reconfigured temporarily for alleviating the effects of complete shading on the performance of PV module. The algorithm is presented in this section is for the PV module shown in Fig 4-15. The partial or complete shading detection algorithm start scanning when the $P_{measured}$ is not equal to the $P_{expected}$ as shown in Fig 4-16. Once the $P_{measured}$ goes outside the upper or lower bound, then the

FPGA board starts sending the data packet to the reconfigurable PV module so that affected PV cells can be detected and corrective action is taken.



Fig 4-16 Flow chart for initiating the partial/complete shading detection

4.5.1 Row search algorithm

Once the partial shading algorithms start searching for affected PV cells they first scan for the PV cells located at the boundary of the PV module. The reason for this start point is that, if shading is happening then, shading will certainly shield the PV cells located at the edges of the PV module. Once the affected PV cell at the edge is found, PV cell will be removed temporarily. Next, the cells located adjacent to the affected PV cells are checked for the partial shading condition. If they are under partial shading condition then they, too, are either removed from the module or the overall configuration of the module is altered by sending appropriate data packet by the FPGA. There might also be a case when a $P_{measured}$ is not equal to the $P_{expected}$ due to faulty PV cells located at the edges of the PV module. To address this issue, the algorithm will try (after fixed timed delay) to bring back the PV cell that was previously removed due to partial shading from the module. Once

partial shading condition, such as a shadow of objects nearby or clouds covering the PV module partially, is no longer there then, the previously removed PV cells can be reconnected to the PV module using the three switches. Since faulty PV cells such as those damaged physically or open circuit /short circuits in connections of individual PV cells cannot be fixed without human intervention, they will never be able to satisfy the $P_{measured}$ equal to the $P_{expected}$ requirement. Therefore, the faulty PV cells located at the edge of the PV module, even when the algorithm recognizes them as cells under partial shading, they will never be connected back with healthy PV cells in the module. Since we are using only eight PV cells and all of them are at the edge of the PV modules, each of them can be under partial shading condition. Therefore, interactively, each of them will be checked one by one for partial shading condition.

Once the FPGA board receives the signal to initiate the boundary scan algorithm, it starts sending the corrective data packet to the reconfigurable PV module. These data packets are such that each row is removed, one at a time, and then, for that configuration, the $P_{expected}$ is compared with the $P_{measured}$ result. If they are same then that row is placed back into the module and the iteration is increased by Ns in accordance with the flow chart for the row search in Fig 4-17. To understand the row search let us assume that we have a 4×2 PV cell matrix. The FPGA controller receives a signal indicating the presence of a PV cell under shade; consequently a row search algorithm is initiated shown in Fig 4-17.



Fig 4-17 Flow chart for the row search

Since, Ns=2, the FPGA controller sends a data sequence that turns off the N-switch at APS switch with an address of 2. Then, based on Np and Ns-1, $P_{calculated}$ will be generated. $P_{measured}$ is compared with the $P_{calculated}$. If $P_{measured}$ = $P_{calculated}$ then faulty PV cell is between 2 and 2-Ns. Otherwise, the counter *i*, will be incremented by Ns and the same steps will repeat until the end of the PV module

is reached. If shaded PV cells are found in a row then the column search algorithm is initiated and neighboring PV cells will be scanned for the presence of partial shading conditions.



Fig 4-18 Illustration of Row search algorithm

4.5.2 Columns search algorithm

The column search algorithm starts from the faulty row detected by the row search algorithm. The algorithm first removes the faulty row from the PV module. Then one by one the cells from the faulty row are connected with the PV cells from the next adjacent row in accordance with the column search flow chart shown in Fig 4-19. At each step, the $P_{measured}$ is compared with the $P_{calculated}$; if these are found to be equal, then, using the shifting approach described previously, the next cell from the faulty row will be added to the adjacent healthy PV module row. This step will continue until $P_{measured}$ is not equal to the $P_{calculated}$. Once such condition is reached the last added PV cell is determined to be faulty.



Fig 4-19 Flow chart for finding PV cell under shade in a row

4.5.3 Complete shading detection and mitigation algorithm

During the search for partial shaded cells with each row, it might happen that more than one row in the module has PV cells under shade. If these are that removed from the PV module, then the performance of the PV module will be affected very badly! Therefore, depending on the kind of load (high voltage with low current or high current with low voltage), the reconfigurability will be done accordingly as per the flow chart is shown in Fig 4-20.



Fig 4-20 Flow chart for complete shading based on load requirement

4.6 SPICE simulation results

To better understand the effectiveness of the partial and complete shading algorithms presented in this work we did SPICE simulation by extracting the netlist of the switches using Tanner tools and build the PV cells SPICE model by extracting the Rs, Rp, Iph and Is of the diode by employing curve fitting techniques. Next, the Iph of the affected PV cells was incorporated into the PV cells model to simulate partial shading effect on PV module's performance. In Fig 4-21, we the results of the simulation configuration for PV arrays arrangement from 4x2 to 2x4 without affecting the overall performance of the PV module.



Fig 4-21Simulation result for the PV module of configuration 4x2 when all of PV cells are under shade

4.7 Summary

In this chapter, we presented a novel mechanism that can stop the flow of unwanted current through the body terminal of the MOSFET. This flow of unwanted current does not let the switch turn-OFF a PV cell in an array. This novel architecture can be integrated monolithically with the PV cells, thereby creating reconfigurable power islands of variable levels. Additionally, an algorithm to detect partial shading is also presented. Using this kind of architecture we showed how the PV module can be reconfigured based on load requirements scenarios of high voltage with low current or high current with low voltage.

Chapter 5.

5.1 Conclusion

A Photovoltaic (PV) module can have many faults or defects, such as: short/open connection, physical cell damage, bypass diode failure and others. Compared with bypass diode alone, it is shown that use of a MOSFET switch instead of a diode can address most of these issues. In this dissertation, we investigated techniques to build a fault resilient PV module. This kinds of fault tolerant PV modules had PV cells integrated with CMOS based switches that have its own digital address.

The major contribution of this dissertation work is following:

- Typically, single-diode, double-diode or three-diode models are used for modelling solar cells. Since diodes have an exponential term in their current equation, the computation of output power of PV module becomes very power intensive and difficult to implement on an embedded system. To resolve this issue, a novel N-channel MOSFET based PV module modelling technique is presented in the dissertation. This new method yields a close form solution for calculating output current based on the output voltage, temperature, and irradiation, which was previously not possible.
- 2. A newer reconfigurable PV module architecture is presented in this dissertation. The previously presented reconfigurable PV module scheme suffered from the unwanted flow of body current through the MOSFET. This lead to the MOSFET transistor, not turning-OFF. Moreover, the time taken to reconfigure the PV module was much slower since each switch in the module had its own digital address. Therefore, in this dissertation, a newer and faster SerDes circuit is being presented. Additionally, a new kind of switches are presented that
doesn't have unwanted body current and it can be integrated with a feedback enable fault detection algorithm.

3. Additionally, an efficient algorithm to detect faulty cells in a PV module in real time is developed. This helps in preventing load performance degradation in case of failure or partial shading of individual or group of cells in an array.

5.2 Future Works

Since, in this dissertation, mostly silicon-based PV modules are being used, whereas for space application III-V based PV cells are used, more extensive experimental analysis should be done before deployment of this approach in space application. The MOSFET based PV module technique is presented in this work will be very useful if it is integrated with the fault detection as well as partial shading detection algorithm.

Also, for increasing the reliability of the connection between PV cells and MOSFET transistor, monolithically growing them on the same substrate is desirable. Therefore, a process development plans should be established for growing such kinds of architecture.

Additionally, for the fault detection and mitigation an on-field computing architecture is presented. But that means the embedded system needs to continuously measure the output power and compared it with the computed power. Although this is a solid technique, it can result in an embedded system consuming a good deal of power. Instead, an embedded system, where the present power performance can be compared with the previously measured power performance will be much more beneficial.

In this dissertation, building of a MPPT algorithm for a battery and PV module working together is ignored. Since the battery synching with the PV module is not required. However, there are

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some applications where they are a necessity. Therefore, an MPPT algorithm which combines the reconfigurable PV module and the battery can also be explored.

REFERENCES

- [1] IEA, "Technology Roadmap Solar Photovoltaic Energy," International Energy Agency, 2014.
- [2] S. Pillai, K. R. Catchpole, T. Trupke, and M. A. Green, "Surface plasmon enhanced silicon solar cells," *J. Appl. Phys.*, vol. 101, no. 9, p. 93105, May 2007.
- [3] M. Pagliaro, R. Ciriminna, and G. Palmisano, "Flexible Solar Cells," *ChemSusChem*, vol. 1, no. 11, pp. 880–891, Nov. 2008.
- [4] G. Li, R. Zhu, and Y. Yang, "Polymer solar cells," *Nat. Photonics*, vol. 6, no. 3, pp. 153–161, Mar. 2012.
- [5] M. Boxwell, Solar Electricity Handbook 2015 Edition: A simple, practical guide to solar energy - designing and installing solar PV systems., 2015 Edition edition. Coventry: Greenstream Publishing, 2015.
- [6] Y. Zhao, "Fault analysis in solar photovoltaic arrays," 2010.
- [7] X. Lin, Y. Wang, M. Pedram, J. Kim, and N. Chang, "Designing Fault-Tolerant Photovoltaic Systems," *IEEE Des. Test*, vol. 31, no. 3, pp. 76–84, Jun. 2014.
- [8] Y. Wang, X. Lin, Y. Kim, N. Chang, and M. Pedram, "Enhancing efficiency and robustness of a photovoltaic power system under partial shading," in 2012 13th International Symposium on Quality Electronic Design (ISQED), 2012, pp. 592–600.
- [9] J. West, S. Imani, O. Lavrova, W. Cavanaugh, J. Ju, K. Pupuhi, S. Keshavmurthy, J. Aarestad, and P. Zarkesh-Ha, "Reconfigurable power management using novel monolithically integrated CMOS-on-PV switch," in *Photovoltaic Specialist Conference (PVSC), 2014 IEEE 40th*, 2014, pp. 1389–1392.
- [10] "PVEducation." [Online]. Available: http://pveducation.org/. [Accessed: 10-Apr-2016].

- [11] S. Fahrenbruch, "Solar Bypass Diodes: Then and Now," Solar: A PV Management Magazine, 2010.
- [12] N. G. Dhere, N. Shiradkar, E. Schneller, and V. Gade, "The reliability of bypass diodes in PV modules," 2013, vol. 8825, p. 88250I–88250I–8.
- [13] G. Bhattacharya and C. Neogy, "Removal of the hot-spot problem in photovoltaic modules and arrays," *Sol. Cells*, vol. 31, no. 1, pp. 1–12, Feb. 1991.
- [14] J. K. Mathew, J. Kuitche, and G. TamizhMani, "Test-to-failure of PV modules: Hotspot testing," in 2010 35th IEEE Photovoltaic Specialists Conference (PVSC), 2010, pp. 002839– 002843.
- [15] G. TamizhMani and S. Sharma, "Hot spot evaluation of photovoltaic modules," 2008, vol. 7048, p. 70480K–70480K–7.
- [16] N. A. Al-Rawi, M. M. Al-Kaisi, and D. J. Asfer, "Reliability of photovoltaic modules II. Interconnection and bypass diodes effects," *Sol. Energy Mater. Sol. Cells*, vol. 31, no. 4, pp. 469–480, Jan. 1994.
- [17] R. Mahto, O. Lavrova, P. Zarkesh-Ha, and L. Lester, "Reconfigurable and Programmable Photovoltaic Power for Micro Autonomous Systems," in *ReSpace/MAPLD 2010*, Albuquerque, NM, 2010.
- [18] R. Mahto, P. Zarkesh-Ha, and O. Lavrova, "Reconfigurable Power Management for Monolithic CMOS-on-Photovoltaic under Partial and Complete Shading," in *Reliability Physics Symposium*, 2016 IEEE International, 2016.
- [19] X. Lin, Y. Wang, D. Zhu, N. Chang, and M. Pedram, "Online fault detection and tolerance for photovoltaic energy harvesting systems," in 2012 IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2012, pp. 1–6.

- [20] Y. Wang, X. Lin, Y. Kim, N. Chang, and M. Pedram, "Enhancing efficiency and robustness of a photovoltaic power system under partial shading," in 2012 13th International Symposium on Quality Electronic Design (ISQED), 2012, pp. 592–600.
- [21] K.-H. Chao, P.-Y. Chen, M.-H. Wang, C.-T. Chen, K.-H. Chao, P.-Y. Chen, M.-H. Wang, and C.-T. Chen, "An Intelligent Fault Detection Method of a Photovoltaic Module Array Using Wireless Sensor Networks, An Intelligent Fault Detection Method of a Photovoltaic Module Array Using Wireless Sensor Networks," *Int. J. Distrib. Sens. Netw. Int. J. Distrib. Sens. Netw.*, vol. 2014, 2014, p. e540147, May 2014.
- [22] W. Xiao, W. G. Dunford, and A. Capel, "A novel modeling method for photovoltaic cells," in *Power Electronics Specialists Conference*, 2004. PESC 04. 2004 IEEE 35th Annual, 2004, vol. 3, p. 1950–1956 Vol.3.
- J. Ma, K. L. Man, T. O. Ting, N. Zhang, S.-U. Guan, P. W. H. Wong, J. Ma, K. L. Man, T. O. Ting, N. Zhang, S.-U. Guan, and P. W. H. Wong, "Approximate Single-Diode Photovoltaic Model for Efficient I-V Characteristics Estimation, Approximate Single-Diode Photovoltaic Model for Efficient I-V Characteristics Estimation," *Sci. World J. Sci. World J.*, vol. 2013, 2013, p. e230471, Nov. 2013.
- [24] Y. Mahmoud, W. Xiao, and H. H. Zeineldin, "A Simple Approach to Modeling and Simulation of Photovoltaic Modules," *IEEE Trans. Sustain. Energy*, vol. 3, no. 1, pp. 185– 186, Jan. 2012.
- [25] M. G. Villalva, J. R. Gazoli, and E. R. Filho, "Comprehensive Approach to Modeling and Simulation of Photovoltaic Arrays," *IEEE Trans. Power Electron.*, vol. 24, no. 5, pp. 1198– 1208, May 2009.

- [26] J. A. Gow and C. D. Manning, "Development of a photovoltaic array model for use in power-electronics simulation studies," *Electr. Power Appl. IEE Proc.* -, vol. 146, no. 2, pp. 193–200, Mar. 1999.
- [27] H. Tsai, C. Tu, and Y. Su, "Development of Generalized Photovoltaic Model Using MATLAB/SIMULINK," in *Proceedings of the World Congress on Engineering and Computer Science 2008*, San Francisco, USA, 2008.
- [28] H. N. Mohamed and S. A. Mahmoud, "Modeling photovoltaic modules using N-channel MOS transistor," in 2013 IEEE 20th International Conference on Electronics, Circuits, and Systems (ICECS), 2013, pp. 743–746.
- [29] H. N. Mohamed and S. A. Mahmoud, "Novel Circuit Model of the Photovoltaic Modules Based on N-Channel MOS Transistor," in *Modelling Symposium (EMS), 2013 European*, 2013, pp. 396–401.
- [30] H. Park and H. Kim, "PV cell modeling on single-diode equivalent circuit," in *IECON* 2013 39th Annual Conference of the IEEE Industrial Electronics Society, 2013, pp. 1845–1849.
- [31] K. Ishaque, Z. Salam, and H. Taheri, "Simple, fast and accurate two-diode model for photovoltaic modules," *Sol. Energy Mater. Sol. Cells*, vol. 95, no. 2, pp. 586–594, Feb. 2011.
- [32] Z. Salam, K. Ishaque, and H. Taheri, "An improved two-diode photovoltaic (PV) model for PV system," in 2010 Joint International Conference on Power Electronics, Drives and Energy Systems (PEDES) 2010 Power India, 2010, pp. 1–5.
- [33] K. Nishioka, N. Sakitani, Y. Uraoka, and T. Fuyuki, "Analysis of multicrystalline silicon solar cells by modified 3-diode equivalent circuit model taking leakage current through

periphery into consideration," Sol. Energy Mater. Sol. Cells, vol. 91, no. 13, pp. 1222–1227, Aug. 2007.

- [34] E. Gadjeva and M. Hristov, "Generalized SPICE model of photovoltaic modules," in *Mixed Design of Integrated Circuits Systems (MIXDES)*, 2015 22nd International Conference, 2015, pp. 476–480.
- [35] Y. Jiang, J. A. A. Qahouq, and M. Orabi, "Matlab/Pspice hybrid simulation modeling of solar PV cell/module," in 2011 Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), 2011, pp. 1244–1250.
- [36] Krismadinata, N. A. Rahim, H. W. Ping, and J. Selvaraj, "Photovoltaic Module Modeling using Simulink/Matlab," *Procedia Environ. Sci.*, vol. 17, pp. 537–546, 2013.
- [37] J. Luther, S. Guo, F.-J. Ma, B. Hoex, A. G. Aberle, and M. Peters, "Analysing Solar Cells by Circuit Modelling," *Energy Procedia*, vol. 25, pp. 28–33, Jan. 2012.
- [38] L. Castañer and S. Silvestre, *Modelling Photovoltaic Systems Using PSpice*. John Wiley & Sons, 2003.
- [39] D. Iero, R. Carbone, R. Carotenuto, C. Felini, M. Merenda, G. Pangallo, and F. G. D. Corte,
 "One-shot SPICE simulation of photovoltaic modules, storage elements, inverter and load," in
 2015 AEIT International Annual Conference (AEIT), 2015, pp. 1–4.
- [40] J. L. Díaz-Bernabé and A. Morales-Acevedo, "Photovoltaic module simulator implemented in SPICE and Simulink," in 2015 12th International Conference on Electrical Engineering, Computing Science and Automatic Control (CCE), 2015, pp. 1–5.
- [41] S. Lun, C. Du, T. Guo, S. Wang, J. Sang, and J. Li, "A new explicit I–V model of a solar cell based on Taylor's series expansion," *Sol. Energy*, vol. 94, pp. 221–232, Aug. 2013.

- [42] S. Lun, C. Du, J. Sang, T. Guo, S. Wang, and G. Yang, "An improved explicit I–V model of a solar cell based on symbolic function and manufacturer's datasheet," *Sol. Energy*, vol. 110, pp. 603–614, Dec. 2014.
- [43] M. Wang and R. Zhao, "Practicable approaches to predicting PV array model parameters and I-U characteristics based on datasheet," *Renew. Energy Resour.*, vol. 30, no. 3, pp. 102– 107.
- [44] R. Mahto, P. Zarkesh-Ha, and O. Lavrova, "MOSFET-Based Modeling and Simulation of Photovoltaics Module," in 2016 IEEE 43rd Photovoltaic Specialist Conference (PVSC), Portland, OR, 2016.
- [45] H. N. Mohamed and S. A. Mahmoud, "Modeling photovoltaic modules using N-channel MOS transistor," in 2013 IEEE 20th International Conference on Electronics, Circuits, and Systems (ICECS), 2013, pp. 743–746.
- [46] X. Lin, Y. Wang, D. Zhu, N. Chang, and M. Pedram, "Online fault detection and tolerance for photovoltaic energy harvesting systems," in 2012 IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2012, pp. 1–6.
- [47] X. Lin, Y. Wang, M. Pedram, and N. Chang, "Optimal switch configuration design for reconfigurable photovoltaic modules," in 2014 IEEE PES General Meeting | Conference Exposition, 2014, pp. 1–5.
- [48] R. T. Howe and C. G. Sodini, *Microelectronics: an integrated approach*. Prentice Hall Upper Saddle River, NJ USA:, 1997.
- [49] L. Lester, K. Yang, M. El-Emawy, T. Saiz, R. Clark, A. Hollowell, and O. Lavrova, "Solar power for unmanned autonomous vehicles | SPIE Homepage: SPIE."

- [50] A. M. Imtiaz and F. H. Khan, "Light-Generated Effects on Power Switches Used in a Planar PV Power System With Monolithically Embedded Power Converters," *IEEE J. Photovolt.*, vol. 3, no. 1, pp. 394–400, Jan. 2013.
- [51] R. Mahto, P. Zarkesh-Ha, and O. Lavrova, "Reconfigurable Photovoltaic Integrated with CMOS for a Fault Tolerant System," in 2016 IEEE 43rd Photovoltaic Specialist Conference (PVSC), Portland, OR, 2016. (accepted)