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Microcontroller (8051-core) instruction susceptibility to intentional electromagnetic interference (IEMI)

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THESIS

Submitted in Partial Fulfillment of the
Requirements for the Degree of

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The University of New Mexico
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DEDICATION

For Ashley and Eloise.

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ABSTRACT OF THESIS

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ABSTRACT

Intentional Electromagnetic Interference (IEMI) is a rising threat to the electronic systems that are used and depended upon in everyday life of civil society. To address this threat, it is important to develop an understanding of what IEMI is and how it can be used to disrupt sophisticated electronic systems. By understanding IEMI and its disruptive effects, predictive models and protection standard can be developed for various types of electronic systems to address the threat.

The focus of this thesis is to detail the experimental results involved when investigating the susceptibility of a single microcontroller instruction. A microcontroller represents a system on a chip and provides an ideal starting point for developing a predictive model for the upset effects that can be caused by an IEMI attack on a digital system. The microcontroller device used in the experiment is the ATMEL AT89LP2052, which is an 8051-core based microcontroller device that processes instructions in parallel. The experiment involves targeting specific moments within an instruction cycle, based on the parallel processing of the LP2052, to determine whether or not different actions within the cycle have different susceptibility levels to IEMI.

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Chapter 1 The Threat of IEMI

1 Introduction and Background

The primary purpose of this thesis is to develop a better understanding of the upset mechanisms of a microcontroller when it is injected with an intentional electromagnetic interference signal (IEMI). The susceptibility of the different actions processed within an assembly instruction will be measured on a microcontroller of the 8051-core family – the ATMEL AT89LP2052. To understand why this microcontroller upset investigation is necessary, an overview of high-power electromagnetics (HPEM) and IEMI is presented in this introductory chapter.

IEMI is a rising threat to the electronic systems that are used and depended upon in everyday life of civil society. To address this threat, it is important to first develop an understanding of what IEMI is and how it can be used to disrupt sophisticated electronic systems. The recent Special Issue of the IEEE Transactions on Electromagnetic Compatibility on HPEM and IEMI [1-16] provides an excellent overview on the disruptive nature of HPEM and IEMI.

In recent years, the scientific community has decided to promote IEMI as being defined as: “The intentional malicious generation of electromagnetic energy introducing noise or signals into electric and electronic systems, thus disrupting, confusing, or damaging these systems for terrorist or criminal purposes” [17]. The special issue is divided into four topic areas: 1.) IEMI waveform classification and generation capabilities [2-4], 2.) The coupling process as applied to cables and systems [5-7], 3.) The effects of IEMI on equipment, system and communications [8-13], and 4.) Protection, measurements and standards related to IEMI and HPEM [14-16]. As an introduction to

the special issue, Radasky et al. [1] provides a brief description of each topic areas being addressed, beginning with past incidents involving HPEM effects.

Reviewing historical effects of HPEM on electronic systems, various incidents involving electromagnetic interference (EMI) have occurred in the military, the automobile industry, and in the medical care business. In 1967, one of the most severe cases of EMI occurred on the USS Forrestal. A military aircraft was exposed to the ship's radar as it was landing on the carrier. This exposure caused the aircraft to accidently fire its munitions into the ship, causing severe carrier damage and resulting in 134 deaths. In the automobile industry, EMI caused problems in antilock braking systems (ABS) when they were first introduced. On the autobahn in Germany, EMI from nearby radio transmitters caused the brakes to apply on passing autos. In the medical care industry, a radio transmitter in an ambulance caused the monitor and defibrillator to shut down every time it was used, resulting in the death of a 93-year-old heart attack victim [1, 18].

Radasky et al. [1] highlights many reasons to be concerned about the impacts of IEMI on society. To help spread awareness of these concerns, the International Radio Scientific Union (URSI) created the "Resolution of Criminal Activities using Electromagnetic Tools" in 1999. The URSI council provided recommended actions for the scientific community and, specifically, the EMC community to undertake on account of this threat. Each individual topic area of the "Special Issue" will now be discussed in detail to describe the overall threat of IEMI. Emphasis will be placed on the topic areas that directly relate to how the microcontroller upset investigation fits within this broad overview.

1.1 Classification and Capabilities to Generate IEMI Waveforms

The first step in understanding the threats posed by IEMI to electronic equipment is to become familiar with the different types of intentional electromagnetic environments (IEME) that exist and the various worldwide capabilities that exist to generate these IEMEs. Chapter 1.1.1 will provide an overview on different IEMEs and Chapter 1.1.2 will provide details on the various capabilities that exist to generate these waveforms, along with a survey of worldwide wideband capabilities.

1.1.1 Electromagnetic Environments

When it comes to intentional electromagnetic environments (IEME), Giri et al. [2] describes three categories of classification: 1.) Classification based on environmental attributes, 2.) Classification in terms of HPEM source technology, and 3.) Classification in terms of system effects. Classification in terms of environmental attributes is the preferred method to describe IEME. This is because environmental attributes are quantitative measurements, whereas the other two methods tend to be subjective in measurement.

When looking at environmental attributes, Figure 1 provides a comparison of different EM environments based on spectral density versus frequency [19]. Natural occurring phenomena such as lightning is the most common cause of malfunction to commercial electronics. Surge protectors and lightning rods can be used in these environments to help minimize the effects caused by these types of EM environments. Another area to be concerned with are the HPEM environments. These types of environments are intentionally caused to disrupt electronic systems, hence the name

IEME. The two major categories of HPEM environments are narrowband and wideband [2].

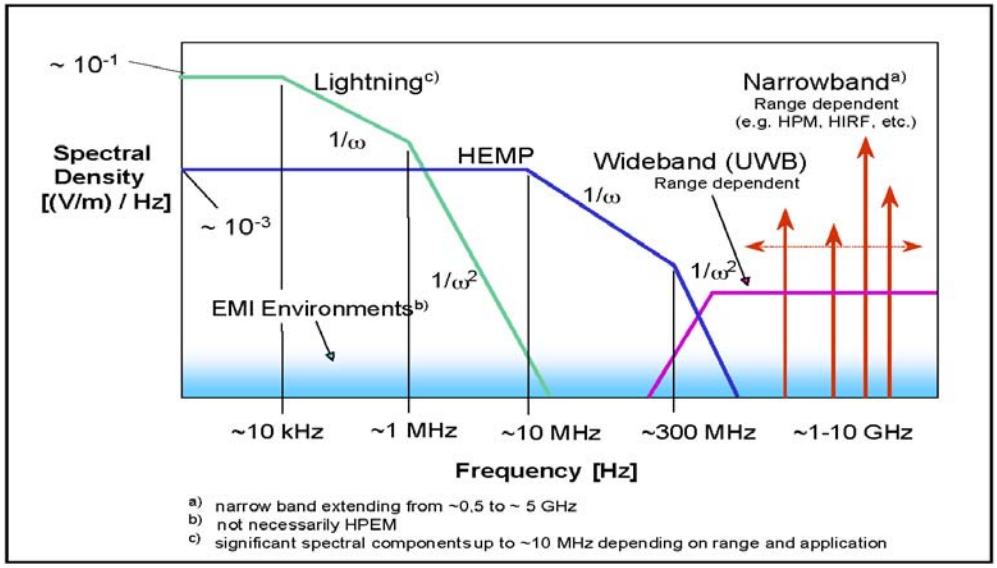

Figure 1. EM environments based on spectral density as a function of frequency. The narrowband and wideband environments are the two major categories in terms of HPEM (from [19]).

In the first category of HPEM environments, a narrowband waveform can be described as “nearly a single frequency… of power delivered over a fixed time frame” [1]. In general, experiments in narrowband environments have shown that electronic systems appear to be the most vulnerable to radiated fields in the frequency band between 0.2 and 5 GHz. This bandwidth of common vulnerability is often referred to as high-power microwaves (HPM).

In the second category, a wideband environment can be described as “one in which a time domain pulse is delivered, often in a repetitive fashion. The term ‘wideband’ indicates that the energy in the waveform is produced over a substantial frequency range relative to the ‘center frequency’” [1]. Furthermore, to better describe various wideband waveforms, subcategories have been defined based on the bandratio of a waveform.

To characterize wideband waveforms in terms of bandwidth, four definitions have been proposed for bandwidth classification based on the frequency content of the IEME spectral densities [2]. These bandwidth classifications are narrowband, moderate band, ultramoderate band, and hyperband, where this terminology is consistent with the IEC 61000-2-13 Standard, "EMC, high-power electromagnetic (HPEM) environments—radiated and conducted (draft)." Table I provides the classification of IEME based on bandwidth. The bandratio br is defined as: $br = \frac{f_h}{f_l}$, where f_h is the upper frequency limit and f_l is the lower frequency limit of the wideband waveform.

Table I. IEME classifications based on frequency content of the IEME spectral densities (from [2]).

Band type	**Percent bandwidth** $pbw = 200\left(\frac{br-1}{br+1}\right)$ (%)	**Bandratio** ***br***
Narrow or hypoband	$< 1\%$	< 1.01
Moderate or mesoband	$1\% < pbw \leq 100\%$	$1.01 < br \leq 3$
Ultra-moderate or sub-hyperband	$100\% < pbw < 163.4\ \%$	$3 < br \leq 10$
Hyperband	$163.4\% < pbw < 200\%$	$br \geq 10$

In terms of system vulnerabilities, the narrowband threat can be described as one of very high power in which the electrical energy is contained in a narrow frequency band. Comparatively, the wideband threat can be described as one of much less power in which the energy is spread out across many frequencies. Damage is much more likely to occur to electronic systems in the narrowband case, but vulnerabilities are easier to identify in the wideband case [1].

Another way to characterize IEME attributes produced by an HPEM source is to "examine the electric field (E-field) strength at a specified distance from the source, the frequency agility of the source, the duration and repetition rates for pulsed sources, and the burst lengths." As an example of this type of characterization, Table II provides the aperture E-field and the far-field voltage for two antenna power levels for an assumed aperture area of A=10 m^2. From Table II, the electric field levels as a function of frequency and range can be estimated, leading to the results shown in Table III. From these results, consideration can be given to the possible effects that can be induced on illuminated systems at the various ranges and which frequency range will be likely to cause the most damage.

Table II. Aperture fields and far voltages. This table shows the aperture E-field and the far voltage for two antenna power levels for an aperture area of A=10 m^2 (from [2]).

Qty.	Peak Power = 2 kW				Peak Power = 20 MW			
	0.5 GHz	1 GHz	2 GHz	3 GHz	0.5 GHz	1 GHz	2 GHz	3 GHz
Aperture field E_o	274 V/m	274 V/m	274 V/m	274 V/m	27.4 kV/m	27.4 kV/m	27.4 kV/m	27.4 kV/m
Far voltage $r E_f$	4.57 kV	9.13 kV	18.27 kV	27.40 kV	457 kV	913 kV	1.83 MV	2.74 MV

Table III. Range of radiated E-field at various frequencies and two different power levels. This can help to identify frequency ranges that are likely to cause the most damage (from [2]).

Frequency	Range	Antenna aperture of 10 m^2 and output power of 2 kW	Antenna aperture of 10 m^2 and output power of 20 MW
500 MHz	300m 1km	15.23 V/m 4.57 V/m	1.52 kV/ m 457 V/m
1 GHz	300 m 1 km	30.43 V/m 9.13 V/m	3.04 kV/m 913 V/m
2 GHz	300m 1km	60.90 V/m 18.27 V/m	6.09 kV/m 1.83 kV/m
3 GHz	300m 1km	91.33 V/m 27.40 V/m	9.13 kV/m 2.74 kV/m

A second way to classify IEME is in terms of source technology. The sophistication and technologies required in producing an EM environment can vary in level such as low, medium, and high-tech generator systems. A low-tech HPEM source is characterized by having a marginal performance, minimal technical capabilities, and is easily assembled and deployable. A medium-tech system will most likely require the skills of an electrical engineer, along with acquiring fairly sophisticated components to modify into an HPEM source, such as a commercially available radar. A high-tech HPEM source would require specialized and sophisticated technologies to develop and may be used to cause severe damage to specific targets. Giri et al. [2] provides detailed examples for each sophistication level of source technology.

A third IEME classification approach is to classify the IEME by the type of effects the environment might have on a system. These effects could include generating noise in a receiver, sending false information to a receiver, affecting the logic state of an electronic component (transient upset), or permanent damage. More details on these upset effects are provided in [2].

1.1.2 Worldwide Capabilities to Generate HPEM Waveforms

To provide a general idea of capabilities that exist to generate HPEM waveforms, a quick overview of four European HPM narrow-band test facilities is provided. These facilities are used to study the technical feasibility of HPM source technologies, along with assessing RF susceptibility of electronic systems, RF interference coupling behaviors, and RF induced effects [3].

The first test facility overview is that of the Swedish Microwave Test Facility (MTF), which was designed to test aircraft against high-intensity radiated fields. The

characteristic parameters of the MTF are summarized in Table IV. It should be noted that not all of the maximum characteristics within Table IV can be attained simultaneously.

Table IV. Characteristic parameters of the MTF (from [3]).

Radar Band	L	S (PCS)	C	X	Ku
f (GHz)	1.30	2.86	5.71	9.30	15.00
Max. Average power (kW)	49	20	5	1	0.28
Max. power (MW)	25	20 (140)	5	1	0.25
Max. PRF (pps)	1000	1000	1000	1000	2100
Max. Pulse duration (μs)	5	5 (0.4)	5	3.8	0.53
Epeak@15 m (kV/m)	30	30 (80)	17	10	6

PCS: Pulse Compression System

A second high-power microwave test facility worth evaluating is the Orion HPM test facility. Orion is located in the UK and uses four tunable magnetrons to generate HPM radiation over a tunable bandwidth of 1 to 3 GHz. The specifications for Orion are outlined in Table V [3].

Table V. Characteristic parameters of Orion (from [3]).

Parameter	Specification
Peak power (Pulse Power System)	5 GW
HF-Source	Magnetron
Frequency	1 – 3 GHz
Pulse duration	100 – 500 ns
PRF	Single Shot to 100 Hz
Burst Duration	10 s (Maximum)
Inter Burst Delay	8 minutes (Minimum)

Hyperion, located in France, is the third HPM test facility to be evaluated. Hyperion was designed to test systems such as airplanes against homogeneous

microwave beams and has a continuously tunable bandwidth from 0.72 to 3.0 GHz. The characteristic parameters for Hyperion are shown in Table VI.

Table VI. Characteristic parameters of Hyperion (from [3]).

Parameter	Specification
HF-Source	Magnetron
Frequency	1.3 – 1.8 GHz 2.4 – 3.0 GHz
Pulse duration	100 ns
Epeak	60
HF-Source	Reltron
Frequency	0.72 – 1.44 GHz
Pulse duration	200 ns
PRF	1 Hz
Epeak	40 kV/m

Supra is the fourth HPM test facility looked into, and it is located in Germany. The Supra test chamber accommodates the testing of full size cars, small tanks, or shelters. Table VII provides the characteristic parameters of Supra.

Table VII. Characteristic parameters of Supra (from [3]).

Parameter	Specification
HF-Source	4 Super Reltrons (8*)
Frequency	0.675 –1.44 GHz (3 GHz*)
Pulse Duration	> 300 ns
Epeak @ 15 m	70 kV/m (45 kV/m *)
RF Peak Power	400 MW – 200 MW (100 MW *)
PRF	10 Hz
Max. Shots / Burst	100
3dB Illumination Area	12 m^2 (9 m^2*)

* 2005 Upgrade

When it comes to further developments in HPM test facilities, the maximum generated power that is reached can be attributed to a combination of different limitations. These limitations are the result of limiting parameters such as RF breakdown,

beam guidance and focusing, and cathode design. The cathode is one of the most critical components of an HPM source and its optimization has been the primary focus of recent research activities [3].

Examples of various wideband sources are provided by Prather et al. [4], along with a discussion on the limitations of wideband test facilities. For wideband testing, various advantages and limitations exist between indoor test facilities and outdoor testing. Suitable indoor wideband test facilities include anechoic chambers, two-conductor transmission lines, and transverse electromagnetic (TEM) cells. For an anechoic chamber, the primary limitation is that they usually cannot accommodate an ultrawide signal in the low-frequency band. For a two-conductor transmission line, efficient use is made of generator voltages, but radiating fringe fields may cause problems for nearby electronics or personnel. A three-conductor transmission line can be used to reduce the fringing fields from the two-conductor setup and a TEM cell can be used when absolutely no radiation from the experiment is allowed.

By acquiring a proper frequency clearance, wideband HPM testing can also be performed on an outdoor test range [4]. Outdoor ranges are preferable for wideband HPM testing because they provide the most realistic environment for the source and the device under test.

Radiated IEME has been the primary topic of this section, but IEME signals can also be conducted. These conducted signals are a potential threat to electronic systems connected to power lines and communication lines. From outside a building, the HPEM conducted pulsed voltages and currents can be transmitted to the inside of a building and disrupt the electronic equipment. Additionally, the conducted HPEM signal can be

directly injected onto a transmission line or it can be coupled onto the line from a radiated HPEM signal [3]. The coupling process as applied to cables and systems will be described in the next section, where radiative and conductive coupling will both be covered.

1.2 The Coupling Process as Applied to Cables and Systems

When applying a disruptive waveform into a system, two primary delivery methods exist: radiated and conducted. Through radiated fields, frequencies above 100 MHz tend to penetrate through poor shielding and couple into the systems most efficiently. Thus, fields in this upper frequency band, which includes HPM, are of primary concern. On the other hand, conducted signals below 10 MHz are of primary concern. This is because a conducted signal propagates more efficiently at lower frequencies compared to higher frequencies [1].

New propagation models for electromagnetic waves along uniform and nonuniform cables were introduced by Haase et al. [5]. Having knowledge of and being able to mathematically describe coupling paths of EM energy is an important area in HPEMs. An extension to the usual transmission-line theory, the transmission-line super theory (TLST), can be used as a way to achieve the mathematical description of the coupling paths.

To provide an overview of TLST, Haase et al. [5] explain the derivation of the generalized telegrapher equations and TLST by dividing the primary procedure into three parts. “First, the mixed-potential integral equation is set up… Second, a trial function for the current is introduced… Third, these integral equations are solved iteratively to calculate the parameters and source terms for an actual transmission-line geometry” [5].

This method can achieve acceptable results at a fraction of the time needed by other time-domain methods. By solving the generalized telegrapher equations, the currents and fields that propagate along the transmission line can be calculated. Examples that demonstrate the capabilities of the TLST have successfully demonstrated that the calculations agree well with experimental data.

In the EM interaction process, EM topology presents a fundamental concept for system protection. For the EM interaction process, the illumination of a system in which the waveform optimally couples into critical circuits of interest also needs to be addressed. First off, it is important to note that the waveform reaching a critical circuit is generally different from the waveform that was originally incident onto the system. Furthermore, the use of norms can maximize the ratio of the circuit waveform to the environmental waveform. Lastly, electronic systems tend to be built in dimensions that resonate around 1 GHz, indicating that frequencies near this value are important for IEMI [1].

As an introduction to EM topology, an overview of EMEC, an EM simulator based on topology, provides a good starting point. EMEC utilizes a graphical user interface to give the analysis of a system based on a topological description. Its primary application is the computation of responses due to radiated and conducted disturbances in complex systems. In addition, it can separately calculate shielding effectiveness for volumes, compute cable parameters, or analyze lumped element circuits. Figure 2 shows an example layout in the EMEC user-interface at the overall system level, Figure 3 shows the user-interface for the cable parameter module, and Figure 4 shows the user-interface for the circuit simulator module [6].

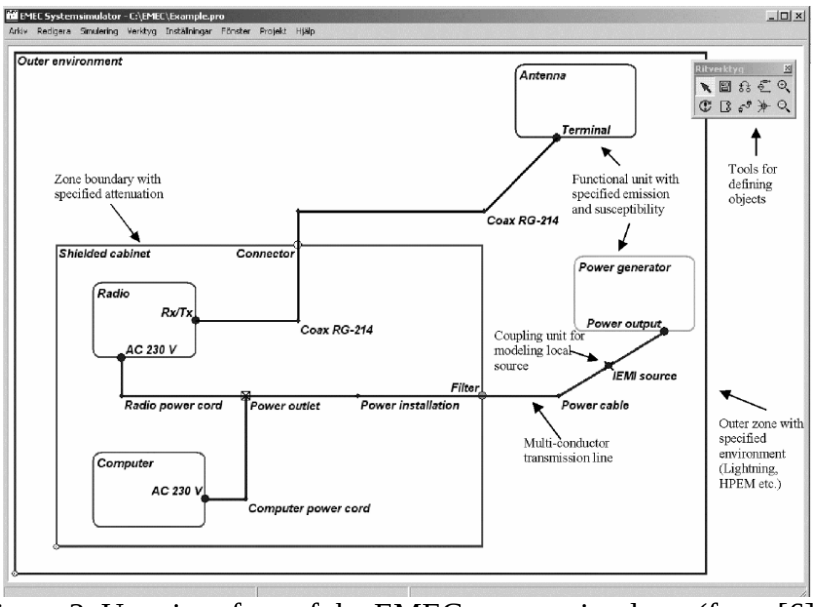

Figure 2. User-interface of the EMEC system simulator (from [6]).

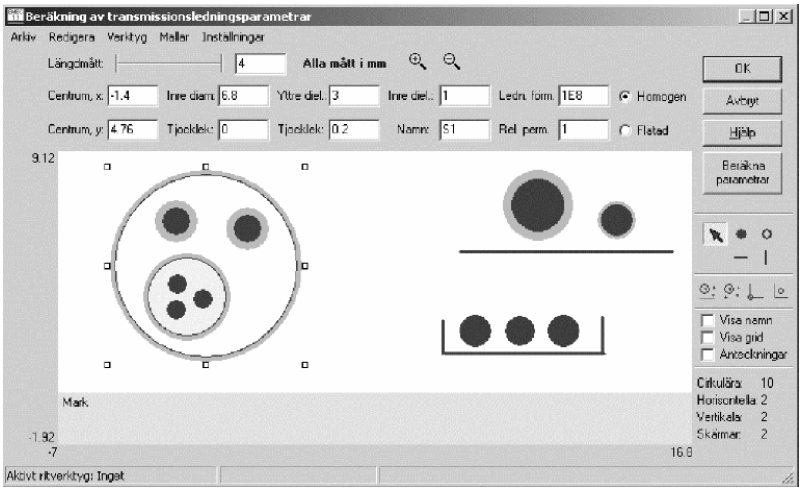

Figure 3. User-interface of the cable parameter module (from [6]).

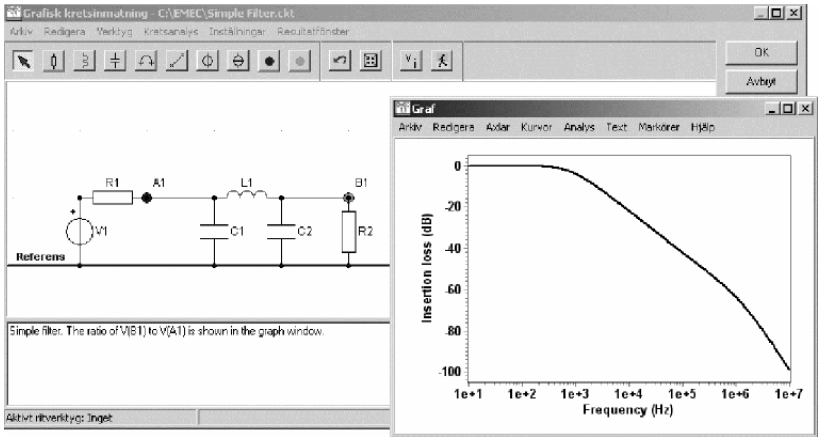

Figure 4. User-interface of the circuit simulator module (from [6]).

To further address the theory of EM topology, Parmantier [7] provides an overview of numerical simulation capabilities for the modeling of an entire system. First, a system-level analysis is investigated, where EM topology is shown to provide a guideline to performing a system's topological analysis. Along with the topological analysis of a system, Parmantier further discusses appropriate techniques to use in order to combine several specific numerical tools and broaden the scope of the entire system simulation. Parmantier concludes by addressing statistical trends and how they can help to identify future modeling challenges.

In order to withstand the effects of various EM threats, EM topology theory was developed to formalize the design of electrical systems. This led to the development of the topological shielding diagram, which provides a description of how the EM signals propagate within a system between defined volumes and surfaces that are each labeled with a relative shielding level. Figure 5 depicts an example of a topological shielding diagram [7].

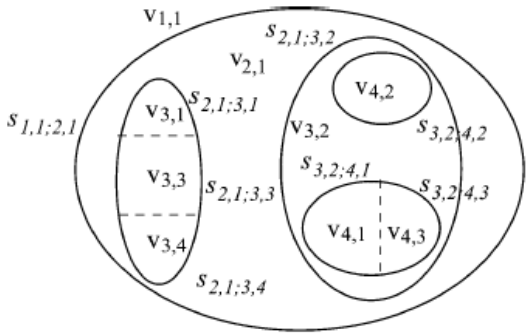

Figure 5. Topological shielding diagram. Volumes and surfaces are each labeled with a relative shielding level to provide a description of how the EM signals propagate within a system (from [7]).

Parmantier also explains how the "good shielding approximation" (GSA) provides an approximate description of how the EM field flux behaves inside the system. The GSA "supposes that the signal generated in an external volume can generate

interference inside an inner volume, but the reaction of the EM interference induced inside this volume on the external volume can be neglected" [7]. An interaction sequence diagram, shown in Figure 6, can be used to summarize the general EM interaction within the entire system. In the diagram, the signal flow of the flux of interference from the outside to the inside is represented by the directed branches.

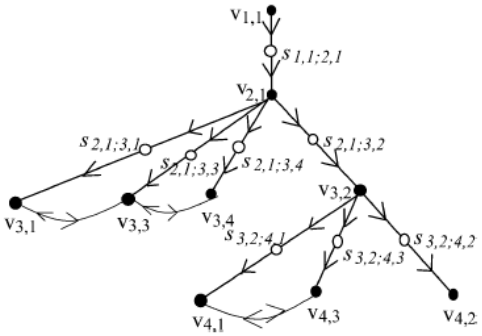

Figure 6. Interaction sequence diagram. The directed branches represent the signal flow of the flux of interference from the outside to the inside (from [7]).

Using the interaction sequence diagram, the network topology of a system can be deduced. The topological network corresponding to Figure 6 is shown in Figure 7. In this diagram, a junction is associated with each volume node and surface node, where response quantities are described using the Baum-Liu-Tesche (BLT) network equations described by Radasky et al. [1].

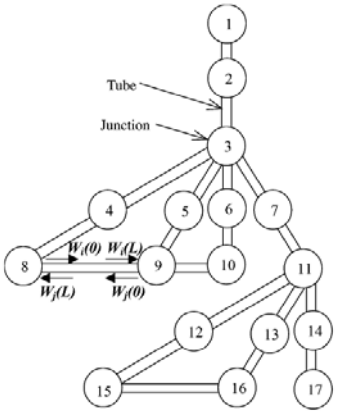

Figure 7. Example of the topological network associated with the interaction sequence diagram of Figure 6 (from [7]).

Essentially, EM topology establishes a guide for chaining calculations together. For each separate calculation involved in the topology chain, there are three main types of tools available for EM numerical simulations. The first type of available tools are 3-D numerical codes that solve EM scattering problems based on the system geometry. First, this includes volume techniques such as the Finite-Difference-Time-Domain (FDTD) method or the Finite Element Method (FEM). These techniques take the entire volume of the calculation and mesh it into volume cells. Limitations to these methods are due to the absorbing boundary conditions that are required to simulate an infinite medium.

Another type of 3-D numerical modeling code involves surface techniques, such as the Method of Moments (MoM). In surface techniques, only the surfaces of the diffracting object are meshed. Limitations for these techniques are the calculations, which are made on a frequency by frequency basis. In addition the size of the system matrix that is to be inverted increases as the square of the number of unknowns.

A third technique that involves 3-D numerical modeling code use what are called asymptotic techniques. These are based on an asymptotic formulation of Maxwell's equations when the frequency is much greater than the size of the object. Equations for these techniques combine methods such as the physical theory of diffraction (PTD) with ray techniques such as geometrical optics (GO) or the uniform theory of diffraction (UTD). Additionally, there are multiple domain techniques where Thevenin equivalents are determined for the network applications [7].

The second type of available tools are cable network tools. These tools apply to the topological shielding level associated with cabling, where a multiconductor transmission line network (MLTN) is used as the basic model. For MTLNs, there are two

primary aspects: 1.) The sources are distributed along the wiring with different amplitudes, and 2.) Cross coupling is an important issue to account for to ensure it does not contaminate "clean" EM zones in the system. Important factors that need to be accounted for in a cable network include: 1.) the frequency dependence of the electrical parameters, 2.) The existence of inhomogeneous propagation media such as dielectric insulators, and 3.) The independence of the model computation time from the length of the cable. This indicates that the most appropriate equations are ones that are based on a frequency formulation, such as the BLT equation for MTLN [7].

The third type of available tools are electrical circuit tools. Calculations for electrical circuit tools are limited to the input of the equipment and internal topology is excluded. These types of tools include circuit simulators such as SPICE and are usually restricted to finding only equipment responses [7].

Overall, the EM topology design of a usual system makes it difficult to use available numerical tools because of their limited capabilities. The frequency range required for analysis is a common application limit in these numerical techniques. The analysis methodology is still in a validation stage, especially at the higher frequencies [7].

Finally, another model for understanding the coupling of electromagnetic energy with systems and facilities is the Random Coupling Model (RCM) developed at the University of Maryland, which was not mentioned in the Special Issue. The RCM is a method for making statistical predictions of induced voltages and currents for objects and components contained in complicated enclosures and subjected to IEMI[1].

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[1] For additional information on the Random Coupling Model, see http://www.cnam.umd.edu/anlage/RCM/index.htm

1.3 The Effects of IEMI on Equipment, Systems and Communications

Chapter 1.3 provides an overview on the susceptibility levels of electronic equipment and systems. Significant experiments have been performed that test the response commercial equipment has to narrowband and wideband threats. In the range of 1-10 GHz, tests seem to indicate that malfunctions occur at lower field levels at lower frequencies. These experiments are typically performed by directly radiating the equipment under test with EM energy. Additionally, it should be noted that most of these experiments did not include a thorough examination on the effects of polarization and angle of incidence. Also, experiments where narrowband voltages are injected into the grounding system of a building have shown to cause significant malfunctions to the equipment inside [1].

The investigation by Camp et al. [8] on the prediction of breakdown behaviors of microcontrollers under EMP/UWB impact will be the only discussion covered in detail in this section. This is because this investigation directly pertains to the EM topology (described in Chapter 1.2) that the microcontroller instruction susceptibility research of Chapter 3 falls under. Camp et al. provides data primarily on the radiated coupling of HPEM to microcontroller devices, whereas the microcontroller instruction susceptibility research in Chapter 3 focuses more on using conducted coupling methods to further understand the internal upset mechanisms inside of a microcontroller. Camp et al. [8] performs experiments on three different microcontroller systems to measure their susceptibility against a transient electromagnetic field threat. The purpose of this is to determine how different circuit parameters influence the RF coupling and cause different levels of breakdown effects.

To begin the investigation [8], the Breakdown Failure Rate (BFR), the Breakdown Failure Probability (BFP), the Destruction Failure Rate (DFR) and the Destruction Failure Probability (DFP) are initially defined. These parameters are used to describe the different failure effects, where breakdown implies no physical damage is done to the system and destruction implies physical damage where the system will not recover without repair or replacement. Furthermore, BFR and DFR are estimators of the BFP and DFP. In terms of the number of breakdowns ($N_{Breakdown}$), number of destructions ($N_{Destruction}$), and number of pulses (N_{Pulses}) applied, these quantities are defined as follows:

$$BFR = \frac{N_{Breakdown}}{N_{Pulse}}, \tag{1}$$

$$BFP = \lim_{N_{Pulse}\to\infty} BFR, \tag{2}$$

$$DFR = \frac{N_{Destruction}}{N_{Pulse}}, \text{ and} \tag{3}$$

$$DFP = \lim_{N_{Pulse}\to\infty} DFR. \tag{4}$$

These quantities follow the principal behavior shown in Figure 8. To further define system susceptibility, four more parameters are introduced. The Breakdown Threshold (BT) and Destruction Threshold (DT) specify the electric field strength, where the BFR and DFR reach 0.05, respectively. The Breakdown Bandwidth (BB) and Destruction Bandwidth (DB) specify the span in which the BFR and DFR change from 0.05 to 0.95, respectively.

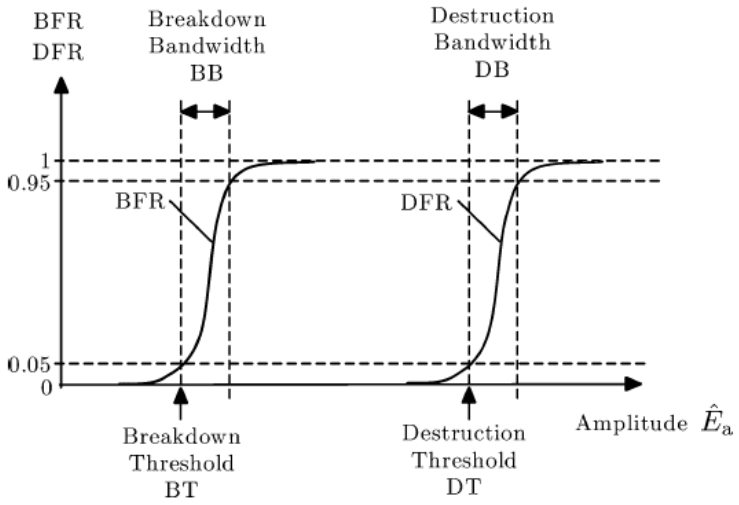


Figure 8. BFR and DFR (or BFP and DFP) principle behavior and definitions (from [8]).

To analyze the susceptibility of microcontrollers, three different microcontrollers are incorporated into the test that feature a RISC architecture, high-speed CMOS processor technology, 32x8 general purpose working registers, an on-board flash, and an on-board EEPROM. The general microcontroller test setup, along with the test variables to be modified, are shown in Figure 9. Additionally, during the test, the microcontrollers are executing a program that changes between two different states. The flow diagram for the microcontroller test program is shown in Figure 10. The purpose of the two states is to monitor the microcontrollers for a self-reboot, which is not possible to observe through any other method [8].

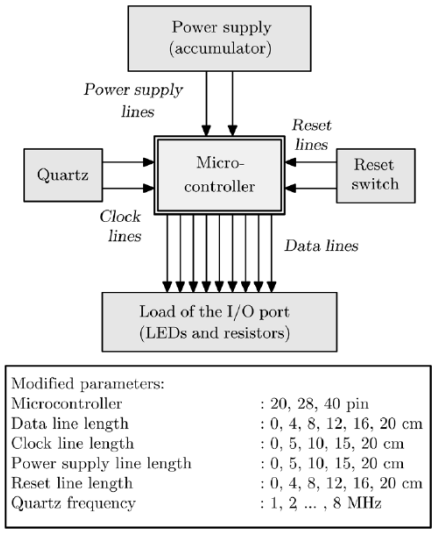


Figure 9. Microcontroller test setup. This shows how the bus line lengths are modified throughout the experiment and the quartz frequency test range (from [8]).

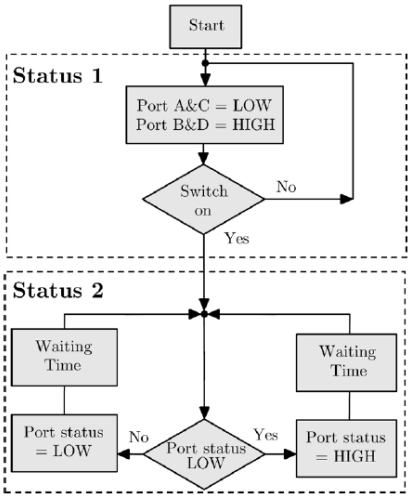


Figure 10. Two-state flow diagram for the microcontroller test program (from [8]).

A basic reference configuration for the microcontroller setup is defined for the measurements. For this reference setup, the clock, data, reset, and power-supply lines are at a minimum length and the clock rate is set to 1 MHz. The susceptibility is then determined for different port states (LOW and HIGH) as the signal lines are extended incrementally from 0 to 20 cm and the clock rates are changed incrementally from 1 to 8 MHz [8].

Analyzing the experimental results, Camp et al. report that the effect of the port state (HIGH/LOW) had little influence over the susceptibility of the microcontrollers. Regarding the effect of different signal line lengths, though, the results greatly varied in susceptibility levels between the data, clock, power supply, and reset line length. The results for the variation in BT and BB at each signal line as the data line length changes are shown in Figure 11 (a) and (b), respectively. By extending the length of the signal lines, the transfer function is enhanced, resulting in an increase in induced currents and voltages. Basically, the longer signal line lengths allow for more of the radiated energy to couple into the circuitry of the microcontroller.

Also, the variation of the clock rate from 1 MHz up to 8 MHz resulted in no effect on the BT or BB [8]. Table VIII summarizes the susceptibility level each parameter had on the influence of BT and BB [9]. The variation in the reset line length proved to be the most susceptible parameter.

When it comes to the effect of the pulse shape, the influence on breakdown behavior is very high. Basically, this influence is caused by the spectral energy distribution of the different pulses. Electronic systems at different frequencies have a stochastical distribution of susceptibility levels. Lastly, a larger BB is going to be associated with a pulse that has long rise times compared to a pulse with short rise times. The discussion by Camp et al. [8] concludes by describing statistical methods that can be used in the prediction of the microcontroller breakdown behavior based on the previously described parameters.

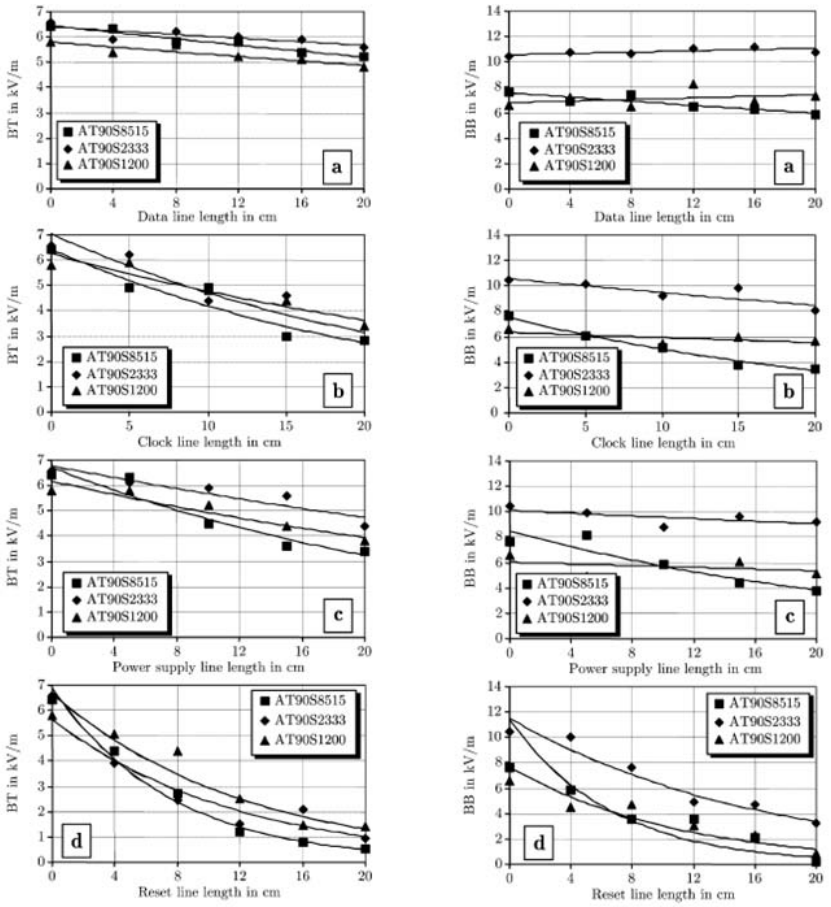


Figure 11. UWB test pulse: (a) BT for three microcontrollers with various signal line lengths. (b) BB for three microcontrollers with various signal line lengths (from [8]).

Table VIII. Susceptibility parameter influence on BT and BB (from [8]).

	Data Line Length	Reset Line Length	Osc. Line Length	Power Supply Line Length	Clock Rate	Type of Controller
BT	Low	High	Medium	Medium	None	Low
BB	None	High	Low	Medium	None	High

In addition to the microcontroller susceptibility work, Nitsch et al. [9] provide an overview of the susceptibility of a number of common electronic devices. These devices include computer networks, computer systems, microprocessor boards, microcontrollers, and basic integrated circuits (ICs). Susceptibility levels of these devices are determined

for various EM threats such as electromagnetic pulses (EMP), UWB pulses, and HPM pulses. Table IX summarizes the susceptibility level BT for the various equipment under test (EUT). Generally, the susceptibility level trends lower as the device complexity increases.

Table IX. Susceptibility levels BT (DT). A summary of the BT (DT) that various electronic devices have when disrupted by UWB, EMP, and/or HPM signals (from [9]).

EUT	UWB in kV/m	EMP in kV/m	HPM in kV/m
Logic Devices	25 (75)	120	
Microcontroller	7.5	42	
Microprocessor Boards	4	25	0.2
PC Systems	12		
PC Networks	0.2	0.5	

For further information on the effects IEMI can have on electronic systems, a vast amount of research studies and journal articles exist on the topic. To better understand the disruptive effects IEMI can have on personal computers, Hoad et al. [10] present an overview on the trends found in EM susceptibility of information technology (IT) equipment. Bäckström and Lövstrand [11] discuss susceptibility results for a number of electronic systems, including missiles, radios, cars, telecom stations, and generic electronic objects. For an in-depth study on conducted IEMI threats, Parfenov et al. [12] discusses conducted threats associated with commercial buildings. For communication devices, Jeffrey et al. [13] presents an investigation into using IEMI to disrupt and severely degrade Ethernet communication while still maintaining complete computer functionality in all other aspects.

By understanding the susceptibility levels that various electronic systems have to different EM threats, an understanding of the upset mechanisms may be achievable. An

understanding of the upset mechanisms will result the development of more advanced and effective protection concepts.

1.4 Protection, Measurements and Standards

Regarding protection concepts, Chapter 1.4.1 provides an overview of how various security measures can reduce and provide specific protection against IEMI threats. Key aspects that need to be considered in order to design protection into a system include: 1.) Distance, 2.) Shielding, 3.) Penetration Control, 4.) Resonance Reduction, 5.) Fault-tolerant Computation, and 6.) Circumvention [1].

In addition to HPEM protection concepts, Chapter 1.4.2 addresses IEMI standardization. Currently, there are two major IEMI standardization efforts underway. The first effort is being performed by the International Electrotechnical Commission (IEC), assigned to Subcommittee 77C, covering environment, protection, and test standards for commercial equipment that might be exposed to HPEM. The second effort has begun in the IEEE EMC society to develop standard practices to protect publicly accessible computers [1].

1.4.1 IEMI Protection Concepts

Regarding IEMI protection concepts, Weber et al. [14] investigates various linear and nonlinear filters that could possibly be used to suppress ultrawideband (UWB) pulses. Because of the broad frequency spectrum of these signals, UWB pulses have a very high probability to hit the resonant frequency of an electronic system, thus disrupting or destroying the system. It is therefore necessary to address whether traditional protection concepts provide adequate protection when it comes to UWB

signals with significant amplitudes, picosecond rise times, and pulse durations of a few nanoseconds.

In the discussion given in [14], different suppression devices are distinguished as being applicable to low frequency transmission lines (i.e., power lines) or to high frequency transmission lines (i.e., printed circuit boards). For the low frequency case, Weber et al. addresses various advantages and limitations for available devices, which includes spark gaps, varistors, and feed through capacitors. In the high frequency cases, the article considers zener-diodes and bandpasses in microstrip techniques. The testing in both cases reveals that linear and nonlinear protection circuits are capable of reducing the energy by UWB signals. It is concluded that optimized protection against UWB signals can be achieved by utilizing a proper selection of linear filter structures and nonlinear elements on the system.

In another discussion, Weber et al. [15] investigates the various measurement techniques that exist for conducted HPEM signals. Essentially, different methods can be used to measure conducted transients. The use of inductive sensors, characterized by a transfer function, are initially addressed. These current sensing techniques are shown to provide differential behavior in lower frequencies, proportional behavior in mid frequencies, and identifiable limitations at higher frequencies. Other common methods discussed that are currently used include: shunts, magneto- and electro-optic sensors, and resistive and capacitive voltage dividers. These various methods tend to not be applicable to frequencies much greater than 1 GHz and also have high voltage limitations. To overcome this, Weber et al. concludes by introducing a new technique, the picoTEM

method, that can be used to measure conducted HPEM signals beyond the limitations of previous techniques.

1.4.2 IEMI Standards

When it comes to the development of HPEM standardization, two efforts are currently underway. The first effort is being performed by the IEC and the second effort is being performed by the IEEE EMC society. For the IEC, SC77 is the assigned subcommittee and operates under the following scope: “Standardization in the fields of electromagnetic compatibility to protect civilian equipment, systems, and installations from threats by man-made high-power phenomena including the electromagnetic fields produced by nuclear detonations at high altitude” [16]. Therefore, SC77 has been developing environment, protection, and test standards for commercial equipment that might be exposed to HPEM. These IEC standards are published in the following structure (Part 1-6, Part 9):

- Part 1: General. This section includes general considerations, definitions, and terminology.
- Part 2: Environment. This section provides a description of the environment and its classification.
- Part 3: Limits. This section includes emission limits and immunity limits.
- Part 4: Testing and measurement techniques.
- Part 5: Installation and mitigation guidelines.
- Part 6: Generic standards.
- Part 9: Miscellaneous.

For further information on these standards, brief descriptions of each section pertaining to the SC77 standard are provided by Wik and Radasky [16].

A second effort to look into standardization, the one started by the IEEE EMC society, has also been developing standard practices to protect publicly accessible computers from IEMI [1]. Protection guidelines and tests are expected to be defined as a part of this effort.

Chapter 2 Microcontroller Overview and Previous Experiments

With an understanding of the IEMI threat provided in Chapter 1, Chapter 2 provides background research and experiments into the effects IEMI has on microcontrollers. First off, an overview of two 8051-core microcontrollers is provided in Chapter 2.1. Next, a review of previous research on microcontroller upset mechanisms is provided in Chapter 2.2. Chapter 2.1 addresses how an instruction is accomplished, explaining the details of a standard 8051-core machine cycle. The two 8051-core microcontrollers discussed in detail are the ATMEL AT89S2051 (S2051) and the ATMEL AT89LP2052 (LP2052). The key difference between these two 8051-core architectures is that the LP2052 utilizes an "enhanced" 8051-core that allows instructions to be processed in a parallel manner and the S2051 utilizes a standard 8051-core where instructions are processed serially.

The LP2052 will be used as the device under test (DUT) for the experiment outlined in Chapter 3, whereas the S2051 will be part of the Chapter 5 discussion in regards to follow-on experiments based on the LP2052 results presented in Chapter 4.

In Chapter 2.2, the earlier experiments were performed by the Air Force Research Lab HPM effects branch (AFRL/RDHE) [20]. These initial experiments were performed on the LP2052 and another microcontroller, the ATMEL MEGA8515L, which utilizes an AVR-core architecture and not the 8051-core architecture.

2.1 Microcontroller Test Device Overview

The terms microcontroller and microprocessor tend to be used interchangeably with each other at times, but they are not the same device. It is important to distinguish the difference between the two devices and to provide an understanding of how a generic

microcontroller operates. For a microprocessor to be used in a complete microcomputer system, it would require additional external peripherals such as Read Only Memory (ROM), Random Access Memory (RAM), decoders, drivers, and a number of input/output devices. Basically, a microprocessor provides a means to build a complete digital system in a very flexible manner by not including these additional peripherals in the actual design. On the other hand, a microcontroller incorporates all the features found in a microprocessor, but also incorporates a number of features (i.e., memory, I/O interfacing, and various peripheral devices) to make a complete microcomputer system on a single IC chip. The differences between a microprocessor and a microcontroller are outlined in Table X [21].

Table X. Differences between a microprocessor and a microcontroller (from [21]).

No.	Microprocessor	Microcontroller
1.	Microprocessor contains ALU, control unit (clock and timing circuit), different register and interrupt circuit.	Microcontroller contains microprocessor, memory (ROM and RAM), I/O interfacing circuit and peripheral devices such as A/D converter, serial I/O, timer etc.
2.	It has many instructions to move data between memory and CPU.	It has one or two instructions to move data between memory and CPU.
3.	It has one or two bit handling instructions.	It has many bit handling instructions.
4.	Access times for memory and I/O devices are more.	Less access times for built-in memory and I/O devices.
5.	Microprocessor based system requires more hardware.	Microcontroller based system requires less hardware reducing PCB size and increasing the reliability.
6.	Microprocessor based system is more flexible in design point of view.	Less flexible in design point of view.
7.	It has single memory map for data and code.	It has separate memory map for data and code.
8.	Less number of pins are multifunctioned.	More number pins are multifunctioned.

In a microcontroller, the internal processor accomplishes an instruction by performing the following actions: fetch, decode, execute, and store. For example, if the microcontroller were programmed to calculate a math based problem, the first step to accomplish this would be for the control unit to fetch the math problem's instructions and

data from the memory. In the second step, the control unit would decode the instructions of the math problem and send the instructions and data to the Arithmetic Logic Unit (ALU). The third step would involve the ALU performing the calculation of the problem. Finally, in the fourth step, the result from the ALU would be stored in memory. The steps involved in a generic machine cycle are shown in Figure 12 [22].

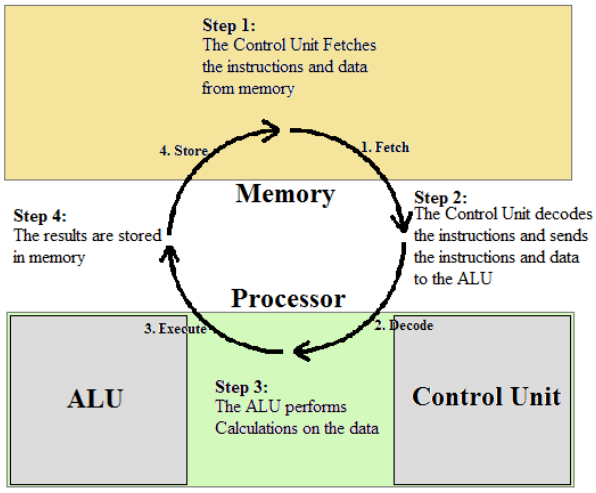


Figure 12. Machine cycle for processing instructions inside a microcontroller (from [22]).

Both the S2051 and the LP2052 microcontrollers follow a Harvard architecture for memory organization. The Harvard architecture is a computer architecture with physically separate storage and signal pathways for instructions and data [27]. Figure 13 provides a block diagram for a Harvard architecture [28].

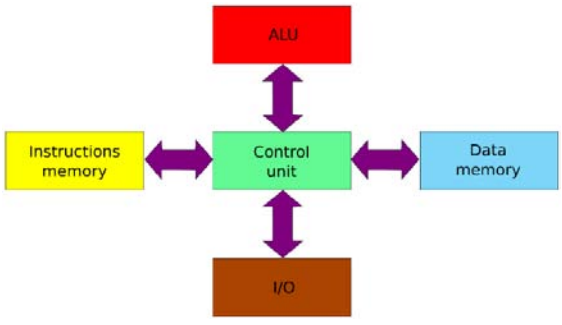


Figure 13. Harvard architecture block diagram. The memory banks, arithmetic logic unit (ALU), and inputs/outputs (I/O) each have a separate signal pathway to the control unit (from [28]).

The S2051 and the LP2052 microcontrollers are both descendants of the Intel 8051 microcontroller, utilizing a similar generic architecture as part of the 8051-core family (also known as the MCS-51 family), which is shown in Figure 14 [23]. The core architecture of the S2051 is shown in Figure 15 [26]. It can be seen that it is only a two-port device which utilizes a flash memory instead of an Erasable Programmable Read-Only Memory / Read-Only Memory (EPROM/ROM) compared to the original 8051 microcontroller. The LP2052 is also a two-port device with flash memory, but the architecture is built around an “enhanced” 8051-core (proprietary) that is able to fetch more data bits per clock cycle compared to the standard 8051-core.

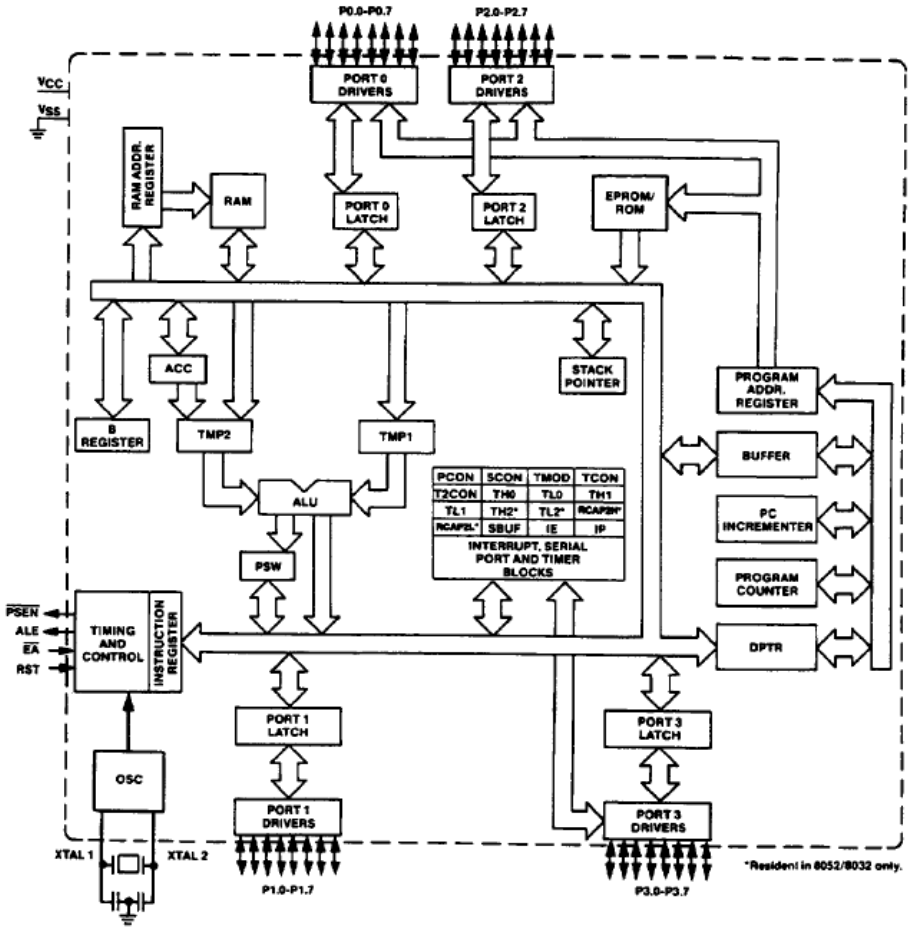


Figure 14. 8051-Core architecture. A standard 8051-core includes 4-ports and utilizes an EPROM/ROM (from [23]).

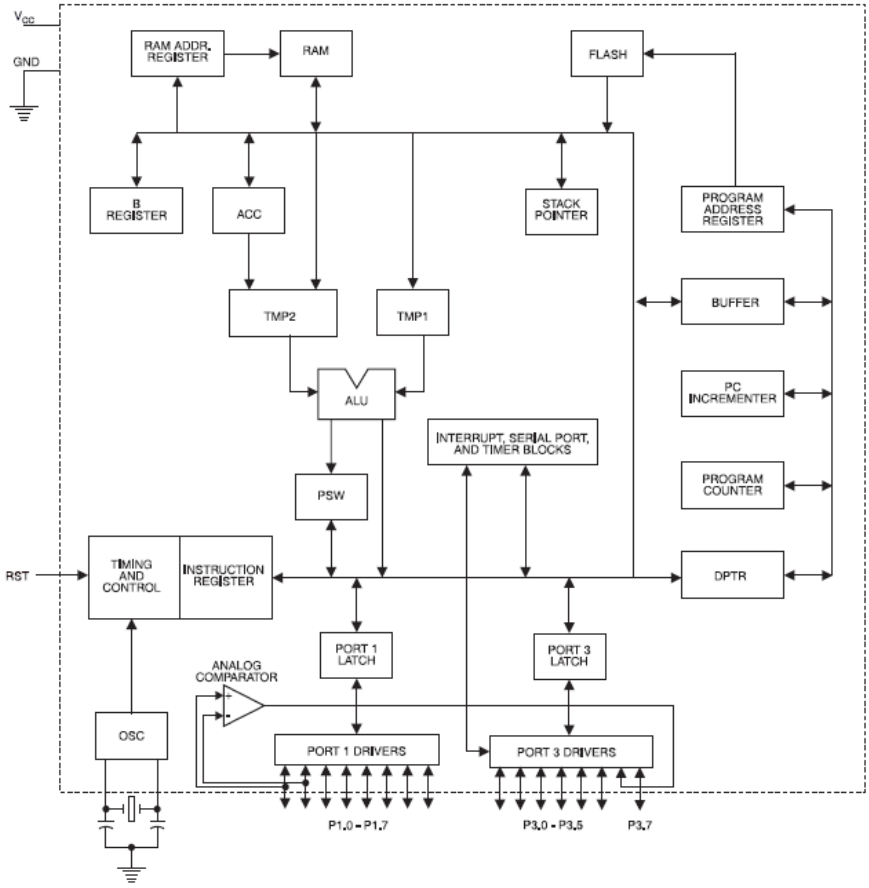


Figure 15. AT89S2051 core architecture. This is a variant of the 8051-core architecture, where it has only two-ports and utilizes a flash memory (from [26]).

For the S2051, a serial computational process is utilized where each instruction is executed entirely before a new instruction begins. This method of serial processing is how instructions are processed by standard 8051-core microcontrollers. For the S2051 and standard 8051-core microcontrollers, 1 machine cycle requires 12 clock cycles to execute, where a machine cycle is equivalent to 1 byte of data. Clock cycles within the machine cycle are grouped together between states and phases. One complete machine cycle (12 clock cycles) contains a total of 6 states, where each state contains two phases (or 2 clock pulses). This process is depicted in Figure 16 [23]. Typically, phase 1 handles the arithmetic and logic operations, whereas phase 2 handles internal register-to-register transfers [25].

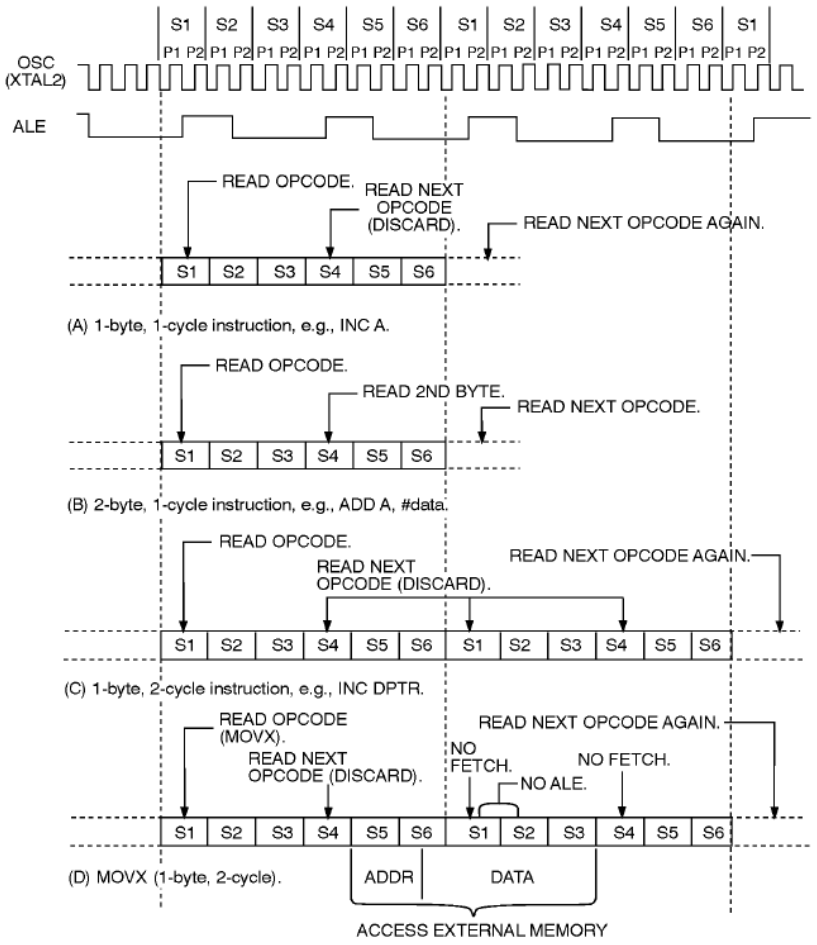
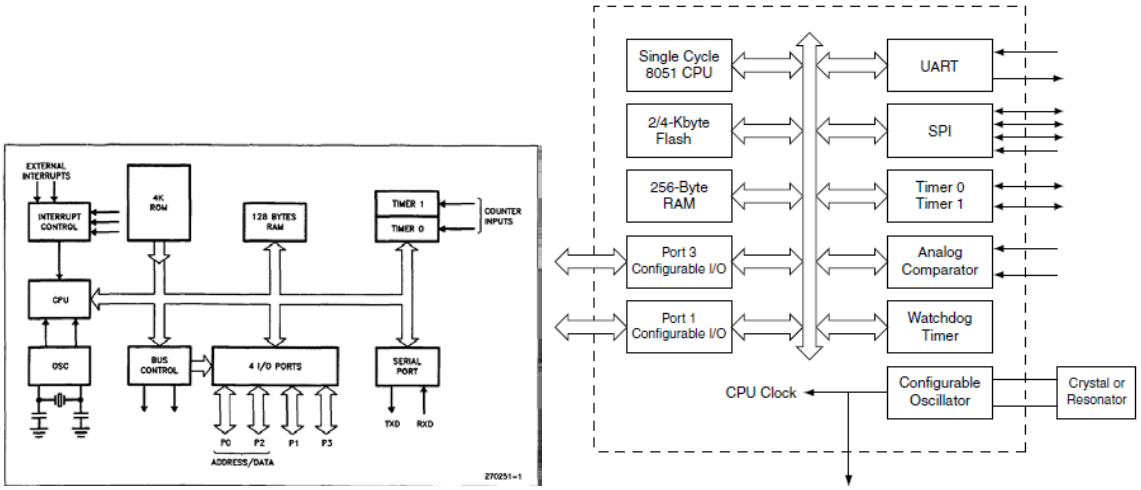


Figure 16. Standard 8051 serial instruction processing. A machine cycle contains 6 states, where each state contains two phases. Typically, phase 1 handles the arithmetic and logic operations and phase 2 handles inter-register transfers. (A) and (B) provide examples of assembly commands that take only 1 machine cycle to execute. (C) and (D) provide examples of assembly commands that require two machine cycles to execute (from [23]).

In contrast, the LP2052 can process 1 byte of data per clock cycle and can execute an instruction while the next instruction is being fetched. This implies that instructions only require between 1 to 4 clock cycles to fully execute. For standard 8051-core architectures, including the S2051, instructions required 12, 24, or 48 clock cycles (1 to 3 machine cycles) to fully execute an instruction. Therefore, the LP2052 executes an instruction with 6 to 12 times greater throughput compared to standard 8051s.

A comparison between the basic architectural structure of the classic 8051 and the LP2052 is depicted in Figure 17. The LP2052 is fully compatible with the MCS-51

instruction set, but it utilizes an enhanced “Single Cycle 8051 CPU”. The term “single cycle” is meant to imply that a single instruction cycle on the LP2052 is accomplished in one clock cycle as opposed to the standard 8051- core where one instruction cycle requires 12 clock cycles.



(a) (b)

Figure 17. Architectural structure of the 8051-core compared to the architectural structure of the LP2052. (a) Block diagram of the 8051-core (from [23]). (b) Block diagram of the LP2052 (from [27]). Key differences of the LP2052 are that it is only a two-port device, utilizes a flash memory, and has an enhanced Single Cycle 8051 CPU. The term “Single Cycle” implies that an instruction cycle completes in one clock cycle compared to 12 clock cycles (from [23,27]).

Two factors can be attributed to the LP2052 core being identified as an “enhanced” 8051 CPU: 1.) One instruction byte is fetched from the code memory every clock cycle, and 2.) A simple two-stage pipeline is used by the CPU to fetch and execute instructions in parallel. What this means is that while one instruction is being executed, the instruction that directly follows is being fetched from the memory at the same time. This parallel instruction processing is shown in Figure 18, and a single-cycle and a two-cycle ALU operation is shown in Figure 19 and Figure 20, respectively [27].

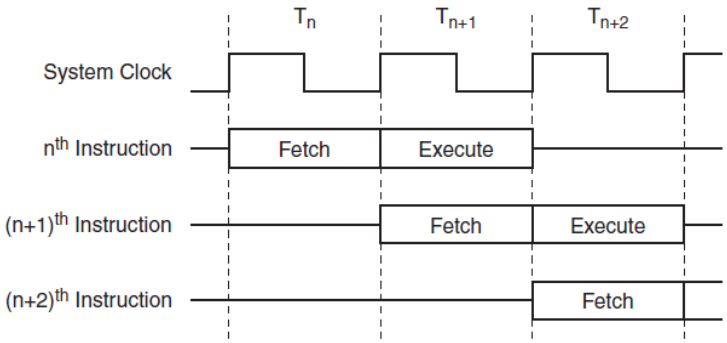


Figure 18. Parallel instruction fetches and executions (from [27]).

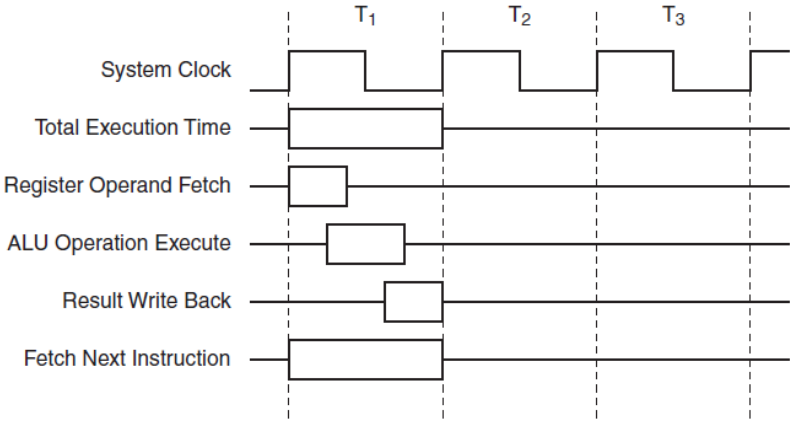


Figure 19. Single-cycle ALU operation (i.e. INC R0) (from [27]).

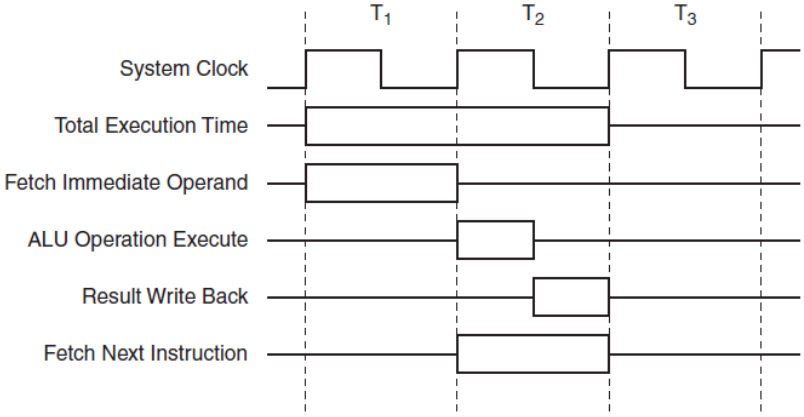


Figure 20. Two-cycle ALU operation (i.e. ADD A, #data) (from [27]).

2.2 Previous Microcontroller Upset Research Experiments

At Kirtland AFB, NM, AFRL/RDHE initiated microcontroller susceptibility experiments in 2009 as part of an effort to develop predictive models for HPEM upset effects on digital systems as a function of system, software used, and RF waveform

parameters. As an intermediate objective, it was decided to develop a statistical model for RF upset on microcontrollers as a function of the specific assembler instruction and the incident waveform. Microcontrollers were selected as the DUTs because they represented an intermediate level in complexity between a single CMOS device and a complete digital system such as a personal computer (PC). Essentially, a microcontroller represents a complete, yet simple, digital system packaged into a single IC chip, but does not contain all of the additional wires and peripherals that are packaged into a PC [20]. Figure 21 illustrates how a microcontroller would be represented by a topological model as previously discussed in Chapter 1 [29].

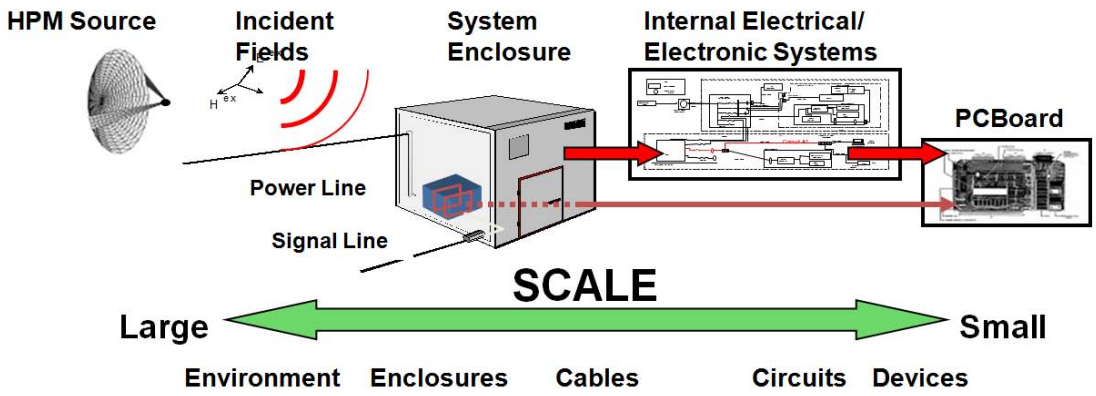


Figure 21. Topological diagram for building a predictive model of a digital system. A microcontroller represents an intermediate level on the scale between a PC and single electrical devices (i.e., a PC includes an enclosure, cables, circuits and devices whereas a microcontroller only includes circuitry and devices) (from [29]).

For this effort, the two main objectives have been to: 1.) Build a mathematical model for predicting upset effects in microcontrollers exposed to incident radio frequency (RF) pulses, and 2.) To ascertain the validity of that model, refining it as appropriate, based upon results of experiments performed on selected microcontrollers.

In the first year of the microcontroller research, the effort started with the development of a probabilistic model for theoretically describing digital upset of the microcontroller as a function of RF pulse parameters and the assembly-instruction-

induced microcontroller signal streams. There are four relevant areas that impact the details of the model that have been constructed to date. The first area pertains to the mode of exposure of the microcontroller to the incident RF pulse: RF radiation field immersion or direct RF voltage injection into selected ports. The second area pertains to the type of signal stream being addressed – clock or data. The third area pertains to the characterization of the injected RF pulse, which is essentially a Gaussian modulated sine wave with the modulation envelope extending between voltage extremes. The fourth area pertains to the relative timing between the signal train and the onset of the injected RF pulse. This model continues to be developed and refined based upon the experiments performed on selected microcontrollers [30].

During the second year of the microcontroller upset investigation, four microcontrollers were selected to be used as DUTs to validate and refine the theoretical model based on direct injection experiments. These four DUTs were selected based on previous research into the immunity of digital electronics to transient pulses [31, 32]. This previous work investigated how a burst of 50 ns transient electrical pulses affected a simple 8-bit 8051 microcontroller while a single assembler instruction was repeatedly executed. The assembly instruction was two machine cycles long for a total of 24 consecutive clock pulses. The incident RF pulses were timed precisely to make them coincide with a specific state and phase of one of the machine cycles (also called a microinstruction) during the assembly instruction. The authors were able to determine an empirical susceptibility probability for each microinstruction, and were therefore able to predict the susceptibility for the entire assembly instruction by aggregating these

probabilities. These results are summarized by the model developed by Dietz [30] in Figure 22.

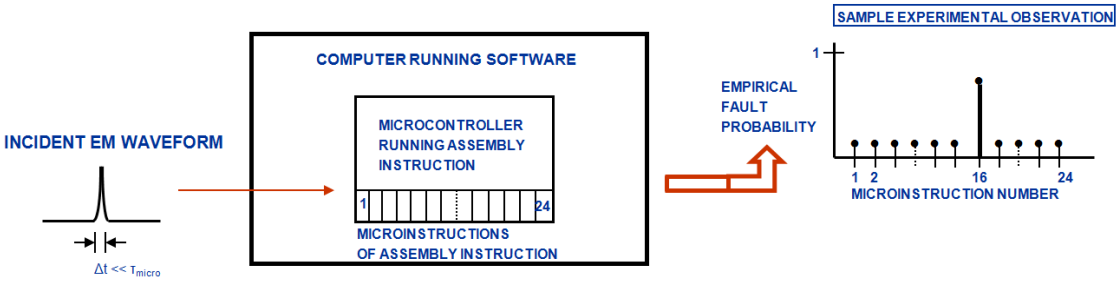


Figure 22. An incident waveform couples into a microcontroller. Based on the empirical susceptibility probability for each microinstructions, the susceptibility for the entire assembly instruction can be predicted (from [30]).

In this past research [31,32], the manufacturer or the precise microcontroller model used in the experiments was not identified other than it being compatible with the MCS-51 instruction set. As a substitute, two models of the 8051-core architecture produced by ATMEL were selected. Additionally, the AFRL investigation extended the research to be performed on another family of microcontrollers, the AVR-core family, and selected two models produced by ATMEL within this family.

For the 8051 microcontrollers, the AT89C2051 and the AT89LP2052 were initially selected as the test devices, but the AT89C2051 was recently replaced by the AT89S2051 model for the experiments (this had to do with compatibility/programming difficulties related to the AT89C2051). The second family of microcontrollers selected was ATMEL's AVR-core line, which included the ATTINY28L and the ATmega8515L. The AVR-core is based on Reduced Instruction Set Computing (RISC) architecture. Basically, an AVR-core can be characterized by having a Harvard Architecture, single-level pipelining (i.e., instructions are processed in parallel), short execution time, and a small, highly optimized instruction set [34].

Initial experiments have only been performed so far on the AT89LP2052 and on the ATmega8515L. The effects induced on these microcontrollers were explored by directly injecting them with RF signals (conductive coupling) while a simple binary counter program was executing. The value of the counter program was monitored at the output ports of the microcontroller, allowing for easy effects diagnosis. There are a number of locations where an RF signal can be injected into the microcontroller, but the initial experiments focused on injecting RF into the external clock line input.

Upset data was collected as a function of the RF voltage and pulse duration for when an induced RF signal was directly injected into the clock pin of the microcontroller. For both microcontrollers, experiments have helped to identify a frequency dependent susceptibility, where an increase in the injected peak voltage is required to cause an upset at higher RF carrier frequencies. Furthermore, various levels of RF effects were identified, ranging from minor disruptions to the counter program output value, all the way to a complete lockup of the microcontrollers. When a microcontroller end-state resulted in lockup, this was identified as being an upset state, where a power cycle was required to bring the microcontroller back to normal operation.

Simple initial models were built for these effects, addressing both the case where the onset of the RF signal has a known timing relative to the clock pulses and the case where the timing is unknown. These initial models are regularly refined based on experimental results [20]. Currently, for the AVR microcontroller family, experiments are still being performed on the ATmega8515L. In the most recent of these experiments, the RF waveform was synchronized to inject during precise target instructions on either

the clock line, various input/output lines, or the reset line. This investigation demonstrated that different target instructions have different levels of susceptibility.

The present experiments have started to investigate using software to map and understand microcontroller susceptibility. By determining various levels of susceptibility for instructions and the individual actions performed by the instruction, the individual actions can be related to different blocks within the functional layout of the microcontroller. The functional block can then be related to part of the physical layout of the microcontroller. This is represented in Figure 23 [29], and the experiment explained in Chapter 3 provides the basis and direction for this investigation.

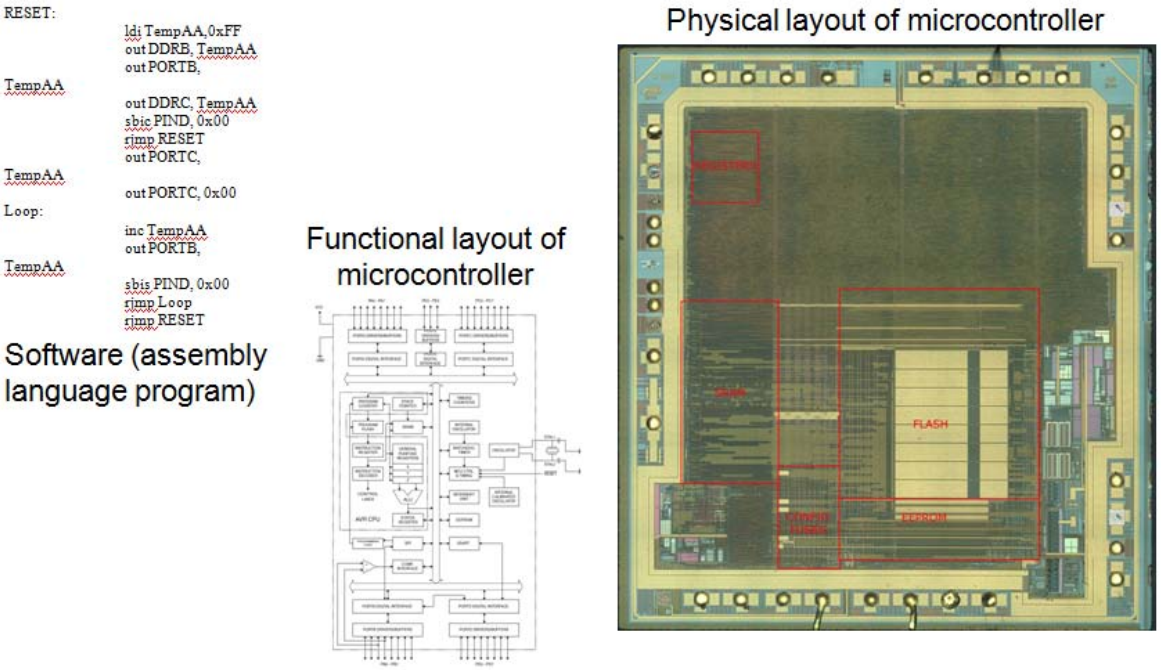


Figure 23. Use software to map and understand susceptibility. The individual actions that make up an instruction can be investigated for different levels of susceptibility. The actions can then be related to specific blocks of the microcontroller functional layout. Then, the blocks can be related to specific locations on the physical layout of the chip (from [29]).

For the experiments being performed on the 8051 family, the next step in the experimental investigation is described in Chapter 3. A target instruction is divided up

into 9 sections of interest for the LP2052 microcontroller based on the parallel processing of an instruction cycle. This is to characterize the susceptibility of different actions or microinstructions within the target instruction and investigate whether it may be feasible to use software (assembly code) to map them to the internal core architecture.

CHAPTER 3 METHODOLOGY

3.1 Purpose and Objectives of Experiment

From Chapter 2, it can be seen that experiments to date have primarily been on a general characterization of how an induced RF signal affects a microcontroller when it is directly injected into the clock pin. These experiments have helped to identify a common state of upset in the microcontroller, a locked-logic upset state, but have not provided an in-depth investigation into the possible upset mechanisms. The purpose of this experiment is to investigate the susceptibility each individual instruction of a microcontroller has to a directly injected RF signal. By identifying the susceptibility of each instruction, the susceptibility of the internal microcontroller functions that process each instruction can possibly be identified and can lead to further insight on the upset mechanisms.

To perform the experiment, an RF signal was injected into the clock line input of a microcontroller and precisely synchronized to target a specific instruction at any one point during the instruction cycle. In general, a microcontroller instruction cycle accomplishes the following actions: 1.) Fetches an instruction from memory, 2.) Decodes the instruction, 3.) Executes the instruction, and 4.) Stores the results in memory [22]. The baseline target instruction will be the ‘no-operation’ command and its susceptibility will be compared relative to the susceptibility of all other target instructions.

The microcontroller used as the DUT is the ATMEL AT89LP2052 (LP2052) and is fully compatible with the MCS-51 instruction set utilized by a standard 8051-core architecture. The LP2052 processes instructions in a parallel manner, whereas standard 8051-core microcontrollers process instructions serially. As previously explained in

Chapter 2.1, serial processing implies that each instruction executes entirely before the next instruction begins. Parallel processing implies that multiple instructions may be executing at the same time within a pipeline. For the 8051-core architecture, this means that instructions processed in serial take 12, 24, or 48 clock cycles to complete an instruction, whereas the parallel processing in the LP2052 will only take 1 to 4 clock cycles to complete the exact same instructions.

The purpose of this experiment is to test the hypothesis that different moments in time of an instruction cycle of an LP2052 have different levels of susceptibility. Essentially, by breaking up an instruction cycle into multiple target locations, microinstructions within the target instruction will have different levels of susceptibility to IEMI. These results would agree with the German work previously mentioned in Chapter 2.2 [31,32] and would help to provide a basis for using software to map out susceptibility levels of the internal 8051-core architecture.

3.2 Microcontroller Programming and Target Instructions

On the LP2052 microcontroller, an up-counter operation was programmed into the flash memory using assembly code. By using assembly code to program the microcontroller, the exact state of the microcontroller can be calculated and determined based on the total number of clock cycles applied to the external clock input. The MCS-51 instruction set and the number of clock pulses required for each command for standard 8051-core microcontrollers and for LP2052 microcontrollers is provided in Appendix A.

In order to program the microcontroller with an assembly code, the program ‘ASEM-51’ version 1.3 for Windows (a freely provided, simple assembler) is used to convert the assembly file into a HEX file. Then, the ‘MikroElektronika 8051-Flash’

program, the software provided with the Easy8051B Development Board, is used to load the HEX file into the flash memory of the microcontroller. This was a straightforward process to accomplish, where the instructions for each program explained how to perform each action in the file conversion and the flash programming.

Within the assembly code, a target instruction is programmed at a specific clock count location to be induced with an injected RF signal. For example, Figure 24 shows a disruptive RF signal being synchronized to clock pulse 6. Clock pulse 6 can be identified based on the assembly code used to program the microcontroller. With the target location identified for synchronization, the disruptive RF injection can be used to determine the susceptibility of the target instruction or a specific part of the instruction.

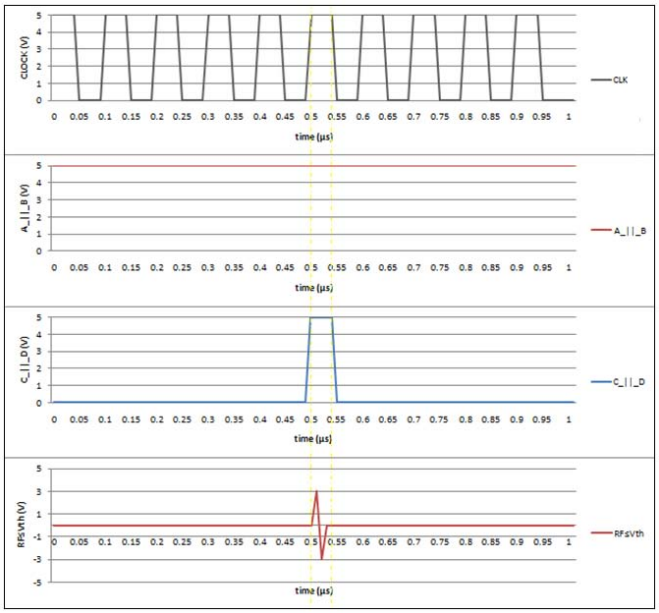


Figure 24. Example of how a target instruction is associated to a specific clock pulse. If the target instruction were located at clock pulse 6 (beginning at 0.5 µs), an RF pulse is synchronized to inject at the exact target location within the target instruction.

For the experiment, the LP2052 is programmed with the assembly code shown in Figure 25. In the first 5 clock cycles, the microcontroller is initialized and the first instruction is being fetched. At clock pulse 10, the target command (a NOP instruction) is

being executed. The 14th clock cycle initiates the binary up-counter program. Following the 22nd clock cycle, P1.0 through P1.7 (port 1) have all been initialized to a count of 0b00000000 by the instruction 'MOV 144, #0' (this instruction sets the port 1 special function register to 0b00000000, where each bit corresponds to an output lead with P1.0 as the Least Significant Bit (LSB) and P1.7 as the Most Significant Bit (MSB), see Figure 27 (a)). After 6 more clock cycles, the counter increments to 0b0000001, beginning the up-count sequence. Following the first counter increment, each subsequent increment occurs every 9 clock pulses, continuing on in an infinite loop until the power source or clock signal is removed from the microcontroller under normal operation.

```
;LP2052, 5 clock cycles to initialize microcontroller
_main:
    MOV 129, #128           ;3 clock cycles

;Provide buffer time before target command, begins after 8 clock cycles
    NOP ;1 Clock Cycle

;Target command for RF injection, begins after 9 clock cycles
    NOP ;1 Clock Cycle

;Provide buffer time following target command, begins after 10 clock cycles
    NOP ;1 Clock Cycle
    NOP ;1 Clock Cycle
    NOP ;1 Clock Cycle


;Initialize Up-Counter inputs and outputs, begins after 13 clock cycles
    MOV 194, #1   ;3 Clock Cycles
    MOV 195, #1   ;3 Clock Cycles
    MOV 144, #0   ;3 Clock Cycles, P1.0-P1.7 LEDs light up on development board following this command

;Up-Counter infinite loop
L_main0:
    MOV A, 144    ;2 Clock Cycles
    ADD A, #1     ;2 Clock Cycles
    MOV 144, A    ;2 Clock Cycles
    SJMP L_main0 ;3 Clock Cycles
```

Figure 25. Assembly code used to program the microcontroller. Clock cycle 10 corresponds to the target instruction for RF injection. After 13 clock cycles, an up-counter program is initialized. After 22 clock cycle, the binary up-counter enters into a continuous loop, incrementing every 9 clock cycles.

For the target instruction, 9 target locations have been defined for RF injection based on the LP2052 instruction cycle shown in Figure 18 from Chapter 2.1. For each target location, the RF pulse is synchronized to couple into the microcontroller for the

complete duration required to cover the location. The 9 target locations are shown in Figure 26, where they include the complete instruction cycle, the logic high, the logic low, and the transitions between the logic levels within the instruction cycle.

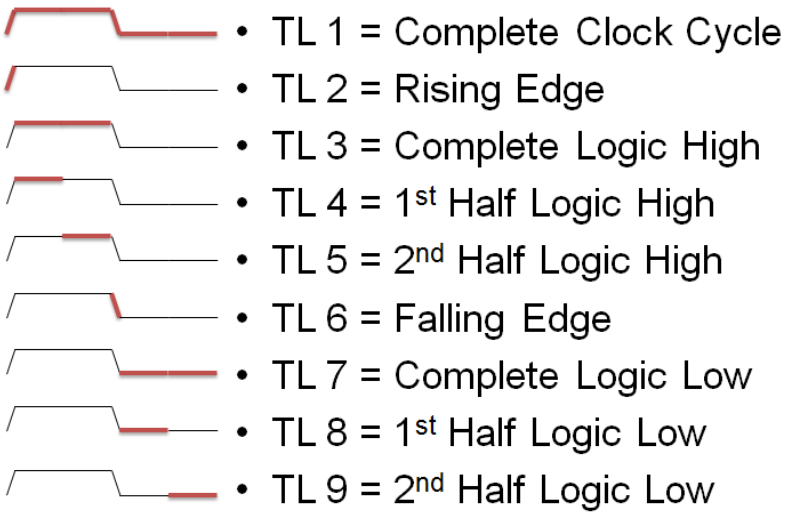
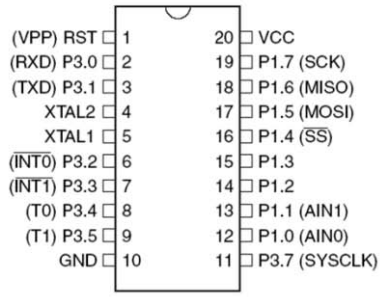


Figure 26. Based on the LP2052 parallel instruction cycle process, 9 different target locations have been defined to be injected with RF.

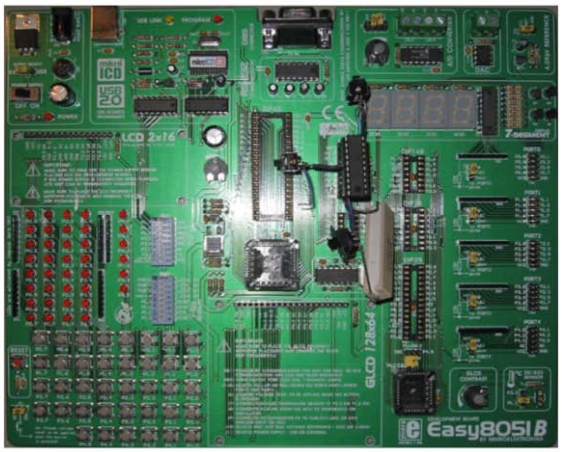
3.3 Experimental Setup and Configuration

For the LP2052 test device, a pinout of the microcontroller is shown in Figure 27(a) [27], and Figure 27(b) shows the microcontroller device mounted on to the Easy8051B Development Board. For the experiment, the RF signal is injected through the XTAL1 line, which corresponds to pin 5 on the microcontroller. XTAL1 is the external clock input, meaning that the RF signal is being conductively coupled into the circuit with the externally provided clock signal. The Easy8051B Development Board allows the chip to be easily programmed and also allows a means to verify the functionality of the microcontroller during normal operation and following RF injection.



LP2052 20-Pin μC

(a)



Easy8051B Development Board

(b)

Figure 27. (a) Pinout of the LP2051 microcontroller. The microcontroller is in a 20-pin DIP package. (b) The microcontroller is mounted on the Easy8051B Development Board to provide an easy means for programming and evaluation.

To mount the microcontroller to the development board, a modified 20-pin DIP mount was created and is shown in Figure 28. The mount provides extended lead lines to the microcontroller to allow for easy RF injection and measurements. At the XTAL1 pin (pin 5), an oscillator bypass switch is incorporated. This switch is necessary to provide an external clock signal to the microcontroller other than the 10 MHz external oscillator clock that is built into the development board. Additionally, as a future option for experiments, a low value resistor (between 1 to 10 Ω) can be placed in series with either the VCC line, the GND line, or both lines by properly setting the VCC switch or GND switch. This is so that average current measurements can be taken during normal operation and compared to the average current values when the microcontroller is induced into an upset state. Average current measurements were not taken throughout this experiment, so the VCC switch and the GND switch can be ignored.

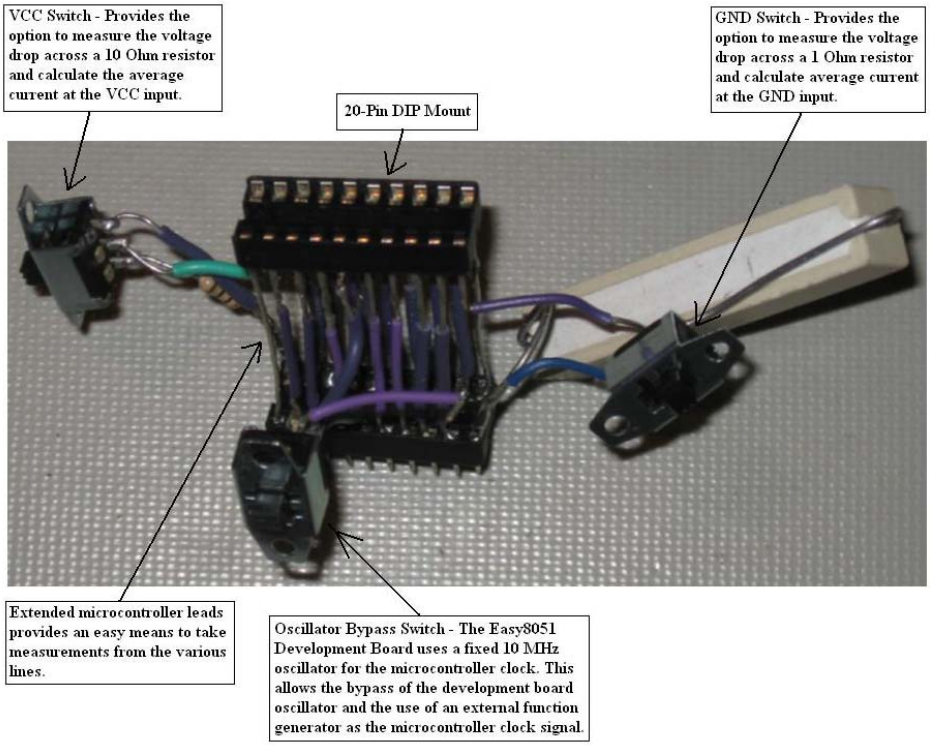


Figure 28. Modified 20-Pin DIP mount.

For the experiment, a schematic of the test setup is shown in Figure 29 and a photograph of the test setup is shown in Figure 30. The HP8116A Pulse/Function Generator is used to provide an external clock signal to the microcontroller. The function generator is used in the burst mode so that a specific number of clock pulses can be applied to the microcontroller. By knowing the total number of applied clock pulses, the final output state of the microcontroller can be determined (i.e., an up-counter program has been incremented to an expected output value associated with the applied burst of clock pulses, where it requires a specific number of additional clock pulses to increment the count to the next value). Additionally, the function generator's trigger output channel activates the DG535 4-CH Digital Delay/Pulse Generator.

On the DG535, the A ⊓ B channel is used to activate the DPO3054 digital oscilloscope so it will collect measurement data on CH1 through CH4 from the beginning

of the clock signal burst. The C ⊓ D channel is used to synchronize the RF signal injection to pulse for the duration of a specific target instruction and target location. The waveforms recorded by the oscilloscope include the clock signal with the coupled RF signal, the microcontroller system clock output (pin 11, labeled P3.7(SYSCLK) in Figure 27(a)), P1.0 (pin 12), and P1.7 (pin 19). P1.0 and P1.7 represent the Least Significant Bit (LSB) and the Most Significant Bit (MSB) outputs, respectively, from a programmed up-counter code on the microcontroller.

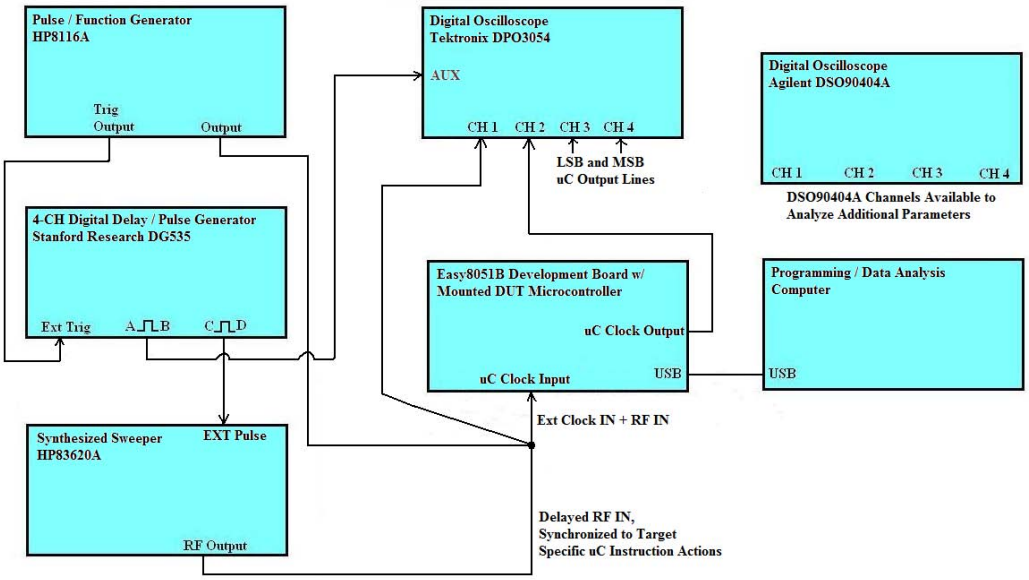


Figure 29. Schematic of test setup.

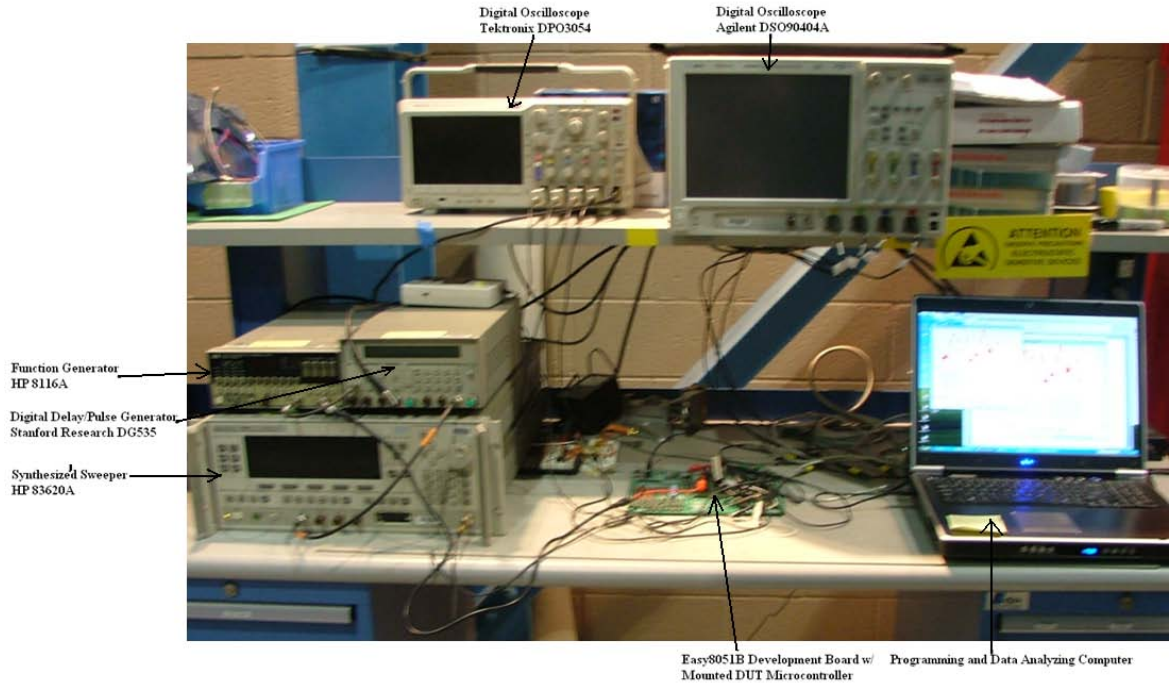


Figure 30. Photograph of the experimental test setup.

3.4.1 Overview of Test Equipment

HP 8116A Pulse/Function Generator:

In the experiment, an HP8116A Pulse/Function Generator, shown in Figure 31, is used to generate an external clock signal and to trigger the DG535 digital delay pulse generator. The 8116A is used in the "External Burst" mode and is set to output a specific number of square wave pulses. For the experiment, a square wave is set to have a logic low at 0 volts, a logic high at 5 volts and to pulse at a frequency of 1 MHz. This square wave burst signal is used as the clock signal to operate the microcontroller. The "MAN" button triggers the burst output waveform, while also sending a trigger output signal to additional test equipment. Additionally, to send a single clock cycle and increment the microcontroller through each instruction, the "1 CYCLE" button can be used. This allows the full stepping through of an instruction to verify how many clock cycles are necessary until the next instruction begins execution.

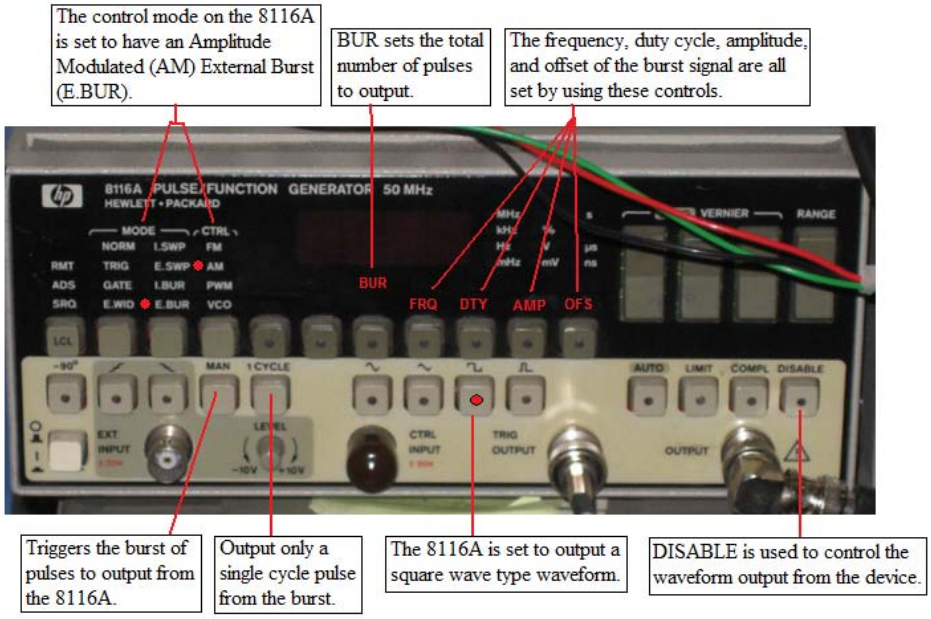


Figure 31. Photograph of the HP 8116A pulse/function generator used in the experiments.

Stanford Research DG535 Digital Delay/Pulse Generator:

The Stanford Research DG535 Digital Delay/Pulse Generator (Figure 32), which is triggered by the burst output of the 8116A function generator, is used to trigger the oscilloscope for data collection and to synchronize the RF injection pulse to occur for a set duration during a specific target instruction. Channel A ⊓ B is set to send a pulse output starting at 0 seconds (exactly when it is triggered) and stay high for a duration of 1 second. This is to ensure the DG535 is not triggered additional times during the 8116A burst signal. Additionally, channel A ⊓ B triggers the oscilloscope and initializes the data collection at the beginning of the burst output. Channel C ⊓ D is set to output a pulse beginning at the specific moment of a target location of the target instruction on the microcontroller.

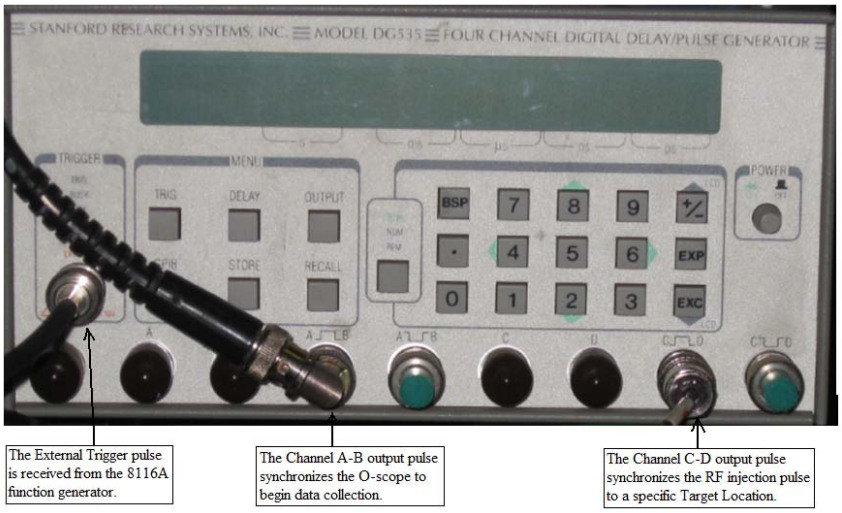


Figure 32. Photograph of the Stanford Research DG535 4-channel digital delay/pulse generator used in the experiments.

HP83620A Synthesized Sweeper:

To generate the IEMI signal, an HP83620A Synthesized Sweeper (Figure 33) is used as the RF source. The injected RF signal is set as a continuous wave (CW) and fixed at a frequency of 50 MHz throughout the test experiment, while the power level is varied between shots as part of characterizing the instruction susceptibility. For the RF output, the C ⊓ D channel on the DG535 is connected to the pulse input of the sweeper. The mode of the sweeper is set to external pulse, which means that while the C ⊓ D is sending a pulse, the RF output of the sweeper will turn on for the full duration. When the C ⊓ D is no longer a logic high value, the sweeper will no longer output an RF signal. The RF output signal is directly coupled into the microcontroller XTAL1 signal line, along with the external clock signal from the 8116A function generator.

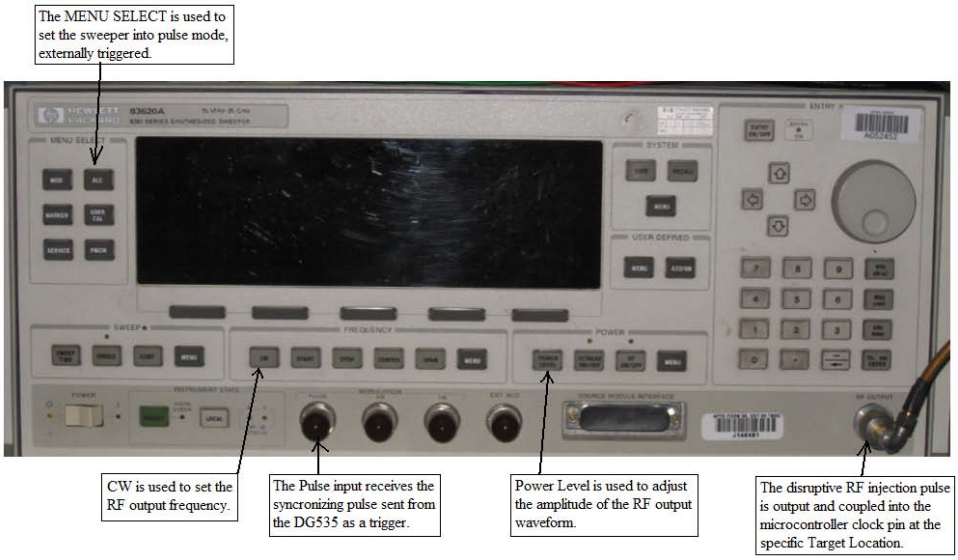


Figure 33. Photograph of the HP 83620A synthesized sweeper used in the experiments.

Tektronix DPO3054 Digital Oscilloscope:

To collect waveform data, a Tektronix DPO3054 digital oscilloscope (Figure 34) is used. The scope is triggered by the auxiliary input (Aux In), where the DG535 A ⊓ B channel triggers the oscilloscope. With the A ⊓ B channel set to immediately output a one second pulse, the data collection begins when the clock burst is manually triggered from the 8116A function generator.

The primary data captured by the scope is the target clock pulse, which includes the coupled RF injection signal, and is captured on channel 1. Channel 2, 3, and 4 each monitor a separate output line on the microcontroller. Channel 2 monitors the system clock output, channel 3 monitors the P1.0 LSB output of the counter, and channel 4 monitors the P1.7 MSB output of the counter. The Agilent DSO90404A oscilloscope pictured in the test experiment is not used for this specific experiment and is therefore not discussed in detail.

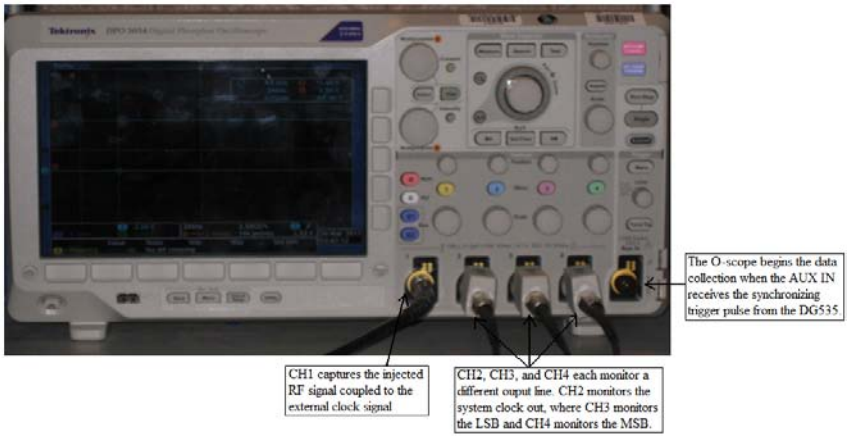


Figure 34. Photograph of the Tektronix DPO3054 digital oscilloscope used in the experiments.

3.5 Experimental Data Collection Procedures

To perform the experiment, the programmed LP2052 is mounted on the development board and set up with the equipment configured as previously explained. For taking shot data, the oscilloscope is triggered when the clock burst pulse is initialized, and the primary data is captured on channel 1. The data captured on channel 1 is that of the injected RF pulse coupled onto the external clock signal. For the external clock signal, the function generator is set to a fixed 999 clock pulse burst at a frequency of 1 MHz. With the set burst of clock pulses, the final output count of the up-counter under normal operation is at 0b01101100, requiring a single clock pulse to increment to 0b01101101. After applying an RF injection signal, the final counter value can be verified by applying one clock cycle at a time from the function generator to see if glitches occurred in the microcontroller operation (i.e., the counter is incremented past the expected value) or if an upset state has been induced.

When RF is injected into the clock signal line at a specific target location, disruptive effects to the counter output become more common as the RF power increases and approaches an approximate threshold value. When the RF power reaches the

threshold (which happens to be probabilistic in nature), the injected RF pulse causes the microcontroller to freeze operation and no longer count or register applied clock pulses. When this occurs, the microcontroller is considered to be in an upset state.

To record the results for each shot, a data acquisition table is used. The data table keeps track of the important data necessary to analyze each RF injection shot, ranging from the specific target location to the average peak voltage of the injected RF signal, where an example of the data table is provided as follows:

ShotNumber	TargetLocation	TestDevice	RFFrequency-MHz	RFStartTime-us	RFStopTime-us	RFTotalDuration-us	RFAvgPk-Volts	RFMaxPk-Volts	Upset
1	1	LP2052-1	50	8.84	10.78	1.94	0.4671	0.6228	0
2	1	LP2052-1	50	8.84	10.78	1.94	0.4943	0.5656	0
3	1	LP2052-1	50	8.84	10.78	1.94	0.4713	0.5702	0

Figure 35. Data acquisition table.

The data table consists of the following parameters:

1.) Shot Number. The shot number is in sequential order of when a shot was taken.

2.) Target Location. The target location of the target instruction is recorded in the second column. There are a total of 9 target locations, as shown in Figure 26.

3.) Test Device. The microcontroller model and the asset number are listed under the Test Device column. For this experiment, the LP2052 is the only microcontroller model being tested. There are two LP2052 test assets utilized in the experiment, where LP2052-1 is test device #1 and LP2052 is test device #2 in the data acquisition table.

4.) Injected RF Frequency (MHz). This column records the frequency of the injected RF pulse. In this current experiment, the frequency is held constant at 50 MHz.

5.) RF Injection Start Time (μs). The RF injection start time records the setting of the DG535 at time C for when the pulse outputs from channel C ⊓ D. This synchronizes the RF injection to a specific target location. The recorded value is ~60 ns before the

theoretical value of each target location. This is due to a slight delay in the test equipment and is necessary to achieve precise synchronization.

6.) RF Injection Stop Time (μs). The RF injection stop time is the setting of the DG535 at time D for when the pulse ceases to output from channel C ⌐ D. This represents the end of the target location time and cuts off the RF injection pulse.

7.) Total Duration of the RF Injection Pulse (μs). The total duration of the RF injection pulse is recorded by subtracting the start time from the stop time. This value correlates with the total duration of the specific target location.

8.) Average RF Peak Voltage. The average RF peak voltage is the average value of all of the peak voltages included in the injected RF pulse at a target location.

9.) Maximum RF Peak Voltage. The maximum RF peak voltage is the highest peak value during an RF injection into a target location.

10.) Upset. The upset column indicates whether or not the RF injection pulse caused an upset state to the microcontroller at a specific target location. A ‘0’ represents that no upset occurred, whereas a ‘1’ represents that an upset did occur.

To characterize the susceptibility at each target location, three parameters are necessary from the data acquisition table: the target location, the average RF peak voltage, and the upset indicator value (‘0’=no upset, ‘1’=upset effect). In the experiment, data was collected for two LP2052 microcontroller devices and the susceptibility at each target location on each of the devices was characterized. The characterization was performed for each target location by generating a probabilistic model of the upset effect based on Bayesian statistics. This requires many repetitive shots at each target location on each device, where the only varied parameter between each shot at a specific target

location is the power level of the injected RF signal. To give an idea as to how many shots were necessary, Appendix B provides a complete record of the shot data, where it can be seen that a target location typically required 50 to 150 shots on each device in order to characterize its susceptibility level.

To measure the average peak voltage, the waveform data recorded on channel 1 of the oscilloscope requires additional processing. Each shot is saved to the data acquisition computer from the oscilloscope, where an example of the channel 1 through channel 4 measurement data is shown in Figure 36. The channel 1 data is the important data for this experiment, where channels 2-4 provide secondary data for future investigations.

Additionally, it can be seen how the injected RF waveform is coupling throughout the internals of the microcontroller and creating added noise on the channel 2-4 output lines.

An important aspect to note about the external clock signal is that it is not a perfect square wave signal. This is due to a slight impedance mismatch between the function generator and the synthesized sweeper. The mismatch caused negligible clock signal degradation, especially compared to the alternate methods that were attempted to resolve the mismatch. Moreover, the system clock out measured on channel 2 demonstrates how the microcontroller was able to quantify the external clock signal into a well-defined square wave (logic levels are clearly defined, along with a 50% duty cycle). These alternate methods attempting to resolve the mismatch are included in the Chapter 5 discussion.

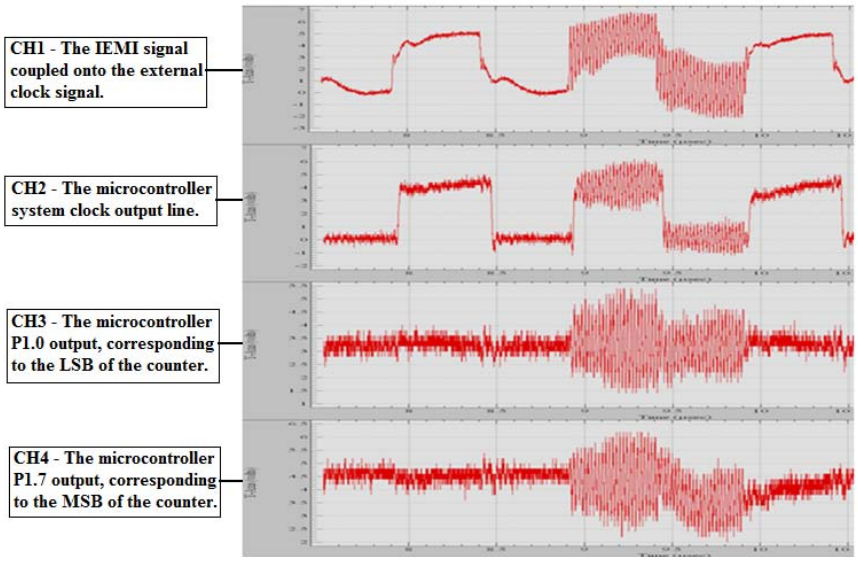


Figure 36. The oscilloscope Channel 1 through Channel 4 data measurements for two complete clock cycles. The channel 1 data is the important data for this experiment.

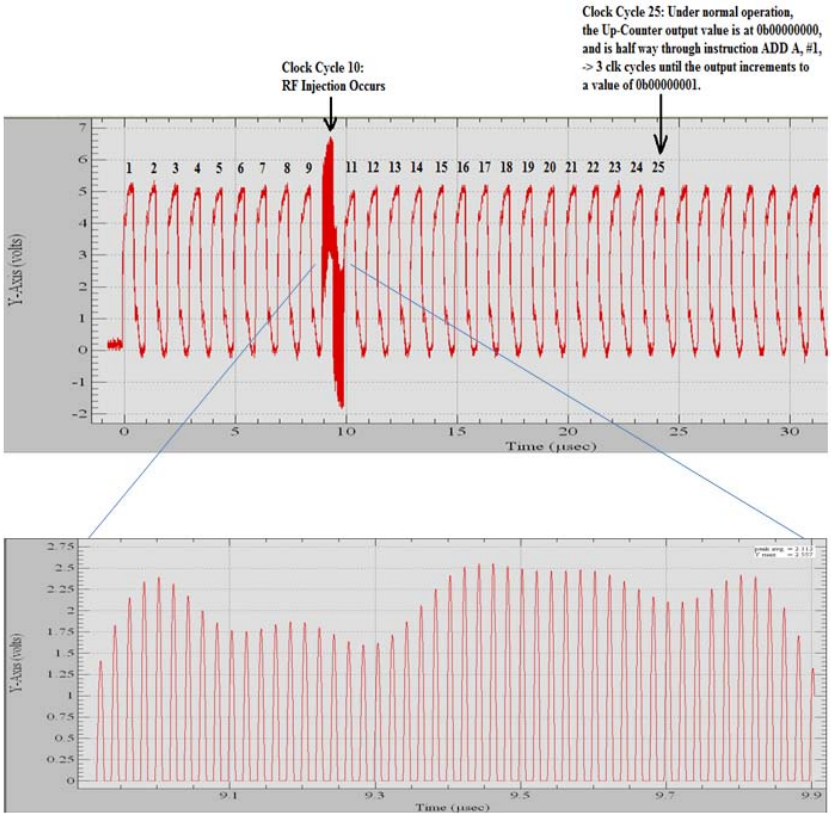


Figure 37. The waveform for each shot at each target location is processed through data acquisition software to extract the peak voltage values of the injected RF waveform. With the RF peak values, an average is taken to quantify the relative power level of the injected signal. This example shows the peak RF voltages extracted from an IEMI signal injected at Target Location 1, which corresponds to the complete instruction cycle.

For the measurements on channel 1, specific functions are applied to the original waveform to extract the peak values of the 50 MHz RF injection signal. An example of the extracted RF peak value waveform is shown in Figure 37. To process the waveform and extract the average peak voltage for each disruptive RF waveform, a data acquisition software known as 'DAAAC, version 4.0', developed by Voss Scientific, is used.

To process a waveform through DAAAC, a database for the process must first be created. In the new database, an arbitrary instrument with a single channel needs to be defined in order to process a waveform through a signal chain. Within the instrument channel, a process is defined as a 50 MHz band-pass filter. This process extracts the 50 MHz RF signal from the 1 MHz external clock signal. A second process is defined to clip the waveform to a time window equivalent to the total duration of the target location for which the data is being processed. To finish the configuration, figures of merit (FOMs) are defined to provide the average peak voltage of a processed waveform, along with the maximum peak voltage of the waveform.

Next, through the DAAAC analyze window, the 'Import Waveforms…' option is selected. This allows a series of waveforms to be imported into the acquisition software all at once. Therefore, all the shot data for a specific target location and a specific test device can be imported into the software at the same time. With the waveforms imported, the 'Reduce Processed' option is selected in the Analyze window and the waveforms to be processed through the defined signal chain are selected. The average peak value of an injected waveform is now extracted and can be directly correlated to an upset effect. Using the DAAAC software to process and extract data from the original waveforms is outlined in Figures 38-45.

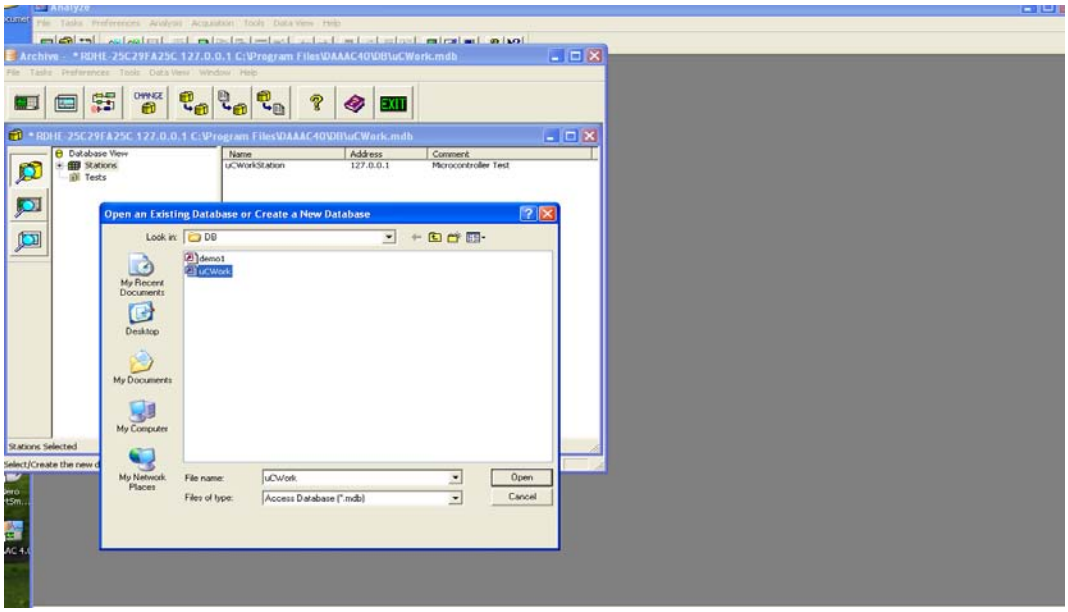


Figure 38. A new database is defined in the DAAAC software.

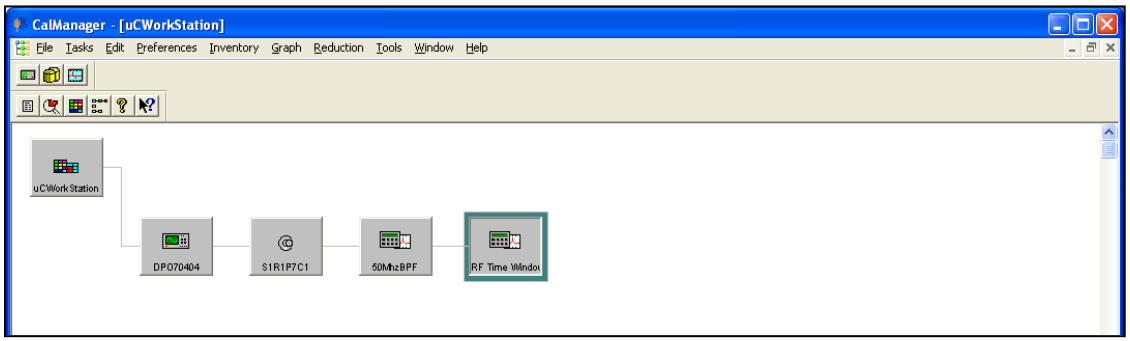


Figure 39. In the new database, an arbitrary channel is created, where a signal chain can be defined to process waveforms.

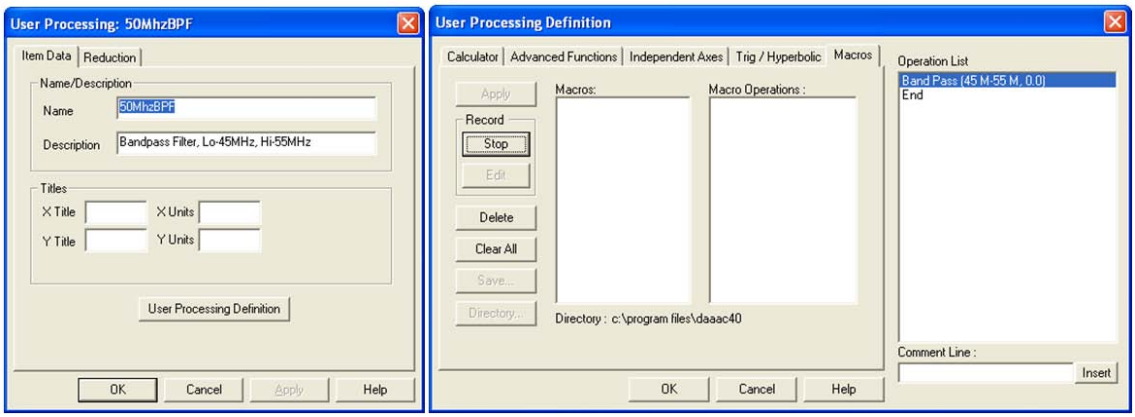


Figure 40. A 50 MHz band-pass filter is defined in the signal chain to extract the injected RF signal.

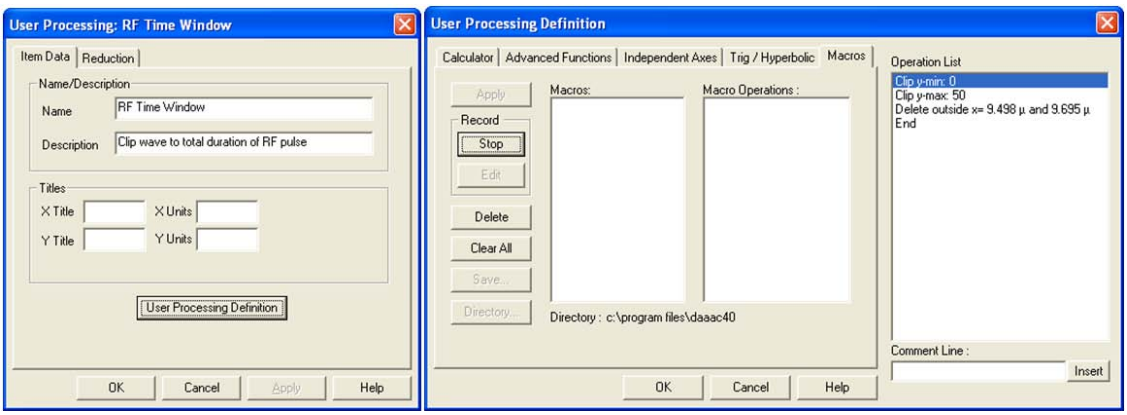


Figure 41. A window is defined to for the time duration of the injected RF signal. This time duration is equivalent to the corresponding target location time window.

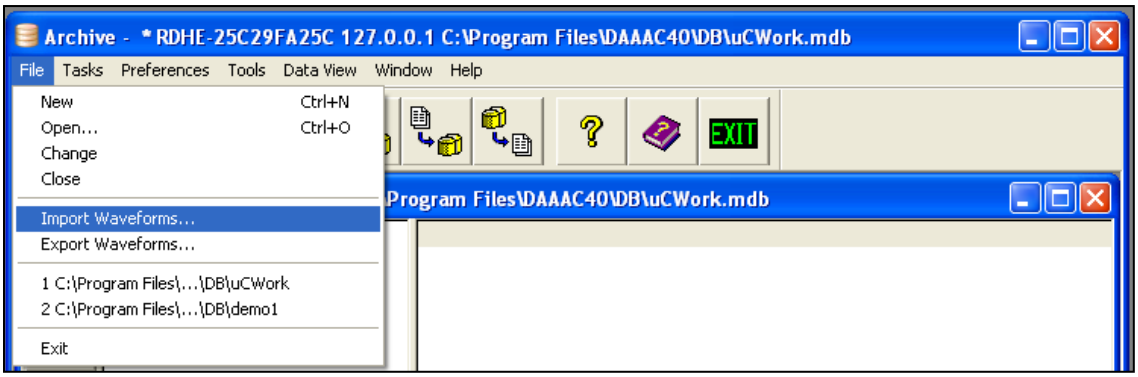


Figure 42. The 'Import Waveforms…' command is selected under the File Menu in the Archive window.

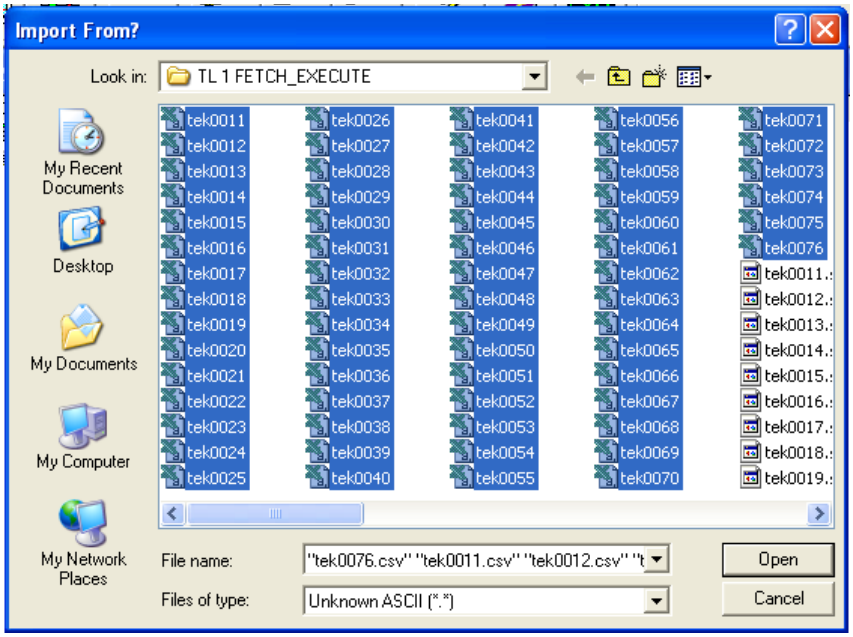


Figure 43. The files for a specific target location (corresponding to the time window process previously defined) are selected all at once for import.

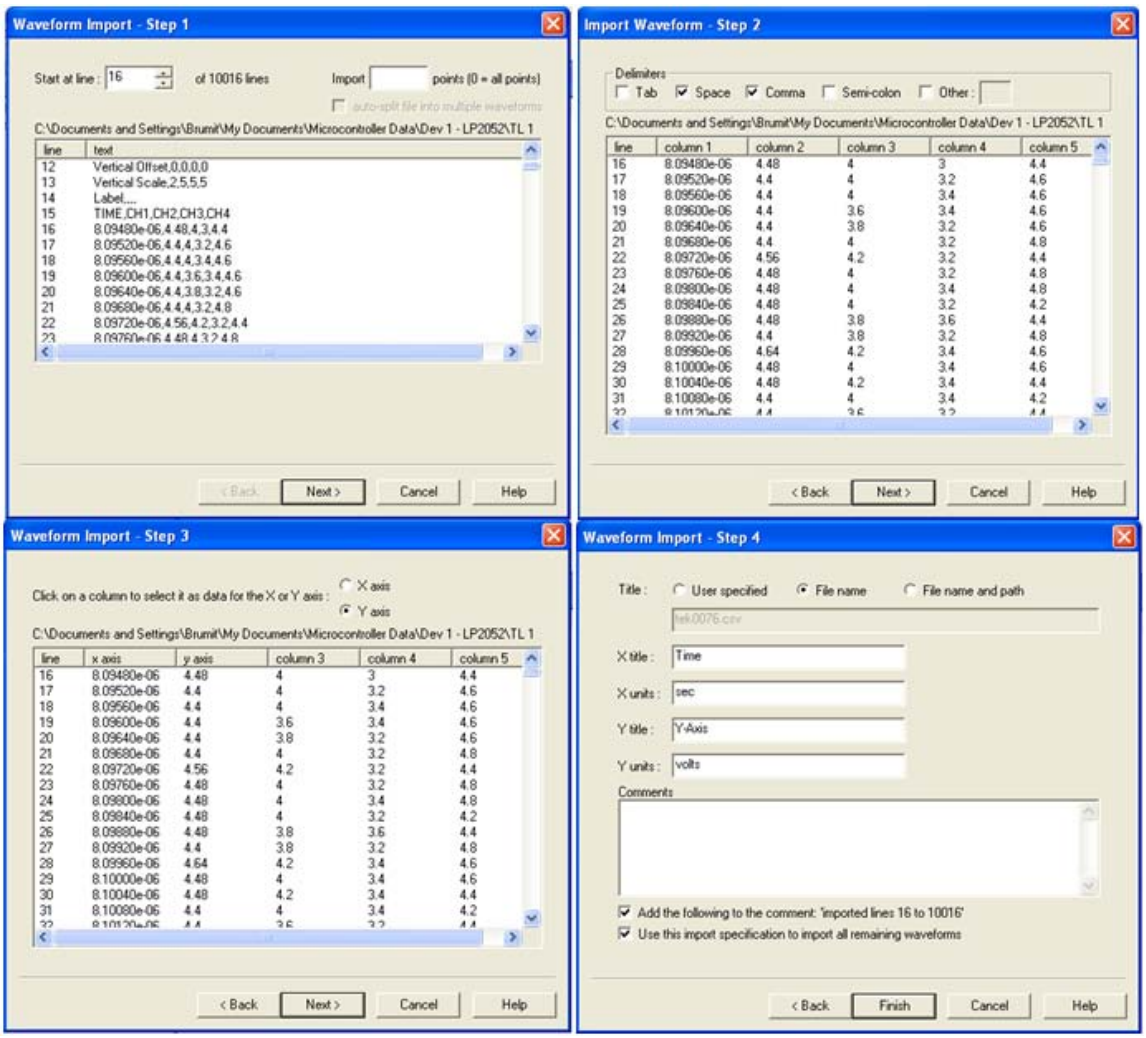


Figure 44. Completing the data import is a four step process. Step 1 selects the line in the data file where the actual data begins. Step 2 selects how to separate different data columns within the file. Step 3 sets the X axis and the Y axis to specific data columns. Step 4 allows the axes to be titles and the units to be defined, along with the option to apply the same settings to all data files being imported.

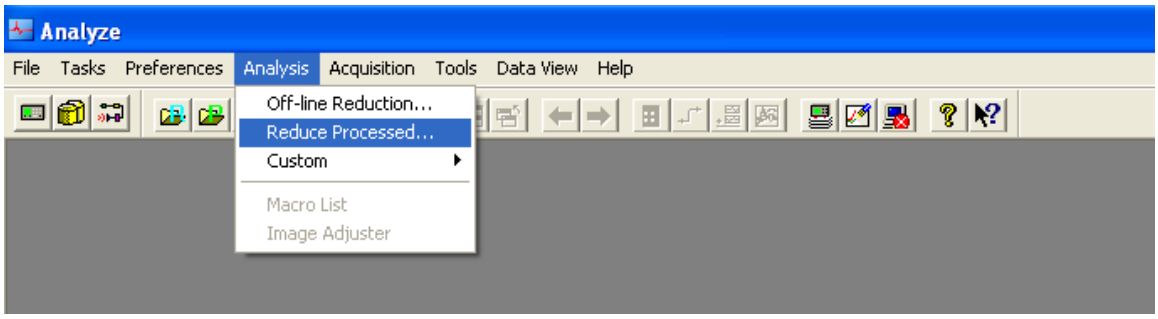


Figure 45. The 'Reduce Processed…' command is selected in the Analyze window. Select all the newly imported data to be processed and it will process it through the signal chain on the specified channel. The average RF peak voltage is now acquired.

Chapter 4 Experimental Results

Following the data acquisition and the data processing, probability of effects (P_E) curves were generated for each LP2052 test device at each target location by using the proprietary software 'ANODE', developed by AFRL/RDHE. ANODE applies a Bayesian analysis method to generate a P_E curve for predicting future upsets based on the upset effect results of a series of previous shots, where applied relative power is the controlled variable in each shot of a series.

Figure 46 provides a recap of the previously defined target locations for the target instruction at clock cycle 10, where P_E curves were generated for two devices of the same model for each of the nine target locations. For the P_E curve data, the Y-axis is defined as the probability of an upset effect between 0 and 1. The X-axis is defined as the average peak voltage of the disruptive IEMI waveform, and is set in a $\log_{10}$ scale between 0.1 to 10. Furthermore, the blue line represents the calculated P_E value, where the red line represent a 95% confidence boundary. At a P_E=50%, a blue marker is placed on the X-axis to help identify the corresponding average peak voltage.

Figures 47-55 provide the generated P_E curves for each target location, where each test device is paired together for the associated target location. The level of steepness on the P_E curves helps to identify the threshold voltage range required to induce an upset. This threshold voltage range is an equivalent parameter to the breakdown bandwidth parameter previously defined in Chapter 1.3.

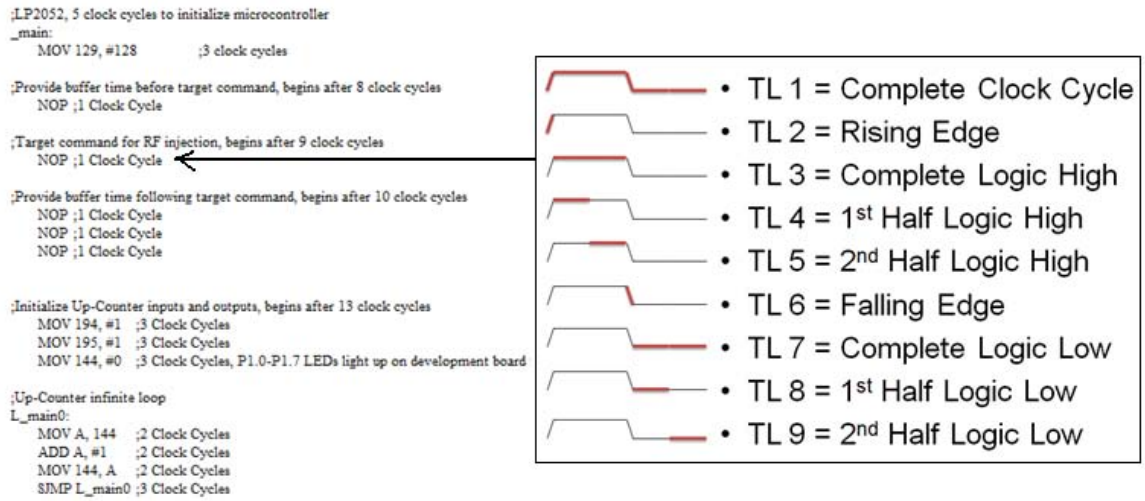
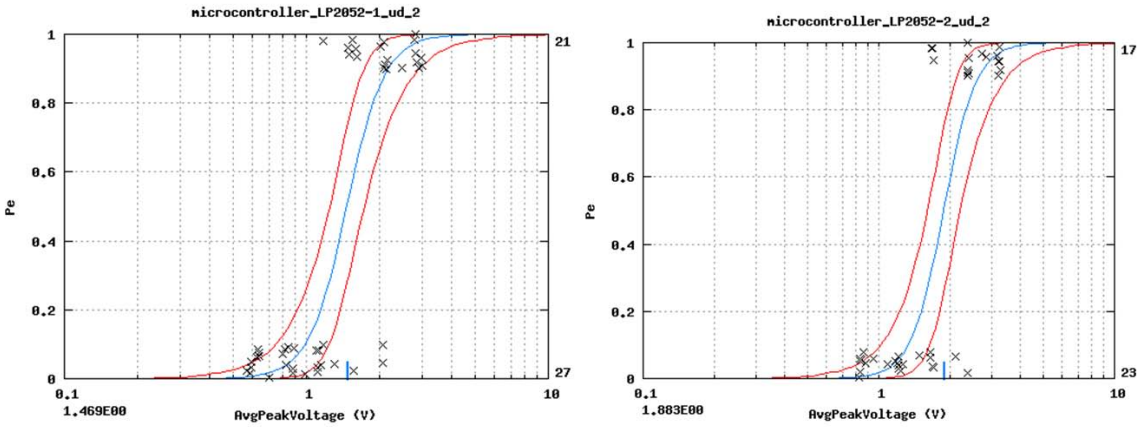


Figure 46. The defined Target Locations for the Target Instruction (clock cycle 10).

Target Location 1: Clock Cycle 10, One Complete Instruction Cycle:

The P_E curves generated for Target Location 1 cover an RF injection signal synchronized to the entire clock cycle 10 of the programmed assembly code. It can be seen that the results between the two devices at Target Location 1 are approximately equal and are within 0.5 dB of each other for the P_E=50%. Furthermore, the slope throughout each P_E curve is approximately the same for both devices, indicating a similar range required to induce an upset at this target location.

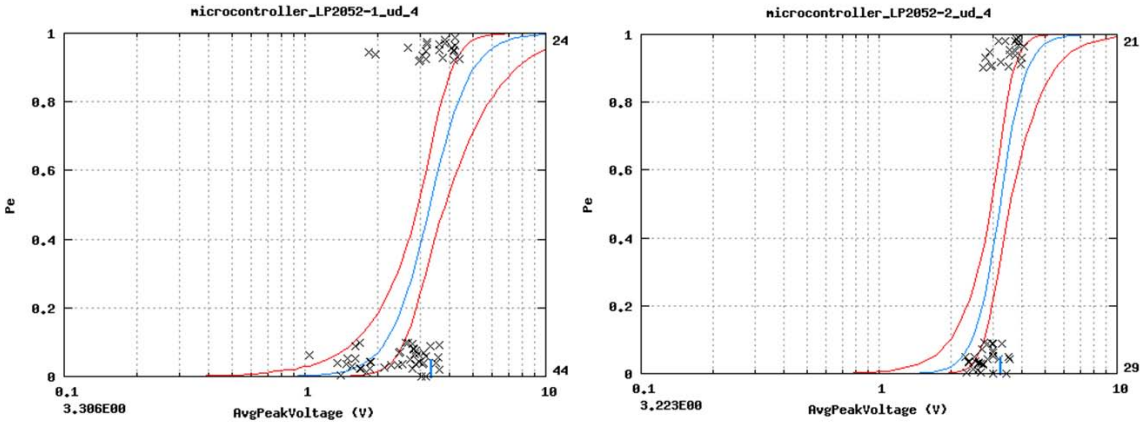


(a) LP2052 Device #1 (b) LP2052 Device #2

Figure 47. Target Location 1, Clock Cycle 10, Complete Cycle.

Target Location 2: Clock Cycle 10, The Rising Edge Transition of the Cycle:

The P_E curves generated at Target Location 2 cover an RF injection signal synchronized to the rising edge transition for clock cycle 10. The rising edge transition is defined for a slightly longer duration than the actual rising edge (i.e., 10% to 90%). A slight overlap with the tail end of clock cycle 9's Low and a slight overlap on the very beginning of clock cycle 10's High is defined in the transition location. This overlap is introduced to provide adequate rise time (~10s of ns) of the injected RF pulse to reach consistent peak values throughout the entire transition. It can be seen that the results between the two devices at Target Location 2 are approximately equal for the P_E=50%. Furthermore, the slope throughout each P_E curve is approximately the same for both devices, indicating a similar range required to induce an upset at this target location.



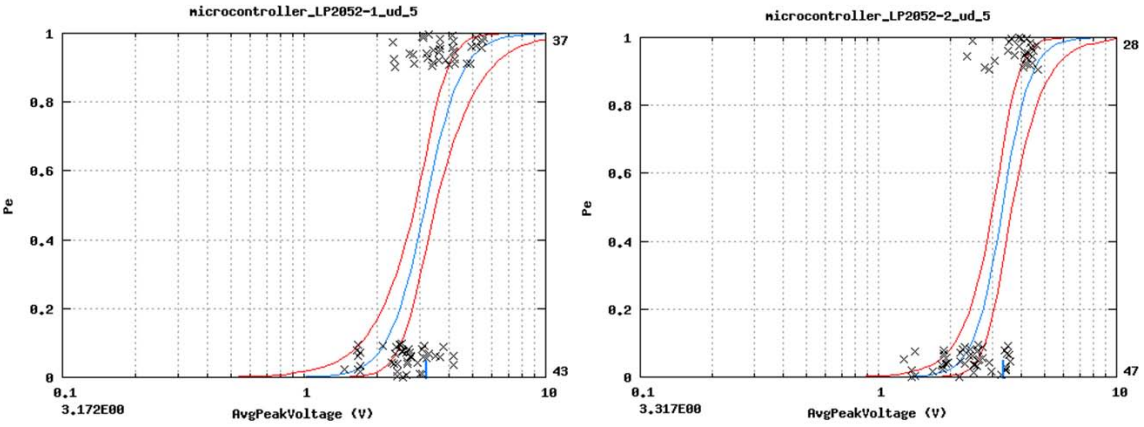
(a) LP2052 Device #1 (b) LP2052 Device #2

Figure 48. Target Location 2, Clock Cycle 10, Rising Edge Transition.

Target Location 3: Clock Cycle 10, The Complete Logic High of the Cycle:

The P_E curves generated for Target Location 3 cover an RF injection signal synchronized to the complete logic high of clock cycle 10. It can be seen that the results between the two devices at Target Location 3 are approximately equal and are within 0.5 dB of each other for the P_E=50%. Furthermore, the slope throughout each P_E curve is

approximately the same for both devices, indicating a similar range required to induce an upset at this target location.

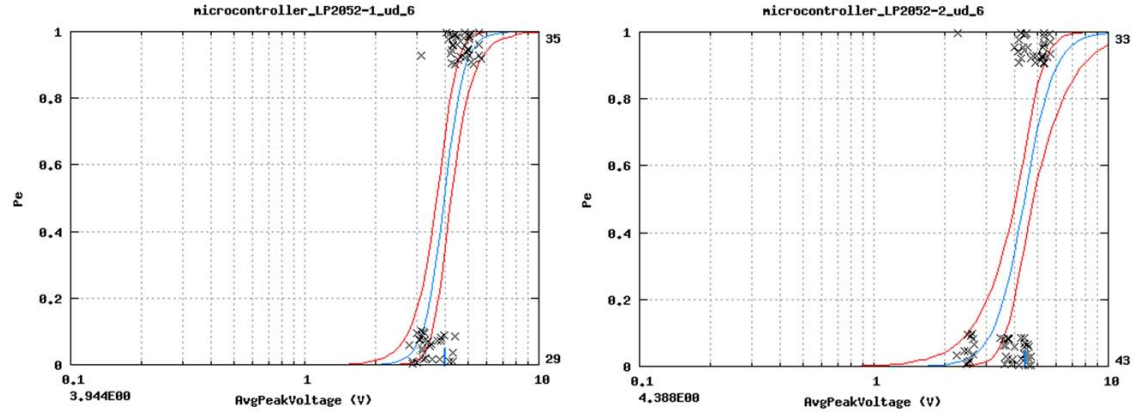


(a) LP2052 Device #1 (b) LP2052 Device #2

Figure 49. Target Location 3, Clock Cycle 10, Complete Logic High.

Target Location 4: Clock Cycle 10, 1st Half of the Logic High of the Cycle:

The P_E curves generated for Target Location 4 cover an RF injection signal synchronized to the 1st half of the logic high of clock cycle 10. It can be seen that the results between the two devices at Target Location 4 are approximately equal and are within 0.5 dB of each other for the P_E=50%. Furthermore, the slope throughout each P_E curve is approximately the same for both devices, indicating a similar range required to induce an upset at this target location.

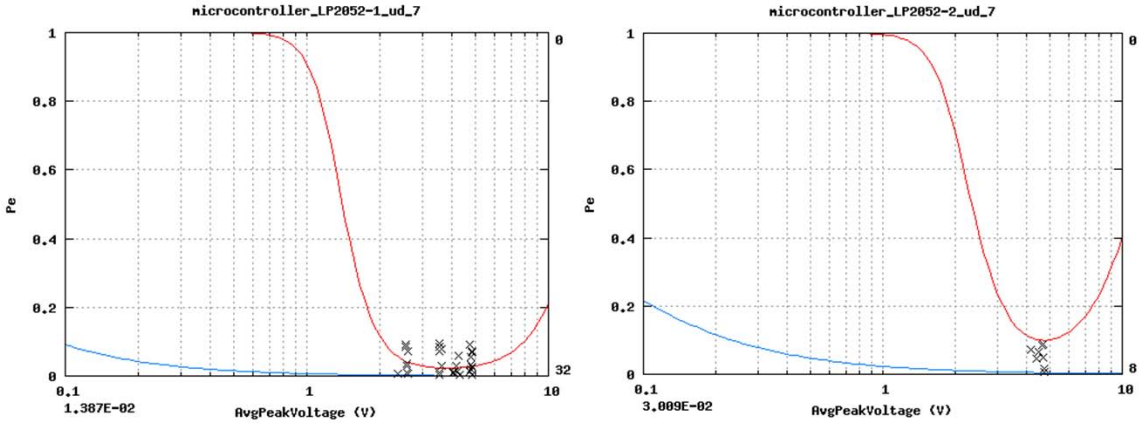


(a) LP2052 Device #1 (b) LP2052 Device #2

Figure 50. Target Location 4, Clock Cycle 10, 1st Half of Logic High.

Target Location 5: Clock Cycle 10, 2nd Half of Logic High of the Cycle:

The P_E curves generated for Target Location 5 cover an RF injection signal synchronized to the 2nd half of the logic high of clock cycle 10. At Target Location 5, a maximum output power from the RF source was achieved, yet unable to produce an upset effect at the target location on both devices. An RF source with a higher power out would be required to further characterize the susceptibility at Target Location 5, but is unnecessary within the scope of this thesis.



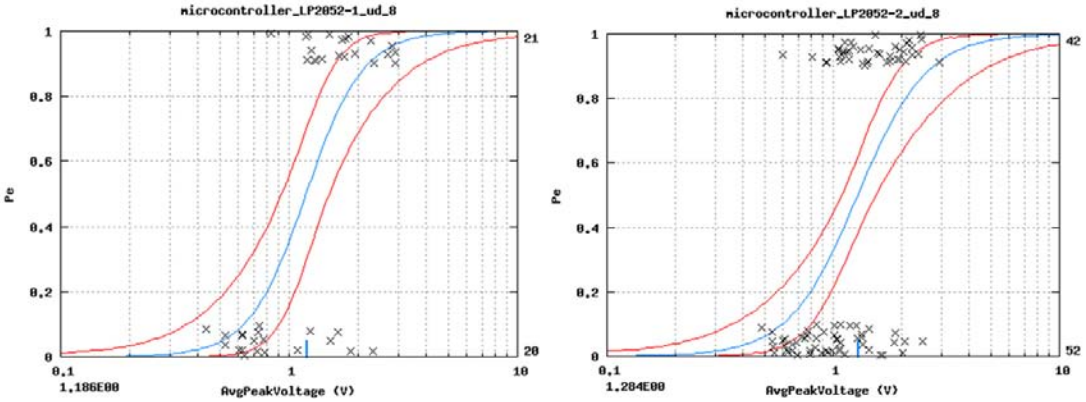
(a) LP2052 Device #1 (b) LP2052 Device #2

Figure 51. Target Location 5, Clock Cycle 10, 2nd Half of Logic High.

Target Location 6: Clock Cycle 10, The Falling Edge Transition of the Cycle:

The P_E curves generated at Target Location 6 cover an RF injection signal synchronized to the falling edge transition for clock cycle 10. The falling edge transition is defined for a slightly larger duration than the actual falling edge (i.e., 10% to 90%), similar to how Target Location 2 was defined. A slight overlap with the tail end of clock cycle 10's High and a slight overlap on the very beginning of clock cycle 10's Low is defined in the transition location. This overlap is introduced to provide adequate rise time (~10s of ns) of the injected RF pulse to reach consistent peak values throughout the entire transition. It can be seen that the results between the two devices at Target Location 6 are

approximately equal for the P_E=50%. Furthermore, the slope throughout each P_E curve is approximately the same for both devices, indicating a similar range required to induce an upset at this target location. Additionally, Target Location 6 resulted in the lowest average peak voltage necessary to induce a P_E=50%. The slope for the curves was also the smallest among all the target locations, indicating Target Location 6 has the widest range of average peak voltage values that will induce an upset.



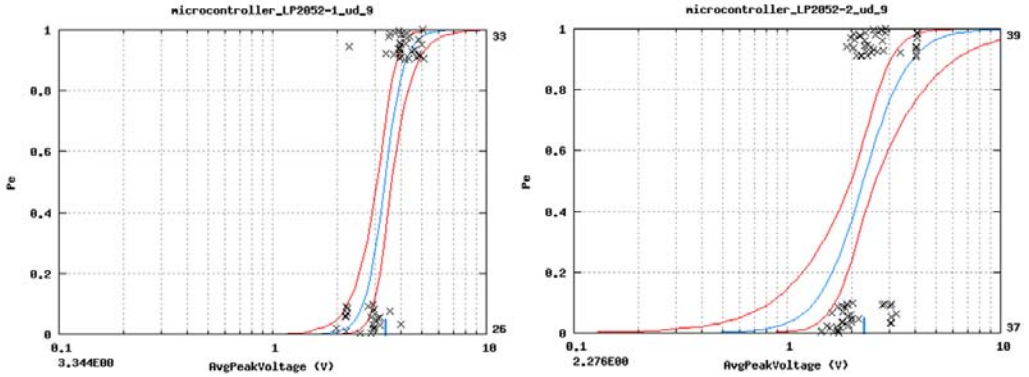
(a) LP2052 Device #1 (b) LP2052 Device #2

Figure 52. Target Location 6, Clock Cycle 10, Falling Edge Transition.

Target Location 7: Clock Cycle 10, The Complete Logic Low of the Cycle:

The P_E curves generated for Target Location 7 cover an RF injection signal synchronized to the complete logic low of clock cycle 10. Target Location 7 was the only location where the P_E curves did not agree with each other between the two test devices. The difference between the P_E=50% is approximately 1dB and the slope for device #1 is observably steeper compared to the slope for device #2. The difference between the two test devices requires further investigation. Susceptibility characterizations on additional LP2052 test devices could provide insight into the discrepancy between the two P_E curves. Furthermore, as will be discussed in more detail in Chapter 5, the difference could be due to the two identified types of upset having different susceptibility levels at this specific target location. This reason is suggested in Figure 53(b), where there is an

approximate 1 dB gap between two groupings of data for values that do or do not cause an upset effect.

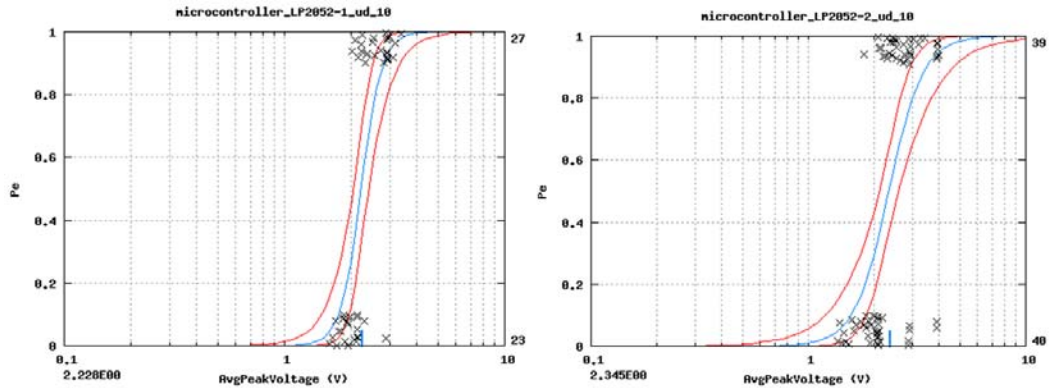


(a) LP2052 Device #1 (b) LP2052 Device #2

Figure 53. Target Location 7, Clock Cycle 10, Complete Logic Low.

Target Location 8: Clock Cycle 10, 1st Half of the Logic Low of the Cycle:

The P_E curves generated for Target Location 8 cover an RF injection signal synchronized to the 1st half of the logic low of clock cycle 10. It can be seen that the results between the two devices at Target Location 8 are approximately equal and are within 0.5 dB of each other for the P_E=50%. The slop for (b) appears to be less than (a), but the results for each device are still in good agreement. Susceptibility characterization of additional test devices at the target location could be performed to further verify this agreement.

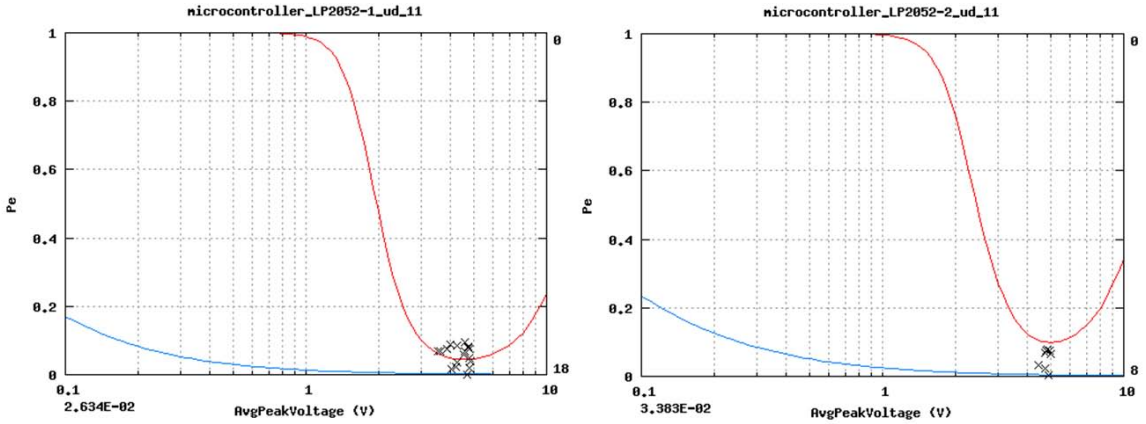


(a) LP2052 Device #1 (b) LP2052 Device #2

Figure 54. Target Location 8, Clock Cycle 10, 1st Half of Logic Low.

Target Location 9: Clock Cycle 10, 2nd Half of Logic Low of the Cycle:

The P_E curves generated for Target Location 9 cover an RF injection signal synchronized to the 2nd half of the logic low of clock cycle 10. At Target Location 9, a maximum power output from the RF source was achieved, yet unable to produce an upset effect at the target location on both devices. An RF source with a higher power out would be required to further characterize the susceptibility at Target Location 9, but is unnecessary within the scope of this thesis.



(a) LP2052 Device #1 (b) LP2052 Device #2

Figure 55. Target Location 9, Clock Cycle 10, 2nd Half of Logic Low.

Summary of P_E=50% with Confidence Bounds for All Target Locations:

Figure 56 provides a summarized comparison between the P_E=50% with 95% confidence bounds for all 9 target locations. In this summary, it can be seen that 8 out of 9 target locations are in excellent agreement for the two test devices. This data clearly shows that different locations within an instruction cycle have a different susceptibility level on the LP2052 microcontroller, where the results are consistent between two devices.

This data provides a basis for research on using software to map out susceptible functional blocks of a microcontroller by correlating the functional block to the associated action of a specific target location. Follow-on research efforts are discussed in Chapter 5.

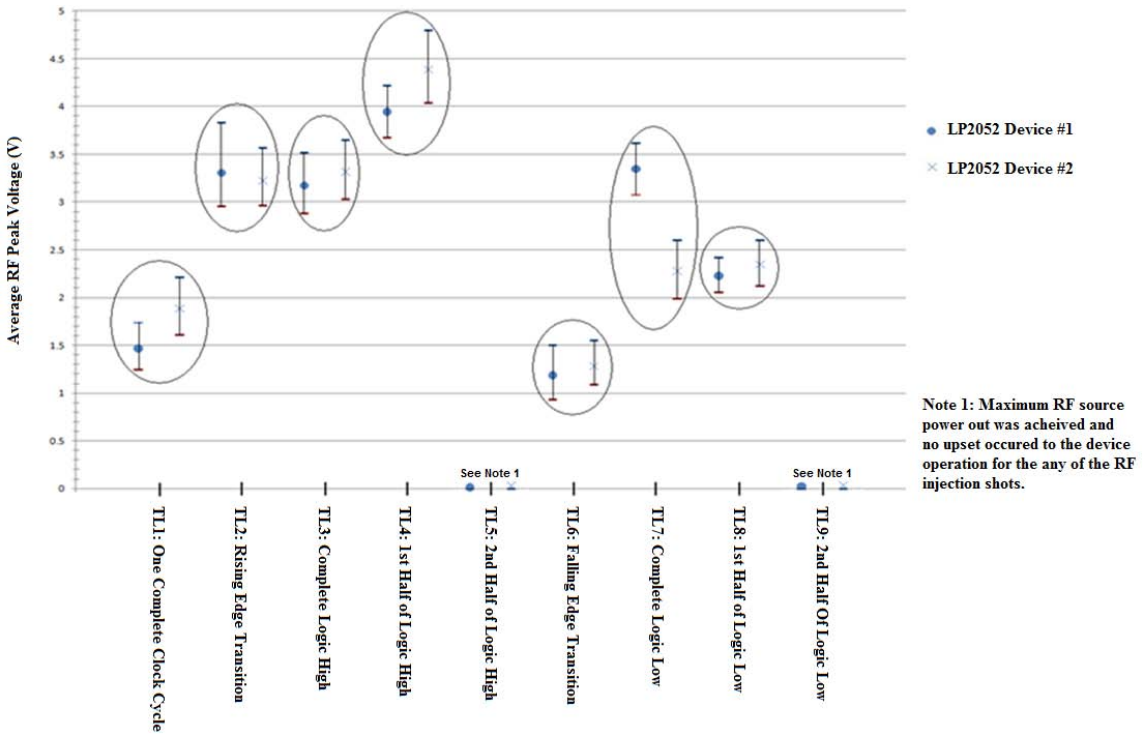


Figure 56. The probability of effect for each target location. The LP2052 test devices, #1 and #2, are paired together at each location. 8 out of 9 target locations are in perfect agreement for the two test devices.

Chapter 5 Discussion and Conclusion

5.1 Secondary Experimental Observations

Throughout the experiment, additional observations were noted that did not directly apply to the experiment at hand. The first observation made was that the IEMI signal would sometime cause a delay in the microcontroller outputs P1.0 to P1.7, but resulted in a correct counter output value expected under normal operation. A second observation was that as the power level of the injected RF signal increased, the microcontroller registered additional clock cycles due to the interference. A third observation that occurred was that there were two identifiable types of upset effects, although they were both quantified together throughout the experiment.

For the first type of observation, the injected RF signal would sometimes cause a delay in the microcontroller outputs at port P1, where LEDs on the development board provided a visual indication of the output values. For this delay, an observable time difference between output values could be visually recognized on the development board. For example, when the IEMI signal caused the delay, P1.0-P1.4 may initialize at the time expected, whereas P1.5-P1.7 may initialize a half-second to a second later. Typically, the final counter output value would result in the correct output value for the number of applied clock pulses, even though the observable delay occurred at initialization. This effect typically occurred at lower RF power levels compared to power levels required to induce an upset effect and requires further investigation.

The second observation made throughout the experiment occurred when injected RF power level increased but did not cause the microcontroller to enter into an upset state. At these power levels, the induced RF signal caused additional clock pulses to be

registered by the microcontroller. At power levels just above the levels necessary to cause the output delay effect, one additional clock pulse might be registered by the microcontroller compared to normal operation. As the power output from the RF source increased towards the levels necessary to cause an upset effect for a given target location, more clock pulses tended to be registered. The highest number of additional clock pulses observed throughout the experiment was 8 additional pulses, but usually only between 1 to 5 additional clock pulses were registered by the microcontroller. This may be a function of the total number of 50 MHz cycles injected by the RF source for the duration of the specific target location. Further investigation into this observation could help develop an understanding as to how output bit errors relate to the injected RF pulse duration and the upset effects.

A third observation made throughout the experiment was that two different types of upset effects occurred. The first type of upset effect resulted in a locked-logic output state in one or more of the output leads P1.0 through P1.7. Typically, when this type of upset occurred, only P1.0 would respond to the clock signal while P1.1 through P1.7 remained in a locked-logic High state until the microcontroller power was cycled through (ie, turn off, turn on). Following the power cycle, the microcontroller would resume normal operation.

The second upset state identified resulted in the output port P1 locking up with all pins High, where, consistently, the addition of approximately 4000 clock cycles re-initialized the microcontroller back to normal operation. This consistent number of clock cycles required for the microcontroller to self-recover would suggest that an internal timer circuit is built into the microcontroller to help protect against disruptive effects

caused by noisy input signals. On a few shots, the self-recovery initialized around 1500 clock pulses, but this type of self-recovery was a very rare occurrence.

Furthermore, although throughout this experiment the two types of upset occurred with a fairly similar probability, the two upset states may have slightly different susceptibility levels. If the susceptibility levels are different, further investigation could possibly reveal the reason for the discrepancy between the two test device susceptibility levels found at Target Location 9. This observation requires further investigation and would require large amounts of shot data to be recorded for each target location and each test device in order to generate separate P_E curves at each location for each of the two observed upset states. The data collection for the overall experiment maintains a record of the type of upset for each shot. Therefore, this data can be utilized in future experiments to investigate into the two upset states.

5.2 Future Experiments

Based on the experimental results presented in Chapter 4, follow-on experiments are currently being planned for the next steps in the research. One of the follow-on experiments is to characterize the susceptibility levels for different types of target instructions, but at the same target locations defined in Chapter 3. A second follow-on experiment to be performed is to repeat the experiments from the LP2052 microcontroller on the AT89S2051 microcontroller and compare the results between the two 8051-core microcontrollers.

For the first follow-on experiment, the susceptibility of different types of target instructions at the 9 original target locations is to be characterized. The MSC-51 instruction set consists of the following different types of instructions: Arithmetic,

Logical, Data Transfer, and Bit. The full instruction set is listed in Appendix A and details the type of each instruction in the set. By characterizing the susceptibility of each type of instruction, the susceptibility levels of each target location can be compared to each other. This may allow similar actions within different instruction types to be identified and associated with the microcontroller's internal hardware. This experiment is to further investigate into the feasibility of mapping susceptible instruction actions to the 8051-core architecture, which now has a basis for investigation based on the results in Chapter 4.

For the second follow-on experiment, the same experiments performed on the LP2052 will be performed on the S2051 microcontroller. The S2051 microcontroller processes instruction serially, so will therefore require a newly defined set of target locations. By performing fairly identical experiments on the S2051, commonalities between upset effects and the actions performed within an instruction can be identified. By identify common susceptibilities between the parallel and the serial processing microcontrollers, it may be possible to identify upset mechanisms within the core 8051-microcontroller (and potentially within other families of microcontrollers). Identifying upset mechanisms common among various types of microcontrollers is a key aspect involved in the development of a predictive model and is part of the research effort being performed by AFRL/RDHE at Kirtland AFB, NM.

5.3 Experimental Difficulties

Within the experimental setup described in Chapter 3, various difficulties in carrying out the experiment had to be overcome. The biggest difficulty to overcome was developing a way to quantify susceptibility at each target location. The second biggest

difficulty was in minimizing the impedance mismatch the synthesized sweeper caused to the external clock signal.

To develop a way to quantify susceptibility at each target location, multiple parameters had to be defined. Determining what constituted being an upset state or not was the first parameter that required defining. Based on pre-experimental observations, it was decided that an upset state would qualify as any state that caused the microcontroller to either enter a self-recovery state or required a power cycle to resume normal operation. Although these two upset states are associated with clearly different effects, they occurred at similar power levels as previously mentioned in Chapter 5.1. Therefore, they were grouped together into the overall category defined as an upset state.

A second parameter that required a quantifying definition was the susceptibility level for a specific target location. Initially, it was thought that a deterministic voltage threshold would exist between a non-upset state and an upset state. The problem that existed in testing this hypothesis was related to having a slight instability with the RF source, where power levels tended to drift between shots, even though the power setting was fixed to specific value. It was observed that the injected waveforms maintained consistent peak to peak levels for any given shot; therefore, the peak average voltage for each shot could be calculated. With an identifiable parameter associated with an upset effect, P_E curves could be generated and used to identify relative susceptibility levels at each target location.

The second biggest difficulty to overcome was in dealing with the impedance mismatch caused by the conductive IEMI RF source (synthesized sweeper). In the initial experimental test setup, a microwave RF switch was being utilized to help isolate the RF

source from the external clock source. The difficulty in using this setup was that the RF switch introduced additional higher order harmonics within the injected RF signal. Furthermore, power levels necessary to consistently induce an upset effect were not achievable due to the additional attenuation introduced by the RF switch on the RF source injection line. Therefore, alternate methods were attempted to try and resolve this issue, such as using a splitter to combine the external clock signal with the RF source signal. These methods failed to properly isolate the two signals, and it was then discovered that the cleanest signal to generate required the least amount of additional test equipment. By using the sweeper in pulse mode and directly connecting the RF output line to the external clock line, a slight impedance mismatch caused degradation to the external clock signal, but allowed for a clean RF signal of 50 MHz to couple onto the clock signal at a target location. Although the clock signal was not an ideal square wave, the microcontroller recognized the signal as a square wave with 50% duty cycle and operated as expected under minimum RF injection levels. Therefore, the impedance mismatch was deemed negligible for the microcontroller experiment.

5.4 Conclusion

IEMI is a rising threat to the electronic systems that are used and depended upon in everyday life of civil society. To address this threat, it is important to develop an understanding of what IEMI is and how it can be used to disrupt sophisticated electronic systems. By understanding IEMI and its disruptive effects, predictive models and protection standard can be developed for various types of electronic systems to address the threat.

Experimental results were detailed throughout this investigation that involved characterizing the susceptibility of a single microcontroller instruction at different moments within the instruction cycle. The microcontroller device used throughout the experiment was the ATMEL AT89LP2052, which is an 8051-core based microcontroller device that processes instructions in parallel. The experiment involved targeting specific moments within an instruction cycle, based on the parallel processing of the LP2052, to determine whether or not different actions within the cycle have different susceptibility levels to IEMI.

Detailed in the Chapter 4 results, it was determined that susceptibility levels are different at defined target locations within the instruction cycle, yet consistent at each target location between two of the same microcontroller test devices. This research establishes a basis to initiate further investigation into the susceptibility level of different moments within an instruction cycle. A way forward is now provided in an effort to try and map out the susceptibility levels of the internal hardware of a microcontroller by correlating the functional blocks to the associated target locations within the software.

By being able to use software to map out the hardware susceptibility levels, a better understanding of the upset mechanisms can be achieved and possibly contribute to the development of a predictive model for IEMI induced upset in microcontrollers. A microcontroller represents a simplified system on a single chip. Therefore, by understanding the upset mechanisms within a microcontroller, similar upset mechanisms of more complex electronic systems may be identifiable. With the growing threat of IEMI, being able to identify upset mechanism and develop predictive models in electronic systems can significantly reduce this threat to everyday life of civil society.

Appendix A. MCS-51 instruction set, including the clock cycle requirements for standard 8051 microcontrollers compared to the AT89LP2052 microcontroller.

Table XI. Typical cycle count for general instruction types on the LP2052.

Instruction Type	Cycle Count
Most arithmetic, logical, bit and transfer instructions	# bytes
Branches and Calls	# bytes + 1
Single Byte Indirect (i.e. ADD A, @Ri, etc.)	2
RET, RETI	4
MOVC	3
MUL	2
DIV	4
INC DPTR	2

Table XII. Overview of MCS-51 arithmetic instructions.

		Clock Cycles		
Arithmetic Instruction	Bytes	8051	LP2052	Hex Code
ADD A, Rn	1	12	1	28-2F
ADD A, direct	2	12	2	25
ADD A, @Ri	1	12	2	26-27
ADD A, #data	2	12	2	24
ADDC A, Rn	1	12	1	38-3F
ADDC A, direct	2	12	2	35
ADDC A, @Ri	1	12	2	36-37
ADDC A, #data	2	12	2	34
SUBB A, Rn	1	12	1	98-9F
SUBB A, direct	2	12	2	95
SUBB A, @Ri	1	12	2	96-97
SUBB A, #data	2	12	2	94
INC Rn	1	12	1	08-0F
INC direct	2	12	2	05
INC @Ri	1	12	2	06-07
INC A	1	12	1	04
DEC Rn	1	12	1	18-1F
DEC direct	2	12	2	15
DEC @Ri	1	12	2	16-17
DEC A	1	12	1	14
INC DPTR	1	24	2	A3
MUL AB	1	48	2	A4
DIV AB	1	48	4	84
DA A	1	12	1	D4

Table XIII. Overview of MCS-51 logical instructions.

		Clock Cycles		
Logical Instruction	Bytes	8051	LP2052	Hex Code
CLR A	1	12	1	E4
CPL A	1	12	1	F4
ANL A, Rn	1	12	1	58-5F
ANL A, direct	2	12	2	55
ANL A, @Ri	1	12	2	56-57
ANL A, #data	2	12	2	54
ANL direct, A	2	12	2	52
ANL direct, #data	3	24	3	53
ORL A, Rn	1	12	1	48-4F
ORL A, direct	2	12	2	45
ORL A, @Ri	1	12	2	46-47
ORL A, #data	2	12	2	44
ORL direct, A	2	12	2	42
ORL direct, #data	3	24	3	43
XRL A, Rn	1	12	1	68-6F
XRL A, direct	2	12	2	65
XRL A, @Ri	1	12	2	66-67
XRL A, #data	2	12	2	64
XRL direct, A	2	12	2	62
XRL direct, #data	3	24	3	63
RL A	1	12	1	23
RLC A	1	12	1	33
RR A	1	12	1	03
RRC A	1	12	1	13
SWAP A	1	12	1	C4

Table XIV. Overview of MCS-51 data transfer instructions.

Data Transfer Instruction	Bytes	Clock Cycles		Hex Code
		8051	LP2052	
MOV A, Rn	1	12	1	E8-EF
MOV A, direct	2	12	2	E5
MOV A, @Ri	1	12	2	E6-E7
MOV A, #data	2	12	2	74
MOV Rn, A	1	12	1	F8-FF
MOV Rn, direct	2	24	2	A8-AF
MOV Rn, #data	2	12	2	78-7F
MOV direct, A	2	12	2	F5
MOV direct, Rn	2	24	2	88-8F
MOV direct, direct	3	24	3	85
MOV direct, @Ri	2	24	2	86-87
MOV direct, #data	3	24	3	75
MOV @Ri, A	1	12	1	F6-F7
MOV @Ri, direct	2	24	2	A6-A7
MOV @Ri, #data	2	12	2	76-77
MOV DPTR, #data16	3	24	3	90
MOVC A, @A+DPTR	1	24	3	93
MOVC A, @A+PC	1	24	3	83
PUSH direct	2	24	2	C0
POP direct	2	24	2	D0
XCH A, Rn	1	12	1	C8-CF
XCH A, direct	2	12	2	C5
XCH A, @Ri	1	12	2	C6-C7
XCHD A, @Ri	1	12	2	D6-D7

Table XV. Overview of MCS-51 bit instructions.

Bit Instruction	Bytes	Clock Cycles		Hex Code
		8051	LP2052	
CLR C	1	12	1	C3
CLR bit	2	12	2	C2
SETB C	1	12	1	D3
SETB bit	2	12	2	D2
CPL C	1	12	1	B3
CPL bit	2	12	2	B2
ANL C, bit	2	24	2	82
ANL C, /bit	2	24	2	B0
ORL C, bit	2	24	2	72
ORL C, /bit	2	24	2	A0
MOV C, bit	2	12	2	A2
MOV bit, C	2	24	2	92
JC rel	2	24	3	40
JNC rel	2	24	3	50
JB bit, rel	3	24	4	20
JNB bit, rel	3	24	4	30
JBC bit, rel	3	24	4	10
JZ rel	2	24	3	60
JNZ rel	2	24	3	70
SJMP rel	2	24	3	80
ACALL addr11	2	24	3	11,31,51,71,91,B1,D1,F1
LCALL addr16	3	24	4	12
RET	1	24	4	22
RETI	1	24	4	32
AJMP addr11	2	24	3	01,21,41,61,81,A1,C1,E1
LJMP addr16	3	24	4	02
JMP @A+DPTR	1	24	2	73
CJNE A, direct, rel	3	24	4	B5
CJNE A, #data, rel	3	24	4	B4
CJNE Rn, #data, rel	3	24	4	B8-BF
CJNE @Ri, #data, rel	3	24	4	B6-B7
DJNZ Rn, rel	2	24	3	D8-DF
DJNZ direct, rel	3	24	4	D5
NOP	1	12	1	00

Appendix B. Complete table of experimental shot data.

Note: The data table of the experimental shot data includes two additional target locations defined for a separate experiment not within the scope of this thesis. Target location 1 and target location 3 in the data table the two target locations from a separate experiment. For the nine target locations defined in Chapter 3, the corresponding target locations in the data table are as follows:

Target Locations Defined in Chapter 3	Corresponding Target Location in Data
Target Location 1 →	Target Location 2 in data table
Target Location 2 →	Target Location 4 in data table
Target Location 3 →	Target Location 5 in data table
Target Location 4 →	Target Location 6 in data table
Target Location 5 →	Target Location 7 in data table
Target Location 6 →	Target Location 8 in data table
Target Location 7 →	Target Location 9 in data table
Target Location 8 →	Target Location 10 in data table
Target Location 9 →	Target Location 11 in data table

Appendix B. Continued…

ShotNumber	TargetLocation	TestDevice	RFFrequency-MHz	RFStartTime-us	RFStopTime-us	RFTotalDuration-us	RFAvgPk-Volts	RFMaxPk-Volts	Upset
1	1	LP2052-1	50	8.84	10.78	1.94	0.4671	0.6228	0
2	1	LP2052-1	50	8.84	10.78	1.94	0.4943	0.5656	0
3	1	LP2052-1	50	8.84	10.78	1.94	0.4713	0.5702	0
4	1	LP2052-1	50	8.84	10.78	1.94	0.4987	0.6029	0
5	1	LP2052-1	50	8.84	10.78	1.94	0.5168	0.6255	0
6	1	LP2052-1	50	8.84	10.78	1.94	0.5107	0.6181	0
7	1	LP2052-1	50	8.84	10.78	1.94	0.5107	0.6181	0
8	1	LP2052-1	50	8.84	10.78	1.94	0.445	0.5384	0
9	1	LP2052-1	50	8.84	10.78	1.94	0.5041	0.6102	0
10	1	LP2052-1	50	8.84	10.78	1.94	0.5205	0.63	0
11	1	LP2052-1	50	8.84	10.78	1.94	0.6475	0.8452	0
12	1	LP2052-1	50	8.84	10.78	1.94	0.6196	0.7496	0
13	1	LP2052-1	50	8.84	10.78	1.94	0.6665	0.8067	0
14	1	LP2052-1	50	8.84	10.78	1.94	0.6072	0.7349	0
15	1	LP2052-1	50	8.84	10.78	1.94	0.6761	0.8183	0
16	1	LP2052-1	50	8.84	10.78	1.94	0.7787	0.9422	0
17	1	LP2052-1	50	8.84	10.78	1.94	0.6198	0.7498	0
18	1	LP2052-1	50	8.84	10.78	1.94	0.6119	0.7405	0
19	1	LP2052-1	50	8.84	10.78	1.94	0.6474	0.7833	0
20	1	LP2052-1	50	8.84	10.78	1.94	0.7371	0.892	0
21	1	LP2052-1	50	8.84	10.78	1.94	0.7551	1.007	0
22	1	LP2052-1	50	8.84	10.78	1.94	0.7943	0.9608	0
23	1	LP2052-1	50	8.84	10.78	1.94	0.8447	1.021	1
24	1	LP2052-1	50	8.84	10.78	1.94	1.009	1.219	0
25	1	LP2052-1	50	8.84	10.78	1.94	0.85	1.028	1
26	1	LP2052-1	50	8.84	10.78	1.94	0.9014	1.091	0
27	1	LP2052-1	50	8.84	10.78	1.94	0.8444	1.021	0
28	1	LP2052-1	50	8.84	10.78	1.94	0.8141	0.9854	0
29	1	LP2052-1	50	8.84	10.78	1.94	0.8464	1.023	0
30	1	LP2052-1	50	8.84	10.78	1.94	0.9386	1.136	1
31	1	LP2052-1	50	8.84	10.78	1.94	0.9654	1.276	1
32	1	LP2052-1	50	8.84	10.78	1.94	1.151	1.392	0
33	1	LP2052-1	50	8.84	10.78	1.94	1.287	1.557	1
34	1	LP2052-1	50	8.84	10.78	1.94	1.23	1.489	1
35	1	LP2052-1	50	8.84	10.78	1.94	1.151	1.394	0
36	1	LP2052-1	50	8.84	10.78	1.94	1.174	1.419	1
37	1	LP2052-1	50	8.84	10.78	1.94	1.172	1.418	0
38	1	LP2052-1	50	8.84	10.78	1.94	1.151	1.393	0
39	1	LP2052-1	50	8.84	10.78	1.94	1.171	1.416	0
40	1	LP2052-1	50	8.84	10.78	1.94	1.142	1.382	1
41	1	LP2052-1	50	8.84	10.78	1.94	1.424	1.898	1
42	1	LP2052-1	50	8.84	10.78	1.94	1.618	1.957	1
43	1	LP2052-1	50	8.84	10.78	1.94	1.503	1.817	0
44	1	LP2052-1	50	8.84	10.78	1.94	1.553	1.878	1
45	1	LP2052-1	50	8.84	10.78	1.94	2.039	2.468	1
46	1	LP2052-1	50	8.84	10.78	1.94	1.553	1.88	1
47	1	LP2052-1	50	8.84	10.78	1.94	1.488	1.801	0
48	1	LP2052-1	50	8.84	10.78	1.94	1.535	1.857	1
49	1	LP2052-1	50	8.84	10.78	1.94	1.517	1.837	0
50	1	LP2052-1	50	8.84	10.78	1.94	1.547	1.873	1
ShotNumber	TargetLocation	TestDevice	RFFrequency-MHz	RFStartTime-us	RFStopTime-us	RFTotalDuration-us	RFAvgPk-Volts	RFMaxPk-Volts	Upset
51	1	LP2052-1	50	8.84	10.78	1.94	1.962	2.615	1
52	1	LP2052-1	50	8.84	10.78	1.94	2.13	2.578	1
53	1	LP2052-1	50	8.84	10.78	1.94	2.135	2.584	1
54	1	LP2052-1	50	8.84	10.78	1.94	2.155	2.608	1
55	1	LP2052-1	50	8.84	10.78	1.94	2.111	2.555	1
56	1	LP2052-1	50	8.84	10.78	1.94	2.13	2.576	1
57	1	LP2052-1	50	8.84	10.78	1.94	2.149	2.6	1
58	1	LP2052-1	50	8.84	10.78	1.94	2.204	2.667	1
59	1	LP2052-1	50	8.84	10.78	1.94	2.142	2.592	1
60	1	LP2052-1	50	8.84	10.78	1.94	2.165	2.619	1
61	1	LP2052-2	50	8.84	10.78	1.94	0.4176	0.5568	0
62	1	LP2052-2	50	8.84	10.78	1.94	0.4848	0.5865	0
63	1	LP2052-2	50	8.84	10.78	1.94	0.5151	0.6227	0
64	1	LP2052-2	50	8.84	10.78	1.94	0.5256	0.636	0
65	1	LP2052-2	50	8.84	10.78	1.94	0.5175	0.6257	0
66	1	LP2052-2	50	8.84	10.78	1.94	0.4496	0.5442	0
67	1	LP2052-2	50	8.84	10.78	1.94	0.4613	0.5577	0
68	1	LP2052-2	50	8.84	10.78	1.94	0.4777	0.5776	0
69	1	LP2052-2	50	8.84	10.78	1.94	0.5055	0.6116	0
70	1	LP2052-2	50	8.84	10.78	1.94	0.4954	0.5994	0
71	1	LP2052-2	50	8.84	10.78	1.94	0.6288	0.761	0
72	1	LP2052-2	50	8.84	10.78	1.94	0.6048	0.7318	0
73	1	LP2052-2	50	8.84	10.78	1.94	0.6832	0.8267	0
74	1	LP2052-2	50	8.84	10.78	1.94	0.6494	0.7859	0
75	1	LP2052-2	50	8.84	10.78	1.94	0.6006	0.7269	0
76	1	LP2052-2	50	8.84	10.78	1.94	0.6064	0.7339	0
77	1	LP2052-2	50	8.84	10.78	1.94	0.6622	0.8013	0
78	1	LP2052-2	50	8.84	10.78	1.94	0.6429	0.7779	0
79	1	LP2052-2	50	8.84	10.78	1.94	0.6736	0.8147	0
80	1	LP2052-2	50	8.84	10.78	1.94	0.6577	0.7961	0
81	1	LP2052-2	50	8.84	10.78	1.94	0.7254	0.9577	0
82	1	LP2052-2	50	8.84	10.78	1.94	0.8462	1.024	0
83	1	LP2052-2	50	8.84	10.78	1.94	0.8256	0.9988	0
84	1	LP2052-2	50	8.84	10.78	1.94	0.8323	1.007	0
85	1	LP2052-2	50	8.84	10.78	1.94	0.8335	1.008	0
86	1	LP2052-2	50	8.84	10.78	1.94	0.8279	1.002	0
87	1	LP2052-2	50	8.84	10.78	1.94	0.8909	1.078	0
88	1	LP2052-2	50	8.84	10.78	1.94	0.837	1.012	0
89	1	LP2052-2	50	8.84	10.78	1.94	0.8196	0.9914	0
90	1	LP2052-2	50	8.84	10.78	1.94	0.817	0.9887	0
91	1	LP2052-2	50	8.84	10.78	1.94	1.199	1.451	1
92	1	LP2052-2	50	8.84	10.78	1.94	1.04	1.328	1
93	1	LP2052-2	50	8.84	10.78	1.94	1.157	1.401	1
94	1	LP2052-2	50	8.84	10.78	1.94	1.165	1.408	1
95	1	LP2052-2	50	8.84	10.78	1.94	1.149	1.39	0
96	1	LP2052-2	50	8.84	10.78	1.94	1.162	1.405	1
97	1	LP2052-2	50	8.84	10.78	1.94	1.155	1.398	0
98	1	LP2052-2	50	8.84	10.78	1.94	1.195	1.447	1
99	1	LP2052-2	50	8.84	10.78	1.94	1.146	1.387	0
100	1	LP2052-2	50	8.84	10.78	1.94	1.172	1.418	1

Appendix B. Continued…

ShotNumber	TargetLocation	TestDevice	RFFrequency-MHz	RFStartTime-us	RFStopTime-us	RFTotalDuration-us	RFAvgPk-Volts	RFMaxPk-Volts	Upset
101	1	LP2052-2	50	8.84	10.78	1.94	1.353	1.696	0
102	1	LP2052-2	50	8.84	10.78	1.94	1.551	1.876	1
103	1	LP2052-2	50	8.84	10.78	1.94	1.539	1.861	0
104	1	LP2052-2	50	8.84	10.78	1.94	1.546	1.87	1
105	1	LP2052-2	50	8.84	10.78	1.94	1.598	1.934	1
106	1	LP2052-2	50	8.84	10.78	1.94	1.589	1.923	1
107	1	LP2052-2	50	8.84	10.78	1.94	1.544	1.868	1
108	1	LP2052-2	50	8.84	10.78	1.94	1.632	1.975	1
109	1	LP2052-2	50	8.84	10.78	1.94	1.623	1.964	1
110	1	LP2052-2	50	8.84	10.78	1.94	1.516	1.834	1
111	1	LP2052-2	50	8.84	10.78	1.94	1.933	2.456	1
112	1	LP2052-2	50	8.84	10.78	1.94	2.126	2.573	1
113	1	LP2052-2	50	8.84	10.78	1.94	2.196	2.658	1
114	1	LP2052-2	50	8.84	10.78	1.94	2.24	2.709	1
115	1	LP2052-2	50	8.84	10.78	1.94	2.188	2.645	1
116	1	LP2052-2	50	8.84	10.78	1.94	2.168	2.623	1
117	1	LP2052-2	50	8.84	10.78	1.94	2.147	2.597	1
118	1	LP2052-2	50	8.84	10.78	1.94	2.148	2.599	1
119	1	LP2052-2	50	8.84	10.78	1.94	2.194	2.655	1
120	1	LP2052-2	50	8.84	10.78	1.94	2.131	2.577	1
121	2	LP2052-1	50	8.84	9.835	0.995	0.5652	0.75636	0
122	2	LP2052-1	50	8.84	9.835	0.995	0.5927	0.7168	0
123	2	LP2052-1	50	8.84	9.835	0.995	0.5878	0.7107	0
124	2	LP2052-1	50	8.84	9.835	0.995	0.6402	0.7748	0
125	2	LP2052-1	50	8.84	9.835	0.995	0.6314	0.7641	0
126	2	LP2052-1	50	8.84	9.835	0.995	0.6403	0.7748	0
127	2	LP2052-1	50	8.84	9.835	0.995	0.6246	0.7558	0
128	2	LP2052-1	50	8.84	9.835	0.995	0.5915	0.7155	0
129	2	LP2052-1	50	8.84	9.835	0.995	0.7009	0.9303	0
130	2	LP2052-1	50	8.84	9.835	0.995	0.877	1.062	0
131	2	LP2052-1	50	8.84	9.835	0.995	0.8805	1.066	0
132	2	LP2052-1	50	8.84	9.835	0.995	0.893	1.081	0
133	2	LP2052-1	50	8.84	9.835	0.995	0.8136	0.984	0
134	2	LP2052-1	50	8.84	9.835	0.995	0.8021	0.9707	0
135	2	LP2052-1	50	8.83	9.825	0.995	0.845	1.022	0
136	2	LP2052-1	50	8.83	9.825	0.995	0.8248	0.9981	0
137	2	LP2052-1	50	8.83	9.825	0.995	0.994	1.235	0
138	2	LP2052-1	50	8.83	9.825	0.995	1.115	1.35	0
139	2	LP2052-1	50	8.83	9.825	0.995	1.175	1.421	0
140	2	LP2052-1	50	8.83	9.825	0.995	1.151	1.392	0
141	2	LP2052-1	50	8.83	9.825	0.995	1.11	1.344	0
142	2	LP2052-1	50	8.83	9.825	0.995	1.128	2.364	0
143	2	LP2052-1	50	8.83	9.825	0.995	1.101	1.333	0
144	2	LP2052-1	50	8.83	9.825	0.995	1.175	1.423	1
145	2	LP2052-1	50	8.83	9.825	0.995	1.305	1.737	0
146	2	LP2052-1	50	8.83	9.825	0.995	1.623	1.065	1
147	2	LP2052-1	50	8.83	9.825	0.995	1.57	1.901	0
148	2	LP2052-1	50	8.83	9.825	0.995	1.481	1.792	1
149	2	LP2052-1	50	8.83	9.825	0.995	1.499	1.815	1
150	2	LP2052-1	50	8.83	9.825	0.995	1.558	1.886	1
ShotNumber	TargetLocation	TestDevice	RFFrequency-MHz	RFStartTime-us	RFStopTime-us	RFTotalDuration-us	RFAvgPk-Volts	RFMaxPk-Volts	Upset
151	2	LP2052-1	50	8.83	9.825	0.995	1.6	1.937	1
152	2	LP2052-1	50	8.83	9.825	0.995	1.508	1.823	1
153	2	LP2052-1	50	8.83	9.825	0.995	2.032	2.709	1
154	2	LP2052-1	50	8.83	9.825	0.995	2.112	2.557	1
155	2	LP2052-1	50	8.83	9.825	0.995	2.093	2.533	1
156	2	LP2052-1	50	8.83	9.825	0.995	2.096	2.537	1
157	2	LP2052-1	50	8.83	9.825	0.995	2.158	2.612	1
158	2	LP2052-1	50	8.83	9.825	0.995	2.146	2.598	1
159	2	LP2052-1	50	8.83	9.825	0.995	2.081	2.518	0
160	2	LP2052-1	50	8.83	9.825	0.995	2.078	2.515	0
161	2	LP2052-1	50	8.83	9.825	0.995	2.478	3.303	1
162	2	LP2052-1	50	8.83	9.825	0.995	2.807	3.395	1
163	2	LP2052-1	50	8.83	9.825	0.995	2.835	3.428	1
164	2	LP2052-1	50	8.83	9.825	0.995	2.852	3.452	1
165	2	LP2052-1	50	8.83	9.825	0.995	2.996	3.623	1
166	2	LP2052-1	50	8.83	9.825	0.995	3.02	3.652	1
167	2	LP2052-1	50	8.83	9.825	0.995	2.926	3.541	1
168	2	LP2052-1	50	8.83	9.825	0.995	2.829	3.423	1
169	2	LP2052-2	50	8.83	9.825	0.995	0.8819	1.151	0
170	2	LP2052-2	50	8.83	9.825	0.995	0.8389	1.015	0
171	2	LP2052-2	50	8.83	9.825	0.995	0.8323	1.006	0
172	2	LP2052-2	50	8.83	9.825	0.995	0.8609	1.042	0
173	2	LP2052-2	50	8.83	9.825	0.995	0.8339	1.009	0
174	2	LP2052-2	50	8.83	9.825	0.995	0.832	1.006	0
175	2	LP2052-2	50	8.83	9.825	0.995	0.8283	1.002	0
176	2	LP2052-2	50	8.83	9.825	0.995	0.9503	1.15	0
177	2	LP2052-2	50	8.83	9.825	0.995	1.089	1.385	0
178	2	LP2052-2	50	8.83	9.825	0.995	1.172	1.418	0
179	2	LP2052-2	50	8.83	9.825	0.995	1.27	1.535	0
180	2	LP2052-2	50	8.83	9.825	0.995	1.219	1.475	0
181	2	LP2052-2	50	8.83	9.825	0.995	1.213	1.468	0
182	2	LP2052-2	50	8.83	9.825	0.995	1.205	1.458	0
183	2	LP2052-2	50	8.83	9.825	0.995	1.215	1.47	0
184	2	LP2052-2	50	8.83	9.825	0.995	1.235	1.494	0
185	2	LP2052-2	50	8.83	9.825	0.995	1.493	1.961	0
186	2	LP2052-2	50	8.83	9.825	0.995	1.653	2.001	0
187	2	LP2052-2	50	8.83	9.825	0.995	1.7	2.057	0
188	2	LP2052-2	50	8.83	9.825	0.995	1.683	2.037	1
189	2	LP2052-2	50	8.83	9.825	0.995	1.704	2.062	1
190	2	LP2052-2	50	8.83	9.825	0.995	1.686	2.04	0
191	2	LP2052-2	50	8.83	9.825	0.995	1.674	2.026	1
192	2	LP2052-2	50	8.83	9.825	0.995	1.662	2.011	0
193	2	LP2052-2	50	8.83	9.825	0.995	2.111	2.554	0
194	2	LP2052-2	50	8.83	9.825	0.995	2.414	2.921	1
195	2	LP2052-2	50	8.83	9.825	0.995	2.384	2.883	1
196	2	LP2052-2	50	8.83	9.825	0.995	2.379	2.879	1
197	2	LP2052-2	50	8.83	9.825	0.995	2.383	2.882	1
198	2	LP2052-2	50	8.83	9.825	0.995	2.419	2.927	1
199	2	LP2052-2	50	8.83	9.825	0.995	2.374	2.873	0
200	2	LP2052-2	50	8.83	9.825	0.995	2.374	2.87	1

Appendix B. Continued…

ShotNumber	TargetLocation	TestDevice	RFFrequency-MHz	RFStartTime-us	RFStopTime-us	RFTotalDuration-us	RFAvgPk-Volts	RFMaxPk-Volts	Upset
201	2	LP2052-2	50	8.83	9.825	0.995	2.724	3.158	1
202	2	LP2052-2	50	8.83	9.825	0.995	2.87	3.469	1
203	2	LP2052-2	50	8.83	9.825	0.995	3.234	3.912	1
204	2	LP2052-2	50	8.83	9.825	0.995	3.176	3.845	1
205	2	LP2052-2	50	8.83	9.825	0.995	3.203	3.876	1
206	2	LP2052-2	50	8.83	9.825	0.995	3.212	3.888	1
207	2	LP2052-2	50	8.83	9.825	0.995	3.257	3.941	1
208	2	LP2052-2	50	8.83	9.825	0.995	3.286	3.974	1
209	3	LP2052-1	50	9.825	10.82	0.995	1.129	1.505	0
210	3	LP2052-1	50	9.825	10.82	0.995	1.213	1.468	0
211	3	LP2052-1	50	9.825	10.82	0.995	1.243	1.504	0
212	3	LP2052-1	50	9.825	10.82	0.995	1.187	1.436	0
213	3	LP2052-1	50	9.825	10.82	0.995	1.225	1.483	0
214	3	LP2052-1	50	9.825	10.82	0.995	1.263	1.527	0
215	3	LP2052-1	50	9.825	10.82	0.995	1.218	1.474	0
216	3	LP2052-1	50	9.825	10.82	0.995	1.2	1.452	0
217	3	LP2052-1	50	9.825	10.82	0.995	1.522	2.029	1
218	3	LP2052-1	50	9.825	10.82	0.995	1.753	2.122	0
219	3	LP2052-1	50	9.825	10.82	0.995	1.713	2.072	1
220	3	LP2052-1	50	9.825	10.82	0.995	1.699	2.056	1
221	3	LP2052-1	50	9.825	10.82	0.995	2.703	2.062	1
222	3	LP2052-1	50	9.825	10.82	0.995	1.689	2.043	1
223	3	LP2052-1	50	9.825	10.82	0.995	1.703	2.059	1
224	3	LP2052-1	50	9.825	10.82	0.995	1.696	2.053	1
225	3	LP2052-1	50	9.825	10.82	0.995	2.137	2.842	1
226	3	LP2052-1	50	9.825	10.82	0.995	2.088	2.525	1
227	3	LP2052-1	50	9.825	10.82	0.995	2.062	2.495	1
228	3	LP2052-1	50	9.825	10.82	0.995	2.07	2.505	1
229	3	LP2052-1	50	9.825	10.82	0.995	2.115	2.557	1
230	3	LP2052-1	50	9.825	10.82	0.995	2.114	2.556	1
231	3	LP2052-1	50	9.825	10.82	0.995	2.162	2.616	1
232	3	LP2052-1	50	9.825	10.82	0.995	2.108	2.551	1
233	3	LP2052-2	50	9.825	10.82	0.995	1.109	1.478	0
234	3	LP2052-2	50	9.825	10.82	0.995	1.249	1.511	0
235	3	LP2052-2	50	9.825	10.82	0.995	1.247	1.509	0
236	3	LP2052-2	50	9.825	10.82	0.995	1.234	1.493	0
237	3	LP2052-2	50	9.825	10.82	0.995	1.24	1.5	0
238	3	LP2052-2	50	9.825	10.82	0.995	1.211	1.465	0
239	3	LP2052-2	50	9.825	10.82	0.995	1.223	1.48	0
240	3	LP2052-2	50	9.825	10.82	0.995	1.247	1.509	0
241	3	LP2052-2	50	9.825	10.82	0.995	1.566	2.085	1
242	3	LP2052-2	50	9.825	10.82	0.995	1.731	2.093	1
243	3	LP2052-2	50	9.825	10.82	0.995	1.729	2.092	1
244	3	LP2052-2	50	9.825	10.82	0.995	1.714	2.075	1
245	3	LP2052-2	50	9.825	10.82	0.995	1.709	2.066	0
246	3	LP2052-2	50	9.825	10.82	0.995	1.74	2.106	0
247	3	LP2052-2	50	9.825	10.82	0.995	1.742	2.109	1
248	3	LP2052-2	50	9.825	10.82	0.995	1.77	2.139	0
249	3	LP2052-2	50	9.825	10.82	0.995	2.464	2.982	1
250	3	LP2052-2	50	9.825	10.82	0.995	2.081	2.428	1
ShotNumber	TargetLocation	TestDevice	RFFrequency-MHz	RFStartTime-us	RFStopTime-us	RFTotalDuration-us	RFAvgPk-Volts	RFMaxPk-Volts	Upset
251	3	LP2052-2	50	9.825	10.82	0.995	2.426	2.935	1
252	3	LP2052-2	50	9.825	10.82	0.995	2.466	2.982	1
253	3	LP2052-2	50	9.825	10.82	0.995	2.434	2.943	1
254	3	LP2052-2	50	9.825	10.82	0.995	2.463	2.978	1
255	3	LP2052-2	50	9.825	10.82	0.995	2.448	2.962	1
256	3	LP2052-2	50	9.825	10.82	0.995	2.468	2.987	1
257	5	LP2052-1	50	8.86	9.34	0.48	1.471	1.949	0
258	5	LP2052-1	50	8.86	9.34	0.48	1.677	2.029	0
259	5	LP2052-1	50	8.86	9.34	0.48	1.664	2.014	0
260	5	LP2052-1	50	8.86	9.34	0.48	1.708	2.067	0
261	5	LP2052-1	50	8.86	9.34	0.48	1.709	2.067	0
262	5	LP2052-1	50	8.86	9.34	0.48	1.7	2.057	0
263	5	LP2052-1	50	8.86	9.34	0.48	1.669	2.021	0
264	5	LP2052-1	50	8.86	9.34	0.48	1.651	1.995	0
265	5	LP2052-1	50	8.86	9.34	0.48	2.115	2.809	0
266	5	LP2052-1	50	8.86	9.34	0.48	2.423	2.931	0
267	5	LP2052-1	50	8.86	9.34	0.48	2.35	2.844	1
268	5	LP2052-1	50	8.86	9.34	0.48	2.346	2.839	0
269	5	LP2052-1	50	8.86	9.34	0.48	2.38	2.878	1
270	5	LP2052-1	50	8.86	9.34	0.48	2.44	2.952	0
271	5	LP2052-1	50	8.86	9.34	0.48	2.388	2.89	0
272	5	LP2052-1	50	8.86	9.34	0.48	2.332	2.822	1
273	5	LP2052-1	50	8.86	9.34	0.48	2.685	3.104	0
274	5	LP2052-1	50	8.86	9.34	0.48	3.116	3.771	1
275	5	LP2052-1	50	8.86	9.34	0.48	3.211	3.887	0
276	5	LP2052-1	50	8.86	9.34	0.48	3.161	3.824	0
277	5	LP2052-1	50	8.86	9.34	0.48	3.095	3.746	0
278	5	LP2052-1	50	8.86	9.34	0.48	3.104	3.757	1
279	5	LP2052-1	50	8.86	9.34	0.48	3.234	3.911	1
280	5	LP2052-1	50	8.86	9.34	0.48	3.103	3.755	0
281	5	LP2052-1	50	8.86	9.34	0.48	3.653	4.712	0
282	5	LP2052-1	50	8.86	9.34	0.48	4.149	5.022	0
283	5	LP2052-1	50	8.86	9.34	0.48	4.214	5.1	1
284	5	LP2052-1	50	8.86	9.34	0.48	4.109	4.972	1
285	5	LP2052-1	50	8.86	9.34	0.48	4.165	5.036	0
286	5	LP2052-1	50	8.86	9.34	0.48	4.22	5.105	1
287	5	LP2052-1	50	8.86	9.34	0.48	4.14	5.009	1
288	5	LP2052-1	50	8.86	9.34	0.48	4.221	5.104	1
289	5	LP2052-1	50	8.86	9.34	0.48	4.922	6.564	1
290	5	LP2052-1	50	8.86	9.34	0.48	4.711	5.701	1
291	5	LP2052-1	50	8.86	9.34	0.48	4.885	5.908	1
292	5	LP2052-1	50	8.86	9.34	0.48	5.157	6.239	1
293	5	LP2052-1	50	8.86	9.34	0.48	5.157	6.239	1
294	5	LP2052-1	50	8.86	9.34	0.48	5.507	6.666	1
295	5	LP2052-1	50	8.86	9.34	0.48	5.577	6.751	1
296	5	LP2052-1	50	8.86	9.34	0.48	5.428	6.569	1
297	5	LP2052-2	50	8.86	9.34	0.48	1.286	1.715	0
298	5	LP2052-2	50	8.86	9.34	0.48	1.867	2.258	0
299	5	LP2052-2	50	8.86	9.34	0.48	1.964	2.375	0
300	5	LP2052-2	50	8.86	9.34	0.48	2.3	2.782	0

Appendix B. Continued…

ShotNumber	TargetLocation	TestDevice	RFFrequency-MHz	RFStartTime-us	RFStopTime-us	RFTotalDuration-us	RFAvgPk-Volts	RFMaxPk-Volts	Upset
301	5	LP2052-2	50	8.86	9.34	0.48	1.43	1.731	0
302	5	LP2052-2	50	8.86	9.34	0.48	1.385	1.676	0
303	5	LP2052-2	50	8.86	9.34	0.48	1.372	1.66	0
304	5	LP2052-2	50	8.86	9.34	0.48	1.421	1.72	0
305	5	LP2052-2	50	8.86	9.34	0.48	1.698	2.265	0
306	5	LP2052-2	50	8.86	9.34	0.48	1.891	2.288	0
307	5	LP2052-2	50	8.86	9.34	0.48	1.874	2.264	0
308	5	LP2052-2	50	8.86	9.34	0.48	1.841	2.229	0
309	5	LP2052-2	50	8.86	9.34	0.48	1.931	2.337	0
310	5	LP2052-2	50	8.86	9.34	0.48	1.862	2.254	0
311	5	LP2052-2	50	8.86	9.34	0.48	1.921	2.322	0
312	5	LP2052-2	50	8.86	9.34	0.48	1.883	2.277	0
313	5	LP2052-2	50	8.86	9.34	0.48	2.218	2.645	0
314	5	LP2052-2	50	8.86	9.34	0.48	2.654	3.209	0
315	5	LP2052-2	50	8.86	9.34	0.48	2.615	3.165	0
316	5	LP2052-2	50	8.86	9.34	0.48	2.63	3.182	0
317	5	LP2052-2	50	8.86	9.34	0.48	2.5	3.026	0
318	5	LP2052-2	50	8.86	9.34	0.48	2.539	3.073	0
319	5	LP2052-2	50	8.86	9.34	0.48	2.585	3.129	0
320	5	LP2052-2	50	8.86	9.34	0.48	2.434	2.946	0
321	5	LP2052-2	50	8.86	9.34	0.48	2.968	3.688	0
322	5	LP2052-2	50	8.86	9.34	0.48	3.55	4.296	1
323	5	LP2052-2	50	8.86	9.34	0.48	3.455	4.181	0
324	5	LP2052-2	50	8.86	9.34	0.48	3.514	4.252	1
325	5	LP2052-2	50	8.86	9.34	0.48	3.441	2.165	0
326	5	LP2052-2	50	8.86	9.34	0.48	3.578	4.329	0
327	5	LP2052-2	50	8.86	9.34	0.48	3.422	4.154	0
328	5	LP2052-2	50	8.86	9.34	0.48	3.552	4.299	0
329	5	LP2052-2	50	8.86	9.34	0.48	3.493	4.597	0
330	5	LP2052-2	50	8.86	9.34	0.48	4.406	5.332	1
331	5	LP2052-2	50	8.86	9.34	0.48	4.456	5.393	1
332	5	LP2052-2	50	8.86	9.34	0.48	4.629	5.595	1
333	5	LP2052-2	50	8.86	9.34	0.48	4.14	5.007	1
334	5	LP2052-2	50	8.86	9.34	0.48	4.235	5.124	1
335	5	LP2052-2	50	8.86	9.34	0.48	4.421	5.352	1
336	5	LP2052-2	50	8.86	9.34	0.48	4.691	5.677	1
337	6	LP2052-1	50	8.86	9.1	0.24	2.894	3.858	0
338	6	LP2052-1	50	8.86	9.1	0.24	3.217	3.894	0
339	6	LP2052-1	50	8.86	9.1	0.24	3.124	3.778	0
340	6	LP2052-1	50	8.86	9.1	0.24	3.142	3.802	0
341	6	LP2052-1	50	8.86	9.1	0.24	3.191	3.862	0
342	6	LP2052-1	50	8.86	9.1	0.24	3.21	3.882	0
343	6	LP2052-1	50	8.86	9.1	0.24	3.193	3.864	0
344	6	LP2052-1	50	8.86	9.1	0.24	3.244	3.926	0
345	6	LP2052-1	50	8.86	9.1	0.24	3.134	3.79	1
346	6	LP2052-1	50	8.86	9.1	0.24	4.257	5.153	1
347	6	LP2052-1	50	8.86	9.1	0.24	4.282	5.182	1
348	6	LP2052-1	50	8.86	9.1	0.24	4.281	5.181	0
349	6	LP2052-1	50	8.86	9.1	0.24	4.281	5.181	1
350	6	LP2052-1	50	8.86	9.1	0.24	4.529	5.482	1
ShotNumber	TargetLocation	TestDevice	RFFrequency-MHz	RFStartTime-us	RFStopTime-us	RFTotalDuration-us	RFAvgPk-Volts	RFMaxPk-Volts	Upset
351	6	LP2052-1	50	8.86	9.1	0.24	4.261	5.154	1
352	6	LP2052-1	50	8.86	9.1	0.24	4.31	5.216	1
353	6	LP2052-1	50	8.86	9.1	0.24	4.942	5.98	1
354	6	LP2052-1	50	8.86	9.1	0.24	5.548	6.715	1
355	6	LP2052-1	50	8.86	9.1	0.24	5.025	6.082	1
356	6	LP2052-1	50	8.86	9.1	0.24	5.667	6.858	1
357	6	LP2052-1	50	8.86	9.1	0.24	5.003	6.055	1
358	6	LP2052-1	50	8.86	9.1	0.24	5.533	6.696	1
359	6	LP2052-1	50	8.86	9.1	0.24	5.033	6.087	1
360	6	LP2052-1	50	8.86	9.1	0.24	5.559	6.727	1
361	6	LP2052-2	50	8.86	9.1	0.24	2.253	2.979	0
362	6	LP2052-2	50	8.86	9.1	0.24	2.632	3.183	0
363	6	LP2052-2	50	8.86	9.1	0.24	2.51	3.036	0
364	6	LP2052-2	50	8.86	9.1	0.24	2.488	3.011	0
365	6	LP2052-2	50	8.86	9.1	0.24	2.655	3.213	0
366	6	LP2052-2	50	8.86	9.1	0.24	2.504	3.029	0
367	6	LP2052-2	50	8.86	9.1	0.24	2.544	3.075	0
368	6	LP2052-2	50	8.86	9.1	0.24	2.649	3.204	0
369	6	LP2052-2	50	8.86	9.1	0.24	3.718	4.499	0
370	6	LP2052-2	50	8.86	9.1	0.24	3.726	4.505	0
371	6	LP2052-2	50	8.86	9.1	0.24	3.565	4.31	0
372	6	LP2052-2	50	8.86	9.1	0.24	3.578	4.329	0
373	6	LP2052-2	50	8.86	9.1	0.24	4.173	5.051	1
374	6	LP2052-2	50	8.86	9.1	0.24	4.161	5.036	1
375	6	LP2052-2	50	8.86	9.1	0.24	4.25	5.139	1
376	6	LP2052-2	50	8.86	9.1	0.24	4.229	5.117	0
377	6	LP2052-2	50	8.86	9.1	0.24	4.899	5.93	1
378	6	LP2052-2	50	8.86	9.1	0.24	5.465	6.61	1
379	6	LP2052-2	50	8.86	9.1	0.24	5.231	6.332	1
380	6	LP2052-2	50	8.86	9.1	0.24	5.649	6.836	1
381	6	LP2052-2	50	8.86	9.1	0.24	5.175	6.263	1
382	6	LP2052-2	50	8.86	9.1	0.24	5.666	6.855	1
383	6	LP2052-2	50	8.86	9.1	0.24	4.945	5.985	1
384	6	LP2052-2	50	8.86	9.1	0.24	5.628	6.811	1
385	7	LP2052-1	50	9.1	9.34	0.24	2.37	3.159	0
386	7	LP2052-1	50	9.1	9.34	0.24	2.595	3.14	0
387	7	LP2052-1	50	9.1	9.34	0.24	2.564	3.104	0
388	7	LP2052-1	50	9.1	9.34	0.24	2.634	3.187	0
389	7	LP2052-1	50	9.1	9.34	0.24	2.607	3.155	0
390	7	LP2052-1	50	9.1	9.34	0.24	2.563	3.102	0
391	7	LP2052-1	50	9.1	9.34	0.24	2.592	3.138	0
392	7	LP2052-1	50	9.1	9.34	0.24	2.613	3.158	0
393	7	LP2052-1	50	9.1	9.34	0.24	3.534	4.274	0
394	7	LP2052-1	50	9.1	9.34	0.24	3.605	4.359	0
395	7	LP2052-1	50	9.1	9.34	0.24	3.555	4.296	0
396	7	LP2052-1	50	9.1	9.34	0.24	3.541	4.285	0
397	7	LP2052-1	50	9.1	9.34	0.24	3.553	4.3	0
398	7	LP2052-1	50	9.1	9.34	0.24	3.546	4.289	0
399	7	LP2052-1	50	9.1	9.34	0.24	3.606	4.363	0
400	7	LP2052-1	50	9.1	9.34	0.24	3.545	4.29	0

Appendix B. Continued…

ShotNumber	TargetLocation	TestDevice	RFFrequency-MHz	RFStartTime-us	RFStopTime-us	RFTotalDuration-us	RFAvgPk-Volts	RFMaxPk-Volts	Upset
401	7	LP2052-1	50	9.1	9.34	0.24	4.191	5.073	0
402	7	LP2052-1	50	9.1	9.34	0.24	4.802	5.805	0
403	7	LP2052-1	50	9.1	9.34	0.24	4.31	5.21	0
404	7	LP2052-1	50	9.1	9.34	0.24	4.835	5.849	0
405	7	LP2052-1	50	9.1	9.34	0.24	4.042	4.887	0
406	7	LP2052-1	50	9.1	9.34	0.24	4.148	5.019	0
407	7	LP2052-1	50	9.1	9.34	0.24	4.072	4.926	0
408	7	LP2052-1	50	9.1	9.34	0.24	4.265	5.163	0
409	7	LP2052-1	50	9.1	9.34	0.24	4.723	5.714	0
410	7	LP2052-1	50	9.1	9.34	0.24	4.765	5.768	0
411	7	LP2052-1	50	9.1	9.34	0.24	4.735	5.729	0
412	7	LP2052-1	50	9.1	9.34	0.24	4.817	5.831	0
413	7	LP2052-1	50	9.1	9.34	0.24	4.772	5.771	0
414	7	LP2052-1	50	9.1	9.34	0.24	4.813	5.819	0
415	7	LP2052-1	50	9.1	9.34	0.24	4.789	5.79	0
416	7	LP2052-1	50	9.1	9.34	0.24	4.786	5.793	0
417	7	LP2052-2	50	9.1	9.34	0.24	4.151	5.473	0
418	7	LP2052-2	50	9.1	9.34	0.24	4.661	5.637	0
419	7	LP2052-2	50	9.1	9.34	0.24	4.7	5.688	0
420	7	LP2052-2	50	9.1	9.34	0.24	4.638	5.607	0
421	7	LP2052-2	50	9.1	9.34	0.24	4.691	5.677	0
422	7	LP2052-2	50	9.1	9.34	0.24	4.72	5.712	0
423	7	LP2052-2	50	9.1	9.34	0.24	4.381	5.303	0
424	7	LP2052-2	50	9.1	9.34	0.24	4.494	5.435	0
425	9	LP2052-1	50	9.42	9.79	0.37	1.986	2.648	0
426	9	LP2052-1	50	9.42	9.79	0.37	2.193	2.652	0
427	9	LP2052-1	50	9.42	9.79	0.37	2.205	2.669	0
428	9	LP2052-1	50	9.42	9.79	0.37	2.223	2.689	0
429	9	LP2052-1	50	9.42	9.79	0.37	2.273	2.752	1
430	9	LP2052-1	50	9.42	9.79	0.37	2.202	2.665	0
431	9	LP2052-1	50	9.42	9.79	0.37	2.242	2.713	0
432	9	LP2052-1	50	9.42	9.79	0.37	2.201	2.664	0
433	9	LP2052-1	50	9.42	9.79	0.37	2.966	3.589	0
434	9	LP2052-1	50	9.42	9.79	0.37	2.949	3.569	0
435	9	LP2052-1	50	9.42	9.79	0.37	2.944	3.559	0
436	9	LP2052-1	50	9.42	9.79	0.37	2.942	3.559	0
437	9	LP2052-1	50	9.42	9.79	0.37	2.956	3.575	0
438	9	LP2052-1	50	9.42	9.79	0.37	2.958	3.577	0
439	9	LP2052-1	50	9.42	9.79	0.37	2.997	3.626	0
440	9	LP2052-1	50	9.42	9.79	0.37	3.192	3.862	0
441	9	LP2052-1	50	9.42	9.79	0.37	3.915	4.736	1
442	9	LP2052-1	50	9.42	9.79	0.37	3.924	4.748	1
443	9	LP2052-1	50	9.42	9.79	0.37	3.925	4.75	1
444	9	LP2052-1	50	9.42	9.79	0.37	3.976	4.811	1
445	9	LP2052-1	50	9.42	9.79	0.37	3.953	4.778	1
446	9	LP2052-1	50	9.42	9.79	0.37	3.954	4.781	1
447	9	LP2052-1	50	9.42	9.79	0.37	3.923	4.747	1
448	9	LP2052-1	50	9.42	9.79	0.37	3.971	4.805	0
449	9	LP2052-1	50	9.42	9.79	0.37	4.77	5.772	1
450	9	LP2052-1	50	9.42	9.79	0.37	5.052	6.113	1
ShotNumber	TargetLocation	TestDevice	RFFrequency-MHz	RFStartTime-us	RFStopTime-us	RFTotalDuration-us	RFAvgPk-Volts	RFMaxPk-Volts	Upset
451	9	LP2052-1	50	9.42	9.79	0.37	5.092	6.161	1
452	9	LP2052-1	50	9.42	9.79	0.37	4.613	5.581	1
453	9	LP2052-1	50	9.42	9.79	0.37	4.714	5.702	1
454	9	LP2052-1	50	9.42	9.79	0.37	4.81	5.821	1
455	9	LP2052-1	50	9.42	9.79	0.37	4.9	5.931	1
456	9	LP2052-1	50	9.42	9.79	0.37	5	6.051	1
457	9	LP2052-2	50	9.42	9.79	0.37	2.801	3.735	0
458	9	LP2052-2	50	9.42	9.79	0.37	3.091	3.738	0
459	9	LP2052-2	50	9.42	9.79	0.37	3.066	3.709	0
460	9	LP2052-2	50	9.42	9.79	0.37	3.233	3.912	0
461	9	LP2052-2	50	9.42	9.79	0.37	3.091	3.74	0
462	9	LP2052-2	50	9.42	9.79	0.37	3.032	3.668	0
463	9	LP2052-2	50	9.42	9.79	0.37	3.091	3.737	0
464	9	LP2052-2	50	9.42	9.79	0.37	3.049	3.691	0
465	9	LP2052-2	50	9.42	9.79	0.37	4.065	4.916	1
466	9	LP2052-2	50	9.42	9.79	0.37	4.039	4.886	1
467	9	LP2052-2	50	9.42	9.79	0.37	4.046	4.892	1
468	9	LP2052-2	50	9.42	9.79	0.37	4.065	4.913	1
469	9	LP2052-2	50	9.42	9.79	0.37	4.032	4.875	1
470	9	LP2052-2	50	9.42	9.79	0.37	4.035	4.883	1
471	9	LP2052-2	50	9.42	9.79	0.37	4.041	4.89	1
472	9	LP2052-2	50	9.42	9.79	0.37	4.023	4.869	1
473	10	LP2052-1	50	9.42	9.605	0.185	1.851	2.147	0
474	10	LP2052-1	50	9.42	9.605	0.185	2.139	2.588	0
475	10	LP2052-1	50	9.42	9.605	0.185	2.116	2.558	0
476	10	LP2052-1	50	9.42	9.605	0.185	2.142	2.592	0
477	10	LP2052-1	50	9.42	9.605	0.185	2.299	2.783	0
478	10	LP2052-1	50	9.42	9.605	0.185	2.135	2.583	0
479	10	LP2052-1	50	9.42	9.605	0.185	2.13	2.576	0
480	10	LP2052-1	50	9.42	9.605	0.185	2.161	2.616	1
481	10	LP2052-1	50	9.42	9.605	0.185	2.926	3.538	1
482	10	LP2052-1	50	9.42	9.605	0.185	2.903	3.514	1
483	10	LP2052-1	50	9.42	9.605	0.185	2.97	3.593	1
484	10	LP2052-1	50	9.42	9.605	0.185	2.959	3.582	1
485	10	LP2052-1	50	9.42	9.605	0.185	2.908	3.519	1
486	10	LP2052-1	50	9.42	9.605	0.185	2.935	3.55	1
487	10	LP2052-1	50	9.42	9.605	0.185	2.926	3.54	1
488	10	LP2052-1	50	9.42	9.605	0.185	2.892	3.5	1
489	10	LP2052-1	50	9.42	9.605	0.185	2.919	3.531	1
490	10	LP2052-2	50	9.42	9.605	0.185	1.8	2.088	1
491	10	LP2052-2	50	9.42	9.605	0.185	2.12	2.563	0
492	10	LP2052-2	50	9.42	9.605	0.185	2.127	2.574	0
493	10	LP2052-2	50	9.42	9.605	0.185	2.094	2.534	0
494	10	LP2052-2	50	9.42	9.605	0.185	2.092	2.529	0
495	10	LP2052-2	50	9.42	9.605	0.185	2.081	2.519	0
496	10	LP2052-2	50	9.42	9.605	0.185	2.096	2.534	0
497	10	LP2052-2	50	9.42	9.605	0.185	2.139	2.589	0
498	10	LP2052-2	50	9.42	9.605	0.185	2.102	2.544	0
499	10	LP2052-2	50	9.42	9.605	0.185	2.906	3.516	0
500	10	LP2052-2	50	9.42	9.605	0.185	2.899	3.508	0

Appendix B. Continued…

ShotNumber	TargetLocation	TestDevice	RFFrequency-MHz	RFStartTime-us	RFStopTime-us	RFTotalDuration-us	RFAvgPk-Volts	RFMaxPk-Volts	Upset
501	10	LP2052-2	50	9.42	9.605	0.185	2.878	3.481	0
502	10	LP2052-2	50	9.42	9.605	0.185	2.911	3.522	0
503	10	LP2052-2	50	9.42	9.605	0.185	2.954	3.572	1
504	10	LP2052-2	50	9.42	9.605	0.185	2.961	3.584	1
505	10	LP2052-2	50	9.42	9.605	0.185	2.923	3.538	1
506	10	LP2052-2	50	9.42	9.605	0.185	2.92	3.534	1
507	10	LP2052-2	50	9.42	9.605	0.185	3.918	4.737	1
508	10	LP2052-2	50	9.42	9.605	0.185	3.961	4.793	1
509	10	LP2052-2	50	9.42	9.605	0.185	3.925	4.75	1
510	10	LP2052-2	50	9.42	9.605	0.185	3.916	4.74	1
511	10	LP2052-2	50	9.42	9.605	0.185	3.878	4.693	1
512	10	LP2052-2	50	9.42	9.605	0.185	3.894	4.709	1
513	10	LP2052-2	50	9.42	9.605	0.185	3.893	4.712	0
514	10	LP2052-2	50	9.42	9.605	0.185	3.887	4.704	0
515	11	LP2052-1	50	9.605	9.79	0.185	3.612	4.369	0
516	11	LP2052-1	50	9.605	9.79	0.185	3.545	4.29	0
517	11	LP2052-1	50	9.605	9.79	0.185	4.18	5.059	0
518	11	LP2052-1	50	9.605	9.79	0.185	4.748	5.74	0
519	11	LP2052-1	50	9.605	9.79	0.185	4.25	5.141	0
520	11	LP2052-1	50	9.605	9.79	0.185	4.76	5.757	0
521	11	LP2052-1	50	9.605	9.79	0.185	3.858	4.669	0
522	11	LP2052-1	50	9.605	9.79	0.185	3.962	4.795	0
523	11	LP2052-1	50	9.605	9.79	0.185	4.023	4.868	0
524	11	LP2052-1	50	9.605	9.79	0.185	4.224	5.112	0
525	11	LP2052-1	50	9.605	9.79	0.185	4.547	5.499	0
526	11	LP2052-1	50	9.605	9.79	0.185	4.571	5.533	0
527	11	LP2052-1	50	9.605	9.79	0.185	4.556	5.515	0
528	11	LP2052-1	50	9.605	9.79	0.185	4.768	5.772	0
529	11	LP2052-1	50	9.605	9.79	0.185	4.699	5.687	0
530	11	LP2052-1	50	9.605	9.79	0.185	4.749	5.749	0
531	11	LP2052-1	50	9.605	9.79	0.185	4.761	5.755	0
532	11	LP2052-1	50	9.605	9.79	0.185	4.809	5.82	0
533	11	LP2052-2	50	9.605	9.79	0.185	4.438	5.917	0
534	11	LP2052-2	50	9.605	9.79	0.185	4.871	5.892	0
535	11	LP2052-2	50	9.605	9.79	0.185	4.825	5.838	0
536	11	LP2052-2	50	9.605	9.79	0.185	4.739	5.734	0
537	11	LP2052-2	50	9.605	9.79	0.185	4.791	5.798	0
538	11	LP2052-2	50	9.605	9.79	0.185	4.749	5.746	0
539	11	LP2052-2	50	9.605	9.79	0.185	4.932	5.968	0
540	11	LP2052-2	50	9.605	9.79	0.185	5.01	6.063	0
541	4	LP2052-1	50	8.8	8.87	0.07	1.405	1.7	0
542	4	LP2052-1	50	8.8	8.87	0.07	1.57	1.899	0
543	4	LP2052-1	50	8.8	8.87	0.07	1.808	2.189	0
544	4	LP2052-1	50	8.8	8.87	0.07	1.626	1.968	0
545	4	LP2052-1	50	8.8	8.87	0.07	1.716	2.077	0
546	4	LP2052-1	50	8.8	8.87	0.07	1.858	2.249	0
547	4	LP2052-1	50	8.8	8.87	0.07	2.133	2.579	0
548	4	LP2052-1	50	8.8	8.87	0.07	2.667	3.228	1
549	4	LP2052-1	50	8.8	8.87	0.07	1.042	1.261	0
550	4	LP2052-1	50	8.8	8.87	0.07	1.364	1.649	0
ShotNumber	TargetLocation	TestDevice	RFFrequency-MHz	RFStartTime-us	RFStopTime-us	RFTotalDuration-us	RFAvgPk-Volts	RFMaxPk-Volts	Upset
551	4	LP2052-1	50	8.8	8.87	0.07	1.499	1.814	0
552	4	LP2052-1	50	8.8	8.87	0.07	1.479	1.79	0
553	4	LP2052-1	50	8.8	8.87	0.07	1.614	1.953	0
554	4	LP2052-1	50	8.8	8.87	0.07	1.89	2.286	0
555	4	LP2052-1	50	8.8	8.87	0.07	1.856	2.246	0
556	4	LP2052-1	50	8.8	8.87	0.07	2.529	3.059	0
557	4	LP2052-1	50	8.8	8.87	0.07	3.614	4.374	0
558	4	LP2052-1	50	8.8	8.87	0.07	3.634	4.394	0
559	4	LP2052-1	50	8.8	8.87	0.07	1.964	2.377	1
560	4	LP2052-1	50	8.8	8.87	0.07	1.849	2.235	1
561	4	LP2052-1	50	8.8	8.87	0.07	2.287	2.765	0
562	4	LP2052-1	50	8.8	8.87	0.07	1.692	2.048	0
563	4	LP2052-1	50	8.8	8.87	0.07	1.692	2.048	0
564	4	LP2052-1	50	8.8	8.87	0.07	2.445	2.958	0
565	4	LP2052-1	50	8.8	8.87	0.07	2.872	3.475	0
566	4	LP2052-1	50	8.8	8.87	0.07	2.497	3.021	0
567	4	LP2052-1	50	8.8	8.87	0.07	2.785	3.371	0
568	4	LP2052-1	50	8.8	8.87	0.07	2.896	3.505	0
569	4	LP2052-1	50	8.8	8.87	0.07	3.013	3.647	1
570	4	LP2052-1	50	8.8	8.87	0.07	3.199	3.872	1
571	4	LP2052-1	50	8.8	8.87	0.07	3.595	4.35	0
572	4	LP2052-1	50	8.8	8.87	0.07	3.823	4.626	1
573	4	LP2052-1	50	8.8	8.87	0.07	3.715	4.492	1
574	4	LP2052-1	50	8.8	8.87	0.07	4.221	5.107	1
575	4	LP2052-1	50	8.8	8.87	0.07	3.834	4.639	1
576	4	LP2052-1	50	8.8	8.87	0.07	4.382	5.302	1
577	4	LP2052-1	50	8.8	8.87	0.07	4.172	5.043	1
578	4	LP2052-1	50	8.8	8.87	0.07	4.204	5.083	1
579	4	LP2052-1	50	8.8	8.87	0.07	4.168	5.042	1
580	4	LP2052-1	50	8.8	8.87	0.07	4.088	4.945	1
581	4	LP2052-1	50	8.8	8.87	0.07	4.301	5.205	1
582	4	LP2052-1	50	8.8	8.87	0.07	4.163	5.038	1
583	4	LP2052-1	50	8.8	8.87	0.07	4.157	5.031	1
584	4	LP2052-1	50	8.8	8.87	0.07	2.793	3.377	0
585	4	LP2052-1	50	8.8	8.87	0.07	2.975	3.601	1
586	4	LP2052-1	50	8.8	8.87	0.07	3.173	3.841	1
587	4	LP2052-1	50	8.8	8.87	0.07	3.496	4.232	0
588	4	LP2052-1	50	8.8	8.87	0.07	3.62	4.382	1
589	4	LP2052-1	50	8.8	8.87	0.07	3.116	3.767	0
590	4	LP2052-1	50	8.8	8.87	0.07	3.224	3.903	1
591	4	LP2052-1	50	8.8	8.87	0.07	3.6	4.353	1
592	4	LP2052-1	50	8.8	8.87	0.07	3.165	3.827	0
593	4	LP2052-1	50	8.8	8.87	0.07	3.306	3.997	0
594	4	LP2052-1	50	8.8	8.87	0.07	3.165	3.831	1
595	4	LP2052-1	50	8.8	8.87	0.07	2.687	3.253	0
596	4	LP2052-1	50	8.8	8.87	0.07	2.743	3.319	0
597	4	LP2052-1	50	8.8	8.87	0.07	2.814	3.405	0
598	4	LP2052-1	50	8.8	8.87	0.07	2.849	3.447	0
599	4	LP2052-1	50	8.8	8.87	0.07	3.065	3.709	0
600	4	LP2052-1	50	8.8	8.87	0.07	3.081	3.728	1

Appendix B. Continued…

ShotNumber	TargetLocation	TestDevice	RFFrequency-MHz	RFStartTime-us	RFStopTime-us	RFTotalDuration-us	RFAvgPk-Volts	RFMaxPk-Volts	Upset
601	4	LP2052-1	50	8.8	8.87	0.07	2.467	2.986	0
602	4	LP2052-1	50	8.8	8.87	0.07	2.615	3.162	0
603	4	LP2052-1	50	8.8	8.87	0.07	2.838	3.433	0
604	4	LP2052-1	50	8.8	8.87	0.07	2.977	3.604	0
605	4	LP2052-1	50	8.8	8.87	0.07	3.06	3.704	0
606	4	LP2052-1	50	8.8	8.87	0.07	2.956	3.577	0
607	4	LP2052-1	50	8.8	8.87	0.07	3.128	3.785	0
608	4	LP2052-1	50	8.8	8.87	0.07	3.182	3.847	0
609	4	LP2052-2	50	8.8	8.87	0.07	3.021	3.657	0
610	4	LP2052-2	50	8.8	8.87	0.07	3.426	4.147	0
611	4	LP2052-2	50	8.8	8.87	0.07	3.498	4.228	0
612	4	LP2052-2	50	8.8	8.87	0.07	3.554	4.302	0
613	4	LP2052-2	50	8.8	8.87	0.07	3.232	3.912	1
614	4	LP2052-2	50	8.8	8.87	0.07	3.393	4.107	1
615	4	LP2052-2	50	8.8	8.87	0.07	3.491	4.226	1
616	4	LP2052-2	50	8.8	8.87	0.07	3.87	4.683	1
617	4	LP2052-2	50	8.8	8.87	0.07	3.839	4.647	1
618	4	LP2052-2	50	8.8	8.87	0.07	3.971	4.801	1
619	4	LP2052-2	50	8.8	8.87	0.07	3.738	4.525	1
620	4	LP2052-2	50	8.8	8.87	0.07	3.952	4.782	1
621	4	LP2052-2	50	8.8	8.87	0.07	4.049	4.899	1
622	4	LP2052-2	50	8.8	8.87	0.07	3.86	4.672	1
623	4	LP2052-2	50	8.8	8.87	0.07	3.725	4.504	1
624	4	LP2052-2	50	8.8	8.87	0.07	3.009	3.642	0
625	4	LP2052-2	50	8.8	8.87	0.07	3.296	3.99	0
626	4	LP2052-2	50	8.8	8.87	0.07	2.685	3.25	0
627	4	LP2052-2	50	8.8	8.87	0.07	3.025	3.661	0
628	4	LP2052-2	50	8.8	8.87	0.07	2.797	3.386	1
629	4	LP2052-2	50	8.8	8.87	0.07	2.974	3.6	0
630	4	LP2052-2	50	8.8	8.87	0.07	3.017	3.652	0
631	4	LP2052-2	50	8.8	8.87	0.07	3.008	3.641	0
632	4	LP2052-2	50	8.8	8.87	0.07	3.187	3.858	1
633	4	LP2052-2	50	8.8	8.87	0.07	2.588	3.132	0
634	4	LP2052-2	50	8.8	8.87	0.07	2.867	3.47	0
635	4	LP2052-2	50	8.8	8.87	0.07	2.738	3.311	0
636	4	LP2052-2	50	8.8	8.87	0.07	2.914	3.526	1
637	4	LP2052-2	50	8.8	8.87	0.07	2.947	3.567	1
638	4	LP2052-2	50	8.8	8.87	0.07	2.378	2.878	0
639	4	LP2052-2	50	8.8	8.87	0.07	2.515	3.041	0
640	4	LP2052-2	50	8.8	8.87	0.07	2.686	3.249	0
641	4	LP2052-2	50	8.8	8.87	0.07	2.608	3.157	0
642	4	LP2052-2	50	8.8	8.87	0.07	2.613	3.163	0
643	4	LP2052-2	50	8.8	8.87	0.07	2.77	3.35	0
644	4	LP2052-2	50	8.8	8.87	0.07	2.723	3.296	1
645	4	LP2052-2	50	8.8	8.87	0.07	2.549	3.085	0
646	4	LP2052-2	50	8.8	8.87	0.07	2.313	2.8	0
647	4	LP2052-2	50	8.8	8.87	0.07	2.337	2.829	0
648	4	LP2052-2	50	8.8	8.87	0.07	2.382	2.881	0
649	4	LP2052-2	50	8.8	8.87	0.07	2.736	3.31	0
650	4	LP2052-2	50	8.8	8.87	0.07	2.487	3.01	0
ShotNumber	TargetLocation	TestDevice	RFFrequency-MHz	RFStartTime-us	RFStopTime-us	RFTotalDuration-us	RFAvgPk-Volts	RFMaxPk-Volts	Upset
651	4	LP2052-2	50	8.8	8.87	0.07	2.844	3.442	0
652	4	LP2052-2	50	8.8	8.87	0.07	2.701	3.266	0
653	4	LP2052-2	50	8.8	8.87	0.07	2.978	3.604	1
654	4	LP2052-2	50	8.8	8.87	0.07	3.188	3.856	0
655	4	LP2052-2	50	8.8	8.87	0.07	3.521	4.261	1
656	4	LP2052-2	50	8.8	8.87	0.07	3.759	4.55	1
657	4	LP2052-2	50	8.8	8.87	0.07	3.725	4.507	1
658	4	LP2052-2	50	8.8	8.87	0.07	3.545	4.29	1
659	5	LP2052-1	50	8.86	9.34	0.48	2.829	3.424	1
660	5	LP2052-1	50	8.86	9.34	0.48	3.09	3.738	0
661	5	LP2052-1	50	8.86	9.34	0.48	3.223	3.9	1
662	5	LP2052-1	50	8.86	9.34	0.48	3.404	4.12	1
663	5	LP2052-1	50	8.86	9.34	0.48	3.996	4.836	1
664	5	LP2052-1	50	8.86	9.34	0.48	4.161	5.036	1
665	5	LP2052-1	50	8.86	9.34	0.48	3.772	4.564	0
666	5	LP2052-1	50	8.86	9.34	0.48	3.846	4.654	1
667	5	LP2052-1	50	8.86	9.34	0.48	3.41	4.126	1
668	5	LP2052-1	50	8.86	9.34	0.48	3.661	4.427	1
669	5	LP2052-1	50	8.86	9.34	0.48	3.287	3.978	0
670	5	LP2052-1	50	8.86	9.34	0.48	3.487	4.22	0
671	5	LP2052-1	50	8.86	9.34	0.48	3.617	4.377	1
672	5	LP2052-1	50	8.86	9.34	0.48	2.548	3.082	0
673	5	LP2052-1	50	8.86	9.34	0.48	2.754	3.332	0
674	5	LP2052-1	50	8.86	9.34	0.48	2.534	3.065	0
675	5	LP2052-1	50	8.86	9.34	0.48	2.572	3.11	0
676	5	LP2052-1	50	8.86	9.34	0.48	2.749	3.326	1
677	5	LP2052-1	50	8.86	9.34	0.48	2.314	2.8	0
678	5	LP2052-1	50	8.86	9.34	0.48	2.441	2.954	0
679	5	LP2052-1	50	8.86	9.34	0.48	2.397	2.901	0
680	5	LP2052-1	50	8.86	9.34	0.48	2.502	3.028	0
681	5	LP2052-1	50	8.86	9.34	0.48	2.498	3.023	0
682	5	LP2052-1	50	8.86	9.34	0.48	2.659	3.217	0
683	5	LP2052-1	50	8.86	9.34	0.48	2.692	3.258	0
684	5	LP2052-1	50	8.86	9.34	0.48	2.702	3.271	0
685	5	LP2052-1	50	8.86	9.34	0.48	2.737	3.313	0
686	5	LP2052-1	50	8.86	9.34	0.48	2.852	3.451	1
687	5	LP2052-1	50	8.86	9.34	0.48	2.963	3.586	0
688	5	LP2052-1	50	8.86	9.34	0.48	3.025	3.659	0
689	5	LP2052-1	50	8.86	9.34	0.48	3.077	3.725	1
690	5	LP2052-1	50	8.86	9.34	0.48	2.576	3.118	0
691	5	LP2052-1	50	8.86	9.34	0.48	2.658	3.215	0
692	5	LP2052-1	50	8.86	9.34	0.48	2.766	3.347	0
693	5	LP2052-1	50	8.86	9.34	0.48	3.637	4.402	1
694	5	LP2052-1	50	8.86	9.34	0.48	4.11	4.974	1
695	5	LP2052-1	50	8.86	9.34	0.48	3.653	4.421	1
696	5	LP2052-1	50	8.86	9.34	0.48	3.414	4.126	1
697	5	LP2052-1	50	8.86	9.34	0.48	3.626	4.385	1
698	5	LP2052-1	50	8.86	9.34	0.48	3.283	3.973	1
699	5	LP2052-2	50	8.86	9.34	0.48	2.301	2.784	0
700	5	LP2052-2	50	8.86	9.34	0.48	2.406	2.91	0

Appendix B. Continued…

ShotNumber	TargetLocation	TestDevice	RFFrequency-MHz	RFStartTime-us	RFStopTime-us	RFTotalDuration-us	RFAvgPk-Volts	RFMaxPk-Volts	Upset
701	5	LP2052-2	50	8.86	9.34	0.48	2.497	3.021	1
702	5	LP2052-2	50	8.86	9.34	0.48	2.219	2.685	0
703	5	LP2052-2	50	8.86	9.34	0.48	2.186	2.644	0
704	5	LP2052-2	50	8.86	9.34	0.48	2.267	2.743	0
705	5	LP2052-2	50	8.86	9.34	0.48	2.359	2.853	1
706	5	LP2052-2	50	8.86	9.34	0.48	2.31	2.795	0
707	5	LP2052-2	50	8.86	9.34	0.48	2.523	3.053	0
708	5	LP2052-2	50	8.86	9.34	0.48	2.482	3.002	0
709	5	LP2052-2	50	8.86	9.34	0.48	2.592	3.137	0
710	5	LP2052-2	50	8.86	9.34	0.48	2.608	3.152	0
711	5	LP2052-2	50	8.86	9.34	0.48	2.742	3.319	0
712	5	LP2052-2	50	8.86	9.34	0.48	2.747	3.325	0
713	5	LP2052-2	50	8.86	9.34	0.48	2.796	3.384	1
714	5	LP2052-2	50	8.86	9.34	0.48	2.918	3.528	0
715	5	LP2052-2	50	8.86	9.34	0.48	2.933	3.547	1
716	5	LP2052-2	50	8.86	9.34	0.48	3.091	3.742	1
717	5	LP2052-2	50	8.86	9.34	0.48	3.284	3.974	0
718	5	LP2052-2	50	8.86	9.34	0.48	3.388	4.098	0
719	5	LP2052-2	50	8.86	9.34	0.48	3.441	4.162	0
720	5	LP2052-2	50	8.86	9.34	0.48	4.103	4.965	1
721	5	LP2052-2	50	8.86	9.34	0.48	4.454	5.388	1
722	5	LP2052-2	50	8.86	9.34	0.48	4.058	4.911	1
723	5	LP2052-2	50	8.86	9.34	0.48	3.622	4.383	1
724	5	LP2052-2	50	8.86	9.34	0.48	3.727	4.507	1
725	5	LP2052-2	50	8.86	9.34	0.48	3.917	4.739	1
726	5	LP2052-2	50	8.86	9.34	0.48	4.112	4.976	1
727	5	LP2052-2	50	8.86	9.34	0.48	4.329	5.234	1
728	5	LP2052-2	50	8.86	9.34	0.48	4.344	5.257	1
729	5	LP2052-2	50	8.86	9.34	0.48	3.985	4.821	1
730	5	LP2052-2	50	8.86	9.34	0.48	4.188	5.068	1
731	5	LP2052-2	50	8.86	9.34	0.48	3.895	4.714	1
732	5	LP2052-2	50	8.86	9.34	0.48	4.196	5.078	1
733	5	LP2052-2	50	8.86	9.34	0.48	4.215	5.096	1
734	6	LP2052-1	50	8.86	9.1	0.24	3.286	3.977	0
735	6	LP2052-1	50	8.86	9.1	0.24	4.095	4.951	1
736	6	LP2052-1	50	8.86	9.1	0.24	4.435	5.367	1
737	6	LP2052-1	50	8.86	9.1	0.24	4.51	5.453	1
738	6	LP2052-1	50	8.86	9.1	0.24	4.623	5.593	1
739	6	LP2052-1	50	8.86	9.1	0.24	4.182	5.056	1
740	6	LP2052-1	50	8.86	9.1	0.24	4.398	5.321	1
741	6	LP2052-1	50	8.86	9.1	0.24	2.781	3.365	0
742	6	LP2052-1	50	8.86	9.1	0.24	2.889	3.495	0
743	6	LP2052-1	50	8.86	9.1	0.24	3.021	3.654	0
744	6	LP2052-1	50	8.86	9.1	0.24	3.012	3.647	0
745	6	LP2052-1	50	8.86	9.1	0.24	3.072	3.717	0
746	6	LP2052-1	50	8.86	9.1	0.24	3.244	3.926	0
747	6	LP2052-1	50	8.86	9.1	0.24	3.179	3.845	0
748	6	LP2052-1	50	8.86	9.1	0.24	3.369	4.078	0
749	6	LP2052-1	50	8.86	9.1	0.24	3.416	4.132	0
750	6	LP2052-1	50	8.86	9.1	0.24	3.473	4.202	0
ShotNumber	TargetLocation	TestDevice	RFFrequency-MHz	RFStartTime-us	RFStopTime-us	RFTotalDuration-us	RFAvgPk-Volts	RFMaxPk-Volts	Upset
751	6	LP2052-1	50	8.86	9.1	0.24	3.495	4.229	0
752	6	LP2052-1	50	8.86	9.1	0.24	3.712	4.493	0
753	6	LP2052-1	50	8.86	9.1	0.24	3.802	4.602	0
754	6	LP2052-1	50	8.86	9.1	0.24	3.76	4.551	0
755	6	LP2052-1	50	8.86	9.1	0.24	3.799	4.594	0
756	6	LP2052-1	50	8.86	9.1	0.24	3.941	4.764	0
757	6	LP2052-1	50	8.86	9.1	0.24	4.003	4.843	1
758	6	LP2052-1	50	8.86	9.1	0.24	4.15	5.021	0
759	6	LP2052-1	50	8.86	9.1	0.24	4.154	5.027	1
760	6	LP2052-1	50	8.86	9.1	0.24	4.311	5.218	0
761	6	LP2052-1	50	8.86	9.1	0.24	4.374	5.293	0
762	6	LP2052-1	50	8.86	9.1	0.24	4.38	5.295	1
763	6	LP2052-1	50	8.86	9.1	0.24	4.491	5.435	1
764	6	LP2052-1	50	8.86	9.1	0.24	4.788	5.795	1
765	6	LP2052-1	50	8.86	9.1	0.24	4.841	5.855	1
766	6	LP2052-1	50	8.86	9.1	0.24	5.003	6.052	1
767	6	LP2052-1	50	8.86	9.1	0.24	5.07	6.13	1
768	6	LP2052-1	50	8.86	9.1	0.24	5.13	6.21	1
769	6	LP2052-1	50	8.86	9.1	0.24	5.263	6.368	1
770	6	LP2052-1	50	8.86	9.1	0.24	5.032	6.09	1
771	6	LP2052-1	50	8.86	9.1	0.24	5.028	6.085	1
772	6	LP2052-1	50	8.86	9.1	0.24	4.808	5.818	1
773	6	LP2052-1	50	8.86	9.1	0.24	4.843	5.86	1
774	6	LP2052-2	50	8.86	9.1	0.24	2.28	2.758	1
775	6	LP2052-2	50	8.86	9.1	0.24	2.425	2.935	0
776	6	LP2052-2	50	8.86	9.1	0.24	2.567	3.105	0
777	6	LP2052-2	50	8.86	9.1	0.24	2.507	3.03	0
778	6	LP2052-2	50	8.86	9.1	0.24	2.598	3.143	0
779	6	LP2052-2	50	8.86	9.1	0.24	2.67	3.232	0
780	6	LP2052-2	50	8.86	9.1	0.24	3.449	4.175	0
781	6	LP2052-2	50	8.86	9.1	0.24	3.613	4.368	0
782	6	LP2052-2	50	8.86	9.1	0.24	3.646	4.413	0
783	6	LP2052-2	50	8.86	9.1	0.24	3.714	4.494	0
784	6	LP2052-2	50	8.86	9.1	0.24	3.658	4.427	0
785	6	LP2052-2	50	8.86	9.1	0.24	3.784	4.578	0
786	6	LP2052-2	50	8.86	9.1	0.24	3.87	4.679	0
787	6	LP2052-2	50	8.86	9.1	0.24	3.977	4.81	0
788	6	LP2052-2	50	8.86	9.1	0.24	3.917	4.735	0
789	6	LP2052-2	50	8.86	9.1	0.24	4.094	4.954	1
790	6	LP2052-2	50	8.86	9.1	0.24	4.149	5.016	0
791	6	LP2052-2	50	8.86	9.1	0.24	4.224	5.112	0
792	6	LP2052-2	50	8.86	9.1	0.24	4.233	5.123	0
793	6	LP2052-2	50	8.86	9.1	0.24	4.363	5.279	1
794	6	LP2052-2	50	8.86	9.1	0.24	4.374	5.294	0
795	6	LP2052-2	50	8.86	9.1	0.24	4.384	5.303	0
796	6	LP2052-2	50	8.86	9.1	0.24	4.404	5.33	0
797	6	LP2052-2	50	8.86	9.1	0.24	4.376	5.296	0
798	6	LP2052-2	50	8.86	9.1	0.24	4.505	5.453	0
799	6	LP2052-2	50	8.86	9.1	0.24	4.49	5.431	0
800	6	LP2052-2	50	8.86	9.1	0.24	4.523	5.474	0

Appendix B. Continued…

ShotNumber	TargetLocation	TestDevice	RFFrequency-MHz	RFStartTime-us	RFStopTime-us	RFTotalDuration-us	RFAvgPk-Volts	RFMaxPk-Volts	Upset
801	6	LP2052-2	50	8.86	9.1	0.24	4.493	5.431	0
802	6	LP2052-2	50	8.86	9.1	0.24	4.568	5.528	0
803	6	LP2052-2	50	8.86	9.1	0.24	4.548	5.503	0
804	6	LP2052-2	50	8.86	9.1	0.24	4.582	5.546	0
805	6	LP2052-2	50	8.86	9.1	0.24	4.691	5.671	0
806	6	LP2052-2	50	8.86	9.1	0.24	4.662	5.642	0
807	6	LP2052-2	50	8.86	9.1	0.24	4.758	5.758	1
808	6	LP2052-2	50	8.86	9.1	0.24	4.356	5.271	1
809	6	LP2052-2	50	8.86	9.1	0.24	5.23	6.327	1
810	6	LP2052-2	50	8.86	9.1	0.24	5.247	6.351	1
811	6	LP2052-2	50	8.86	9.1	0.24	5.285	6.389	1
812	6	LP2052-2	50	8.86	9.1	0.24	5.294	6.407	1
813	6	LP2052-2	50	8.86	9.1	0.24	5.26	6.359	1
814	6	LP2052-2	50	8.86	9.1	0.24	5.306	6.415	1
815	6	LP2052-2	50	8.86	9.1	0.24	5.32	6.436	1
816	6	LP2052-2	50	8.86	9.1	0.24	5.324	6.443	1
817	6	LP2052-2	50	8.86	9.1	0.24	5.288	6.397	1
818	6	LP2052-2	50	8.86	9.1	0.24	5.34	6.463	1
819	6	LP2052-2	50	8.86	9.1	0.24	4.48	5.423	1
820	6	LP2052-2	50	8.86	9.1	0.24	3.988	4.821	1
821	6	LP2052-2	50	8.86	9.1	0.24	4.239	5.13	1
822	6	LP2052-2	50	8.86	9.1	0.24	4.401	5.327	1
823	6	LP2052-2	50	8.86	9.1	0.24	4.436	5.369	1
824	6	LP2052-2	50	8.86	9.1	0.24	4.519	5.466	1
825	6	LP2052-2	50	8.86	9.1	0.24	4.667	5.646	1
826	8	LP2052-1	50	9.32	9.38	0.06	0.7238	0.8751	0
827	8	LP2052-1	50	9.32	9.38	0.06	0.7432	0.8986	0
828	8	LP2052-1	50	9.32	9.38	0.06	0.8324	1.008	1
829	8	LP2052-1	50	9.32	9.38	0.06	0.701	0.8473	0
830	8	LP2052-1	50	9.32	9.38	0.06	0.436	0.5273	0
831	8	LP2052-1	50	9.32	9.38	0.06	0.6226	0.753	0
832	8	LP2052-1	50	9.32	9.38	0.06	0.5234	0.6335	0
833	8	LP2052-1	50	9.32	9.38	0.06	0.622	0.7518	0
834	8	LP2052-1	50	9.32	9.38	0.06	0.528	0.6391	0
835	8	LP2052-1	50	9.32	9.38	0.06	0.7832	0.948	0
836	8	LP2052-1	50	9.32	9.38	0.06	0.7756	0.9387	0
837	8	LP2052-1	50	9.32	9.38	0.06	0.6218	0.7523	0
838	8	LP2052-1	50	9.32	9.38	0.06	0.6061	0.733	0
839	8	LP2052-1	50	9.32	9.38	0.06	0.6365	0.7706	0
840	8	LP2052-1	50	9.32	9.38	0.06	0.7353	0.8898	0
841	8	LP2052-1	50	9.32	9.38	0.06	1.195	1.447	1
842	8	LP2052-1	50	9.32	9.38	0.06	1.091	1.321	0
843	8	LP2052-1	50	9.32	9.38	0.06	1.191	1.442	1
844	8	LP2052-1	50	9.32	9.38	0.06	1.293	1.565	1
845	8	LP2052-1	50	9.32	9.38	0.06	1.311	1.587	1
846	8	LP2052-1	50	9.32	9.38	0.06	1.397	1.689	1
847	8	LP2052-1	50	9.32	9.38	0.06	1.242	1.503	0
848	8	LP2052-1	50	9.32	9.38	0.06	1.207	1.459	1
849	8	LP2052-1	50	9.32	9.38	0.06	1.247	1.509	1
850	8	LP2052-1	50	9.32	9.38	0.06	1.507	1.825	1
ShotNumber	TargetLocation	TestDevice	RFFrequency-MHz	RFStartTime-us	RFStopTime-us	RFTotalDuration-us	RFAvgPk-Volts	RFMaxPk-Volts	Upset
851	8	LP2052-1	50	9.32	9.38	0.06	1.512	1.83	0
852	8	LP2052-1	50	9.32	9.38	0.06	1.703	2.06	1
853	8	LP2052-1	50	9.32	9.38	0.06	1.749	2.118	1
854	8	LP2052-1	50	9.32	9.38	0.06	1.64	1.986	0
855	8	LP2052-1	50	9.32	9.38	0.06	1.767	2.14	1
856	8	LP2052-1	50	9.32	9.38	0.06	1.657	2.005	1
857	8	LP2052-1	50	9.32	9.38	0.06	1.95	2.36	1
858	8	LP2052-1	50	9.32	9.38	0.06	1.814	2.195	1
859	8	LP2052-1	50	9.32	9.38	0.06	1.865	2.256	0
860	8	LP2052-1	50	9.32	9.38	0.06	2.36	2.856	1
861	8	LP2052-1	50	9.32	9.38	0.06	2.274	2.751	1
862	8	LP2052-1	50	9.32	9.38	0.06	2.334	2.824	0
863	8	LP2052-1	50	9.32	9.38	0.06	2.837	3.431	1
864	8	LP2052-1	50	9.32	9.38	0.06	2.919	3.529	1
865	8	LP2052-1	50	9.32	9.38	0.06	2.714	3.28	1
866	8	LP2052-1	50	9.32	9.38	0.06	2.924	3.539	1
867	8	LP2052-2	50	9.32	9.38	0.06	1.008	1.219	0
868	8	LP2052-2	50	9.32	9.38	0.06	0.8298	1.004	0
869	8	LP2052-2	50	9.32	9.38	0.06	0.9095	1.101	0
870	8	LP2052-2	50	9.32	9.38	0.06	0.9241	1.118	1
871	8	LP2052-2	50	9.32	9.38	0.06	0.8419	1.018	0
872	8	LP2052-2	50	9.32	9.38	0.06	0.8882	1.075	0
873	8	LP2052-2	50	9.32	9.38	0.06	0.7867	0.9517	0
874	8	LP2052-2	50	9.32	9.38	0.06	1.06	1.283	1
875	8	LP2052-2	50	9.32	9.38	0.06	1.046	1.266	0
876	8	LP2052-2	50	9.32	9.38	0.06	1.068	1.293	0
877	8	LP2052-2	50	9.32	9.38	0.06	1.197	1.447	1
878	8	LP2052-2	50	9.32	9.38	0.06	1.08	1.308	0
879	8	LP2052-2	50	9.32	9.38	0.06	1.008	1.219	0
880	8	LP2052-2	50	9.32	9.38	0.06	1.033	1.249	0
881	8	LP2052-2	50	9.32	9.38	0.06	1.227	1.485	1
882	8	LP2052-2	50	9.32	9.38	0.06	1.07	1.295	1
883	8	LP2052-2	50	9.32	9.38	0.06	1.189	1.44	0
884	8	LP2052-2	50	9.32	9.38	0.06	1.342	1.624	0
885	8	LP2052-2	50	9.32	9.38	0.06	1.407	1.702	1
886	8	LP2052-2	50	9.32	9.38	0.06	1.345	1.626	0
887	8	LP2052-2	50	9.32	9.38	0.06	1.442	1.744	0
888	8	LP2052-2	50	9.32	9.38	0.06	1.543	1.868	1
889	8	LP2052-2	50	9.32	9.38	0.06	1.325	1.604	1
890	8	LP2052-2	50	9.32	9.38	0.06	1.079	1.306	1
891	8	LP2052-2	50	9.32	9.38	0.06	0.6568	0.7942	0
892	8	LP2052-2	50	9.32	9.38	0.06	0.8454	1.023	0
893	8	LP2052-2	50	9.32	9.38	0.06	0.6598	0.7987	0
894	8	LP2052-2	50	9.32	9.38	0.06	0.7271	0.8793	0
895	8	LP2052-2	50	9.32	9.38	0.06	0.9328	1.129	1
896	8	LP2052-2	50	9.32	9.38	0.06	0.6343	0.7676	0
897	8	LP2052-2	50	9.32	9.38	0.06	0.7752	0.9382	0
898	8	LP2052-2	50	9.32	9.38	0.06	0.5463	0.6604	0
899	8	LP2052-2	50	9.32	9.38	0.06	0.7451	0.9007	0
900	8	LP2052-2	50	9.32	9.38	0.06	0.6093	0.7376	0

Appendix B. Continued…

ShotNumber	TargetLocation	TestDevice	RFFrequency-MHz	RFStartTime-us	RFStopTime-us	RFTotalDuration-us	RFAvgPk-Volts	RFMaxPk-Volts	Upset
901	8	LP2052-2	50	9.32	9.38	0.06	0.8031	0.9716	1
902	8	LP2052-2	50	9.32	9.38	0.06	1.092	1.321	1
903	8	LP2052-2	50	9.32	9.38	0.06	1.18	1.428	1
904	8	LP2052-2	50	9.32	9.38	0.06	1.082	1.31	0
905	8	LP2052-2	50	9.32	9.38	0.06	1.381	1.671	1
906	8	LP2052-2	50	9.32	9.38	0.06	1.607	1.946	1
907	8	LP2052-2	50	9.32	9.38	0.06	1.875	2.269	1
908	8	LP2052-2	50	9.32	9.38	0.06	1.871	2.263	0
909	8	LP2052-2	50	9.32	9.38	0.06	2.084	2.522	1
910	8	LP2052-2	50	9.32	9.38	0.06	2.027	2.453	0
911	8	LP2052-2	50	9.32	9.38	0.06	2.073	2.509	0
912	8	LP2052-2	50	9.32	9.38	0.06	2.472	2.992	0
913	8	LP2052-2	50	9.32	9.38	0.06	2.964	3.587	1
914	9	LP2052-1	50	9.42	9.79	0.37	2.58	3.122	0
915	9	LP2052-1	50	9.42	9.79	0.37	2.803	3.39	0
916	9	LP2052-1	50	9.42	9.79	0.37	2.872	3.476	0
917	9	LP2052-1	50	9.42	9.79	0.37	2.893	3.501	0
918	9	LP2052-1	50	9.42	9.79	0.37	2.982	3.608	0
919	9	LP2052-1	50	9.42	9.79	0.37	3.014	3.644	0
920	9	LP2052-1	50	9.42	9.79	0.37	3.122	3.776	0
921	9	LP2052-1	50	9.42	9.79	0.37	3.173	3.84	0
922	9	LP2052-1	50	9.42	9.79	0.37	3.894	4.711	1
923	9	LP2052-1	50	9.42	9.79	0.37	3.49	4.221	1
924	9	LP2052-1	50	9.42	9.79	0.37	3.537	4.276	0
925	9	LP2052-1	50	9.42	9.79	0.37	3.693	4.468	1
926	9	LP2052-1	50	9.42	9.79	0.37	3.748	4.533	1
927	9	LP2052-1	50	9.42	9.79	0.37	3.84	4.645	1
928	9	LP2052-1	50	9.42	9.79	0.37	3.978	4.814	1
929	9	LP2052-1	50	9.42	9.79	0.37	4.005	4.847	1
930	9	LP2052-1	50	9.42	9.79	0.37	4.13	4.994	1
931	9	LP2052-1	50	9.42	9.79	0.37	4.244	5.131	1
932	9	LP2052-1	50	9.42	9.79	0.37	4.24	5.13	1
933	9	LP2052-1	50	9.42	9.79	0.37	4.218	5.105	1
934	9	LP2052-1	50	9.42	9.79	0.37	4.368	5.286	1
935	9	LP2052-1	50	9.42	9.79	0.37	4.467	5.407	1
936	9	LP2052-1	50	9.42	9.79	0.37	4.148	5.02	1
937	9	LP2052-1	50	9.42	9.79	0.37	4.32	5.224	1
938	9	LP2052-1	50	9.42	9.79	0.37	3.402	4.112	1
939	9	LP2052-1	50	9.42	9.79	0.37	3.523	4.263	1
940	9	LP2052-1	50	9.42	9.79	0.37	2.989	3.618	0
941	9	LP2052-2	50	9.42	9.79	0.37	3.378	4.086	1
942	9	LP2052-2	50	9.42	9.79	0.37	2.901	3.509	1
943	9	LP2052-2	50	9.42	9.79	0.37	2.373	2.872	1
944	9	LP2052-2	50	9.42	9.79	0.37	1.912	2.314	0
945	9	LP2052-2	50	9.42	9.79	0.37	1.964	2.377	0
946	9	LP2052-2	50	9.42	9.79	0.37	2.005	2.427	0
947	9	LP2052-2	50	9.42	9.79	0.37	2.055	2.486	1
948	9	LP2052-2	50	9.42	9.79	0.37	2.21	2.675	1
949	9	LP2052-2	50	9.42	9.79	0.37	2.313	2.799	1
950	9	LP2052-2	50	9.42	9.79	0.37	2.458	2.974	1
ShotNumber	TargetLocation	TestDevice	RFFrequency-MHz	RFStartTime-us	RFStopTime-us	RFTotalDuration-us	RFAvgPk-Volts	RFMaxPk-Volts	Upset
951	9	LP2052-2	50	9.42	9.79	0.37	2.592	3.136	1
952	9	LP2052-2	50	9.42	9.79	0.37	2.67	3.228	1
953	9	LP2052-2	50	9.42	9.79	0.37	2.782	3.366	1
954	9	LP2052-2	50	9.42	9.79	0.37	2.877	3.483	1
955	9	LP2052-2	50	9.42	9.79	0.37	2.534	3.067	1
956	9	LP2052-2	50	9.42	9.79	0.37	2.117	2.56	1
957	9	LP2052-2	50	9.42	9.79	0.37	1.726	2.086	0
958	9	LP2052-2	50	9.42	9.79	0.37	1.826	2.21	0
959	9	LP2052-2	50	9.42	9.79	0.37	1.893	2.291	1
960	9	LP2052-2	50	9.42	9.79	0.37	1.531	1.851	0
961	9	LP2052-2	50	9.42	9.79	0.37	1.583	1.916	0
962	9	LP2052-2	50	9.42	9.79	0.37	1.625	1.967	0
963	9	LP2052-2	50	9.42	9.79	0.37	1.65	1.996	0
964	9	LP2052-2	50	9.42	9.79	0.37	1.72	2.082	0
965	9	LP2052-2	50	9.42	9.79	0.37	1.735	2.098	0
966	9	LP2052-2	50	9.42	9.79	0.37	1.779	2.153	0
967	9	LP2052-2	50	9.42	9.79	0.37	1.806	2.186	0
968	9	LP2052-2	50	9.42	9.79	0.37	1.853	2.242	0
969	9	LP2052-2	50	9.42	9.79	0.37	1.918	2.321	0
970	9	LP2052-2	50	9.42	9.79	0.37	1.977	2.393	1
971	10	LP2052-1	50	9.42	9.605	0.185	2.17	2.625	0
972	10	LP2052-1	50	9.42	9.605	0.185	2.235	2.703	1
973	10	LP2052-1	50	9.42	9.605	0.185	2.391	2.894	1
974	10	LP2052-1	50	9.42	9.605	0.185	2.551	3.087	1
975	10	LP2052-1	50	9.42	9.605	0.185	2.88	3.486	0
976	10	LP2052-1	50	9.42	9.605	0.185	3.192	3.864	1
977	10	LP2052-1	50	9.42	9.605	0.185	3.38	4.09	1
978	10	LP2052-1	50	9.42	9.605	0.185	2.822	3.413	1
979	10	LP2052-1	50	9.42	9.605	0.185	2.965	3.584	1
980	10	LP2052-1	50	9.42	9.605	0.185	3.121	3.778	1
981	10	LP2052-1	50	9.42	9.605	0.185	2.562	3.101	1
982	10	LP2052-1	50	9.42	9.605	0.185	2.728	3.301	1
983	10	LP2052-1	50	9.42	9.605	0.185	2.227	2.695	1
984	10	LP2052-1	50	9.42	9.605	0.185	2.341	2.834	1
985	10	LP2052-1	50	9.42	9.605	0.185	1.852	2.24	0
986	10	LP2052-1	50	9.42	9.605	0.185	1.925	2.329	0
987	10	LP2052-1	50	9.42	9.605	0.185	1.948	2.357	0
988	10	LP2052-1	50	9.42	9.605	0.185	2.022	2.447	1
989	10	LP2052-1	50	9.42	9.605	0.185	1.604	1.941	0
990	10	LP2052-1	50	9.42	9.605	0.185	1.663	2.013	0
991	10	LP2052-1	50	9.42	9.605	0.185	1.701	2.058	0
992	10	LP2052-1	50	9.42	9.605	0.185	1.727	2.09	0
993	10	LP2052-1	50	9.42	9.605	0.185	1.763	2.133	0
994	10	LP2052-1	50	9.42	9.605	0.185	1.796	2.174	0
995	10	LP2052-1	50	9.42	9.605	0.185	1.859	2.248	0
996	10	LP2052-1	50	9.42	9.605	0.185	1.889	2.287	0
997	10	LP2052-1	50	9.42	9.605	0.185	1.946	2.355	0
998	10	LP2052-1	50	9.42	9.605	0.185	1.995	2.415	0
999	10	LP2052-1	50	9.42	9.605	0.185	2.065	2.499	0
1000	10	LP2052-1	50	9.42	9.605	0.185	2.095	2.535	1

Appendix B. Continued…

ShotNumber	TargetLocation	TestDevice	RFFrequency-MHz	RFStartTime-us	RFStopTime-us	RFTotalDuration-us	RFAvgPk-Volts	RFMaxPk-Volts	Upset
1001	10	LP2052-1	50	9.42	9.605	0.185	2.248	2.72	1
1002	10	LP2052-1	50	9.42	9.605	0.185	2.356	2.851	1
1003	10	LP2052-1	50	9.42	9.605	0.185	2.519	3.049	1
1004	10	LP2052-2	50	9.42	9.605	0.185	2.084	2.522	0
1005	10	LP2052-2	50	9.42	9.605	0.185	2.14	2.589	1
1006	10	LP2052-2	50	9.42	9.605	0.185	2.267	2.744	1
1007	10	LP2052-2	50	9.42	9.605	0.185	2.426	2.936	1
1008	10	LP2052-2	50	9.42	9.605	0.185	2.526	3.054	1
1009	10	LP2052-2	50	9.42	9.605	0.185	2.656	3.215	1
1010	10	LP2052-2	50	9.42	9.605	0.185	2.771	3.35	1
1011	10	LP2052-2	50	9.42	9.605	0.185	2.874	3.476	1
1012	10	LP2052-2	50	9.42	9.605	0.185	2.37	2.868	1
1013	10	LP2052-2	50	9.42	9.605	0.185	2.509	3.036	1
1014	10	LP2052-2	50	9.42	9.605	0.185	2.071	2.506	0
1015	10	LP2052-2	50	9.42	9.605	0.185	2.088	2.524	0
1016	10	LP2052-2	50	9.42	9.605	0.185	2.161	2.614	1
1017	10	LP2052-2	50	9.42	9.605	0.185	1.741	2.107	0
1018	10	LP2052-2	50	9.42	9.605	0.185	1.81	2.19	0
1019	10	LP2052-2	50	9.42	9.605	0.185	1.842	2.228	0
1020	10	LP2052-2	50	9.42	9.605	0.185	1.885	2.278	0
1021	10	LP2052-2	50	9.42	9.605	0.185	1.921	2.322	0
1022	10	LP2052-2	50	9.42	9.605	0.185	1.987	2.402	0
1023	10	LP2052-2	50	9.42	9.605	0.185	2.018	2.442	0
1024	10	LP2052-2	50	9.42	9.605	0.185	2.076	2.511	0
1025	10	LP2052-2	50	9.42	9.605	0.185	2.116	2.561	1
1026	10	LP2052-2	50	9.42	9.605	0.185	2.303	2.787	1
1027	10	LP2052-2	50	9.42	9.605	0.185	2.42	2.929	1
1028	10	LP2052-2	50	9.42	9.605	0.185	2.527	3.059	1
1029	10	LP2052-2	50	9.42	9.605	0.185	2.736	3.311	1
1030	10	LP2052-2	50	9.42	9.605	0.185	2.85	3.449	1
1031	8	LP2052-2	50	9.32	9.38	0.06	1.1234	1.492	1
1032	8	LP2052-2	50	9.32	9.38	0.06	0.9327	1.129	0
1033	8	LP2052-2	50	9.32	9.38	0.06	1.174	1.421	1
1034	8	LP2052-2	50	9.32	9.38	0.06	0.9478	1.147	0
1035	8	LP2052-2	50	9.32	9.38	0.06	0.9944	1.204	0
1036	8	LP2052-2	50	9.32	9.38	0.06	1.127	1.364	0
1037	8	LP2052-2	50	9.32	9.38	0.06	1.15	1.392	1
1038	8	LP2052-2	50	9.32	9.38	0.06	1.112	1.345	1
1039	8	LP2052-2	50	9.32	9.38	0.06	1.355	1.641	1
1040	8	LP2052-2	50	9.32	9.38	0.06	1.437	1.737	1
1041	8	LP2052-2	50	9.32	9.38	0.06	1.277	1.545	0
1042	8	LP2052-2	50	9.32	9.38	0.06	1.271	1.537	0
1043	8	LP2052-2	50	9.32	9.38	0.06	1.341	1.623	0
1044	8	LP2052-2	50	9.32	9.38	0.06	1.427	1.725	1
1045	8	LP2052-2	50	9.32	9.38	0.06	1.434	1.736	0
1046	8	LP2052-2	50	9.32	9.38	0.06	1.573	1.903	1
1047	8	LP2052-2	50	9.32	9.38	0.06	1.723	2.086	1
1048	8	LP2052-2	50	9.32	9.38	0.06	1.777	2.15	1
1049	8	LP2052-2	50	9.32	9.38	0.06	1.653	2.001	0
1050	8	LP2052-2	50	9.32	9.38	0.06	1.623	1.964	0
ShotNumber	TargetLocation	TestDevice	RFFrequency-MHz	RFStartTime-us	RFStopTime-us	RFTotalDuration-us	RFAvgPk-Volts	RFMaxPk-Volts	Upset
1051	8	LP2052-2	50	9.32	9.38	0.06	1.791	2.167	1
1052	8	LP2052-2	50	9.32	9.38	0.06	1.963	2.376	1
1053	8	LP2052-2	50	9.32	9.38	0.06	1.889	2.286	0
1054	8	LP2052-2	50	9.32	9.38	0.06	1.969	2.384	1
1055	8	LP2052-2	50	9.32	9.38	0.06	2.048	2.478	1
1056	8	LP2052-2	50	9.32	9.38	0.06	2.127	2.575	1
1057	8	LP2052-2	50	9.32	9.38	0.06	2.24	2.711	1
1058	8	LP2052-2	50	9.32	9.38	0.06	2.172	2.627	1
1059	8	LP2052-2	50	9.32	9.38	0.06	2.223	2.688	1
1060	8	LP2052-2	50	9.32	9.38	0.06	2.436	2.948	1
1061	8	LP2052-2	50	9.32	9.38	0.06	2.379	2.88	1
1062	8	LP2052-2	50	9.32	9.38	0.06	2.446	2.96	1
1063	8	LP2052-2	50	9.32	9.38	0.06	1.912	2.315	1
1064	8	LP2052-2	50	9.32	9.38	0.06	1.068	1.292	0
1065	8	LP2052-2	50	9.32	9.38	0.06	1.055	1.275	1
1066	8	LP2052-2	50	9.32	9.38	0.06	0.7612	0.9214	0
1067	8	LP2052-2	50	9.32	9.38	0.06	0.596	0.7212	1
1068	8	LP2052-2	50	9.32	9.38	0.06	0.6271	0.7592	0
1069	8	LP2052-2	50	9.32	9.38	0.06	0.4826	0.5842	0
1070	8	LP2052-2	50	9.32	9.38	0.06	0.6955	0.8415	0
1071	8	LP2052-2	50	9.32	9.38	0.06	0.6839	0.8271	0
1072	8	LP2052-2	50	9.32	9.38	0.06	0.5978	0.723	0
1073	8	LP2052-2	50	9.32	9.38	0.06	0.538	0.6512	0
1074	8	LP2052-2	50	9.32	9.38	0.06	0.5403	0.6535	0
1075	8	LP2052-2	50	9.32	9.38	0.06	0.5353	0.648	0
1076	8	LP2052-2	50	9.32	9.38	0.06	0.7864	0.9516	0
1077	8	LP2052-2	50	9.32	9.38	0.06	0.6082	0.736	0
1078	9	LP2052-2	50	9.42	9.79	0.37	2.773	3.697	1
1079	9	LP2052-2	50	9.42	9.79	0.37	2.829	3.423	1
1080	9	LP2052-2	50	9.42	9.79	0.37	2.351	2.843	1
1081	9	LP2052-2	50	9.42	9.79	0.37	2.542	3.073	1
1082	9	LP2052-2	50	9.42	9.79	0.37	2.046	2.477	1
1083	9	LP2052-2	50	9.42	9.79	0.37	2.189	2.646	1
1084	9	LP2052-2	50	9.42	9.79	0.37	2.327	2.816	1
1085	9	LP2052-2	50	9.42	9.79	0.37	1.91	2.311	0
1086	9	LP2052-2	50	9.42	9.79	0.37	1.921	2.322	0
1087	9	LP2052-2	50	9.42	9.79	0.37	2.003	2.423	0
1088	9	LP2052-2	50	9.42	9.79	0.37	2.021	2.446	1
1089	9	LP2052-2	50	9.42	9.79	0.37	2.159	2.612	0
1090	9	LP2052-2	50	9.42	9.79	0.37	2.225	2.693	1
1091	9	LP2052-2	50	9.42	9.79	0.37	2.309	2.794	1
1092	9	LP2052-2	50	9.42	9.79	0.37	2.369	2.868	1
1093	9	LP2052-2	50	9.42	9.79	0.37	2.481	3.002	1
1094	9	LP2052-2	50	9.42	9.79	0.37	2.662	3.221	1
1095	9	LP2052-2	50	9.42	9.79	0.37	1.712	2.073	0
1096	9	LP2052-2	50	9.42	9.79	0.37	1.745	2.109	0
1097	9	LP2052-2	50	9.42	9.79	0.37	1.798	2.176	0
1098	9	LP2052-2	50	9.42	9.79	0.37	1.816	2.197	0
1099	9	LP2052-2	50	9.42	9.79	0.37	2.856	2.247	0
1100	9	LP2052-2	50	9.42	9.79	0.37	1.939	2.346	0

Appendix B. Continued…

ShotNumber	TargetLocation	TestDevice	RFFrequency-MHz	RFStartTime-us	RFStopTime-us	RFTotalDuration-us	RFAvgPk-Volts	RFMaxPk-Volts	Upset
1101	9	LP2052-2	50	9.42	9.79	0.37	1.981	2.397	0
1102	9	LP2052-2	50	9.42	9.79	0.37	2.025	2.451	0
1103	9	LP2052-2	50	9.42	9.79	0.37	2.067	2.502	1
1104	9	LP2052-2	50	9.42	9.79	0.37	2.207	2.671	1
1105	9	LP2052-2	50	9.42	9.79	0.37	2.356	2.848	1
1106	9	LP2052-2	50	9.42	9.79	0.37	1.442	1.745	0
1107	9	LP2052-2	50	9.42	9.79	0.37	1.45	1.755	0
1108	10	LP2052-2	50	9.42	9.605	0.185	1.847	2.236	0
1109	10	LP2052-2	50	9.42	9.605	0.185	1.903	2.303	0
1110	10	LP2052-2	50	9.42	9.605	0.185	1.947	2.355	0
1111	10	LP2052-2	50	9.42	9.605	0.185	1.976	2.392	0
1112	10	LP2052-2	50	9.42	9.605	0.185	2.032	2.458	0
1113	10	LP2052-2	50	9.42	9.605	0.185	2.098	2.537	1
1114	10	LP2052-2	50	9.42	9.605	0.185	2.191	2.652	0
1115	10	LP2052-2	50	9.42	9.605	0.185	2.211	2.676	1
1116	10	LP2052-2	50	9.42	9.605	0.185	2.354	2.85	1
1117	10	LP2052-2	50	9.42	9.605	0.185	2.455	2.969	1
1118	10	LP2052-2	50	9.42	9.605	0.185	2.532	3.064	1
1119	10	LP2052-2	50	9.42	9.605	0.185	2.747	3.325	1
1120	10	LP2052-2	50	9.42	9.605	0.185	2.945	3.561	1
1121	10	LP2052-2	50	9.42	9.605	0.185	3.055	3.698	1
1122	10	LP2052-2	50	9.42	9.605	0.185	3.201	3.872	1
1123	10	LP2052-2	50	9.42	9.605	0.185	3.286	3.973	1
1124	10	LP2052-2	50	9.42	9.605	0.185	3.445	4.166	1
1125	10	LP2052-2	50	9.42	9.605	0.185	2.295	2.778	1
1126	10	LP2052-2	50	9.42	9.605	0.185	1.357	1.641	0
1127	10	LP2052-2	50	9.42	9.605	0.185	1.391	1.683	0
1128	10	LP2052-2	50	9.42	9.605	0.185	1.423	1.721	0
1129	10	LP2052-2	50	9.42	9.605	0.185	1.455	1.758	0
1130	10	LP2052-2	50	9.42	9.605	0.185	1.492	1.806	0
1131	10	LP2052-2	50	9.42	9.605	0.185	1.535	1.858	0
1132	10	LP2052-2	50	9.42	9.605	0.185	1.58	1.912	0
1133	10	LP2052-2	50	9.42	9.605	0.185	1.626	1.966	0
1134	10	LP2052-2	50	9.42	9.605	0.185	1.65	1.996	0

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