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Numerical Modeling Analysis of Wafer Warpage and Carrier Mobility Change due to Tapered Through-Silicon-Via Geometry

by

Jingjing Dou

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Abstract

Three-dimensional integration is a solution that vertically stacks multiple layers of silicon chips by Through-Silicon-Vias (TSVs) to enhance the performance of microelectronic devices. The tapered TSV profile can help to overcome the technical difficulties. However, an easily overlooked issue is that tapered TSV can cause wafer warpage during the fabrication processes. Wafer warpage can cause chip misalignment and impose additional deformation. In an effort to investigate the TSV geometric effect, a large number of finite element analysis (FEA) simulations were performed to quantify the thermal stress distribution and the thermally induced curvature. It was found that the tapered geometry alone can induce significant wafer bending, which has not been reported by other researchers. The effect of taper angle, TSV radius, TSV pitch, and wafer thickness were quantitatively studied. In addition, the incorporations of anisotropic silicon property and intermediate layers between the copper TSV and silicon into the numerical models were assessed. Thermally induced stress concentration around copper TSV near the wafer surface can lead to degradation of the device performance by affecting the carrier mobility in transistors. This piezoresistivity effect can cause serious reliability concerns. The size of keep-out zone (KOZ), which is identified as a threshold of 5% carrier mobility change, was also quantified for various transistor types in different channel directions.

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Acronym

TSV	through-silicon-via
FEA	finite element analysis
KOZ	keep-out zone
3D	three-dimensional
IC	integrated circuit
RC	resistive-capacitive
CMOS	complementary metal-oxide-semiconductor
CIS	complementary metal-oxide-semiconductor image sensor
MEMS	micro-electro-mechanical systems
RF	radio frequency
CTE	coefficient of thermal expansion
DRIE	deep reactive-ion etching
PECVD	plasma-enhanced chemical vapor deposition
PVD	physical-vapor deposition
CMP	chemical-mechanical polishing
STS	surface technology system
ICP	inductive coupled plasma
SACVD	sub-atmospheric chemical vapor deposition
DoE	design of experiment

CNT   carbon nanotubes

FEOL   front end-of-line

BEOL   back end-of-line

RDL   fine redistribution layer

Fab   semiconductor fabrication plant

Chapter 1

Introduction

When the size of microelectronic devices is scaled down, physical limitations are encountered [1]. Three-dimensional integration is a solution that vertically stacks multiple layers of electronic components by Through-Silicon-Vias (TSVs), to enhance the performance of microelectronic devices beyond the 22 nm technology node. 3D integration comprises 3D IC integration and 3D silicon integration [2-3]. In 3D silicon integration, TSV wafers are bonded without any bumps by wafer-to-wafer bonding technique, while in 3D IC integration, active IC chips are integrated by microbumps, which are between them, or by solder bumps with the substrate [3]. There are many benefits to 3D integration, including lower power dissipation, higher electrical performance, wider bandwidth, and lower cost. TSV is the heart of three-dimensional integration technology that provides the shortest interconnection with high chip density to enable direct transmission of signals and to reduce the resistive-capacitive (RC) delay. TSV interconnection has been applied to wafer-level packaging of complementary metal-oxide-semiconductor (CMOS) image sensor (CIS) [4] and to other heterogeneous devices, such as MEMS, RF, and optical devices. The embedded TSVs in the chips may cause some critical reliability concerns and thermal management challenges. Due to the significant mismatch in coefficient of thermal expansion (CTE) between different materials, such as copper-filled via ($17.5\times10^{-6}/\mathrm{℃}$) and surrounding silicon ($2.5\times10^{-6}/\mathrm{℃}$), large thermo-mechanical stresses will be generated during wafer fabrication [5]. This would lead to the failures of materials, such as low-k dielectric material cracking, delamination, and severe electromigtation, all of which will

eventually shorten the chip's lifetime [5]. Overheating is another issue because (a) some materials in 3D-ICs (TSV structure), such as solder bumps and oxide layers, have poor heat conductivities; (b) the heat generated in multi stacked chips is high; and (c) there is limited space for cooling channels. The silicon dioxide and back end-of-line (BEOL) layers can be cracked due to copper pumping during heating [6]. Keep-out zone (KOZ) is a term for the highly stressed region around TSV, where the performance of electronic devices is degraded. Owing to large carrier mobility change in KOZ, no transistors should exist. X-ray mircodiffraction used to measure the stress near the interface of TSV shows that the KOZ is approximately 17 µm in radius [7]. Known-good die (KGD) is a characteristic that affects the 3D integration manufacturing yield. Enhancing KGD is a significant issue. For homogeneous structures, the yield is $y = Y^N$, in which N is the stacking number of the chips and Y is the yield of the individual chip. The heterogeneous structure chips can be stacked in one package to achieve multiple functions. The yield of heterogeneous chips is given by $y = X^N Y^M Z^P$.... In addition, more efforts should be made on improving thin-wafer handling, process parameter optimization, wafer-to-wafer bonding misalignment, wafer distortion, among others.

Thermal stress in straight TSV structure has been studied extensively [8-12]. However, the effect of tapered TSV geometry has received little attention. The tapered TSV profile helps to overcome the technical difficulties of conformal depositions of the isolation dielectric layer, diffusion barrier layer, and copper seed layer, and to ease the void-free copper electroplating process [13]. It has been reported that the tapered TSV has the lowest reflection noise and signal loss, compared to straight TSV [14]. An easily overlooked issue is that the tapered TSV can cause chip warpage. Many sources, such as thick copper overburden, thin film residual stresses, and high annealing temperature, can result in wafer warpage. The large thermal stress generated by CTE mismatch between microbumps and chips or two neighboring heterogeneous chips in multilayer stacking configurations also can cause warpage. Wafer warpage can cause bump failure and die misalignment issues. Che et al. reported that the TSV wafer warpage linearly increases with the annealing temperature and copper overburden thickness [15]. The warpage decreases with the number of stacked chips because each additional chip stiffens the structure further [16]. A primary contribution of the present thesis work is to illustrate, through numerical analysis,

that the tapered TSV can give rise to wafer warpage, the extent of which is comparable to typically measured warpage caused by other means. Throughout the present analysis, the thermal stress and deformation fields, along with their influence on carrier mobility change, are also examined.

Chapter 2

Overview of Fabrication Process

The overall TSV fabrication process flow consists of five main steps and can be summarized as follows. First, the vias are etched by deep reactive-ion etching (DRIE). The dielectric layer is subsequently deposited by plasma-enhanced chemical vapor deposition (PECVD) [1]. Next, the barrier and seed metallization are carried out by physical-vapor deposition (PVD). The following step is via filling by electroplating. The last step is copper overburden removal and wafer thinning by chemical-mechanical polishing (CMP).

Vias can be fabricated by two means of etching processes, laser drilling and deep reactive-ion etching (DRIE). It is very efficient to etch a small amount of low aspect ratio vias in a single chip by laser drilling. However, because the surface is rough after drilling, chemical polishing is required to attain a smooth wall, which increases the manufacturing cost. Compared to laser drilling, DRIE plays a more important role in 3D integration. Because the vias are formed as blind holes through the wafers, the thickness of which ranges from 30 µm to 200 µm, the aspect ratio may exceed 50. The Bosch process, which originally was developed for MEMS fabrication to achieve vertical sidewalls, has been applied extensively for high aspect ratio straight vias. The DRIE Bosch technology is an anisotropic etching process which the etching and passivation steps alternate to form the vias. The vias are etched in a Surface Technology System (STS) inductive coupled plasma (ICP) system [17]. The chemical reactions are taken by F+ and SFx+ ion bombardment to silicon by using sulfur hexafluoride (SF_6) as the feedgas. The passivation is accomplished by deposition of a $(C_xF_y)_n$ polymer layer on the sidewall, which decomposed from C_4F_8 feedgas. It is known that the Bosch process fabricates the vias with rough and scalloped

sidewalls because of the cyclic etching/passivation processes. Klumpp et al. developed a sub-atmospheric chemical vapor deposition (SACVD) process to reduce the sidewall roughness [18]. Tapered sidewall vias could ensure that there is adequate coverage during silicon dioxide/diffusion barrier/seed layer depositions and ease the subsequent via electroplating process. Numerous studies have been devoted to parametrically investigating the tapered TSV etching process with small scalloped sidewalls while keeping the required aspect ratio.

Tapered sidewall vias normally are developed by three etching process steps. First, straight sidewalls with slightly reentrant are accomplished with a high etch rate by using the Bosch anisotropic etching process. The second step is a non-Bosch isotropic process that to control the positive sidewall angle. The final step is the corner-rounding.

Ranganathan et al. introduced the step-by-step etching mechanism and profile evolution of tapered via [13]. Praveen et al. improved the Bosch process to produce tapered vias with a single DRIE step by gradually ramping down the platen power during alternating etching and passivating cycles, and tuning the etch recipe cycle time and gas flow to reduce the scallop size [19]. Other researchers [20-21] studied the effect of the process parameters, such as SF_6/O_2 mixture gas pressure and gas flow ratio, to efficiently etch the vias by adjustment of the platen power for given gas mixture and process pressure. The design of experiment (DoE) is executed to determine the optimal etch rate of the TSVs. It is found that the larger the via diameter, the higher the TSV etch rate [22].

There are two methods for depositing dielectric layers to avoid current leakage and cross talk. One is the thermal oxidation, and the other is plasma-enhanced chemical vapor deposition (PECVD). The uniform SiO_2 can be fabricated in a furnace over 1000 ℃. Because most devices on the chips could endure only less than 400 ℃, the thermal oxidation must be dropped for most cases. The dielectric layers deposited by PECVD are nonuniform, however, they could be formed under 400 ℃ in the PECVD systems manufactured by SPTS or other companies.

The diffusion barrier layer and seed layer are formed by physical vapor deposition (PVD). The common materials of the barrier layer are titanium (Ti) and tantalum (Ta).

TSV is filled by copper by electroplating. Copper has good heat and electrical conductivities. Some researchers studied other materials, such as carbon nanotubes (CNT) [23-24] and tungsten, as filling via materials. Plating solution and plating current are the key contributors to void-free copper filling for high aspect ratio tapered vias [25]. Selvanayagam et al. suggested that partially electroplating the via walls with copper, instead of completely filling the whole vias, could reduce the thermal stress and lower the cost [26].

Copper overburden needs to be removed by chemical-mechanical polishing (CMP). It can cause severe wafer warpage. Huang, et al suggested that partially removing copper overburden prior to the annealing process can reduce the wafer warpage [27].

Front end-of-line (FEOL) is a process that devices are fabricated in semiconductor fabrication plants (fabs) from a bare wafer to layer metallization. Back end-of-line (BEOL) is a process that connects the devices with the wafer. Vias can be formed by via-first (via fabrication before FEOL), via-middle (via fabrication after FEOL and prior to BEOL), and via-last (via fabrication after BEOL). Via-last usually is carried out in fabs with small diameter vias and fine redistribution layers (RDLs).
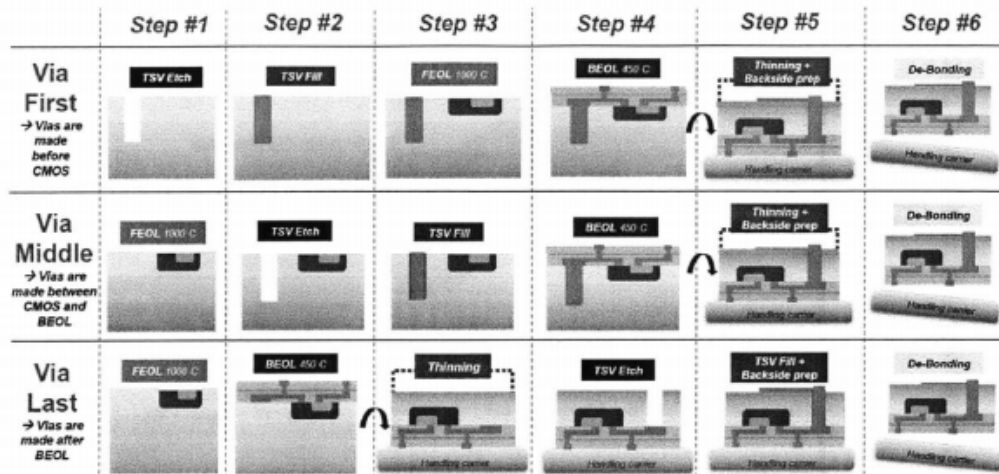
Figure 1: Comparison between via-first, via-middle and via-last 3D TSV integration scenarios [28].

Chapter 3

Numerical Model

Finite element analysis (FEA) simulations are carried out to predict the thermally induced out-of-plane deformation and to gain insight into thermal stress distribution in silicon wafers containing tapered TSVs. The simulations are performed by the ANSYS mechanical software package.

Figure 2 (a) shows a part of the periodic arrangement of the TSV silicon wafer. The xz-plane is the silicon wafer plane, with the thickness direction being along the y-axis. The square enclosed by the dashed lines indicates a full unit cell (repeating unit structure). To enhance the computational efficiency, a quarter of a 3D TSV unit cell model was established with the suitable boundary conditions applied. Figure 2 (b) shows the actual computational domain. It is not practical to model the entire wafer with the detailed TSV structure, because doing so will require a large number of nodes [15]. Due to the symmetry, the displacement of the boundary planes, x = 0 and z = 0, are constrained to be zero in the x and z directions, respectively, during the analysis. The nodes in these two boundary planes, x = 0 and z = 0, are permitted to have tangential displacements. Point O in Figure 2 (b) is set to be fixed in order to avoid deviation-induced error. The top and bottom surfaces of the model are set to be traction free. In reality, the Bosch etch process will cause sidewall roughness and scallops. In the model, it is assumed that the sidewall is smooth. The copper-filled TSV and its surrounding silicon are perfectly bonded, therefore the

displacement field across the interface is continuous [5]. The 3D coupled-field solid element was used for the entire analysis. The radius and diameter of the TSV top surface, the radius and diameter of the TSV bottom surface, the pitch between two adjacent TSVs, and the thickness of the wafer (TSV depth) are denoted as r1, d1, r2, d2, p, and h, respectively.

(a)
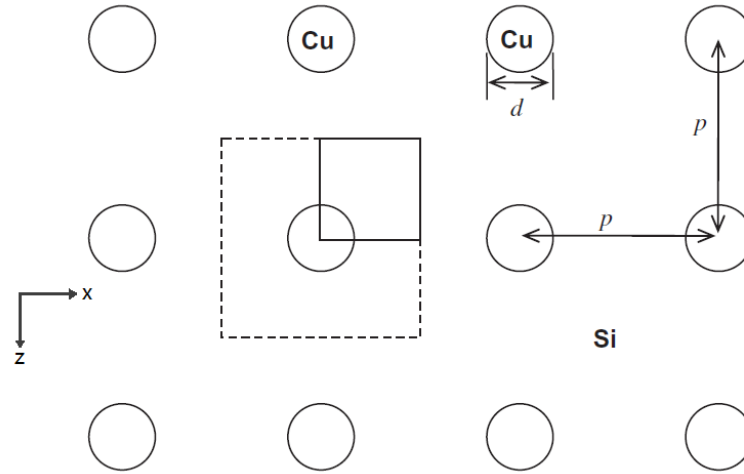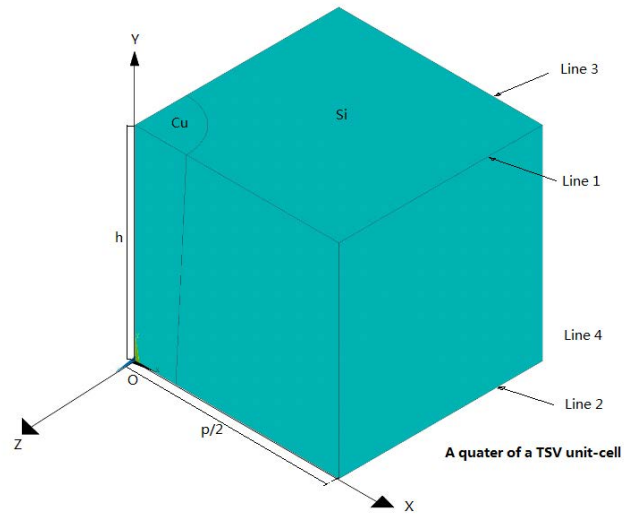
(b)

Figure 2 (a) The top view of the periodic arrangement of TSV silicon wafer, and (b) the 3D computational domain

In some of the models, a 1µm-thick silicon dioxide layer and a 0.1µm-thick tantalum (Ta) diffusion barrier layer between copper and silicon are included. The diameters of the copper TSVs in these models are kept as the same as the ones in models that without intermediate layers.

The intrinsic stresses induced by additional fabrication processes could interfere with the thermal stress generated by the cooling process or other thermal loading conditions. In the present study, the intrinsic stresses are ignored for simplicity.

The TSVs are assumed to be equally distributed as a square arrangement with the same pitch in the wafer. The TSV unit cell structure is periodic with respect to the entire wafer, rather than being a stand-alone module. In order to maintain the periodic structure, appropriate boundary conditions are needed. The nodes in the planes x = p/2 and z = -p/2 are constrained by the "slider" element, which allows a "slave" node to slide on a line joining by two "master" nodes. The nodes in Line 1, Line 2, Line 3 and Line 4 are treated as master nodes. The nodes in Line 1 and Line 2 are separately coupled in the x direction, therefore the nodes along their respective lines have the same x-component of displacement. At the same time, the master nodes in Line 3 and Line 4 are separately coupled in the z direction.

In reality, there could be three kinds of wafer warpages, cylindrical, spherical, and saddle, which are caused by various reasons [29]. The CTE-mismatch induced deformation in the current model setups will only generate spherical warpage.

Because the appropriate kind of coupled-field element is used, the coupled structural and steady-state thermal analyses can be performed. The initial temperature and the reference temperature are specified as 250 ℃, because the cooling process usually is carried out from this temperature. The reference temperature is applied as the stress-free temperature for thermal-stress calculations. In most cases, a 20 ℃ temperature is applied on all the nodes in the models for the static analyses. In the analysis that quantifies the wafer curvature with respect to the temperature change, the temperature function T=250-38.3333×Step Number (℃) is applied on all the nodes in the models. Therefore, a six-step procedure is implemented.

The silicon, silicon dioxide, and tantalum are considered as isotropic linear elastic solids. The copper is defined as an isotropic elastic-plastic solid material with linear-strain hardening, which follows the von Mises criterion and flow theory [5].

The material properties used in the FEA models are listed in the Table 1 below.

	Copper	Silicon	Silicon Dioxide	Tantalum
Yongs Modulus (MPa)	1.1×10^5	1.3×10^5	7.31×10^4	1.86×10^5
Poisson's Ratio	0.34	0.28	0.17	0.34
CTE (1/℃)	1.70×10^{-5}	2.60×10^{-6}	5.50×10^{-7}	6.50×10^{-6}
Thermal conductivity (W/(m×K))	401	149	1.4	57.5
Density (g/(mm)^3)	8.90×10^{-3}	2.33×10^{-3}	2.20×10^{-3}	1.67×10^{-2}
Initial Yield Stress (MPa)	155			
Tangent Modulus (GPa)	17.8			

Table 1: Material properties

A large number of models with regular configurations are simulated, as listed in the Table 2.

Section	the angle of the tapered TSV				the base radius of the TSV					wafer thickness				pitch		silicon elastic property		intermediate layers		loading condition	
	0°	3°	6°	9°	5 µm	10 µm	15 µm	20 µm	25 µm	h=50 µm	h=75 µm	h=100 µm	h=125 µm	p=100 µm	p=200 µm	isotropic	anisotropic	without	with	cooling process	pure mechanical bending
4.1 baseline models	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆				◆		◆		◆		◆	
4.2 curvature evolution		◆				◆				◆				◆		◆		◆		◆	
4.3 pure mechanical bending		◆				◆				◆				◆		◆		◆			◆
4.4 models with intermediate layers	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆				◆		◆			◆	◆	
4.5 anisotropic models	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆				◆			◆	◆		◆	
4.6 different thicknesses models	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆		◆		◆		◆	
4.7 different pitches models	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆					◆	◆		◆		◆	

Table 2: Configurations of model

Chapter 4

Results and Discussion: Thermal Stresses and Wafer Curvature

4.1 The Stress fields and Curvature after the Cooling Process

The baseline models without silicon dioxide and barrier/seed layers are first considered. The pitch between two adjacent TSVs is fixed at 100 µm. The units for displacements and stresses in contour plots generated by ANSYS are millimeter (mm) and mega Pascal (MPa) correspondingly.

Figure 3 (a)-(e) show the contour plots of the x displacement (u_x), the x-component of stress (σ_{xx}), the xy-shear stress (σ_{xy}), the von Mises stress, and the equivalent plastic strain after the cooling process, respectively. The TSV structure in the model has a base radius of 10 µm and a 3° tapered profile. It can be seen that the boundary surface area x = p/2 is perfectly constrained to be a plane by the slider elements in Figure 3 (a). The displacement field is very nonuniform. The edge of the TSV at the boundary plane z = 0 near the top and bottom free surfaces has the greatest negative x deformation. This is because the top and bottom surfaces of copper TSV are free, so their contraction is less constrained by silicon compared to the central portion of the TSV. In other words, the strain energy can be more easily released from these surfaces. The TSV is perfectly bonded with its surrounding

silicon. The interface between copper and silicon is continuous, therefore the edge of the silicon has the same displacement as the edge of the copper TSV. It is noticed in the contour plot of the x-component of stress (Figure 3 (b)) that the tensile x-component of stress exceeds 333 MPa at the center of the TSV, and both ends of the TSV are subject to compressive x-component of stresses. There are x-component of stress concentrations at the edge of the TSV near the top and bottom surfaces of silicon. In Figure 3 (c), the shear stress is located at the copper and silicon interfaces near the free surface. The shear stress may cause delamination at the interface and result in "copper-pumping" to crack the on-chip structures. The large stress concentration at the interface can also be observed in the von Mises stress contour plot, as shown in Figure 3 (d). The maximum value of the von Mises stress exceeds 645 MPa inside silicon. The equivalent plastic strain also is located near the top and bottom free surfaces along the material interface, as shown in Figure 3 (e). The observations above indicate that the internal damage in the TSV structure is a real possibility, due to the thermally induced stresses alone.

(a)

(b)

(c)

(d)

14
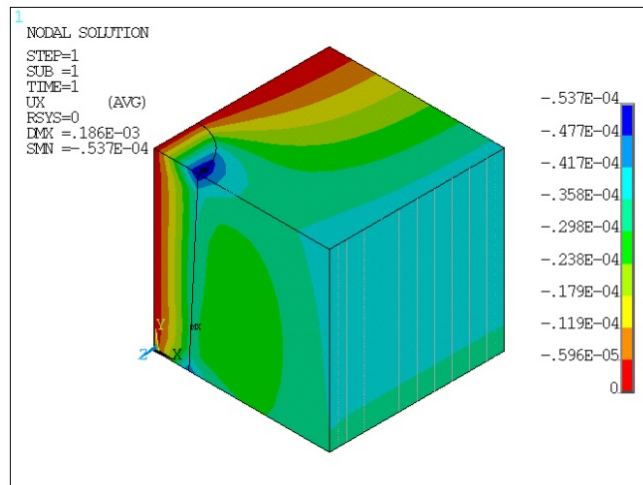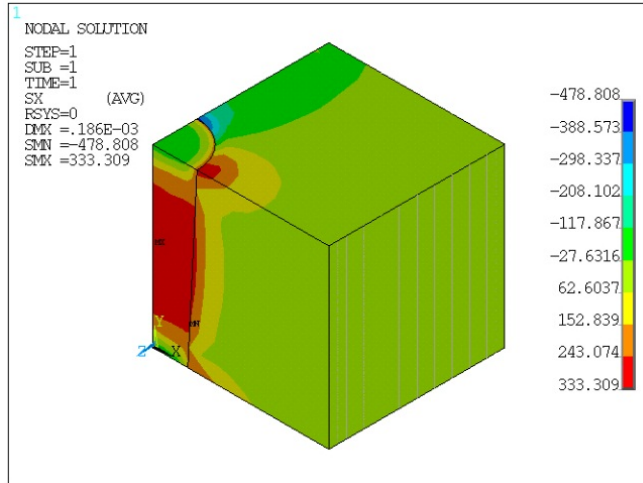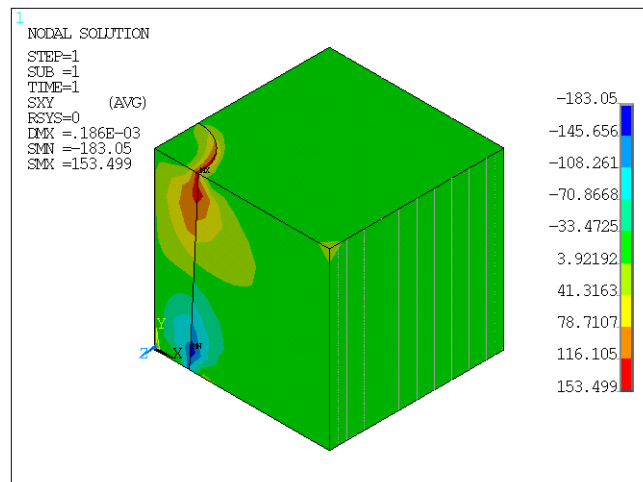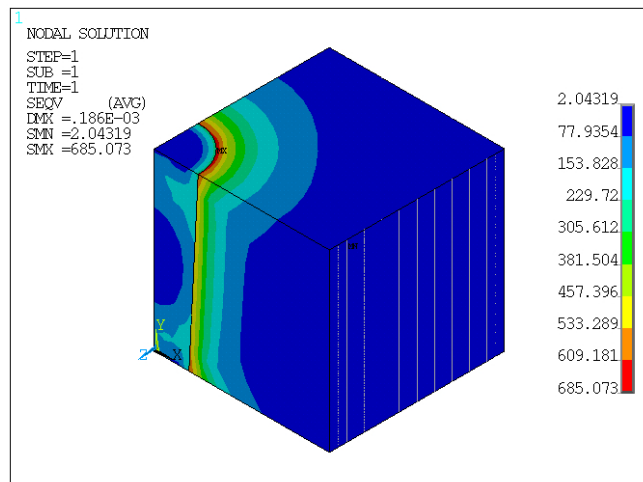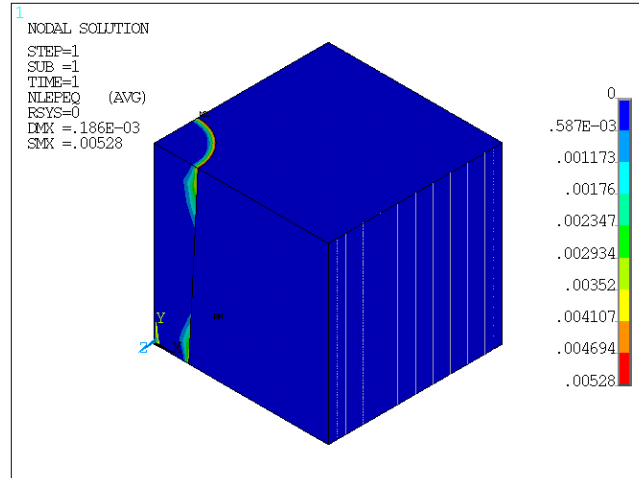
(e)

Figure 3: Contour plots of (a) the x displacement (u_x) (mm), (b) the x-component of stress (σ_{xx}) (MPa), (c) the xy-shear stress (σ_{xy}) (MPa), (d) the von Mises stress (MPa), and (e) the equivalent plastic strain after the cooling process. The model represents a quarter of a TSV unit cell in the 50 µm thickness isotropic silicon wafer. The TSV structure has a base radius of 10 µm and a 3° tapered profile.

The models with a fixed 10 µm base radius of the TSV and increased taper angles are analyzed. Figure 4 (a)-(d) show the x-displacements in the cases of 0°, 3°, 6°, and 9° taper angles, respectively, after cooling. It can be seen in Figure 4 (a) that the surface x = p/2 is vertical in the model which has the straight TSV structure. It indicates that the entire wafer is flat, therefore no warpage occurs. Figure 5 shows that the maximum magnitude of the x displacement increases linearly as the angle of the tapered TSV increases.
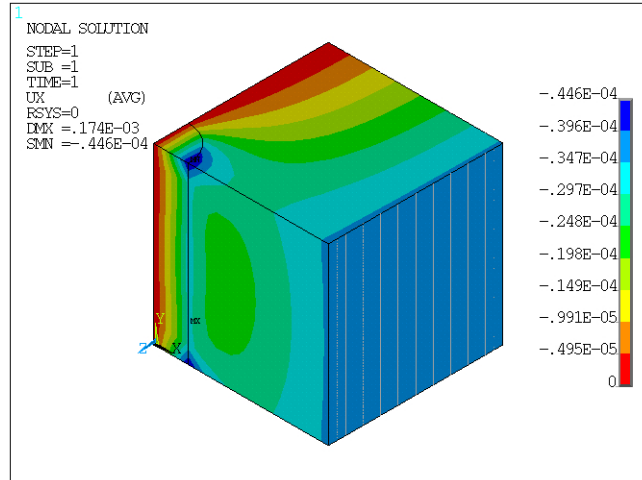
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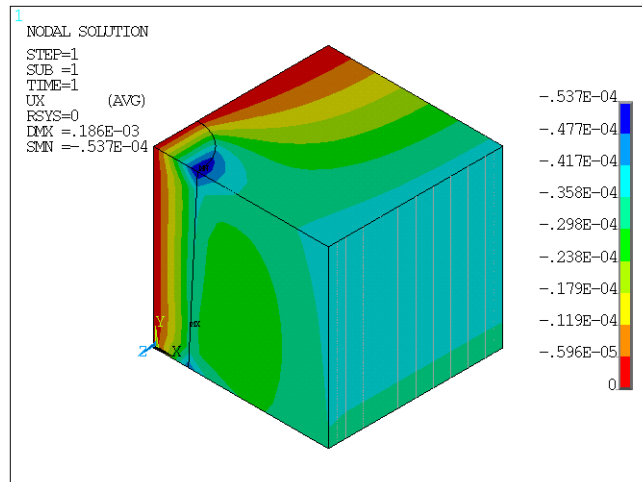
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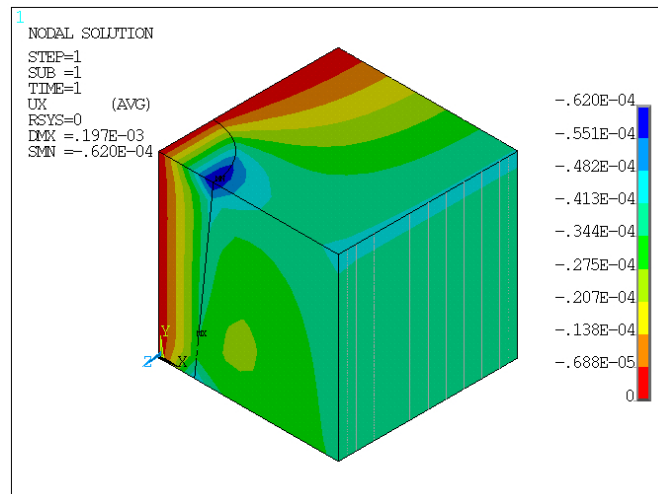
(c)

(d)

Figure 4: Comparison of the contour plots of the x displacement after the cooling process. The models represent a quarter of a TSV unit cell in the 50 µm thickness isotropic silicon wafer. The TSV structures have a fixed 10 µm base radius and (a) 0°, (b) 3°, (c) 6°, and (d) 9° tapered profiles.

Figure 5: The maximum values of the x displacement with respect to different angles of TSVs when the base radius of the TSV is fixed at 10 µm.

Figure 6 (a)-(d) show the x-component of stresses in the cases of 0°, 3°, 6°, and 9° taper angles, respectively, after cooling. Figure 7 (a)-(d) illustrate the von Mises stresses in the cases of 0°, 3°, 6°, and 9° taper angles after cooling, respectively. It is observed in Figure 6 and Figure 8 that the area, where high x-component of stress and von Mises stress are concentrated, tends to expand as the taper angle increases. Figure 8 demonstrates that the maximum compressive σ_{xx} in silicon increases linearly with the taper angle, while the maximum tensile σ_{xx} in copper stays relatively unchanged. The maximum value of the von Mises stress also approximately increases linearly with tapering, as shown in Figure 9.
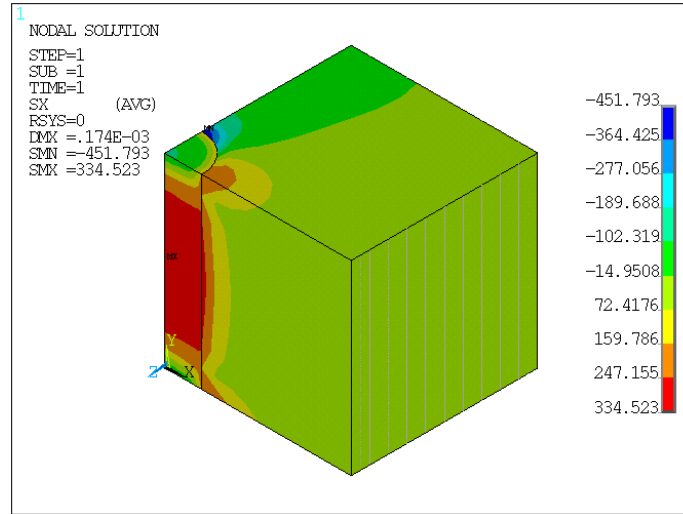
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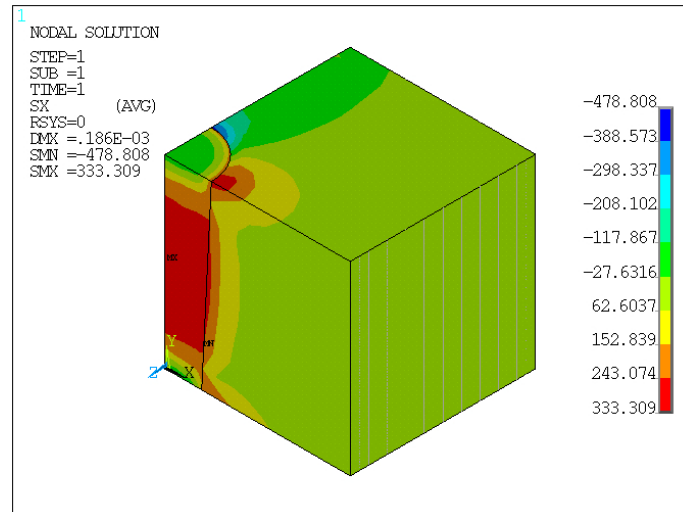
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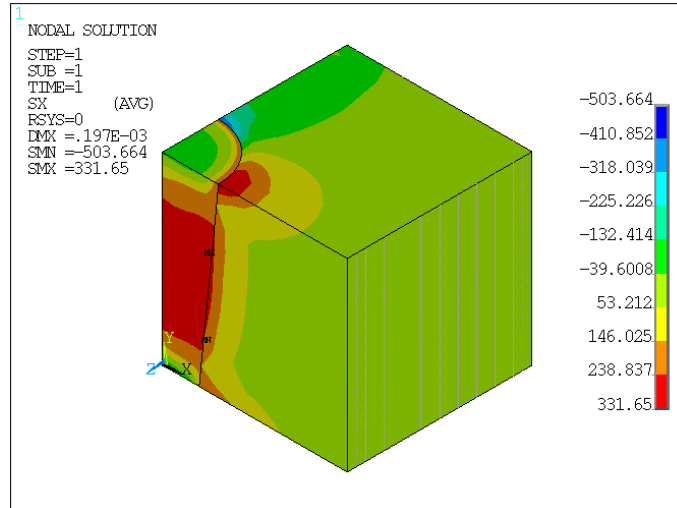
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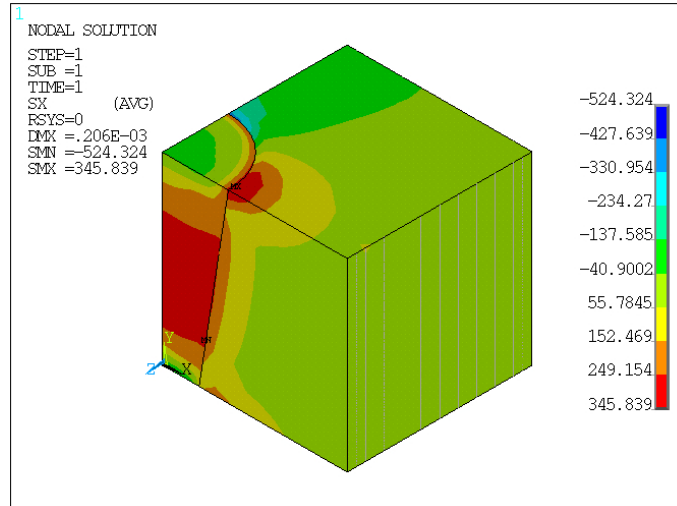
(d)

Figure 6: Comparison of the contour plots of the x-component of stress after the cooling process. The models represent a quarter of a TSV unit cell in the 50 μm thickness isotropic silicon wafer. The TSV structures have a fixed 10 μm base radius and (a) 0°, (b) 3°, (c) 6°, and (d) 9° tapered profiles.

(a)

(b)

(c)

(d)

Figure 7: Comparison of the contour plots of the von Mises stress after the cooling process. The models represent a quarter of a TSV unit cell in the 50 μm thickness isotropic silicon wafer. The TSV structures have a fixed 10 μm base radius and (a) 0°, (b) 3°, (c) 6°, and (d) 9° tapered profiles.

Figure 8: The maximum values of the x-component of stress with respect to different angles of TSVs when the base radius of the TSV is fixed at 10 μm.

Figure 9: The maximum values of the von Mises stress with respect to different angles of TSVs when the base radius of the TSV is fixed at 10 µm.

Figure 10 (a)-(d) show the xy-shear stresses in the cases of 0°, 3°, 6°, and 9° TSV tapered profiles, respectively, after cooling. It can be seen in the straight TSV model that the largest positive and negative xy-shear stresses are in silicon near the top and bottom surfaces. However, in the tapered TSV models, the largest positive xy-shear stress near the top surface is inside the TSV and the largest negative xy-shear stress near the bottom surface is inside the silicon. Apparently, the deviation from 90° between the interface and free surface created an uneven material distribution, which influences the local shear stress across the interface.
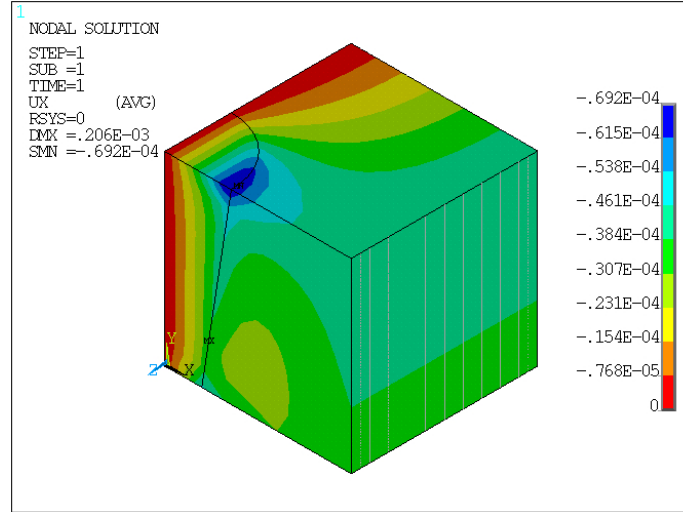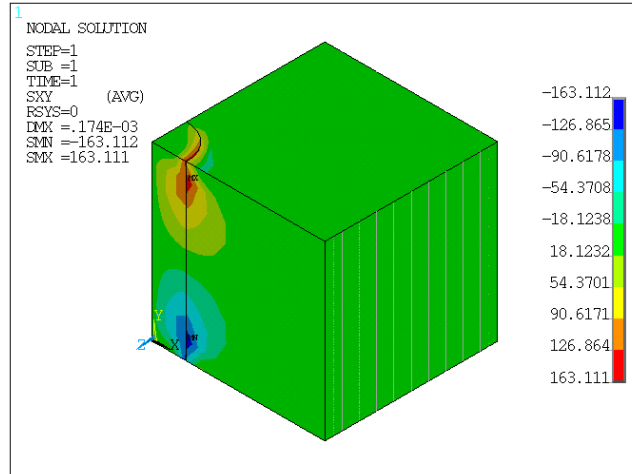
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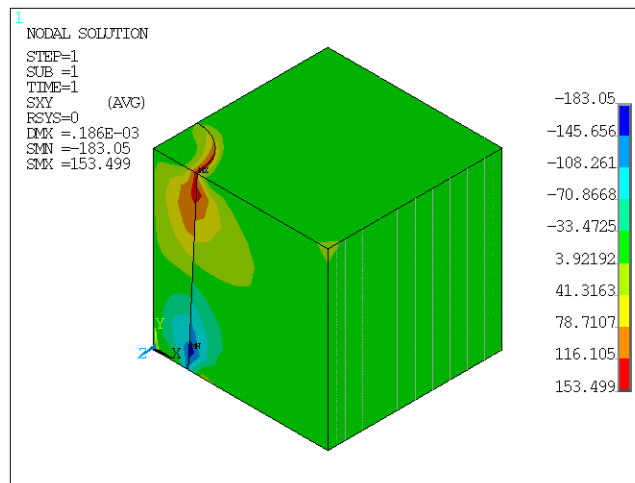
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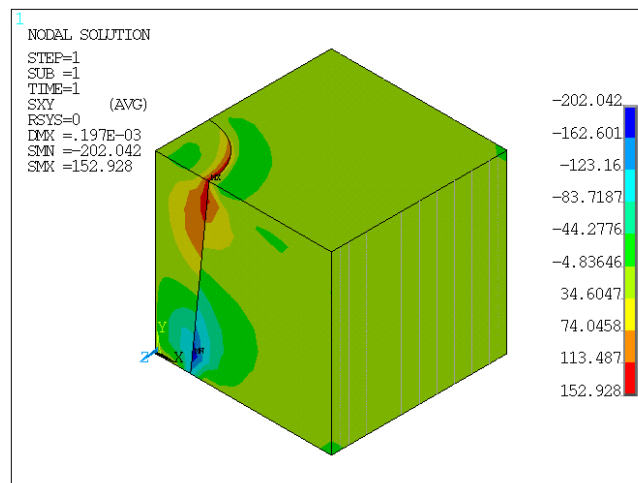
(c)

(d)

Figure 10: Comparison of the contour plots of the xy-shear stress after the cooling process. The models represent a quarter of a TSV unit cell in the 50 μm thickness isotropic silicon wafer. The TSV structures have a fixed 10 μm base radius and (a) 0°, (b) 3°, (c) 6°, and (d) 9° tapered profiles.
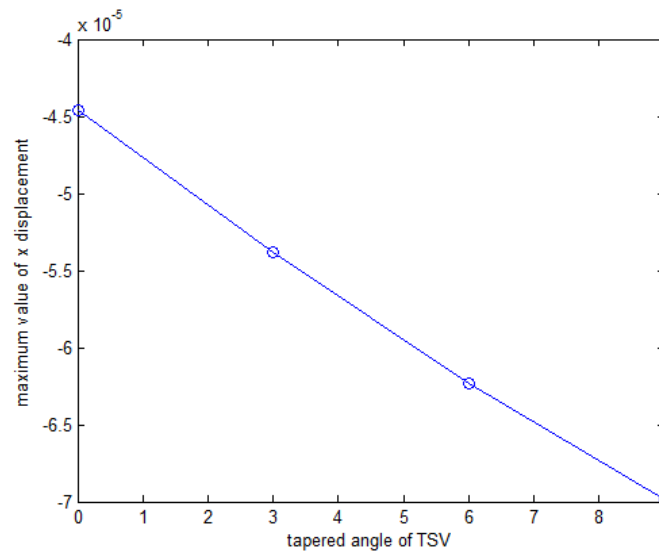
Figure 11 shows the maximum values of the xy-shear stress with respect to different taper angles. It indiacates that the maximum magnitudes of the positive and negetive xy-shear stresses are the same in the straight TSV model. It can also be seen that the maximum negetive σ_{xy} in silicon increases linearly with the taper angle, while the maximum positive σ_{xy} in copper stays relatively unchanged. This phenomenon suggests that the delamination concern may rise with the taper angle.
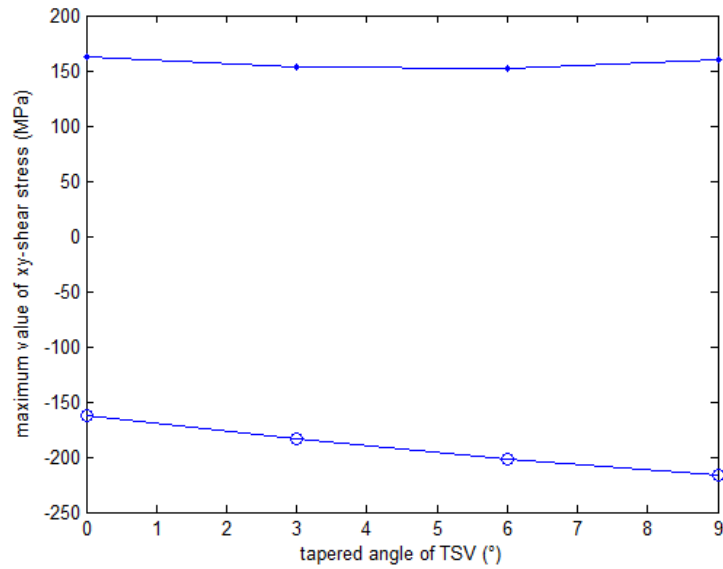
Figure 11: The maximum values of the xy-shear stress with respect to different angles of TSVs when the base radius of the TSV is fixed at 10 μm.

Figure 12 (a)-(d) show the equivalent plastic strains in the cases of 0°, 3°, 6°, and 9° TSV tapered profiles, respectively, after cooling. The plasticity in TSV is stronger at the wider end of the TSV. Figure 13 shows the maximum values of the equivalent plastic strain with respect to different angles of TSVs. The trend is not strictly monotonic increasing. However, in general, the maximum equivalent plastic strain increases with the taper angle when the angle is greater than 3°, as shown in Figure 13.
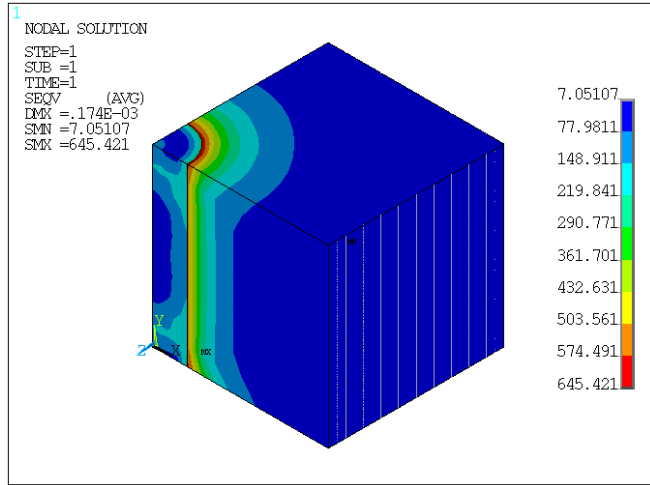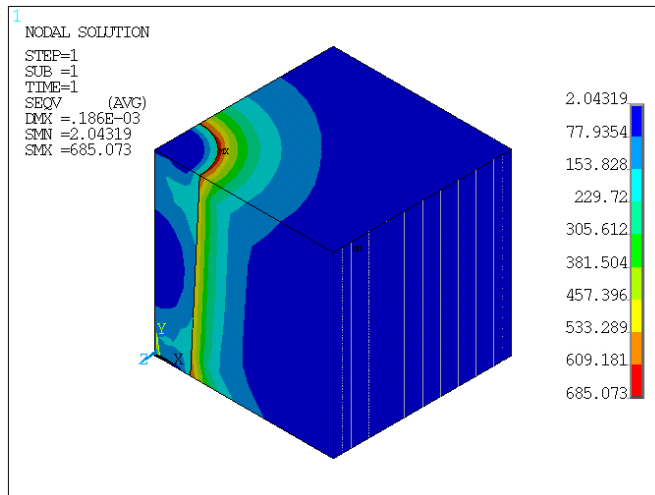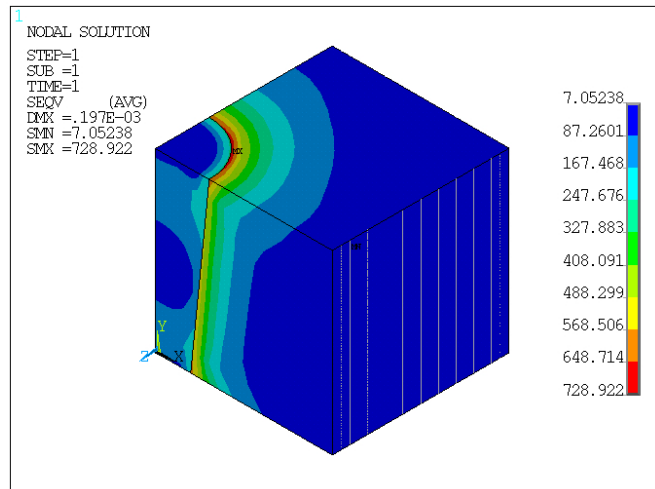
(a)

(b)

(c)

26
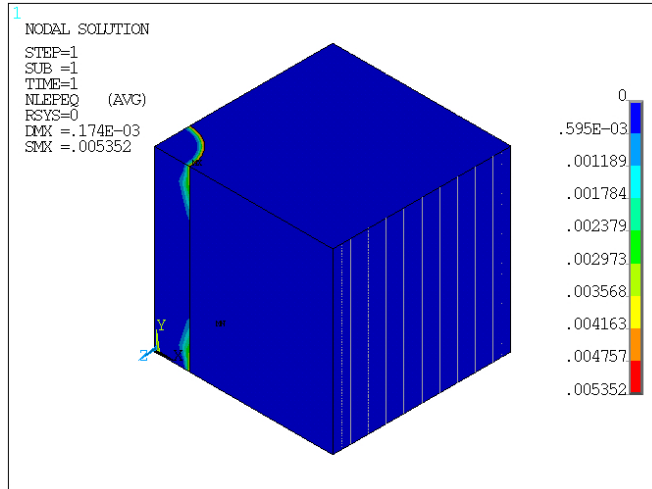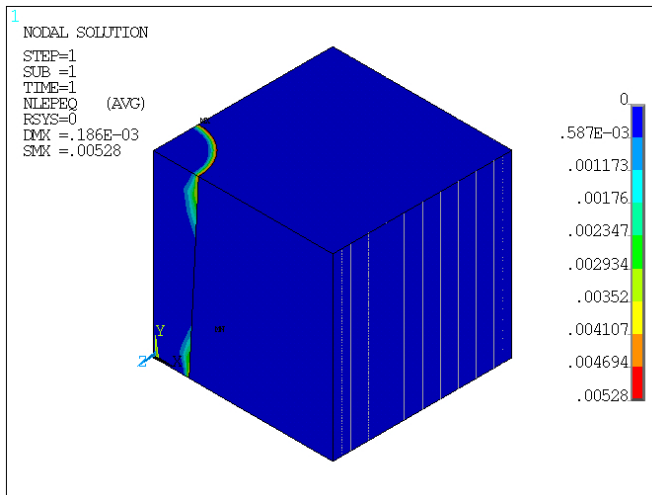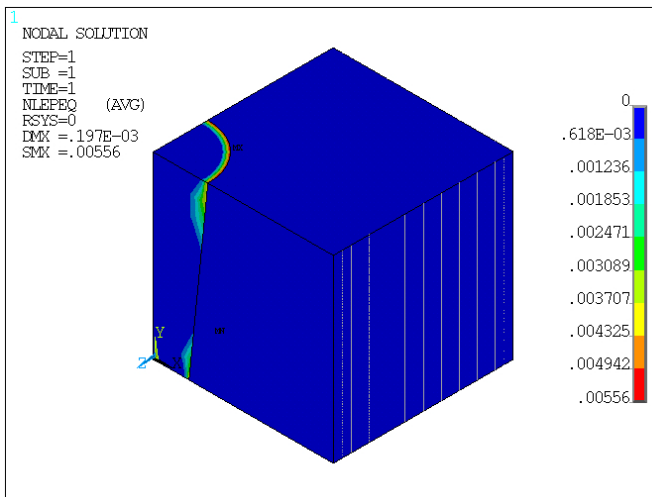
(d)

Figure 12: Comparison of the contour plots of the equivalent plastic strain after the cooling process. The models represent a quarter of a TSV unit cell in the 50 μm thickness isotropic silicon wafer. The TSV structures have a fixed 10 μm base radius and (a) 0°, (b) 3°, (c) 6°, and (d) 9° tapered profiles.
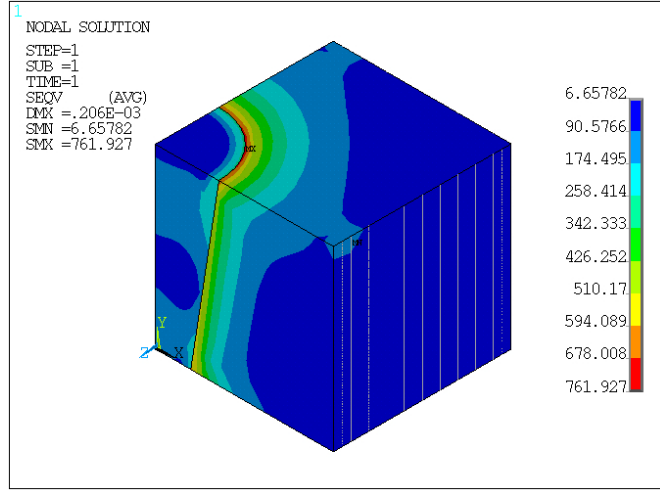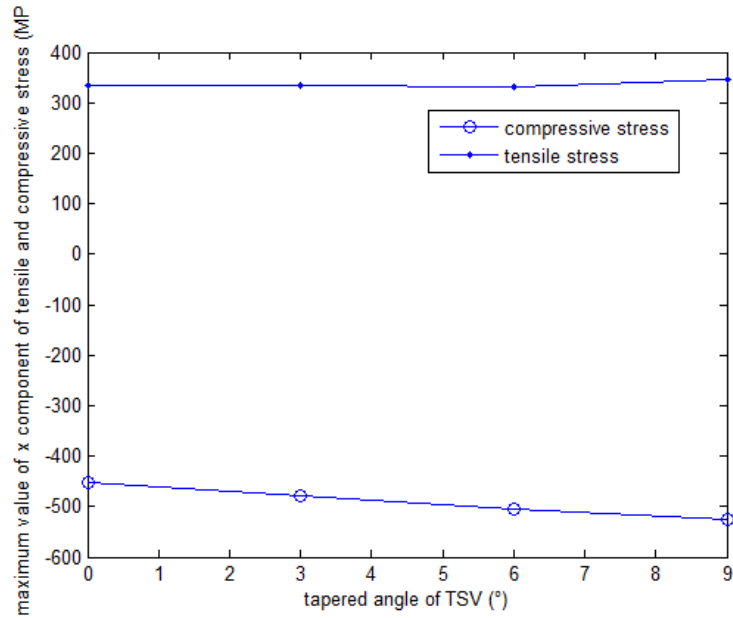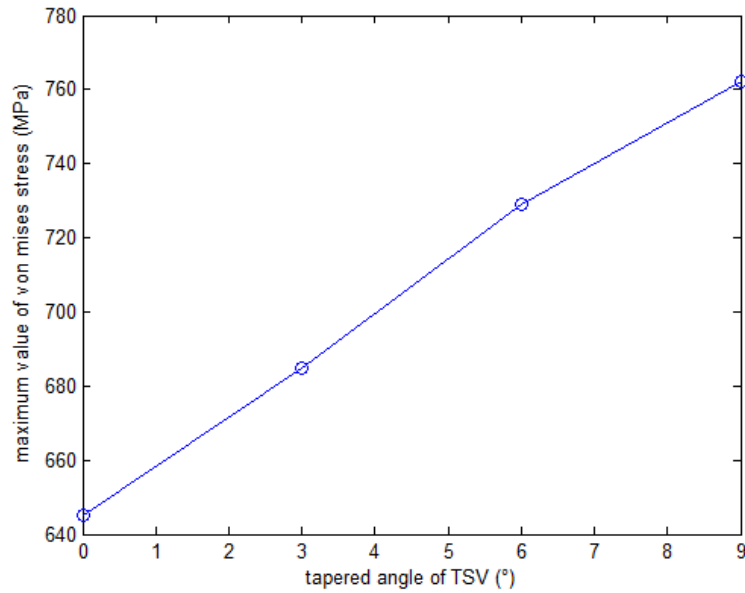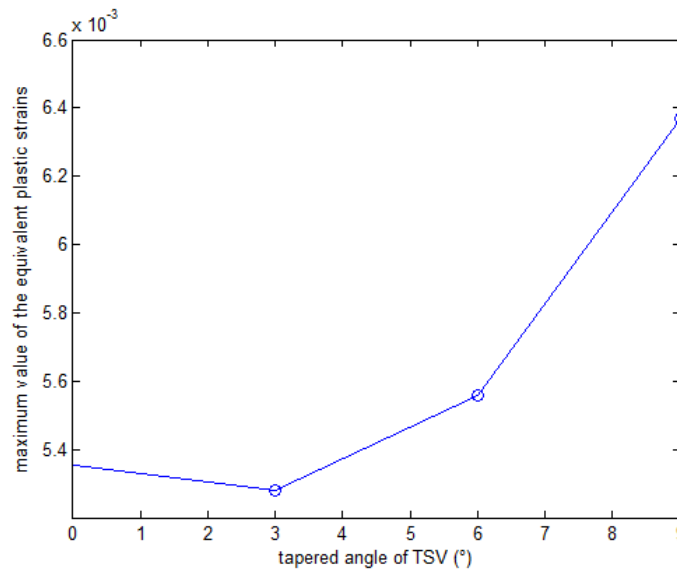

Figure 13: The maximum values of the equivalent plastic strain with respect to different angles of TSVs when the base radius of the TSV is fixed at 10 μm.

The x displacements of the specific nodes in the models shown above are extracted to calculate the curvatures, as shown in Figure 14. It is found that the curvature approximately increases linearly with the TSV sidewall inclining when the base radius of the TSV is fixed.
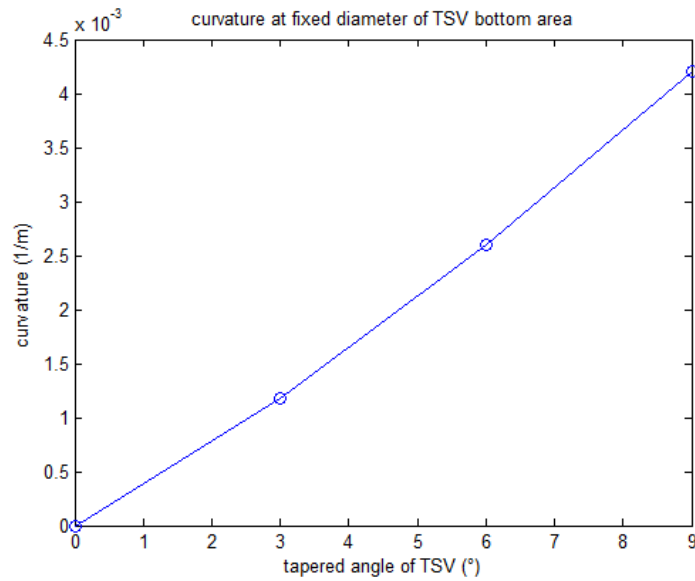
Figure 14: Wafer curvatures with respect to different angles of TSVs when the base radius of the TSV is fixed at 10 µm.

Attention is now focused on the variation of the TSV width, under a fixed taper angle.

Figure 15 shows the x displacement fields in the models with 5 µm, 10 µm, 15 µm, 20 µm, and 25 µm TSV base radii, respectively, and a fixed 3° taper angle.
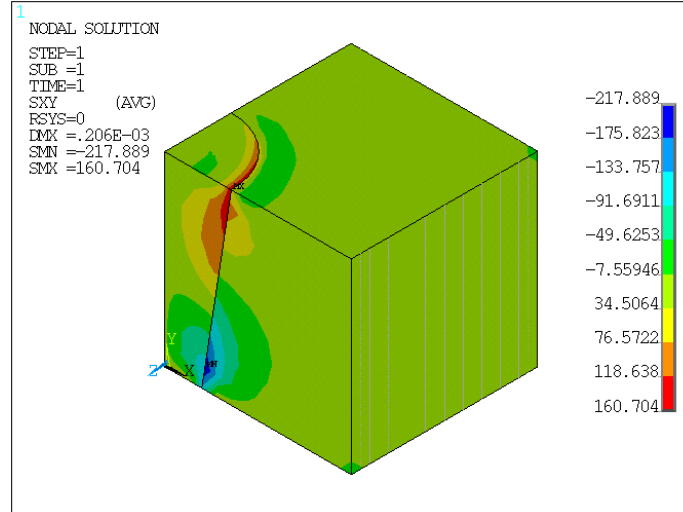
(a)

(b)

(c)

29
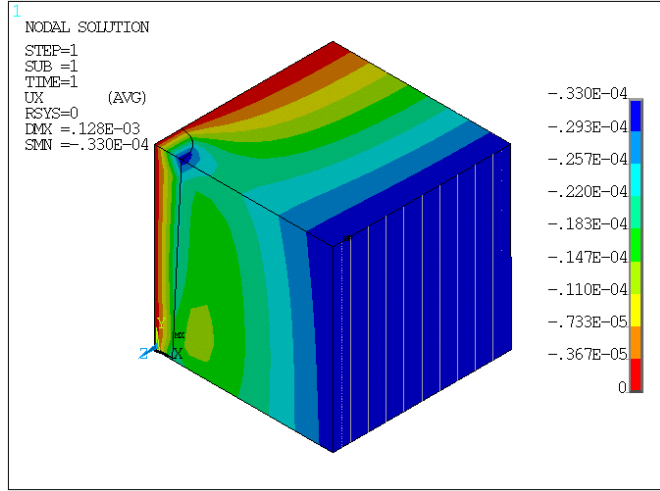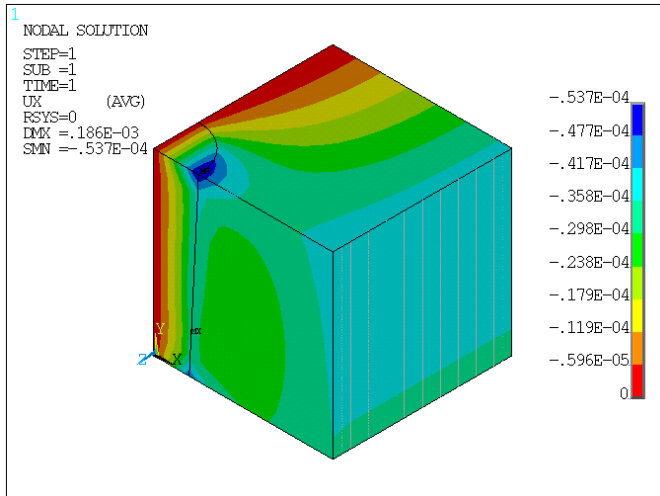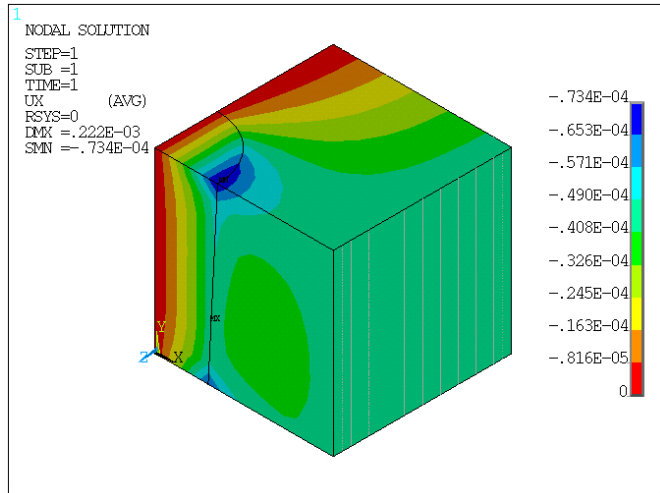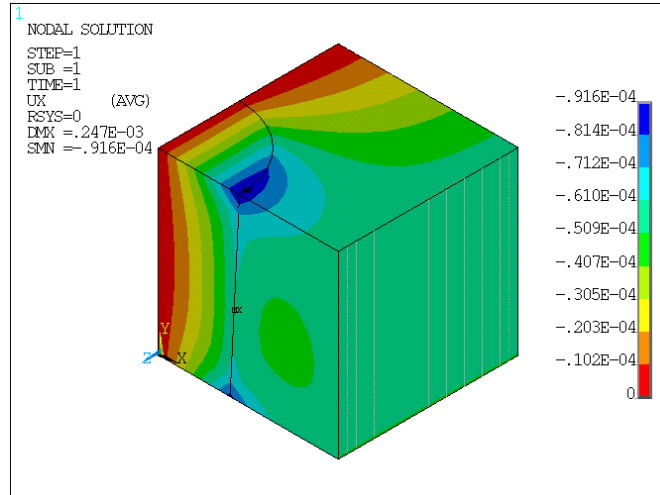
(d)
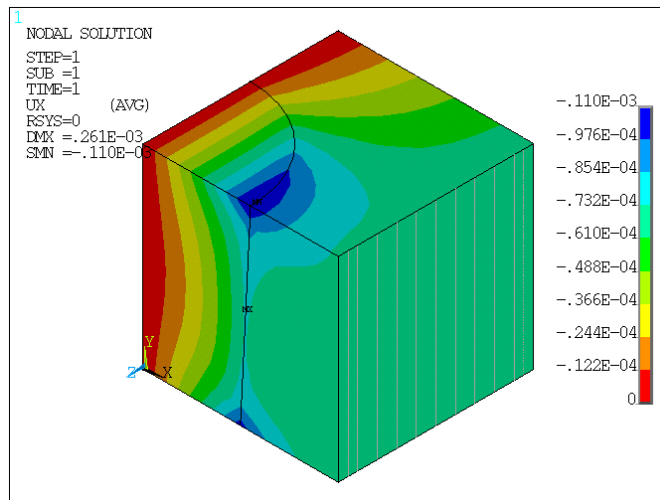
(e)

Figure 15: Comparison of the contour plots of the x displacement after the cooling process. The models represent a quarter of a TSV unit cell in the 50 μm thickness isotropic silicon wafer. The TSV structures have (a) 5 μm, (b) 10 μm, (c) 15 μm, (d) 20 μm, and (e) 25 μm base radii and a fixed 3° tapered profile.

Figure 16 shows the maximum values of the x displacement with respect to different base radii of the TSVs when the angle of tapered TSV is fixed at 3°. It demonstrates that the maximum value of the x displacement increases with the volume fraction of TSV in a linear manner, when the 3° angle of tapered TSV is fixed. The greatest negative x displacement

occurs at the top surface in the interface area, due to the large copper volume at the wider end. Therefore a greater curvature can be expected, which will be shown later in this section.
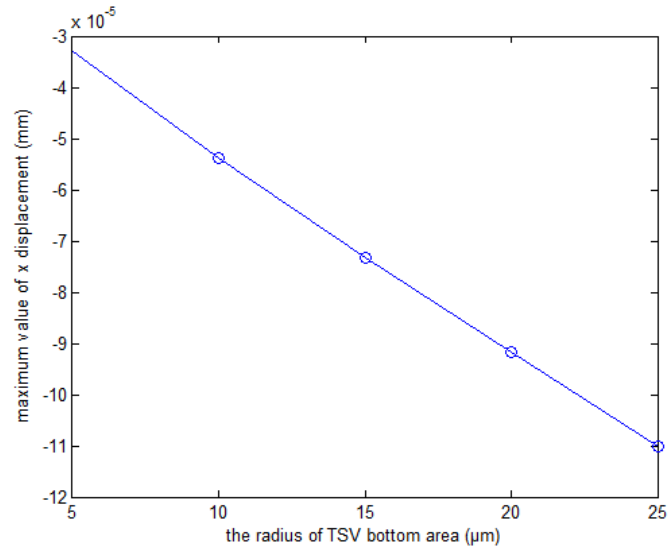
Figure 16: The maximum values of the x displacement with respect to different base radii of the TSVs when the angle of tapered TSV is fixed at 3°.

Figure 17 and Figure 18 show the x-component of stress and the von Mises stress fields in the models with 5 µm, 10 µm, 15 µm, 20 µm, and 25 µm TSV base radii and a fixed 3° taper angle, respectively. It is seen that the high tensile σ_{xx} (over 300 MPa) exists at the center of the TSV after cooling. Within silicon, the thermally induced stresses will reach high magnitudes and become concentrated near the top and bottom free surfaces around the interface. Figure 19 shows that the maximum value of the x-component of compressive stress stays relatively constant with the base radius of the TSV. Figure 20 illustrates that the maximum value of the von Mises stress generally is linearly enlarged with an increase in TSV volume fraction. Figure 21 shows that the curvature is proportional to the base radius of the TSV when the angle of tapered TSV is fixed at 3°.
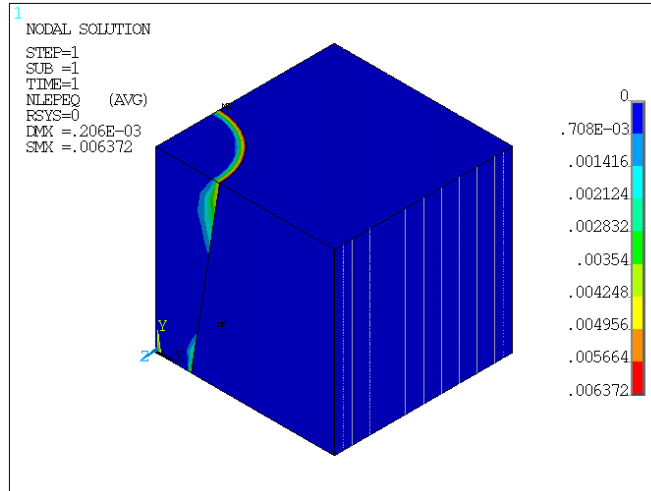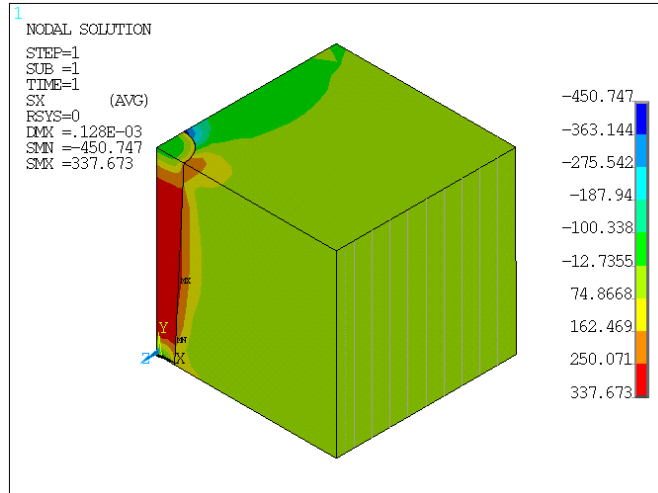
(a)
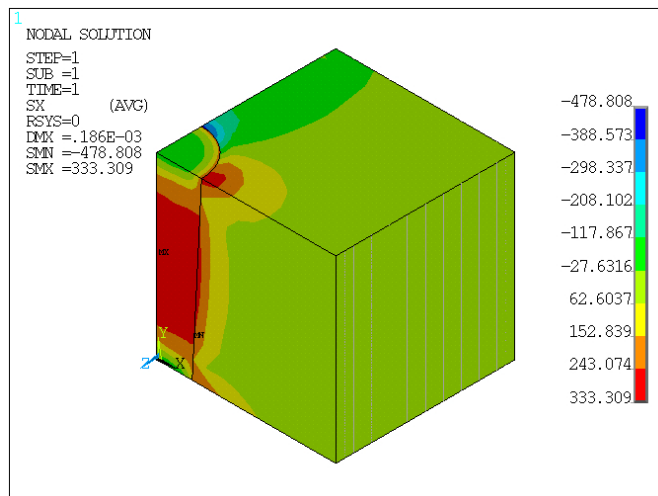
(b)
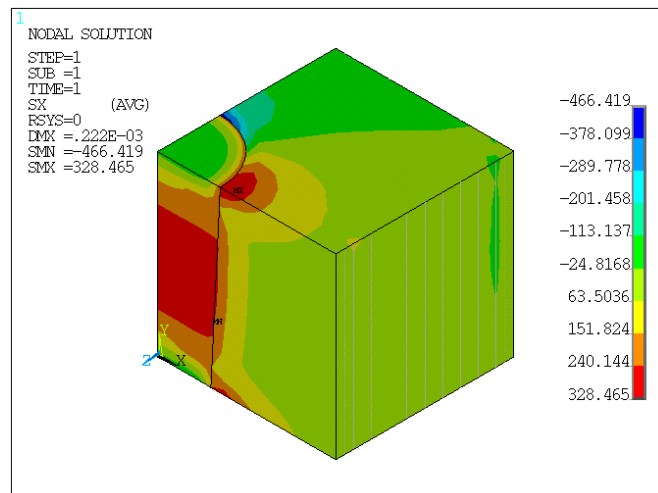
(c)
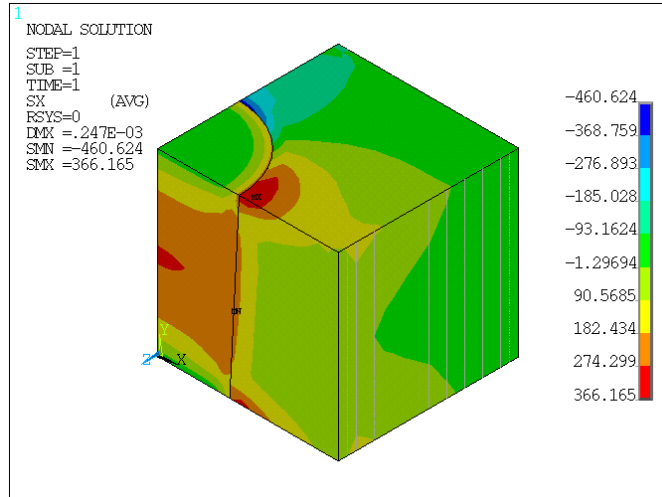
(d)
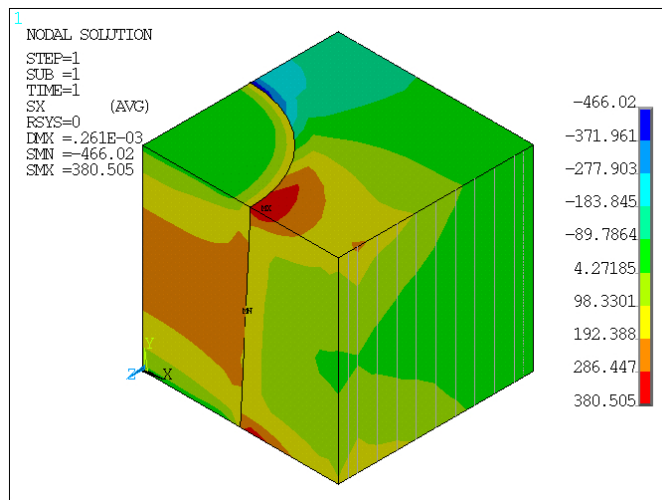
(e)

Figure 17: Comparison of the contour plots of the x-component of stress after the cooling process. The models represent a quarter of a TSV unit cell in the 50 µm thickness isotropic silicon wafer. The TSV structures have (a) 5 µm, (b) 10 µm, (c) 15 µm, (d) 20 µm, and (e) 25 µm base radii and a fixed 3° tapered profile.
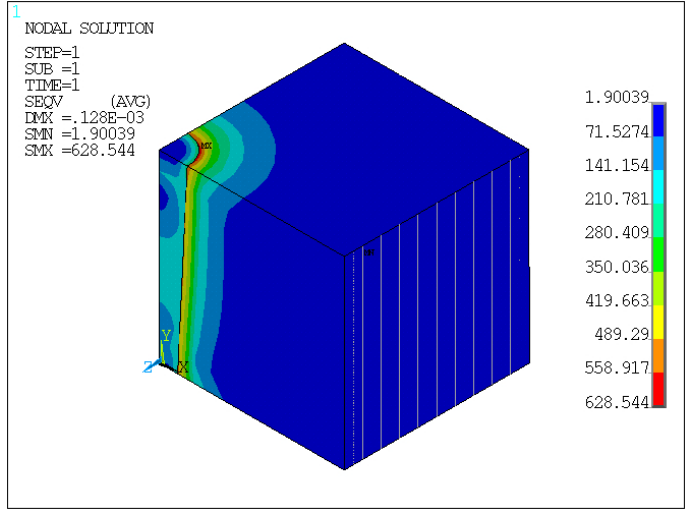
(a)
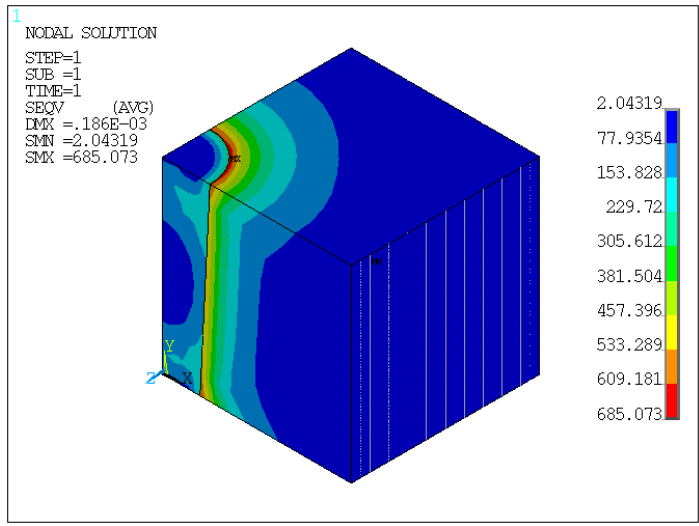
(b)
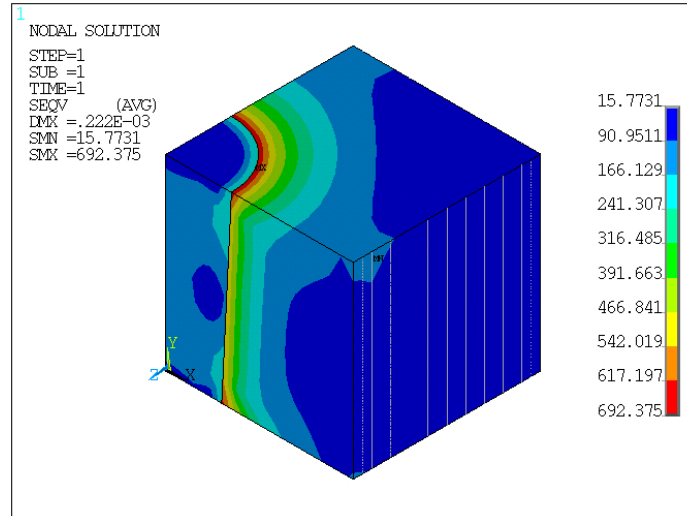
(c)
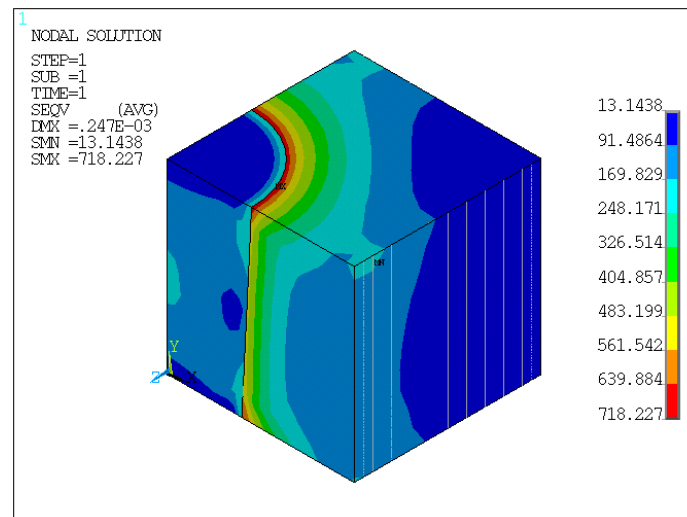
(d)
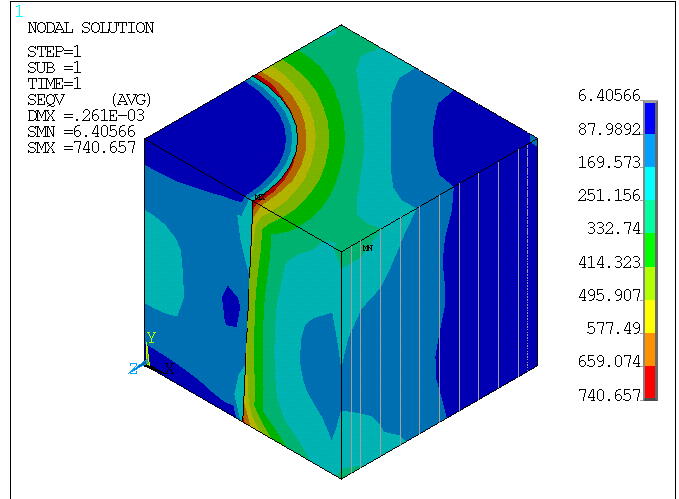
(e)

Figure 18: Comparison of the contour plots of the von Mises stress after the cooling process. The models represent a quarter of a TSV unit cell in the 50 μm thickness isotropic silicon wafer. The TSV structures have (a) 5 μm, (b) 10 μm, (c) 15 μm, (d) 20 μm, and (e) 25 μm base radii and a fixed 3° tapered profile.
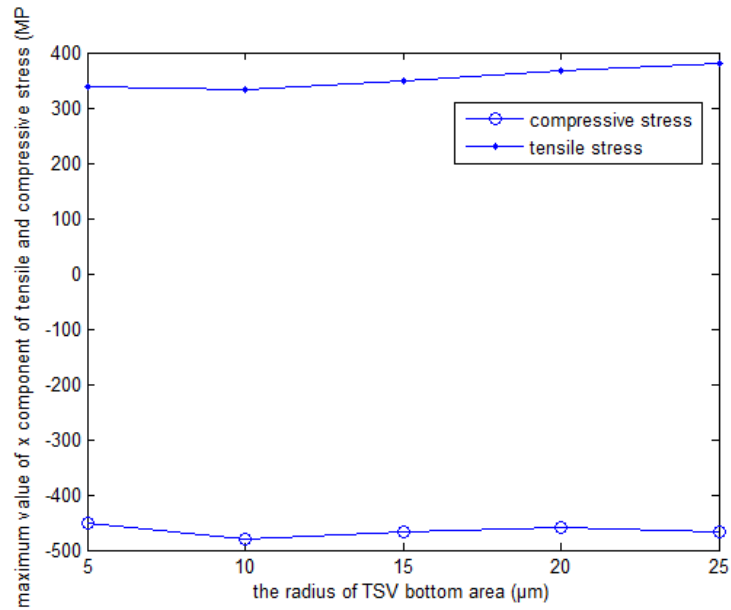
Figure 19: The maximum values of the x-component of stress with respect to different base radii of the TSVs when the angle of tapered TSV is fixed at 3°.
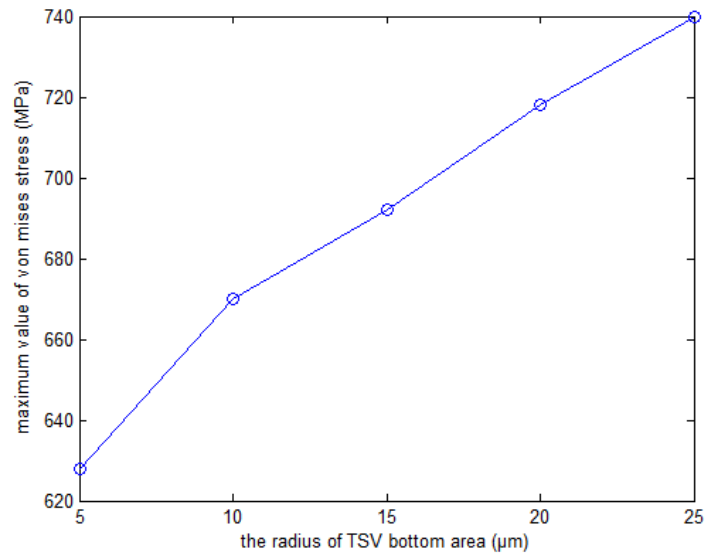
Figure 20: The maximum values of the von Mises stress with respect to different base radii of the TSVs when the angle of tapered TSV is fixed at 3°.
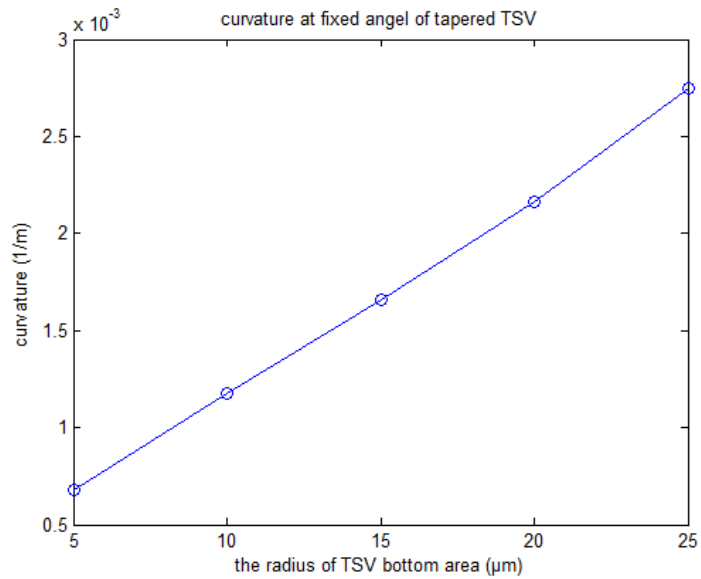
Figure 21: Wafer curvatures with respect to different base radii of the TSVs when the angle of tapered TSV is fixed at 3°.

Finally, the 3D curvature surface plot is generated with respect to two variables, the angle and the base diameter of the tapered TSV, as shown in Figure 22. It can be seen that the

curvature is largely proportional to the value of one variable while the value of the other is fixed. Therefore, the curvature value for any combination of the TSV size, of which the base radius ranges from 3 µm to 25 µm, and the taper angle, which ranges from 0° to 9°, may be easily estimated.
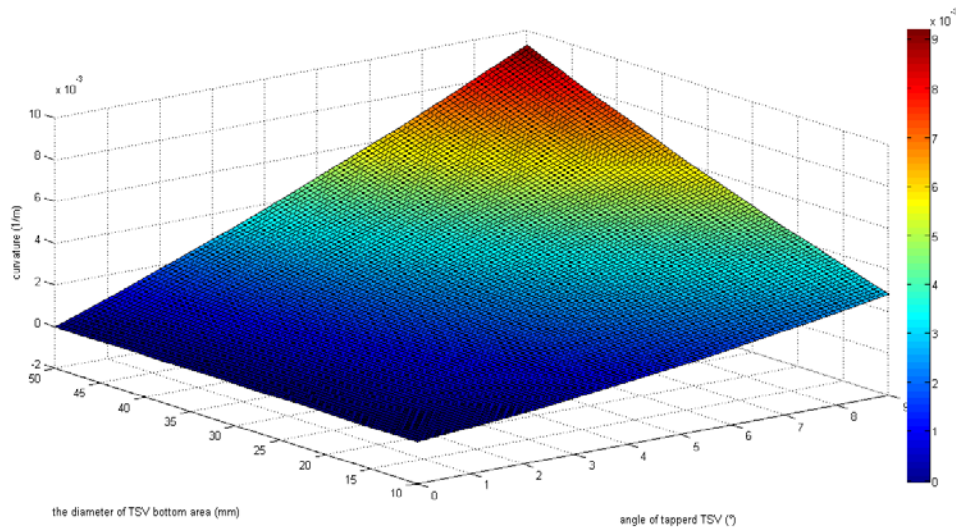
Figure 22: 3D curvature surface plot of the 50 µm thickness isotropic tapered TSV wafers with respect to different angles and base diameters of the TSVs.

4.2 Curvature Evolution as a Function of Temperature Change

Depending on the processing history, such as the wafer annealing temperature and bonding temperature, the TSV structure may be subject to various temperature changes. Here, the evolution of wafer curvature is presented as a function of temperature change for different combinations of TSV base radii and taper angles.

Figure 23 and Figure 24 show the wafer curvatures with respect to the temperature change. It is observed that the evolution of curvature with respect to temperature change generally follows a linear relationship. It is thus straightforward to estimate the wafer curvature if the temperature change involved in the processing is not 230 ℃. In fact, the same type of linear

relationship was found to hold true when the temperature change extended to about 400 ℃. In experiments, the precision wafer curvature technique was used to measure the curvature change during thermal cycling [30]-[33]. The values of the curvature obtained from the present simulation results fall in the general range of the experimental data gained from the precision wafer curvature technique, even though the curvature technique was used to detect the blind vias causing wafer warpage [30]. This demonstrates that the TSV tapered geometry effect is a significant source of wafer bending.
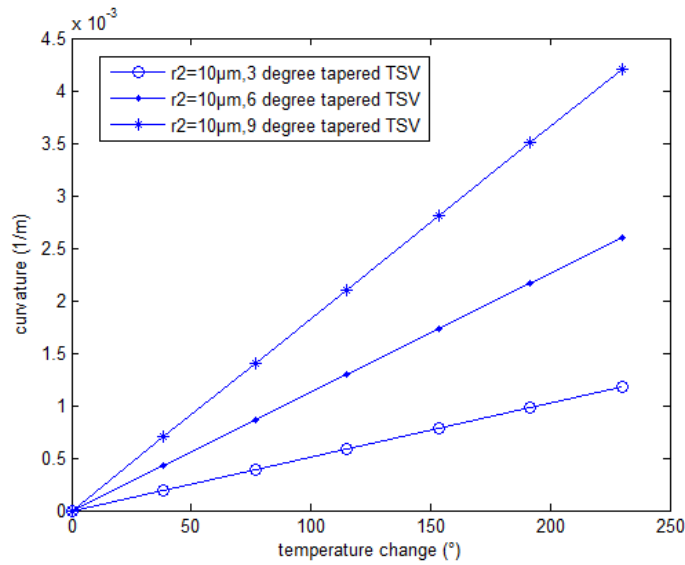
Figure 23: The curvature evolution during temperature change. The TSV structures have a fixed 10 μm base radius and 3°, 6°, and 9° tapered profiles. The TSVs are in the 50 μm thickness isotropic silicon wafer.
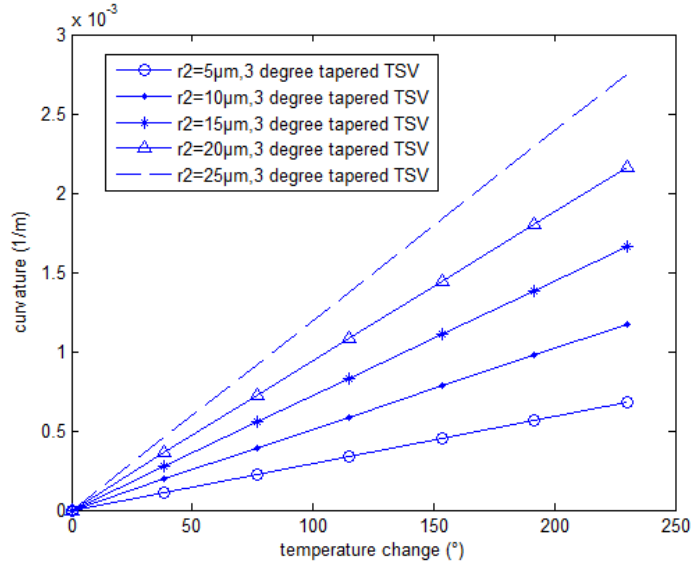
Figure 24: The curvature evolution during temperature change. The TSV structures have a fixed 3° tapered profile and different base radii. The TSVs are in the 50 μm thickness isotropic silicon wafer.

4.3 Wafer Warpage under Pure Mechanical Bending

For gaining insight into the stress fields, pure mechanical bending was also investigated. In the case of thermal-stress-induced warpage of the 50 µm thickness isotropic silicon wafer, which has 10 µm base radius and 3° profile tapered TSVs, the curvature was found to be 6.808×10^{-4}/m and the rotations of the planes x = p/2 and z = -p/2 in each quarter unit cell were 3.4×10^{-5} rad. Here, the same extent of curvature is simulated using pure mechanical bending. First, two single points, denoted as A and B, are set up outside of the model. The rigid beam element is used to constrain all of the nodes in the boundary plane x = p/2 with the single point A and all of the nodes in z = -p/2 with the point B. A large rotation or a moment can be prescribed by using the rigid-beam element. A rotation of 3.4×10^{-5} rad with respect to z axis is imposed on the point A, therefore all of the nodes in the boundary plane x = p/2 are subject to the same rotation at the same time. The same value rotation with respect to x axis is imposed on the nodes in z = -p/2 plane as well.

40

Figure 25 shows the contour plots of the x displacement, the x-component of stress, the xy-shear stress, and the von Mises stress of the same configuration model as in Section 4.1. The maximum value of the x-component of stress is 38.3 MPa. The maximum value of the von Mises stress is 39.6 MPa. The stress values are thus much smaller than those caused by cooling process. This indicates that, under the same overall deformation, the thermally induced stress in the TSV structure plays a dominant role in affecting the structural integrity.

(a)

(b)

(c)

NODAL SOLUTION
STEP=1
SUB =1
TIME=1
SEQV   (AVG)
DMX =.238E-05
SMN =.001047
SMX =39.590

.001047
4.39986
8.79868
13.1975
17.5963
21.9951
26.3939
30.7928
35.1916
39.5904
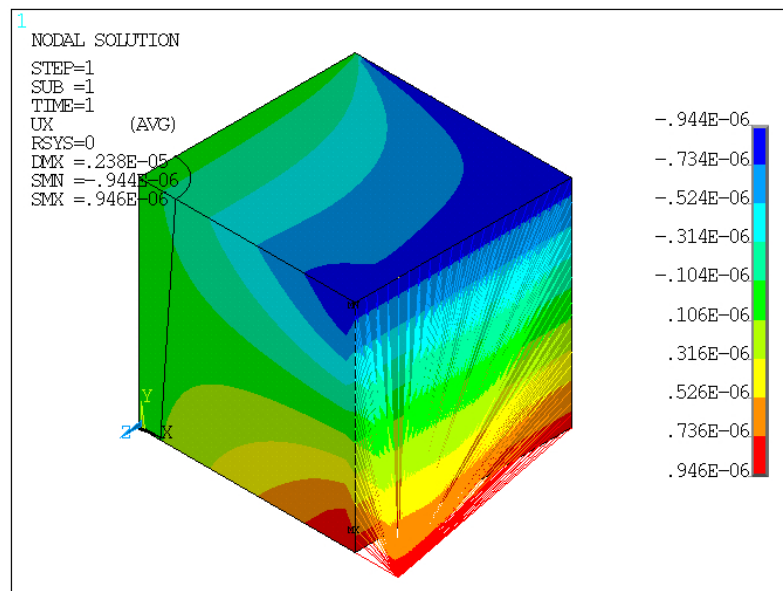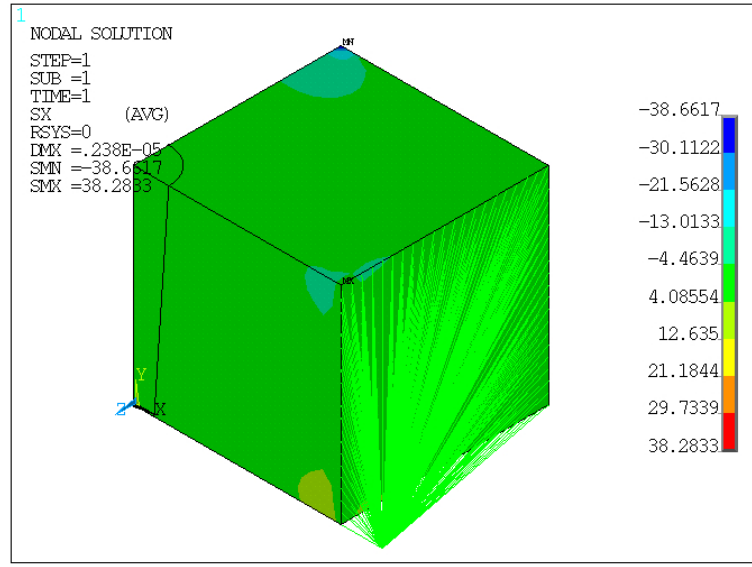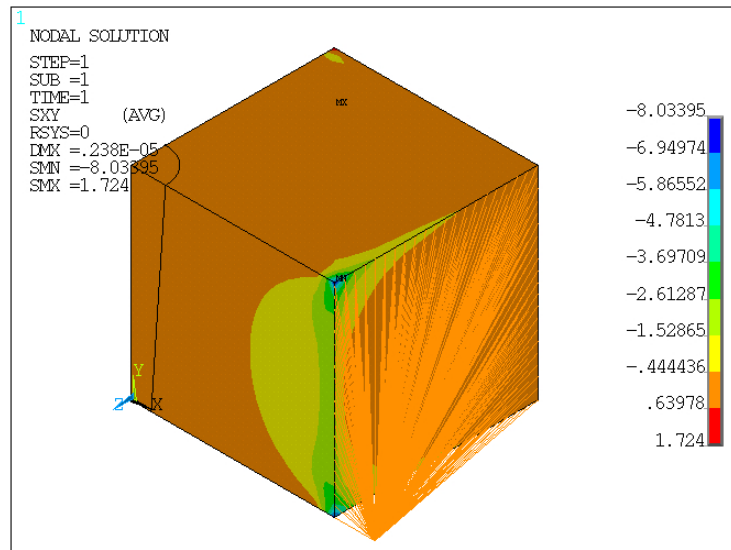
(d)

Figure 25: Contour plots of (a) the x displacement, (b) the x-component of stress, (c) the xy-shear stress, and (d) the von Mises stress. The model represents a quarter of a TSV unit cell in the 50 µm thickness isotropic silicon wafer. The TSV structure has a 5 µm base radius and a 3° tapered profile. The model is subject to pure mechanical bending.

4.4 Effect of Intermediate Layers

Next we consider the TSV structure with a dielectric silicon dioxide layer and a barrier layer, in order to mimic the conditions in real life. The silicon dioxide layer and tantalum (Ta) diffusion-barrier layer between copper TSV and its surrounding silicon are set as 1 µm-thick and 0.1-µm thick, respectively, based on the typical dimensions used in experiments.

One major issue about including the ultra-thin intermediate layers is the need to mesh every part of the TSV structure extremely well so as to resolve the deformation characteristics in sufficient detail. In each of these models, more than 250,000 nodes have been generated.

Simulating such highly meshed models dramatically increases the CPU time and may pose numerical convergence problems.

Figure 26 and Figure 27 show the contour plots of the x displacement, the x-component of stress, the xy-shear stress, the von Mises stress, and the equivalent plastic strain after the cooling process. The models in both Figures have inter-layers. The TSV structure in Figure 26 has a 10 µm base radius and a 6° tapered profile, while in Figure 27, it includes a 25 µm base radius and a 9° tapered profile. It can be noticed that the contour plots of these models have similar patterns as the ones of the same configuration models which are without the intermediate layers, except that the maximum magnitude of each stress component is much higher. The maximum value of the x-component of stress is 100 MPa higher, and the maximum value of the von Mises stress is 200 MPa higher in the model with the intermediate layers, as shown in Figure 26. The von Mises stress even exceeds 1,117 MPa, and the equivalent plastic strain is generated in the central part of the wider TSV, as shown in Figure 27 (d). Because the intermediate layers are extremely thin, large thermal stresses are concentrated at the interface between these ultra-thin layers. Debonding is thus a real concern, which can cause crosstalk, electromigration damage, and current leakage.
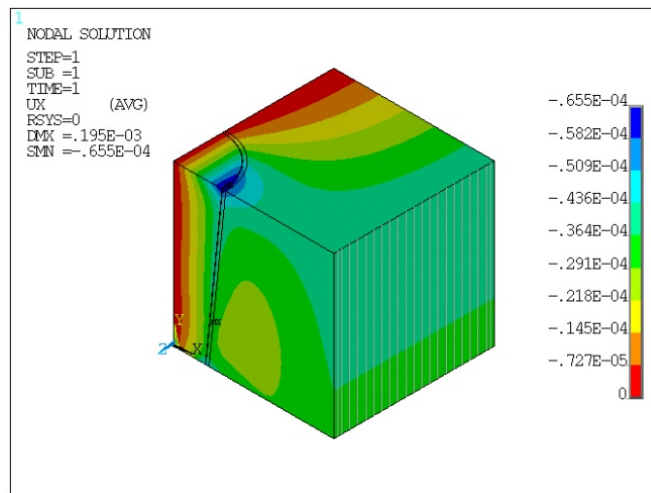
(a)
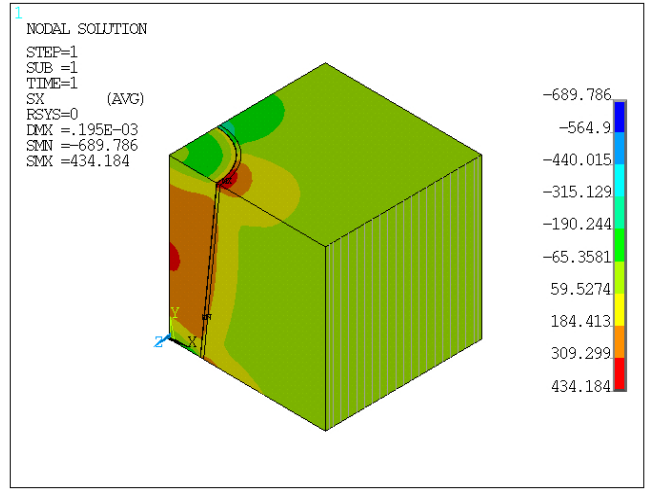
(b)
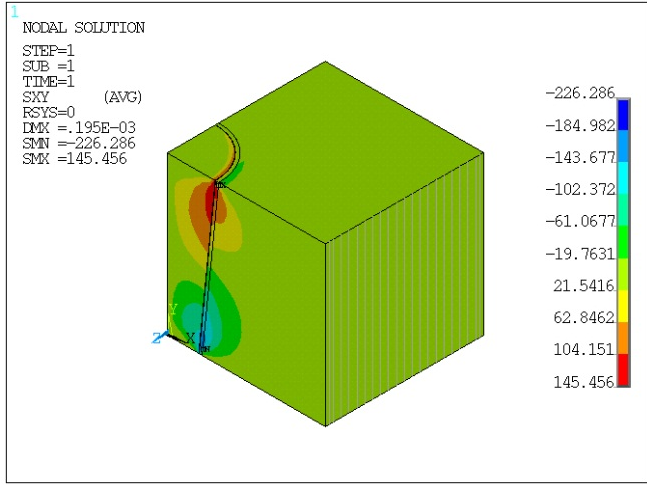
(c)
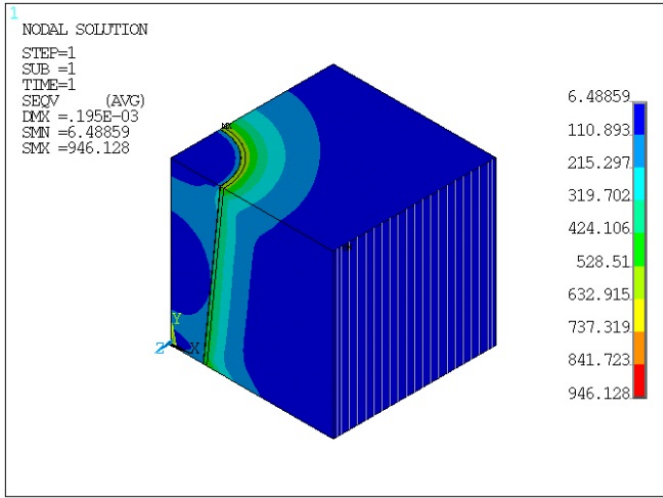
(d)
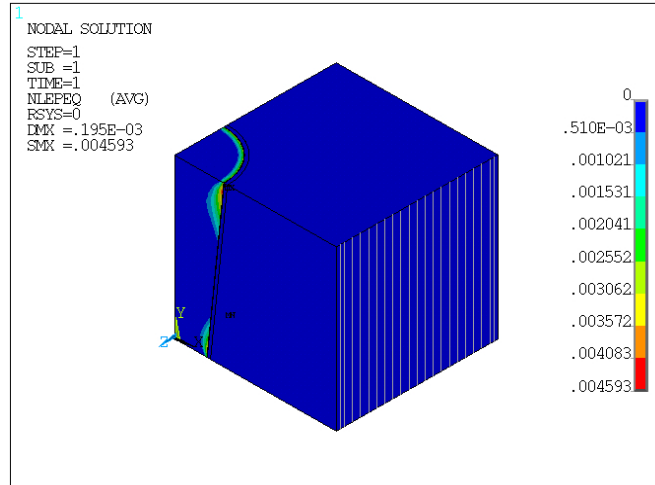
(e)

Figure 26: Contour plots of (a) the x displacement, (b) the x-component of stress, (c) the xy-shear stress, (d) the von Mises stress, and (e) the equivalent plastic strain after cooling. The model represents a quarter of a TSV unit cell in the 50 µm thickness isotropic silicon wafer. The model has a silicon dioxide layer and a Ta barrier layer. The TSV structure has a 10 µm base radius and a 6° tapered profile.
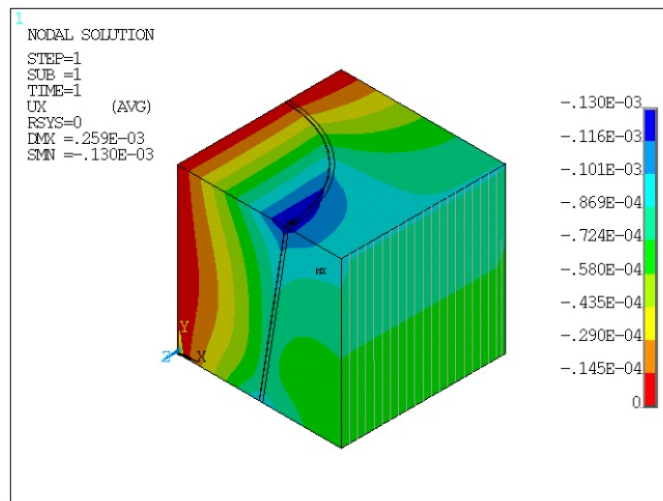
(a)
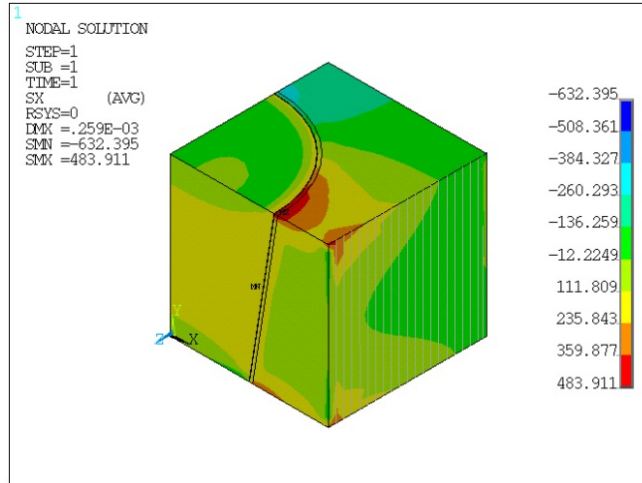
(b)
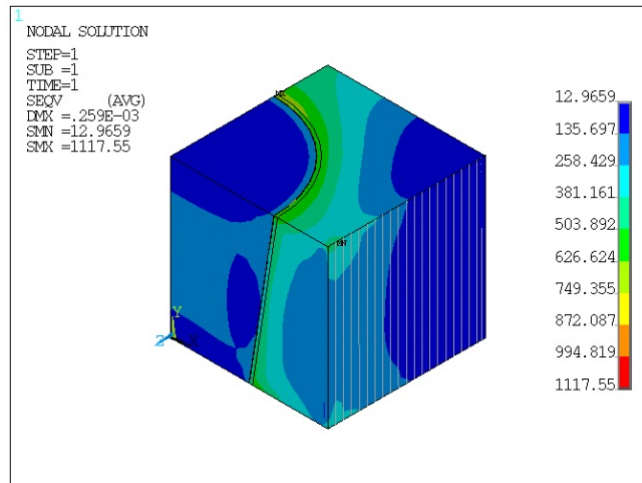
(c)
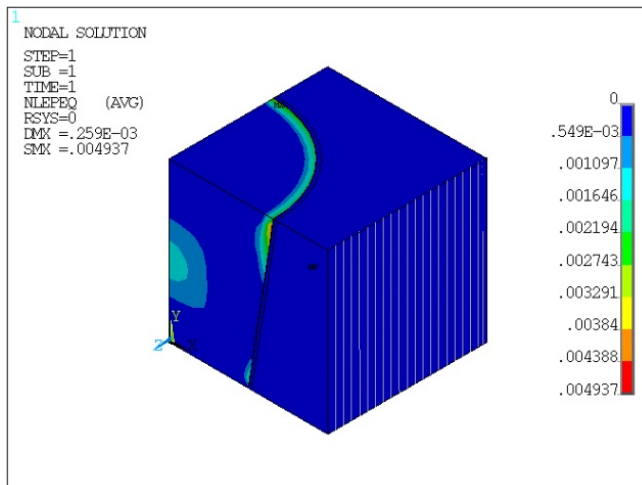
(d)

Figure 27: Contour plots of (a) the x displacement, (b) the x-component of stress, (c) the von Mises stress, and (d) the equivalent plastic strain after cooling. The model represents a quarter of a TSV unit cell in the 50 μm thickness isotropic silicon wafer. The model has a silicon dioxide layer and a Ta barrier layer. The TSV structure has a 25 μm base radius and a 9° tapered profile.

Figure 28 and Figure 29 show the contour plots of the individual silicon dioxide layer and barrier layer, respectively, in the model with a 10 μm base radius and a 6° taper angle TSV. It can be seen that the x-component of stress, and the von Mises stress is higher than the ones in the model without inter-layers.
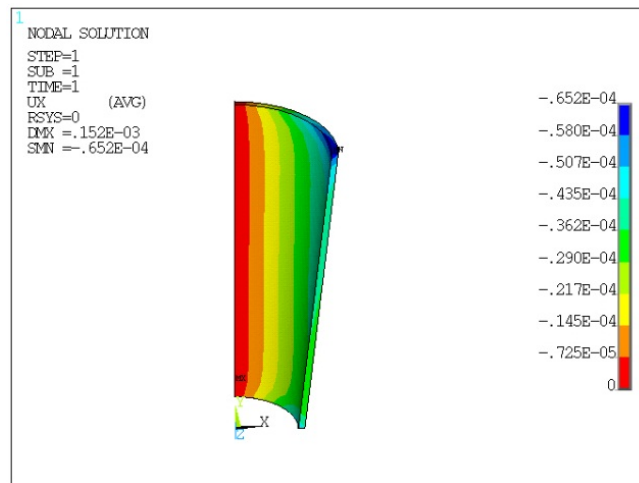
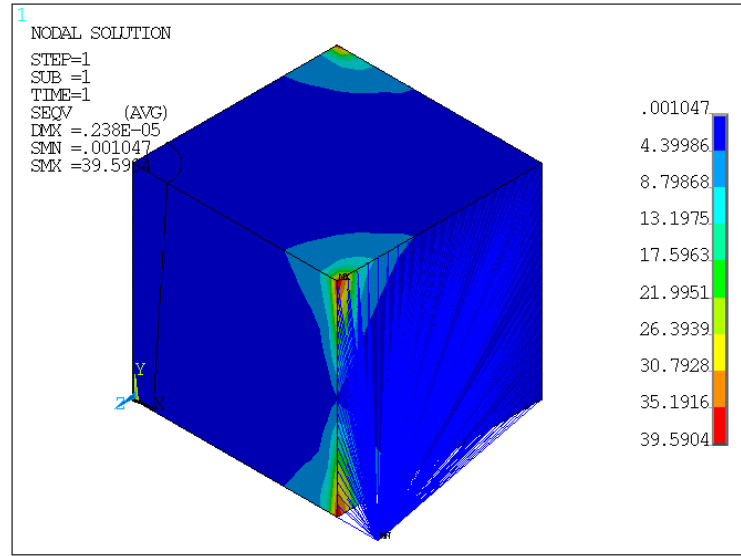(a)
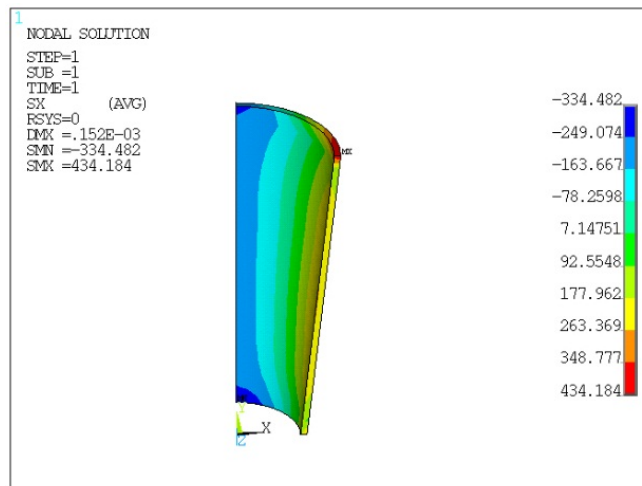
(b)
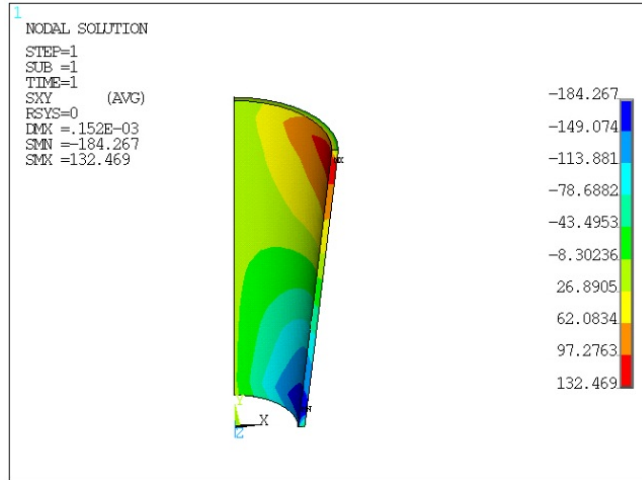
(c)
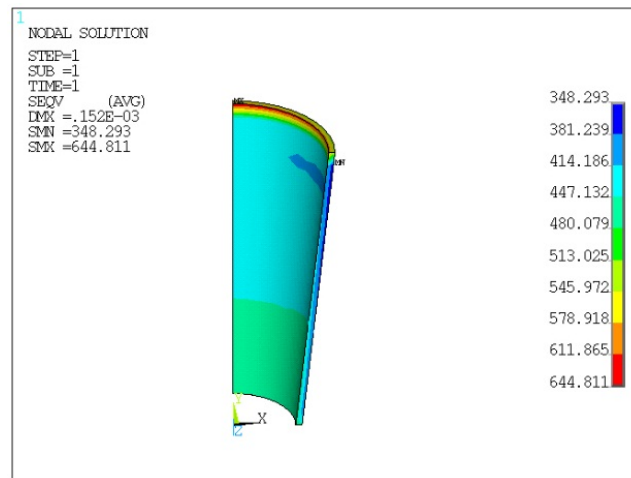
(d)

Figure 28: Contour plots of (a) the x displacement, (b) the x-component of stress, (c) the xy-shear stress, and (d) the von Mises stress in the silicon dioxide layer after cooling. The model represents a quarter of silicon dioxide layer in a TSV unit cell model. The model is in the 50 μm thickness isotropic silicon wafer and has a silicon dioxide layer and a Ta barrier layer. The TSV structure has a 10 μm base radius and a 6° tapered profile.

(a)

(b)

(c)

(d)

Figure 29: Contour plots of (a) the x displacement, (b) the x-component of stress, (c) the xy-shear stress, and (d) the von Mises stress in the barrier layer after cooling. The model represents a quarter of barrier layer in a TSV unit cell model. The model is in the 50 μm thickness isotropic silicon wafer and has a silicon dioxide layer and a Ta barrier layer. The TSV structure has a 10 μm base radius and a 6° tapered profile.

Figure 30 shows the 3D curvature surface plot of the models with the inter-layers with respect to the angle and the base diameter of the tapered TSV. Even though there are high thermal stresses in intermediate layers, the volume occupied by these layers is relatively small. The 3D curvature surface plot of the models with intermediate layers indicates that the wafer curvature is generally the same, except slightly lower, compared to the one of the models without layers. Because this thesis mainly focuses on the wafer warpage under thermal loading, from this point on we ignore the details of the intermediate layers between the TSV and silicon in order to enhance the computational efficiency.
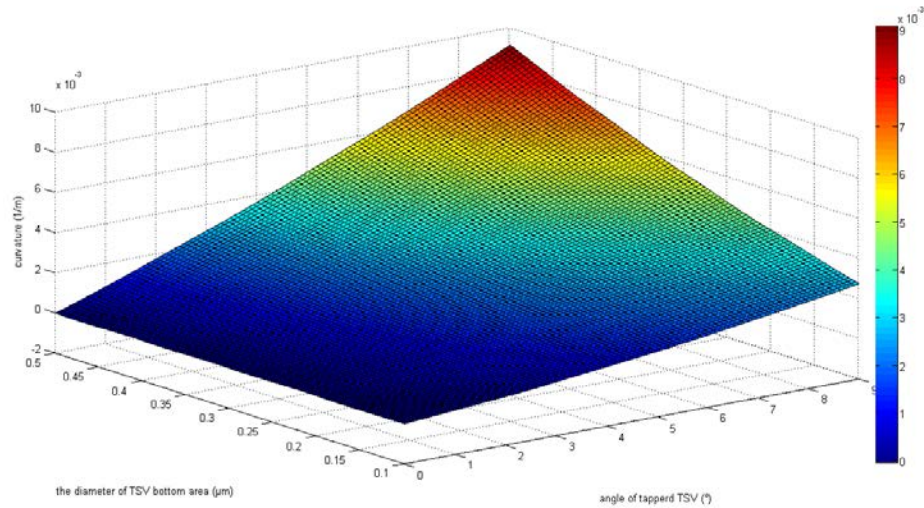
Figure 30: 3D curvature surface plot with respect to different angles and base diameters of TSVs. The TSVs have a silicon dioxide layer and a Ta barrier layer, and are in 50 µm thickness isotropic silicon wafers

4.5 Effect of Anisotropic Silicon

The thermally induced wafer warpage had been characterized above. The silicon wafer was assumed to have isotropic elastic material properties. However, in reality, the single-crystal silicon wafer is anisotropic. The effect of silicon anisotropy is now examined. The x, y, and z directions of the anisotropic model are taken to be along the crystallographic [100], [001], and [010] directions, respectively. The FEA models are built with the following silicon stiffness matrix.

$$
C_{(001)} = \begin{bmatrix}
166.2 & 64.4 & 64.4 & 0 & 0 & 0 \\
64.4 & 166.2 & 64.4 & 0 & 0 & 0 \\
64.4 & 64.4 & 166.2 & 0 & 0 & 0 \\
0 & 0 & 0 & 79.8 & 0 & 0 \\
0 & 0 & 0 & 0 & 79.8 & 0 \\
0 & 0 & 0 & 0 & 0 & 79.8
\end{bmatrix} \text{GPa.}
$$

The anisotropic models have the same geometry and boundary conditions as the ones in the section 4.1.

Figure 31 shows the contour plots of the x displacement, the x-component of stress, the xy-shear stress, the von Mises stress, and the equivalent plastic strain of the anisotropic model after the cooling process. The stress concentration is more severe at the interfaces near the top and bottom free surface in the anisotropic model. In the isotropic model, the von Mises stress contour plot exhibits axisymmetry around the TSV (e.g. Figure 7). While in the anisotropic model, a fourfold symmetry can be seen in Figure 31 (d), due to the cubic symmetry of the silicon. This demonstrates that the von Mises stress in the anisotropic model is highly dependent on the orientation of the silicon.

(a)

(b)

(c)

(d)

54

NODAL SOLUTION
STEP=1
SUB =1
TIME=1
NLEPEQ   (AVG)
RSYS=0
DMX =.194E-03
SMX =.006561

0
.729E-03
.001458
.002187
.002916
.003645
.004374
.005103
.005832
.006561
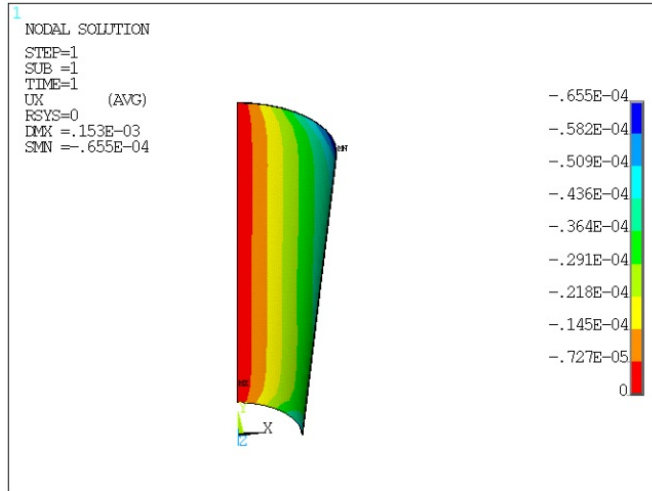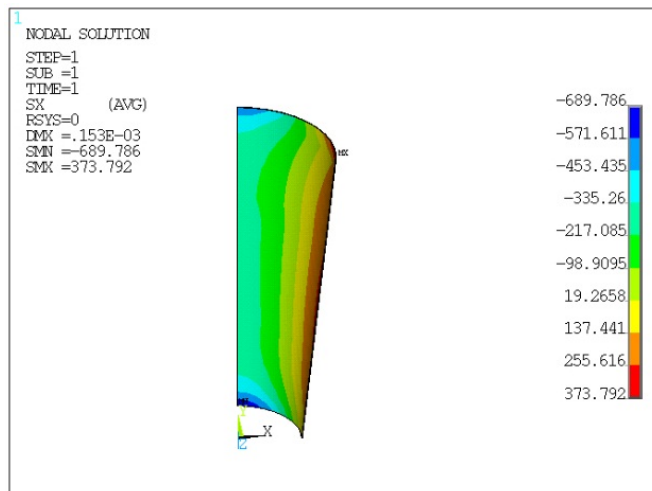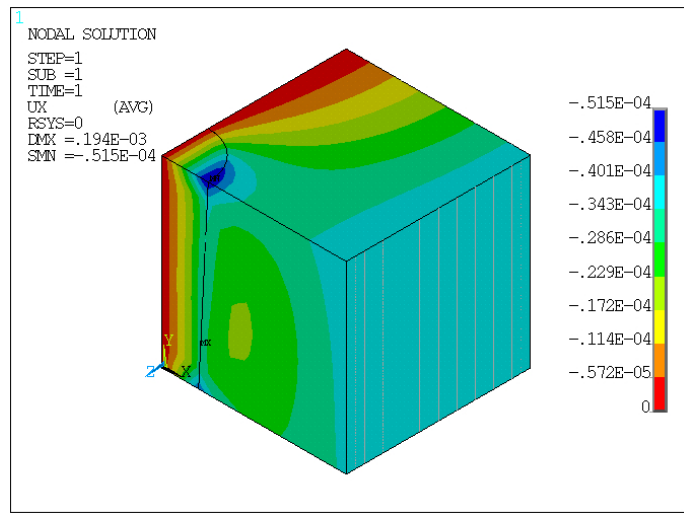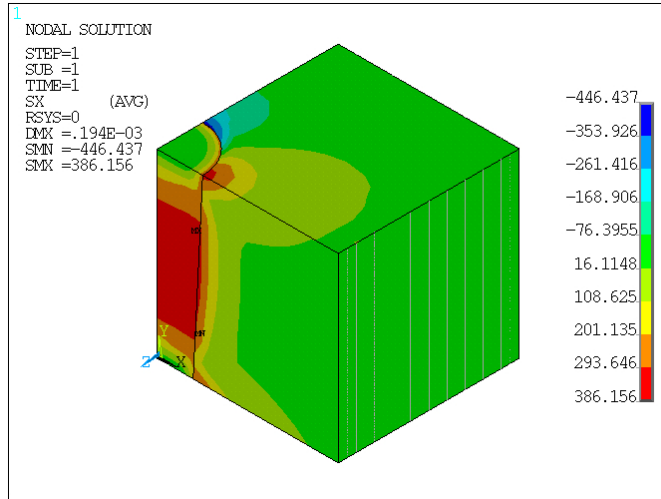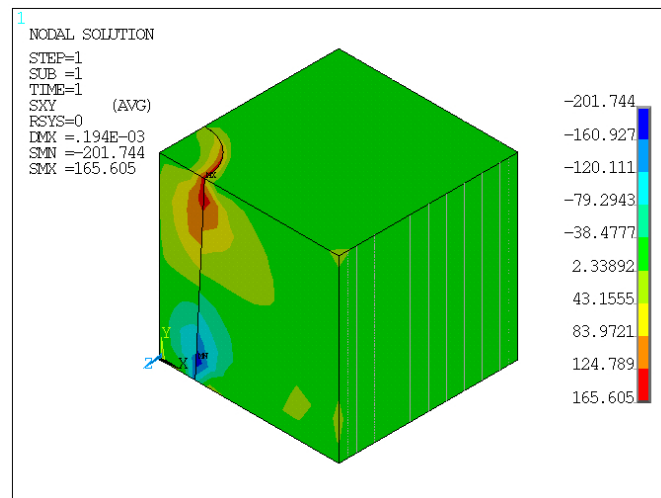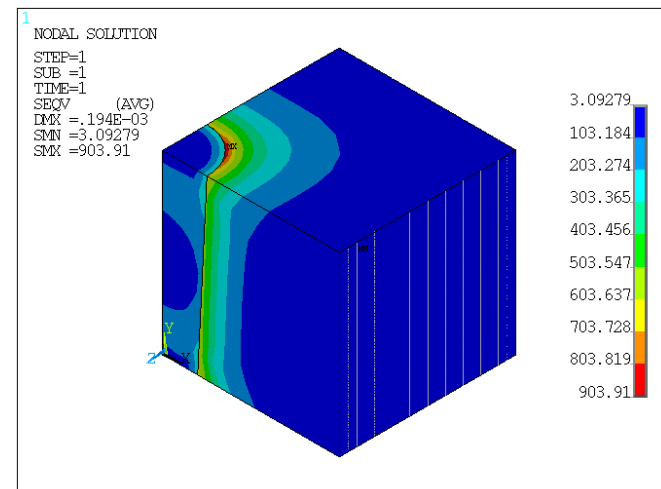
(e)

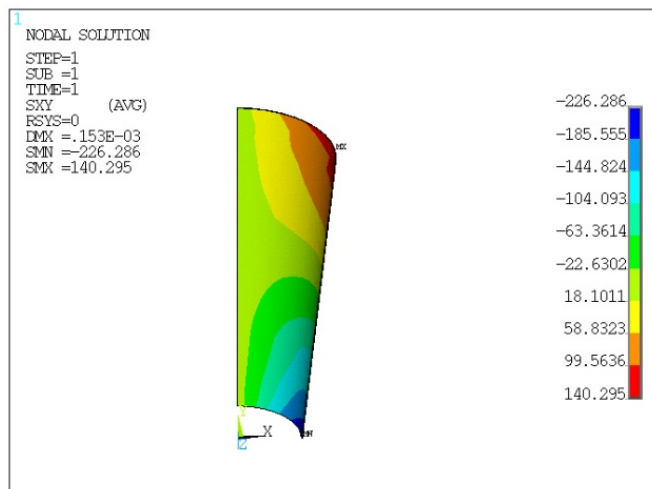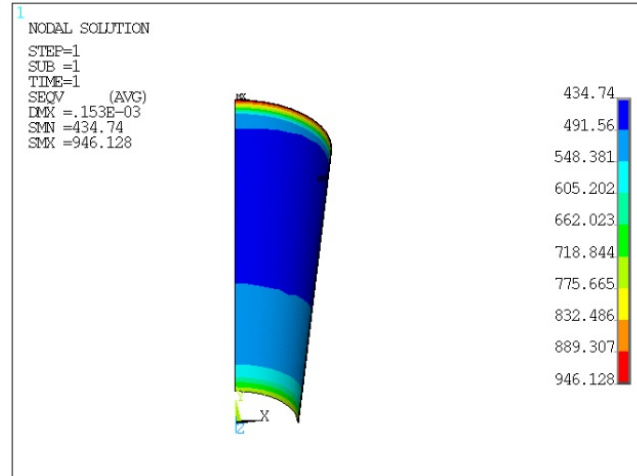*Figure 31: Contour plots of (a) the x displacement, (b) the x-component of stress, (c) the xy-shear stress, (d) the von Mises stress, and (e) the equivalent plastic strain after cooling. The model represents a quarter of a TSV unit cell in the 50 μm thickness anisotropic silicon wafer. The TSV structure has a base radius of 10 μm and a 3° tapered profile.*

Figure 32 and Figure 33 show the contour plots of the x-component of stress and the von Mises stress fields, respectively, of the anisotropic models, which have 0°, 3°, 6°, and 9° taper angles and a fixed 10 µm base radius TSVs.

Figure 34 and Figure 35 show that the maximum magnitudes of the compressive σ_{xx} and the von Mises stress of the anisotropic models generally increase linearly with the taper angle, except for the tensile σ_{xx} which stays relatively constant. The tensile σ_{xx} is higher than the corresponding one in isotropic model, but the magnitude of the compressive σ_{xx} is lower. This indicates that the x-component of stress in anisotropic model is also highly dependent on the orientation of the silicon.
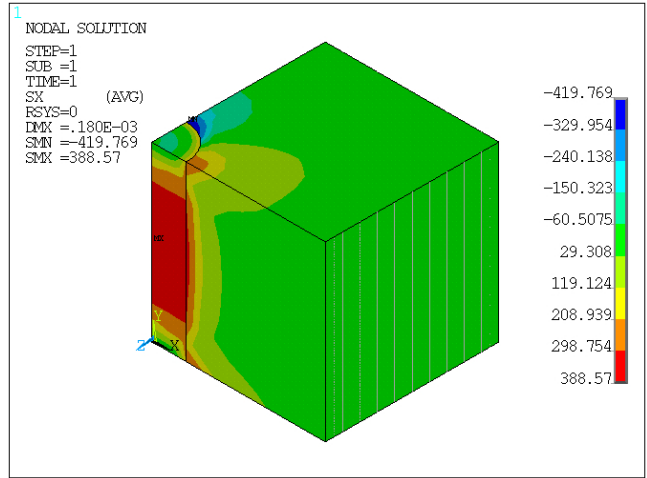
(a)
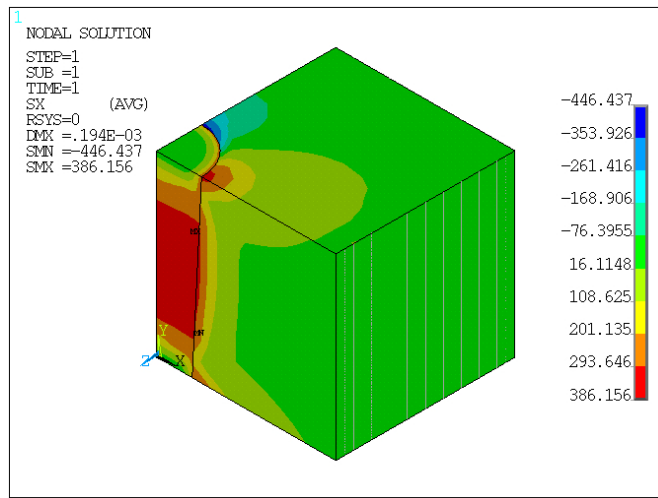
(b)
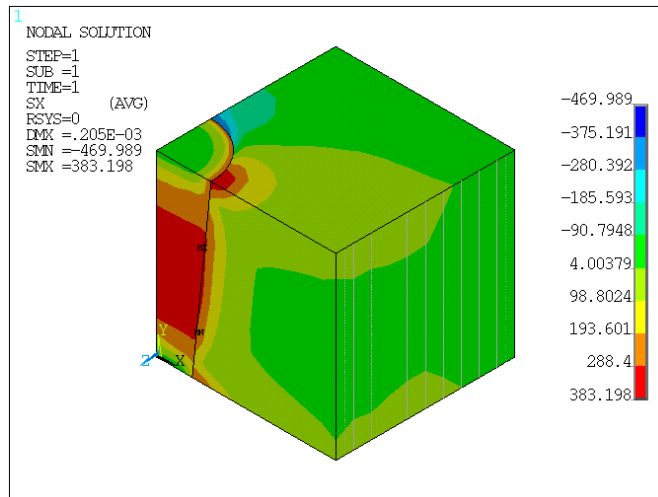
(c)
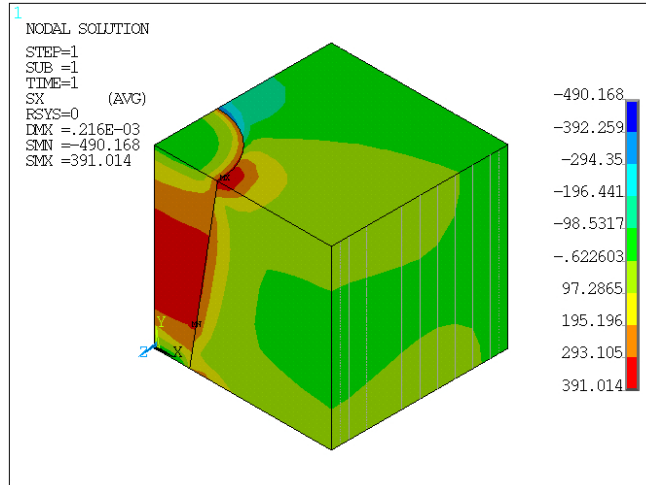
(d)

Figure 32: Comparison of the contour plots of the x-component of stress after cooling. The models represent a quarter of a TSV unit cell in the 50 µm thickness anisotropic silicon wafer. The TSV structures have a fixed 10 µm base radius and (a) 0°, (b) 3°, (c) 6°, and (d) 9° tapered profiles.

(a)

(b)

(c)

(d)

58
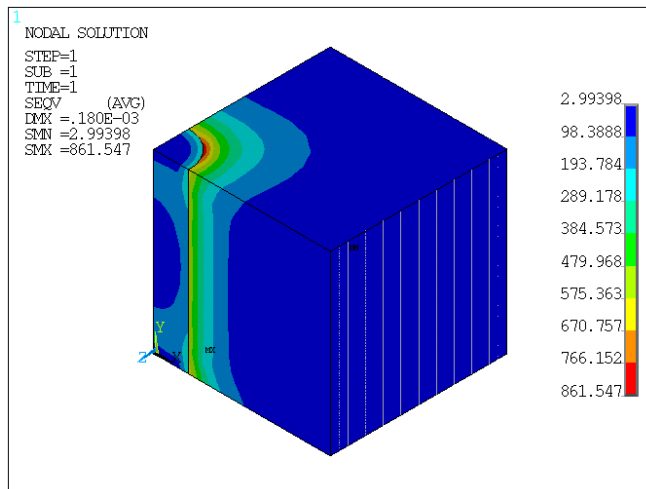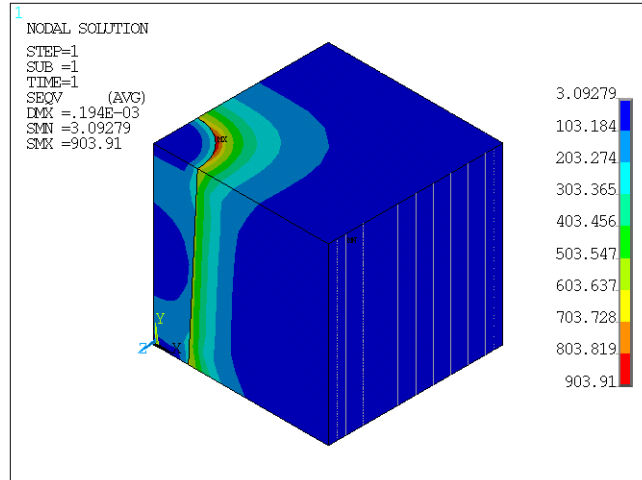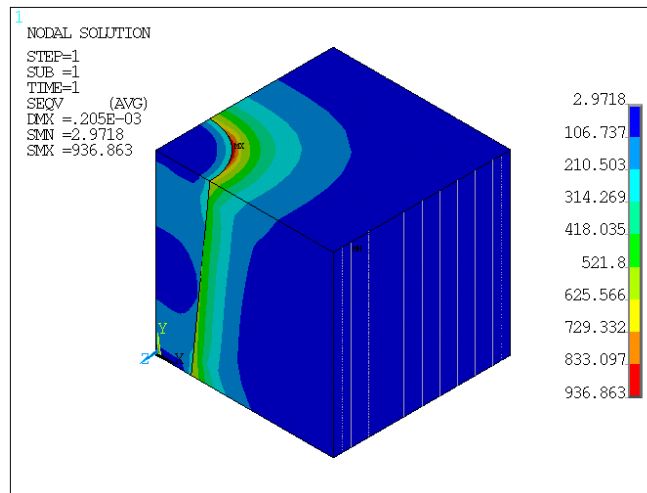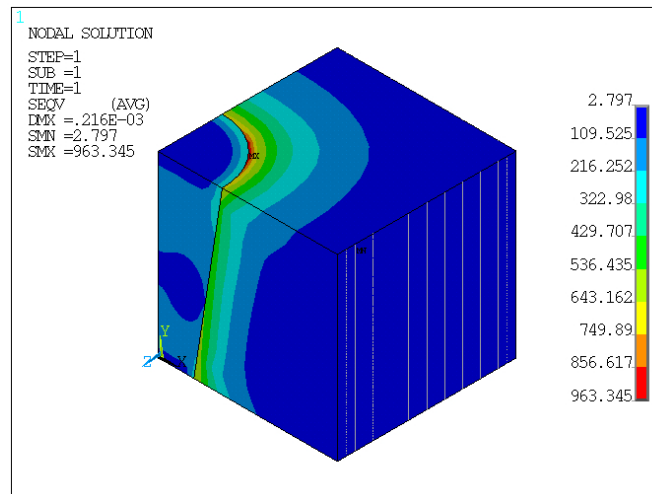
Figure 33: Comparison of the contour plots of the von Mises stress after cooling. The models represent a quarter of a TSV unit cell in the 50 μm thickness anisotropic silicon wafer. The TSV structures have a fixed 10 μm base radius and (a) 0°, (b) 3°, (c) 6°, and (d) 9° tapered profiles.
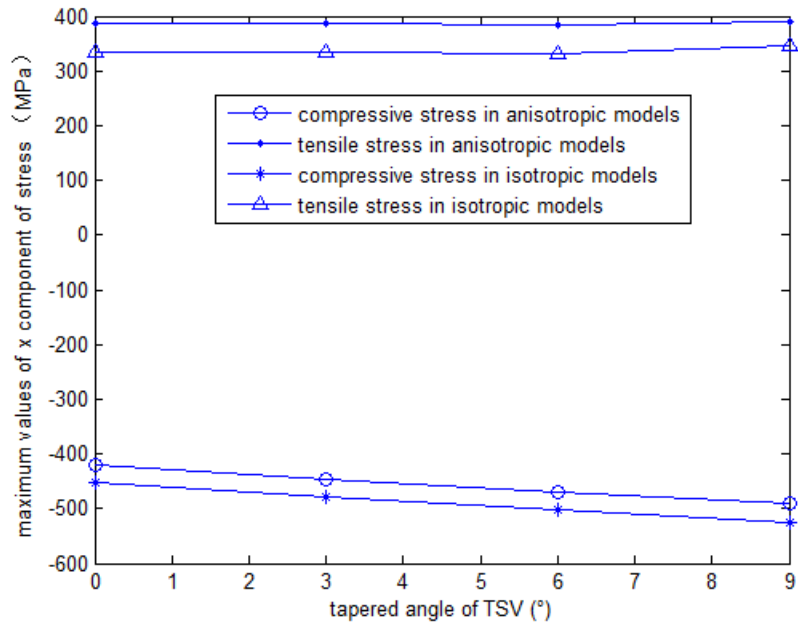
Figure 34: Comparision of the maximum values of x-component of stress *between isotropic and anisotropic models with respect to different angles of TSVs when the base radius of the TSV is fixed at 10 μm.*
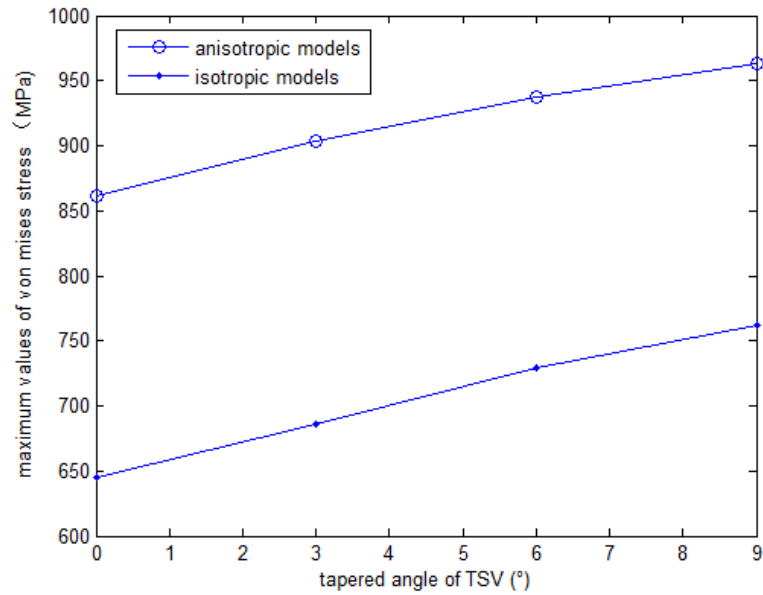
Figure 35: Comparision of the maximum values of the von Mises stress *between isotropic and anisotropic models with respect to different angles of TSVs when the base radius of the TSV is fixed at 10 μm.*

Figure 36 and Figure 37 demonstrate that the maximum values of the x-component of tensile and compressive stresses in the anisotropic models stay fairly constant with the TSV base radius, and the maximum value of the von Mises stress increases with a larger volume fraction of TSV at a fixed angle. The von Mises stress and tensile σ_{xx} in anisotropic models are higher than the ones in isotropic models.
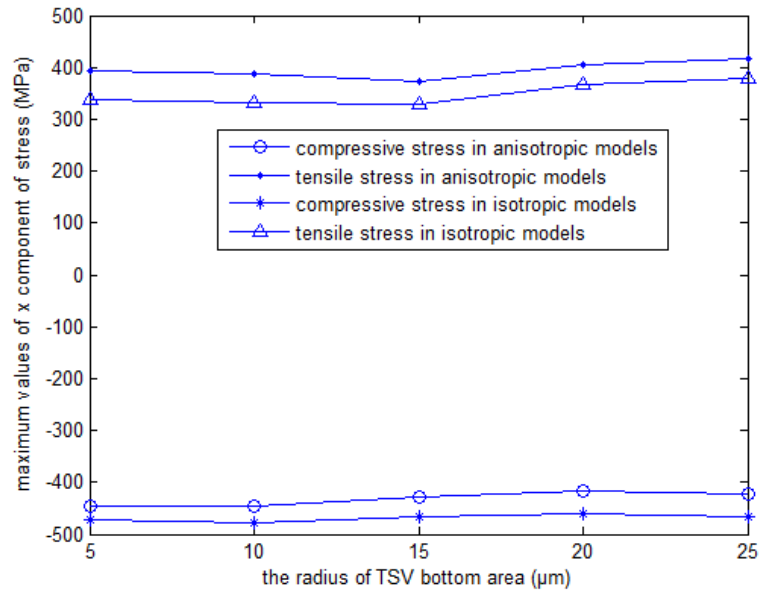
Figure 36: Comparison of the maximum values of the x-component of stress *between isotropic and anisotropic models with respect to different base radii of the TSVs when the angle is fixed at 3°.*
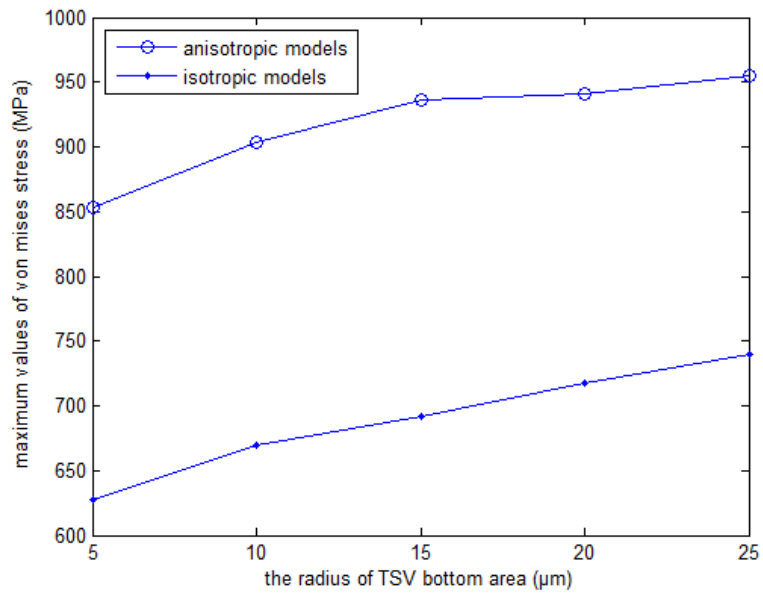
Figure 37: Comparision of the maximum values of the von Mises stress *between isotropic and anisotropic models with respect to different base radii of the TSVs when the taper angle is fixed at 3°.*

The curvature data are compiled to generate the 3D curvature surface plot with respect to the angle and the base diameter of the tapered TSV, as shown in Figure 38. It can be seen that the value of curvature is nearly proportional to the value of one variable while fixing the other. Figure 38 shows that the curvature of the anisotropic silicon wafer is only slightly smaller than the one of the isotropic silicon wafer.

Figure 38: 3D curvature surface plot of the 50 µm thickness anisotropic tapered TSV wafers with respect to different angles and base diameters of the TSVs.

4.6 Effect of Wafer Thickness

In addition to studying the 50µm-thick wafer, various models with 75 µm, 100 µm, and 125 µm wafer thicknesses have been established to study the effect of wafer thickness.

Figure 39, Figure 40, and Figure 41 show the contour plots of the models with 75 µm, 100 µm, and 125 µm thicknesses, respectively. The patterns in the corresponding contour plots are very similar.
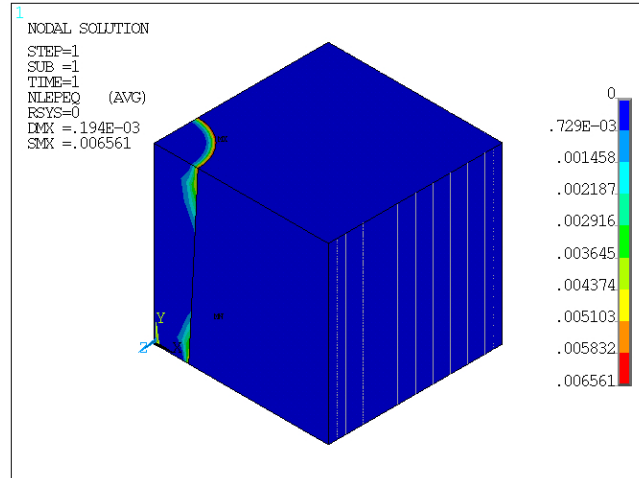
(a)

(b)

(c)

63
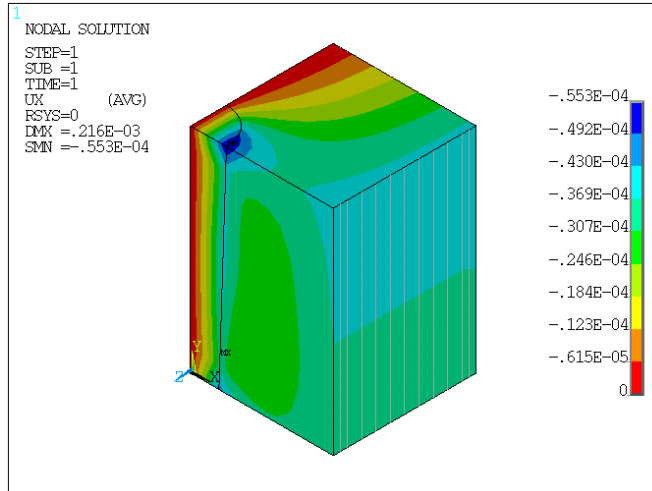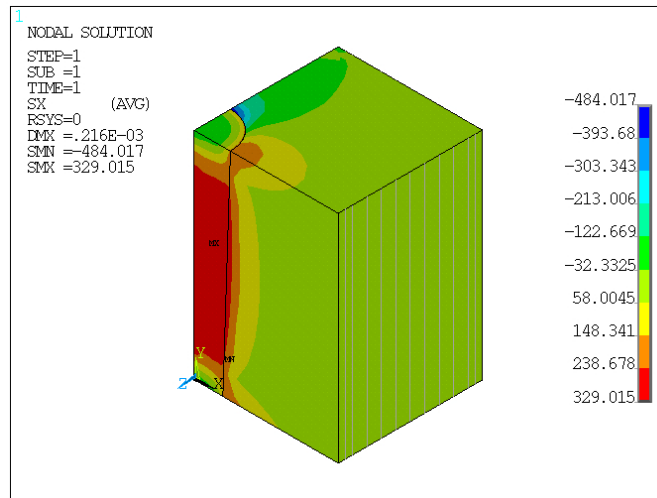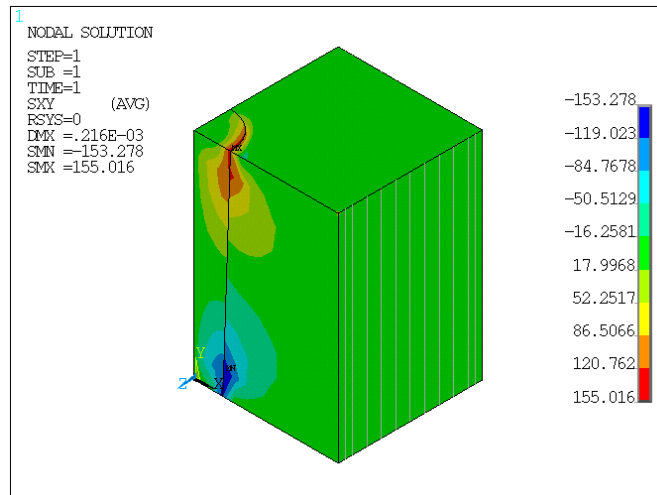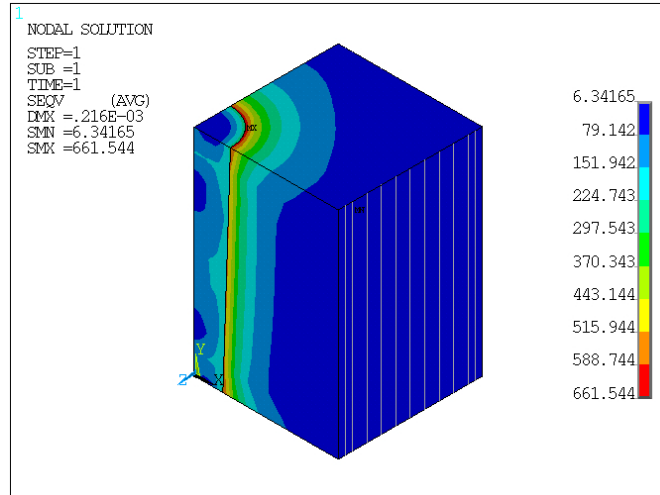
(d)
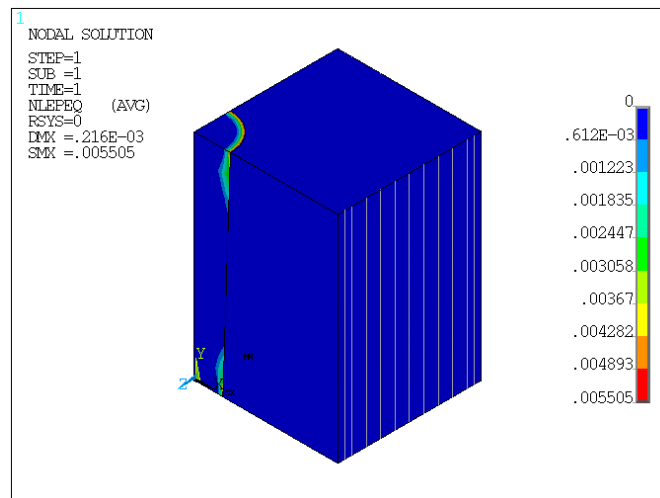
(e)

Figure 39: Contour plots of (a) the x displacement, (b) the x-component of stress, (c) the xy-shear stress, (d) the von Mises stress, and (e) the equivalent plastic strain after cooling. The model represents a quarter of a TSV unit cell in the 75 µm thickness isotropic silicon wafer. The TSV structure has a base radius of 10 µm and a 3° tapered profile.

(a)

(b)

(c)

65
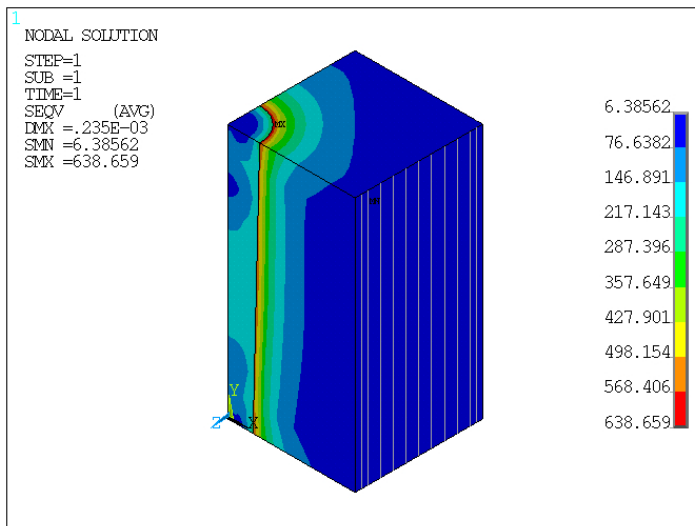
(d)
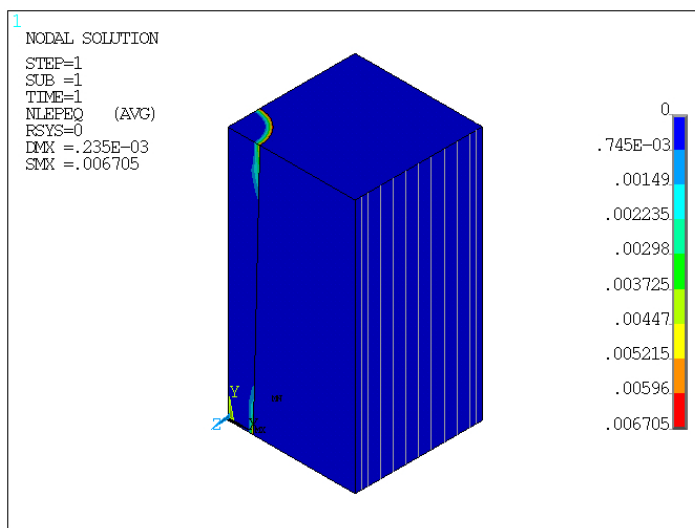
(e)

Figure 40: Contour plots of (a) the x displacement, (b) the x-component of stress, (c) the xy-shear stress, (d) the von Mises stress, and (e) the equivalent plastic strain after cooling. The model represents a quarter of a TSV unit cell in the 100 μm thickness isotropic silicon wafer. The TSV structure has a base radius of 10 μm and a 3° tapered profile.

(a)

(b)

(c)
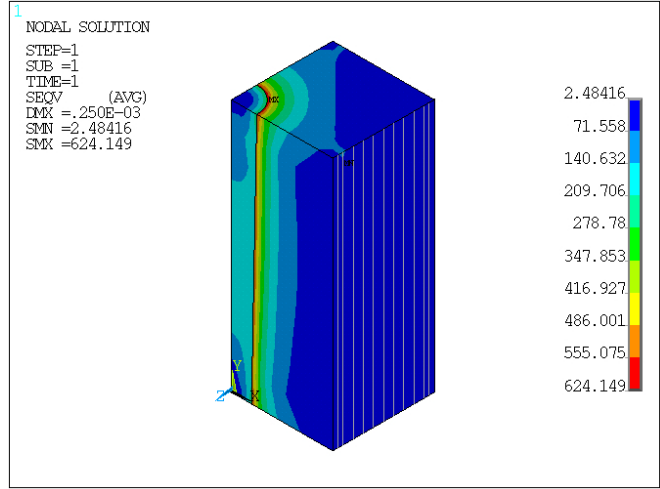
(d)
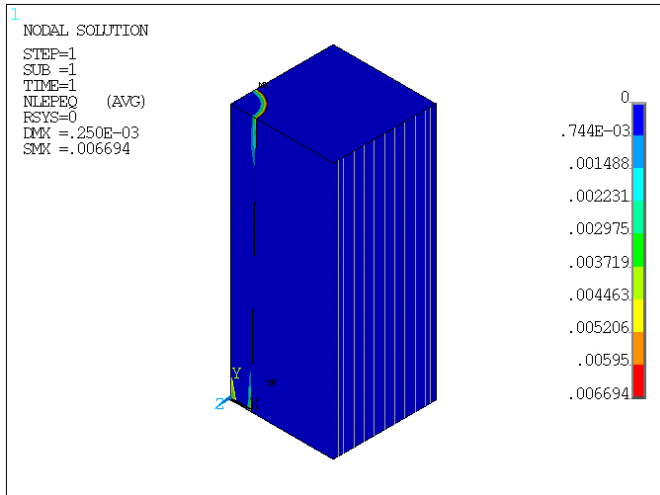
(e)

Figure 41: Contour plots of (a) the x displacement, (b) the x-component of stress, (c) the xy-shear stress, (d) the von Mises stress, and (e) the equivalent plastic strain after cooling. The model represents a quarter of a TSV unit cell in the 125 µm thickness isotropic silicon wafer. The TSV structure has a base radius of 10 µm and a 3° tapered profile.

Figure 42 shows the maximum values of the von Mises stress with respect to different angles of TSVs and different wafer thicknesses when the base radius of the TSV is fixed at 10 µm. It is evident that the maximum value of the von Mises stress generally increases linearly with the taper angle. The von Mises stress value decreases as the wafer thickness increases.
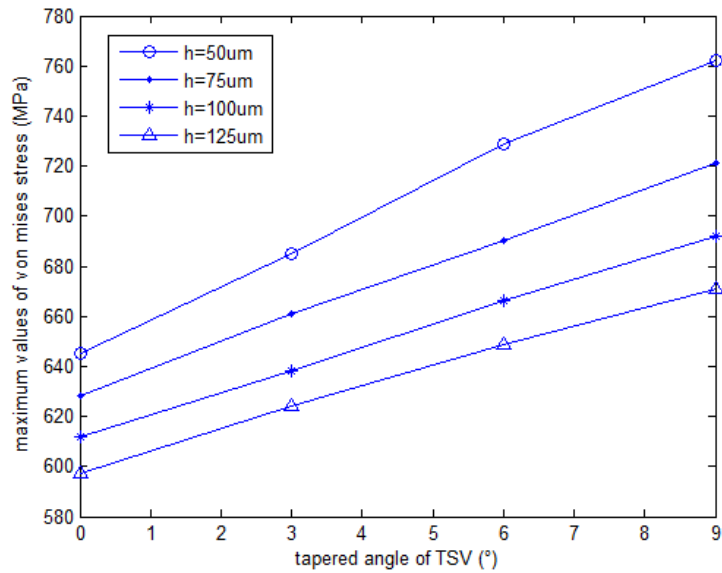
Figure 42: Comparision of the maximum values of the von Mises stress with respect to different angles of TSVs and different wafer thicknesses when the base radius of the TSV is fixed at 10 µm.

Figure 43 shows the maximum values of the von Mises stress with respect to different base radii of the TSVs and different wafer thicknesses when the angle of the TSV is fixed at 3°. The maximum values of the von Mises stress are observed to increase with the base radius of the TSV, and the von Mises stress magnitude decreases with the wafer thickness.
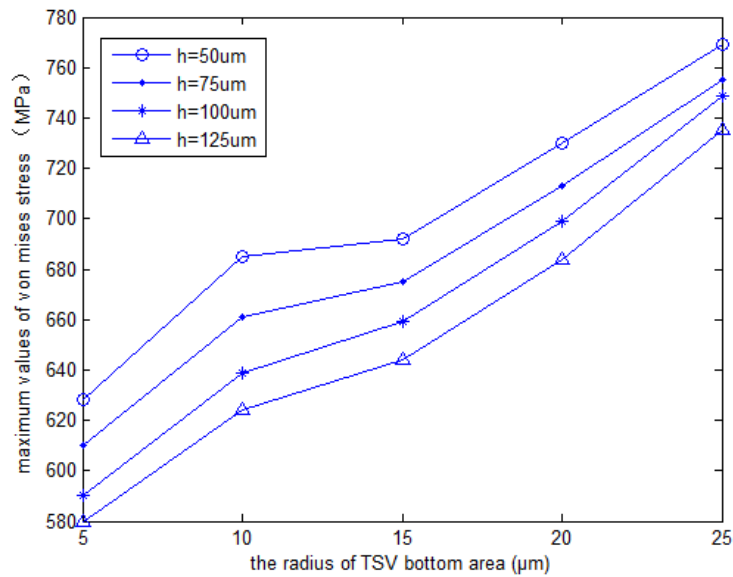
Figure 43: Comparision of the maximum values of the von Mises stress with respect to different base radii of the TSVs and different wafer thicknesses when the angle of the TSV is fixed at 3°.

Figure 44, Figure 45, and Figure 46 show the 3D curvature surface plots of the 75 µm, 100 µm, 125 µm thicknesses isotropic tapered TSV wafers with respect to different angles and different base diameters of the TSVs, respectively.
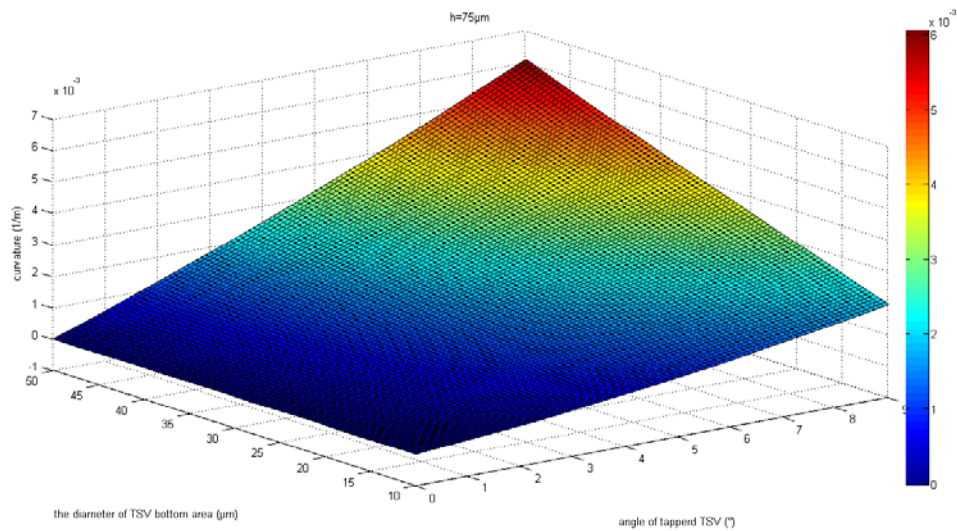
Figure 44: 3D curvature surface plot of the 75 µm thickness isotropic tapered TSV wafers with respect to different angles and different base diameters of the TSVs.
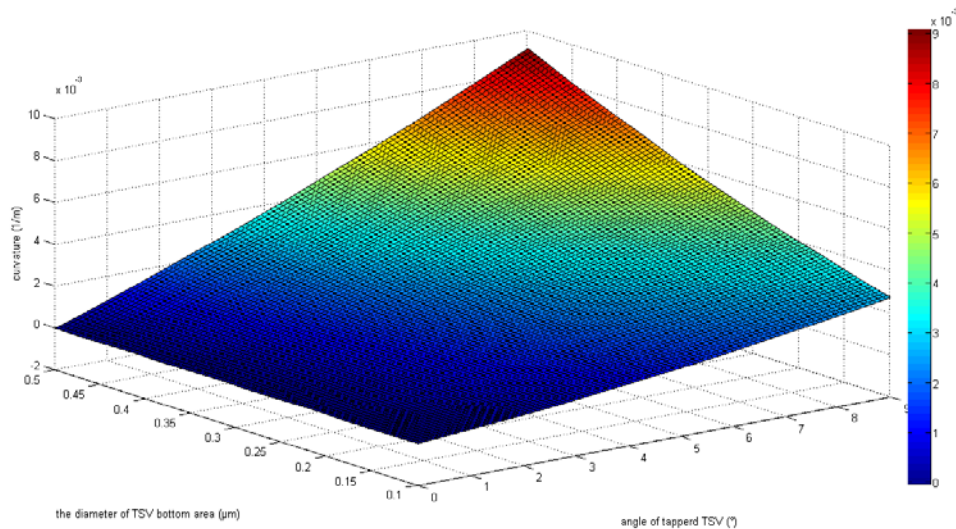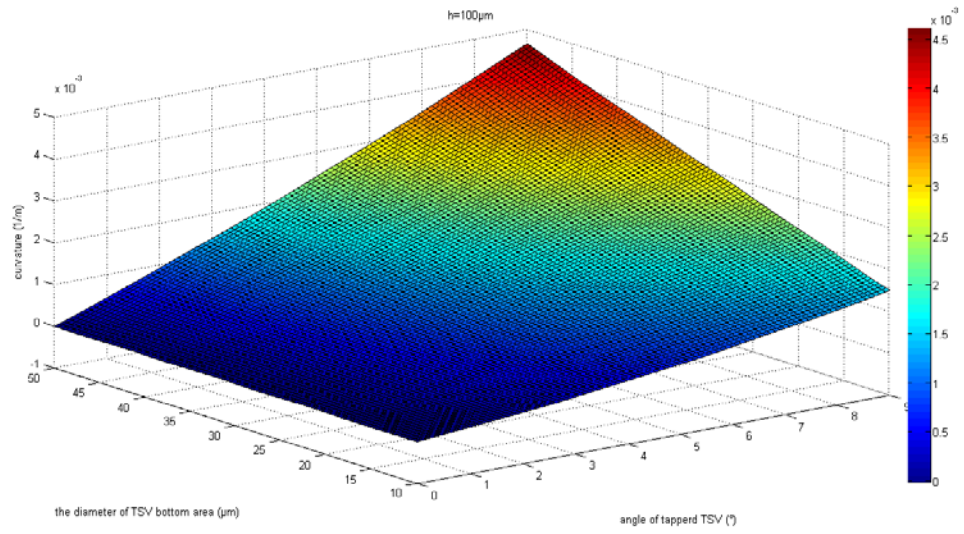
Figure 45: 3D curvature surface plot of the 100 μm thickness isotropic tapered TSV wafers with respect to different angles and different base diameters of the TSVs.
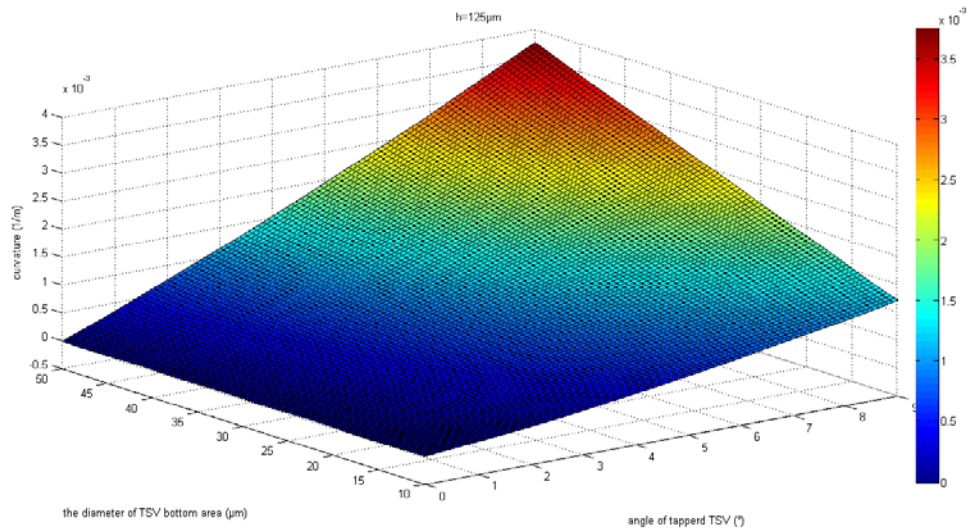
*Figure 46: 3D curvature surface plot of the 125 μm thickness isotropic tapered TSV wafers with respect to different angles and different base diameters of the TSVs.*

Figure 47 shows the overall curvature plots. It demonstrates that increasing the wafer thickness can dramatically reduce the wafer curvature caused by thermal loading. This is because the thick TSV wafer stiffens the wafer matrix and reduces wafer warpage. However, the high aspect ratio TSVs, caused by a thicker wafer, may bring some other problems, such as the difficulties of depositions of intermediate layers and copper electroplating.
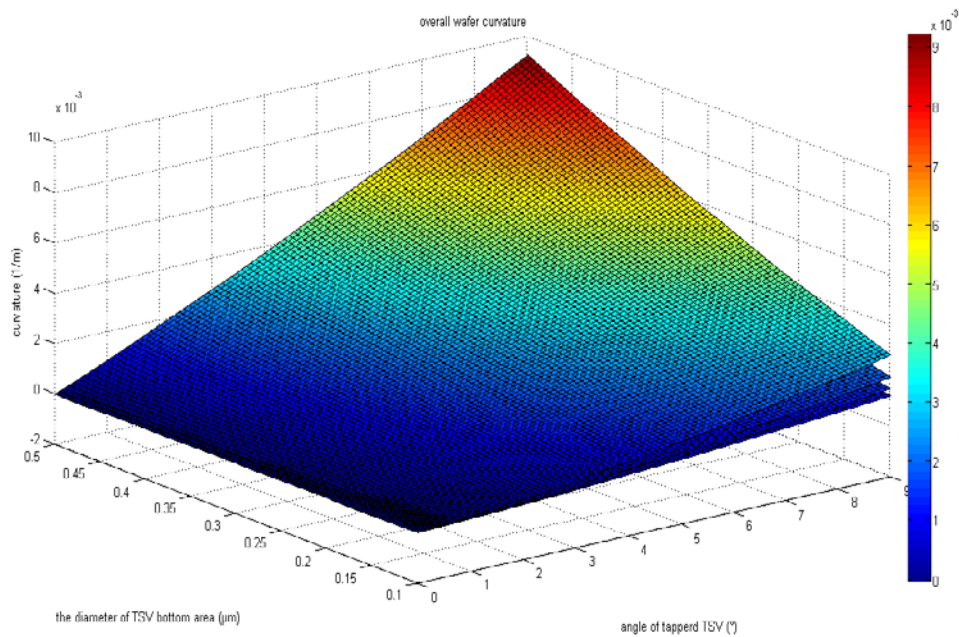
Figure 47: The overall 3D curvature surface plots of the 50 µm, 75 µm, 100 µm, and 125 µm thicknesses of isotropic tapered TSV wafers with respect to different angles and different base diameters of the TSVs.

4.7 Effect of TSV Pitch

Up to this point, the distance between two adjacent TSVs was considered as 100 µm. To study the effect of TSV pitch, a distance of 200 µm is now used in the models.

Figure 48 shows the contour plots of the x displacement, the x-component of stress, the von Mises stress, and the equivalent plastic strain of 200 µm-pitch model. The TSV structure has a base radius of 10 µm and a 3° tapered profile.
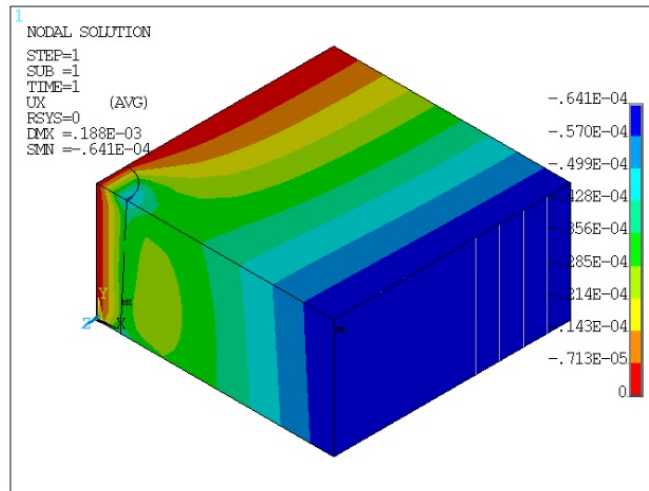
(a)
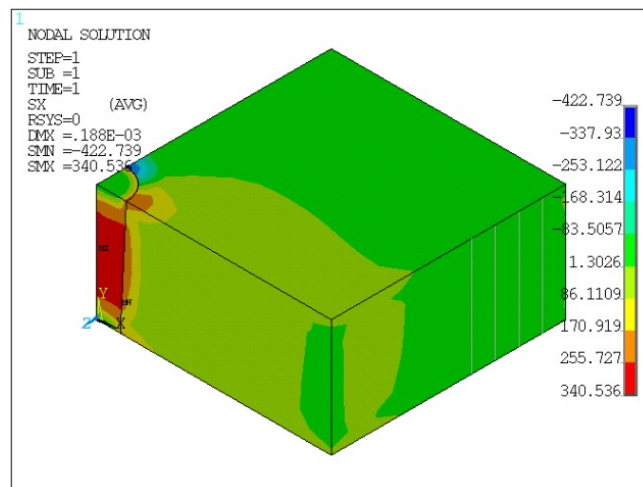
(b)
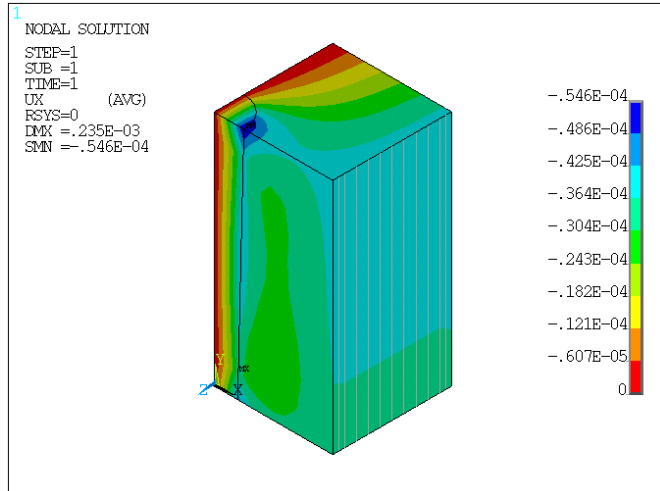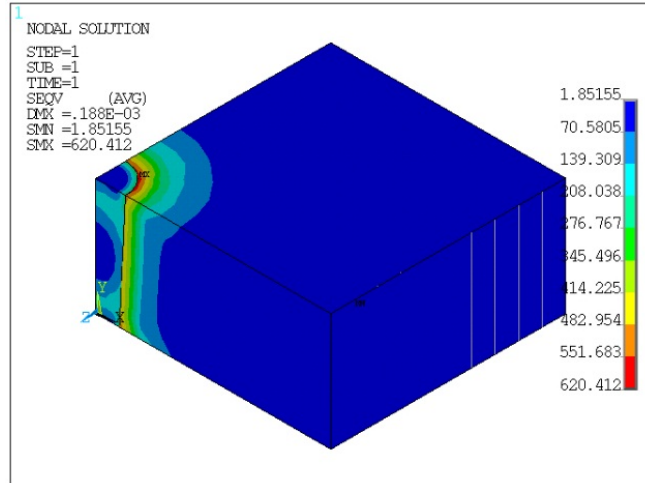
(c)
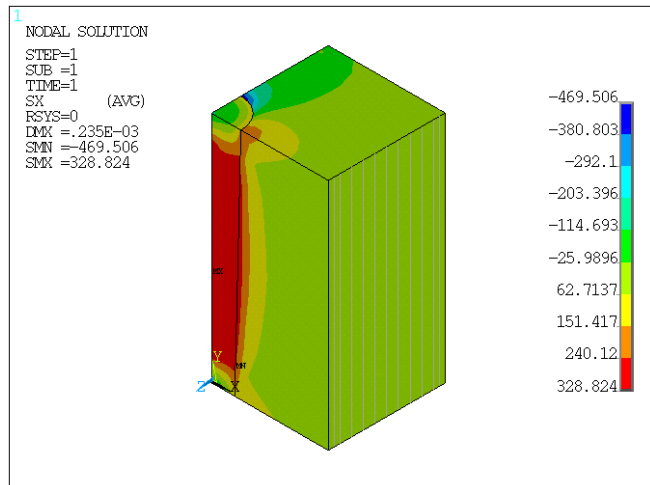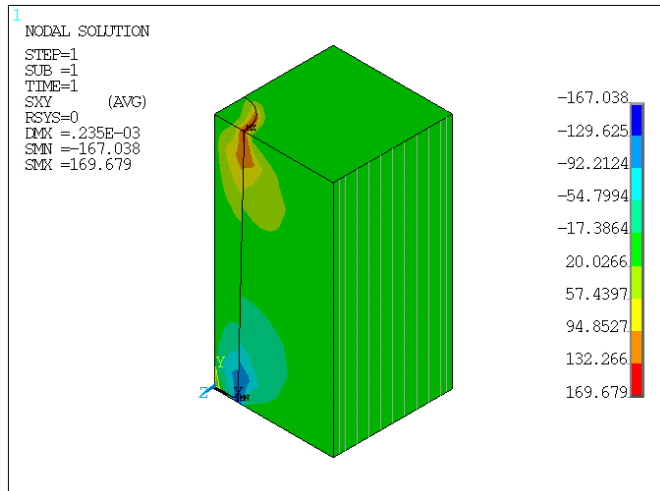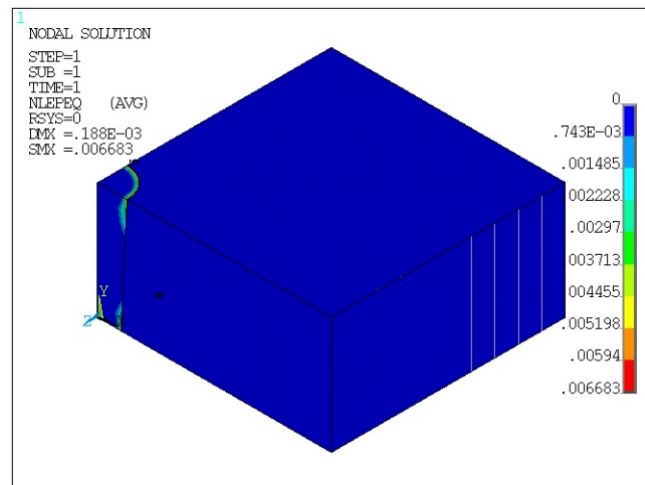

(d)

Figure 48: Contour plots of the (a) the x displacement, (b) the x-component of stress, (c) the von Mises stress, and (d) the equivalent plastic strain after cooling. The model represents a quarter of a TSV unit cell in the 50 μm thickness isotropic silicon wafer. The TSV structure has a base radius of 10 μm and a 3° tapered profile. The pitch between two adjacent TSVs is 200 μm.
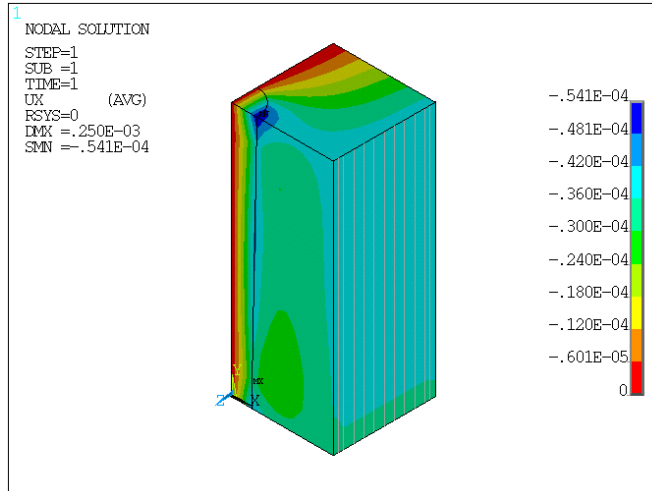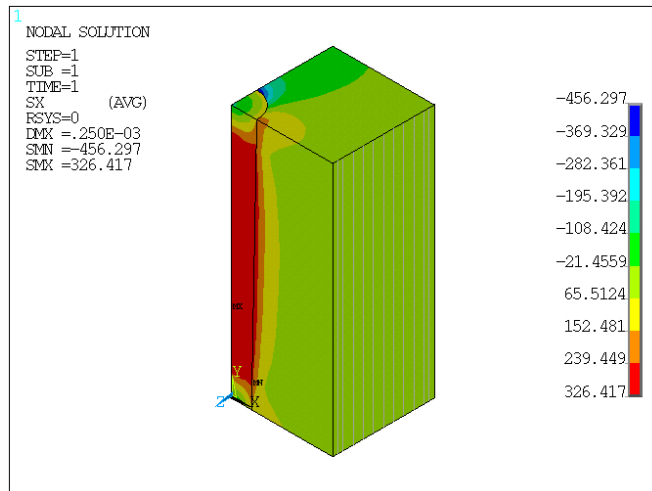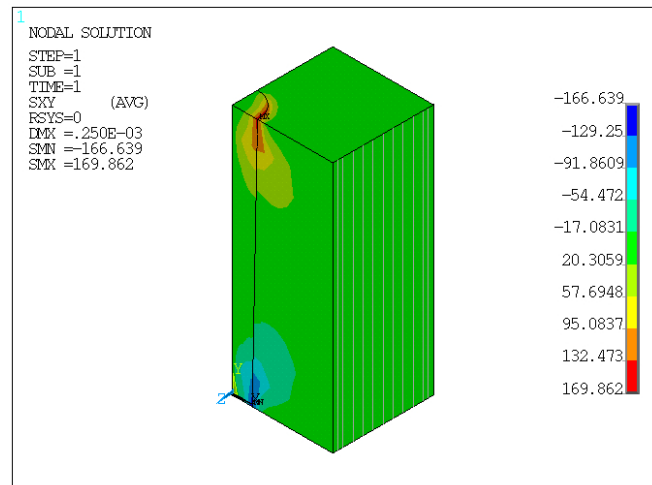
Figure 49 shows a comparison of the maximum values of the von Mises stress between p = 100 μm and p = 200 μm models with respect to different angles. The maximum value of the von Mises stress in the 200 μm-pitch model increases linearly with the taper angle. The von Mises stress in the 200 μm-pitch model is much lower compared to the one in the 100 um-pitch model.
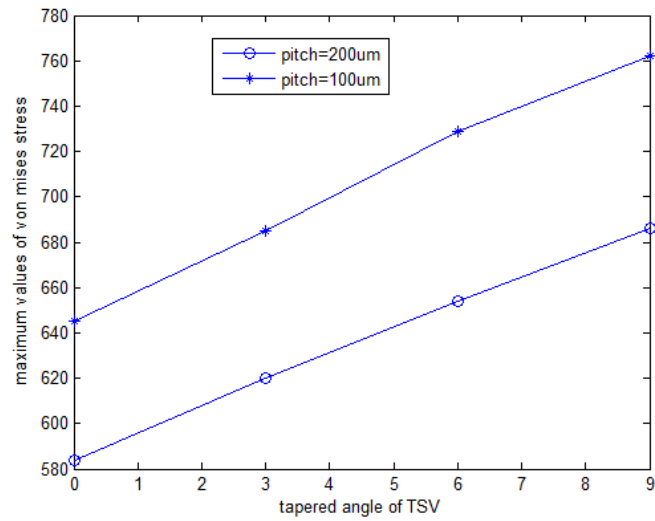
Figure 49: Comparision of the maximum values of the von Mises stress between p = 100 μm and p = 200 μm models with respect to different angles of TSVs when the base radius of the TSV is fixed at 10 μm.

Figure 50 shows the 3D curvature surface plot of the 50 µm thickness isotropic tapered TSV wafers with respect to the angle and the base diameter of the TSV. The pitch between two adjacent TSVs is 200 µm.
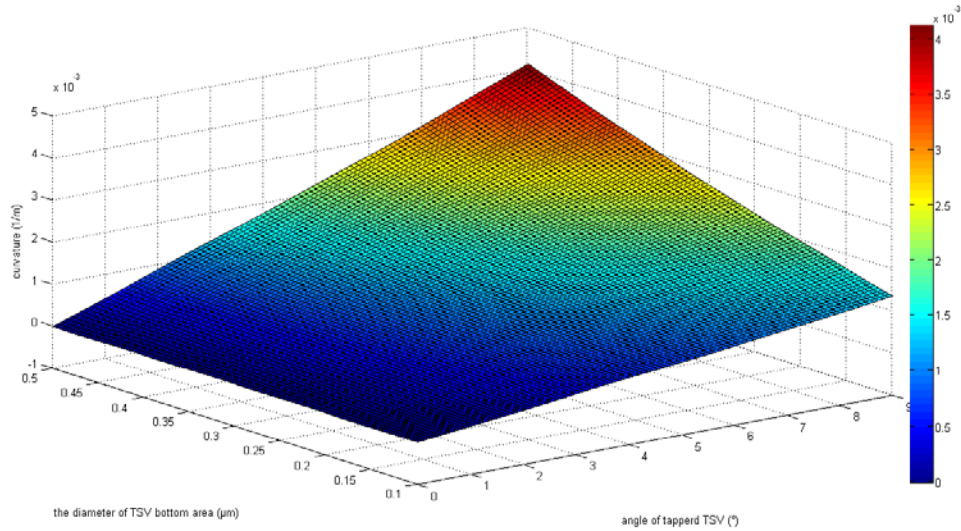
Figure 50: 3D curvature surface plot of the 50 μm thickness isotropic tapered TSV wafers with respect to different angles and different base diameters of the TSVs. The pitch between two adjacent TSVs is 200 μm.

It is noticed that, compared to Figure 22, the curvature of the 200 µm-pitch TSV wafer is approximately half of the 100 um-pitch case, because there is a greater silicon volume in each unit cell and it stiffens the entire TSV wafer with less bending.

Chapter 5

Carrier Mobility Change and Keep-Out Zone (KOZ)

Thermally induced stress concentration around copper TSV can lead to degradation of the device performance by affecting the MOSFET device's carrier mobility. It causes some serious reliability concerns. Piezoresistivity of silicon refers to the change in the electrical resistivity while mechanical stress is applied. This effect can be used to make piezoresistive devices for stress sensing [34]. However, the same effect also detrimentally impacts the performance of microelectronic devices. The electronic components are fabricated near the silicon wafer surface. KOZ is a region near the silicon wafer surface where high stresses are concentrated, therefore active transistors should be kept away. In this chapter, the KOZ is identified based on the thermal stress modeling results and a threshold mobility change of 5%.

3D FEA models are used to characterize the thermal stress distribution as in the previous chapter. The mobility change and the size of KOZ are further calculated by extracting the near-surface stresses and putting them into relevant equations (see below). The anisotropic elastic silicon wafer is considered, as in section 4.5. Two vertical channel directions, [100] and [010], and two types of MOSFET devices, n-type and p-type, are considered to quantify the piezoresistivity effect on transistor's carrier mobility [35].

The resistivity change ($\Delta\rho_i$) is related to stress (σ_k) by a piezoresistance tensor (π_{ik}) [36],

$$\Delta\rho_i/\rho = \pi_{ik}\,\sigma_k \tag{1}$$

Here, for cubic semiconducting crystals, the piezoresistance tensor is a 6×6 matrix:

$$\pi_{ik} = \begin{pmatrix} \pi_{11} & \pi_{12} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{11} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{12} & \pi_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \pi_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \pi_{44} \end{pmatrix}.$$

The piezoresistance coefficients of n-MOSFET and p-MOSFET measured along with the current in the [100] direction are given in Table 3.

	π_{11}	π_{12}	π_{44}
n-type Si	-102.2	53.7	-13.6
p-type Si	6.6	-1.1	138.1

Table 3: The piezoresistance coefficients for n-MOSFET and p-MOSFET (unit: 10^{-11} Pa^{-1})

Resistivity is inversely proportional to mobility, and thus the carrier mobility change ($\Delta\mu$) owing to piezoresistivity can be presented as following:

$$\Delta\mu/\mu = -\Delta\rho/\rho. \tag{2}$$

For the case that the transistors' channels are along with the [100] direction, and the current is imposed in the same direction, the magnitude of the carrier mobility change can be presented as follows [35, 37]:

$$\Delta\mu/\mu = |\pi_{11}\sigma_{xx} + \pi_{12}(\sigma_{zz} + \sigma_{yy})|\,. \tag{3}$$

For the case that the transistors' channels are along with the [010] direction, and the current is imposed in the same direction, the magnitude of the carrier mobility change is then expressed as follows [35, 37]:

$$\Delta\mu/\mu = |(\pi_{11} + \pi_{12})\,(\sigma_{xx} + \sigma_{zz})/2 + \pi_{44}\sigma_{xz}| \tag{4}$$

The values of the stress components on the top surface of the TSV structure were extracted from the FEA simulation results to calculate the carrier mobility change. Figure 51 shows the top view of a quarter of the TSV unit cell structure. The contour plots shown in Figure 51 represent the carrier mobility change for n-MOSFET and p-MOSFET devices that are along with the [100] and [010] directions in the model with a 3° taper angle and 10 µm base radius TSV.

(a)

mobility change Δμ/μ (%)

(b)
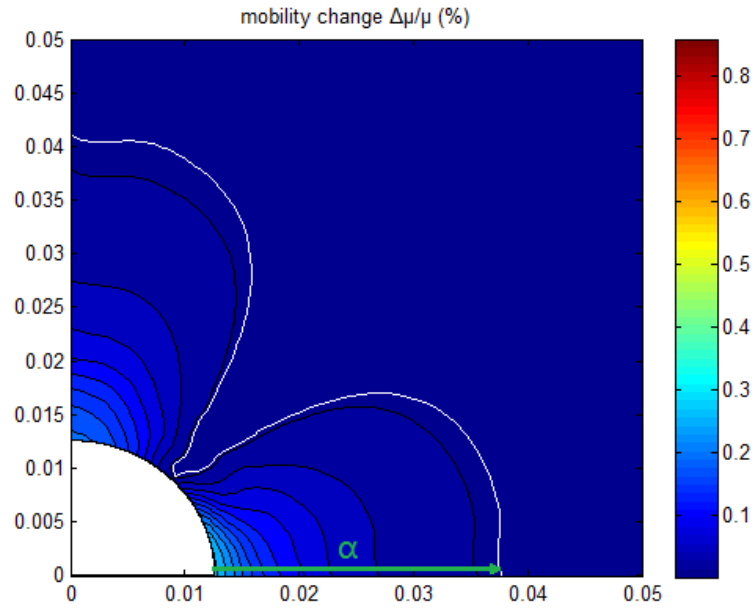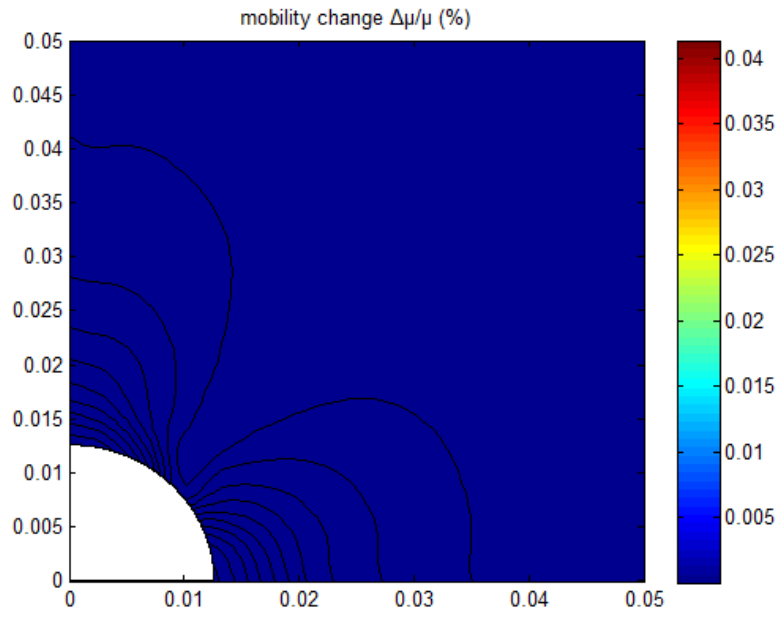
mobility change Δμ/μ (%)
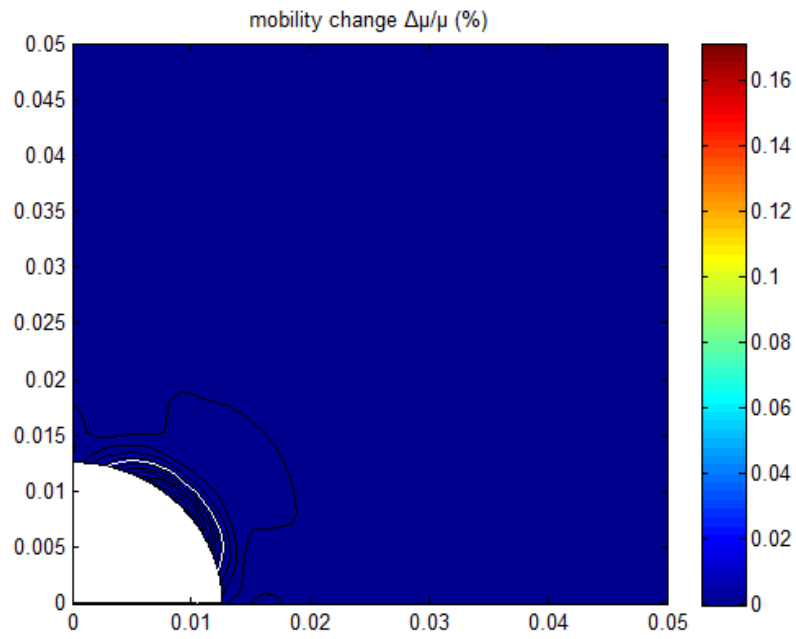
(c)
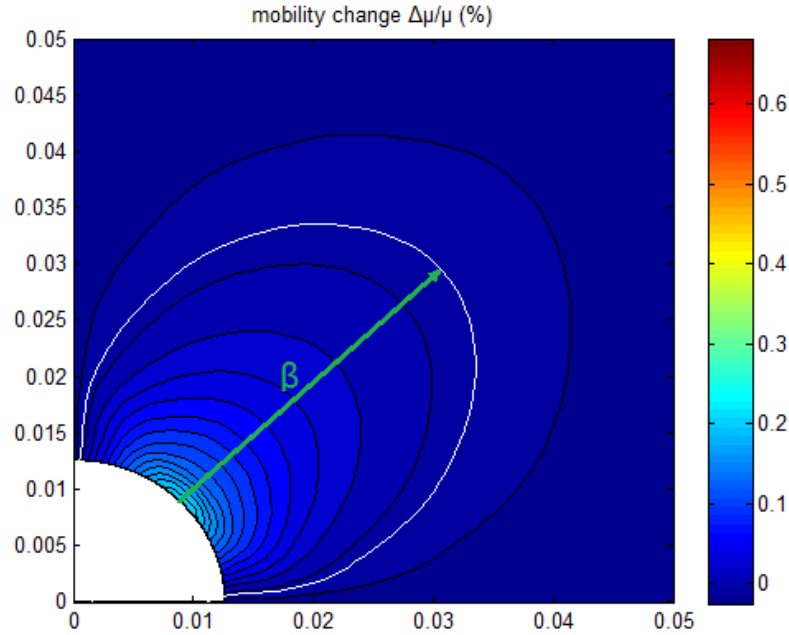
(d)

Figure 51: Mobility change contour plots for (a) n-MOSFET aligned along the [100] channel, (b) p-MOSFET aligned along the [100] channel, (c) n-MOSFET aligned along the [010] channel, (d) p-MOSFET aligned along the [010] channel. The model represents a quarter of a TSV unit cell in the 50 μm thickness isotropic silicon wafer. The TSV structure has a base radius of 10 μm and a 3° tapered profile.

The boundary of KOZ is marked with the white line, within which the carrier mobility change is more than 5%. It can be seen that the effect of piezoresistivity is much more prominent for n-MOSFET along with the [100] channel and p-MOSFET along with the [010] channel. The lengths of KOZs for n-MOSFET along with the [100] direction and p-MOSFET along with the [010] direction are denoted by α and β, respectively. In the model that has the TSV with a base radius of 10 μm and a 3° tapered profile, the characteristic length α is 25.5 μm and the characteristic length β is 29.2 μm.

Figure 52, Figure 53, and Figure 54 show the contour plots of the carrier mobility change for n-MOSFET and p-MOSFET devices that are in the [100] and [010] directions in the cases with 0°, 6°, 9° taper angles, respectively, and a fixed 10 μm base radius TSVs.
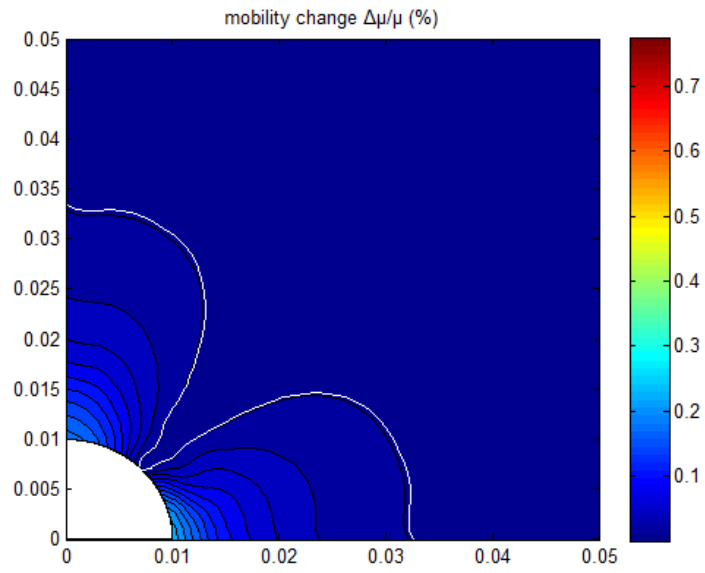
(a)
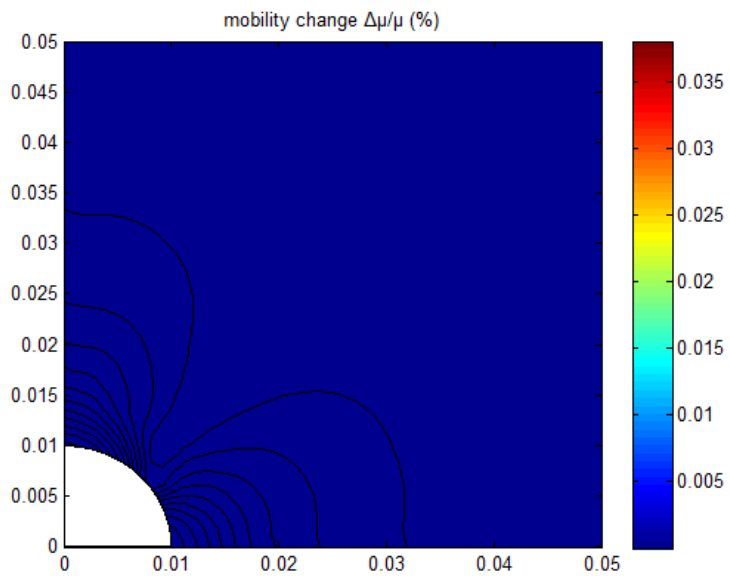
(b)
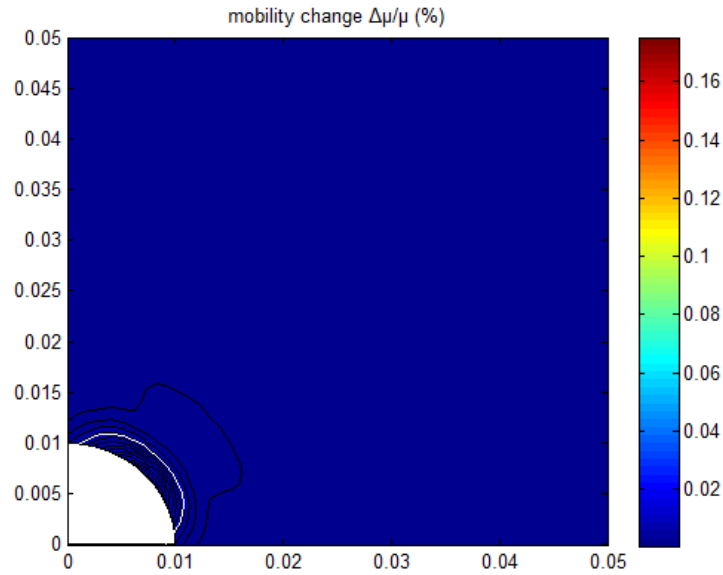
(c)
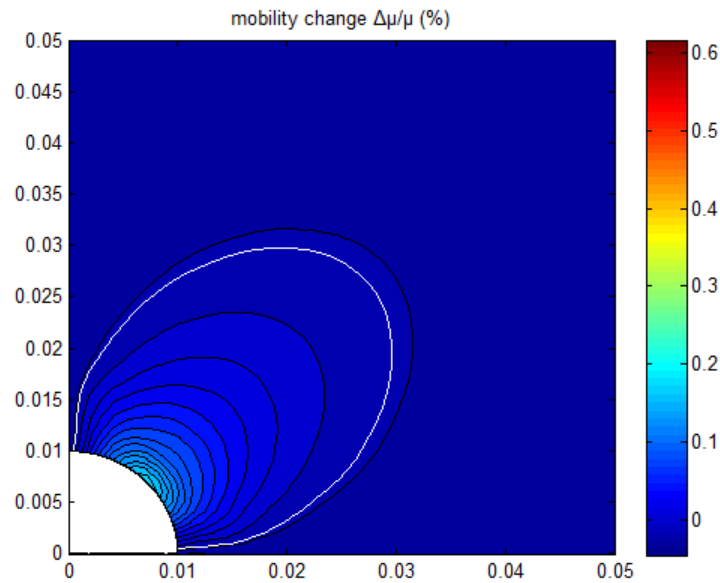
(d)

Figure 52: Mobility change contour plots for (a) n-MOSFET aligned along the [100] channel, (b) p-MOSFET aligned along the [100] channel, (c) n-MOSFET aligned along the [010] channel, (d) p-MOSFET aligned along the [010] channel. The model represents a quarter of a TSV unit cell in the 50 μm thickness isotropic silicon wafer. The TSV structure has a base radius of 10 μm and a straight profile.

(a)

(b)

mobility change Δμ/μ (%)

(c)
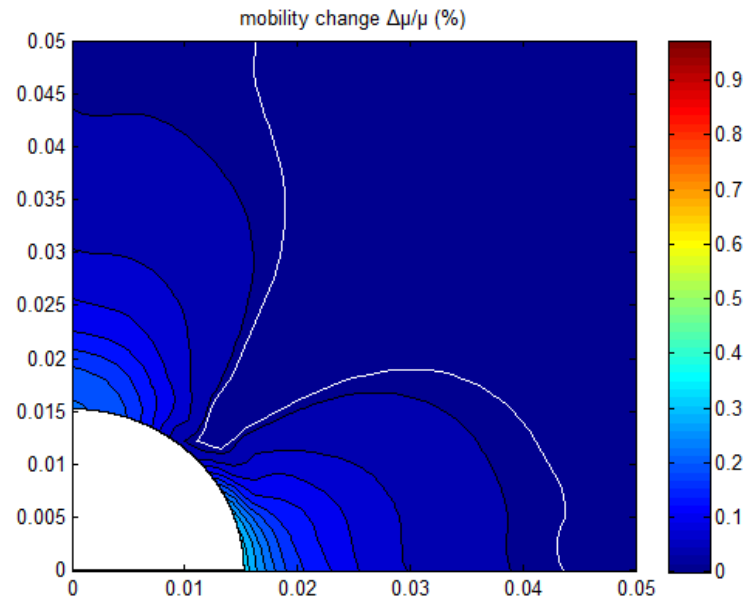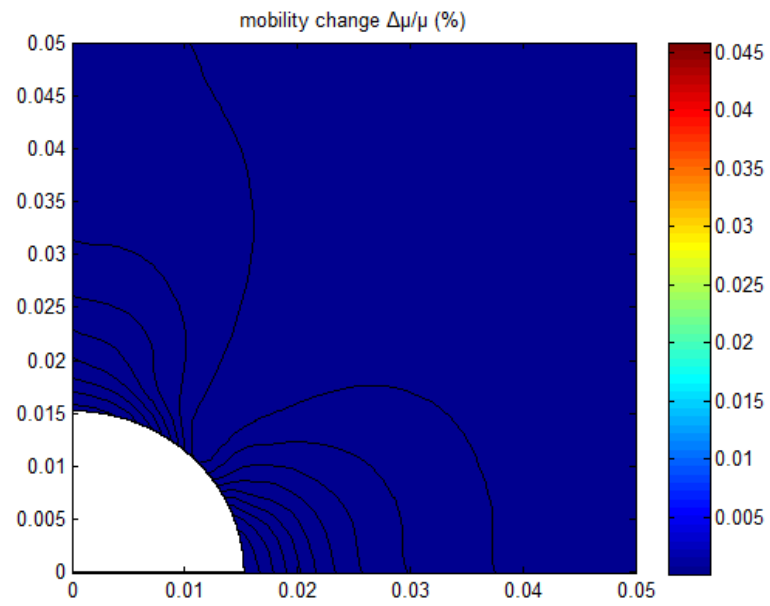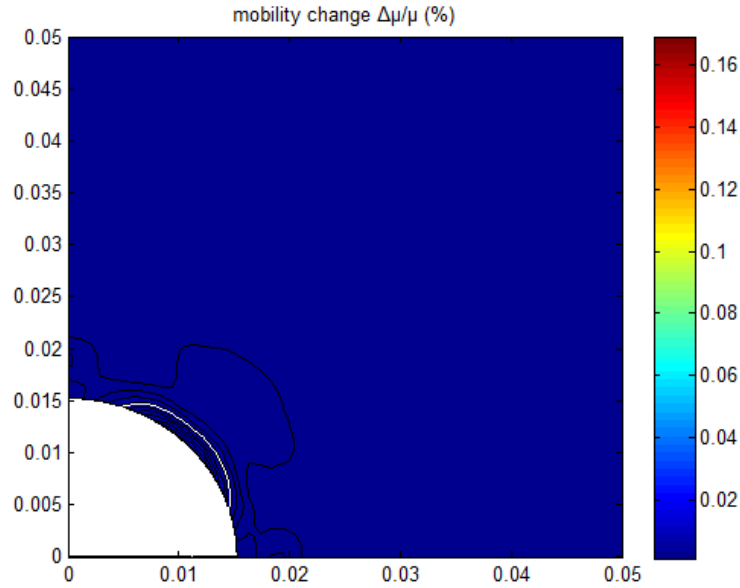
mobility change Δμ/μ (%)
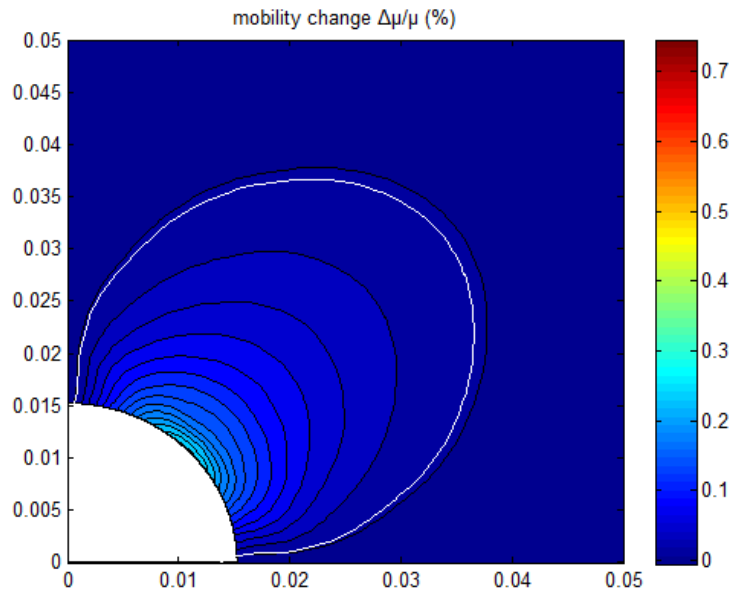
(d)

Figure 53: Mobility change contour plots for (a) n-MOSFET aligned along the [100] channel, (b) p-MOSFET aligned along the [100] channel, (c) n-MOSFET aligned along the [010] channel, (d) p-MOSFET aligned along the [010] channel. The model represents a quarter of a TSV unit cell in the 50 μm thickness isotropic silicon wafer. The TSV structure has a base radius of 10 μm and a 6° tapered profile.
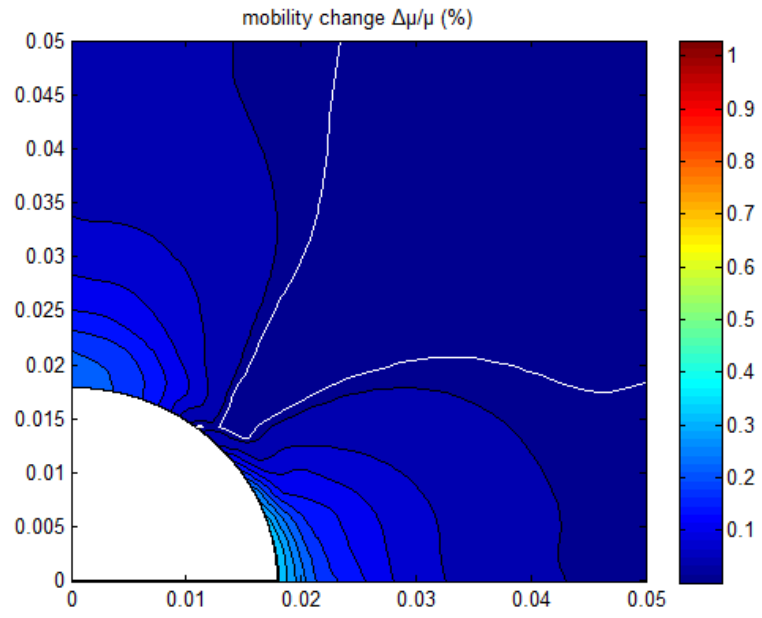
(a)
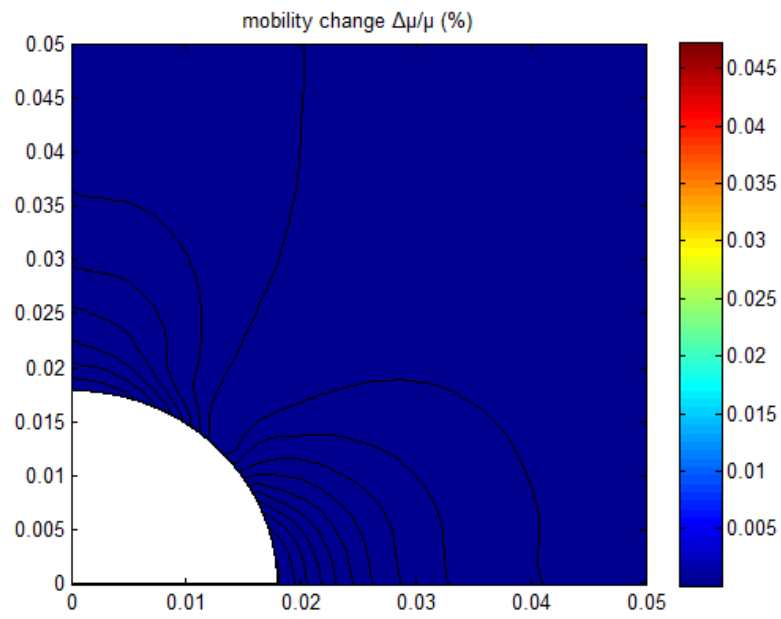
(b)
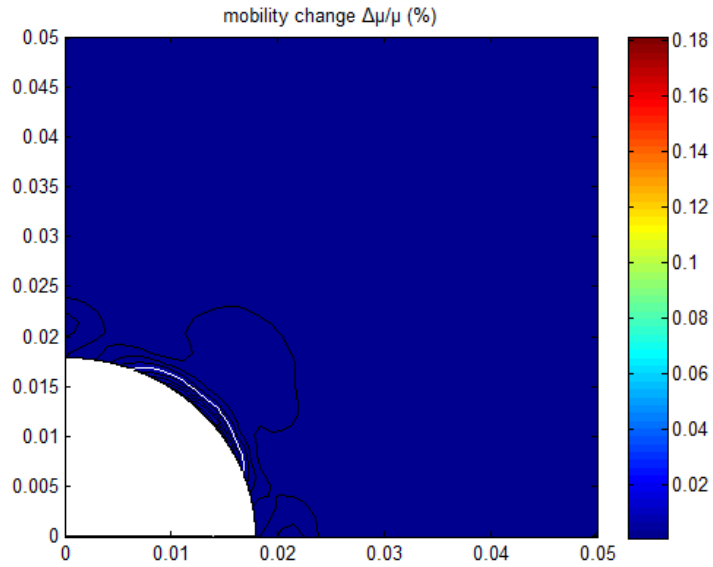
(c)
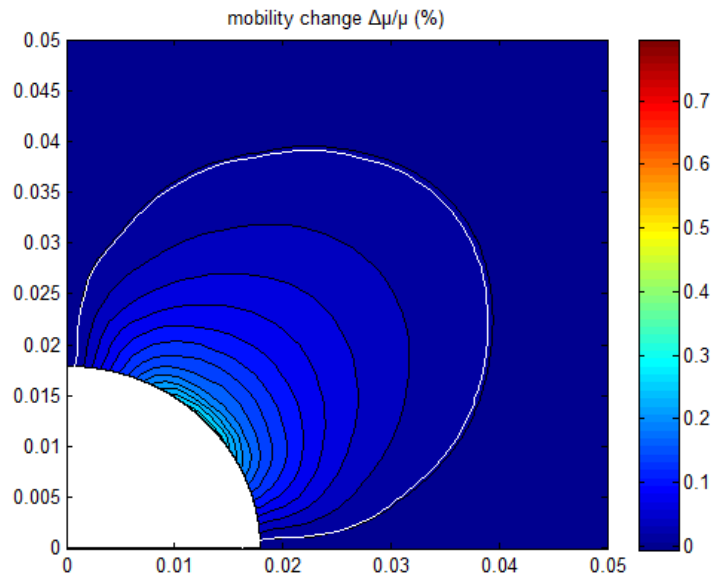
(d)

Figure 54: Mobility change contour plots for (a) n-MOSFET aligned along the [100] channel, (b) p-MOSFET aligned along the [100] channel, (c) n-MOSFET aligned along the [010] channel, (d) p-MOSFET aligned along the [010] channel. The model represents a quarter of a TSV unit cell in the 50 μm thickness isotropic silicon wafer. The TSV structure has a base radius of 10 μm and a 9° tapered profile.
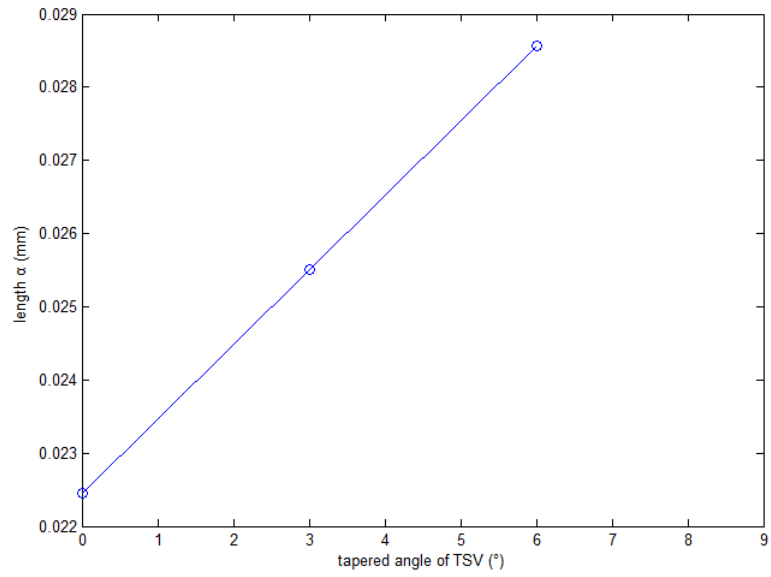
Figure 55: The characteristic length α with respect to the angle of tapered TSV when the base radius is fixed at 10 μm.
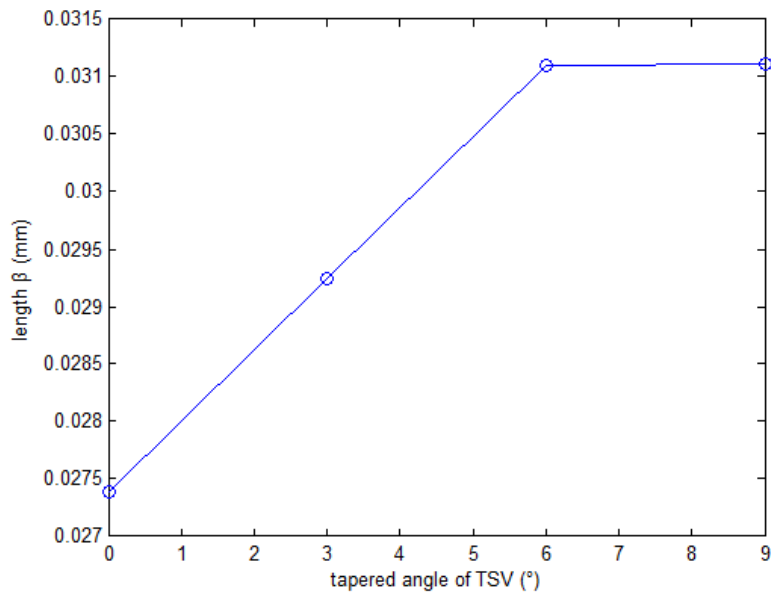
Figure 56: The characteristic length β with respect to the angle of tapered TSV when the base radius is fixed at 10 μm.

Figure 55 and Figure 56 show the characteristic lengths α and β, respectively, as a function of taper angle when the base radius of the TSV is fixed at 10 μm. In both cases, the KOZ characteristic length increases linearly with the angle from 0° to 6°. Beyond 6°, however, the length α could not be used to quantify the size of KOZ, because it is out of domain, while for length β, it remains relatively constant.

Figure 57 shows a comparison of mobility change contour plots for p-MOSFET aligned along the [010] channel direction.
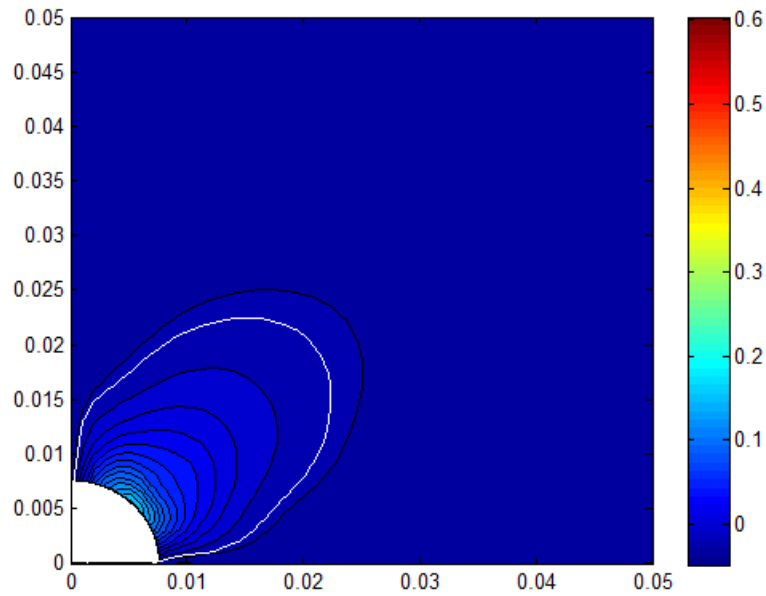
(a)
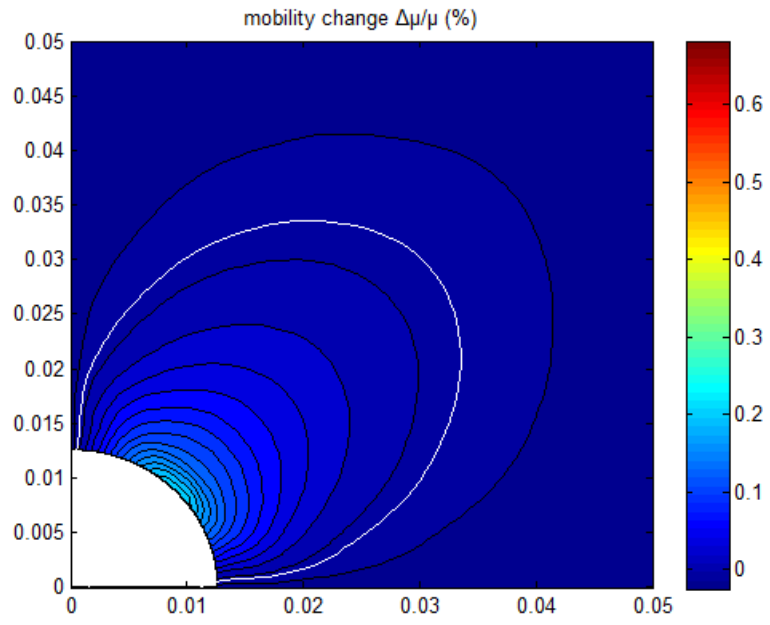
(b)
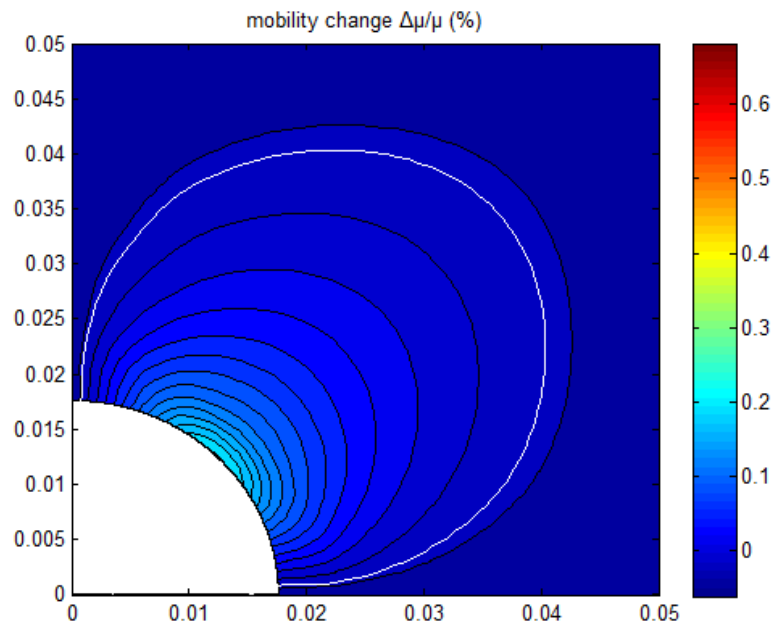
(c)
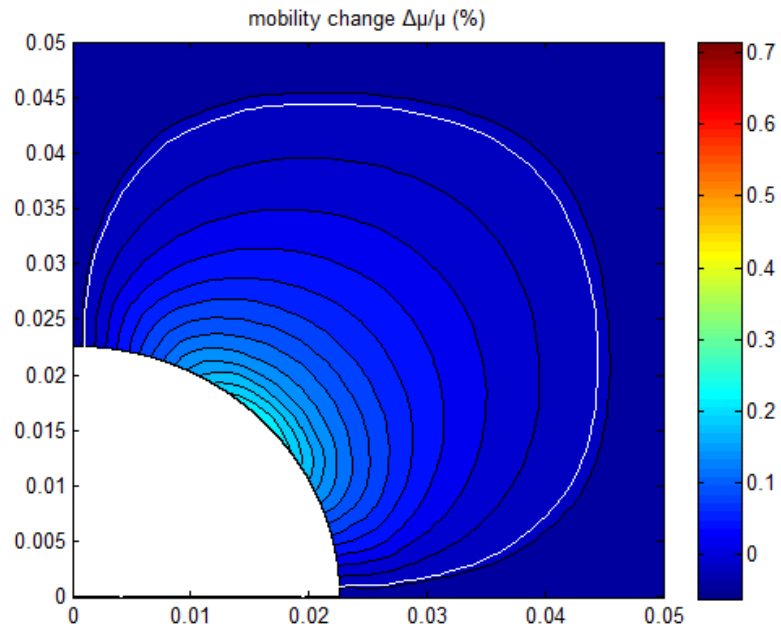
(d)
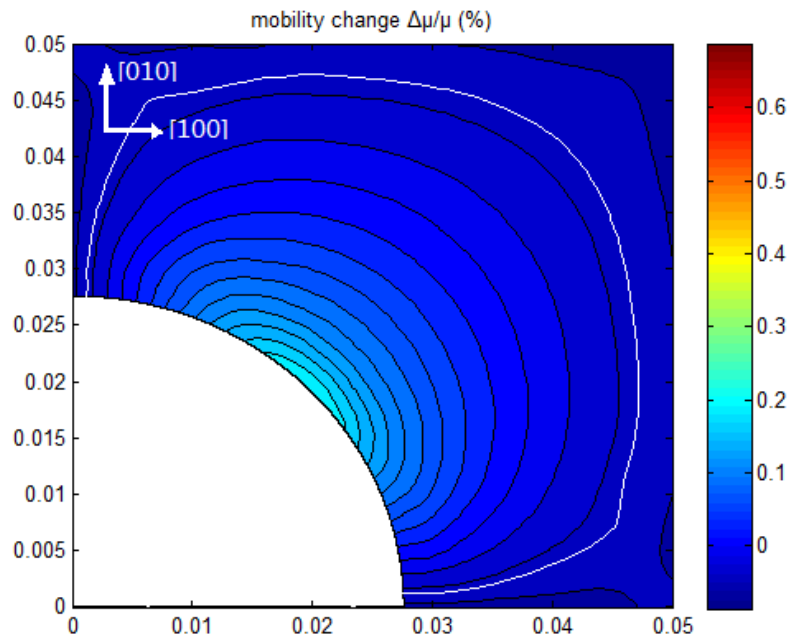
(e)

Figure 57 Comparison of mobility change contour plots for p-MOSFET aligned along the [010] channel. The model represents a quarter of a TSV unit cell in the 50 μm thickness

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isotropic silicon wafer. The TSV structures have (a) 5 µm, (b) 10 µm, (c) 15 µm, (d) 20 µm, and (e) 25 µm base radii and a fixed 3° tapered profile.

Figure 58 shows the length β with respect to the base radius of the TSV when the angle of tapered TSV is fixed at 3°. It can be seen that the KOZ size first increases with the TSV size and then decreases when the TSV base radius is beyond 15 µm. It is noticed that when the TSV base radius is greater than about 15 µm, the KOZ becomes large enough that practically no transistors should exist on the silicon wafer surface for this p-MOSFET [010] channel configuration.
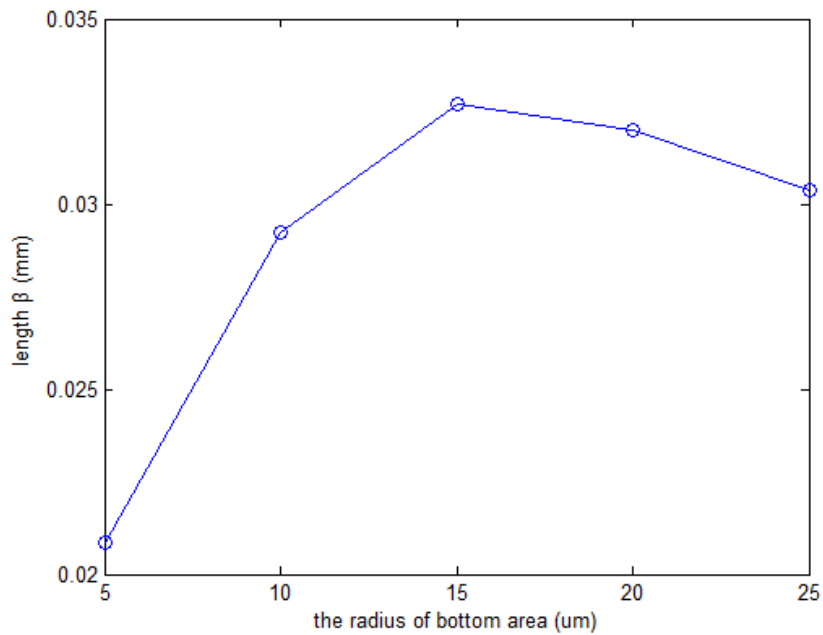
Figure 58: The characteristic length β with respect to the base radius of the TSV when the angle of tapered TSV is fixed at 3°.

Chapter 6

Conclusions

The key finding of this thesis is that the tapered TSV can cause wafer warpage under thermal loading. In order to quantify the wafer curvature, a large number of simulations with different TSV geometries were performed by FEA software package. It was found that the CTE mismatch-induced stresses increase linearly with the angle and the radius of the tapered TSV. The resulting wafer curvature is also proportional to the angle and the radius of the tapered TSV, as well as to the temperature change involved during the thermal loading process. The internal thermal stresses were found to be much higher than those caused by mechanical bending, under the same extent of overall wafer curvature. Incorporation of intermediate layers between copper and silicon into the model leads to higher local stresses, but the curvature remains relatively unchanged. The effect of anisotropic elastic property of silicon is also studied. The stresses are highly dependent on the orientation of silicon. The curvature of the anisotropic silicon wafer is only slightly lower than the isotropic counterpart. The wafer thickness and interspacing between adjacent TSVs were also found that can affect the curvature. In general, a thicker wafer and farther spaced TSVs tend to reduce the warpage, because a greater silicon volume enhances the stiffeness of the wafer matrix.

Due to piezoresistivity, the thermal-mismatch-induced stress can change the carrier mobility and degrade the performance of MOSFET devices. The n-MOSFET and p-MOSFET devices along with two channel directions were taken into account. The KOZ is

defined based on the critical 5% carrier mobility change. The sizes of KOZ in different models were quantified. The effect of piezoresistivity was found to be much more prominent for n-MOSFET along with the [100] channel and p-MOSFET along with the [010] channel. The KOZ size of n-MOSFET along with the [100] channel direction and p-MOSFET along with the [010] channel direction can be significantly affected by the taper angle and the size of the TSV.

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