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Room temperature operational single electron transistor fabricated by focused ion beam deposition

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We present the fabrication and room temperature operation of single electron transistors using 8 nm tungsten islands deposited by focused ion beam deposition technique. The tunnel junctions are fabricated using oxidation of tungsten in peracetic acid. Clear Coulomb oscillations, showing charging and discharging of the nanoislands, are seen at room temperature. The device consists of an array of tunnel junctions; the tunnel resistance of individual tunnel junction of the device is calculated to be as high as 25.13 GΩ. The effective capacitance of the array of tunnel junctions was found to be 0.499 aF, giving a charging energy of 160.6 meV. © *2007 American Institute of Physics.* [DOI: 10.1063/1.2761837]

I. INTRODUCTION

Single electron transistors (SETs), operating on the principle of Coulomb blockade (CB) in nanostructures, are promising candidates for future ultralow power and high density integrated devices.[1–5] SETs can be potentially used as electron pumps[6,7] for the transfer of one electron at a time and as electrometers.[8] Despite the observation of single electron charging effects a quarter century ago[9] the progress toward SETs operating at room temperature has been rather slow.[10,11] For room temperature operation, which is a critical requirement for practical applications, the capacitance of the SET device needs to be of the order of attofarads, thus limiting the dimension of the quantum confining islands below 10 nm. Fabrication of uniform-sized, sub-10 nm quantum confining islands in a device configuration has been a major challenge in the progress of SET technology. Different methods, such as the oxidation, anisotropic wet etching, scanning tunneling microscope nano-oxidation and, side gate on thin silicon-on-insulator (SOI) substrates, have been used in the past to fabricate low-dimension quantum islands in SET devices.[12] Here, we present an approach to fabricate SETs using tungsten islands that exhibit excellent room temperature operation. The key to our approach has been the application of the focused ion beam (FIB) deposition technique to create nearly uniform size nanoislands. Our fabrication method has allowed us to deposit nanoislands with a diameter of ~8 nm. Although the size of the deposited islands varied substantially in the present work, FIB technology shows the potential for better control of the deposited island size. The large value of the tunnel resistance coupled with the small island size assures room temperature operation of the device.[13] The *I-V* characteristics of the device show the CB and Coulomb oscillations (COs) at room temperature.

II. EXPERIMENT

The devices were fabricated on a Si substrate of dimensions 0.5×0.5 cm^2. The substrates were cleaned in a solution of H_2O_2 and H_2SO_4 in a 1:1 ratio (piranha solution) to remove any surface contaminants. The samples were rinsed in de-ionized water and dried in a nitrogen ambient. Subsequently, a thin film of Al_2O_3 was deposited on the silicon wafer in a Perkin-Elmer 2400-8J parallel plate rf sputtering system. This oxide layer isolates the device from the substrate; the thickness of the Al_2O_3 was 300 nm. The silicon wafer having Al_2O_3 thin film was then introduced into the Hitachi 2000A FIB system. The Hitachi 2000A FIB system has a selection of beams with different apertures.[14] Among the beams available, the beam MI-200 has a beam aperture of 200 μm; the beam current for MI-200 is 2.0–3.5 nA. Using the MI-200 beam, tungsten nanoparticles with an average diameter of 8 nm were deposited on the Al_2O_3 thin film on an area of 16×16 μm^2. The tungsten nanoparticles deposited by the FIB system are shown in the scanning electron microscopy (SEM) micrograph in Fig. 1. The nanoparticles are deposited in a random arrangement over the 16×16 μm^2 area due to the competition between deposition and sputter etch. Efforts to realize single dot systems using FIB deposition are in progress. Single dot SET structures were realized in Ni using FIB etching.[15] The minimum island size by FIB etching was limited to 45 nm and hence could not result in room temperature operation. The sample with the deposited tungsten nanoparticles was placed in piranha solution for the duration of 30 s to further reduce the size of the deposited nanoislands and their capacitance. The tungsten nanoparticles were then oxidized in peracetic acid, which is a combination of H_2O_2 and acetic acid, in a volume ratio of 1:1 for 4 min. Peracetic acid, being a strong oxidizing agent, oxidizes the surface of the tungsten nanoparticles, forming a thin layer of tungsten oxide. The tunnel junctions
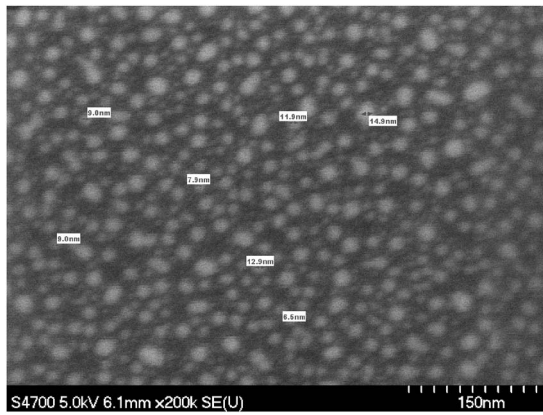
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FIG. 1. Tungsten nanoparticles fabricated by FIB deposition. The average particle diameter is 8 nm.

for the SET were fabricated during the chemical oxidation of tungsten. After a thorough clean in de-ionized water, the samples were introduced into the Hitachi 2000A FIB system to fabricate the connecting nanoleads and the microscale probing pads for the device. These electrodes and pads shown in Fig. 2 can also be fabricated by microfabrication techniques capable of 50 nm features. The dimensions of the probing pads for the device are 100×100 μm^2 and the nanoscale connecting leads from source, drain, and gate terminals are 50 μm in length and have a width of 250 nm. The protruding structures on the source and drain nanoscale leads have dimensions of 1 μm in length and 250 nm in width. The nanoscale tunnel leads and the probing pads for the device were also fabricated by FIB deposition, where a beam with an aperture of 50 μm was used. After the deposition of the pads and the nanoscaled leads, a thin film of Al_2O_3 having a thickness of 30 nm was sputtered on the sample. This oxide film of 30 nm acts as a passivating layer for the device. A SEM micrograph of the fabricated SET structure is shown in Fig. 3. The inset of Fig. 3 shows the active area after the oxidation of the nanoparticles. The fabricated device consists of an array of tunnel junctions between the leads. From measured average size and spacing between the nanoislands, we estimate that approximately 20 tunnel junctions per device are formed. The active area in this SEM micrograph was
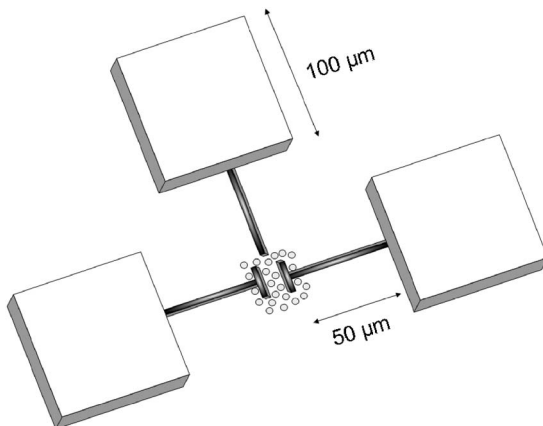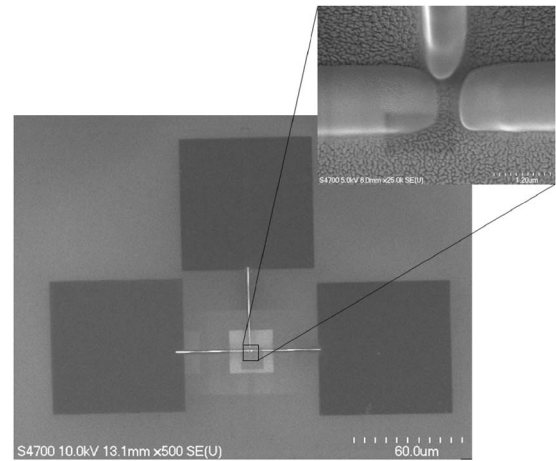

FIG. 3. SEM micrograph of the FIB deposited SET structure prior to the sputter deposition of the passivating layer. The inset in the figure shows the active area of the device; the measured device has protruding structures near the source-drain terminals.

imaged prior to the sputter deposition of the passivating layer. The device tested incorporates broad electrodes with a length of 1 μm and a width of 250 nm at the source and drain terminals, as shown in Fig. 2. After the deposition of the blanket passivating layer of Al_2O_3, the sample was introduced in the Hitachi 2000A FIB system to expose the probing pads under the Al_2O_3 thin film. The Al_2O_3 oxide above the probing pads was etched using the beam with a current of 4.0–8.0 nA. The etch time for each pad was 10 min for the oxide of 30 nm thickness. The I-V characteristics of the fabricated SET devices were measured in a custom-built vacuum probe chamber interfaced with a Keithley 4200-SCS system. The I-V measurements were performed at room temperature (298 and 293 K).

III. RESULTS AND DISCUSSION

The room temperature current-voltage (I-V) characteristics of the device with the source-drain voltage (V_{sd}) swept from -3.0 to $+3.0$ V at the gate bias (V_g) of -3.0 V and 33.3 mV are shown in Fig. 4. It can be seen from the nonlinear I_d-V_{sd} characteristics of the device in Fig. 4 that the Coulomb blockade is clearly visible for the gate voltage bias

FIG. 2. Top view of the device architecture. The source and drain terminals have protruding structures near the quantum dot islands.
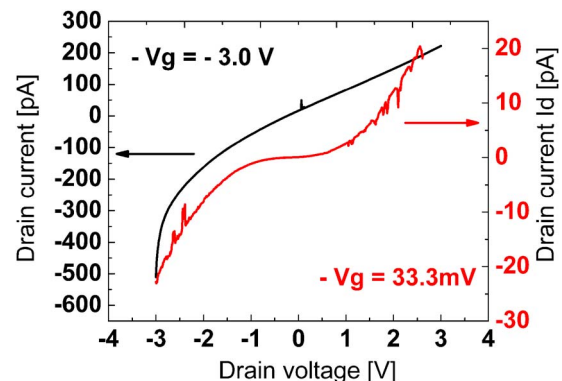

FIG. 4. (Color online) Source-drain characteristics of SET device at room temperature. Coulomb blockade is clearly visible for a lower gate bias of 33.3 mV.
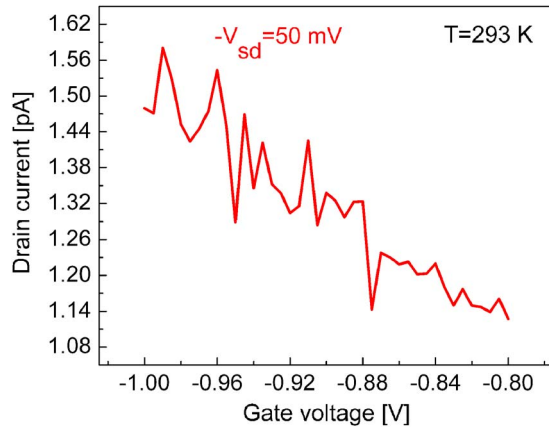
FIG. 5. (Color online) Periodic Coulomb oscillations measured at room temperature for a source-drain voltage of 50.0 mV.

of 33.3 mV. For a higher gate voltage of −3.0 V, the Coulomb blockade is not prominent. The drain current of the device is on the order of picoamperes, and the magnitude of the drain current changes by two orders of magnitude for a change of 3.3 V in gate bias.

Figure 5 shows the Coulomb oscillations in the device with respect to the gate voltage V_g. The V_g was swept from −1.0 to −0.8 V for a fixed V_{sd}=50.0 mV. The Coulomb oscillations are visible for the applied source-drain voltage; the drain current, which is in the picoampere range, oscillates periodically with the increase in the gate bias, showing clearly that the oscillations arise from the confinement of electrons on the tungsten quantum islands. Figure 6 shows the conductance oscillations for V_g swept from −1.0 to −0.4 V for a V_{sd} of 50.0 mV. It can be seen that the conductance of the SET oscillates periodically with the gate voltage, confirming the Coulomb oscillations at room temperature.

For a multiple-junction device, the device parameters can be calculated from the measured data using "orthodox theory."[16] Utilizing the measured average size of the nanoislands (∼8 nm) and the spacing between source and drain terminals, we estimate that the device consists of an array of 20 tunnel junctions. Assuming that the tunnel junctions
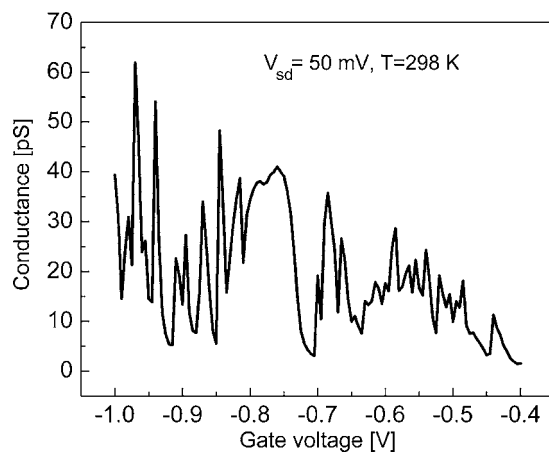
within the SET device have the same resistance and capacitance, we can calculate the charging energy of the device according to[17]

$$\Delta G/G_T = (E_c/3k_BT)[(N-1)/N], \tag{1}$$

where E_c is the charging energy $E_c=e^2/2C^*$, C^* is the capacitance of the array, N is the number of junctions in the array, ΔG is the dip in the measured conductance around zero source-drain bias of the device, and G_T is the asymptotic conductance at large positive and negative source-drain biases of the device measured. The capacitance per junction C is related to the total capacitance C^* as[18] $C^*=NC/[2(N-1)]$. The dip in the normalized conductance as measured from the conductance of the device is 0.978, which gives a charging energy of the device, $E_c=160.0$ meV. This gives an effective capacitance, C^*, of the device=0.499 aF, and the capacitance of the individual junction, $C=0.947$ aF. The value of the measured E_c (=160 meV) is six times higher than the room temperature thermal energy, which allows the observation of the Coulomb oscillations at room temperature, as reported here. The resistance of the tunnel junctions, which is related to the charging energy, the temperature of operation, and the number of tunnel junctions in an array,[19] is calculated to be 25.13 GΩ per tunnel junction.

IV. CONCLUSIONS

An approach based on FIB deposition technique was developed to fabricate SETs operating at room temperature. The SETs were fabricated with tungsten islands having an average diameter of less than 8 nm. The connecting leads and the measuring pads for the device were also fabricated with tungsten using FIB deposition technique. The fabricated SET devices clearly show Coulomb blockade and Coulomb oscillations at room temperature. The SET device consists an array of tunnel junctions. The resistance per tunnel junction of the device is calculated to be 25.13 GΩ, which is over five orders of magnitude higher than the quantum resistance (26.0 kΩ), thus enabling the confinement of electrons to the tungsten quantum dots. The effective capacitance of the device is estimated to be 0.499 aF, which gives the capacitance of individual tunnel junction ∼0.947 aF and a charging energy of the device ∼160.6 meV. The estimated E_c is much higher than the thermal fluctuations at room temperature, resulting in the observation of Coulomb oscillations even at room temperature.

FIG. 6. Room temperature conductance oscillations of SET for a source-drain bias of 50.0 mV.

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