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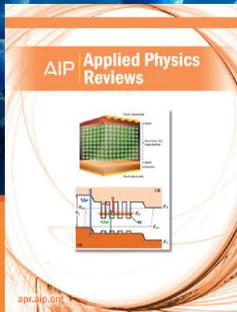Appl. Phys. Lett. **81**, 733 (2002); 10.1063/1.1492318

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Simulation of charge transport in multi-island tunneling devices: Application to disordered one-dimensional systems at low and high biases

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Although devices have been fabricated displaying interesting single-electron transport characteristics, there has been limited progress in the development of tools that can simulate such devices based on their physical geometry over a range of bias conditions up to a few volts per junction. In this work, we present the development of a multi-island transport simulator, MITS, a simulator of tunneling transport in multi-island devices that takes into account geometrical and material parameters, and can span low and high source-drain biases. First, the capabilities of MITS are demonstrated by modeling experimental devices described in the literature, and showing that the simulated device characteristics agree well with the experimental observations. Then, the results of studies of charge transport through a long one-dimensional (1D) chain of gold nano-islands on an insulating substrate are presented. Current-voltage (IV) characteristics are investigated as a function of the overall chain-length and temperature. Under high bias conditions, where temperature has a minimal effect, the IV characteristics are non-Ohmic, and do not exhibit any Coulomb staircase (CS) structures. The overall resistance of the device also increases non-linearly with increasing chain-length. For small biases, IV characteristics show clear CS structures that are more pronounced for larger chain-lengths. The Coulomb blockade and the threshold voltage (V_{th}) required for device switching increase linearly with the increase in chain length. With increasing temperature, the blockade effects are diminished as the abrupt increase in current at V_{th} is washed out and the apparent blockade decreases. Microscopic investigations demonstrate that the overall IV characteristics are a result of a complex interplay among those factors that affect the tunneling rates that are fixed *a priori* (island sizes, island separations, temperature, etc.), and the evolving charge state of the system, which changes as the applied source-drain bias (V_{SD}) is changed. In a system of nano-islands with a broad distribution of sizes and inter-island spacings, the applied bias is divided across the junctions as one would expect of a voltage divider, with larger potential drops across the wider junctions and smaller drops across the narrower junctions. As a result, the tunneling resistances across these wider junctions decrease dramatically, relative to the other junctions, at high V_{SD} thereby increasing their electron tunneling rates. IV behavior at high V_{SD} follows a power-law scaling behavior with the exponent dependent on the length of the chain and the degree of disorder in the system. © 2013 AIP Publishing LLC. [http://dx.doi.org/10.1063/1.4821224]

I. INTRODUCTION

With major functional issues confronting the scaling of dimensions in the mainstream metal oxide semiconductor field effect transistor (MOSFET) devices, such as gate leakage, power dissipation, quantum effects such as tunneling current, and non-deterministic behavior of charge transport, researchers have been exploring single-electron transport as one of several possible nano-scale technologies to overcome the challenges resulting from technology scaling of MOSFETs.

Single-electron devices (SEDs) consist of one or multiple nanometer-size islands or quantum dots made of metallic or semiconducting materials deposited between the two metallic source and drain electrodes, forming a one-dimensional (1D) or a multi-dimensional (2D or 3D) device structure. The islands are isolated from one another by a dielectric material such as an oxide or a nitride that forms the tunnel junctions. The overall device current depends on the individual junction currents that flow between pairs of nano-islands through the tunnel junction between the two islands. SEDs operate on the principle of a Coulomb blockade wherein the tunneling of electrons through the tunnel junction is suppressed at low bias voltages and low temperatures giving them unique non-Ohmic properties such as staircase IV characteristics. Coulomb blockade characteristics are a manifestation of charging effects of the nanometer-size islands. Many research groups have been working on different aspects of experimental SEDs and their applications. In a few cases, devices have been fabricated with just a single-island displaying clear Coulomb staircases at room temperature.[1] On the other hand, multiple-island devices that show a large blockade potential at room temperature useful for switching in multiple-level logic have also been demonstrated.[2]

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Single-electron transistor (SET) devices have been explored to demonstrate their use as single-electron memory devices at room temperature[3] while low power consumption and strong charge sensitivity make SET devices potential candidates for sensing and ULSI based applications.[4] SETs have been used for nanometer-scale displacement sensing[5] while SEDs made up of arrays of tunnel junctions have been used in thermometry that could substitute the commercially available field independent resistance and capacitance thermometers.[6]

While intense experimental research has been ongoing, continued development of robust simulation tools has been lacking for multi-island SED devices. A few fairly robust tools have been developed for the simulations of SED and SET circuits[7–11] for which independent knowledge of the electrical circuit parameters, namely, junction resistances and capacitances, is required. The utility of these tools is rather limited for studying SEDs as a function of more direct physical characteristics such as geometrical structures (e.g., the shapes, sizes and spacing of the islands, and some degree of randomness in these parameters), and the material properties of the constituent parts (e.g., the work functions of the islands, the dielectric properties of the substrate and the tunnel junctions, etc). Furthermore, in multiple-island systems, the tunneling resistances of the junctions are not fixed but are expected to change with the voltage drops across the junctions that continuously change during the course of the simulation. It is therefore desirable to develop a physical model of SEDs that takes into account the geometrical structure of island arrays, disorder in the system, the material properties, and the state-dependent tunneling resistances.

In this paper, we discuss the development of a new multi-island transport simulator, MITS, that can simulate multi-island SED behavior based on physical models, rather than circuit models of a device. Like other tools, it can also be used for circuit simulations of SEDs if the circuit parameters are known. On the other hand, unlike other tools, dynamically varying tunneling resistances, non-ideal behaviors and non-uniform geometries can be successfully modeled with MITS, providing strong linkage between the physical characteristics of the system and the resulting SED device *IV* characteristics.

To demonstrate its capabilities and its accuracy, we first present comparisons of results from simulations with those for experimental devices described in literature.[1,12] The bulk of this paper focuses on MITS studies of charge transport through a long one-dimensional chain of gold nano-islands deposited on an insulating substrate. The effects of chain-length and temperature on the device characteristics are presented and compared with experimental results by Lee *et al.*[13] Finally, we briefly discuss extensions of our simulation model to two-dimensional systems of various geometries and the inclusion of a gate electrode.

II. THEORY AND SIMULATION

A. Theoretical model

For our initial investigations, we focus on one-dimensional systems. In particular, we first study a model device consisting of chains of up to 199 gold islands (200 junctions) deposited on an insulating wire between source and drain electrodes. The geometry of this system is related to recent experimental work by Lee *et al.*[13] for gold islands deposited on insulating multi-walled boron-nitride nanotubes. The radius of each island is randomly selected to be between 3 and 10 nm, while the junction widths are randomly chosen to be between 1 and 5 nm. A fixed island at the end of the chain is selected as the drain electrode, while the source (ground) electrode is chosen from among the remaining islands in the chain according to the desired number of islands in the system (chain).

For a given voltage across the source and drain electrodes, the current through the device is computed using kinetic Monte Carlo (KMC) simulation methods[14,15] based on computed electron tunneling rates across the junctions. The various tunneling probabilities at any given time depend on the charge states of the islands, the voltage drops across junctions, and their tunneling resistances. Unlike most models, the tunneling resistances are not fixed, but instead depend on the voltage drops across the junctions at any given time, as is described below.

For the calculation of the tunneling rates, we follow a semi-classical approach (orthodox theory), which assumes that (i) the energy spectrum of the conductive islands may be considered continuous (ii) the tunneling time is negligible compared to the time between tunneling events, and (iii) coherent tunneling events are ignored.[7,16] Condition (i) is a fair assumption taking into account the size and the metallic nature of the islands, which are expected to have sub-nanometer DeBroglie wavelength. For a pair of adjacent islands i and j, the tunneling rate is thus given by[7,16,17]

$$\Gamma_{ij}(\Delta W_{ij}) = \left(\frac{-\Delta W_{ij}}{e^2 R_{ij}}\right)\left[1 - \exp\left(\frac{\Delta W_{ij}}{k_B T}\right)\right]^{-1}, \quad (1)$$

where R_{ij} is the tunneling resistance of the junction, T is the temperature, e is the electron charge, k_B is the Boltzmann constant, and ΔW_{ij} is the change in the free energy of the system due to the tunneling event (see below).

The tunneling resistance of a junction R_{ij} plays a key role in determining the tunneling rate across a junction, as it depends exponentially on the separation d_{ij} and the height of the potential barrier between the two islands that form the junction. The barrier height is strongly influenced by the work function of the islands ϕ_i and ϕ_j and the potential drop V_{ij} across the two islands. It decreases approximately linearly from one island to the next given by $\phi_{eff}(x) = \phi_i - (\phi_i - \phi_j + eV_{ij})\frac{x}{d_{ij}}$, where x is the distance from the barrier interface. Since all of the islands in this case are of gold, $\phi_i = \phi_j = \phi$ and $\phi_{eff}(x) = \phi - (eV_{ij})\frac{x}{d_{ij}}$. If the drop V_{ij} is small compared to ϕ, it has a negligible effect on the barrier height and R_{ij} remains constant. Under simulation conditions in which all the junction resistances in a given chain remain constant, the device *IV* characteristics follow a linear behavior for large source-drain voltage biases. However, where there is a large charge build up or under large source-drain biases, the potential difference between the neighboring islands can be significant compared to the work function, leading to significant band bending. As a

result, the effective barrier height would strongly depend on V_{ij}. To simplify the calculations, the tunneling barrier is taken to be of constant height across the width of the junction, but with a reduced height whose variation is given by $\phi_{eff}(x) = \phi_{eff} = \phi - eV_{ij}/2$. This is a reasonable approximation as long as the V_{ij} does not exceed ϕ.[18] Tunnel resistances also depend on other system parameters like the Fermi energies E_F and the island radii. Approximate values of E_F and ϕ for gold have been chosen as 5.5 eV and 4.8 eV, respectively. Thus the tunneling resistance is given by[19]

$$R_{ij} = \left(\frac{h^3}{64\pi^2 m_e e^2}\right)\left(\frac{E_F + \phi_{eff}}{E_F}\right)^2 \frac{\exp(2\beta k_0 d_{ij})}{\phi_{eff}}\left(\frac{\beta k_0}{r_a}\right)\frac{1}{G_{ij}},$$

(2)

where $k_0 = (2\pi/h)(2m_e\phi_{eff})^{1/2}$, h is the Planck constant, and m_e is the free electron mass. β is an enhancement parameter that was taken to be 0.115 to set an overall current scale comparable to that measured by Lee *et al.*[13] The average radius of the two spherical islands forming the junction is r_a, and d_{ij} is the closest distance between their surfaces (the junction width). G_{ij} is a purely geometrical factor that takes into account the solid angle subtended by one spherical island at the other across the tunnel junction when considering the current flux and is given by[19]

$$G_{ij} = 1 - \left(1 - \left\{\frac{r_a}{(r_a + d_{ij})}\right\}^2\right)^{\frac{1}{2}}.$$

(3)

The change in free energy due to the transition is given by,

$$\Delta W_{ij} = -eV_{ij} + E_{c,ij}.$$

(4)

ΔW_{ij} depends on the potential drop V_{ij} across the junction before the transition, which is influenced by the capacitances of the system and the charge state of the system. The charge present on the island is influenced by the discrete charge tunneling to or from the island, continuous charge induced by an external electrode such as a gate, or a background charge. Background charge is any charge that may exists in the form of charged impurities or traps that can influence the current flowing through the device. Background charge can also be caused by parasitic and stray capacitances that may induce charges on the nanoislands. $E_{c,ij}$ is the junction charging energy, which is the energy required for a single electron transition across a junction between the two coupled islands, as determined by all of the capacitances of the system.[7,16,17] An analytical method employing image charges was used for the calculation of junction capacitances C_{ij} between neighboring islands.[20,21] Using this method, the junction capacitances are given by

$$C_{ij} = 4\pi\varepsilon\varepsilon_0 \frac{r_i r_j}{d_{c,ij}}(\sinh x)\sum_{n=1}^{\infty}(\sinh nx)^{-1},$$

$$\text{where}\quad x \equiv \cosh^{-1}\left[\frac{d_{c,ij}^2 - (r_i^2 + r_j^2)}{2r_i r_j}\right],$$

(5)

where r_i and r_j are the radii of the respective islands forming the junction, and $d_{c,ij}$ is the center-center distance between them. ε is the dielectric constant of the junction material (taken as 1 here) and ε_0 is the vacuum permittivity. The number of image charges n required for good convergence consistent with the boundary conditions depends on the ratio of junction width to the radius of the spheres (d/r).[20] For the system studied here, 100 to 125 image charges were found to be sufficient for good convergence. In addition to the junction capacitances, the charging energy also depends on the self-capacitances of the island given by $C_{self}^i = 4\pi\varepsilon\varepsilon_0 r_i$.

A capacitance matrix is built by setting up a matrix equation $\boldsymbol{Q} = \boldsymbol{CV}$, where any diagonal element of the capacitance matrix C_{ii} is the sum of all capacitances associated with the respective island i, and the off-diagonal elements C_{ij} are the negative of inter-island capacitances. Since the potential matrix $\boldsymbol{V}$ consists of the known electrode potentials and the unknown island potentials, the capacitance matrix $\boldsymbol{C}$ is resolved into two parts, one that couples the island charge matrix to the known electrode potential matrix and the other that couples the island charge matrix to the unknown island potential matrix.[16] The matrix equation is then solved for the island potentials that are updated with each new charge state of the system. The kinetic Monte Carlo method used for computing the device current is a stochastic technique based on random number and probability statistics theory that is employed for simulating complex dynamical systems.[14,15] The method uses the n-fold way algorithm wherein the system evolves with time based on the transition rates in the system, computed as outlined above.

B. Simulation flow

A comprehensive set of Monte Carlo simulation codes called MITS has been developed in MATLAB® to carry out the simulations. The workflow of MITS is shown in Fig. 1. First, a physical model of the device is generated using hard-sphere Metropolis Monte Carlo simulation to generate a configuration of spherical islands with desired mean density (linear or areal in 1D or 2D, respectively), and randomized distribution of sizes and spacings. For the 1D systems of interest in this paper, the capacitances are calculated using the analytical approach described above. A finite-element-method (FEM) of calculating the capacitances has been developed (to be published) for systems composed of a 2D array of islands. The circuit-matrix solver builds capacitance matrices that couple the varying island charges to the varying island potentials and the fixed electrode potentials (see Sec. II A). With the capacitance matrices known, the charging energies for the transfer of a single electron are calculated across all the junctions in a given chain. For the given fixed electrode potentials and the known island charges (taken to be zero in the initial system configuration), the island potentials are then determined. The adaptive tunnel resistance solver computes the tunneling resistances across all the nearest-neighbor junctions. In a quasi-2D system, resistances are computed of only those junctions whose widths are smaller than a pre-determined cut off. Once all the relevant parameters in the system are determined, tunneling rates
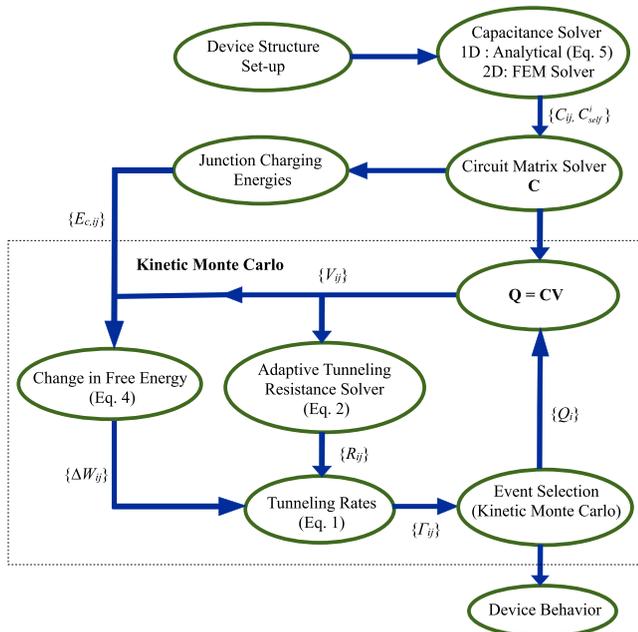
FIG. 1. Simulation flow diagram of MITS.

across the junctions are computed. Following the kinetic Monte Carlo method, a particular tunneling event is randomly selected from among the available events, and the corresponding transition is carried out. Once all the individual tunneling rates are known, the total tunneling rate and the lifetime of the current charge state are determined. After carrying out the transition, the charges on the islands and the time are updated. For the new system charge configuration, the potential drops, the tunneling resistances, and the tunneling rates across all the junctions are recalculated, and the process is repeated for large number of time steps until the current through the device reaches a steady state with satisfactory statistical accuracy.

The number of time steps required for satisfactory statistical convergence of the measured currents increases with the number of junctions in the chain as N^2. For the maximum chain-length $(N = 200)$ studied at $T = 0$ K, approximately 2×10^6 time steps were required to achieve a standard deviation of less than 5%. The number of time steps required increase substantially for non-zero temperatures, however. For example, the simulation time steps for a single point in the IV characteristic for a 100-junction device increased from $\sim 1 \times 10^6$ steps at $T = 0$ K to $\sim 5 \times 10^7$ steps at $T = 100$ K in order to achieve comparable precision in the current value. To increase the simulation speed, especially at higher temperatures, single program/multiple data (SPMD) parallel computing capabilities in MATLAB® have been built into the MITS tool.

C. Model testing

In order to test and validate MITS, three test studies are described in this section that compare experimental results for systems described in the literature with results for comparable MITS models. The first test demonstrates the capability of MITS in simulating a single-island device at non-zero

temperature wherein the IV characteristics show a clear Coulomb staircase.[1] The second test is carried out to show its capability in simulating transistor characteristics where the effect of a gate on the IV characteristics is studied for a single-island device.[1] The test also shows the effect of temperature on the observed gate oscillations.[1] The third test looks at a multi-island device wherein a 1D chain of 50 junctions is simulated. This chain is taken to represent one dominant conducting path in a multi-island multi-dimensional device with a distribution of sizes and spacings such as the device fabricated and studied by Parthasarathy *et al.*[12] The test also proves the accuracy of the physical model used for the calculations of different system parameters like tunneling resistances and capacitances and hence the device current in 1D and multi-dimensional multi-island devices.

1. Test 1

Single-island devices have been fabricated by Ray *et al.*[1] using gold nanoparticles that are positioned on the exposed sidewall of the dielectric film of silicon oxide that separates the source and drain electrodes forming a vertically self-aligned structure. The current flow takes place between the source and drain through a single nano-particle effectively forming a single-island device.

In order to simulate the corresponding device characteristics, the appropriate device parameters such as the capacitances, junction resistances, and the background charge along with the source-drain bias from Ref. 1 are given as input to MITS. The experimental device IV characteristics from Ray *et al.*[1] are shown in Fig. 2(a), along with simulation results they obtained using the code SIMON,[8,9] which uses a circuit model with fixed junction resistances and capacitances. In comparison, simulated device characteristics obtained using MITS are shown in Fig. 2(b). The scale of the current and key features, such as the Coulomb staircase step widths and the step positions, agree well with the experimental and SIMON results. The staircase structure is a manifestation of the charging effect due to the small size of the nano-island. With increasing bias, the step sharpness decreases and finally the steps disappear.

2. Test 2

A second test was carried out to demonstrate the capabilities of MITS in modeling SET characteristics, such as the device current modulation by gate bias and the thermal effect on gate oscillations. The SET device is fabricated by adding a gate electrode to the single-electron device architecture similar to the one used in test 1. The silicon oxide sidewall is surrounded by the gate electrode, forming a side gate structure. As in test 1, the device parameters from Ray *et al.*[1] are used for simulating the single-island device. Figure 3(a) shows the Coulomb staircase of the experimental device consisting of a single island and the effect of the side gate on the Coulomb staircase. The simulated device characteristics shown in Fig. 3(b) are in good agreement with the experimental characteristics. The positive gate bias shifts the blockade, showing its asymmetric nature about $V_{SD} = 0$. Besides shifting the Coulomb staircase, the gate appears to
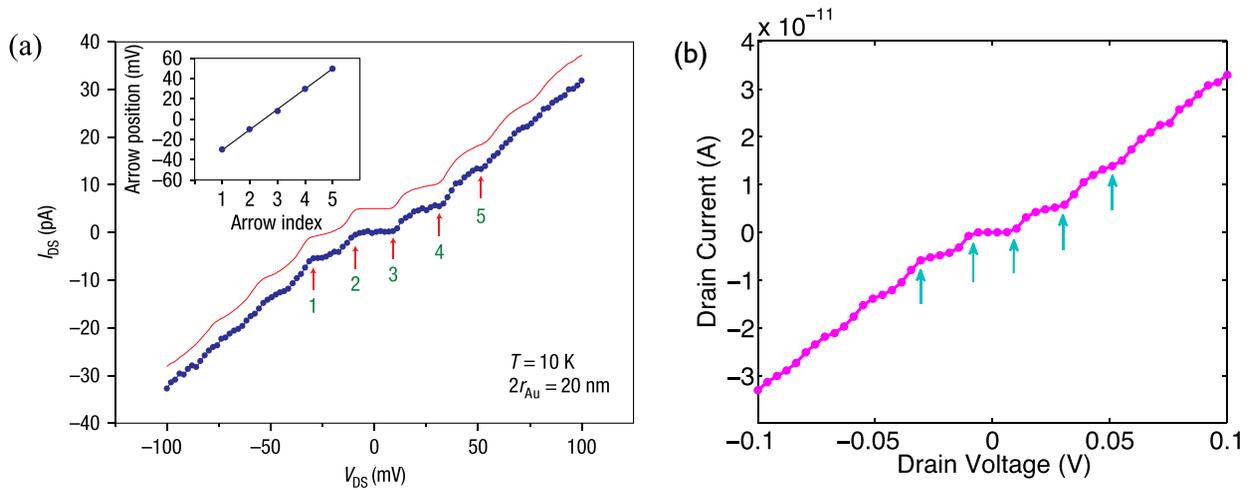
FIG. 2. (a) *IV* characteristics at $T = 10$ K of an experimental (dots in blue) single-island device comprised of a $\sim$20 nm colloidal gold particle, compared with simulation results using SIMON (solid line in red) by Ray *et al.*[1] V_{DS} is the source-drain voltage. Reprinted with permission from Ray *et al.*, Nat. Nanotechnol. **3**, 603–608 (2008). Copyright 2008 Macmillan Publishers Ltd. (b) Simulated *IV* characteristics at $T = 10$ K using MITS using the following parameters gleaned from Ref. 1: junction capacitances $C_1 = 7.30$ aF, $C_2 = 0.88$ aF, fixed tunneling resistances $R_1 = 2.05$ GΩ, $R_2 = 0.40$ GΩ, and background charge $Q_0 = 0.05\,e$. The source electrode is set to ground. Key characteristics (indicated by the arrows) and scales are in good agreement with Ref. 1.
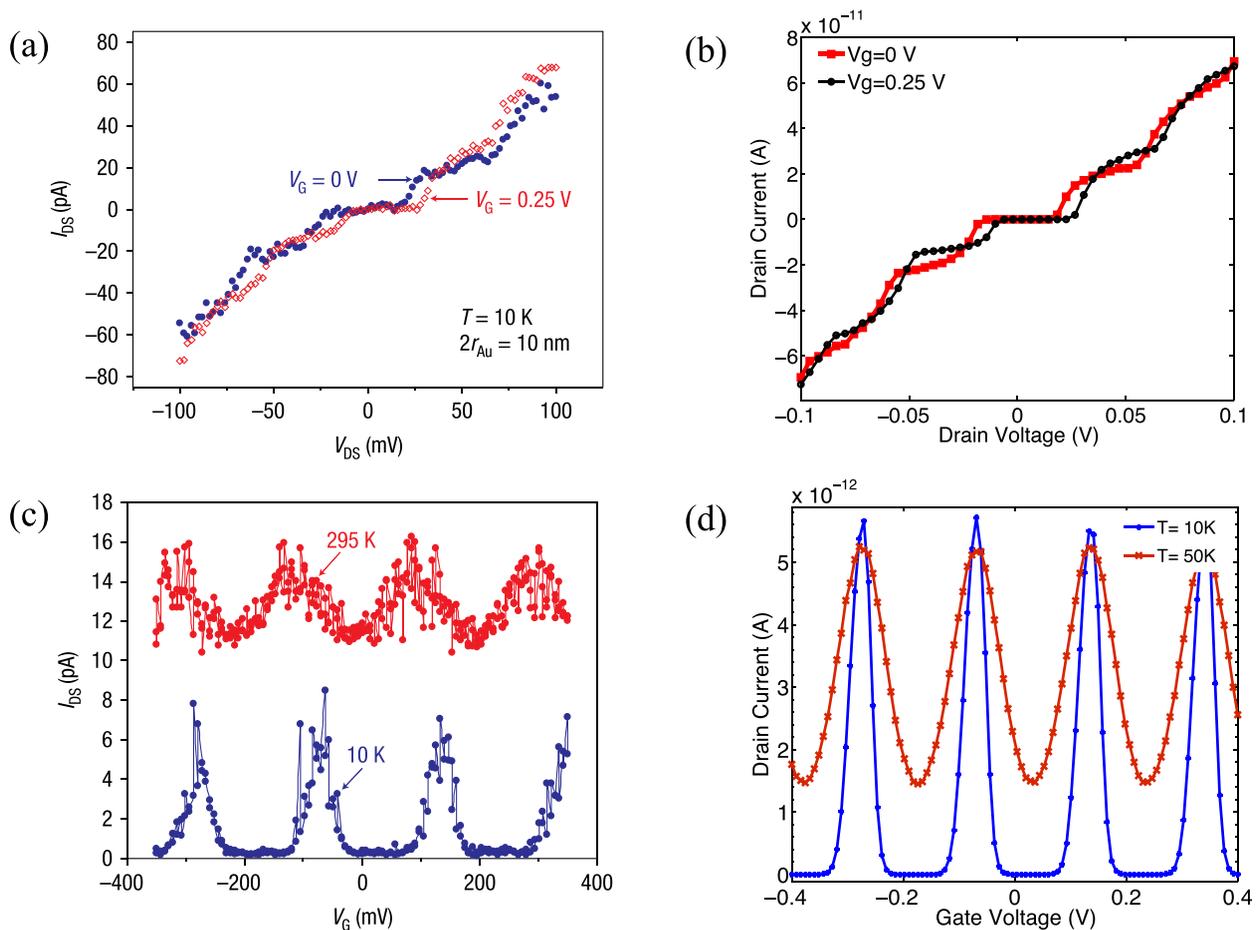

FIG. 3. (a) *IV* characteristics of an experimental single-island device comprised of a $\sim$10 nm colloidal gold particle for different gate biases. Reprinted with permission from Ray *et al.*, Nat. Nanotechnol. **3**, 603–608 (2008). Copyright 2008 Macmillan Publishers Ltd. (b) *IV* characteristics obtained by MITS using the same parameters as found in the experimental device. The gate bias shifts the Coulomb staircase without changing the blockade length. (c) Coulomb oscillations observed in an experimental single-island device comprised of a $\sim$10 nm gold particle at different temperatures and fixed $V_{SD} = 10$ mV. Reprinted with permission from Ray *et al.*, Nat. Nanotechnol. **3**, 603–608 (2008). Copyright 2008 Macmillan Publishers Ltd. Room-temperature data are shifted by 10 pA for clarity. (d) Simulated Coulomb oscillations using MITS at $V_{SD} = 10$ mV using the same parameters as in (c). Parameters used for (b) and (d) are junction and gate capacitances $C_1 = 3.4$ aF, $C_2 = 0.24$ aF, $C_g = 0.78$ aF, fixed tunneling resistances $R_1 = 0.79$ GΩ, $R_2 = 0.19$ GΩ and background charge $Q_0 = 0.05\,e$.

have an appreciable effect on the height of staircase steps. The steps are observed to be asymmetric about $V_{SD} = 0$ in the presence of gate. Figures 3(c) and 3(d) show Coulomb oscillations at different temperatures in the experimental and simulated devices, respectively, when the gate bias is varied at a fixed V_{SD}. Since there is only a single island, the oscillations are periodic with a period that depends on the gate capacitance. At higher temperatures, the current on/off ratio decreases with no appreciable change in the peak current. With increasing temperature, the period of the gate oscillations does not change but the oscillations begin to wash out due to thermal broadening, as can be seen in the increase in the oscillation peak width at higher temperature [Fig. 3(d)]. The experimentally measured Coulomb oscillations in Fig. 3(c) show a shift in peak positions between the two temperatures that is not evident in the simulation results in Fig. 3(d). Such a shift in peak positions is attainable in MITS simulations only by changing the background charge or the source-drain bias, but not by temperature changes alone. The peak shifts in Fig. 3(c) may therefore be due to slight differences in experimental conditions or perhaps capacitance changes due to thermal expansion of the device materials.

3. Test 3

Devices fabricated by Parthasarathy *et al.*[12] consist of monolayers of 1-dodecanethiol-ligated gold nanocrystals deposited on silicon substrates coated with a 100 nm thick layer of silicon nitride. The device has a quasi-two-dimensional structure in which the current paths are not expected to be straight but meander depending on the disorder in the system. The inter-particle current flow takes place through the 1-dodecanethiol ligands that act as mechanical spacer between the particles, and which modify the height of the tunneling barrier.[22] The device structure has a narrow distribution of island radii (2.2–2.8 nm) and junction widths (2.2–2.6 nm).

In a 2D system with a sufficiently broad distribution of junction widths, the majority of the device current might be expected to be carried by one dominant conducting path.[19] The number of current paths will increase as the distribution

becomes narrower. To demonstrate the simulator capability, the experimental device of Parthasarathy *et al.* has been modeled by simulating a random 1D chain representing a dominant current path, and using the same distributions of island radii and junction widths. The chain consists of 49 gold islands (50 junctions) that are expected to span the longitudinal length of the experimental device between the source and drain. The electron effective mass and the tunneling barrier height parameters for such a system are chosen from Ref. 23. The experimental and the simulated *IV* characteristics at $T = 12$ K are shown in Figs. 4(a) and 4(b), respectively. Since the experimental device is actually a two-dimensional structure having a relatively narrow distribution of junction widths, it is expected to have multiple current paths and thus higher current than would a single conducting path. Therefore, the experimental device current [Fig. 4(a)] is expected to be higher than the current through the simulated 1D device chain shown in Fig. 4(b). The existence of multiple current paths in a two-dimensional device will also wash out the discrete Coulomb staircase steps that are otherwise observed in a 1D chain. Multiple paths and capacitive effects from the other dimensions are expected to influence the Coulomb blockade and its sharpness at the threshold point. Despite these effects due to the dimensionality, the simulator gives a reasonable estimate of the current scale and the threshold voltage in the experimental device, thus validating its physical model.

III. RESULTS AND DISCUSSION

Having established confidence in MITS simulation, a detailed study was carried out on charge transport through a one-dimensional (1D) chain of gold nano-islands deposited on an insulating wire as illustrated in Fig. 5. The system is modeled by a chain of 199 spherical conductors (islands), with nearest neighbors separated by an insulating tunnel junction (vacuum). The radius of each island is randomly selected from a uniform distribution between 3 and 10 nm [Fig. 6(a)], while the junction widths are randomly selected from a uniform distribution between 1 and 5 nm [Fig. 6(b)]. A fixed island at the end of the chain is selected as the drain
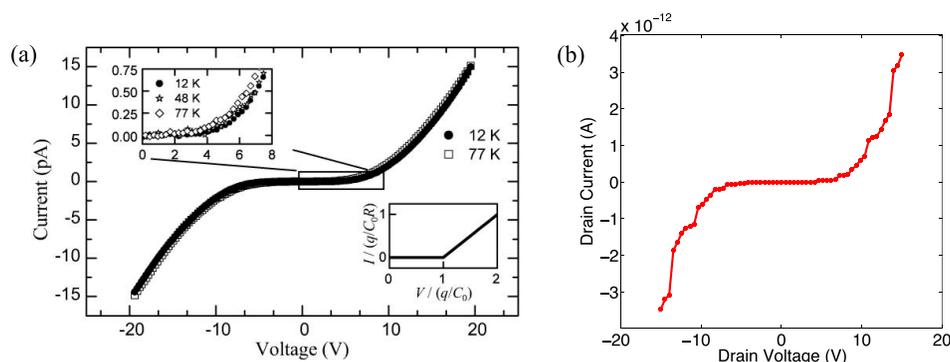

FIG. 4. (a) *IV* characteristics of a quasi-two-dimensional device consisting of gold nanocrystals with a narrow distribution of island radii (2.2–2.8 nm) ligated by 1-dodecanethiol, and with a narrow junction-width distribution of (2.2–2.6 nm). Reprinted figure with permission from Parthasarathy *et al.*, Phys. Rev. Lett. **87**, 186807 (2001). Copyright 2001 The American Physical Society. The magnified data in the inset give an estimate of the Coulomb blockade threshold voltage. (b) Simulated *IV* characteristics at $T = 12$ K using MITS of a 1D chain of gold nanocrystals ligated by 1-dodecanethiol having similar distribution. The current scale and Coulomb blockade fairly agree with those in (a). The source is set to ground. Multiple current paths in the experimental device are expected to drive up the current and wash out the staircase steps.
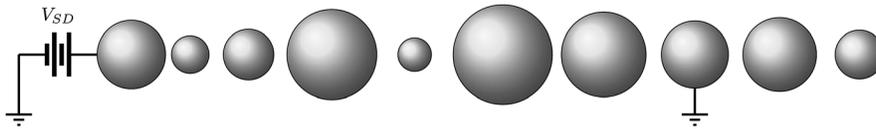
FIG. 5. Schematic of the geometrical model of a 1D chain of gold nano-islands deposited on an insulating wire used for the MITS simulation. The island radii and junction widths are randomly selected over uniform distributions to model the position of metallic islands in an experimental device fabricated by Lee *et al.*[13]
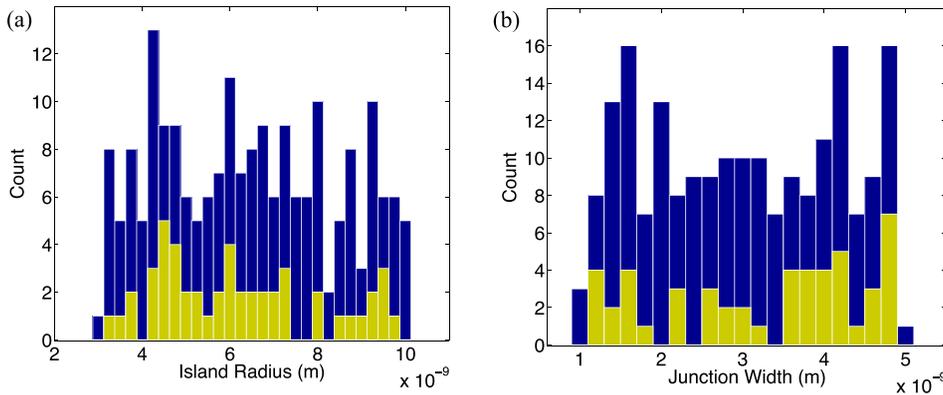

FIG. 6. (a) Distribution of radii of the islands along the chain of 50 junctions (yellow/light) and 200 junctions (blue/dark). (b) Distribution of widths of the junctions that couple the neighboring islands and through which the electron tunneling takes place. The 200-junction chain contains more large-width tunneling junctions, which play a dominant role in determining the device characteristics.

electrode, while the source (fixed to ground) electrode is chosen from among the remaining islands in the chain according to the desired number of islands in the system.

IV characteristics of the device at $T = 0$ K are as shown in Fig. 7 for a series of different source-drain gap lengths, with N ranging from 12 to 200 junctions. Under large source-drain biases (V_{SD}), the *IV* characteristics are non-Ohmic [Fig. 7(a)]. By conducting separate simulations in which the barrier heights did not vary with V_{ij}, it was determined that the non-Ohmic nature of the *IV* characteristics originates from the reduction in the potential barrier height of the junctions, $\phi_{eff}(x)$. The overall resistance of the device also increases non-linearly with increasing chain-length. *IV*

characteristics at low V_{SD} exhibit discrete Coulomb staircase structures that are the manifestations of charging effects on the individual islands [Fig. 7(b)]. Furthermore, the steps of the Coulomb staircase are more pronounced for longer chain-length devices. The first step, which rises at the threshold voltage V_{th}, represents the opening up of the first conduction channel (time sequence of charge states of the islands that occurs with a certain probability and evolves with a set of rates) that carries current across the entire length of the device. Each subsequent step represents opening of a new channel (a different time sequence of island-charge states that occurs with another probability and evolves with a different set of rates) when V_{SD} reaches subsequent critical
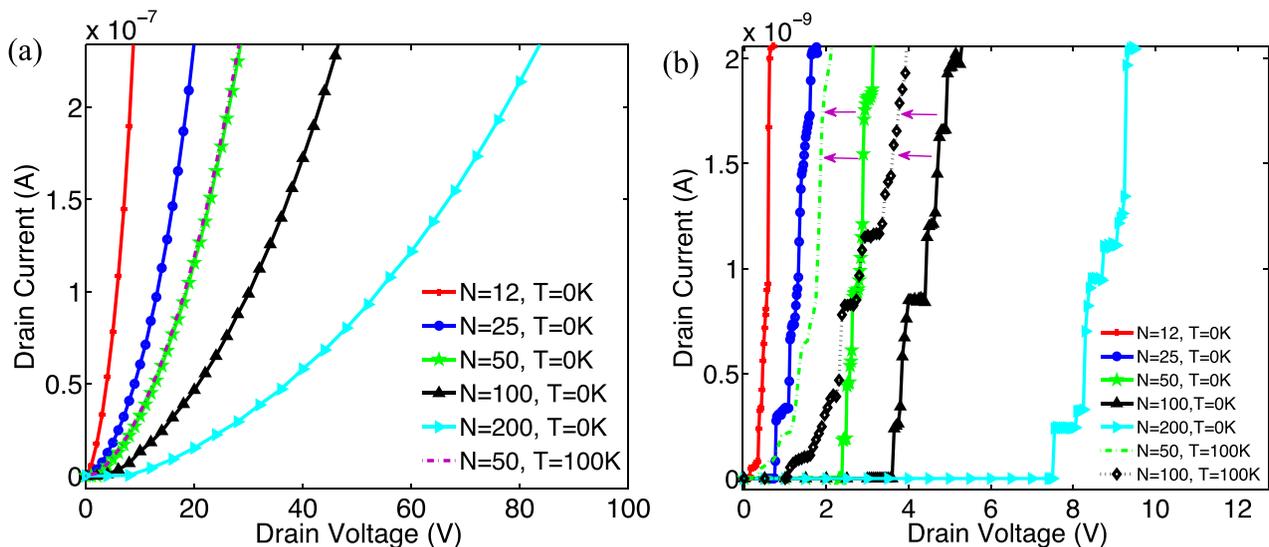

FIG. 7. (a) Simulated *IV* characteristics in the high-bias regime for devices of different numbers of islands ($N-1$). Non-Ohmic behavior stems from effective lowering of the tunneling barriers by the voltage drops across the junctions. (b) Simulated *IV* characteristics at low biases revealing Coulomb staircase structures that are the manifestations of charging effects of the nano-islands. Solid lines show results for $T = 0$ K, and dashed lines show results for $T = 100$ K. Increase in temperature shortens the blockade length.
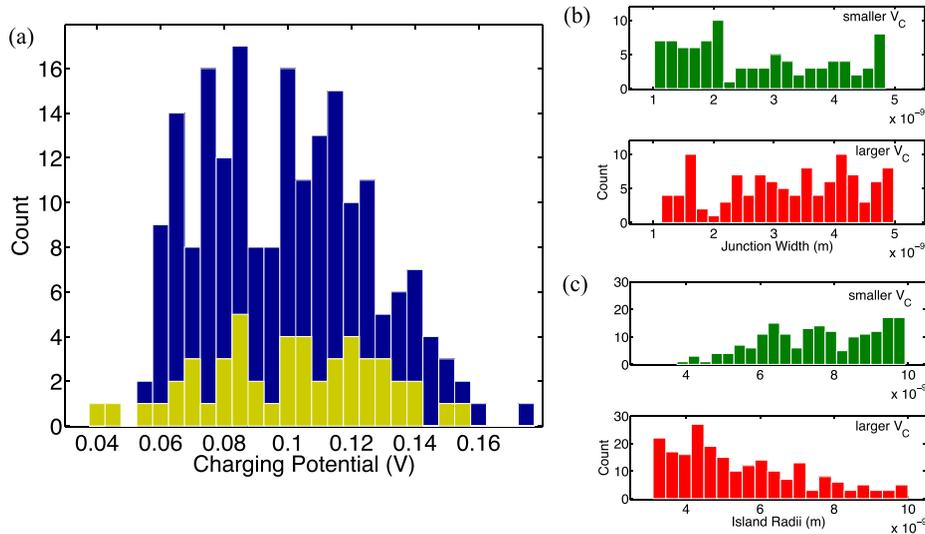
FIG. 8. (a) Distributions of charging potentials of the junctions for a 200-junction device (blue/dark) and a 50-junction device (yellow/light). (b) Charging potential distributions for the junction widths for the 200-junction device separating those junctions with smaller charging potentials (top/green) in part (a) from those with larger charging potentials (bottom/red). (c) Distributions of island radii for the same 200-junction device, separating islands associated with those junctions with smaller charging potentials (top/green) from those with larger charging potentials (bottom/red). The double counting corrects for the counting errors that are caused by counting of those islands that couple both types of junctions, one having a smaller V_C and the other with a larger V_C.

thresholds. At $T = 0$ K, the conduction channel across an individual junction does not open unless the drop across the junction, which depends on the charge state, is sufficiently large so as to overcome the junction charging energy (E_c). Tunneling across any one junction may only be a transient, however, leading to a new charge state but not necessarily a cascade of tunneling events leading to a steady state current. Such, in fact, is the case in the Coulomb blockade region for $V_{SD} < V_{th}$. Above the threshold, the pronounced staircase structures stem from the three factors: (i) the charge state of the system in steady state, (ii) the distribution of charging potentials ($V_C \equiv E_C/e$), [see Fig. 8(a), which shows the distribution of charging potentials for two different chain lengths], and (iii) the distribution of tunneling resistances across the chain (Fig. 9), which are a reflection of the disorder in the chain. The charging potentials depend on the capacitances in the system, which are directly influenced by distribution of island radii [Fig. 6(a)], junction widths [Fig. 6(b)], and the dielectric constant of the materials of which the tunnel junctions are made.

A closer examination of the distributions of charging potentials reveals that the island sizes play a more significant role in determining the charging potentials than do the junction widths. Consider, for example, the distributions of junction widths separating those with larger charging potentials from those with smaller charging potentials as shown in Fig. 8(b). The top/green histogram in Fig. 8(b) shows the distribution of junction widths only for those junctions with smaller charging potentials (0% to 50% of the maximum charging potential), while the bottom/red histogram shows the distribution of junction widths only for those junctions with larger charging potentials (50% to 100% of the maximum charging potential). Junctions with higher charging potentials have nearly the same range of junction widths compared with those with lower charging potentials, although there is a slight asymmetry—the distribution of

junction widths for junctions with smaller charging potentials being slightly skewed toward smaller junction widths, and vice versa. On the other hand, the charging potentials depend strongly on the island radii, as illustrated in Fig. 8(c). The junctions with smaller charging potentials (top/green) tend to couple the larger islands, while the junctions with larger charging potentials (bottom/red) tend to couple islands with smaller radii. The dominance of island size over junction width in affecting the charging potentials in these devices is due to the self-capacitances (0.72 ± 0.22 aF) of the
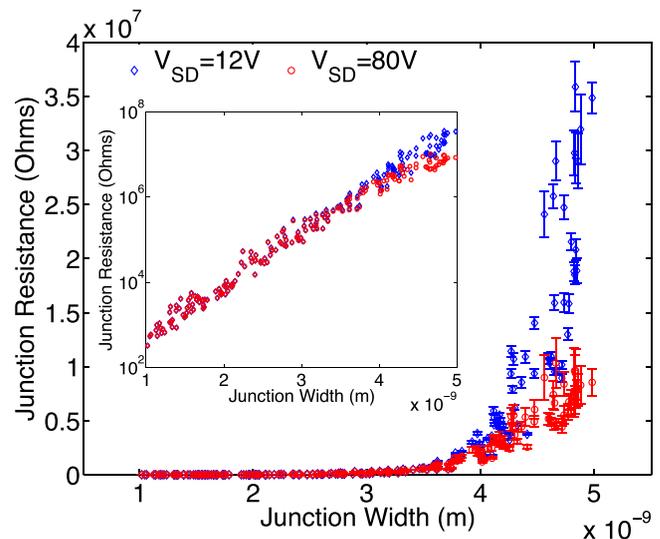

FIG. 9. Variation of junction resistances with the junction widths in a chain of $N = 200$ junctions at two different source-drain biases. At the lower bias $V_{SD} = 12$ V (blue diamonds), a Coulomb-staircase structure is observed in the IV characteristics (Fig. 7), while at the higher bias $V_{SD} = 80$ V (red circles) no Coulomb staircase structure is observed. Error bars about the mean values show the standard deviations in the junction resistances (over 5000 Monte Carlo steps, corresponding to approximately 1 ns at 12 V and 18 ps at 80 V) after the system has reached a steady state. The inset shows the same data on a logarithmic scale.

islands being comparable to the junction capacitances $(0.39 \pm 0.15$ aF).

When the source electrode is moved to increase the number of junctions and islands in the chain, a larger number of junctions and islands are sampled from the distributions. With the increase in the number of islands and junctions, the longer device requires larger source-drain bias for the junctions to be able to overcome their respective charging potentials. Two factors are primarily responsible for this increase in the required bias. First, is the potential-divider nature of the island chain. In a larger chain, a given source-drain potential is divided among a larger number of junctions leading to a smaller average potential drop across each junction, as compared to a smaller chain, similar to the case of resistors in series. Second, with new junctions and islands being sampled from the distribution in a longer chain, especially wider junctions and smaller islands, the number of junctions with larger charging potentials increases [Fig. 8(a)]. With increasing chain length, there is an increasing chance of also increasing the maximum charging potential in the distribution. Both of these factors contribute to the increase in the device V_{th} with the increase in chain length. Sampling more of the junctions having larger charging potential would also be expected to make more pronounced Coulomb staircase structures in larger chain devices as compared to smaller chain devices, which is indeed observed [Fig. 7(b)].

The linear relationship shown in Fig. 10 between the threshold voltage (V_{th}) and the number of junctions (N) has also been observed in 2-dimensional systems[12,22] and has been the subject of several theoretical and computational studies.[25–27] For an array of islands with uniform capacitances but with potential levels randomly offset by quenched background-charge disorder, Middleton and Wingreen[25] showed that the linear $V_{th}(N)$ behavior can be described by $V_{th} = \alpha N \Delta V$, where the constant α was found to depend on the dimensionality of the system and the junction-capacitance-to-island-self-capacitance ratio. In the limit where the self-capacitance (or gate capacitance) is very
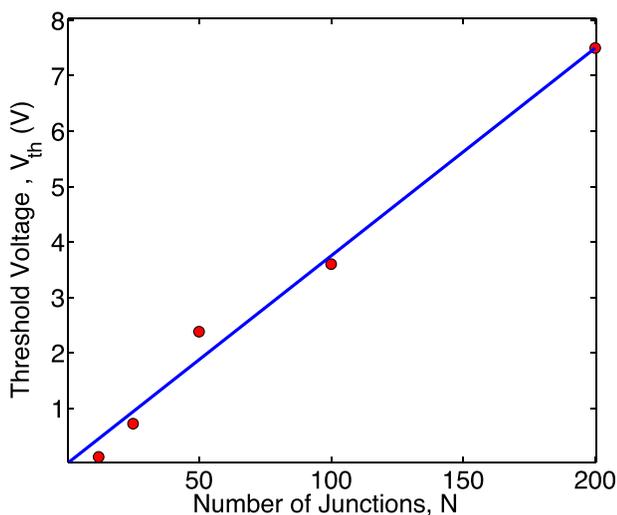
strong compared to the inter-island capacitance, the screening length $\lambda \to 0$, and ΔV is the constant change in potential required in V_{SD} per "up-step" for the charge front to be able to advance toward the other electrode. An up-step is an electronic transition between two islands in the chain that requires a minimum increase in V_{SD}, without which system remains in a static charge state.

In systems with $\lambda \neq 0$, particularly those with non-uniform junction- and self-capacitances as is the case in this work, $V_{th}(N)$ may still be expected to be linear, but the slope is difficult to predict analytically based on the system capacitances and background charges,[22,25–27] since voltage drops vary from junction to junction and also vary with the charge state of the system. Interpreting αN as the number of up-steps[27] that must successively be overcome by increasing V_{SD} to reach the threshold, ΔV represents the average increase in V_{SD} required per up-step. Consider, for example, a given static charge state at some particular V_{SD} at $T = 0$. In a static charge state, the change in free energy for tunneling between any two islands i and j has $\Delta W_{ij} > 0$, and tunneling is forbidden. We consider the next up-step to be the first electronic transition, say between islands i and j, to have $\Delta W_{ij} = 0$ via an increase in the applied V_{SD}. Subsequent to this transition, there may be a cascade of transitions that take place, until once again, at the new value of $V_{SD} < V_{th}$, the system reaches a new static charge state, with a new up-step. The new static charge state may or may not advance the charge front toward the other electrode, and may or may not include a change in the net charge on the device. We note that unlike in the $\lambda = 0$ limit, for $\lambda \neq 0$, the value of ΔV needed to overcome each up-step is not necessarily equal to ΔW_{ij}, as ΔW_{ij} is itself a function of V_{SD} through the V_{ij} term in Eq. (4). On the other hand, the number of up-steps and their associated ΔW_{ij} values are important for understanding the dependence of V_{th} with temperature.[22,27] Unfortunately, neither the number of up-steps, the associated ΔW_{ij}, nor the necessary ΔV values needed to overcome them seem to be readily predictable in advance.

Although a thorough analysis is beyond the scope of this paper, we have examined the up-steps for 25-junction system at $T = 0$. In this case, a total of 27 up-steps were observed while increasing V_{SD} in increments of 7×10^{-6} V from zero to the threshold $V_{th} = 0.74$ V. The first electron moved from the first island to the drain at $V_{SD} = 8.8 \times 10^{-2}$ V. The values of ΔV required to overcome each subsequent up-step ranged from $< 14 \times 10^{-6}$ V up to 0.15 V. In the process, frequently one electron and sometimes anywhere from two to four electrons moved to the drain, leading to a change in the net charge on the device during the overcoming of each up-step. In the process of overcoming an up-step, the charge front does not necessarily advance toward the source, however. During the course of overcoming the 27 up-steps, the charge front advanced only nine times toward the source. Further study is required to investigate the dependence of ΔV, if any, on the distribution of capacitances in the system especially the distribution of junction charging energies shown in Fig. 8(a). A detailed analysis of the up-steps and the dependence of V_{th} with temperature will be presented in future work.

FIG. 10. Variation of the threshold voltage [obtained from Fig. 7(b)] V_{th}, as a function of the number of junctions N along the chain. A linear behavior as has been observed in several experimental studies.[12,13,22,24]

When the applied bias V_{SD} equals V_{th}, the device starts conducting and a considerable distribution in the junction tunneling resistances is observed across the length of the device (Fig. 9). As already discussed, the tunneling resistances at any given time depend on several factors [Eqs. (2) and (3)], especially the junction widths and the charge state. The junction widths play a dominant role in determining the tunneling resistances because of the exponential dependence of tunneling probability on junction width. The wider junctions with their large tunneling resistances and low tunneling rates limit the current flowing through the device. As a result, the wider junctions with the largest resistances generally have a dominant effect on the scale of the device current, especially at lower biases (Fig. 9). However, since the dominant junctions can change as the chain length increases wherein a larger distribution of junctions is contained in the chain, there is a non-linear dependence of the overall resistance of the devices as a function of chain length, as can be inferred from the slopes of the *IV* curves in Fig. 7 at any particular $V_{SD} > V_{th}$.

Figure 11 shows mean values of the voltage drops in a 200-junction system at two different source-drain biases during steady-state current flow. At the lower bias, $V_{SD} = 12$ V, there is a Coulomb-staircase structure in the *IV* characteristics [Fig. 7(b)], while at higher bias, $V_{SD} = 80$ V, no Coulomb staircase is observed [Fig. 7(a)]. At smaller V_{SD}, the distributions in junction widths (Fig. 11) have negligible effects in determining the potential drops across the junctions. However, at large V_{SD}, the wider junctions show larger potential drops across them, as compared to narrower junctions, and furthermore show greater increases in the potential drops with increased V_{SD} (Fig. 11). Band bending effects are therefore not uniform across all junctions, but are greater across the wider ones, which otherwise act as the major roadblocks (higher tunneling resistance) for current flow, especially at lower biases. Hence, at high V_{SD}, there is larger
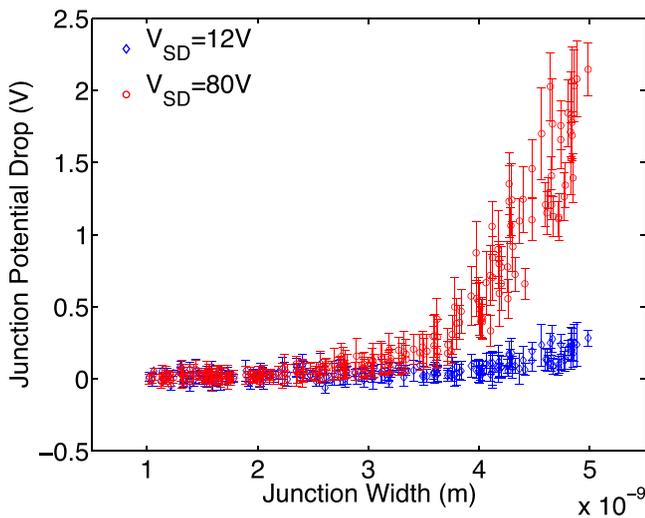
barrier height suppression that partly compensates for their large junction widths. This leads to a decrease in the tunneling resistances of the wider junctions with increasing bias, but without any significant change taking place across the narrower junctions (Fig. 9). The large potential drops ($V_{ij} \gg V_C$) also lead to diminishing of the charging effects and hence to larger changes in the free energy [Eq. (4)] after the electron transitions across the wider junctions. Both these factors lead to a considerable increase in their electron tunneling rates at large V_{SD}. With increasing V_{SD}, more conduction channels open up that increase the chances of electron conduction across the device length. We believe that these multiple effects of increased number of conduction channels and large increase in tunneling rates across the wider junctions are responsible for the diminishing of discrete Coulomb staircase steps at large V_{SD}. Further investigation is underway to understand the exact mechanism behind the disappearance of staircase structures at higher biases.

The *IV* characteristics at $T = 100$ K for the 50-junction and 100-junction devices [Fig. 7(b)] show that V_{th} and the blockade width depend sensitively on temperature. With increasing temperature, blockade effects are diminished as the sharp increase in current at V_{th} is smoothed out and V_{th} decreases. For low source-drain bias values, higher-temperature *IV* curves still show the Coulomb staircase structure but at much lower bias values within the zero-temperature blockade region. On the other hand, temperature has no appreciable effect on the device current at large source-drain bias, which is indicative of quantum tunneling. The sensitivity of V_{th} and the Coulomb staircase structure on temperature may seem surprising since eV_{th} is on the order of electron Volts, while $k_B T$ is less than 25 meV up to room temperature. The relevant energy scale is not eV_{th}, but rather, is the scale in the differences in energy levels of the local up-steps. The dependence of V_{th} on temperature has been studied in some detail by Parthasarathy *et al.*[22] and Elteto *et al.*[27] for the case of transport in systems consisting of metal nanocrystal arrays, and will be further investigated using our model in future work.

Studies done on 1D and 2D Coulomb blockade devices have shown that beyond the threshold bias, the *IV* behavior follows a scaling law $I \propto \left(\frac{V - V_{th}}{V_{th}}\right)^{\zeta}$; however, what values the exponent ζ might be expected to take remains an open question. For infinite arrays in the limit of short screening length, Middleton and Wingreen[25] argue analytically that $\zeta = 1$ and $5/3$ for 1D and 2D systems, respectively, while their computer simulations for finite systems correspondingly give $\zeta = 1$ and 2.0 ± 0.2. Experimental studies done on 1D and 2D arrays of Al islands linked by $Al/Al_xO_y/Al$ tunnel junctions show $\zeta = 1.36 \pm 0.1$ for 1D, and $\zeta = 1.8 \pm 0.16$ for 2D.[28] The investigation of a $\sim 1.2\,\mu$m chain of graphitized carbon nanoparticles self-assembled between two Cr microelectrodes gives different values of ζ for different samples of the same length, with values ranging between 1.0 and 2.35.[29] The review by Deshpande *et al.*,[30] and the Coulomb-blockade transport studies on experimental quasi-one-dimensional polymer nanofibres by Aleshin *et al.*[31] go a step further showing that for a given sample at a given temperature there

FIG. 11. Variation of junction potential drops with the junction widths in a chain of $N = 200$ junctions at two different source-drain biases V_{SD} [12 V (blue diamonds); 80 V (red circles)], as in Fig. 9. Error bars about the mean values show the standard deviations in the junction potential drops (over 5000 Monte Carlo steps, corresponding to approximately 1 ns at 12 V and 18 ps at 80 V) after the system has reached a steady state.
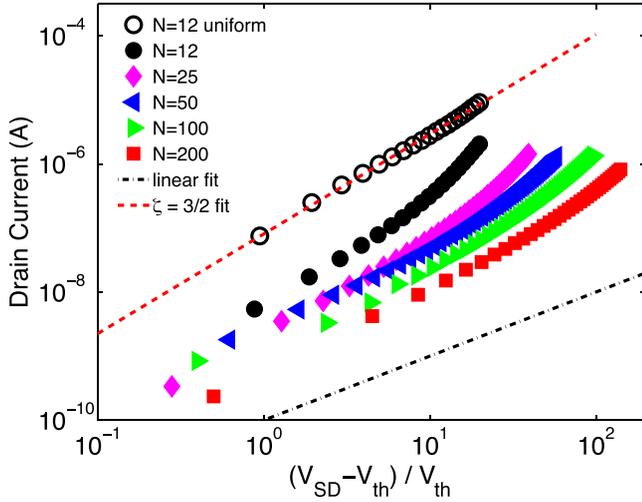
FIG. 12. *IV* characteristics of disordered 1D chains (solid symbols) of different lengths ranging from 12 to 200 junctions over a wide applied bias range. At moderate biases beyond the threshold voltage, the *IV* behavior in larger-chain-length devices shows $\zeta \sim 1$, and increases towards $\zeta \sim 2$ for shorter lengths. For a given chain length, ζ increases with the increase in the applied bias across the chain. The change is more prominent for shorter lengths. The characteristic for a uniform 12-junction chain (open circles) is also shown for comparison. The junction width (3.46 nm) and the island radius (6.92 nm) of this uniform system are the respective mean values of the random junction widths and random island radii in the disordered 12-junction system (black solid circles).

is a transition in the *IV* behavior, wherein the exponent changes as the applied bias is sufficiently increased. In the study by Aleshin *et al.*,[31] the exponent changes from $\zeta \sim 1.3$ at low biases to $\zeta \sim 2.1$ at higher biases. They argue that the change in ζ with the applied bias can be attributed to the crossover from quasi-1D to 2D transport.

Simulated *IV* characteristics of disordered 1D devices with different chain lengths N at source-drain biases beyond the threshold are shown in Fig. 12. At moderate bias values when the staircase structure begins to disappear, the exponent ζ ranges between 1 and 2 for different chain lengths, with $\zeta \sim 1$ for larger N and increasing in value as N decreases. Furthermore, for a given value of N, ζ crosses over from the lower value to a higher value under sufficiently large applied biases, as has been observed in the experimental study of quasi-1D systems.[31] As discussed earlier, the non-Ohmic nature of the *IV* behavior stems from the dependence of the heights of the tunneling barriers on the voltage drops across the respective junctions, and the barrier suppression effects are observed predominantly across the wider junctions in the system, which experience the larger voltage drops.

For comparison with disordered systems, also shown in Fig. 12 is the *IV* characteristic of a uniform 12-junction system, whose island radius and junction spacing were chosen to be the respective mean values for the disordered 12-junction system. The *IV* characteristic for the uniform system follows a power law where the exponent remains fairly constant at $\zeta \sim 3/2$ over a wide bias range as compared to a system with a random distribution of island spacings where the exponent changes appreciably from $\zeta \sim 3/2$ at lower biases to $\zeta \sim 2.8$ at higher biases. The simulations

clearly demonstrate that the scaling exponent is influenced by the system disorder and the chain length.[26] We caution, however, that while MITS captures some of the generic behaviors that may be expected for the exponent in 1D and presumably in 2D systems, the exact exponents are likely dependent on the exact nature of the dependence of the tunneling barriers on voltage drop, for which we have only incorporated a simple model at the moment. Further investigations are planned with MITS but are beyond the scope of the present work.

The scaling exponent of $\zeta \sim 3/2$ that we have observed in 1D systems may resolve the discrepancy between the value $\zeta \sim 2.25$ experimentally observed by Parthasarathy *et al.*[12] in 2D devices, and the smaller value of 5/3 predicted by Middleton and Wingreen.[25] In a 2D system, where there could be multiple current channels, Middleton and Wingreen[25] argued that the 2D scaling exponent is $\zeta = z^{-1} + \zeta_{1D}$, where $z = 3/2$ is the roughness exponent for the KPZ[32] model of interface growth in disordered media, and ζ_{1D} is the *IV* scaling exponent in a single channel. Instead of assuming an Ohmic behavior ($\zeta_{1D} = 1$) for a single channel, as did Middleton and Wingreen,[25] giving $\zeta = 2/3 + 1 = 5/3$, using larger exponent of $\zeta_{1D} \approx 3/2$ from our simulations gives $\zeta = (3/2)^{-1} + 3/2 \approx 2.2$ for 2D devices, which agrees well with experiment.[12]

IV. CONCLUSIONS

MITS is a robust tool that can be used for modeling of one- and multi-dimensional physical systems of metallic islands that conduct by means of single-electron tunneling. The physical model employed, in conjunction with a capacitance solver, advances its capabilities beyond those of existing circuit-model simulators, and allows for the investigation of numerous effects such as the spatial disorder of the islands, size distribution of the islands, and source-drain-gate geometries on device characteristics. Unlike in other simulators, MITS has the capability to elucidate key linkages between the physical characteristics of the system and the resulting device characteristics, such as the Coulomb blockade and Coulomb staircase structures. MITS also provides microscopic details that may give insights into the complex interplay among those factors that affect the tunneling rates that are fixed *a priori* (island sizes, island separations, temperature, etc.), and the evolving charge state of the system, which changes as a function of the applied source-drain bias. Devices of various geometries can be explored to investigate the influence of external factors such as gate bias on the device characteristics, especially in multi-dimensional structures, and to study the gate-dependent properties such as the current on/off ratio and Coulomb oscillations. In addition, different models of tunneling can be incorporated. For example, using a simple model for the effects of tunneling barrier suppression due to applied biases and charging effects has allowed for detailed investigation of a 1D system under reasonably high bias conditions. The structure of the tool is flexible enough to be able to incorporate refined tunneling models based, for example, on electronic structure calculations

specific to materials in a device, more accurate models of the tunneling barrier, or the effects of finite tunneling times as proposed by Nazarov *et al.*[33,34]

Since the overall device resistance predominantly depends on the wider junctions, and the larger charging energies are associated with the smaller islands, we conclude that the structures with smaller island sizes and narrower junctions may be better suited for practical applications, especially at room temperature. MITS should be a valuable tool for predictive modeling of prospective devices and for investigating different device geometries to aid in the design and control of device characteristics. Although it is difficult to analytically predict the number of up-steps in a disordered chain, especially wherein the islands are capacitively coupled, the linear behavior of V_{th} as a function of N, even for disordered systems, suggests that longer chain lengths are more suitable for practical applications because of their larger Coulomb blockades and more pronounced staircase structures. Longer-chain devices can also withstand higher temperatures, as they can exhibit Coulomb staircases despite the decrease in V_{th} with increasing temperature. More detailed investigations are required to ascertain the exact mechanism behind the change of exponent in the high-bias power law behavior and the effects of disorder in the chain on the exponent, in relation to the work in Refs. 22, and 25–27. Further investigations are also underway to study the effects of temperature on the microscopic charge states of the system and the resulting decrease in V_{th} with increasing T.

For practical applications, the effects of a gate bias on device behavior will be of great importance. In a single-island device, the gate bias shifts the Coulomb blockade and produces IV characteristics that are asymmetric about $V_{SD} = 0$. Furthermore, for fixed V_{SD}, the current in a single island device shows sharp periodic oscillations as a function of the gate bias. On the other hand, multi-island devices may be expected to show irregularly spaced gate oscillations due to the disorder in the chain or due to the varying gate influences on the islands. Although not investigated here, MITS has the capability of simulating device characteristics as a function of gate bias for different gate geometries. For nearly uniform two-dimensional devices, we anticipate that the Coulomb staircases are likely to be washed out compared to 1D chains, as the current is expected to be carried by multiple paths between the source and the drain that would diminish the staircase effects. However, a multi-dimensional device with a sufficient disorder may be expected to behave as a quasi-one dimensional device exhibiting a single dominant conducting path that, perhaps, can be affected by adjusting the gate voltage. Larger source-drain bias and higher temperature may open up additional conducting paths in a multi-dimensional device, thereby diminishing any chances of staircase structures in the device characteristics due to the different staircase structures that any one path might exhibit. Studies are currently underway using MITS to explore the characteristics of two-dimensional multi-island devices and the effects of different factors, especially gate geometry, gate bias,

disorder in the island distribution, and temperature, on device characteristics.

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