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## REALIZATION OF A DC MICROGRID USING A HAMILTONIAN BASED CONTROLS SOLUTION

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REALIZATION OF A DC MICROGRID USING A HAMILTONIAN BASED  
CONTROLS SOLUTION

By

Matthew J. Heath

A THESIS

Submitted in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

In Mechanical Engineering

MICHIGAN TECHNOLOGICAL UNIVERSITY

2013

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This thesis has been approved in partial fulfillment of the requirements for the Degree of  
MASTER OF SCIENCE In Mechanical Engineering.

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To my father.

For all those projects that led me to where I am now, this one's for you.

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## **Preface**

This work contains content that is planned for submission as a journal article entitled "Realization of a DC Microgrid Utilizing Hamiltonian Surface Shaping and Power Flow Control". Being the first author, I wrote the manuscript and performed the associated analysis. Robert Smith helped with the physical realization process. Dr. Parker and Dr. Weaver assisted with technical guidance and the revision process. Dr. Wilson and Dr. Robinett acted as the project primary investigators and assisted with technical guidance and revisions throughout the course of the project. A substantial portion of the original manuscript has been included with alterations to fit the tone and flow of this work.

## **Abstract**

Future power grids are envisioned to be serviced by heterogeneous arrangements of renewable energy sources. Due to their stochastic nature, energy storage distribution and management are pivotal in realizing microgrids serviced heavily by renewable energy assets. Identifying the required response characteristics to meet the operational requirements of a power grid are of great importance and must be illuminated in order to discern optimal hardware topologies. Hamiltonian Surface Shaping and Power Flow Control (HSSPFC) presents the tools to identify such characteristics. By using energy storage as actuation within the closed loop controller, the response requirements may be identified while providing a decoupled controller solution. A DC microgrid servicing a fixed RC load through source and bus level storage managed by HSSPFC was realized in hardware. A procedure was developed to calibrate the DC microgrid architecture of this work to the reduced order model used by the HSSPFC law. Storage requirements were examined through simulation and experimental testing. Bandwidth contributions between feed forward and PI components of the HSSPFC law are illuminated and suggest the need for well-known system losses to prevent the need for additional overhead in storage allocations. The following work outlines the steps taken in realizing a DC microgrid and presents design considerations for system calibration and storage requirements per the closed loop controls for future DC microgrids.

# Chapter 1

## Introduction

The following work outlines the realization of a DC microgrid using HSSPFC. Chapter 1 presents the microgrid concept including an overview of current control solutions, storage distribution, management, and HSSPFC. Chapter 2 introduces the DC microgrid architecture used in this work. Assumptions are defined and the mathematical model of the system is presented. The control law of HSSPFC is derived and applied to the DC microgrid architecture where a calibration method for parameter identification is outlined in detail. Storage requirements are first illuminated through simulation analysis and are echoed in hardware testing. Chapter 3 concludes with a summary of findings for this work and offers suggestions on methods for improving the realization process for future microgrids.

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Material contained in this chapter is planned for submission as a journal publication entitled "Realization of a DC Microgrid Utilizing Hamiltonian Surface Shaping and Power Flow Control".

## 1.1 Motivation

The inclusion of high penetration renewables while reducing dependency on fossil fuel storage mediums is a desirable design consideration for future power grids and aligns with the concept of a microgrid; an agile power grid with varying topology of distributed generation, storage, and loads with power flows serviced by an intelligent control system. The microgrid concept was presented by Dr. Robert Lasseter where its ability to intelligently shed loads or decouple portions of the system in response to transients is desirable when considering the stochastic nature of renewable energy sources [1, 2]. While the potential applications of a microgrid are extensive, the dynamic topology of a microgrid has attracted military interest with regard to forward operating bases; specifically in adopting hybrid architectures in military vehicle fleets to meet operational energy requirements. Doing so would allow various grid assets to be replaced or assisted by the power generation and storage capabilities of a hybrid vehicle through a vehicle-to-grid approach which may increase energy security while reducing operational cost [3]. While hybrid technologies are readily available, significant strides in control design are required in order to realize such a system.

## 1.2 Controller and Energy Storage Considerations

Droop control presents one means to manage the operation of a microgrid. By considering the DC bus voltage as local information, the interconnects between the grid assets and the common DC bus can be controlled [4]. This allows for a modular system where a varying topology is achievable without having to re-engineering a controller solution or use a ubiquitous communication network [1]. Harmoniously managing these assets becomes necessary when considering the objectives of the microgrid including maintaining the desired bus voltage while servicing loads of varying priority. Perhaps the greatest enabler of the microgrid design is the notion of distributed storage where an intelligent controls solution becomes paramount when considering the stochastic nature of microgrid assets rich in renewables. Furthermore, this notion may be expanded upon by developing optimal guidance control laws that externize energy storage metrics when coupled to the microgrid control law.

Work conducted by Weaver and Heath et al. suggest utilizing localized fast time scale storage mediums to maintain operational objectives when considering transients and stress the importance of an optimal distribution of storage [5, 6] . As such, identifying the storage and closed loop controller requirements with regards to the objective of the microgrid becomes necessary for efficient design. While conventional storage mediums take the form of fossil fuels or water impoundments, future storage systems are envisioned to be

some combination of batteries, capacitors, and/or flywheels in order to meet the dynamic response requirements of the closed loop microgrid controller. The automotive sector is considering similar prospects of hybrid storage devices where initiatives aim to couple supercapacitor and battery technologies to extremize response times and energy densities to meet power requirements for Electric Vehicles (EVs) [7].

### **1.3 Hamiltonian Surface Shaping and Power Flow Control**

Through their work, Wilson et al. proposed Hamiltonian Surface Shaping and Power Flow Control (HSSPFC) as a novel controls solution for microgrids serviced by high penetration renewables [8, 9, 10]. By utilizing storage devices as the system actuators, a controls solution whose stability is insured by applying concepts of Llyapunov stability to the system's Hamiltonian is achievable [11]. The benefits for fielding HSSPFC in a microgrid are binal in execution. First, the closed loop actuator equations are decoupled and result in a truly modular topology which aligns with the microgrid paradigm. Second, by considering the controller effort the required storage dynamics may be illuminated when subjecting the microgrid to various operation conditions. As such, HSSPFC presents itself as a useful tool in the realization of future microgrids.



# Chapter 2

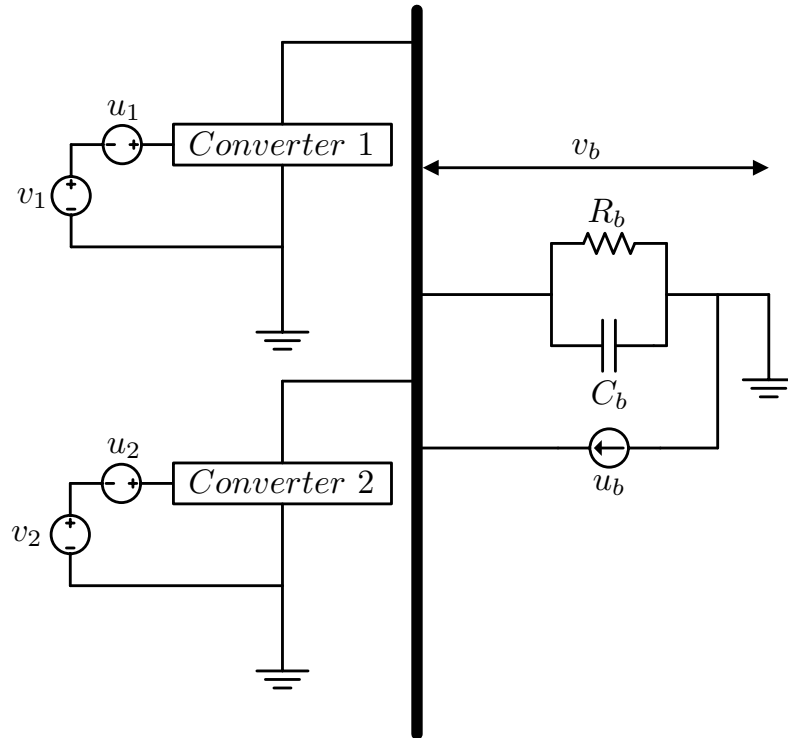
## DC Microgrid Realization

This chapter contains the methodologies used in realizing a DC microgrid and applying HSSPFC to manage the distributed storage assets of the power grid. The DC microgrid architecture is introduced and assumptions are defined. Derivation of the control law is presented per the results of Wilson et al. in [11] and applied to the DC microgrid. The hardware realization process is outlined and described in detail. A calibration procedure is developed to apply the reduced order model used in HSSPFC to the realized system. Storage requirements are illuminated through simulation and hardware testing where two test cases are considered in order to demonstrate the value of HSSPFC. The first of which considers a step event where the total power sourced to the load is maintained while the second examines a step event where a power deficit develops.

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Material contained in this chapter is planned for submission as a journal publication entitled "Realization of a DC Microgrid Utilizing Hamiltonian Surface Shaping and Power Flow Control".

## 2.1 Model Derivation

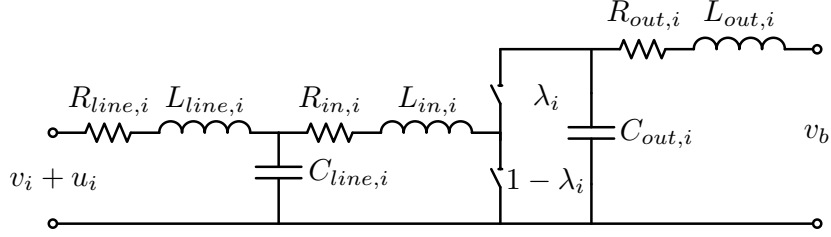


**Figure 2.1:** High level DC microgrid topology consisting of two sources with converter level storage and a constant RC load with bus level storage.

Figure 2.1 depicts a high level overview of the microgrid architecture used for this work. Subsystems 1 and 2 are defined as sources consisting of a renewable voltage source,  $v_i$ , in series with a bidirectional, high bandwidth, storage device denoted  $u_i$ . The series contributions of both  $v_i$  and  $u_i$  interface to the grid via a boost converter. Subsystem 3

is a constant RC load that possesses storage characteristics as denoted by  $u_b$ . The bus storage device is treated as a high bandwidth ideal current source capable of both sourcing and sinking current. Subsystem 4 is the common node DC bus of the microgrid.

To characterize converter dynamics, a continuous average mode modeling approach for a boost converter was used [12]. A five-state model of the source converter is shown in Figure 2.2 with its averaged differential equations shown in Eq. 2.1,

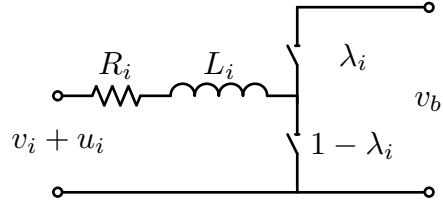


**Figure 2.2:** Five-state boost converter schematic.

$$\begin{aligned}
 L_{line,i} \frac{di_{L_{line,i}}}{dt} &= v_i + u_i - i_{L_{line,i}} R_{line,i} - v_{C_{line,i}}, \\
 C_{line,i} \frac{dv_{C_{line,i}}}{dt} &= i_{L_{line,i}} - i_{L_{in,i}}, \\
 L_{in,i} \frac{di_{L_{in,i}}}{dt} &= v_{C_{line,i}} - i_{L_{in,i}} R_{in,i} - \lambda v_{C_{out,i}}, \\
 C_{out,i} \frac{dv_{C_{out,i}}}{dt} &= \lambda i_{L_{in,i}} - i_{L_{out,i}}, \\
 L_{out,i} \frac{di_{L_{out,i}}}{dt} &= v_{C_{out,i}} - i_{L_{out,i}} R_{out,i} - v_b.
 \end{aligned} \tag{2.1}$$

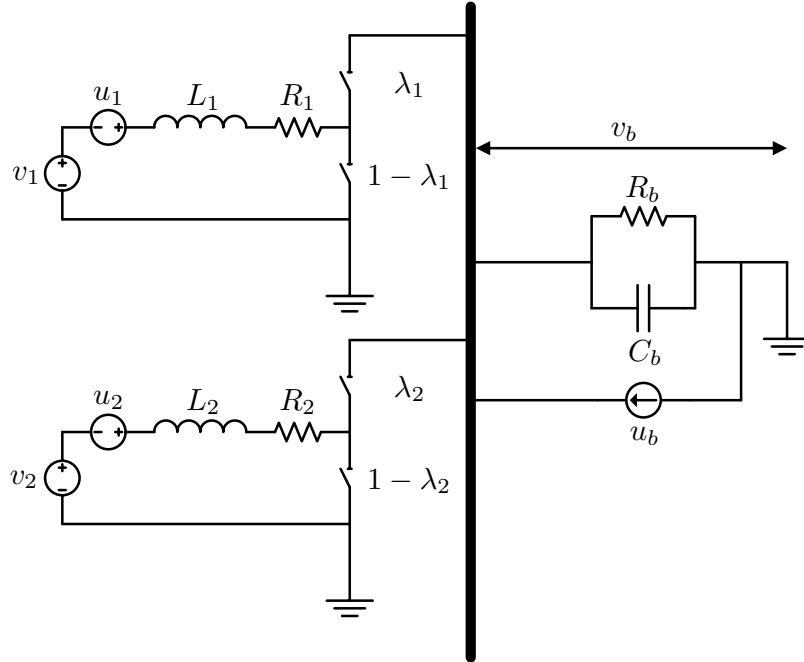
The interconnect between the series input from renewable source  $v_i$  and converter level storage  $u_i$  is modeled through the line parameters  $R_{line,i}$ ,  $L_{line,i}$ , and  $C_{line,i}$  which are the line resistance, inductance, and capacitance, respectively. Regarding the low side of the boost converter, the converter resistance and low side inductor are parameterized by  $R_{in,i}$  and  $L_{in,i}$ . Likewise, the high side of the converter is modeled by output line resistance,  $R_{out,i}$ , and inductance,  $L_{out,i}$ . The capacitor  $C_{out,i}$  is used to maintain a stable output voltage upstream of the converter switching network when connected to the DC bus with bus voltage represented by  $v_b$ .

A single-state reduced order boost converter model was created to deploy HSSPFC to the DC microgrid. To accomplish this, the five-state converter model of Figure 2.2 was reduced to the single-state model of Figure 2.3 through the following assumptions. By considering the resulting contributions to the overall dynamics of the converter model, both the input line inductance,  $L_{line,i}$ , and capacitance,  $C_{line,i}$ , were considered negligible. Furthermore, both the output voltage and current of the converter may readily be determined through the ratiometric relationship between their corresponding input values and the converter duty cycle,  $\lambda_i$ . As such, the contributing dynamics of high side capacitor,  $C_{out,i}$ , and line inductance,  $L_{out,i}$ , are neglected. Regarding the low side inductor of the converter, its value was readily measured from the selected component and was redefined as  $L_i$ . The converter resistance,  $R_{in,i}$ , was redefined as  $R_i$  and represents the net resistance of the converter and line resistances,  $R_{line,i}$  and  $R_{out,i}$ . The empirical value for  $R_i$  was determined through an experimental procedure which is covered in detail in Section 2.4.



**Figure 2.3:** Single-state boost converter schematic.

Substituting the single-state boost converter model of Figure 2.3 into the DC microgrid of Figure 2.1 yields the architecture considered in this work and was chosen such that it would mirror the tutorial architecture in [11].



**Figure 2.4:** DC microgrid consisting of two sources with converter level storage and a constant RC load with bus level storage adapted from tutorial architecture in [11].

Defining the converter inductor current,  $i_i$ , and bus voltage,  $v_b$ , as the states, the resulting governing equations for the DC microgrid are shown in Eq. 2.2,

$$\begin{aligned}
 L_i \frac{di_i}{dt} &= -R_i i_i - \lambda_i v_b + v_i + u_i, \\
 C_b \frac{dv_b}{dt} &= \sum_{i=1}^n \lambda_i i_i - \frac{1}{R_b} v_b + u_b.
 \end{aligned}
 \tag{2.2}$$

The parameters  $L_i$ ,  $R_i$ , and  $\lambda_i$  are the converter's inductance, resistance, and duty cycle, respectively. The RC load is characterized by resistance,  $R_b$ , and capacitance,  $C_b$ .

## 2.2 Control Law

From the work of Wilson et al. in [11], the storage request  $u_i$  and  $u_b$  are defined as the actuators of the system through the control law of Eq. 2.3,

$$\begin{aligned} u_i &= R_i \dot{i}_{i,r} + \lambda_i v_{b,r} - v_i + K_{P,i} e_i + K_{I,i} \int e_i dt, \\ u_b &= - \sum_{i=1}^n \lambda_i \dot{i}_{i,r} + \frac{1}{R_b} v_{b,r} + K_{P,b} e_b + K_{I,b} \int e_b dt, \end{aligned} \quad (2.3)$$

which relies on the state error vector of Eq. 2.4,

$$e = \begin{Bmatrix} e_1 \\ e_2 \\ e_b \end{Bmatrix} = \begin{Bmatrix} x_{1,r} - x_1 \\ x_{2,r} - x_2 \\ x_{b,r} - x_b \end{Bmatrix} = \begin{Bmatrix} i_{1,r} - i_1 \\ i_{2,r} - i_2 \\ v_{b,r} - v_b \end{Bmatrix}. \quad (2.4)$$

Substituting the HSSPFC control law of Eq. 2.3 into the governing system equations of

Eq. 2.2 gives the closed loop system of Eq. 2.5,

$$\begin{aligned} L_i \frac{di_i}{dt} &= (R_i + K_{P,i})e_i + \lambda_i e_b + K_{I,i} \int e_i dt, \\ C_b \frac{dv_b}{dt} &= - \sum_{i=1}^n \lambda_i e_i + \left( \frac{1}{R_b} + K_{P,b} \right) e_b + K_{I,b} \int e_b dt. \end{aligned} \quad (2.5)$$

The physical significance of this control law becomes apparent when considering its contributions in terms of power while delineating between the feed forward and PI terms. Multiplying Eq. 2.3 by its respective state reference values reformulates the control law in terms of required converter storage power,  $P_i$ , and bus storage power,  $P_b$ , as is shown in Eq. 2.6,

$$\begin{aligned} P_i &= i_{i,r} u_i = R_i i_{i,r}^2 + \lambda_i v_{b,r} i_{i,r} - v_i i_{i,r} + i_{i,r} (K_{P,i} e_i + K_{I,i} \int e_i dt), \\ P_b &= v_{b,r} u_b = - \sum_{i=1}^n \lambda_i v_{b,r} i_{i,r} + \frac{1}{R_b} v_{b,r}^2 + v_{b,r} (K_{P,b} e_b + K_{I,b} \int e_b dt). \end{aligned} \quad (2.6)$$

During steady state operation, the PI portion of Eq. 2.6 drops out leaving only the feed forward portion of the control law. For the boost converter power equation, this occurs when the power balance of the converter is met by the source input voltage,  $v_i$ , for a unique set of  $\lambda_i$ ,  $i_{i,r}$ , and  $v_{b,r}$  when  $R_i$  is well-known. The bus power equation occurs when the



load,  $R_b$ , is serviced in full by the contributions of the source subsystems for a given bus voltage. Such operating conditions are potentially inclusive which suggest that if the load and converter losses are well-known, there exist unique sets of converter and bus level parameters which enable the source and bus subsystems to harmoniously operate in steady state. It is at these operating conditions that the converter storage power,  $P_i$ , and bus storage power,  $P_b$ , are zero and therefore no storage is required. If the converter current or bus voltage reference values are selected such that the power balance is not met then a non-zero storage term occurs. Physically, this is the inclusion of the converter storage power,  $P_i$ , or bus storage power,  $P_b$ , within its respective subsystem materialized through the controller effort in the PI terms.

The control law of Eq. 2.3 is derived using Lyapunov's direct method when using an energy functional that is a function of the state error vector of Eq. 2.4. A thorough derivation of the control law is presented in [11] while its key components are considered here; the most important of which being the application of using the system error state Hamiltonian as a Lyapunov candidate function to insure the stability of Eq. 2.3.

Shown in Eq. 2.7 are the governing system equations of Eq. 2.2 recast in matrix notation,

$$\begin{aligned}
 & \begin{bmatrix} L_1 & 0 & 0 \\ 0 & L_2 & 0 \\ 0 & 0 & C_b \end{bmatrix} \begin{Bmatrix} \dot{i}_1 \\ \dot{i}_2 \\ \dot{v}_b \end{Bmatrix} = \\
 & \begin{bmatrix} -R_1 & 0 & -\lambda_1 \\ 0 & -R_2 & -\lambda_2 \\ \lambda_1 & \lambda_2 & -\frac{1}{R_b} \end{bmatrix} \begin{Bmatrix} i_1 \\ i_2 \\ v_b \end{Bmatrix} + \begin{Bmatrix} v_1 \\ v_2 \\ 0 \end{Bmatrix} + \begin{Bmatrix} u_1 \\ u_2 \\ u_b \end{Bmatrix}.
 \end{aligned} \tag{2.7}$$

A compressed variant is given in Eq. 2.8,

$$[\mathbf{M}]\dot{x} = [\bar{\mathbf{R}} + \tilde{\mathbf{R}}]x + v + u, \tag{2.8}$$

where  $\bar{\mathbf{R}}$  is a diagonal matrix of system losses  $R_1$ ,  $R_2$ , and  $\frac{1}{R_b}$  and  $\tilde{\mathbf{R}}$  is a skew-symmetric matrix of converter duty cycles  $\lambda_1$  and  $\lambda_2$ .

The error state vector of Eq. 2.4 is then governed by Eq. 2.9,

$$[\mathbf{M}] \dot{e} = [\tilde{\mathbf{R}} + \tilde{\mathbf{R}}] e + v + \{u_r - u\}, \quad (2.9)$$

where  $u_r$  is the reference control input vector. Having defined the error state governing equations, the control law of Eq. 2.3 may be derived through Lyapunov's direct method when using the system error state Hamiltonian as the Lyapunov candidate function.

The energy based candidate function is defined in Eq. 2.10,

$$\begin{aligned} H &= \frac{1}{2} e^T \mathbf{M} e, \\ &= \frac{1}{2} \left\{ \begin{matrix} e_1 & e_2 & e_b \end{matrix} \right\} \begin{bmatrix} L_1 & 0 & 0 \\ 0 & L_2 & 0 \\ 0 & 0 & C_b \end{bmatrix} \left\{ \begin{matrix} e_1 \\ e_2 \\ e_b \end{matrix} \right\}, \\ &= \frac{1}{2} L_1 e_1^2 + \frac{1}{2} L_2 e_2^2 + \frac{1}{2} C_b e_b^2, \\ &= E_{L_1} + E_{L_2} + E_{C_b}, \end{aligned} \quad (2.10)$$

where  $E_{L_1}$ ,  $E_{L_2}$ , and  $E_{C_b}$  are the energy error values for converter inductors  $L_1$ ,  $L_2$ , and bus

capacitor  $C_b$ . Furthermore, the Hamiltonian function may readily be shown to be positive definite about  $e = 0$  thus satisfying the first lemma of Lyapunov's direct method.

The second lemma, where stability is determined through the inequality  $\dot{H} < 0$ , is examined in Eq. 2.11 - 2.13,

$$\begin{aligned}
 \dot{H} &= e^T M \dot{e}, \\
 &= e^T [M\dot{x}_r - M\dot{x}], \\
 &= e^T [[\bar{R} + \tilde{R}]x_r + v + u_r - [\bar{R} + \tilde{R}]x - v - u], \\
 &= e^T [[\bar{R} + \tilde{R}]e + \{u_r - u\}], \\
 &= e^T \bar{R} e + e^T \Delta u,
 \end{aligned} \tag{2.11}$$

where  $e^T \tilde{R} e = 0$  due to its skew-symmetric form and

$$\Delta u = u_r - u = -K_p e - K_I \int e dt. \tag{2.12}$$

Substitution of Eq. 2.12 into Eq. 2.11 yields the second stability constraint of Lyapunov's

second method,

$$\dot{H} = e^T [\bar{R} - K_P] e - e^T K_I \int e dt < 0, \quad (2.13)$$

where,

$$e^T [K_P - \bar{R}] e > -e^T K_I \int e dt. \quad (2.14)$$

From the stability inequality of Eq. 2.14, it may be shown that the section of  $K_P$  is bound by the constraints of Eq. 2.15 in order to insure the second stability lemma is met,

$$\begin{aligned} K_{P,i} &> -R_i, \\ K_{P,b} &> -\frac{1}{R_b}. \end{aligned} \quad (2.15)$$

Having insured stability, the control law of Eq. 2.3 may be realized when considering the

reference state vector governed by Eq. 2.16,

$$[\mathbf{M}]\dot{x}_r = [\bar{\mathbf{R}} + \tilde{\mathbf{R}}]x_r + v + u_r. \quad (2.16)$$

Substituting Eq. 2.12 into Eq. 2.16,

$$[\mathbf{M}]\dot{x}_r = [\bar{\mathbf{R}} + \tilde{\mathbf{R}}]x_r + v + u - K_p e - K_I \int e dt,$$

and solving for  $u$  in steady state,

$$u = -[\bar{\mathbf{R}} + \tilde{\mathbf{R}}]x_r - v + K_p e + K_I \int e dt, \quad (2.17)$$

yields the final form of the HSSPFC law.

From Eq. 2.17, the resulting closed loop system is linear time-invariant when using the state reference vector and fixed values for converter duty cycles. Using the state vector in

Eq.2.17 and allowing  $\lambda_i$  to vary in order to meet the operational objectives of the microgrid results in a non-linear system with the closed loop equations of Eq. 2.18,

$$[M]\dot{x} = K_P e + K_I \int e dt. \quad (2.18)$$

Here the second derivative of Eq. 2.18 illuminates an undesirable transient response characteristic for changes the state reference vector,

$$\frac{d^2}{dt^2}x_r = \ddot{e} + M^{-1}K_P \dot{e} + M^{-1}K_I e, \quad (2.19)$$

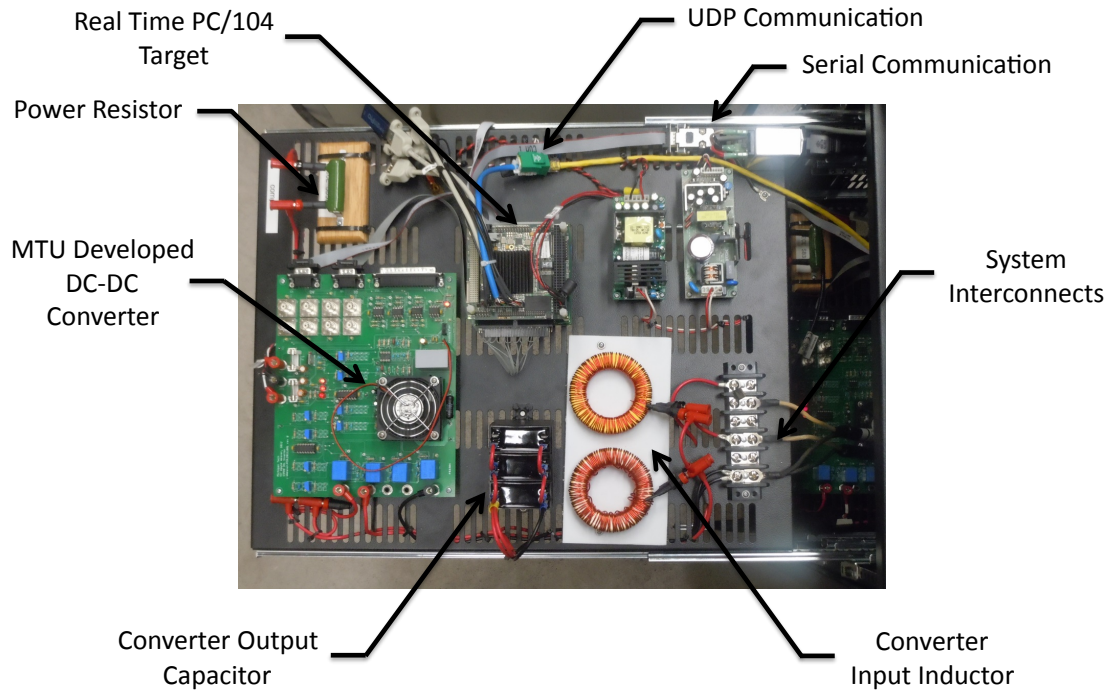
and suggest the use of a pre-filter such as that of Eq. 2.20 to mitigate such behavior per the analysis in [13],

$$\frac{x}{x_r} = \frac{K_I}{K_P s + K_I}. \quad (2.20)$$

## 2.3 System Realization

To apply the HSSPFC control law of Eq. 2.3 in hardware, a test bench scale microgrid was created that mirrors the topology of Figure 2.4. Source subsystems were realized through boost converters where the series contribution of  $v_i$  and  $u_i$  was emulated by a programmable DC power supply. The bus storage took the form of a supercapacitor bank connected to the DC bus through a bidirectional buck-boost converter. For controls implementation, a real-time distributed embedded controller network of PC/104's running instances of xPCTarget was used. A UDP communication network was used to pass reference commands from a supervisory controller to each subsystem controller while RS232 was used to communicate between the source subsystem controllers and their respective power supplies.

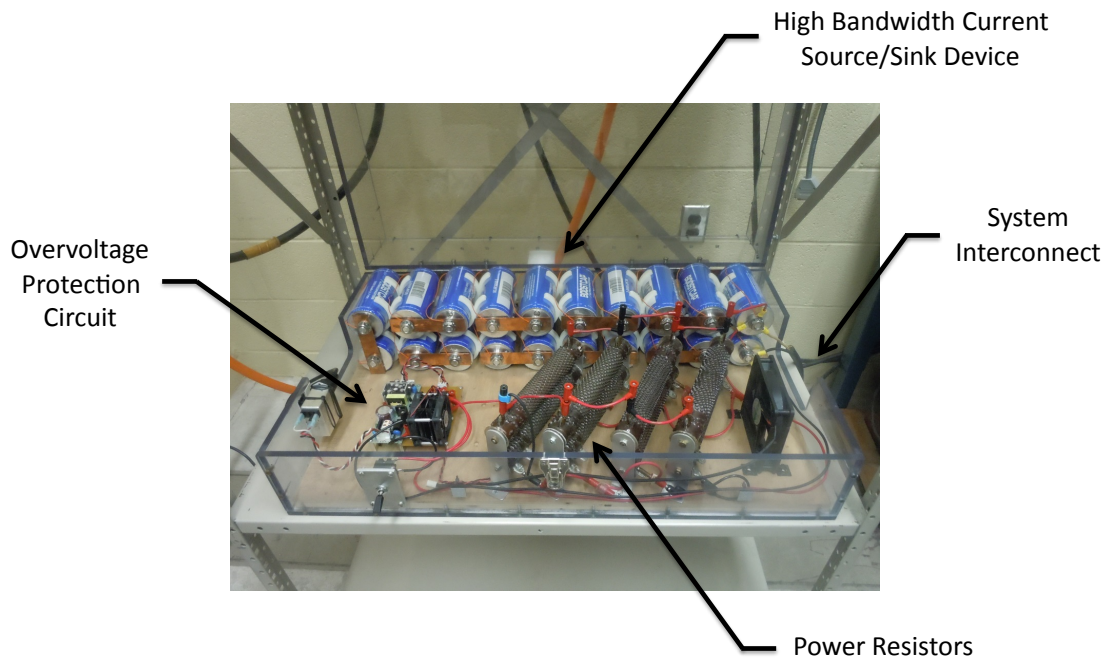




**Figure 2.5:** Source subsystem boost converter and embedded controller.

Figure 2.5 depicts the 4 channel bidirectional power converter and real-time embedded controller of the source subsystem. For the source subsystems, the converter was configured to run in a boost arrangement where power flow was directed through a diode to prevent back feeding into the power supply unit. A Magna Power XR series programmable DC power supply was used to emulate  $v_i$  and  $u_i$  where  $v_i$  was set to a constant and  $u_i$  was determined by the control law of Eq. 2.3. A power resistor was placed in series with the output channel of the power converter in order to add damping to the realized system. These were measured to be  $1.045 \Omega$  and  $1.044 \Omega$  for source subsystems 1 and 2, respectively. While neglected per the assumptions of Section 2.2, a capacitor was attached

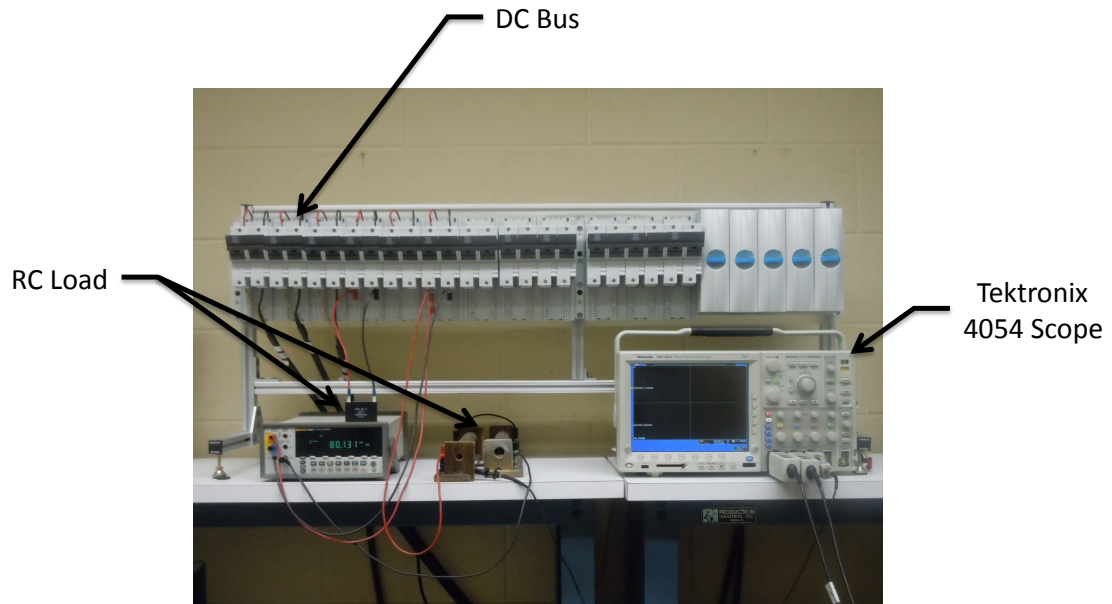
to the output of the boost converter in order to maintain a steady output voltage. A parallel arrangement of film capacitors was chosen in part for its high ripple current while not imposing significant dynamics on the system. These capacitors were measured to be  $31.22 \mu F$  and  $31.231 \mu F$  for source subsystems 1 and 2, respectively. The input inductors  $L_1$  and  $L_2$  were made from two smaller toroid core inductors in series with measured inductances  $1.989 mH$  and  $2.002 mH$ , respectively. Control signals were sampled by the A/D of the PC/104 stack with all values filtered in both hardware and software to reduce artifacts of the converter switching network in the measured signals. The sample rate of the controller was limited to  $100 Hz$  due to the communication and internal closed loop controller bandwidth of the Magna Power system.



**Figure 2.6:** Realization of the high bandwidth current source/sink device.

The high bandwidth current source/sink device is shown in Figure 2.6 and is made of 20 Maxwell K2 BCAP3000 capacitors. This results in a series capacitance of  $150\text{ F}$  at  $54\text{ V}$ . The output terminal voltage of the capacitor bank is monitored by an overvoltage protection circuit which is calibrated to trigger at  $40\text{ V}$ . When active, the power resistors depicted in Figure 2.6 are switched in parallel with the capacitor bank output terminals and dissipate the stored capacitor energy. The circuit remains active until the capacitor bank reaches  $15\text{ V}$ . Current flow is managed by a buck-boost power converter as dictated by the control law of Eq. 2.3; no protection circuitry is utilized. The converter duty cycle is driven by a PID controller wrapped around an error function of the converter output current relative to the commanded value of  $u_b$ . This converter is connected in a similar arrangement as the source subsystems but is operated bidirectionally. Control signals were sampled in an identical manner as the source subsystems where  $v_b$  was defined as the output voltage of the buck-boost converter. As such, it should be noted that the measured value for  $v_b$  was inferred from the output connection from the buck-boost converter and not directly across the RC load.

Both the power converter of Figure 2.5 and super capacitor bank of Figure 2.6 were realized by researchers in the Michigan Tech Electrical and Computer Engineering Department in support of this project.



**Figure 2.7:** Common node DC bus.

Shown in Figure 2.7 is the common node DC bus of the realized microgrid. Connections between the source subsystems, high bandwidth current source/sink device, and fixed RC load interface through selectable breakers. The fixed RC load is comprised of two series power resistors in a parallel arrangement with a film capacitor. These components were measured to be  $R_b = 102.6 \Omega$ , and  $C_b = 10.41 \mu F$ , respectively.

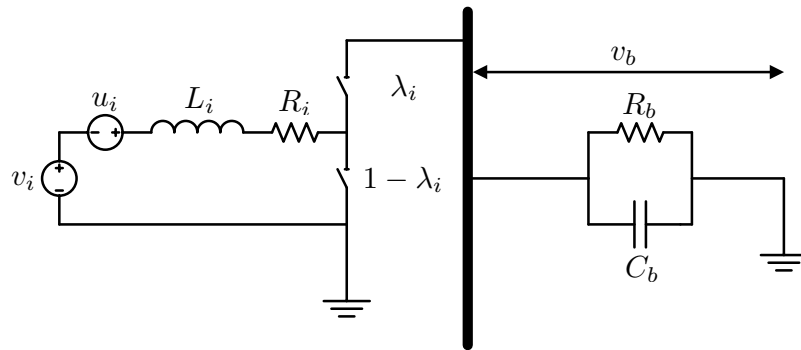
## 2.4 Converter Calibration

To realize the results of [11] and apply the HSSPFC to the DC microgrid, the resistance of the reduced order boost converter model was required. To accomplish this, an experimental

procedure was developed to map the solution space of Eq. 2.21,

$$R_i = \frac{v_i + u_i - \lambda_i v_b - K_{P,i} e_i - K_{I,i} \int e_i dt}{i_{i,r}}, \quad (2.21)$$

which is the analytical solution of the source subsystem control law of Eq. 2.3 when solving for  $R_i$ . Using the topology depicted in Figure 2.8, a single source subsystem connected to a fixed RC load was run in open loop.



**Figure 2.8:** Boost converter calibration topology.

Using a fixed source voltage of  $v_i = 40 \text{ V}$ , the converter was examined at discrete operating points within the range  $20\% \leq \lambda_i \leq 80\%$  and  $0.5 \text{ A} \leq i_{i,r} \leq 3.5 \text{ A}$  in 10% and 0.5 A increments, respectively. At each operating point, a non-zero value developed in  $e_i$  for fixed values of  $v_i$ ,  $\lambda_i$ , and  $i_{i,r}$ . The value of  $u_i$  was adjusted manually through a software

overwrite until the converter current error,  $e_i$ , and associated integral state,  $K_{I,i} \int e_i dt$ , were driven to zero. At this point the power balance within the converter was met and Eq. 2.21 reduces to Eq. 2.22,

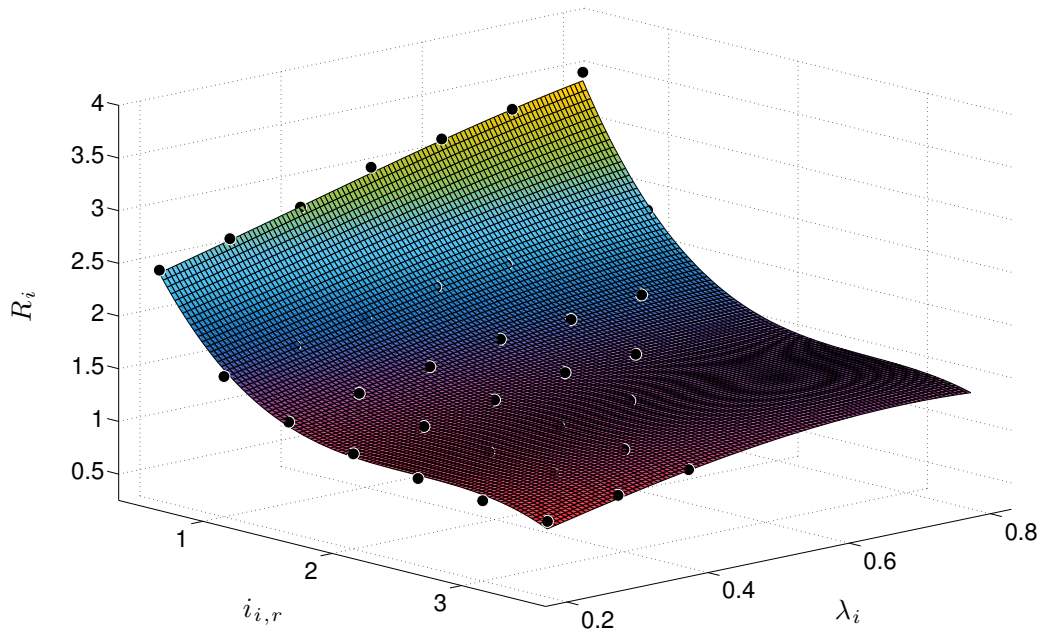
$$R_i = \frac{v_i + u_i - \lambda_i v_b}{i_{i,r}}. \quad (2.22)$$

A measurement of  $v_b$  and the requested aggregate input voltage ( $v_i + u_i$ ) was taken which along with the fixed values of  $\lambda_i$  and  $i_{i,r}$  allowed for the calculation of  $R_i$  at that operating point. Measurements of  $v_b$  were taken across the fixed load while the aggregate input voltage was measured at the output terminals of the programmable DC power supply. It is important to note that as no bus control was present,  $v_b$  was free to vary and is governed by Eq. 2.23,

$$v_b = \lambda_i i_{i,r} (R_b - R_{loss}), \quad (2.23)$$

which includes the losses in the source-to-bus interconnect and is nonlinear in  $\lambda_i i_{i,r}$ . By using the measured value of  $v_b$  in Eq. 2.22, any additional resistive losses are included in the calculated value of  $R_i$  at that operating point.

This process was repeated for 35 discrete points to map the permissible operating space of the boost converter calibration topology. Using this data, a polynomial surface fit of 3<sup>rd</sup> order in  $\lambda_i$  and  $i_{i,r}$  was created to fully map the solution space within the bounds of  $\lambda_i$  and  $i_{i,r}$ . The completed solution space surface is shown in Figure 2.9 along with the 35 discrete  $R_i$  values. The  $R^2$  value of the surface fit was calculated to be 0.9939.



**Figure 2.9:** 3<sup>rd</sup> order polynomial solution space of Eq. 2.22 for  $v_i = 40$  V over the range  $20\% \leq \lambda_i \leq 80\%$  and  $0.5$  A  $\leq i_i \leq 3.5$  A.

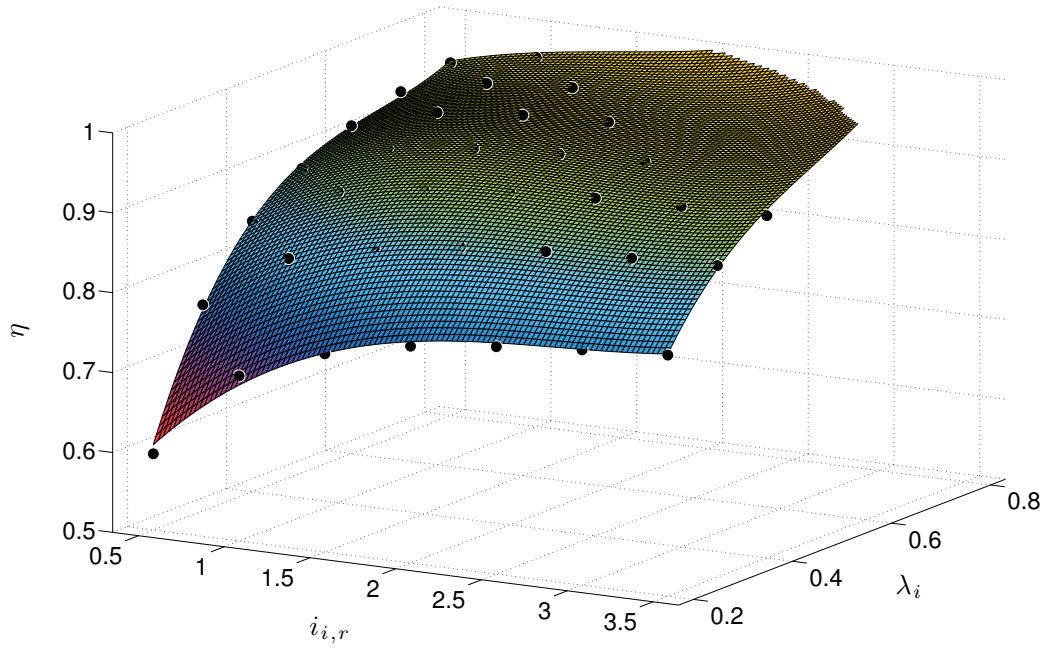
Examination of Figure 2.9 depicts a non-linear relationship in  $R_i$  as a function of  $\lambda_i$  and  $i_{i,r}$ . This behavior is best illustrated when considering  $R_i$  for low  $i_{i,r}$  values where a global maximum is found at maximum  $\lambda_i$  and minimum  $i_{i,r}$ . The results of this suggest that by moving the converter to a higher power operating point through the selection of  $\lambda_i$

and  $i_{i,r}$  the effective converter resistance may be decreased. Considering the efficiency of the boost converter within the permissible operating space provides further insight to this behavior where an interesting relationship between  $R_i$  and converter efficiency is illuminated. Defining the converter efficiency as the ratio of power out to power in per Eq. 2.24,

$$\eta = \frac{P_{out}}{P_{in}} = \frac{i_{i,r}\lambda_i v_b}{i_{i,r}(v_i + u_i)}, \quad (2.24)$$

the converter efficiency at each discrete operating point may be calculated. Shown in Figure 2.10 is a 3<sup>rd</sup> order polynomial surface fit of the converter efficiency when seeded by the results of Eq. 2.24.



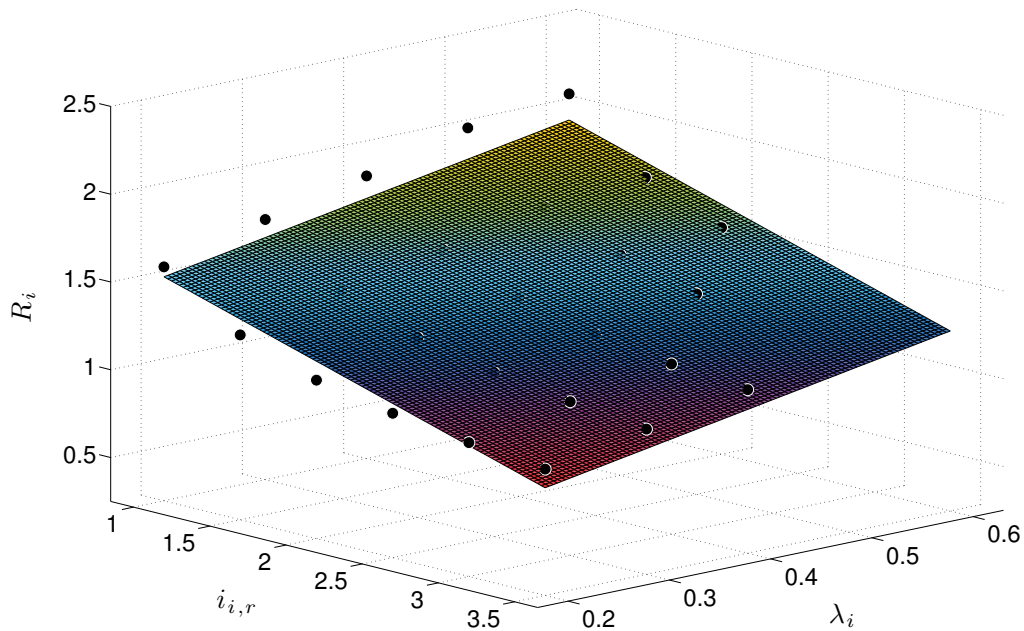


**Figure 2.10:** 3<sup>rd</sup> order polynomial solution space of Eq. 2.24.

Considering the results of Figure 2.9 and Figure 2.10, it may be shown that  $R_i$  decreases and converter efficiency increases when moving to high power operating points through the selection of  $\lambda_i$  and  $i_{i,r}$  when  $\lambda_i$  is chosen to be less than or equal to its initial value. Moving to the same increased power operating point by selecting the proper  $\lambda_i$  and  $i_{i,r}$  where  $\lambda_i$  is free to be larger than its initial value results in even greater efficiency gains but at the cost of increased  $R_i$  relative to the previous operating point. This in turn suggests possible trade-offs between converter losses and overall efficiency through the selection of  $\lambda_i$  and  $i_{i,r}$ . Furthermore, the results suggest that the converter should not be operated at low power operating points, specifically those within the lower bounds of  $i_{i,r}$ . By restricting

the permissible operating space to exclude these points, efficiency losses may be mitigated while simultaneously decreasing the severity of the non-linear behavior in  $R_i$ . Limiting the operating range to  $20\% \leq \lambda_i \leq 60\%$  and  $1.0 A \leq i_i \leq 3.5 A$  yields the solution space of Figure 2.11 where a linear regression was found to have a  $R^2$  value of 0.9103. To assign a value to  $R_i$ , a statistical mean of  $1.4126 \Omega$  was calculated from the experimental data set of Figure 2.11. As the converter will typically be operating in this region, this approach is feasible.

The raw calibration data, as reported post quantization by the PC/104 stack, may be viewed in Appendix A.



**Figure 2.11:** Linear solution space of Eq. 2.22 for  $v_i = 40 V$  over the range  $20\% \leq \lambda_i \leq 60\%$  and  $1.0 A \leq i_i \leq 3.5 A$ .

## 2.5 Simulation Analysis

By considering the power flow  $\sum P_{out_i} = P_{bus}$ , where  $P_{out,i}$  is the source subsystem output power and  $P_{bus}$  is the power supplied to the bus, storage requirements are illuminated through the closed loop system response of Eq. 2.5. Using a Simulink model of the DC microgrid, two test cases are considered. The first of which is a constant power step event while the second concerns a power deficient step event.

For each case the following system parameters were used:

$$\lambda_1 = 0.40$$

$$\lambda_2 = 0.40$$

$$v_1 = 40.0 \text{ V}$$

$$v_2 = 40.0 \text{ V} \tag{2.25}$$

$$v_{b,r} = 100.0 \text{ V}$$

$$i_{1,r} = 1.5 \text{ A}$$

$$i_{2,r} = 1.5 \text{ A}$$

To match the test bench microgrid described above, the physical parameters were set to:

$$L_1 = 2.0 \text{ mH}$$

$$L_2 = 2.0 \text{ mH}$$

$$R_1 = 1.4126 \text{ } \Omega$$

(2.26)

$$R_2 = 1.4126 \text{ } \Omega$$

$$R_b = 102.6 \text{ } \Omega$$

$$C_b = 10.41 \text{ } \mu\text{F}$$

Per the closed loop system of Eq. 2.5, the loop gains were selected such that the converter current response maintain  $\omega_n = 600\pi \frac{\text{rad}}{\text{sec}}$  with 5% overshoot while bus voltage

be over-damped with  $\omega_n = 200\pi \frac{rad}{sec}$ . The loop gains of the Eq. 2.3 were set to:

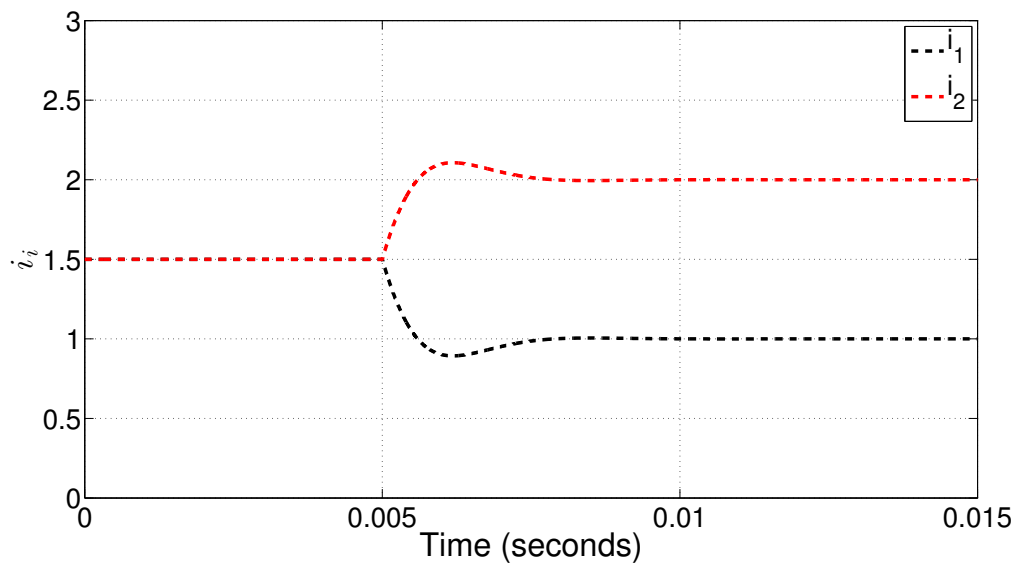
$$\begin{aligned}K_{P,1} &= 3.7906 \\K_{P,2} &= 3.7906 \\K_{P,b} &= 0.12107 \\K_{I,1} &= 7106.1 \\K_{I,2} &= 7106.1 \\K_{I,b} &= 4.1097\end{aligned}\tag{2.27}$$

It should be noted that for each simulation case the pre-filters of Eq. 2.20 were not used due to the time scale of the simulation.

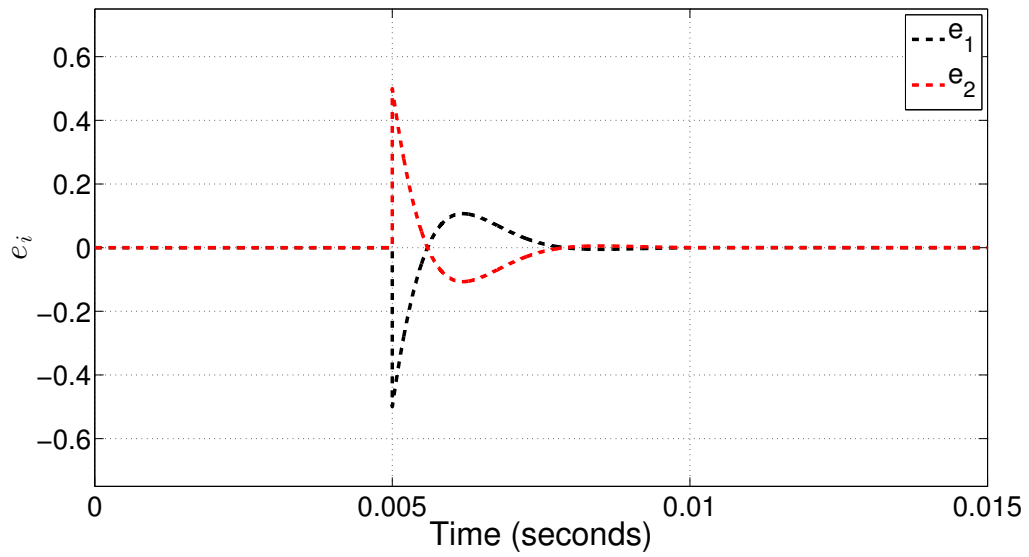
### 2.5.1 Case 1 Simulation - Constant Power Step Event

For this test case, each source subsystem is initially supplying 60 W of power to the bus through the  $\lambda_i i_{i,r} v_{b,r}$  term in Eq. 2.6. As the bus is of fixed resistance,  $R_b$ , the maximum power absorbed by the load is 97.47 W. This creates a surplus of power which is harvested by the bus storage device. From a control law standpoint, this is a negative commanded value in  $u_b$ . At  $t = 0.005$  seconds, a step change in  $i_{1,r} = i_{2,r} = 1.5$  A to  $i_{1,r} = 1.0$  A and

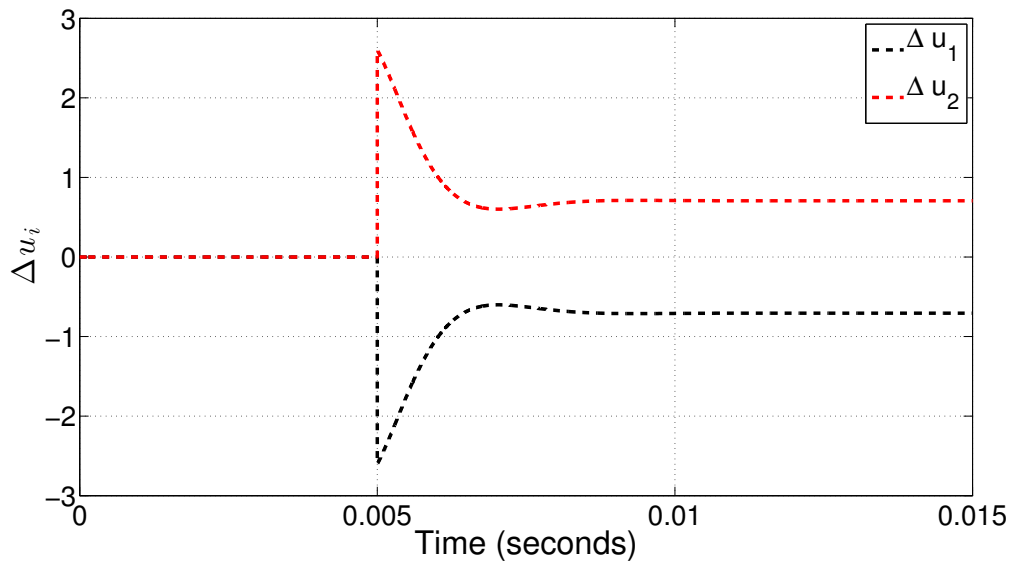
$i_{2,r} = 2.0 \text{ A}$  causes power distribution to shift from  $P_{out,1} = P_{out,2} = \frac{1}{2}P_{bus}$  to  $P_{out,1} = \frac{1}{3}P_{bus}$  and  $P_{out,2} = \frac{2}{3}P_{bus}$ . As the net power to the bus remains constant through the step event, no storage is required from the bus system and  $v_b$  is undisturbed. The results of this simulation are presented here where Fig. 2.12 depicts the state trajectories, Figure 2.13 the respective state errors, and Figure 2.14 illustrates the storage required to facilitate the step changes in  $i_{i,r}$ .



**Figure 2.12:** States  $i_1$  and  $i_2$  for case 1 step changes in  $i_{i,r}$ .



**Figure 2.13:** State errors  $e_1$  and  $e_2$  for case 1 step changes in  $i_{i,r}$ .



**Figure 2.14:**  $\Delta u_i$  in storage systems for case 1 step changes in  $i_{i,r}$ .

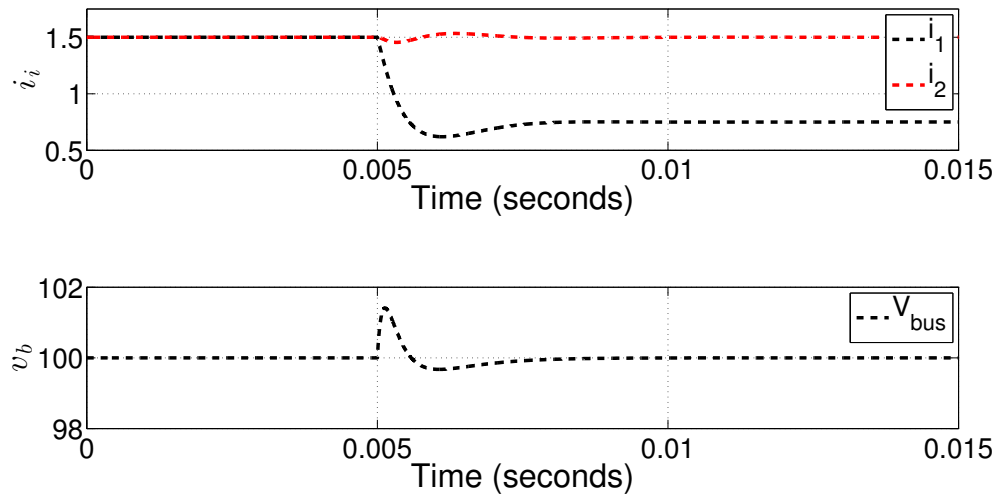
For step changes in  $i_{i,r}$ , the feed forward component  $R_i i_{i,r}$  of Eq. 2.3 overcompensates in its calculation of  $u_i$ . This is demonstrated in Figure 2.14 where the  $\Delta$ 's in  $u_i$  experience a

sudden jump when facilitating the step change in  $i_{i,r}$ . Here the feed forward component drives the converter currents towards the new reference value, quickly dissipating the state error as depicted in Figure 2.13, while the remaining error is corrected by the PI components. This overcompensation, in addition to the PI components of Eq. 2.3, results in the fast decay trajectory of the state error and subsequent  $2^{nd}$  order response with slight overshoot of the converter currents as shown in Figure 2.12. Inspection of the simulation results determined an effective time constant of  $\tau_{i_i} = 297.5 \mu s$  for the closed loop response of the source subsystems and  $\tau_{u_i} = 703.2 \mu s$  for the converter level storage.

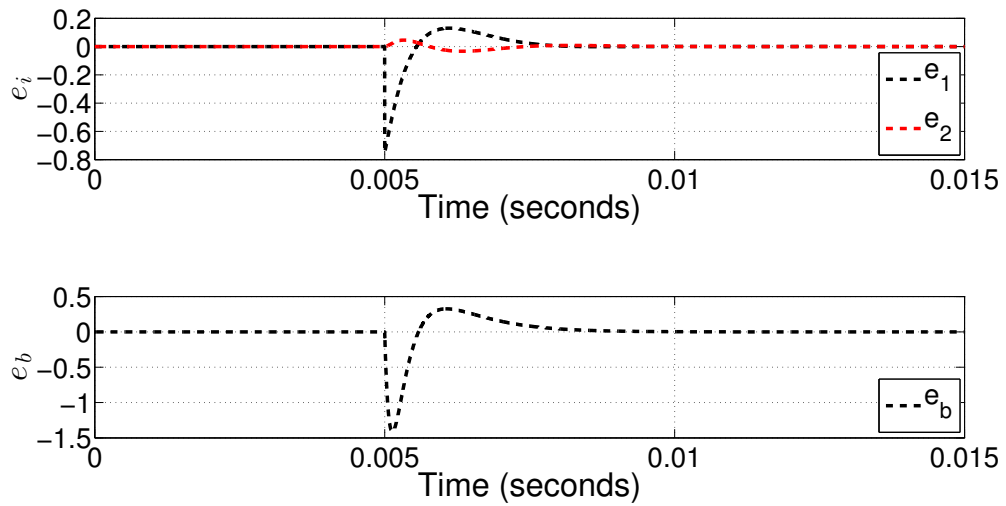
### 2.5.2 Case 2 Simulation - Power Deficit Step Event

Similar to the constant power step event of case 1, each source subsystem is initially supplying 60 W of power to the bus where a surplus of power develops. At  $t = 0.005$  seconds, a step change in  $i_{1,r}$  from 1.5 A to 0.75 A causes the power distribution to shift from  $P_{out,1} = P_{out,2} = \frac{1}{2}P_{bus}$  to  $P_{out,1} = \frac{1}{3}P_{bus}$  and  $P_{out,2} = \frac{2}{3}P_{bus}$ . The net power sourced to the bus is then  $\frac{3}{4}$  that of the initial power contributions from the source subsystems and creates a power deficit across the fixed load,  $R_b$ . A positive value in the  $u_b$  develops as the bus storage device must source current to maintain the reference bus voltage,  $v_{b,r}$ . The state trajectories are depicted in Figure 2.15, their associated error in Figure 2.16, and required storage in Figure 2.17.

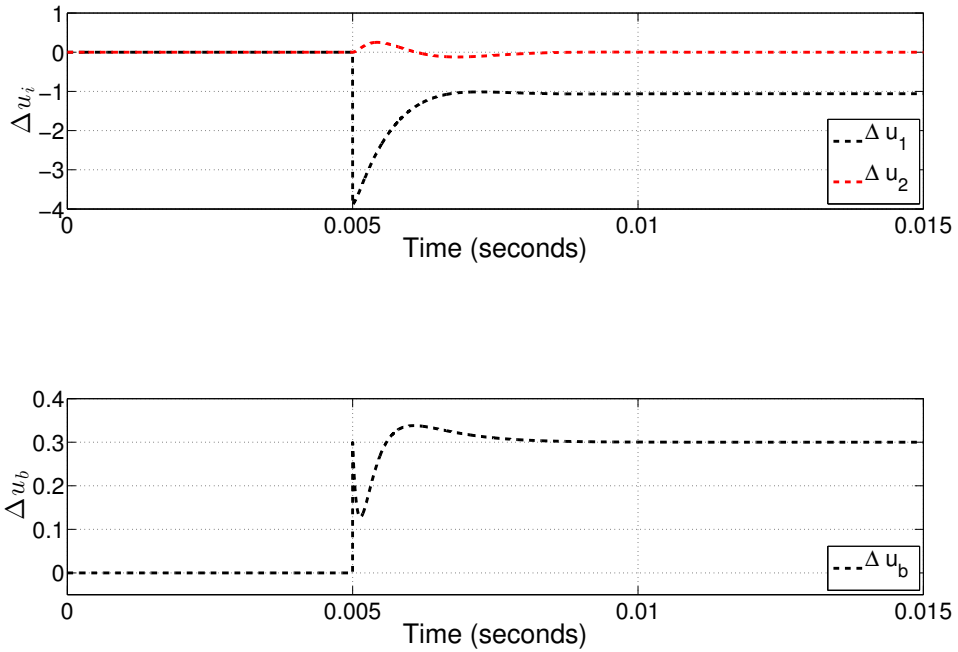




**Figure 2.15:** States  $i_1$ ,  $i_2$ , and  $v_b$  for case 2 step changes in  $i_{1,r}$ .



**Figure 2.16:** State errors  $e_1$ ,  $e_2$ , and  $e_b$  for case 2 step changes in  $i_{1,r}$ .



**Figure 2.17:**  $\Delta u_i$  in storage systems for case 2 step changes in  $i_{1,r}$ .

This  $\Delta$  in the net power supplied to the bus illuminates an interesting feature of the control law of Eq. 2.3 where a coupling effect in the closed loop system is observed. Per the results of Figure 2.17,  $u_1$  is shown to quickly drop negative due to the feed forward terms of Eq. 2.3 in order to facilitate the step change in  $i_{1,r}$ . Similar to the previous test case, the state trajectory of  $i_1$  exhibits the same  $2^{nd}$  order response with slight overshoot, as depicted in Figure 2.15, due to the PI controller terms. Further inspection of Figure 2.15 depicts a perturbation in the measured value of  $i_2$  which indicates a coupling effect in the closed loop system equations of Eq. 2.5. The mechanism of this coupling effect is best illustrated when

considering the state errors depicted in Figure 2.16. As  $i_{2,r}$  is held constant throughout the step event, the net power sourced to the load from the source subsystems experiences a net decrease. In order to maintain  $v_{b,r}$ , the bus storage device becomes active and sources additional power to the load through  $u_b$ . Doing so causes the bus voltage to deviate from  $v_{b,r}$  as it reacts to the  $\Delta$ 's in current being sourced to the load from the various subsystems. This results in a non-zero value in  $e_b$ , as depicted in Figure 2.16, which quickly decays due to the over-damped closed loop controls designed around  $u_b$ . Further inspection of Figure 2.16 depicts non-zero values in both  $e_1$  and  $e_2$  which helps illuminate the perturbation observed in the measured value of  $i_2$ . The closed loop control law of Eq. 2.5 confirms this as a source subsystem dependency on the bus voltage error term,  $\lambda_i e_b$ , and a bus subsystem dependency on the aggregate current error term,  $-\sum \lambda_i e_i$ , is observed. This in turn creates a perturbation in the source subsystem closed loop system equations where a non-zero value in  $e_2$  develops and gives rise to the coupling effect in the storage request of Figure 2.17. Furthermore, inspection of the simulation results determined an effective time constant of  $\tau_{i_i} = 264 \mu\text{s}$  for the source subsystem closed loop response and  $\tau_{u_i} = 611.6 \mu\text{s}$  for the converter level storage.

## 2.6 Experimental Analysis

The simulation cases of Section 2.5 were repeated in hardware to evaluate the closed loop performance of the HSSPFC law when using the calibrated reduced order converter model.

The system parameters were again set to those of Eq. 2.25. For the constant power step event of case 1,  $i_{1,r}$  and  $i_{2,r}$  were again changed from 1.5 to 1.0 A and 2.0 A, respectively. For the power deficit step event of case 2,  $i_{1,r}$  was changed from 1.5 A to 0.75 A. The loop gains were tuned experimentally to:

$$\begin{aligned}K_{P,1} &= 0.0125 \\K_{P,2} &= 0.0125 \\K_{P,b} &= 0.01 \\K_{I,1} &= 0.25 \\K_{I,2} &= 0.25 \\K_{I,b} &= 0.025\end{aligned}\tag{2.28}$$

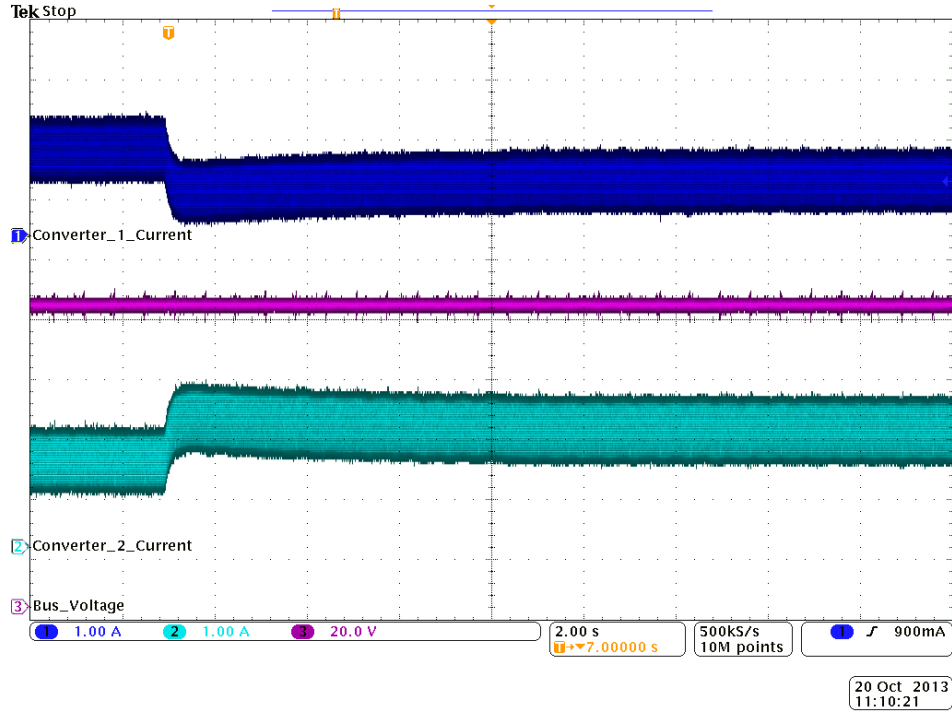
The loop gains of the PID controller used to drive the bus subsystem converter were set to:

$$\begin{aligned}K_P &= 0.1 \\K_I &= 2.5 \\K_D &= 0.001\end{aligned}\tag{2.29}$$

Data traces were captured using a Tektronix MSO 4054 Digital Oscilloscope with a sampling frequency of  $500\text{ kHz}$ .

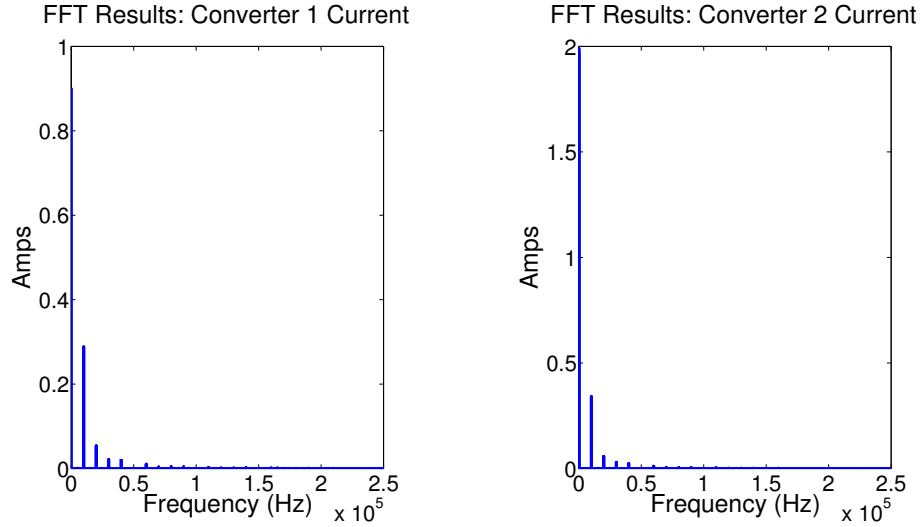
The high bandwidth current source/sink device of the bus subsystem was charged to  $\approx 30.0\text{ V}$  in order to support the considered test cases. This voltage was chosen such that the required conversion ratio to maintain the  $100\text{ V}$  bus reference value would keep the  $1 - \lambda_i$  term of the boost converter below  $0.85$ . Doing so prevents a nonminimum phase operating condition where the linear behavior of boost converter model begins to degrade [14]. The charging procedure was conducted by running the system in open loop while directing power from the source subsystems into the bus storage device. Upon reaching the desired voltage, the system was switched back to closed loop and allowed to reach steady state before being subjected to the step event.

## 2.6.1 Case 1 Hardware Testing - Constant Power Step Event



**Figure 2.18:** Experimental results for case 1 step changes in  $i_{i,r}$ .

Subjecting the realized microgrid to the test conditions of case 1 in Section 2.5 yielded the same second order behavior observed in simulation. The results are depicted in Figure 2.18 where the response was found to have a significantly slower time scale than the simulation results of Section 2.5.1.

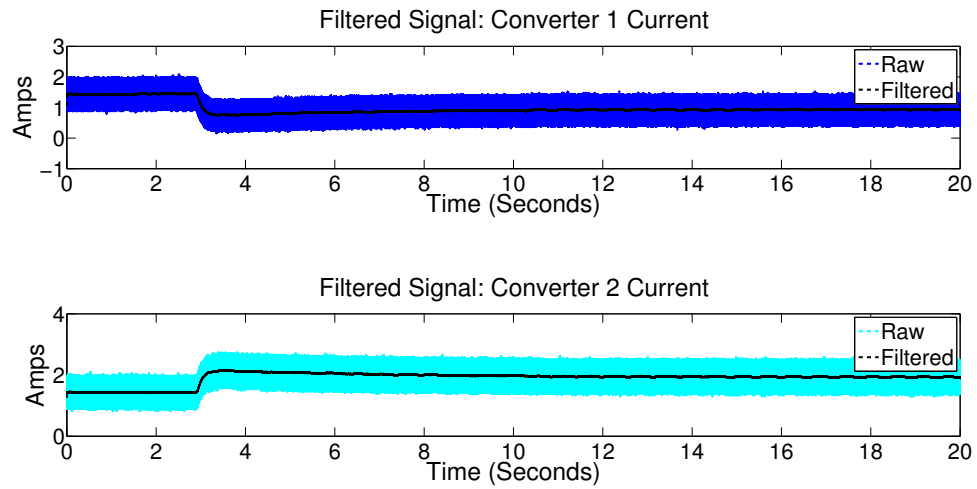


**Figure 2.19:** Converter current FFT results for case 1 step changes in  $i_{i,r}$ .

To better understand the response characteristics of the experimental results, the signal traces of Figure 2.18 were post processed within MATLAB. Shown in Figure 2.19 is the Fast Fourier Transform (FFT) of the source subsystem converter currents. From inspection it may be shown that both traces are dominated by a  $0\text{ Hz}$  signal component; this being the DC gain of the power converter current signal. This component was found to be  $0.902\text{ A}$  for  $i_1$  and  $1.992\text{ A}$  for  $i_2$ . Moving forward in the frequency spectrum illuminates signal component at  $10,000\text{ Hz}$  with additional components decaying in amplitude when increasing in  $10,000\text{ Hz}$  intervals. These components are artifacts from the switching frequency of power converter and its associated harmonics.

Having identified the signal compositions of Figure 2.18, a FIR low-pass filter with  $F_s = 500,000\text{ Hz}$  and  $F_c = 100\text{ Hz}$  was used to extract the DC current signals from the switching

noise of the power converter. The filter was designed at  $250^{th}$  order using a Hanning window to achieve a flat passband with 0 dB gain at 0 Hz for the specified filter parameters. The results of this are shown in Figure 2.20 where the closed loop response of the source subsystems was found to have effective time constants  $\tau_{i_1} \approx 100$  ms and  $\tau_{i_2} \approx 95$  ms.

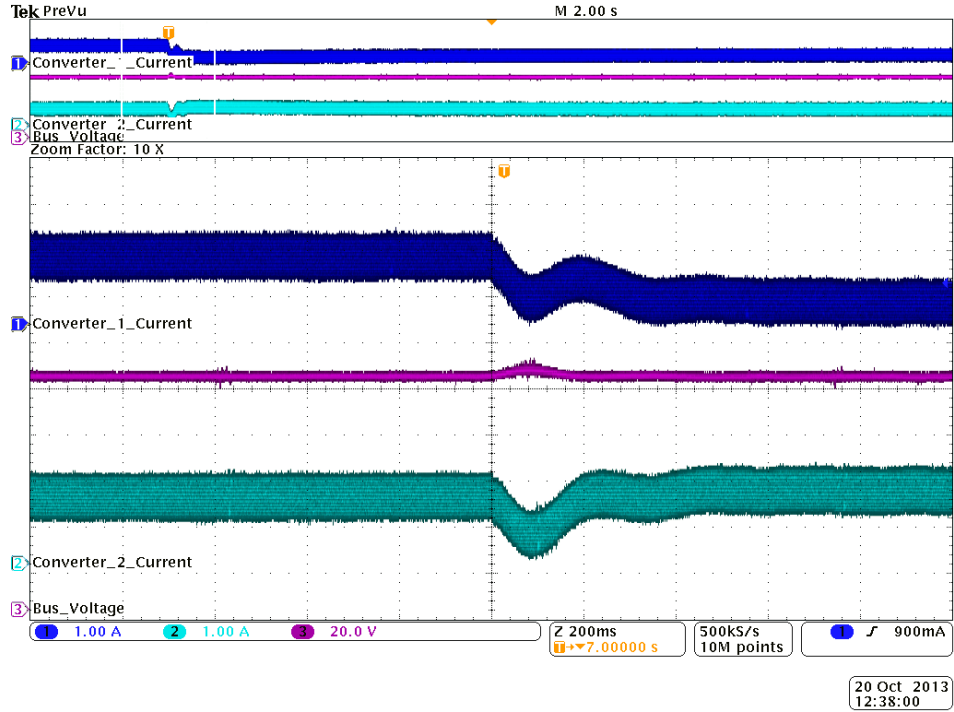


**Figure 2.20:** Filtered converter current signals for case 1 step changes in  $i_{i,r}$ .

The code used to process this data may be viewed in Appendix B.



## 2.6.2 Case 2 Hardware Testing - Power Deficit Step Event



**Figure 2.21:** Experimental results for case 2 step changes in  $i_{1,r}$ .

The closed loop coupling behavior introduced in Section 2.5.2 was again observed when subjecting the realized microgrid to the test conditions of case 2. For step changes in  $i_{1,r}$ , the required actuation through  $u_b$  to maintain the reference bus voltage induces a non-zero value in  $e_b$  and subsequently  $e_2$ . This non-zero value of  $e_b$  drives the closed loop response of  $i_2$  through the coupling term  $\lambda_i e_b$  resulting in the perturbation depicted Figure 2.21. This perturbation then drives the closed loop coupling term  $-\sum \lambda_i e_i$  through the non-zero values in  $e_i$  during the step event which contributes to the blip observed at  $t \approx 10$  seconds in the

bus voltage shown in Figure 2.21.

# Chapter 3

## Conclusions

This chapter presents a summary of findings per the results of Sections 2.5 - 2.6 where the value of HSSPFC in identifying storage requirements is examined. The importance of delineating the bandwidth characteristics of the feed forward and PI terms of the source subsystems of Eq. 2.3 is presented. Design considerations are addressed with regard to the frequency spectrum compositions of the closed loop system. Recommendations regarding the selection of loop gains in Eq. 2.3 are provided with the goal of reducing the coupling behavior observed in Sections 2.5.2 and 2.6.2. A more comprehensive approach in determining the converter resistance is postulated and an example case is formulated.

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Material contained in this chapter is planned for submission as a journal publication entitled "Realization of a DC Microgrid Utilizing Hamiltonian Surface Shaping and Power Flow Control".

### 3.1 Summary of Findings

Considering the simulation results of Section 2.5, the value of using HSSPFC in determining closed loop storage requirements is presented. Per the closed loop controller design, the resulting converter level storage should possess a  $2^{nd}$  order response with an effective time constant  $\tau \approx 600 - 700 \mu s$ . Having identified this, the results may be used as a design benchmark for realizing the converter level storage devices when considering the closed loop controller requirements. Furthermore, the results suggest that for sufficiently large  $\Delta$ 's in  $i_{i,r}$  the feed forward components  $R_i i_{i,r} + \lambda_i v_{b,r} - v_i$  of Eq. 2.3 contain significantly more bandwidth than their associated PI components  $K_{P,i} e_i + K_{I,i} \int e_i dt$ . This stresses the importance of both selected reference values and well-known converter losses if the closed loop system performance is to be extremized.

The hardware results of Section 2.6 tell a similar story where the loop gains were determined experimentally such that the closed loop response of the HSSPFC law was slower than that of the programmable DC power supply's internal controller. What this indicates is that for slow time scale analysis, the reduced order model approached developed in this work is valid. While this result is bounded within the limitations imposed by the programmable DC power supply, it is likely that the model reduction method will hold at faster time scales. If a higher bandwidth power supply could be sourced it is expected that the closed loop system performance could be increased significantly for the

test bench case presented in this work.

The FFT results of Section 2.6.1 provide an interesting design consideration when selecting the controller gains of Eq. 2.3. Should the design require a closed loop response near the 10,000  $Hz$  mark, stability issues may arise when considering the switching frequency of the power converter. An aggressive notch or bandstop filter designed to remove the switching artifacts from the system dynamics provides an elucidation to this issue. While not encountered in the realization process presented in this work, the notion of designing the closed loop controls around the power converter switching frequency band is an important consideration for future microgrids utilizing a similar hardware topology.

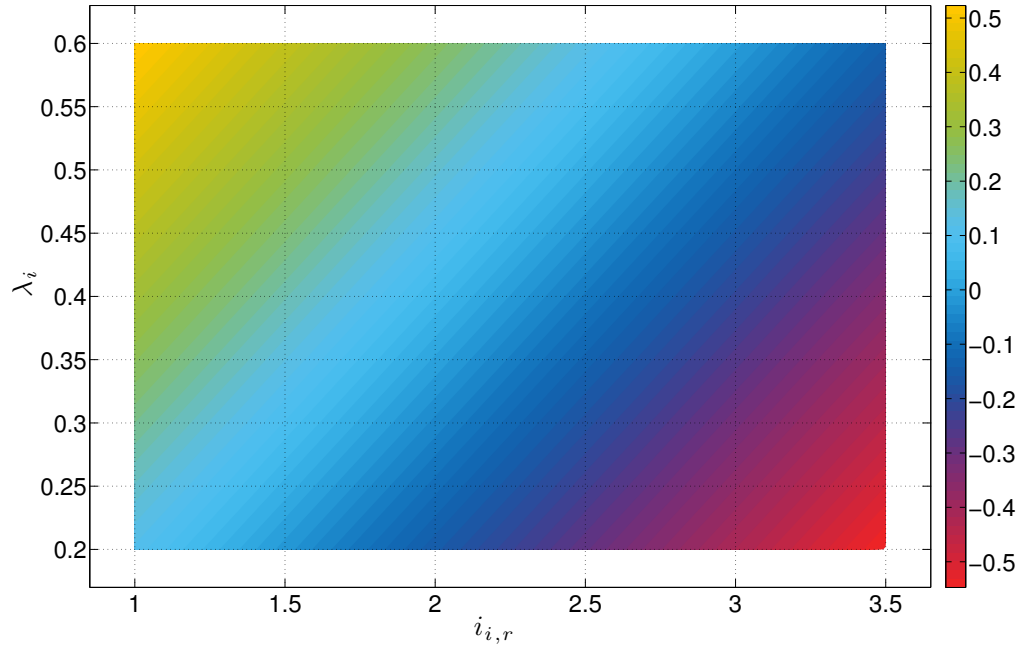
The simulation results of Section 2.5.2 for the power deficit step event of case 2 illuminates the effects of  $\Delta$ 's in the total power sourced to the fixed load through the source subsystems. This suggest that the closed loop controller specifications should be selected such that the bus storage is overdamped. Doing so minimizes oscillation in the controller effort when responding to  $\Delta$ 's in the total power sourced to the bus which would otherwise reflect back into the source subsystems through the coupling terms. Furthermore, this approach may be extended to the closed loop controllers deployed to the source subsystems such that any oscillations in converter current due to changes in  $i_{i,r}$  are minimized and reduce rippling in the bus voltage. Again, the hardware results depicted in Figure 2.21 echo those of the simulation results presented in Section 2.5.2 and experience the same time-scale reduction due to the hardware limitations of the programmable DC power supply. It is recommended

that the controller gains of Eq. 2.3 be selected such that they add significant damping to the closed loop system therefore minimizing the coupling effect of the HSSPFC law.

## 3.2 Future Work

While the statistical mean approximation for  $R_i$  quantified the converter resistance, it introduces an error in the  $R_i i_{i,r}$  feed forward component of Eq. 2.3 which results in the need for additional controller effort in the converter level storage device. Active Disturbance Rejection Control (ADRC) by Han presents an interesting method to address ambiguities in the plant model by considering the derivative of the plant response as an additional state through a state observer [15]. Through its application, the controller would be freed from its dependency on  $R_i$  altogether but require reformulation of the deployed controller solution. While ADRC would rectify this issue, an optimization approach presented as follows and is readily deployable to the realized system.

The absolute error between the linear solution space and mean calculated value of  $R_i$  is depicted in Figure 3.1



**Figure 3.1:** Absolute error between linear regression and calculated mean  $R_i$ .

Here it is shown that the resulting error in  $R_i$  is dependent on the selection of  $\lambda_i$  and  $i_{i,r}$ . One method to address this is to cast the selection of  $\lambda_i$  and  $i_{i,r}$  as an optimization problem which aims to minimize the error in  $R_i$ . Defining the zero error  $R_i$  operating point as  $\lambda_{i_0}$  and  $i_{i,r_0}$ , the cost function of Eq. 3.1,

$$J = \int (\lambda_{i_0} - \lambda_i)^2 + (i_{i,r_0} - i_{i,r})^2 dt, \quad (3.1)$$

accrues cost for selections of  $\lambda_i$  and  $i_{i,r}$  which deviate from the zero error  $R_i$  operating point. This in turn vectors the selection of  $\lambda_i$  and  $i_{i,r}$  towards minimum error in  $R_i$  if the cost function is subjected to the equality constraint of Eq. 3.2,

$$P_{optimal} = P_{HSSPFC}. \quad (3.2)$$

By defining  $P_{optimal}$  as the resulting converter output power through the optimal  $\lambda_i$  and  $i_{i,r}$  selections and  $P_{HSSPFC}$  is the commanded power output requirement from the HSSPFC control law, this method is feasible.

This approach is demonstrated through Fig. 3.1 where the zero error  $R_i$  operating point was found to occur at  $\lambda_i = 29.6\%$  and  $i_{i,r} = 1.8$  A. By defining  $\lambda_{i_0}$  and  $i_{i,r_0}$  appropriately, the cost function of Eq. 3.1 provides an elucidation to the shortcomings of the statistical mean calibration method presented in Section 2.4. As the operating point is likely to deviate from the zero error  $R_i$  operating point, additional overhead in converter level storage will be required. For significantly large microgrid topologies, this results in additional fiscal cost when realizing the system in hardware. The gravity of this becomes more apparent when considering storage cost of \$750 - \$1,000 per kWh for Li-ion battery storage mediums [7]. For the sake of this work, the additional storage required was considered negligible and the mean calculated value of  $R_i$  was used.



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# **Appendix A**

## **Converter Calibration Data**

**Table A.1**  
 Converter calibration data for  $R_i$  and  $\eta$  calculations.

$\lambda_i$	$i_r$	$u_i$	$v_i + u_i$	$v_b$	$R_i$	$P_{in}$	$P_{out}$	$\eta$
0.2	0.5	-36.8999	3.015	8.975	2.44	1.5075	0.8975	0.595356551
0.2	1.0001	-34.55	5.395	19.062	1.582441756	5.3955395	3.81278124	0.70665431
0.2	1.5001	-32.2336	7.753	28.996	1.302446504	11.6302753	8.69937992	0.747994325
0.2	2	-29.9142	10.085	38.895	1.153	20.17	15.558	0.77134358
0.2	2.5001	-27.6193	12.439	48.795	1.071957122	31.0987439	24.3984759	0.784548597
0.2	3.0001	-25.2998	14.773	58.675	1.012632912	44.3204773	35.2061735	0.794354566
0.2	3.5	-22.9987	17.109	68.575	0.969714286	59.8815	48.0025	0.801624876
0.300012	0.5	-34.5744	5.368	13.562	2.598474512	2.684	2.034381372	0.757966234
0.300012	1.0001	-29.8349	10.173	28.135	1.731989181	10.1740173	8.441681704	0.829729443
0.300012	1.5001	-25.0984	14.986	42.775	1.435228785	22.4804986	19.25080325	0.856333465
0.300012	2	-20.3436	19.808	57.535	1.27340479	39.616	34.52238084	0.871425203
0.300012	2.5001	-15.6224	24.605	72.155	1.183006336	61.5149605	54.12057939	0.879795402
0.300012	3.0001	-10.8982	29.415	86.793	1.125315317	88.2479415	78.11942844	0.885226637
0.300012	3.5	-6.1647	34.218	101.487	1.077337759	119.763	106.5656125	0.889804134
0.400006	0.5	-31.4249	8.556	17.941	2.758984708	4.278	3.588253823	0.83876901
0.400006	1.0001	-23.3222	16.782	37.305	1.859590211	16.7836782	14.92371605	0.889180302
0.400006	1.5001	-15.2593	24.973	56.625	1.548336944	37.4619973	33.97777466	0.906993143
0.400006	2	-7.1993	33.173	76.006	1.385071982	66.346	60.80571207	0.916494017
0.400006	2.5001	0.8332	41.315	95.294	1.278680147	103.2916315	95.29924123	0.922623061
0.400006	3.0001	8.8595	49.486	114.564	1.219863543	148.4629486	137.4834448	0.926045495
0.400006	3.5	16.8981	57.657	133.802	1.181542054	201.7995	187.3256098	0.928275887
0.5	0.5	-27.4728	12.571	22.145	2.997	6.2855	5.53625	0.880797073
0.5	1.0001	-15.1646	25.067	46.107	2.01329867	25.0695067	23.05580535	0.91967527
0.5	1.5001	-2.8535	37.591	70.171	1.670221985	56.3902591	52.63175855	0.933348408
0.5	2	9.4241	50.073	94.127	1.50475	100.146	94.127	0.939897749
0.5	2.5001	21.7322	62.568	118.184	1.390344386	156.4262568	147.7359092	0.944444444
0.599994	0.5	-22.663	17.448	26.475	3.1263177	8.724	7.942420575	0.910410428
0.599994	1.0001	-5.2736	35.122	55.059	2.086721682	35.1255122	33.03837315	0.940580538
0.599994	1.5001	12.1342	52.815	83.732	1.717420433	79.2277815	75.36307028	0.951220252
0.599994	2	29.548	70.476	112.327	1.540236981	140.952	134.7910521	0.956290454
0.699988	0.5	-17.1239	23.079	30.636	3.268335264	11.5395	10.72241618	0.929192442
0.699988	1.0001	6.4486	47.034	64.048	2.200948481	47.0387034	44.83731471	0.953200481
0.699988	1.5001	30.015	70.954	97.483	1.811259113	106.4380954	102.362219	0.961706602
0.799997	0.5	-10.5716	29.751	35.014	3.479810084	14.8755	14.00554748	0.941517763
0.799997	1.0001	20.127	60.929	73.256	2.324187349	60.9350929	58.61044069	0.961850354

# Appendix B

## MATLAB Code

### B.1 Data Analysis Script

```
% The following script parses the data collected on a
% Tektronix 4054 Digital Oscilloscope sampling at 500 kHz.
% The output is a FFT of the converter currents and
% filtered DC signals extracted from the switching noise
% of the converter.

% clear/close all
close all
clear all
clc

% import the data via import tool from the .csv file
% produced by the scope

load('case1_data.mat')
```

```

% structure the data as follows:

% current trace - ch 1

data.values(:,1)    = A;

% current trace - ch 2

data.values(:,2)    = A1;

% dt (seconds)

data.dt              = mean(diff(VerticalUnits));

% time vector (seconds)

data.time            = [data.dt:data.dt:data.dt...
                        *length(VerticalUnits)];

% vector header (names)

data.header          = {'Converter 1 Current',...
                        'Converter 2 Current'}

% clean up the workspace

clear A A1 VerticalUnits

save('data.mat')

% parse the workspace for .mat files (allows for modularity)

data_set_ID          = dir('*.mat');

% loop through available options and construct list to
% choose from

disp(sprintf('\nSelect File: \n'));
for i = 1:length(data_set_ID)
    data_string       = [num2str(i), ': ',...
                        data_set_ID(i).name, '\n'];

```

```

        disp(sprintf(data_string))
    end

% prompt to make a selection

data_set_selection = input('Data Set Selection:');
while (isempty(data_set_selection) || data_set_selection...
    <= 0 || data_set_selection > length(data_set_ID))
    disp(sprintf('\n Invalid Selection! \n'))
    data_set_selection = input('Data Set Selection:');
end

% load the data set

signal_set = importdata(data_set_ID...
    (data_set_selection).name)

% setup DSP params

% load FIR filter coefficient vector from FDA tool:

load('filter_coefficients.mat')

% FIR a vector

a_vec = zeros(1,...
    length(filter_coefficients));

% init to 1...

a_vec(1) = 1;

% FIR b vector

b_vec = filter_coefficients;

% block size (N)

N = size(signal_set.values,1);

% sampling frequency (Hz)

```



```

Fs          = 1/signal_set.dt;

% time step (seconds)

dt          = signal_set.dt;

% run FIR LPF and FFT script

for i = 1: size(signal_set.values,2)

    % FIR LPF – uses filtfilt to maintain phase

    signal_set.filtered(:,i) = filtfilt(b_vec, a_vec, ...
                                       signal_set.values(:,i));

    % fft analysis

    % normalize for window

    [sig_normalized, ...
     scale_factor] = heath_normalize(...
                    signal_set.values(:,i));

    % compute fft

    [fft_solution, ...
     frequency_spectrum] = heath_fft(...
                            sig_normalized, ...
                            N, Fs, 2, 1);

    % re-scale the signal

    signal_set.fft(:,i) = fft_solution ...
                        * scale_factor;

    % save off freq spec

    signal_set.fft_freq(:,i) = frequency_spectrum;

end

```

## B.2 Fast Fourier Transform Script

```
function [fft_sol , freq_spectrum] = heath_fft(sig , N,...
                                             Fs, wind, correction)

% The following function produces a single sided linear
% amplitude spectrum FFT on the input signal, sig.
% It requires the block size, sampling frequency,
% and the input signal.

% compute the FFT for the input signal

    % calculate sampling parameters

    % time step (seconds)

    delta_t      = 1/Fs;

    % sampling period (seconds)

    T            = N*delta_t;

    % lowest resolvable freq (Hz)

    delta_f      = 1/T;

    % construct single sided linear frequency spectrum

    freq_spectrum = [0:delta_f:((N/2)-1)*delta_f];

    % calculate the requested window

    [wind, cf] = heath_window(N, Fs, wind, correction);

    % correct window orientation

    wind = transpose(wind);

    % apply window to the input signal

    sig = (sig.*wind)*cf;
```

```

% calculate double sided amplitude spectrum

fft_sol = fft(sig)/N;

% calculate single sided amplitude spectrum

fft_sol(2:N) = (2)*abs(fft_sol(2:N));

% return frequency spectrum (amplitude)

fft_sol = fft_sol(1:(N/2));

```

### **B.3 Fast Fourier Transform Window Script**

```

function [w, cf] = heath_window(N, Fs, wind, correction)

% The following function produces either a rectangular,
% hanning, or flattop window which may be applied to the
% input signal. It requires the block size and sampling
% frequency in addition to the input signal.

% construct a time history for the window

% time step (seconds)

delta_t      = 1/Fs;

time         = zeros(1, N);

% realitive time history (seconds)

time(1)      = 0;

for i = 2:N
    time(i) = time(i-1) + delta_t;
end

% create the window based on the user's selection
% 1: Rectangular Window
% 2: Hanning Window

```

```

% 3: Flattop Window

% calculate the requested window

if wind == 1

    w = ones(1, N);

elseif wind == 2

    w = 0.5 - 0.5*cos((2*pi*time)/(N/Fs));

elseif wind == 3

    w = 0.2395 - 0.4481*cos((2*pi.*time)/(N/Fs)) +...
        0.2585*cos((4*pi.*time)/(N/Fs)) + 0.0439*...
        cos((6*pi.*time)/(N/Fs));

end

% calculate the requested correction factor

if correction == 1

    cf = 1/mean(w);

elseif correction == 2

    cf = 1/(mean(w)^2);

end

```

## B.4 Fast Fourier Transform Normalization Script

```

function [sig_normal, sf] = heath_normalize(sig)

% The following function normalizes the input signal to an
% amplitude of 1 such that a window may be applied

sf = max(sig);

```

```
sig_normal = sig / sf;
```