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STOCHASTIC CHARGE TRANSPORT IN MULTI-ISLAND SINGLE-ELECTRON TUNNELING DEVICES

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STOCHASTIC CHARGE TRANSPORT IN MULTI-ISLAND SINGLE-ELECTRON TUNNELING DEVICES

By

Madhusudan A. Savaikar

A DISSERTATION

Submitted in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

In Engineering Physics

MICHIGAN TECHNOLOGICAL UNIVERSITY

2013

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This dissertation has been approved in partial fulfillment of the requirements for the Degree of DOCTOR OF PHILOSOPHY in Engineering Physics.

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To My Family

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Preface

The present dissertation is based on my PhD work in Engineering Physics that I carried out at Michigan Technological University during the period January-April 2007 and January 2008-December 2013. This preface serves as an explanation of my role in the research work that comprises each of the chapters that make up the body of this dissertation. The research studies conducted in this dissertation work include, in part, text and images published in the following peer-reviewed journal articles.

[1]. C. H. Lee, S. Qin, **M. A. Savaikar**, J. Wang, B. Hao, D. Zhang, D. Banyai, J. A. Jaszczak, K. W. Clark, J.-C. Idrobo, A.-P. Li, and Y. K. Yap, *Adv. Mater*. **25**, 4544 (2013).

[2]. **M. A. Savaikar**, D. Banyai, P. L. Bergstrom, and J. A. Jaszczak, *J. Appl. Phys*. **114**, 114504 (2013).

I have coauthored the two articles listed above and published in "*Advanced Materials,*" a journal of WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim and "*Journal of Applied Physics,*" a journal of AIP Publishing LLC. I have the necessary copyright permission (see the Appendix) to reproduce the text and images from the above listed journal articles in my PhD dissertation titled:

"STOCHASTIC CHARGE TRANSPORT IN MULTI-ISLAND SINGLE-ELECTRON TUNNELING DEVICES"

The work [1] was carried out by the modeling group led by Dr. John A. Jaszczak in collaboration with the experimental group led by Dr. Yoke Khin Yap at Michigan Tech. I worked on modeling and simulations of experimental devices made of boron-nitride nanotubes functionalized with gold quantum dots (QDs-BNNTs) under the guidance of Dr. John A. Jaszczak. Douglas Banyai from my group was involved in

important discussions when the simulations were carried out, and later while writing the manuscript. The experimental work on QDs-BNNTs was directed and performed by the group of Dr. Yoke Khin Yap that consisted of Chee Huei Lee, Jiesheng Wang, Boyi Hao, and Dongyan Zhang, and their collaborators Shengyong Qin, Kendal W. Clark, and An-Ping Li from the Center for Nanophase Materials Sciences (CNMS) and Juan-Carlos Idrobo from Materials Science and Technology Division at Oak Ridge National Laboratory. Chapter 3 of this dissertation includes, in part, the work published in [1].

The work [2] was carried out by the modeling group led by Dr. John A. Jaszczak at Michigan Tech. I worked on developing a new simulation tool, MITS, that enhances the simulation capabilities of single-electron devices. Later, I employed the tool to simulate and study charge transport in one-dimensional multi-island tunneling devices under the guidance of Dr. John A. Jaszczak. The co-authors Douglas Banyai and Dr. Paul L. Bergstrom were involved in important discussions when the simulations were carried out, and later while writing the manuscript. All the work in this publication is included in Chapters 2 and 3.

Chapter 4 is based on the mico-analysis of the data that is generated by simulating single-island and multi-island devices. The chapter details the physical mechanisms that I, along with Dr. John A. Jaszczak, have proposed that are responsible for Coulomb blockade and Coulomb staircase characteristics in single-island and multi-island devices. The chapter discusses the gate and the thermal effects on Coulomb blockade and Coulomb staircase characteristics. My contributions included extensive device simulations and the analysis of the generated data on the microscopic scale. Douglas Banyai and Dr. Paul L. Bergstrom were involved in important discussions when the

simulations were carried out. I plan to submit this work for publication in the near future.

The research work was further extended to two-dimensional systems in Chapter 5. Much of the simulation work involves investigations on systems, which are similar to those experimentally investigated at Michigan Tech by Dr. Daw Don Cheam and his fellow group members under the guidance of Dr. Paul L. Bergstrom. In this chapter, under the guidance of Dr. John A. Jaszczak and Dr. Paul L. Bergstrom I demonstrate, by device simulations, the existence of a dominant conducting path in disordered systems as was hypothesized earlier by another research group. The chapter discusses the effects of an external gate voltage and temperature on two-dimensional device characteristics, and the behavior of a device that is made of only the dominant conducting path nano-islands. I performed the device simulations of the virtual devices using MITS and analyzed the data. Douglas Banyai contributed by calculating the capacitances of the virtual device systems with his newly developed FEM solver, and participated in important discussions. I plan to submit this work for publication in the near future.

Acknowledgements

I would like to thank and express my sincere gratitude to the people who have contributed in the successful completion of this work. First of all, my heartfelt thanks to my advisors Drs. John A. Jaszczak and Paul L. Bergstrom for their constant support and the guidance they provided all along since I started working with them. I am immensely grateful to Dr. John A. Jaszczak for his mentoring and invaluable suggestions without which this work would not have been successfully completed. My sincere appreciation to Dr. Paul L. Bergstrom for giving me the opportunity to work on this interesting project and for his guidance especially on device related experimental issues. I am deeply indebted to them for whatever I have gained from them as a person during my stay at Michigan Tech.

Thanks to my committee members Drs. Ranjit Pati and Bryan H. Suits, and former committee member Dr. Anand Kulkarni whose suggestions have helped in shaping up the dissertation. Special thanks to Douglas Banyai who has contributed substantially especially with his FEM solver, and for all his help and important discussions during the course of the project. I am thankful to Dr. Daw Don Cheam for fruitful discussions on device related experimental issues. My sincere gratitude to Dr. Konstantin Likharev from Stony Brook for meaningful discussions, which helped me immensely during the start of the project.

I am grateful to the Physics Department chair Dr. Ravindra Pandey and the Physics Department for financial support during my graduate studies, and to all the faculty, staff, and fellow graduate students in the department of Physics for their support.

I would like to thank Dr. Gowtham Shankara for all the help he extended whenever there were issues with the computing facilities. I would also like to acknowledge the copyright holders who have given me the necessary permission to reproduce the figures from the published material. Many thanks to some wonderful people I have met and made friends with without whom life at Tech would not have been the same. Special thanks to all my teachers and friends who have contributed in some way or the other during the long journey of my life.

Most importantly my warm and heartfelt gratitude to my family especially my parents and my grandmother for their love and care. Their contribution has been immeasurable in shaping up my life. I would especially like to remember my late father whom I always looked up to as a mentor, a guide and as a friend. I am deeply and forever indebted to my parents and my family.

Houghton, MI | Madhusudan A. Savaikar

December, 2013

Abstract

The physics of the operation of singe-electron tunneling devices (SEDs) and singe-electron tunneling transistors (SETs), especially of those with multiple nanometer-sized islands, has remained poorly understood in spite of some intensive experimental and theoretical research. This computational study examines the current-voltage (*IV*) characteristics of multi-island single-electron devices using a newly developed multi-island transport simulator (MITS) that is based on semi-classical tunneling theory and kinetic Monte Carlo simulation. The dependence of device characteristics on physical device parameters is explored, and the physical mechanisms that lead to the Coulomb blockade (CB) and Coulomb staircase (CS) characteristics are proposed.

Simulations using MITS demonstrate that the overall *IV* characteristics in a device with a random distribution of islands are a result of a complex interplay among those factors that affect the tunneling rates that are fixed *a priori* (e.g. island sizes, island separations, temperature, gate bias, etc.), and the evolving charge state of the system, which changes as the source-drain bias (V_{SD}) is changed. With increasing V_{SD}, a multi-island device has to overcome multiple discrete energy barriers (up-steps) before it reaches the threshold voltage (V_{th}). Beyond V_{th}, current flow is rate-limited by slow junctions, which leads to the CS structures in the *IV* characteristic. Each step in the CS is characterized by a unique distribution of island charges with an associated distribution of tunneling probabilities.

MITS simulation studies done on one-dimensional (1D) disordered chains show that longer chains are better suited for switching applications as V_{th} increases with

increasing chain length. They are also able to retain CS structures at higher temperatures better than shorter chains. In sufficiently disordered 2D systems, we demonstrate that there may exist a dominant conducting path (DCP) for conduction, which makes the 2D device behave as a quasi-1D device. The existence of a DCP is sensitive to the device structure, but is robust with respect to changes in temperature, gate bias, and V_{SD}. A side gate in 1D and 2D systems can effectively control V_{th}. We argue that devices with smaller island sizes and narrower junctions may be better suited for practical applications, especially at room temperature.

Chapter 1: Introduction

In the last few decades the semiconductor industry has continued tremendous growth due to the rapid development of microelectronics technologies. The development has lead to the integration of a large number of functionalities with increasing device density. The scaling down of device dimensions has kept pace with Moore's law, according to which the number of transistors on a single chip doubles almost every eighteen months. Increases in the feasible density of transistors on a single chip have led to the development of integrated circuits (ICs) that have several billion transistors. The larger transistor density has enormously increased the processing speed and the computing power of present day computers. With the present pace of integration processes physical dimensions in the device are expected to reach sub-10 nm range by 2020-2025.[1] The scaling-down process confronts major issues because of the basic physics at work at the nanometer scale. Major functional issues that confront the scaling of devices down to these dimensions, especially in the mainstream metal-oxide-semiconductor field-effect-transistor (MOSFET) devices include gate leakage, power dissipation, quantum effects such as tunneling current, and non-deterministic behavior of charge transport. With these issues in mind, scientists and engineers from both academia and industry are looking at charging-effect-based tunneling devices, such as single electron devices (SEDs) and single electron transistors (SETs), as one of the prime possible candidates that would drive the future of micro- and nano-electronics revolutions. Low power dissipation, small size and strong charge sensitivity make SETs a promising prospect in future ultra-large-scale integration (ULSI) technology. To realize

this dream and to suggest ways that can optimize the fabricated SED and SET devices, the understanding of the physics of electron transport in these devices is indispensable. This dissertation is a step forward that addresses a few of the questions regarding single electron transport that have remained unanswered for a long time.

1.1 Single Electron Device: A Simplistic View

A SED is an electronic device in which the device current can be controlled at the level of a single electron, and either adding or removing a single electron to or from the system can change the device state. In a SET device, the process can be controlled by an external electrode known as a gate. A very simple SET structure (Fig. 1.1) consists of either a metallic or a semiconducting nano particle called a nano-island or a quantum dot that is separated from the two electrodes, the source and the drain, by insulating gaps made of a dielectric material. Since the electrons can tunnel between the island and the electrodes through the gaps, the gaps are called tunneling junctions. The gate is capacitively coupled to the central island.

SEDs and SETs operate on the principle of Coulomb blockade, wherein any transfer of an electron onto or from the island is suppressed at low bias and at low temperature if the charging energy of the nano-island is sufficiently large. For an electron to transfer through the tunneling junction, a minimum energy from an external source has to be supplied to overcome the charging energy barrier and make the device conduct. The basic conditions necessary for having a Coulomb blockade in the system are:

1. The charging energy of the island $E_c = \frac{e^2}{2C}$ has to be greater than the thermal

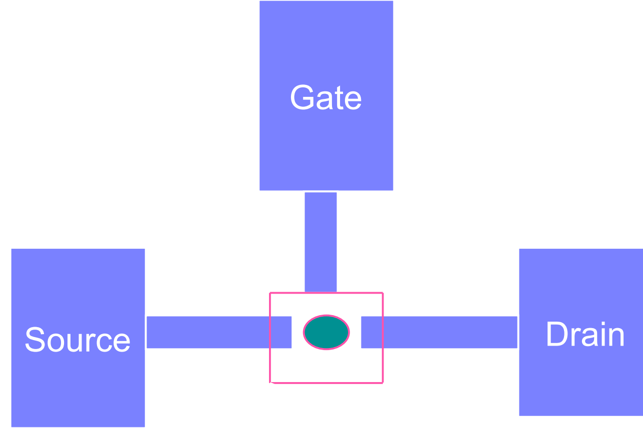

FIG. 1.1 A schematic of a simple single-island device structure. The electron transfer between the island and the electrodes takes place through the tunneling junctions.

energy $k_B T$, where k_B is Boltzmann's constant, e is electron charge, T is temperature and C is the total capacitance of the island. In the case of an isolated spherical island having a capacitance $C = 4\pi\varepsilon_0 r$, for $E_c = \frac{e^2}{2C} \geq k_B T$ at 300K, the capacitance has to be approximately $\leq 3aF$, while it has to be $\leq 12aF$ at 77K. Therefore, for the device to work at room temperature, the capacitance of the device needs to be on the order of $\leq 10^{-18}$ F, and hence the island size on the scale of ≤ 10 nm.

2. To ensure the localization of electrons on the island, the tunneling junction resistance needs to be much greater than the quantum resistance $R_Q = \frac{h}{4e^2} \approx 6k\Omega$, where h is Planck's constant.[2]

The nanometer island size and the large value of the junction resistances make tunneling the only source of current transport in such devices.

1.2 Experimental Single Electron Devices: An Overview

Aside from the simple single-island device structure, experimental devices have been demonstrated with multiple nanometer-size metallic or semiconducting islands, or quantum dots, deposited between two metallic electrodes, the source and the drain, forming a one-dimensional (1D) or a multi-dimensional (2D or 3D) device structure. The islands are isolated from one another by a dielectric material such as an oxide or a nitride that forms the tunnel junctions. The overall device current depends on the individual junction currents that flow through the tunnel junction between pairs of islands. The suppression of electron tunneling at low bias voltages and low temperatures in single-island and multi-island devices gives rise to unique non-Ohmic properties such as the Coulomb blockade and the Coulomb staircase in their *IV* characteristics that are a manifestation of charging effects of the nanometer-size islands.

Many research groups have been working on different developmental aspects of experimental SEDs and SETs exploring their use in a variety of potential applications. In a few cases, devices have been fabricated with just a single-island which display clear Coulomb staircases at room temperature.[3] On the other hand, multiple-island devices that show a large blockade potential at room temperature, useful for switching in multiple-level logic, have also been demonstrated.[4] Single-electron transistor (SET) devices have been explored to demonstrate their use as single-electron memory devices at room temperature.[5] Low power consumption and strong charge sensitivity make SET device a potential candidate for sensing and ULSI based applications.[6] SETs have been used for nanometer-scale displacement sensing,[7] while SEDs made up of arrays of tunnel

junctions have been used in thermometry and could substitute for commercially available field independent resistance and capacitance thermometers.[8] Recently quasi one-dimensional (1D) devices consisting of gold nano-islands deposited on boron nitride nanotubes have been shown to exhibit well-defined Coulomb blockade features and tunneling behaviors at room temperature.[9]

1.3 Dissertation Outline

The experimental work just described has been complemented by a tremendous amount of theoretical and computational research that addresses some of the fundamental issues faced experimentally and explains the physics of charge transport. Despite these prodigious efforts, the physics behind some of the interesting properties, especially in multi-island single electron devices, has remained unanswered. For example, the physical mechanism behind the staircase structure in multi-island devices is not clearly understood although it has been fairly well explained for single-island systems. Middleton and Wingreen[10] were able to explain the linear variation of the Coulomb blockade and the device threshold voltage with the number of islands along the device length in uniform two-dimensional devices having no inter-island coupling. But the cumulative influence of device disorder and the inter-island coupling strength on the linear behavior still remains unknown. The non-linear decrease in the device threshold voltage with the increasing temperature that has been observed in 1D chain of quantum dots[11] can not be convincingly explained by the percolation model proposed by Parthasarathy, *et al.*[12] The change in the exponent of the power law *IV* behavior with the increasing bias, observed

in quasi-one dimensional polymer nanofibers,[13] has not been convincingly explained. Cordan, *et al*.[14] in their study on 1D and 2D arrays of metallic dots proposed that there exists a dominant conducting path (DCP) in disordered multidimensional device structures that carries majority of the device current. In-depth studies are required to test and prove the hypothesis proposed by Cordan, *et al*.[14] We attempt to understand, by simulating the devices, the physics behind some of the above mentioned device properties that have been experimentally observed, and answer a few of the questions which have been posed by the experimental studies that are very relevant for single electron device applications.

In the next chapter, first we discuss the background and implementation of a new simulation tool, MITS, which has been developed within our group to simulate multi-island SEDs and SETs. This simulation tool adds to existing capabilities that other researchers have been using to study transport behavior in such devices. Next, several test cases are discussed wherein the capabilities of MITS are demonstrated, and the model is validated. In Chapter 3, MITS is used in an exhaustive study of single-electron transport in a disordered 1D device chain. The work was carried out in collaboration with the experimental group led by Y. K. Yap.[9] Chapter 4 is devoted to understanding the physics of the transport wherein the mechanism of the blockade and the staircase structure is investigated. The data generated from the 1D chain simulation studies is analyzed at the microscopic level in order to illuminate the possible mechanisms for the onset of conduction as well as for conduction after the threshold voltage is reached. The study answers some of the fundamental questions behind the blockade and the staircase structure in a single-island device, as well as in devices comprised of 1D chains of

different lengths. The effects of temperature and gate voltage on the device properties are then discussed. Having gained an understanding of the conduction mechanism in 1D chains, we further consider disordered 2D devices in Chapter 5. In particular we explore the hypothesis by Cordan, *et al*.[14] that in sufficiently disordered 2D SET devices there exists a dominant conducting path (DCP) that carries most of the device current. The 2D device characteristics are further compared with those of a quasi-1D chain made of only the DCP islands and junctions. Next, the effects of temperature and gate voltage on the device characteristics are investigated. Finally, we conclude in Chapter 6 with a brief discussion on the important observations from this study. We also suggest future work that needs to be pursued to add further capabilities to MITS, and future theoretical research that is required to expand our understanding of these devices.

References

[1]http://www.itrs.net/Links/2012ITRS/Home2012.htm.

[2]K. K. Likharev, Proc. IEEE 87, 606 (1999).

[3]V. Ray, R. Subramanian, P. Bhadrachalam, L. C. Ma, C. Kim, and S. J. Koh, Nat. Nanotechnol. 3, 603 (2008).

[4]P. S. K. Karre, P. L. Bergstrom, G. Mallick, and S. P. Karna, J. Appl. Phys. 102, 024316 (2007).

[5]K. Yano, T. Ishii, T. Hashimoto, T. Kobayashi, F. Murai, and K. Seki, IEEE Trans. Electron Devices 41, 1628 (1994).

[6]R. J. Schoelkopf, P. Wahlgren, A. A. Kozhevnikov, P. Delsing, and D. E. Prober, Science 280, 1238 (1998).

[7]R. G. Knobel and A. N. Cleland, Nature 424, 291 (2003).

[8]J. P. Pekola, K. P. Hirvi, J. P. Kauppinen, and M. A. Paalanen, Phys. Rev. Lett. 73, 2903 (1994).

[9]C. H. Lee, S. Qin, M. A. Savaikar, J. Wang, B. Hao, D. Zhang, D. Banyai, J. A. Jaszczak, K. W. Clark, J.-C. Idrobo, A.-P. Li, and Y. K. Yap, Adv. Mater. 25, 4544 (2013).

[10]A. A. Middleton and N. S. Wingreen, Phys. Rev. Lett. 71, 3198 (1993).

[11]K. Xu, L. Qin, and J. R. Heath, Nat. Nanotechnol. Lett. 4, 368 (2009).

[12]R. Parthasarathy, X.-M. Lin, K. Elteto, T. F. Rosenbaum, and H. M. Jaeger, Phys. Rev. Lett. 92, 076801 (2004)

[13]A. Aleshin, H. J. Lee, S. H. Jhang, H. S. Kim, K. Akagi, and Y. W. Park, Phys. Rev. B. 72, 153202 (2005).

[14]A. S. Cordan, A. Goltzene, Y. Herve, M. Mejias, C. Vieu, and H. Launois, J. Appl. Phys. 84, 3756 (1998).

Chapter 2: Development of a Multi-Island Transport Simulator (MITS): Theoretical Model, Testing, and Validation of MITS[1]

Although intense experimental research has been ongoing, continued development of robust simulation tools has been lacking for multi-island single-electron devices (SEDs). A few fairly robust tools have been developed for the simulation of SED and single-electron transistor (SET) circuits[1,2,3,4,5] for which independent knowledge of the electrical circuit parameters, namely, junction resistances and capacitances, is required. The utility of these tools is rather limited for studying SEDs as a function of more direct physical characteristics such as geometrical structures (e.g. the shapes, sizes and spacings of the islands, and some degree of randomness in these parameters), and the material properties of the constituent parts (e.g. the work functions of the islands, the dielectric properties of the substrate and the tunnel junctions, etc.). Furthermore, in multiple-island systems, the tunneling resistances of the junctions are not fixed but are expected to change with the voltage drop across the junctions that continuously change during the course of the simulation. It is therefore desirable to develop a physical model of SEDs that takes into account the geometrical structure of island arrays, disorder in the system, the material properties, and the state-dependent tunneling resistances.

In this chapter, we discuss the development of a new multi-island transport simulator, MITS, which can simulate multi-island SED behavior based on physical

[1] Much of the work in this Chapter was published in: M. A. Savaikar, D. R. Banyai, P. L. Bergstrom, and J. A. Jaszczak, "Simulation of charge transport in multi-island tunneling devices: Application to disordered one-dimensional systems at low and high biases." *J. Appl. Phys*. 114, 114504 (2013).

models, rather than circuit models of a device. Like other tools, it can also be used for circuit simulations of SEDs if the circuit parameters are known. On the other hand, unlike other tools, dynamically varying tunneling resistances, non-ideal behavior and non-uniform geometries can be successfully modeled with MITS, providing a strong linkage between the physical characteristics of the system and the resulting SED *IV* characteristics.

After describing the theoretical model and simulation flow in MITS, the capabilities and accuracy of MITS are demonstrated by simulating the devices described in the literature and comparing the results with those from the experiments.[6,7]

2.1 Theory and Simulation

2.1.1 Theoretical Model

For a given voltage across the source and drain electrodes, the current through a device is computed using kinetic Monte Carlo (KMC) simulation methods[8,9] based on computed electron tunneling rates across the junctions. The various tunneling probabilities at any given time depend on the charge states of the islands, the voltage drops across junctions, and junction tunneling resistances. Unlike most models, the tunneling resistances are not fixed, but instead depend on the voltage drops across the junctions at any given time, as is described below.

For the calculation of the tunneling rates we follow a semi-classical approach (orthodox theory) which assumes that (i) the energy spectrum of the conductive islands may be considered continuous, (ii) the tunneling time is negligible compared to the time

between tunneling events, and (iii) coherent tunneling events are ignored.[1,10] Condition (i) is a fair assumption taking into account the size and the metallic nature of the islands, which are expected to have sub-nanometer DeBroglie wavelengths. For a pair of adjacent islands *i* and *j*, the tunneling rate Γ_{ij} is thus given by[1,10,11]

$$\Gamma_{ij}(\Delta W_{ij}) = \left(\frac{-\Delta W_{ij}}{e^2 R_{ij}}\right)\left[1-\exp\left(\frac{\Delta W_{ij}}{k_B T}\right)\right]^{-1}, \tag{2.1}$$

where R_{ij} is the tunneling resistance of the junction, T is the temperature, e is the magnitude of electron charge, k_B is the Boltzmann constant, and ΔW_{ij} is the change in the free energy of the system due to the tunneling event (see below).

The tunneling resistance of a junction R_{ij} plays a key role in determining the tunneling rate across a junction, as it depends exponentially on the separation d_{ij} and the height of the potential barrier between the two islands that form the junction. From Fig. 2.1, it is seen that the barrier height is strongly influenced by the work function of the islands φ_i and φ_j and the potential drop V_{ij} across the two islands. It decreases approximately linearly from one island to the next given by $\varphi_{eff}(x) = \varphi_i - (\varphi_i - \varphi_j + eV_{ij})\frac{x}{d_{ij}}$ where x is the distance from the barrier interface. Since all of the islands in this case are of gold, $\varphi_i = \varphi_j = \varphi$ and $\varphi_{eff}(x) = \varphi - (eV_{ij})\frac{x}{d_{ij}}$. If the drop V_{ij} is small compared to φ, it has a negligible effect on the barrier height and R_{ij} remains constant. Under simulation conditions in which all the junction resistances in a given chain remain constant, the device IV characteristics follow a linear behavior for

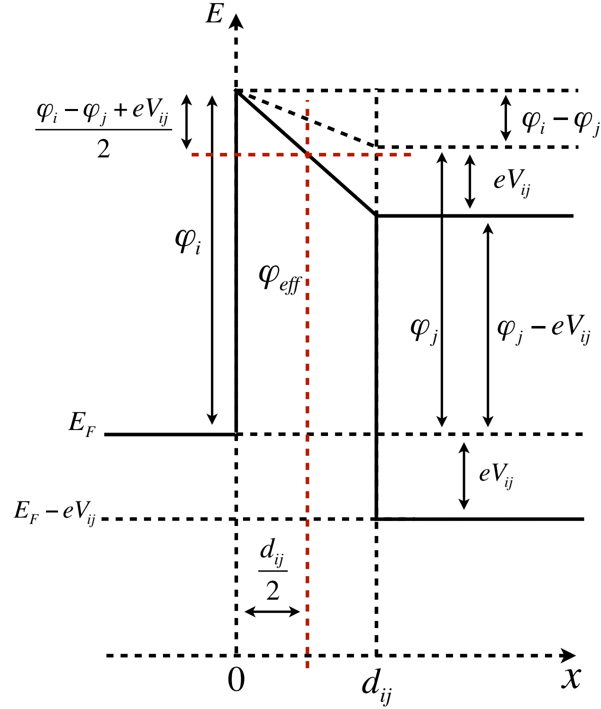

FIG. 2.1 The trapezoidal barrier model for band bending due to the potential drop across a junction coupling two neighboring islands, and the constant but reduced barrier height, shown in dashed red line, employed in our model.

large source-drain voltage biases. However, where there is a large charge build up or under large source-drain biases, the potential difference between the neighboring islands can be significant compared to the work function, leading to significant band bending. As a result, the effective barrier height would strongly depend on V_{ij}. To simplify the calculations, the tunneling barrier is taken to be of constant height across the width of the junction, but with a reduced height whose variation is given by $\varphi_{eff}(x) = \varphi_{eff} = \varphi - eV_{ij}/2$ (Fig. 2.1). This is a reasonable approximation as long as V_{ij} does not exceed φ.[12] Tunnel resistances also depend on other system parameters such as the Fermi energies, E_F,

and the island radii. Thus the tunneling resistance is given by[13]

$$R_{ij} = \left(\frac{h^3}{64\pi^2 m_e e^2}\right)\left(\frac{E_F + \varphi_{eff}}{E_F}\right)^2 \frac{\exp\left(2\beta k_0 d_{ij}\right)}{\varphi_{eff}}\left(\frac{\beta k_0}{r_a}\right)\frac{1}{G_{ij}} \ , \qquad (2.2)$$

where $k_0 = (2\pi/h)(2m_e\varphi_{eff})^{1/2}$, h is the Planck constant and m_e is the free electron mass. β is an enhancement parameter that accounts for tunneling from the sharp surfaces of the islands that are most likely to appear in the experimental devices due to the poor control on the fabrication process. The average radius of the two spherical islands forming the junction is r_a, and d_{ij} is the closest distance between their surfaces (the junction width). G_{ij} is a purely geometrical factor that takes into account the solid angle subtended by one spherical island at the other across the tunnel junction when considering the current flux and is given by[13]

$$G_{ij} = 1 - \left(1 - \left\{ r_a \big/ \left(r_a + d_{ij}\right) \right\}^2 \right)^{1/2} \qquad (2.3)$$

The change in free energy due to the transition is given by,

$$\Delta W_{ij} = -eV_{ij} + E_{c,ij} \ . \qquad (2.4)$$

ΔW_{ij} depends on the potential drop V_{ij} across the junction before the transition, which is influenced by the capacitances of the system and the charge state of the system. $E_{c,ij}$ is the junction charging energy, which is the energy required for a single electron transition across a junction between the two coupled islands, as determined by all the capacitances in the system.[1,10,11] The charge present on the island is influenced by the discrete charge tunneling to or from the island, continuous charge induced by an external electrode such

as a gate, or a background charge. Background charge is any charge that may exist in the form of charged impurities or traps that can influence the current flowing through the device. Background charge can also be caused by parasitic and stray capacitances that may induce charges on the nano-islands. For a one-dimensional (1D) system, an analytical method employing image charges was used for the calculation of junction capacitances, C_{ij}, between neighboring islands.[14,15] Using this method the junction capacitances are given by

$$C_{ij} = 4\pi\varepsilon\varepsilon_0 \frac{r_i r_j}{d_{c,ij}} (\sinh x) \sum_{n=1}^{\infty} (\sinh nx)^{-1}, \text{ where } x \equiv \cosh^{-1}\left[\frac{d_{c,ij}^2 - (r_i^2 + r_j^2)}{2 r_i r_j}\right], \quad (2.5)$$

r_i and r_j are the radii of the respective islands forming the junction, and $d_{c,ij}$ is the center-center distance between them. ε is the dielectric constant of the junction material and ε_0 is the vacuum permittivity. The number of image charges n required for good convergence consistent with the boundary conditions depends on the ratio of junction width to the radius of the spheres (*d/r*).[14] For the system studied here, 100 to 125 image charges were found to be sufficient for good convergence. In addition to all the junction capacitances, an individual junction charging energy also depends on the self-capacitance of all the islands in the system where the self-capacitance of the ith island is given by $C_{self}^{i} = 4\pi\varepsilon\varepsilon_0 r_i$. A finite-element-method (FEM) of calculating the capacitance has been developed (to be published) for systems composed of either a 1D or a two-dimensional (2D) array of islands.[16] In a multi-dimensional system, the neighboring particles are observed to have an appreciable effect on the inter-island capacitance and self-capacitance of the islands, which in turn may affect the resulting device characteristics.

A capacitance matrix is built by setting up a matrix equation $\boldsymbol{Q} = \boldsymbol{CV}$, where any diagonal element of the capacitance matrix C_{ii} is the sum of all capacitances associated with the respective island i, and the off-diagonal elements C_{ij} are the negative of inter-island capacitances. Since the potential matrix $\boldsymbol{V}$ consists of the known electrode potentials and the unknown island potentials, the capacitance matrix $\boldsymbol{C}$ is resolved into two parts, one that couples the island charge matrix to the known electrode potential matrix and the other that couples the island charge matrix to the unknown island potential matrix.[10] The matrix equation is then solved for the island potentials that are updated with each new charge state of the system.

The Monte Carlo method is a stochastic technique based on the use of random numbers and probability statistics to investigate the problems in diverse areas such as nuclear physics, economics and traffic flow. The kinetic Monte Carlo (KMC) method is generally employed for simulating complex, dynamical, physical systems.[8,9] For a process to be simulated by KMC method, the transitions need to be Poissonian in nature and independent of one another. The main idea behind the KMC method is to use known or computed transition rates in the system in order to select a new state of the system and to compute the change in the time. The method uses the standard n-fold way algorithm wherein the system evolves with time based on the transition rates thereby reflecting the microscopic kinetics of the system, The routine is efficient since each and every Monte Carlo step results in a transition with a probability that is proportional to its transition rate. The algorithm runs in the sequential steps as follows:

(i) Initialize the time $t = 0$.

(ii) List the rates Γ_{ij} of all the possible transitions in the system. The transitions to

be allowed are determined in advance by the model.

(iii) Sort the event rates Γ_{ij} in the ascending order giving an array $[\gamma_k]$, where γ_k is the kth event rate.

(iv) Calculate the accumulated rates $\Lambda_p = \sum_1^p \gamma_k$, where p runs from 1 to z. z is the total number of possible transitions, and $\Lambda = \Lambda_z$ is the sum of all the rates.

(v) Generate a random number y_i between 0 and 1.

(vi) Find the event x such that $\Lambda_{x-1} \le \Lambda \times y_i < \Lambda_x$ and carry out the event.

(vii) Update the time $t = t + \Delta t$, where $\Delta t = \frac{-\ln(y_j)}{\Lambda}$ and y_j is a random number between 0 and 1.

(viii) Update the system charge state and the system variables that may have changed. Update the transition rates Γ_{ij}.

(ix) Go back to (ii) and repeat the whole process until the desired termination point.

2.1.2 Simulation Flow

A comprehensive set of Monte Carlo simulation codes called MITS has been developed in MATLAB® to carry out the simulations. The workflow of MITS is shown in Fig. 2.2. First, a physical model of the device is generated using hard-sphere Metropolis Monte Carlo simulation to generate a configuration of spherical islands with the desired mean density (linear or areal in 1D or 2D, respectively), and a randomized distribution of sizes and spacings. For the 1D systems, the capacitances are calculated

using the analytical approach described above, while in a multi-dimensional system, the capacitances from the FEM solver[16] are given as fixed inputs to MITS.

FIG. 2.2 Simulation flow diagram of MITS that generates physical device configurations, solves for the electrical parameters from the physical properties, and simulates the *IV* behavior of the resulting device. Reprinted figure with permission from Savaikar, *et al.*, J. Appl. Phys. 114, 114504 (2013). Copyright 2013, AIP Publishing LLC.

The circuit-matrix solver in MITS builds capacitance matrices, which couple the varying island charges to the varying island potentials and the fixed electrode potentials (see section 2.1.1). With the capacitance matrices known, the charging energies for the transfer of a single electron are calculated across all the junctions in a given system.[10,11,17] For the given fixed electrode potentials and the known island charges (taken to be zero in the initial system configuration), the island potentials are then determined. The adaptive tunnel resistance solver computes the tunneling resistances across all the nearest-neighbor junctions in a 1D system. In a multi-dimensional system, resistances are computed for only those junctions whose widths are smaller than a pre-determined cut off. Once all the relevant parameters in the system are determined, tunneling rates across the junctions are computed. Following the kinetic Monte Carlo method, a particular tunneling event is randomly selected from among the available events, and the corresponding transition is carried out. Events having greater transition rates have a greater chance of getting selected. Once all the individual tunneling rates are known, the total tunneling rate and the lifetime of the current charge state are determined. After carrying out the transition, the charges on the islands and the time are updated. For the new system charge configuration, the potential drops, the tunneling resistances, and the tunneling rates across all the junctions are recalculated, and the process is repeated for large number of time steps until the current through the device reaches a steady state with satisfactory statistical accuracy.

In a 1D system, the number of time steps required for satisfactory statistical convergence of the measured currents increases with the number of junctions in the chain as N^2. For example, for the maximum chain-length (N = 200) studied at T = 0 K,

approximately 2×10^6 time steps were required to achieve a standard deviation of less than 5%. The number of time steps required increases substantially for non-zero temperatures, however. For example, the simulation time steps for a single point in the *IV* characteristic for a 100-junction device increased from $\sim1\times10^6$ steps at $T = 0$ K to $\sim5\times10^7$ steps at $T = 100$ K in order to achieve comparable precision in the current value. A thorough analysis needs to be done in order to understand the relationship, if there exists any, between the time steps required for satisfactory statistical convergence and the temperature.

In a multi-dimensional system the simulation time depends on the degree of disorder present in the system. For a system with a large degree of disorder, a large fraction of the total number of junctions that have comparatively high tunneling resistances may not play a significant role in the device conduction at any particular time, and it is reasonable to neglect those junctions. Therefore, while computing the charge transport in a multi-dimensional system, a tradeoff is required between simulation speed and accuracy without losing the vital information.

To increase the simulation speed, especially at higher temperatures, the single program/multiple data (SPMD) parallel computing capabilities in MATLAB® have been built into the MITS tool. By default, Matlab can use multiple cores, even in a serial computation on a multi-core machine, by employing its multithreading capabilities. However, since all cores are not utilized all the time in a serial computation, the codes have been modified to run in a parallel Matlab environment using its SPMD capabilities to take advantage of multiple cores on a single node. In parallel computing, the job is run exclusively on a specific core with a particular random seed thereby sparing the other cores for the parallel runs of the same job, each with a different random seed. These

divisions of a single job into multiple jobs running simultaneously and exclusively on multiple cores, each one with a smaller number of MC cycles and a different random seed instead of one single job with large number of cycles running in serial on multiple cores. This helps to reduce the simulation time by a factor that approximately equals the number of cores, especially in a 1D system, to get satisfactory average behavior. This feature is of great advantage, especially at higher temperatures where a large number of Monte-Carlo cycles are necessary to overcome the transients, to obtain values of the current to a satisfactory accuracy.

2.2 Testing and Validation of the Model and the Simulator

In order to test and validate MITS, three test studies are described in this section that compare experimental results for systems described in the literature with results for comparable MITS models. The first test demonstrates the capability of MITS in simulating a single-island device at non-zero temperature wherein the *IV* characteristics show a clear Coulomb staircase.[6] The second test is carried out to show its capability in simulating transistor characteristics where the effect of a gate on the *IV* characteristics is studied for a single-island device. The test also shows the effect of temperature on the observed gate oscillations. The third test looks at a multi-island device wherein a 1D chain of 50 junctions is simulated. This chain is taken to represent one dominant conducting path (DCP) in a multi-island multi-dimensional device with a distribution of sizes and spacings such as the device fabricated and studied by Parthasarathy, *et al*.[7] The

third test also proves the accuracy of the physical model used for the calculations of different system parameters such as tunneling resistance and capacitance, and hence the device current in 1D and multi-dimensional multi-island devices.

2.2.1 Test 1

Single-island devices have been fabricated by Ray, *et al.* [6] (Fig. 2.3) using gold nanoparticles positioned on the exposed sidewall of the dielectric film of silicon oxide that separates the source and drain electrodes, forming a vertically self-aligned structure. The current flow takes place between the source and drain through a single nanoparticle sitting on the exposed sidewall, effectively forming a single-island device. In order to simulate the corresponding device characteristics, the appropriate device parameters such as the capacitance, junction resistance, and the background charge along with the source-

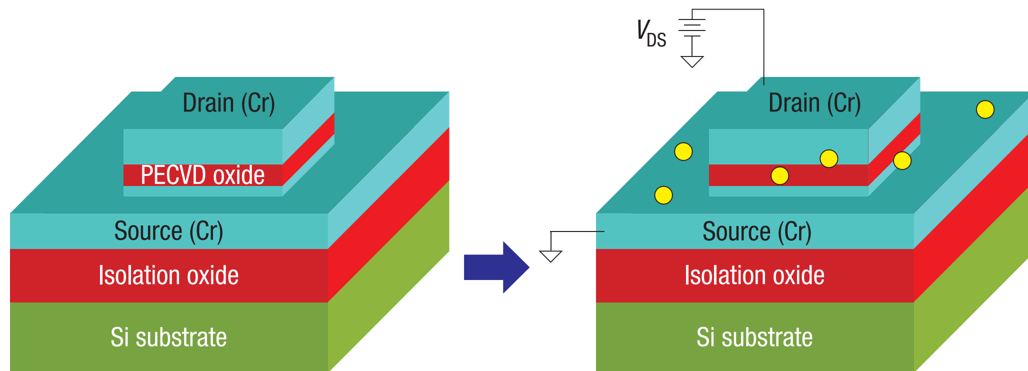

FIG. 2.3 The schematic of a single-island device fabricated by Ray, *et al.* [6] The sidewall of the PECVD oxide is formed along the periphery of the drain electrode and the nanoparticles are attached on the PECVD sidewall by immersing the wafer into gold nanoparticle colloid. Reprinted figure with permission from Ray, *et al.*, Nat. Nanotechnol. 3, 603–608 (2008). Copyright 2008 Macmillan Publishers Ltd.

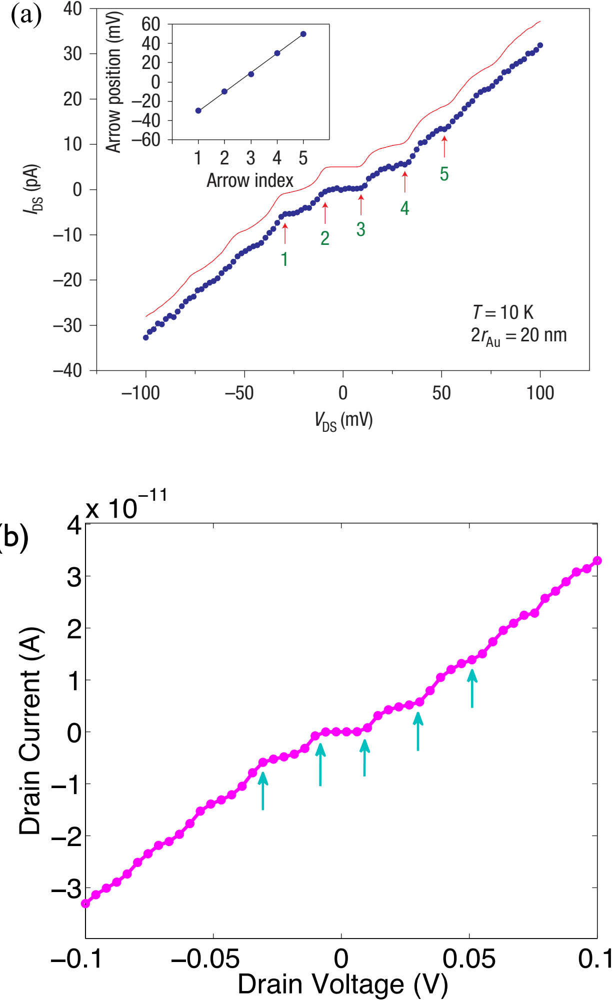

FIG. 2.4 (a) *IV* characteristics at T = 10 K of an experimental single-island device comprised of a ~20 nm colloidal gold particle (dots in blue), compared with simulation results using SIMON (solid line in red) by Ray, *et al.*[6] V_{DS} is the source-drain voltage. Reprinted figure with permission from Ray, *et al.*, Nat. Nanotechnol. 3, 603–608 (2008). Copyright 2008 Macmillan Publishers Ltd. (b) Simulated *IV* characteristics at T = 10 K using MITS using the following parameters gleaned from Ref. 6: junction capacitances $C_1 = 7.30\,\mathrm{aF}$, $C_2 = 0.88\,\mathrm{aF}$, fixed tunneling resistances $R_1 = 2.05\,\mathrm{G\Omega}$, $R_2 = 0.40\,\mathrm{G\Omega}$, and background charge $Q_0 = 0.05\,e$. The source electrode is set to ground. Key characteristics (indicated by the arrows) and scales are in good agreement with Ref. 6. Reprinted figure with permission from Savaikar, *et al.*, J. Appl. Phys. 114, 114504 (2013). Copyright 2013, AIP Publishing LLC.

drain bias from Ref. 6, are given as input to MITS. The experimental device *IV* characteristics from Ray, *et al.*[6] are shown in Fig. 2.4(a), along with simulation results they obtained using the code SIMON,[2,3] which uses a circuit model with fixed junction resistance and capacitance. In comparison, simulated device characteristics obtained using MITS are shown in Fig. 2.4(b). The scale of the current and key features, such as the Coulomb staircase step widths and the step positions, agree well with the experimental and SIMON results. The staircase structure is a manifestation of the charging effect due to the small size of the nano-island. With increasing bias, the step sharpness decreases and finally the steps disappear.

2.2.2 Test 2

A second test was carried out to demonstrate the capabilities of MITS in modeling single-electron transistor (SET) characteristics, such as device current modulation by a gate bias (V_G) and thermal effects on gate oscillation. The SET device was fabricated by Ray, *et al.*[6] by adding a gate electrode to the single-electron device architecture similar to the one described in Test 1 in section 2.2.1. The silicon oxide sidewall was surrounded by the gate electrode, forming a side gate structure. As in Test 1, the device parameters from Ray, *et al.*[6] are used for simulating the single-island transistor device. Figure 2.5(a) shows the Coulomb staircase of the experimental device consisting of a single island, and demonstrates the effect of the side gate on the Coulomb staircase. The simulated device characteristics shown in Fig. 2.5(b) using MITS are in good agreement with the experimental characteristics. The positive gate bias shifts the blockade, showing its asymmetric nature about $V_{SD} = 0$. Besides shifting the Coulomb staircase, the gate

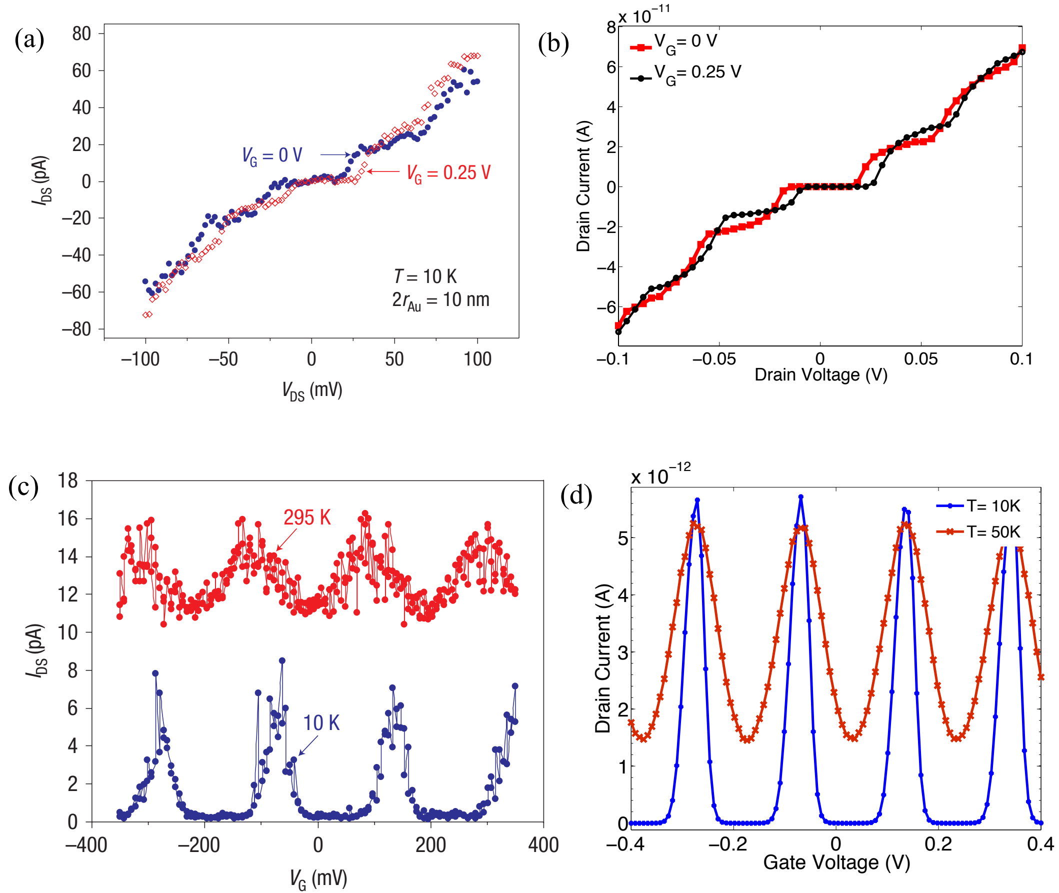

FIG. 2.5 (a) *IV* characteristics of an experimental single-island device comprised of a ~10 nm colloidal gold particle for different gate biases. (b) *IV* characteristics obtained by MITS using the same parameters as found in the experimental device. The gate bias shifts the Coulomb staircase without changing the blockade length. (c) Coulomb oscillations observed in an experimental single-island device comprised of a ~10 nm gold particle device at different temperatures and fixed V_{SD} = 10 mV. Room-temperature data are shifted by 10 pA for clarity. Reprinted figures (a) and (c) with permission from Ray, *et al*., Nat. Nanotechnol. 3, 603–608 (2008). Copyright 2008 Macmillan Publishers Ltd. (d) Simulated Coulomb oscillations using MITS at V_{SD} = 10 mV using the same parameters as in (c). Reprinted figures (b) and (d) with permission from Savaikar, *et al*., J. Appl. Phys. 114, 114504 (2013). Copyright 2013, AIP Publishing LLC. Parameters used for (b) and (d) are junction and gate capacitances $C_1 = 3.4\,\text{aF}$, $C_2 = 0.24\,\text{aF}$, $C_G = 0.78\,aF$, fixed tunneling resistances $R_1 = 0.79\,\text{G}\Omega$, $R_2 = 0.19\,\text{G}\Omega$ and background charge $Q_0 = 0.05\,e$.

appears to have an appreciable effect on the height of the staircase steps. The steps are also observed to be asymmetric about $V_{SD} = 0$ in the presence of a gate bias.

Figures 2.5(c) and 2.5(d) show Coulomb oscillations at different temperatures in the experimental and simulated devices respectively, when the gate bias is varied at a fixed V_{SD}. Since there is only a single island in the device, the oscillations are periodic with a period that depends on the gate capacitance (C_G). At higher temperatures, the current on/off ratio decreases with no appreciable change in the peak current, indicating that the temperature has no effect on the device current away from the threshold point. With increasing temperature, the period of the gate oscillation does not change but the oscillations begin to wash out due to thermal broadening, as can be seen from the increase in the oscillation peak width at higher temperature [Fig. 2.5(c), 2.5(d)]. The experimentally measured Coulomb oscillations in Fig. 2.5(c) show a shift in peak positions between the two temperatures that is not evident in the simulation results in Fig. 2.5(d). Such a shift in the peak positions is attainable in MITS simulations only by changing the background charge or the source-drain bias, but not by temperature changes alone. The peak shifts in Fig. 2.5(c) may therefore be due to slight differences in experimental conditions. We also believe that with an increase in the device temperature, the materials used in the experimental device may expand depending on their coefficients of thermal expansion. The material expansion is likely to affect the capacitances in the system thereby shifting the peak of the gate oscillation. Furthers investigations are necessary to test this hypothesis.

2.2.3 Test 3

Devices fabricated by Parthasarathy, *et al.*[7] consist of monolayers of 1-dodecanethiol-ligated gold nanocrystals deposited on silicon substrates coated with a 100-nm-thick layer of silicon nitride as shown in Fig. 2.6(a). The device has a quasi-two-dimensional structure in which the current paths are not expected to be straight but meander depending on the disorder and the void fraction in the system [Fig. 2.6(b)-(c)]. The inter-particle current flow takes place through the 1-dodecanethiol ligands that act as mechanical spacers between the particles, and which modify the height of the tunneling barrier.[18] The device structure has a narrow distribution of island radii (2.2 - 2.8 nm) and junction widths (2.2 - 2.6 nm).

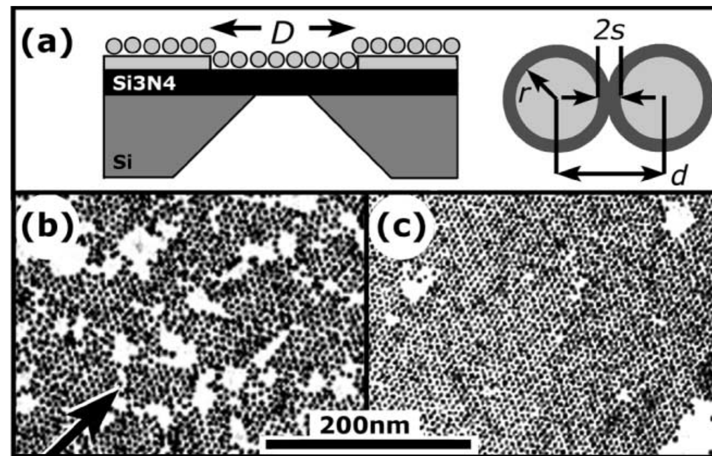

FIG. 2.6 (a) Sketch of a nanocrystal monolayer and in-plane electrodes (not to scale), and of the inter-particle geometry in a device fabricated by Parthasarathy, *et al.*[7] (b) TEM image of a typical array formed without excess dodecanethiol, showing many voids and an absence of long-range order. (c) Typical superlattice formed with excess dodecanethiol, showing < 5% voids and long-range ordering. Reprinted figure with permission from Parthasarathy, *et al*., Phys. Rev. Lett. 87, 186807 (2001). Copyright 2001 by The American Physical Society.

In a 2D system with a sufficiently broad distribution of junction widths, most of the device current might be expected to be carried by one dominant conducting path.[13] The number of current paths might increase as the junction-width distribution becomes narrower. To demonstrate the simulator capability, the experimental device fabricated by Parthasarathy, *et al.*[7] has been modeled by simulating a random 1D chain representing a dominant conducting path, and using the same distributions of island radii and junction widths as in the 2D device. The chain consists of 49 gold islands (50 junctions) that are expected to span the longitudinal length of the experimental device between the source and drain. The electron effective mass (= $0.42m_e$) and the tunneling barrier height (= 1.39 eV) parameters for such a system are chosen from Ref. 19. The experimental and the MITS-simulated *IV* characteristics at T = 12 K are shown in Figs. 2.7(a) and 2.7(b), respectively. Although the simulation results are in reasonable agreement with the experimental results, the current values are somewhat lower in the simulation. Since the experimental device is actually a two-dimensional structure having a relatively narrow distribution of junction widths, it is expected to have multiple current paths and thus higher current than would a single conducting path. Furthermore, even if there exists only a single dominant conducting path in the 2D device, it is likely to be made up of those junctions, which have smaller junctions widths with a distribution that is narrower than that in the full 2D device. These narrower junctions along the single dominant conducting path will drive up the current in 2D. Therefore the experimental 2D device current [Fig. 2.7(a)] is expected to be higher than the current through the simulated 1D device chain shown in Fig. 2.7(b). The possibility of having a staircase structure in the *IV* characteristics in a 2D device is less than that in a 1D device. If the 2D device has

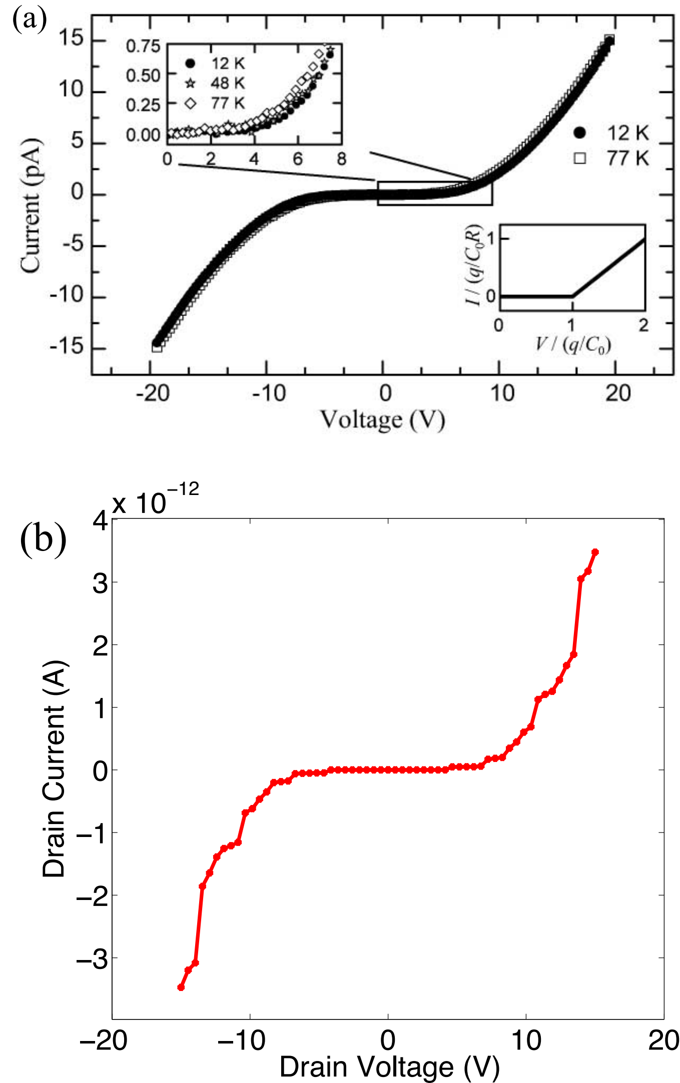

FIG. 2.7. (a) *IV* characteristics of a quasi-two-dimensional device consisting of gold nanocrystals with a narrow distribution of island radii (2.2 - 2.8 nm) ligated by 1-dodecanethiol, and with a narrow junction-width distribution of (2.2 - 2.6 nm). Reprinted figure with permission from Parthasarathy, *et al*., Phys. Rev. Lett. 87, 186807 (2001). Copyright 2001 by The American Physical Society. The magnified data in the inset gives an estimate of the Coulomb blockade threshold voltage. (b) Simulated *IV* characteristics at T = 12 K using MITS of a 1D chain of gold nanocrystals ligated by 1-dodecanethiol having similar distribution. Reprinted figure with permission from Savaikar, *et al*., J. Appl. Phys. 114, 114504 (2013). Copyright 2013, AIP Publishing LLC. The current scale and Coulomb blockade fairly agree with those in (a). The source is set to ground.

multiple conducting paths, multiple paths will wash out the discrete Coulomb staircase steps that any one path may have. On the other hand, if the device has a single dominant conducting path, the smaller junction widths along with their narrow distribution will minimize the chances of having a Coulomb staircase structure in the 2D. Multiple paths and capacitive effects from the islands outside of the dominant conducting path are expected to influence the Coulomb blockade and its sharpness at the threshold point. Despite these effects due to the dimensionality, the simulator gives a reasonable estimate of the current scale and the threshold voltage in the experimental device, thus validating its physical model.

References

[1]K. K. Likharev, Proc. IEEE 87, 606 (1999).

[2]C. Wasshuber and H. Kosina, Superlattices Microstruct. 21, 37 (1997).

[3]C. Wasshuber, H. Kosina, and S. Selberherr, IEEE Trans. Comput.-Aided Des. 16, 937 (1997).

[4]S. Amakawa, H. Majima, H. Fukui, M. Fujishima, and K. Hoh, IEICE Trans. Electron. E81-C, 21 (1998).

[5]N. Allec, R. G. Knobel, and L. Shang, IEEE Trans. Nanotechnol. 7, 351 (2008).

[6]V. Ray, R. Subramanian, P. Bhadrachalam, L. C. Ma, C. Kim, and S. J. Koh, Nat. Nanotechnol. 3, 603 (2008).

[7]R. Parthasarathy, X.-M. Lin, and H. M. Jaeger, Phys. Rev. Lett. 87, 186807 (2001).

[8]A. B. Bortz, M. H. Kalos, and J. L. Lebowitz, J. Comput. Phys. 17, 10 (1975).

[9]M. Kotrla, Comput. Phys. Commun. 97, 82 (1996).

[10]C. Wasshuber, *Computational Single-Electronics* (Springer, Wien, 2001).

[11]D. V. Averin and K. K. Likharev, in *Mesoscopic Phenomena in Solids*, edited by B. Altshuler *et al*. (Elsevier, Amsterdam, 1991), p. 173

[12]J. G. Simmons, J. Appl. Phys. 34, 1793 (1963).

[13]A. S. Cordan, A. Goltzene, Y. Herve, M. Mejias, C. Vieu, and H. Launois, J. Appl. Phys. 84, 3756 (1998).

[14]E. Pisler and T. Adhikari, Phys. Scr. 2, 81 (1970).

[15]J. Lekner, J. Electrost. 69, 11 (2011).

[16]D. Banyai, M. A. Savaikar, P. L. Bergstrom, and J. A. Jaszczak, (to be published).

[17]M. Amman, R. Wilkins, E. Benjacob, P. D. Maker, and R. C. Jaklevic, Phys. Rev. B. 43, 1146 (1991).

[18]R. Parthasarathy, X.-M. Lin, K. Elteto, T. F. Rosenbaum, and H. M. Jaeger, Phys. Rev. Lett. 92, 076801 (2004)

[19]W. Y. Wang, T. Lee, and M. A. Reed, Phys. Rev. B 68, 035416 (2003).

Chapter 3: Simulation of Disordered One-Dimensional Systems at Low and High Biases.[1]

Having established confidence in the utility of the MITS simulator, a detailed study was carried out on charge transport through a one-dimensional (1D) chain of gold nano-islands deposited on an insulating wire, following the experimental system described in Ref. 1, and as illustrated in Fig. 3.1. The system is modeled by a chain of 199 spherical conductors (islands), with nearest neighbors separated by an insulating tunnel junction (vacuum). The radius of each island is randomly selected from a uniform distribution between 3 and 10 nm [Fig. 3.2(a)], while the junction widths are randomly selected from a uniform distribution between 1 and 5 nm [Fig. 3.2(b)]. Approximate values of the Fermi energy, E_F, and the work function, φ, for gold have been chosen as 5.5 eV and 4.8 eV, respectively.[2] While the enhancement parameter β was taken to be 0.115 to set an overall current scale comparable to that measured by Lee, *et al.*[1]

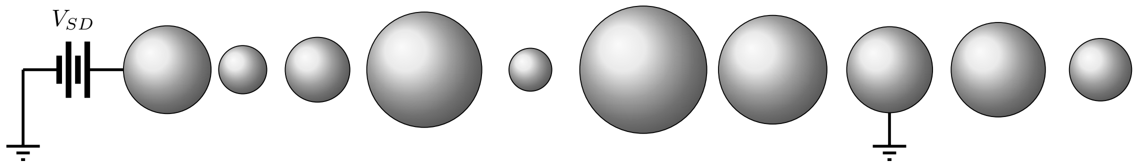

FIG. 3.1 Schematic of the geometrical model of a 1D chain of gold nano-islands deposited on an insulating wire used for the MITS simulation. The island radii and junction widths are randomly selected over uniform distributions to model the position of metallic islands in an experimental device fabricated by Lee, *et al.*[1] Reprinted figure with permission from Savaikar, *et al.*, J. Appl. Phys. 114, 114504 (2013). Copyright 2013, AIP Publishing LLC.

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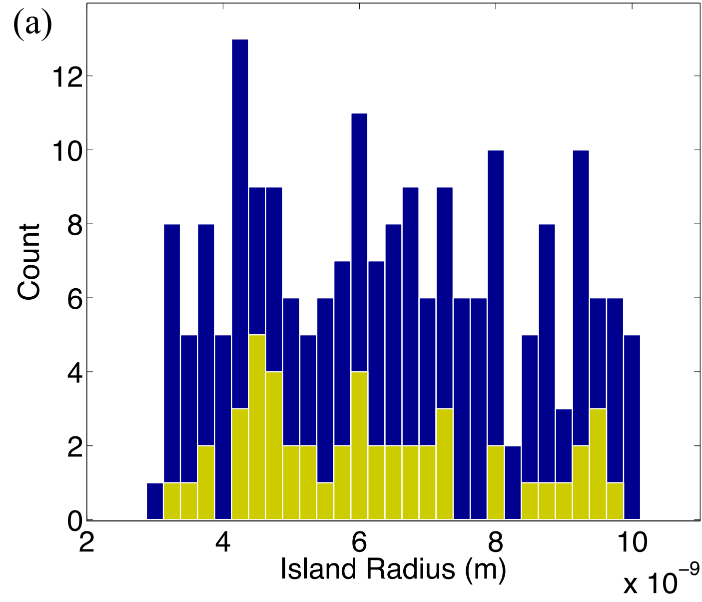
[1]Much of the work in this Chapter was published in Savaikar, *et al.*, *J. Appl. Phys.* 114, 114504 (2013). A subset of the work in this chapter was published in Lee, *et al.*, *Adv. Mater*. 25, 4544 (2013).



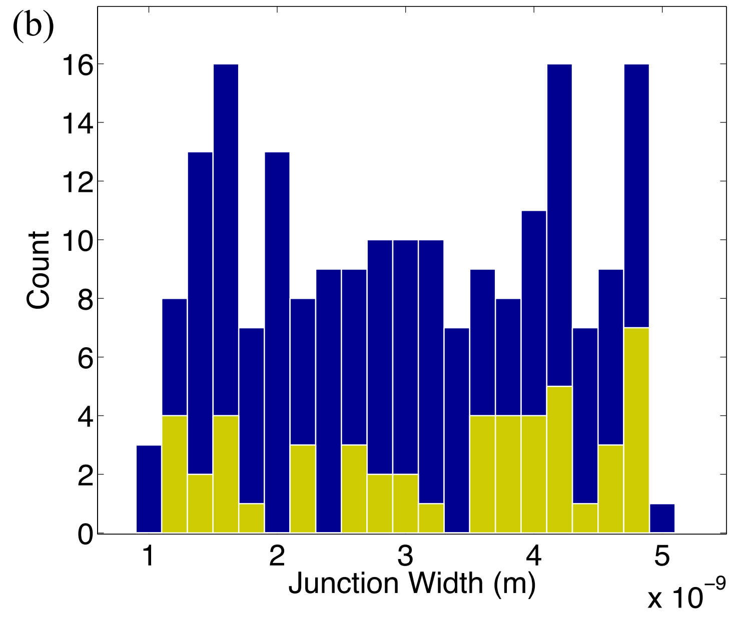


FIG. 3.2 (a) Distribution of radii of the islands along the chain of 50 junctions (yellow/light) and 200 junctions (blue/dark). (b) Distribution of widths of the junctions that couple the neighboring islands and through which the electron tunneling takes place. The 200-junction chain contains more small-radii islands and large-width tunneling junctions, which play a dominant role in determining the device characteristics. Reprinted figure with permission from Savaikar, *et al.*, J. Appl. Phys. 114, 114504 (2013). Copyright 2013, AIP Publishing LLC.

The dielectric constant ε of the junction material is taken as 1. A fixed island at the end of the chain is selected as the drain electrode, while the source electrode (fixed to ground) is chosen from among the remaining islands in the chain according to the desired number of islands in the system.

3.1 *IV* Characteristics in Low- and High-Bias Regime

IV characteristics of the device at $T = 0$ K are as shown in Fig. 3.3 for a series of different source-drain gap lengths, with the number of junctions (N) ranging from 12 to 200 junctions. Under large source-drain biases (V_{SD}) the *IV* characteristics are non-Ohmic [Fig. 3.3(a)]. By conducting separate simulations in which the tunneling barrier heights ($\varphi = 4.8$ eV) did not vary with V_{ij}, it was determined that the non-Ohmic nature of the *IV* characteristics originates from the reduction in the potential barrier height of the junctions, $\varphi_{eff}(x)$ [Fig. 3.4]. The overall resistance of the device also increases non-linearly with increasing chain-length (Fig. 3.5). As discussed later in Section 3.3, the overall device resistance is dominated by tunneling resistances across the wider junctions in the chain. With the increase in the length of the device, a larger number of wider junctions are sampled from the parent chain [Fig. 3.2(b)]. In addition, the maximum value of the junction width in the distribution, which has a dominant effect on the overall device resistance, may also increase with the increasing chain length.

IV characteristics at low V_{SD} exhibit discrete Coulomb staircase structures that are the manifestations of charging effects on the individual islands [Fig. 3.3(b)]. Furthermore, the steps of the Coulomb staircase are more pronounced for longer chain-length devices.

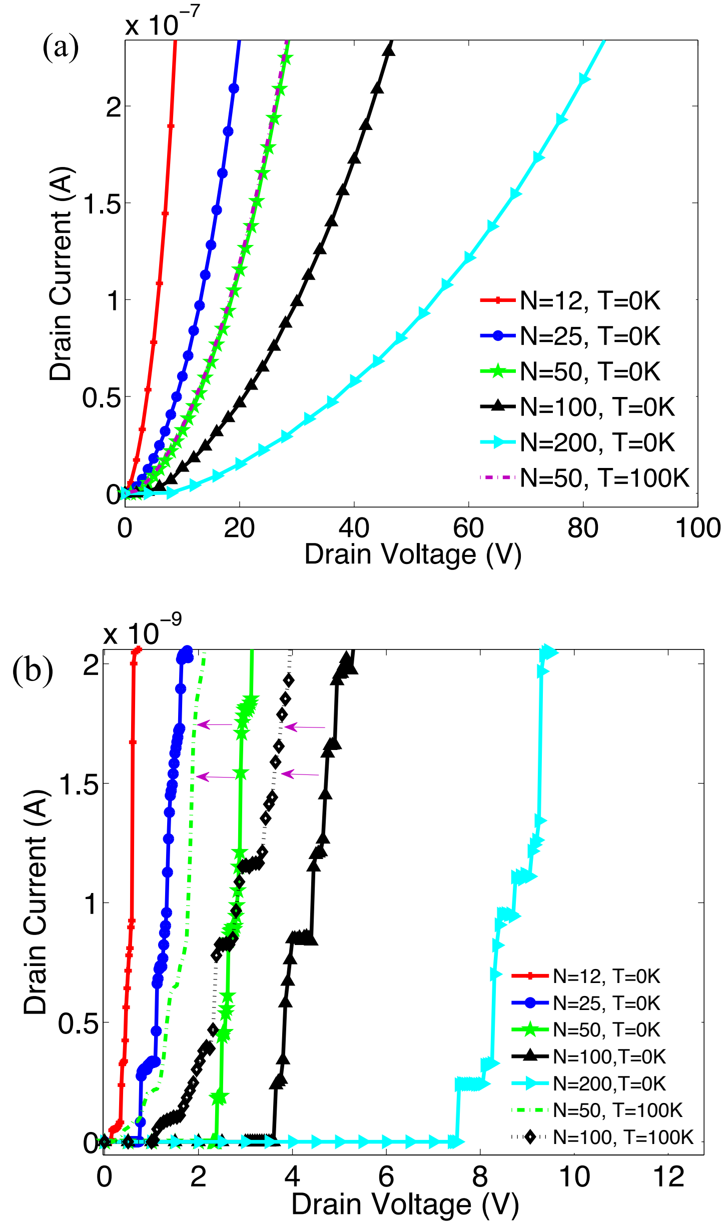


FIG. 3.3 (a) Simulated *IV* characteristics in the high-bias regime for devices with different numbers of islands (*N*-1). Non-Ohmic *IV* behavior stems from effective lowering of the tunneling barriers by the voltage drops across the junctions [see Fig. 3.4]. (b) Simulated *IV* characteristics at low biases revealing Coulomb staircase structures that are the manifestations of charging effects of the nano-islands. Solid lines show results for $T = 0$ K, and dashed lines show results for $T = 100$ K. Increase in temperature shortens the blockade length. Reprinted figure with permission from Savaikar, *et al*., J. Appl. Phys. 114, 114504 (2013). Copyright 2013, AIP Publishing LLC.

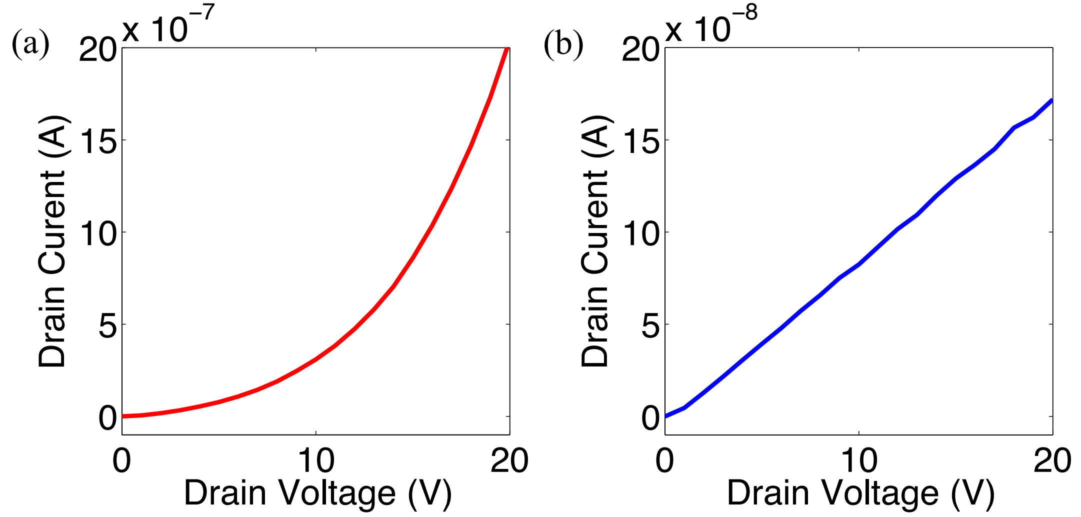


FIG. 3.4 (a) Non-Ohmic *IV* characteristics of a 12-junction chain showing the effect of tunneling junction barrier suppression that occurs due to the finite potential drop across the junctions. (b) Ohmic *IV* characteristics with constant tunneling junction barrier height of 4.8eV and no suppression. Fermi energy, E_F, and the work function, φ, for gold are taken as 5.5 eV and 4.8 eV, respectively.[2] Enhancement parameter β was taken to be 0.115.

The first step, which rises at the threshold voltage V_{th}, represents the opening up of the first conduction channel (temporal sequence of charge states of the islands that occurs with a certain probability and evolves with a set of rates) that carries current across the entire length of the device. Each subsequent step of the staircase represents the opening of a new channel (i.e. a different temporal sequence of island-charge states that occurs with another probability and evolves with a different set of rates) when V_{SD} reaches subsequent critical thresholds. At $T = 0$ K, the conduction channel across an individual junction does not open unless the change in free energy $\Delta W_{ij} \leq 0$, wherein the drop across the junction V_{ij}, which depends on the charge state, is sufficiently large so as to overcome the junction charging energy ($E_{c,ij}$). At $T > 0$ K when there is sufficient

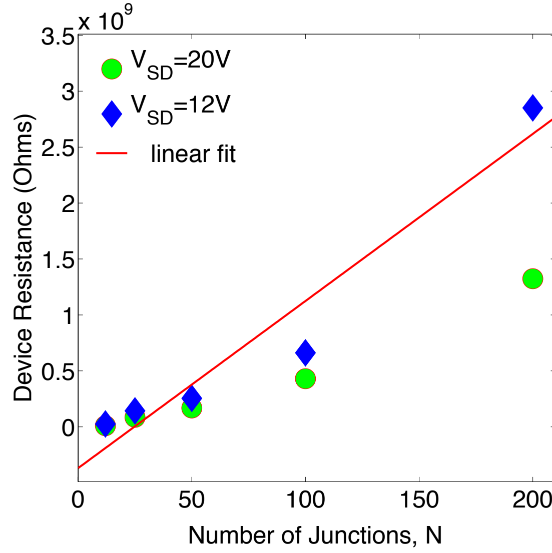


FIG. 3.5 The overall device resistance as a function of the number of junctions for two different source-drain bias values. The device resistance that is predominantly influenced by the wider junctions in the chain varies non-linearly with the chain length. With the increasing chain length, sampling more number of wider junctions and a likely increase in the value of maximum junction width have a large influence on the overall device resistance.

thermal energy in the system, the channel may open even for $\Delta W_{ij} > 0$. Tunneling across any one junction may only be a transient, however, leading to a new charge state but not necessarily a cascade of tunneling events leading to a steady state current. Such, in fact, is the case in the Coulomb blockade region for $V_{SD} < V_{th}$. Above the threshold, the pronounced staircase structures depend on the three factors: (i) the background charge state of the system in steady state, (ii) the distribution of charging potentials ($V_C \equiv E_C/e$), [see Fig. 3.6(a), which shows the distribution of charging potentials for two different chain lengths], and (iii) the distribution of tunneling resistances across the chain (Fig. 3.7), which are a reflection of the disorder in the chain. For a detailed discussion of the mechanism of the charge build-up leading to the threshold point and formation of the

staircase structure in the *IV* characteristics for low biases, see Chapter 4.

3.2 Effect of Island Radii and Junction Width on Junction Charging Potential

The charging potential (V_C), which is defined as the potential required for a single electron transition across a junction that couples two neighboring islands, depends on the capacitances in the system [see Section 2.2.1]. The capacitances, in turn, are directly influenced by distribution of island radii [Fig. 3.2(a)], junction widths [Fig. 3.2(b)], and the dielectric constant of the materials of which the tunnel junctions are made. Figure 3.6(a) shows the distribution of junction charging potentials for a 200-junction (blue/dark) and a 50-junction (yellow/light) chain device. The values range anywhere from ~40-180 mV. A closer examination of the distribution of charging potentials reveals that the island sizes play a more significant role in determining the charging potentials than do the junction widths. Consider, for example, the distribution of junction widths shown in Fig. 3.6(b). The top/green histogram in Fig. 3.6(b) shows the distribution of junction widths only for those junctions with smaller charging potentials (0 to 50% of the maximum charging potential), while the bottom/red histogram shows the distribution of junction widths only for those junctions with larger charging potentials (50 to 100% of the maximum charging potential). For clarity it is noted that the charging potentials from Fig. 3.6(a), first, were sorted according to the junction widths, and then the junction widths of the respective junctions were plotted as shown in Fig. 3.6(b). Similar process was followed for plotting the distribution of island radii that is shown in Fig. 3.6(c).

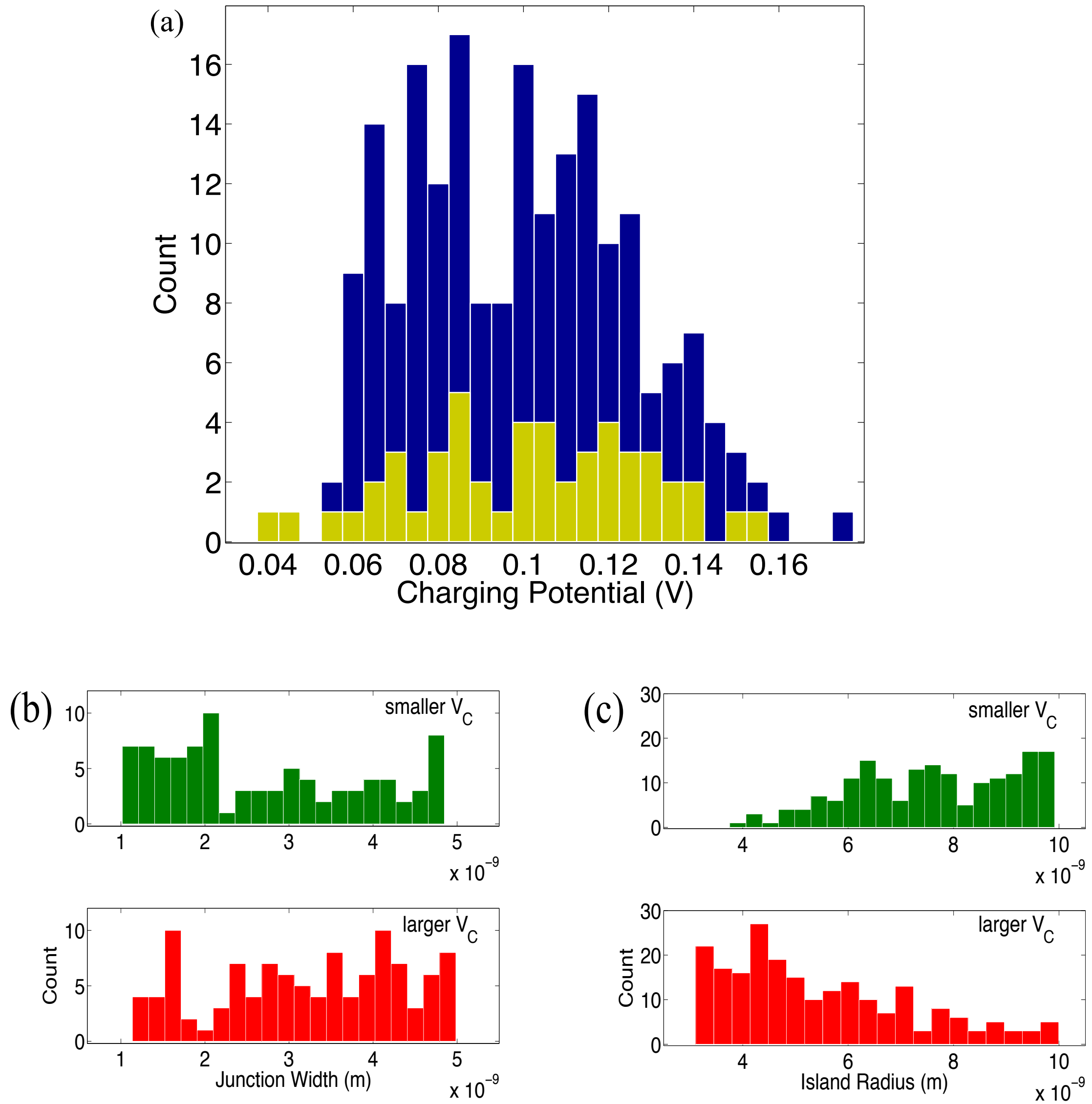


FIG. 3.6 (a) Distributions of charging potentials of the junctions for a 200-junction device (blue/dark) and a 50-junction device (yellow/light). (b) Charging potential distributions for the junction widths for the 200-junction device separating those junctions with smaller charging potentials (top/green) in part (a) from those with larger charging potentials (bottom/red). (c) Distributions of island radii for the same 200-junction device, separating islands associated with those junctions with smaller charging potentials (top/green) from those with larger charging potentials (bottom/red). Reprinted figure with permission from Savaikar, *et al.*, J. Appl. Phys. 114, 114504 (2013). Copyright 2013, AIP Publishing LLC.

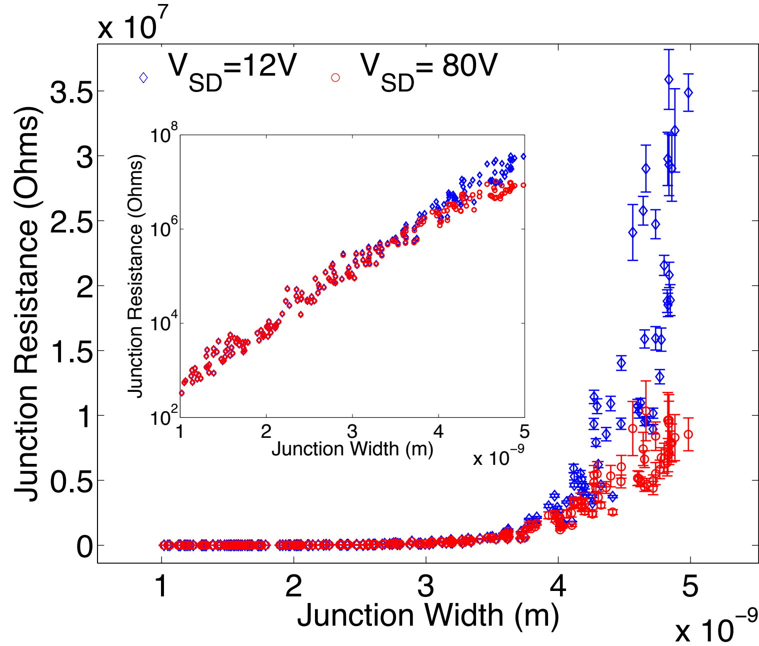


FIG. 3.7 Variation of junction resistances with junction widths in a chain of N = 200 junctions at two different source-drain biases. At the lower bias V_{SD} = 12 V (blue diamonds) a Coulomb-staircase structure is observed in the *IV* characteristics (Fig. 3.3), while at the higher bias V_{SD} = 80V (red circles) no Coulomb staircase structure is observed. Error bars about the mean values show the standard deviation in the junction resistances (over 5000 Monte Carlo steps, corresponding to approximately 1 ns at 12 V and 18 ps at 80 V) after the system has reached a steady state. The inset shows the same data on a logarithmic scale. Reprinted figure with permission from Savaikar, *et al*., J. Appl. Phys. 114, 114504 (2013). Copyright 2013, AIP Publishing LLC.

But in this case, a junction with either a larger or a smaller charging potential may couple both, a larger as well as a smaller island. To account for such a feature, double counting was done which is reflected in the counts in Fig. 3.6(c). In Fig. 3.6(b) we observe that the junctions with higher charging potentials have nearly the same range of junction widths compared with those with lower charging potentials, although there is a slight asymmetry - the distribution of junction widths for junctions with smaller charging potentials being

slightly skewed toward smaller junction widths, and vice versa. On the other hand, the charging potentials depend strongly on the island radii, as illustrated in Fig. 3.6(c). The junctions with smaller charging potentials (top/green) tend to couple the larger islands, while the junctions with larger charging potentials (bottom/red) tend to couple islands with smaller radii. The dominance of island size over junction width in affecting the charging potentials in these devices is due to the self-capacitances (0.72 ± 0.22 aF) of the islands being comparable to the junction capacitances (0.39 ± 0.15 aF).

3.3 Effect of Chain Length, Defect, Junction Width, and Temperature on Device Characteristics and the Device Threshold Voltage

3.3.1 Effect of Chain Length

When the source electrode is moved to increase the number of junctions and islands in the chain, a larger number of junctions and islands are sampled from the distributions of the parent chain. With the increase in the number of islands and junctions, the longer device requires larger source-drain bias for the junctions to be able to overcome their respective charging potentials. Two factors are primarily responsible for the increase in the required bias. First, is the potential-divider nature of the device chain. In a longer chain a given source-drain potential is divided among a larger number of junctions leading to a smaller average potential drop across each junction, as compared to a smaller chain, similar to the case of resistors in series. Second, with new junctions and islands being sampled from the distribution in a longer chain, particularly wider junctions and smaller islands, the number of junctions with larger charging potentials increases

[Fig. 3.6(a)]. With increasing chain length there is an increasing chance of also increasing the maximum charging potential in the distribution. Both of these factors contribute to the increase in the device V_{th} with the increase in chain length. Sampling more of the junctions having larger charging potential would also be expected to make more pronounced Coulomb staircase structures in larger chain devices as compared to smaller chain devices, which is indeed observed [Fig. 3.3(b)].

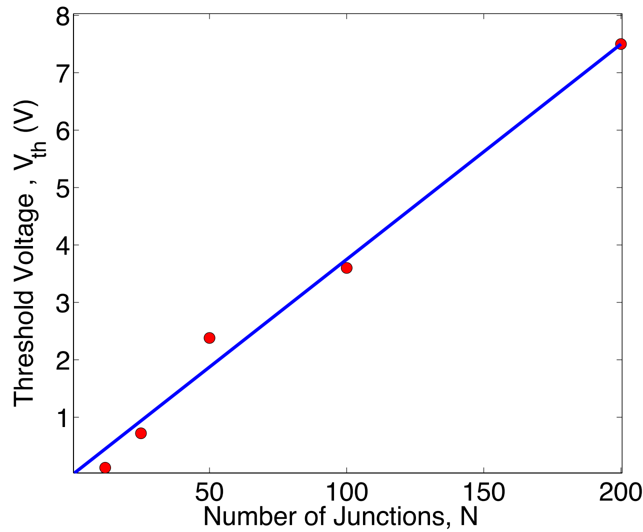


FIG. 3.8 Variation of the threshold voltage V_{th} [obtained from Fig. 3.3(b)], as a function of the number of junctions N along the chain. A linear behavior as has been observed in several experimental studies.[3,4,1,5] Reprinted figure with permission from Savaikar, *et al*., J. Appl. Phys. 114, 114504 (2013). Copyright 2013, AIP Publishing LLC.

The linear relationship shown in Fig. 3.8 between the threshold voltage (V_{th}) and the number of junctions (N) has also been observed in 2-dimensional systems[3,4] and has been the subject of several theoretical and computational studies.[6,7,8] For an array of islands with uniform capacitances but with potential levels randomly offset by quenched

background-charge disorder, Middleton and Wingreen[6] showed that the linear $V_{th}(N)$ behavior can be described by $V_{th} = \alpha N \Delta V$, where the constant α was found to depend on the dimensionality of the system and the ratio of the junction capacitance to the island self-capacitance. In the limit where the self-capacitance (or gate capacitance) is very strong compared to the inter-island capacitances, the screening length $\lambda \rightarrow 0$, and ΔV is the constant change in potential required in V_{SD} per "up-step" for the charge front to be able to advance toward the other electrode. Carrying forward the argument by Middleton and Wingreen[6] to disordered systems with strong inter-island coupling, we define, in a broader sense, an up-step as any electronic transition between two islands or an island and an electrode in the chain that requires a minimum increase in V_{SD}, without which system remains in a static charge state.

In systems with $\lambda \neq 0$, particularly those with non-uniform junction- and self-capacitances as is the case in this work, $V_{th}(N)$ may still be expected to be linear, but the slope is difficult to predict analytically based on the system capacitances and background charges,[4,6,7,8] since voltage drops vary from junction to junction and also vary with the charge state of the system. Interpreting αN as the number of up- steps[8] that must successively be overcome by increasing V_{SD} to reach the threshold, ΔV is then taken to represent the average increase in V_{SD} required per up-step. Consider, for example, a given static charge state at some particular V_{SD} at $T = 0$. In a static charge state, the change in free energy for tunneling between any two islands i and j has $\Delta W_{ij} > 0$, and tunneling is forbidden. We consider the next up-step to be the first electronic transition, say between islands i and j, to have $\Delta W_{ij} = 0$ via a sufficient increase in the applied V_{SD}. Subsequent

to this transition, there may be a cascade of transitions that take place, until once again, at the new value of $V_{SD} < V_{th}$, the system reaches a new static charge state, with a new up-step. The new static charge state may or may not advance the charge front toward the other electrode, and may or may not include a change in the net charge on the device. We note that unlike in the $\lambda = 0$ limit, for $\lambda \neq 0$, the value of ΔV needed to overcome each up-step is not necessarily equal to ΔW_{ij}, as ΔW_{ij} is itself a function of V_{SD} through the V_{ij} term in Eq. (2.4). On the other hand, the number of up-steps and their associated values are important for understanding the dependence of V_{th} with temperature.[4, 5, 8] Unfortunately, neither the number of up-steps, the associated ΔW_{ij}, nor the necessary ΔV values needed to overcome them seem to be readily predictable in advance. The exact mechanism of overcoming the up-steps and the effects of temperature on the up-steps especially in a non-uniform system with $\lambda \neq 0$ are discussed in Chapter 4.

3.3.2 Effect of Defect

In the study conducted by Lee, *et al.*[1] it was observed that although the simulated *IV* characteristics agree qualitatively well with experimental *IV* characteristics, the Coulomb blockade in the experimental device was much larger than the blockade observed in the simulated device. There could be multiple reasons behind the large blockade in the experimental device. Although the nano-islands have been taken to be spherical in shape for simulation purposes, it is highly unlikely that the real islands are exact spheres because of the nature of the fabrication process. This would greatly affect the junction capacitances and especially the self-capacitances in the device that have a large influence on the charging potentials and hence the blockade threshold. Because

of the sensitive nature of the dependence of junction current on the junction width, an accurate measurement of junction widths is crucial for a reasonable estimate of the device current. Accurate junction-width measurements will also influence the junction capacitances, which would affect the blockade and the V_{th} for a given chain length.

In the real device, the islands are not expected to be aligned along the applied field direction between the source and the drain but they would rather form a quasi-1D chain. This reduces the local field strength across a junction between the two neighboring islands thereby necessitating an increase in the applied bias for the transition to take place across such a junction. Furthermore, despite the best efforts to fabricate devices with a junction-width distribution within a certain range (1-5nm), there could be instances of defects occurring in the form of larger junction widths (~10nm). To study the effect of such defects on the device characteristics, additional simulations were conducted on a 50-junction chain (see Fig.3.9).[1] The defects were modeled by randomly removing one or two islands from the chain initially constructed using Metropolis Monte Carlo, as described in Chapter 2. The results show that the device blockade and V_{th} increase significantly in the presence of defects and with the number of defects. This feature of an increase in V_{th} with the number of defects indicates that defects might serve a useful purpose in such devices. The high-bias *IV* characteristics show that defects have no appreciable influence on the overall device resistance but they shift the current curves towards higher bias depending on the amount of increase in the blockade. The extent of the influence of an individual defect on the blockade and the device V_{th} is expected to depend on the position of the defect along the chain. If a defect arising out of the removal of an island is located closer to the biased electrode, especially in a shorter chain, it

may have more pronounced effect thereby increasing the blockade and the device V_{th}, than if it was located away from the biased electrode. The position of defect may become less significant in longer chains.

3.3.3 Effect of Junction Width

When the applied bias V_{SD} reaches V_{th} the device starts conducting. Due to the distribution of junction widths [Fig. 3.2(b)], a considerable distribution in the tunneling resistances is observed across the length of the device (Fig. 3.7). As already discussed,

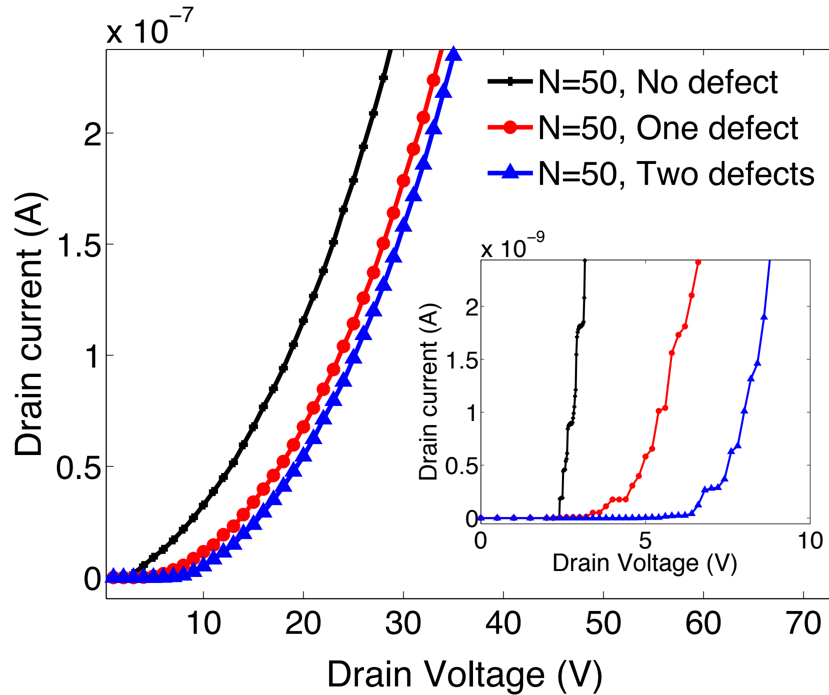


FIG. 3.9 *IV* characteristics for a 50-junction chain with zero, one and two defects (junction widths are ~8-10nm) at $T = 0$ K. The Coulomb blockade and V_{th} for a given chain length increase significantly in the presence of defects, and with an increase in the number of defects. Reprinted figure with permission from Lee, *et al*., Adv. Mater. 25, 4544 (2013). Copyright © 2013 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

the tunneling resistances at any given time depend on several factors, especially the junction widths and the charge state for a given V_{SD}. The junction widths play a dominant role in determining the tunneling resistances because of the exponential dependence of tunneling probability on junction width. The wider junctions with their large tunneling resistances and low tunneling rates limit the current flowing through the device. As a result, the wider junctions with the largest resistances generally have a dominant effect on the scale of the device current, especially at lower biases (Fig. 3.7). However, which junctions are dominant can change as the chain length increases due to the wider

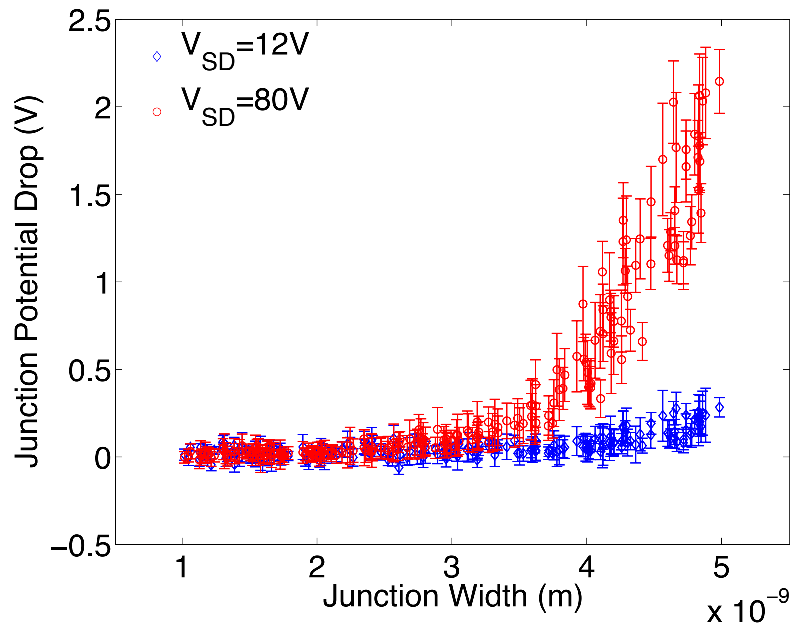


FIG. 3.10 Variation of junction potential drops with junction widths in a chain of $N = 200$ junctions at two different source-drain biases [V_{SD} = 12 V (blue diamonds); V_{SD} = 80 V (red circles)]. Error bars about the mean values show the standard deviation in the junction potential drops (over 5000 Monte Carlo steps, corresponding to approximately 1 ns at 12 V and 18 ps at 80 V) after the system has reached a steady state. Reprinted figure with permission from Savaikar, *et al.*, J. Appl. Phys. 114, 114504 (2013). Copyright 2013, AIP Publishing LLC.

sampling of junction widths from the parent chain's distribution contained in the device. As a result there is a non-linear dependence of the overall resistance of the device as a function of chain length, as can be inferred from the slopes of the *IV* curves in Fig. 3.3, and as observed in Fig. 3.5 for two particular values of $V_{SD} > V_{th}$.

Figure 3.10 shows time-averaged values of the voltage drops in a 200-junction system at two different source-drain biases during steady-state current flow. At a lower bias, $V_{SD} = 12$ V, there is a Coulomb-staircase structure in the *IV* characteristics [Fig. 3.3(b)], while at a higher bias, $V_{SD} = 80$ V, no Coulomb staircase is observed [Fig. 3.3(a)]. At smaller V_{SD} the distributions in junction widths have negligible effects in determining the potential drops across the junctions (Fig. 3.10). However, at large V_{SD}, the wider junctions show larger potential drops across them, as compared to the narrower junctions, and furthermore, show greater increases in the potential drops with increased V_{SD} (Fig. 3.10). Band bending effects are therefore not uniform across all junctions, but are greater across the wider ones, which otherwise act as the major roadblocks (with higher tunneling resistances) for current flow, especially at lower biases. Hence, at higher V_{SD} there is larger barrier suppression that partly compensates for their large junction widths. This leads to a decrease in the tunneling resistances of the wider junctions with increasing bias, but without any significant change taking place across the narrower junctions (Fig. 3.7). The large potential drops ($V_{ij} >> V_C$) also lead to diminishing of the charging effects and hence to larger changes in the free energy [Eq. (2.4)] after the electron transitions across the wider junctions. Both these factors lead to a considerable increase in their electron tunneling rates at large V_{SD}. With increasing V_{SD}, more conduction channels open up that increase the chances of electron conduction across

the device length. We believe that these multiple effects of increased number of conduction channels and large increase in tunneling rates across the wider junctions are responsible for diminishing of the discrete Coulomb staircase steps at large V_{SD}.

3.3.4 Effect of Temperature

The *IV* characteristics at T = 100 K for a 50-junction and a 100-junction device [Fig. 3.3(b)] show that V_{th} and the blockade width depend sensitively on temperature (T). With increasing temperature, blockade effects are diminished as the sharp increase in current at V_{th} is smoothed out and V_{th} decreases. For low source-drain bias values, high temperature *IV* curves still show a Coulomb staircase structure, but at much lower bias values, and within the zero-temperature blockade region. On the other hand, temperature has no appreciable effect on the device current at large source-drain bias, which is indicative of quantum tunneling. The sensitivity of V_{th} and the Coulomb staircase structure on temperature may seem surprising since eV_{th} is on the order of electron Volts, while k_BT is less than 25 meV up to room temperature. The relevant energy scale is not eV_{th}, but rather, it is the separation between the single-electron charging levels on the islands which are thermally broadened with increase in T as explained later in Section 4.4 in Chapter 4. The thermal broadening of the single-electron charging levels has a direct impact on the local up-steps that ultimately lead to decrease in the Coulomb blockade and the V_{th}. The dependence of V_{th} on temperature has been studied in some detail by Parthasarathy, *et al.*[4] and Elteto, *et al.*[8] for the case of charge transport in systems consisting of metal nanocrystal arrays, and are further discussed in Chapter 4.

3.4 Power Law Scaling Behavior: Effect of Chain Length and Disorder on the Exponent

Studies done on 1D and 2D Coulomb blockade devices have shown that beyond the threshold bias, the *IV* behavior follows a scaling law $I \propto \left(\frac{V - V_{th}}{V_{th}}\right)^{\zeta}$; however, what values the exponent ζ might be expected to take remains an open question. For infinite arrays in the limit of short screening length, Middleton and Wingreen[6] argue analytically that $\zeta = 1$ and 5/3 for 1D and 2D systems respectively, while their computer simulations for finite systems correspondingly give $\zeta = 1$ and 2.0 ± 0.2. Experimental studies done on 1D and 2D arrays of Al islands linked by $Al/Al_xO_y/Al$ tunnel junctions show $\zeta = 1.36 \pm 0.1$ for 1D, and $\zeta = 1.8 \pm 0.16$ for 2D.[9] The investigation of a ~1.2 μm chain of graphitized carbon nanoparticles self-assembled between two Cr microelectrodes gives different values of ζ for different samples of the same length, with values ranging between 1.0 and 2.35.[10] The review by Deshpande, *et al.*[11] and the Coulomb-blockade transport studies on experimental quasi-one-dimensional polymer nanofibres by Aleshin, *et al.*[12] go a step further showing that for a given sample at a given temperature there is a transition in the *IV* behavior, wherein the exponent changes as the applied bias is sufficiently increased. In the study by Aleshin, *et al.*[12] the exponent changes from $\zeta \sim 1.3$ at low biases to $\zeta \sim 2.1$ at higher biases. They argue that the change in ζ with the applied bias can be attributed to the crossover from quasi-1D to 2D transport.

Simulated *IV* characteristics of disordered 1D devices with different chain lengths at source-drain biases beyond the threshold are shown in Fig. 3.11(a). At moderate bias

values when the staircase structure begins to disappear, the exponent ζ ranges between 1 and 2 for different chain lengths, with $\zeta \sim 1$ for larger N, and increasing in value as N decreases. Furthermore, for a given value of N, ζ crosses over from the lower value to a higher value under sufficiently large applied biases, as has been observed in the experimental study of quasi-1D systems.[12] As discussed earlier, the non-Ohmic nature of

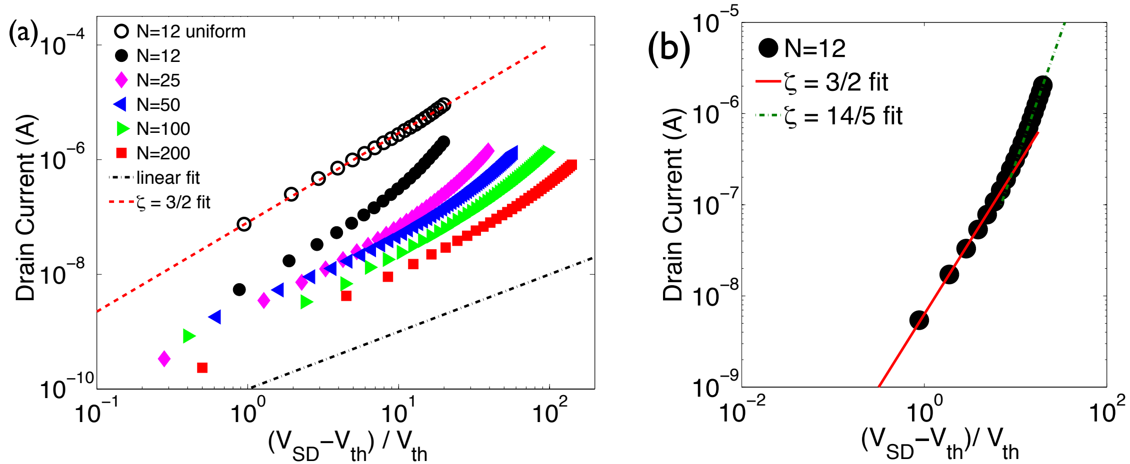


FIG. 3.11 (a) *IV* characteristics of disordered 1D chains (solid symbols) of different lengths ranging from 12 to 200 junctions over a wide applied bias range. At moderate biases beyond the threshold voltage, the *IV* behavior in larger-chain-length devices show $\zeta \sim 1$, and increases towards $\zeta \sim 2$ for shorter lengths. For a given chain length, ζ increases with the increase in the applied bias across the chain. The change is more prominent for shorter lengths. The characteristic for a uniform 12-junction chain (open circles) is also shown for comparison. The junction width (3.46 nm) and the island radius (6.92 nm) of this uniform system are the respective mean values of random junction widths and random island radii in the disordered 12-junction system (black solid circles). Reprinted figure with permission from Savaikar, *et al.*, J. Appl. Phys. 114, 114504 (2013). Copyright 2013, AIP Publishing LLC. (b) *IV* characteristics for a disordered 12-junction chain showing the change in ζ from ~ 3/2 at lower bias to ~2.8 at higher bias. Straight lines are fits to the data.

the *IV* behavior stems from the dependence of the tunneling-barrier height on the voltage drop across the respective junction, and the barrier suppression effects are observed predominantly across the wider junctions in the system, which experience larger voltage drops.

For comparison with the disordered systems, also shown in Fig. 3.11(a) is the *IV* characteristic of a uniform 12-junction system, whose island radius and junction spacing were chosen to be the respective mean values of the disordered 12-junction system. The *IV* characteristic for the uniform system follows a power law where the exponent remains fairly constant at $\zeta \sim 3/2$ over a wide bias range as compared to a system with a random distribution of island spacings where the exponent changes appreciably from $\zeta \sim 3/2$ at lower biases to $\zeta \sim 2.8$ at higher biases [Fig. 3.11(b)]. The simulations clearly demonstrate that the scaling exponent is influenced by the system disorder and the chain length.[7] We caution, however, that while MITS captures some of the generic behaviors that may be expected for the exponent in 1D and presumably in 2D systems, the exact exponents are likely dependent on the exact nature of the dependence of tunneling barrier on voltage drop, for which we have thus far only incorporated a simple model.

The scaling exponent of $\zeta \sim 3/2$ that we have observed in 1D systems may resolve the discrepancy between the value $\zeta \sim 2.25$ experimentally observed by Parthasarathy, *et al*.[3, 4] in 2D devices, and the smaller value of 5/3 theoretically predicted by Middleton and Wingreen.[6] In a 2D system, where there could be multiple current channels, Middleton and Wingreen[6] argued that the 2D scaling exponent is $\zeta = z^{-1} + \zeta_{1D}$, where $z = 3/2$ is the roughness exponent for the KPZ[13] model of interface growth in disordered media, and

ζ_{1D} is the *IV* scaling exponent in a single channel. Instead of assuming an Ohmic behavior ($\zeta_{1D} = 1$) for a single channel, as did Middleton and Wingreen[6] giving $\zeta = 2/3 + 1 = 5/3$, using larger exponent of $\zeta_{1D} \sim 3/2$ from our simulations gives $\zeta = (3/2)^{-1} + 3/2 \approx 2.2$ for 2D devices, which agrees well with experiment.[3, 4]

References

[1]C. H. Lee, S. Qin, M. A. Savaikar, J. Wang, B. Hao, D. Zhang, D. Banyai, J. A. Jaszczak, K. W. Clark, J.-C. Idrobo, A.-P. Li, and Y. K. Yap, Adv. Mater. 25, 4544 (2013).

[2]A. S. Cordan, A. Goltzene, Y. Herve, M. Mejias, C. Vieu, and H. Launois, J. Appl. Phys. 84, 3756 (1998).

[3]R. Parthasarathy, X.-M. Lin, and H. Jaeger, Phys. Rev. Lett. 87, 186807 (2001).

[4]R. Parthasarathy, X.-M. Lin, K. Elteto, T. F. Rosenbaum, and H. M. Jaeger, Phys. Rev. Lett. 92, 076801 (2004).

[5]K. Xu, L. Qin, and J. R. Heath, Nat. Nanotechnol. Lett. 4, 368 (2009).

[6]A. A. Middleton and N. S. Wingreen, Phys. Rev. Lett. 71, 3198 (1993).

[7]A. Middleton and S. Jha, Physics Paper 184 (2005), arXiv:cond-mat/ 0511094v1 [cond-mat.dis-nn], see http://surface.syr.edu/phy/184.

[8]K. Elteto, E. G. Antonyan, T. T. Nguyen, and H. M. Jaeger, Phys. Rev. B 71, 064206 (2005).

[9]A. J. Rimberg, T. R. Ho, and J. Clarke, Phys. Rev. Lett. 74, 4714 (1995).

[10]A. Bezryadin, R. M. Westervelt, and M. Tinkham, Appl. Phys. Lett. 74, 2699 (1999).

[11]V. V. Deshpande, M. Bockrath, L. I. Glazman, and A. Yacoby, Nature 464, 209 (2010).

[12]A. N. Aleshin, H. J. Lee, S. H. Jhang, H. S. Kim, K. Akagi, and Y. W. Park, Phys. Rev. B 72, 153202 (2005).

[13]M. Kardar, G. Parisi, and Y. C. Zhang, Phys Rev Lett 56, 889 (1986).

Chapter 4: Physics of Coulomb Blockade and Coulomb Staircase in Multi-island Systems[1]

Two particularly interesting and important features of single-electron devices (SEDs) are the Coulomb blockade (CB) and the Coulomb staircase (CS). As explained earlier, these features are the manifestations of charging effects of the nano-islands due to their small size. These two device features can be used in many practical applications such as switching, information processing, and sensing. However, to successfully design and fabricate a device that can exhibit these features, it is imperative to understand the physics behind the charge transport in such devises. Many research groups[1-4,5,6,7] have fabricated SEDs, some of which demonstrate the Coulomb blockade and the Coulomb staircase features even at room temperature.[3] Attempts have been made to qualitatively explain the physics behind the origin of these interesting characteristics and the operation of devices exhibiting these characteristics;[2, 4,8, 9,10,11,12] however, no definitive work has been done to demonstrate the mechanisms that give rise to CB and CS, and the factors that control these device properties especially in multi-island devices. In this chapter, we first explain in detail the physics behind the CB and the CS, and the effect of gate modulation and temperature on the device properties in a single-island device. Then we explore the physics of CB and CS characteristics in a multi-island one-dimensional (1D) chain and their modifications by the temperature.

[1]Much of the work in Chapter 4 is planned for submission for publication in the near future.

4.1 Single-island Device and the Physics Behind the Staircase Structure at $T = 0$ K

4.1.1 Asymmetric Device and a Positive Drain (D1)

We first consider a single-island device such as the one studied by Amman, *et al.*[10] using a master-equation approach, and simulation results at $T = 0$ K computed using MITS. A detailed understanding of the conduction mechanisms for a single-island device gives valuable insight into the more complicated mechanisms of conduction in multi-island devices. The device consists of a single island (*m*) having a continuous energy spectrum. The island is separated from the two electrodes (*D* and *S*) by two tunneling junctions *J2* and *J1* respectively. *J1* has tunneling resistance R_1 = 100 MΩ and capacitance C_1 = 100 aF while *J2* has tunneling resistance R_2 = 1 MΩ and capacitance C_2 = 1 aF as shown in Fig. 4.1. The device is biased by a source-drain voltage V_{SD} (the source is grounded) giving rise to the potential drops V_1 and V_2 across *J1* and *J2* respectively. The device is a strongly asymmetric device with $R_1 >> R_2$ and $C_1 >> C_2$. Depending on the two capacitances, the two junctions have characteristic charging energy E_c.[10] The junction charging potential is defined as $V_c = E_c / e$, and is given by

$$V_c = \frac{e}{2(C_1 + C_2)} = 0.792 \times 10^{-3} V \quad (4.1)$$

The respective potential drops V_1 and V_2 across *J1* and *J2* are given by[10, 12]

$$V_1 = \frac{C_2 V_{SD}}{C_1 + C_2} - \frac{ne}{C_1 + C_2} \quad (4.2)$$

$$V_2 = \frac{C_1 V_{SD}}{C_1 + C_2} + \frac{ne}{C_1 + C_2} \quad (4.3)$$

where n is the extra number of electrons on the island at any given point of time.

With the potential drops V_1 and V_2 known, the respective tunneling rates Γ_1 and Γ_2 across $J1$ and $J2$ are given by[10, 12]

$$\Gamma_1 = \frac{V_1 - V_c}{eR_1} \quad \text{and} \quad \Gamma_2 = \frac{V_2 - V_c}{eR_2} \tag{4.4}$$

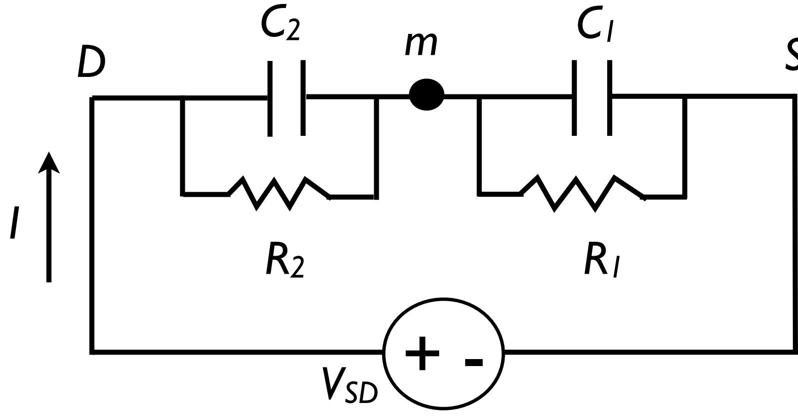


FIG. 4.1 Schematic of a single-island device modeled by Amman, *et al.*[10] using the master-equation approach. The two junctions $J1$ and $J2$ having capacitances C_1=100 aF and C_2 = 1 aF and resistances R_1 = 100 MΩ and R_2 = 1 MΩ respectively are driven by a voltage source V_{SD}. The device characteristics are largely influenced by the device asymmetry.

The device IV characteristics are shown in Fig. 4.2 (blue with + marker). For any charge transfer to take place across any of the junctions at T = 0 K, the total change in the free energy of the system after the transition must be less than or equal to zero: $\Delta W_{ij} \leq 0$ As V_{SD} is increased at T = 0 K, a large fraction of the potential bias drops across $J2$ for a given V_{SD} due to the large asymmetry in the capacitances (C_1>>C_2) [Fig. 4.3(a)]. When $V_{SD} \cong 0.8 \times 10^{-3}$ V [$eV_{SD} \geq E_1$ in Fig. 4.3(b)], the potential drop across the junction $J2$

exceeds V_c, and *J2* gets excited first - that is, an electron makes the first transition from the island *m* to the drain *D* with a transition rate of $\Gamma_2 \cong 206 \times 10^6 s^{-1}$, thereby creating a vacancy on the island and opening the first conduction channel at E_0. Thus the island has one net positive charge (+*e*), the potential on the island rises, and the potential energy drops by ~2 eV_c from E_0 to ~E_2 [Fig. 4.3(b)]. With the increase in the island potential, the potential drop across *J2* becomes negative and the conditions are no longer favorable for electron transition across *J2*. However, the drop across *J1* increases to ~2 V_c favoring the

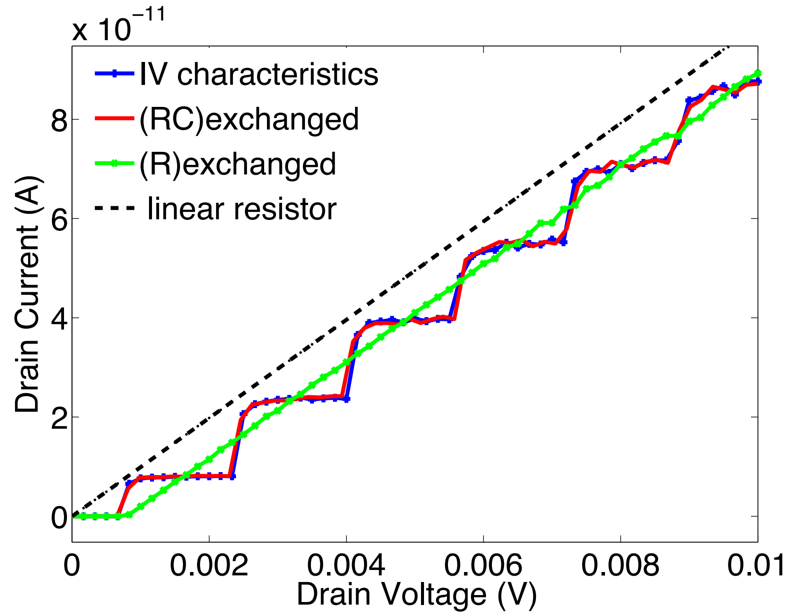


FIG. 4.2 *IV* characteristics of the device D1 shown in Fig. 4.1 and simulated using MITS. The characteristics (blue with + marker) show a clear staircase structure that is the manifestation of a strong asymmetry in the device. Upon interchanging the junctions *J1* and *J2* (device D2), no appreciable difference is observed in the *IV* behavior (red solid line with no marker). Upon interchanging only the tunneling resistances of the junctions (device D3), the staircase structure disappears but the blockade is still retained (green with × marker). Device D3, after it has overcome the blockade, behaves like a linear resistor (shown in black dashed line) with the current increasing linearly with V_{SD}.

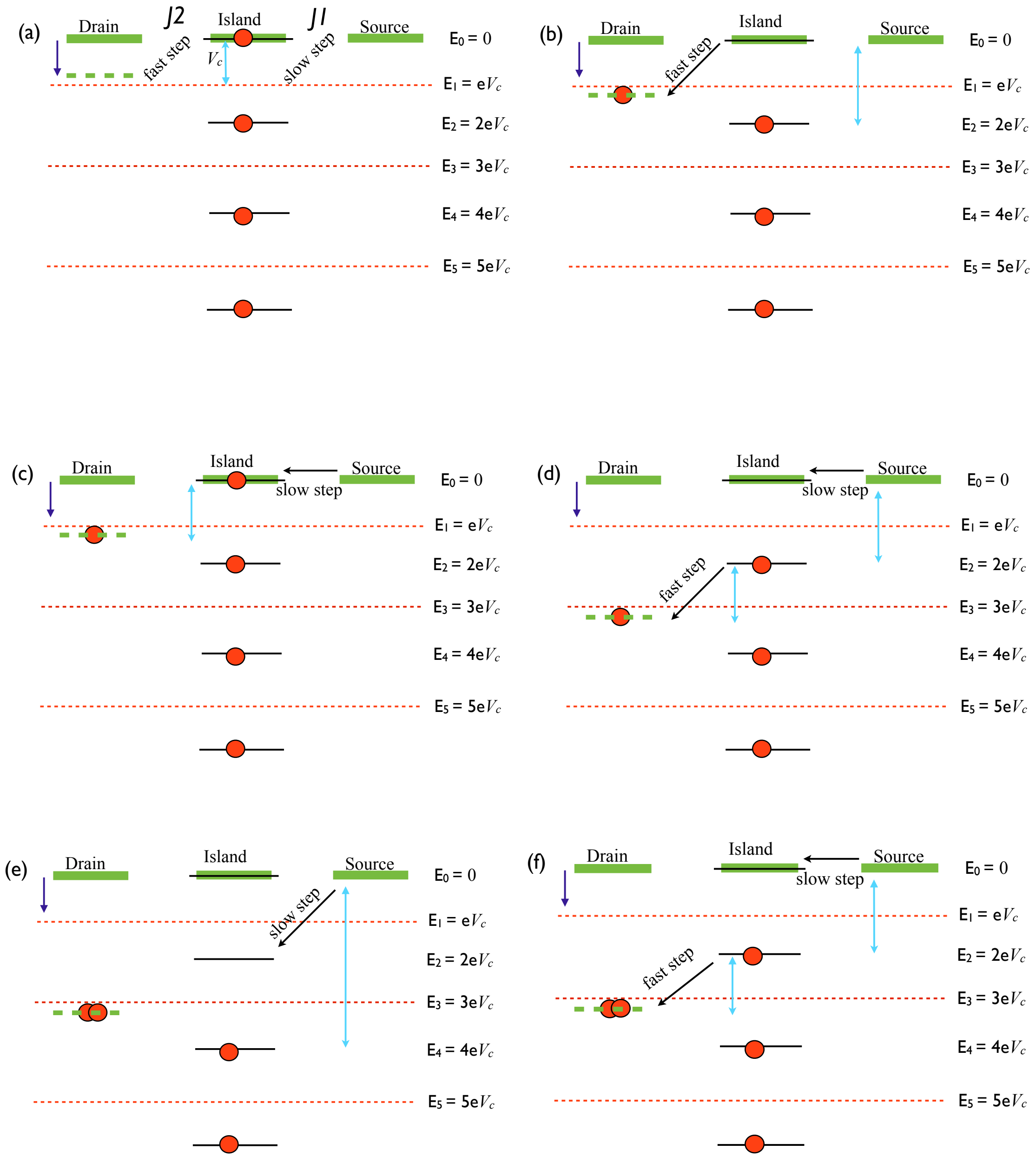


FIG. 4.3 Energy level diagrams of the system wherein the system capacitances determine the charging energy levels (shown on the right) and the potential drops across the junctions. The junction resistances predominantly determine the tunneling rates. The complex interplay among different system variables such as capacitances, resistances, V_{SD}, and the island charge state determine the terminal device characteristics shown in Fig. 4.2.

electron transfer across *J1* from the source *S* to level E_0 on the island *m*, thereby discharging the island [Fig. 4.3(c)]. Although it is energetically favorable, because of the large resistance R_1=100 MΩ across *J1*, the electron transfer across *J1* at this step takes place at a much lower rate of $\Gamma_1 \cong 50.0\times10^6 s^{-1}$ making this transition a rate-limiting step (RLS) that predominantly determines the overall device current. In the overall process of charge transfer from source to drain, junction *J1* is a rate-limiting junction (RLJ). As a result, net one electron flows across the device from the source to the drain thereby turning the device on and giving a threshold voltage $V_{th} = V_{SD} \cong 0.8\times10^{-3}$ that is slightly greater than V_c. The net current flowing through the device when it turns on is $I = 6.6 \text{ pA} \cong e\Gamma_1 = 8.0 \text{ pA}$.

As the bias V_{SD} is increased further from V_{th}, no qualitative change takes place in the device behavior until eV_{SD} approaches E_3 [Fig. 4.3(d)]. For $eV_{SD} < E_3$, the charge flow across the device continues through the channel E_0 on the island with the device current remaining practically constant over a bias range $E_1 \le eV_{SD} < E_3$. This is the bias range where the first step of the staircase is observed in the *IV* characteristics in Fig. 4.2 (blue with + marker). As the bias increases from E_1 to E_3, there is small slope observed in the *IV* characteristics because the RLS rate increases by a small amount due to the increase in the potential drop across RLJ *J1*, but the step appears practically flat on the scale of the figure. When eV_{SD} becomes larger than E_3 [Fig. 4.3(d)] the system still waits for the slow step to occur of the electron tunneling from source to E_0 on the island across *J1*. However with $eV_{SD} > E_3$ it is now favorable for the electron to tunnel from E_2 on the island to the drain across *J2*. If the electron from E_2 on the island tunnels to the drain, one more

vacancy is created giving a net charge of +2*e* on the island [Fig. 4.3(e)]. The transfer of E_2-level electron on the island opens the second conduction channel for the electron flow across the device. With the transfer of an E_2-level electron on the island to the drain, the potential on the island rises to ~$4V_c$ and the drop across *J2* becomes negative, thereby making it unfavorable for any more transition across *J2*. With the increase in the island potential, the drop across *J1* increases to ~$4V_c$ and an electron tunnels across *J1* from the source to the island filling up E_2 and reducing its net charge back to +*e* [Fig. 4.3(e)]. This transition, which is a RLS transition for the channel, takes place with a rate of $\Gamma_1 \cong 150 \times 10^6 s^{-1}$ that is $\sim \frac{4Vc - Vc}{2Vc - Vc} = 3$ times the original RLS rate of $\sim 50.0 \times 10^6 s^{-1}$ when the device current was at its first step in the *IV*. Hence the net device current increases sharply by a factor of ~3 giving the second step of the staircase in the *IV* characteristics. Once the RLS transition has taken place across *J1*, two events are possible [Fig. 4.3(f)]; either the more likely transition may transfer the E_2-electron from the island to the drain, or in a rarer event, one more electron may tunnel from the source to the island thereby discharging the island. But it is observed that a rare event is likely to be followed by two successive transitions from the island to the drain charging the island back, as expected, to its net charge of +2e before the next RLS transition can take place across the RLJ *J1*. As a result, a steady current would continue to flow from the source to the drain at the second staircase step in the *IV* characteristics with the island charge typically oscillating between +*e* and +2*e*. As in the case of first staircase step in the *IV*, the current practically remains constant during the second step as well, increasing by only a small amount until the bias $eV_{SD} \geq E_5$ when the third step appears in the staircase.

Therefore in a single-island system, the width of the staircase step is $2V_c$ with the first step appearing at $V_{SD} \approx V_c$ in the *IV* characteristics (Fig. 4.2). In a highly asymmetric system, it is fairly straightforward to analytically estimate the width and the height of the step from the known value of V_c.

If the drain in D1 is negatively biased instead, similar *IV* characteristics are obtained with a negative current flowing through the device so that the device characteristics are symmetric about $V_{SD} = 0$ V. But whenever the island is charged, it carries a net negative charge as against the positive charge observed in the previous case when the drain is positively biased.

4.1.2 Device after Exchanging the Junctions (D2)

If the two junctions are exchanged (device D2) and the drain is kept at a positive bias, the device exhibits *IV* characteristics (red with no marker) similar to those exhibited by D1 discussed in Section 4.1.1 as can be seen in Fig. 4.2. The width and the height of staircase steps remain the same and the steps are positioned at the same points on the voltage-bias scale. But this symmetrical behavior requires that the self-capacitance of the island and the gate capacitance, both of which have been assumed to be zero in this case, to be negligible compared to the inter-island capacitances. It is observed that *J2*, which is nearer the source in this case, excites first and an electron tunnels from the source to the island, thereby depositing a net negative charge on the island. Therefore the potential on the island falls and the voltage drop across *J1*, which is towards the drain, increases making it favorable for conduction. The extra electron on the island tunnels through *J1* to the drain in a rate-limiting step, and net one electron flows across the device from

source to the drain switching the device on. As V_{SD} is increased further, a similar process takes place as described in Section 4.1.1, giving rise to a staircase structure in the device characteristics. Although the mechanism remains the same as observed in D1, the net charge on the island, whenever it is charged, is observed to be a negative charge. If either the self-capacitance of the island or the gate capacitance were to be large, the device characteristics upon exchanging the junctions (D2) would change substantially. The resulting device would behave differently with a different V_{th} and a different staircase structure, as if it were a different device altogether.

4.1.3 Device after Exchanging the Resistances (D3)

Simulations were also carried out after exchanging the tunneling resistances of the two junctions ($R_1 = 1\ \mathrm{M\Omega}$ and $R_2 = 100\ \mathrm{M\Omega}$) in the device D1 discussed in Section 4.1.1, while keeping the capacitances unchanged. The *IV* characteristics obtained are shown in Fig. 4.2 (green with × marker). The characteristics show that the device has the same blockade and V_{th} characteristics as in the previous two cases (D1 and D2). However, the switch-on current (I_{on}) is smaller by more than an order of magnitude. Furthermore, the device does not exhibit any current staircase structure once it starts conducting. But the device current increases linearly with V_{SD} after overcoming the blockade, mimicking the behavior of a linear resistor (black dashed line). The data from this investigation show that as V_{SD} is increased from 0 to V_{th}, the potential drops developed across *J1* and *J2* are similar to those observed in D1 discussed in Section 4.1.1. The drop across *J2* is much larger than the drop across *J1* and the junction *J2* excites first. When $eV_2 \geq E_1$, *J2* allows

an electron to tunnel from the island to the drain thereby creating a hole on the island. But since *J2* has a larger resistance $(100\ \text{M}\Omega)$ in this case, the tunneling rate is smaller by a factor of 100 $\left(\Gamma_2 \cong 2.06\times10^6\ s^{-1}\right)$ than the rate across *J2* in device D1. With the creation of a hole on the island, the potential on the island rises thereby increasing the drop across *J1* making it favorable for electron transition. An electron tunnels from the source to the island with a transition rate that is 100 times larger $\left(\Gamma_1 \cong 5.002\times10^9\ s^{-1}\right)$ than the transition rate across *J1* in device D1. Since $\Gamma_2 << \Gamma_1$, the transition across *J2* is a RLS with *J2* acting as a RLJ that predominantly determines the overall device current. Therefore the switch-on current $I_{on} = 3.25\times10^{-13}\,\text{A} \approx e\Gamma_2$ in this case is much lower than the $I_{on} = 6.57\times10^{-12}$ A that is observed in device D1.

Once device D3 enters the conducting state after having the channel E_0 open for conduction, any further increase in V_{SD} increases the device current linearly. As V_{SD} is increased further from V_{th}, a large fraction of the increase in V_{SD} drops across the rate-limiting junction *J2*. Hence the limiting rate increases linearly with the increasing bias thereby increasing the device current linearly. When V_{SD} has been raised high enough such that $eV_2 \geq E_3$, the energetic conditions are favorable for the opening of the second channel at E_2. This is the bias value at which the second step appears in the *IV* characteristics in the device D1. But in this case, as the system waits for the slow-step transition to occur in which the electron from the new channel through E_2 can tunnel across *J2* to the drain D, the vacant level E_0 on the island is filled by the fast-step transition across *J1* wherein the electron tunnels from the source *S* to the island. Therefore, at $eV_2 \geq E_3$ the electron from the E_0 level (first channel) on the island,

instead of E_2 (second channel), makes a transition to the drain. The system (almost) never gets an opportunity for the opening of the second channel although it is energetically allowed. This process of current flow only via E_0 continues as V_{SD} is increased further and the device current increases linearly since the RLS transition rate across RLJ *J2* increases linearly. The device effectively behaves as a single junction device with a total resistance of $R1 + R2 \cong R2$ after it has overcome the Coulomb blockade as can be seen from black dashed line in Fig. 4.2.

4.2 Gate Effects in a Single-island Transistor Device at $T = 0$ K

After gaining an understanding of the detailed mechanism of charge transport in a single-island device, we next investigated the charge transport in a single-island transistor device under the influence of gate electrode. The device fabricated by Ray, *et al*.[3], which was discussed in sub-Section 2.2.2 as a test case for the validation of MITS, was investigated at T =0 K for studying transistor behavior. As already explained in Section 2.2.2, the device consists of gold nanoparticles that are positioned on the exposed sidewall of the dielectric film of silicon oxide that separates the source and drain electrodes forming a vertically self-aligned structure. The current flow takes place between the source and drain through a single nanoparticle sitting on the exposed sidewall, effectively forming a single-island device as shown in Fig. 4.1. The silicon oxide sidewall is surrounded by the gate electrode, forming a side gate structure.[3] The device parameters used for the simulation from Ray, *et al*.[3] are junction capacitances $C_1 = 3.4$ aF, $C_2 = 0.24$ aF, gate capacitance $C_G = 0.78$ aF and fixed tunneling

resistances $R_1 = 0.79\ \text{G}\Omega$, $R_2 = 0.19\ \text{G}\Omega$. To exclusively examine the effect of C_G, the self-capacitance of the island has been taken to be zero. Non-zero value of the self-capacitance is expected to shorten the blockade without appreciably affecting the qualitative behavior of the device in the three different modes of its operation that are discussed below. In the presence of gate capacitance C_G and gate voltage V_G, if n is the extra number of electrons on the island,

$$V_c = \frac{e}{2(C_1 + C_2 + C_G)} = 18.1 \times 10^{-3}\ \text{V} \tag{4.5}$$

$$V_2 = \frac{(C_1 + C_G)V_{SD}}{C_1 + C_2 + C_G} + \frac{ne}{C_1 + C_2 + C_G} - \frac{C_G V_G}{C_1 + C_2 + C_G} \tag{4.6}$$

$$V_1 = \frac{C_2 V_{SD}}{C_1 + C_2 + C_G} - \frac{ne}{C_1 + C_2 + C_G} + \frac{C_G V_G}{C_1 + C_2 + C_G} \tag{4.7}$$

$$\frac{e}{C_G} = 0.205\text{V} \quad \text{and} \quad \frac{e}{2C_G} = 0.103\text{V} \tag{4.8}$$

The device *IV* characteristics and the energy level diagrams are shown in Fig. 4.4 and Fig. 4.5 respectively. As explained earlier in Chapter 2, the charge transitions are governed by the change in the free energy ΔW_{ij} of the system as the electron makes a transition across a junction. Besides the numerous other factors such as charge state, potential drop, junction charging energy and junction tunneling resistance, ΔW_{ij} also depends on the background charge and the change in the electrochemical potential of the islands caused by the gate electrode. The background charge in the present simulation has been taken to be zero. Depending on its polarity, the background charge is expected to shift the threshold voltage without qualitatively affecting the device behavior. As shown

in Fig. 4.4, the gate electrode modulates the Coulomb blockade and the device current. Because of the compensation by mobile electrons that tunnel through the junctions, it is sufficient to consider the gate bias range whose effects are equivalent to the effects produced by the fractional induced background charge within the range [-e/2, e/2] or [0, e] on the island. Therefore, with the gate capacitance of $C_G = 0.78\,\text{aF}$, it suffices to consider the gate bias V_G within the range [0 V, 0.205 V] to understand the effect of gate modulation. When $V_G = 0\text{ V}$, the Coulomb blockade is overcome at $V_{SD} = 19.1\,\text{mV}$ and the device starts conducting. It is observed from the data that as V_{SD} is increased from 0 to

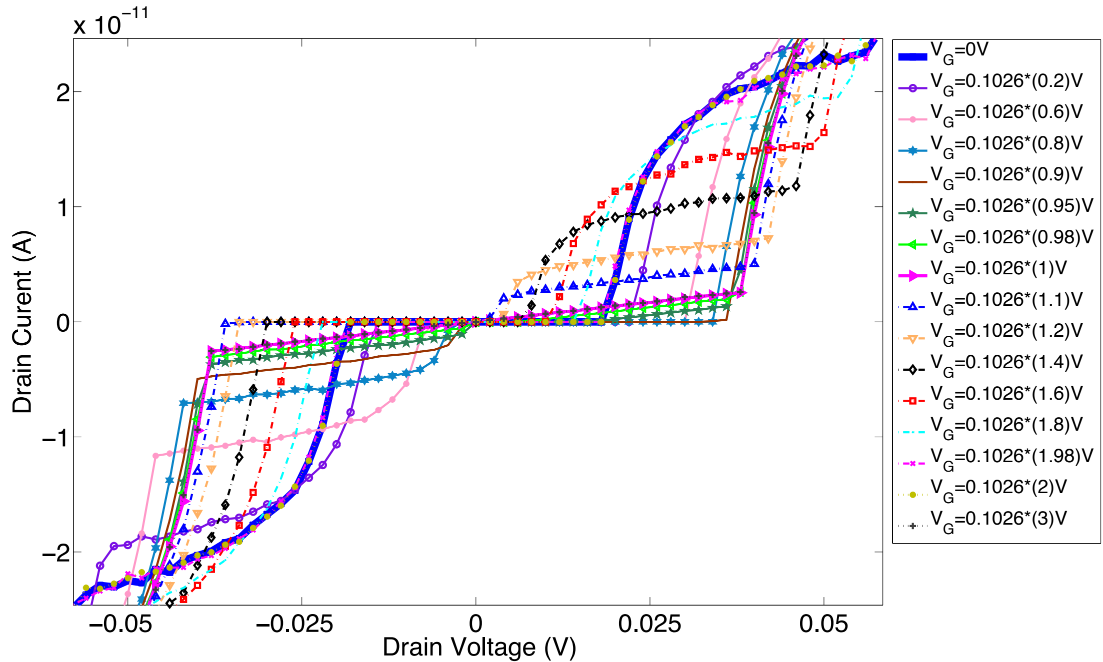


FIG. 4.4 MITS simulated *IV* characteristics of the device fabricated by Ray, *et al.*[3] The characteristics show the effect of gate modulation on the Coulomb blockade, the V_{th}, and the device current.

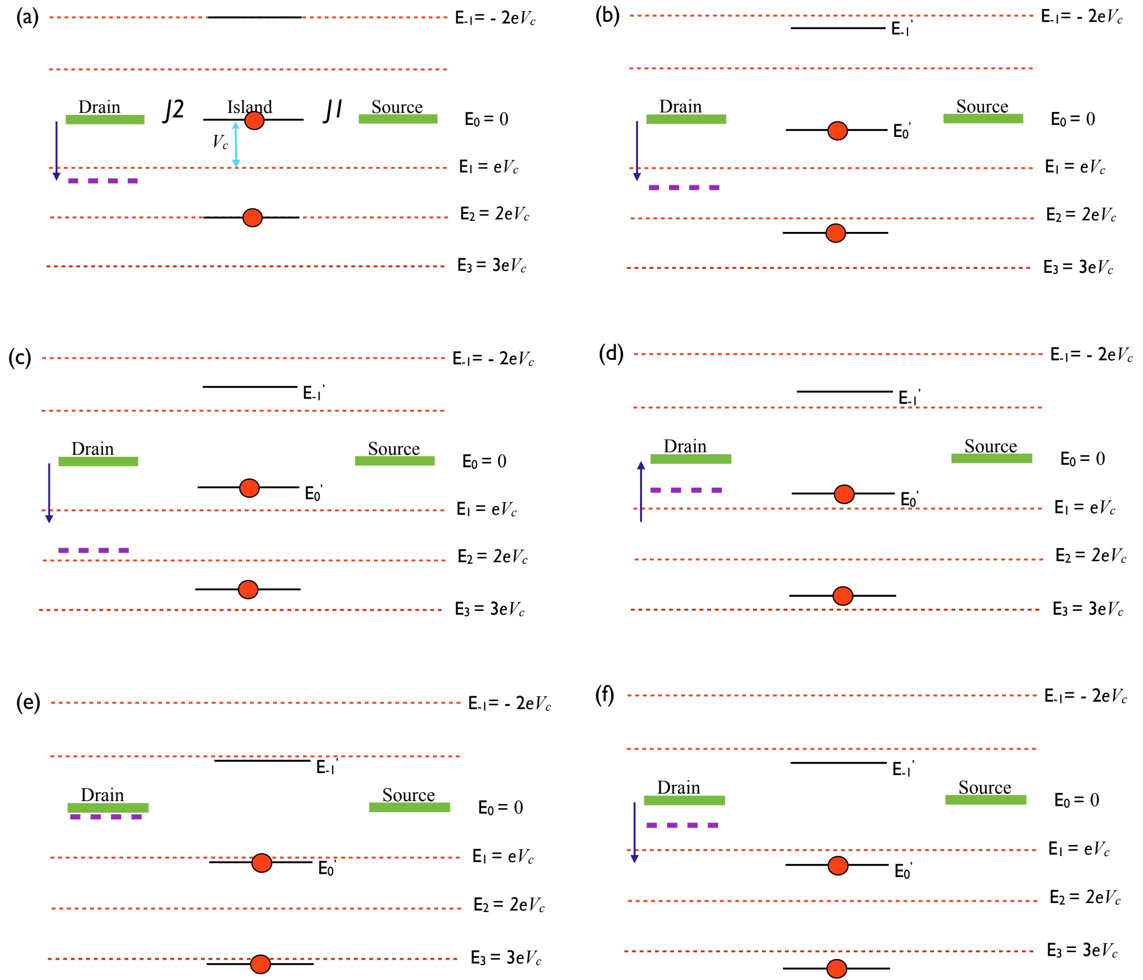


FIG. 4.5 Energy level diagrams of the system wherein the electrochemical potential and hence the conduction channels on the island are modulated by the increasing gate voltage, which in turn gives rise to three different modes of device operation as the source-drain bias is varied.

$V_{SD} = 19.1\,\text{mV}$, more than 90% of the V_{SD} drops across the junction *J2* since $C_1 >> C_2$. Thus, at $V_{SD} = 19.1$ mV *J2* excites first, allowing the transition from the island to the drain that subsequently leads to the current flow across the device [Fig. 4.5(a)]. When V_G is increased from 0 V, it modulates the electrochemical potential on the island and thus

determines the conditions for electron tunneling [Fig. 4.5(b)]. With increasing V_G, the potential on the island increases, leading to a decrease in the drop across *J2* and increase in the drop across *J1*. Therefore, in the first mode of the device operation, V_{SD} has to be increased with the increasing V_G, until the drop across *J2* has sufficient value required for electron tunneling [Fig. 4.5(b), (c)]. Hence, the increase in V_G leads to an increase in V_{th} and the shifting of the blockade as shown in Fig. 4.4. At this new threshold voltage $V_{SD} = V_{th}$, the first transition takes place across *J2* from $E_0^{'}$ to the drain. As explained earlier in Section 4.1, a transition across *J2* is followed by a transition across *J1* from the source to the $E_0^{'}$ on the island resulting in the flow of net one charge across the device. This mechanism continues until $V_G \approx 0.103 \times 0.9 \text{ V} = 0.092 \text{ V}$.

When $V_G \approx 0.093$ V the device enters the second mode of its operation wherein an increase in V_G leads to a decrease in the threshold voltage V_{th} and the Coulomb blockade (Fig. 4.4). At $V_G \approx 0.093$ V as V_{SD} is increased, the drop across *J1* reaches the threshold first before the drop across *J2* could [Fig. 4.5(d)]. Therefore the first transition takes place across *J1* from the source to $E_{-1}^{'}$ level on the island that subsequently tunnels across *J2* to the drain. With further increase in V_G, smaller values of V_{SD} are required for the drop across *J1* to reach the threshold. Hence in the second mode of the device operation, V_{th} decreases with the increase in V_G and ultimately approaches zero when $V_G = \dfrac{e}{2C_G} \cong 0.103\ V$ [Fig. 4.5(e)]. In the second mode, not only does the V_{th} decrease but the blockade width also decreases (Fig. 4.4).

If the gate bias is increased further such that $V_G > 0.103\,V$, the device enters the third mode of its operation [Fig. 4.5(f)]. In this mode it is observed that with increasing V_G, V_{th} increases and the blockade shifts, similar to the behavior observed in the first mode. For gate values $V_G > 0.103\,V$, after the electron has tunneled from the source to the E'_{-1} level on the island, although the drop across *J2* rises, it is not sufficient so that the electron could tunnel across *J2* to the drain and make the electronic transition from source to the drain complete. Therefore V_{SD} needs to be increased to supply the additional energy required for electron tunneling across *J2* [Fig. 4.5(f)]. As V_G is increased further, the drop across *J2* after the electron has tunneled across *J1* keeps decreasing. This necessitates further increase in V_{SD} resulting in an increase in V_{th} with the increasing V_G until $V_G \cong 2\times 0.103\text{ V} = 0.206\text{ V}$. The three modes of device operation repeat as V_G is increased from one even integral multiple of $\frac{e}{2C_G}$ to the next even integral multiple with the device exhibiting a negative slope in $V_{th}(V_G)$ behavior when V_G approaches an odd integral multiple of $\frac{e}{2C_G}$. The range of gate bias in which $V_{th}(V_G)$ variation exhibits a negative slope is expected to depend on degree of asymmetry between the two junctions.

4.3 Physics Behind the Threshold Voltage and the Staircase Structure in a 1D Chain of Islands at $T = 0$ K

4.3.1 Up-steps and the Charge Build-up Leading to the Threshold Voltage V_{th}

The linear variation of device threshold voltage (V_{th}) with the number of

islands along the chain (N) that is proportional to the chain length has been observed in the experimental devices.[1,5,13] The theoretical investigation by Middleton and Wingreen[14] on an array of islands with uniform capacitances but with the potential levels randomly offset by quenched background charges showed that the linear variation of V_{th} with N can be explained by $V_{th} = \alpha N \Delta V$ where α is a constant that depends on the dimensionality of the system and junction-capacitance-to-island-self-capacitance ratio. In the limit where this ratio approaches zero, the screening length $\lambda \rightarrow 0$, and ΔV is a constant change in the applied source-drain bias (V_{SD}) required per "up-step" for the charge front to be able to advance towards the other electrode.[14] The computational study by Elteto, *et al.*[15] has extended this work to a uniform system with a nearest-neighbor inter-island coupling in order to explain the experimental device features observed in the work by Parthasarathy, *et al.*[1] The experimental and computational work by Lee, *et al.*[5], and the computational study done by Savaikar, *et al.*[12] on a disordered system with strong inter-island capacitances and $\lambda \neq 0$, showed that $V_{th}(N)$ is still linear, but ΔV is not a constant and it is difficult to analytically predict the slope of the $V_{th}(N)$ dependence. Carrying forward the argument by Middleton, *et al.*[14] to disordered systems with strong inter-island coupling, we define an up-step in a broader sense, as any electronic transition between two islands or an island and an electrode in the chain that requires a minimum increase in V_{SD}, without which system remains in a static charge state. In this section, we explore and attempt to explain the mechanism at T = 0 K, which has not been addressed in any previous study, of the charge build-up that develops in the system as V_{SD} is increased in order to overcome a series of up-steps, ultimately leading to a steady-state current at V_{th}.

In a disordered system with a sufficiently random distribution in junction widths and island radii, the junction charging energies ($E_c = eV_c$) have a fairly broad distribution [see Fig. 3.6(a) and Fig. 4.6]. As described earlier, junction charging energy is the energy required for a single electron transition across a junction between the two coupled islands determined by all the capacitances in the system. In a system with reasonably strong inter-island coupling such as in the one discussed in Chapter 3, the charging energies that are predominantly influenced by the island radii,[12] and the evolving charge state of the system play a crucial role in determining the V_{th} and the *IV* characteristics. In any static charge state of the system, the change in free energy (ΔW_{ij}) of the system for tunneling between any two islands *i* and *j* has $\Delta W_{ij} > 0$ and the tunneling is forbidden. For any transition to take place at $T = 0$ K, ΔW_{ij} needs to be less than zero and the energy required to overcome the Coulomb energy barrier can be supplied only by the external sources. When a one-dimensional (1D) system such as the one discussed in Chapter 3, consisting of nano-islands with strong inter-island- and self-capacitances and with no background charge is biased by V_{SD} across two semi-infinite electrodes (the source and the drain) the first transition via $\Delta W_{ij} = 0$, at $T = 0$ K, is most likely to take place across the first junction next to the biased electrode, the drain. The semi-infinite sizes of the electrodes decrease the charging energies of their respective associated junctions at the two ends. Furthermore, in the absence of any net charge on the islands, the largest potential drop occurs across the first junction next to the biased drain due to the large self-capacitances of the islands. The largest potential drop allows the first transition to take place across the first junction next to the drain, although the first

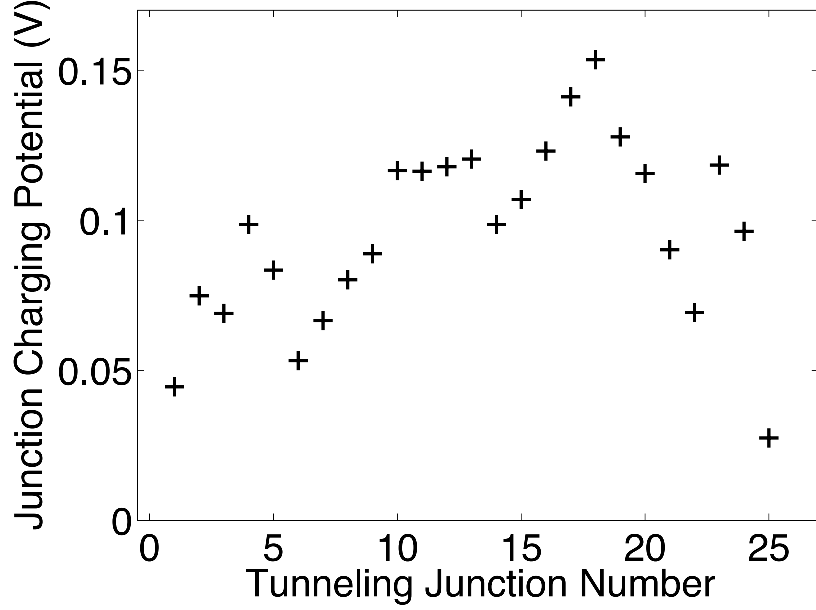


FIG. 4.6 Junction charging potentials of tunneling junctions in sequential order, from the drain on the left to the source on the right, in the 25-junction chain that varies over a range from 0.03V to 0.15V.

junction need not be the one with the minimum E_c in the E_c distribution (Fig. 4.6). If the drain is positively biased the electron tunnels from the first island to the drain thereby creating a hole (+*e*) on the first island. On the other hand, if the drain is negatively biased, the electron tunnels in the reverse direction from the drain to the first island thereby depositing on it a net negative charge (-*e*). In either case, the absolute value of the bias must exceed ΔV of the first up-step that is sufficient to just bring ΔW_{ij} to zero in order for the first transition to take place, thus overcoming the first up-step. This may or may not be followed by a cascade of additional high-rate transitions (avalanche), but ultimately leads to a new static charge state and a new up-step.

We have examined at $T = 0$ K, the up-steps for the disordered 25-junction system that has reasonably strong inter-island couplings, and which was discussed earlier

in Chapter 3. In this case, a total of 27 up-steps were observed while increasing V_{SD} in increments of 7×10^{-6} V from zero to the threshold $V_{th} = 0.74$ V. Table 4.1 shows the static charge distribution in the 25-junction system as it evolves with increasing source-drain bias after overcoming each particular up-step. The vertical axis shows the excess electron number (in this case, a deficiency of electrons) on each island at each particular applied bias, just after the system has overcome an up-step. The horizontal axis indicates the sequential up-step number and the associated increase in the source-drain bias voltage required to overcome the respective up-step. It is observed that upon overcoming an up-step the new static charge state may not necessarily advance the charge front toward the other electrode. For example, as the system overcomes the up-steps 7, 8 and 9 (Table 4.1), the charge front does not advance but is stuck on the 12th island. Furthermore, propagation of the charge front need not necessarily involve a change in the net charge on the device as observed during the overcoming of the last step, although overcoming of all the other up-steps is accompanied by a change in net charge on the device (Fig. 4.7). For a positively biased drain, the net charge in any static charge state on the device is positive with each charged island carrying a net positive charge, while for the negatively biased drain the net charge on each charged island and on the device is negative. At $T = 0$ K, when the drain electrode is positively biased it is highly unlikely that any island would carry a net negative charge when the system is in a static charge state. Note that after the up-step number 27 is overcome, the system has reached its threshold voltage with the arrival of the charge front to the source and a small steady-state current begins to flow. It is observed that the first electron moved from the first island to the drain at $V_{SD} = 8.8\times10^{-2}$ V thereby overcoming the first up-step. The values of ΔV required to overcome

Table 4.1 Excess electron count on each island and the electrodes in a 25-junction chain at critical applied biases when the system just reaches a new static charge state after overcoming an up-step. Vertical axis shows the net charge on the islands starting with drain in the first row and ending with source in the last row. Horizontal axis indicates the up-step number beginning with the first up-step on the left and ending with the last up-step on the right. Overcoming of few of the up-steps is accompanied by the advancement of the charge front while majority of the up-steps (17 out of 27) are overcome when the charge front is stuck at large E_c junctions 13, 15 and 17 that do not allow the charge front to propagate.

ΔV (mV)	87.82	37.00	0.26	0.47	0.07	14.3	0.19	133.71	44.76	37.61	0.10	0.27	14.3	0.70	55.2	0.01	0.14	0.41	0.14	3.89	153.72	0.26	3.44	14.30	37.00	98.75	0.13
Island Number \ Advancement of the Charge Front	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27
1	1	2	3	4	5	7	8	9	10	12	14	15	16	17	19	20	22	23	24	25	26	27	28	29	30	34	834
2	0	0	0	0	0	0	-1	-1	-1	-1	-1	-1	-1	-2	-2	-2	-2	-2	-2	-2	-2	-2	-2	-2	-3	-3	-3
3	-1	-1	-1	-1	-1	-1	-1	-1	-2	-2	-2	-2	-2	-2	-2	-2	-2	-2	-2	-3	-3	-3	-3	-4	-4	-4	-4
4	0	0	0	0	-1	-1	-1	-1	-1	-1	-1	-2	-2	-2	-2	-2	-2	-2	-2	-2	-2	-2	-3	-3	-3	-3	-3
5	0	0	0	0	0	0	0	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-2	-2	-2	-2	-2	-2
6	0	0	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-2	-2	-2	-2	-2	-2	-3	-3	-3	-3	-3	-3	-3	-3	-3
7	0	-1	0	0	0	-1	-1	-1	-1	-1	-2	-2	-2	-2	-2	-2	-2	-2	-2	-2	-3	-3	-3	-3	-3	-3	-3
8	0	0	0	-1	-1	0	0	0	0	-1	-1	-1	-1	-1	-1	-1	-2	-2	-2	-2	-2	-2	-2	-2	-2	-2	-2
9	0	0	-1	0	0	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-2	-1	-2	-2	-2	-2	-2	-2	-2	-2	-2	-2
10	0	0	0	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-2	-2	-2	-2	-2	-2	-2	-2	-2	-2	-2
11	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1
12	0	0	0	0	0	0	0	0	0	0	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1
13	0	0	0	0	0	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-2	-2
14	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1
15	0	0	0	0	0	0	0	0	0	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1
16	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-1	-1
17	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	-1	0	0
18	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-1	-1
19	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
20	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-1	-1
21	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
22	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-1	-1
23	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
24	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
25	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
26	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-800

each subsequent up-step ranged from ~ 14×10^{-6} V up to 0.15 V, as seen in Fig. 4.8. The observed ΔV needed to overcome an up-step may not necessarily be equal to ΔW_{ij} associated with a particular transition, but may be an upper bound since V_{SD} was incrementally changed by a fixed value of 7×10^{-6} V. In the process of overcoming an up-step, frequently one electron and sometimes anywhere from two to four electrons (see Table 4.1 and Fig. 4.7) were seen to move to the drain, leading to a change in the net positive charge on the device during the overcoming of each up-step. The flow of more than a single electron to the drain suggests that there could exist additional up-steps that

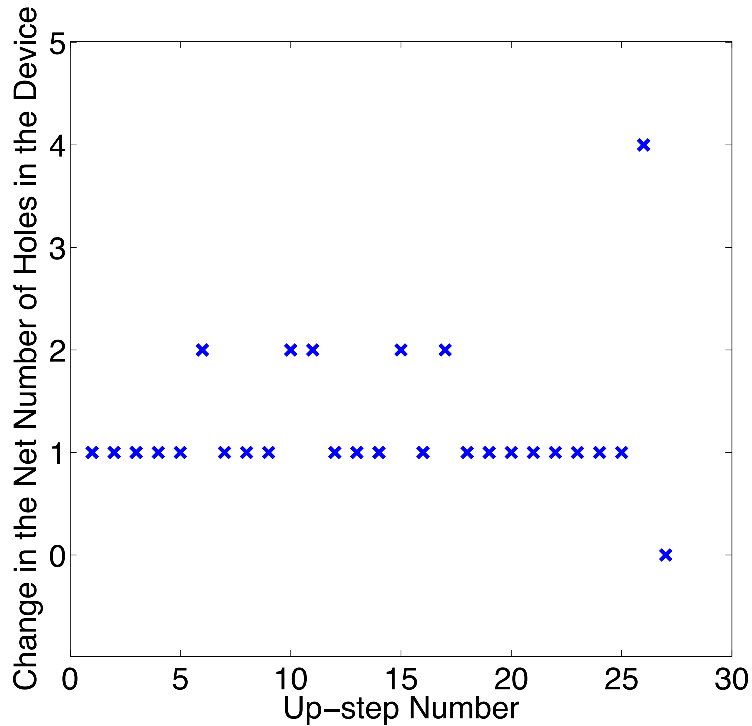


FIG. 4.7 Change in the net number of holes in the device after the system has overcome an up-step. Overcoming of an up-step need not necessarily be accompanied by a change in the net number of holes and hence in the net charge in the device as can be seen during the overcoming of last step.

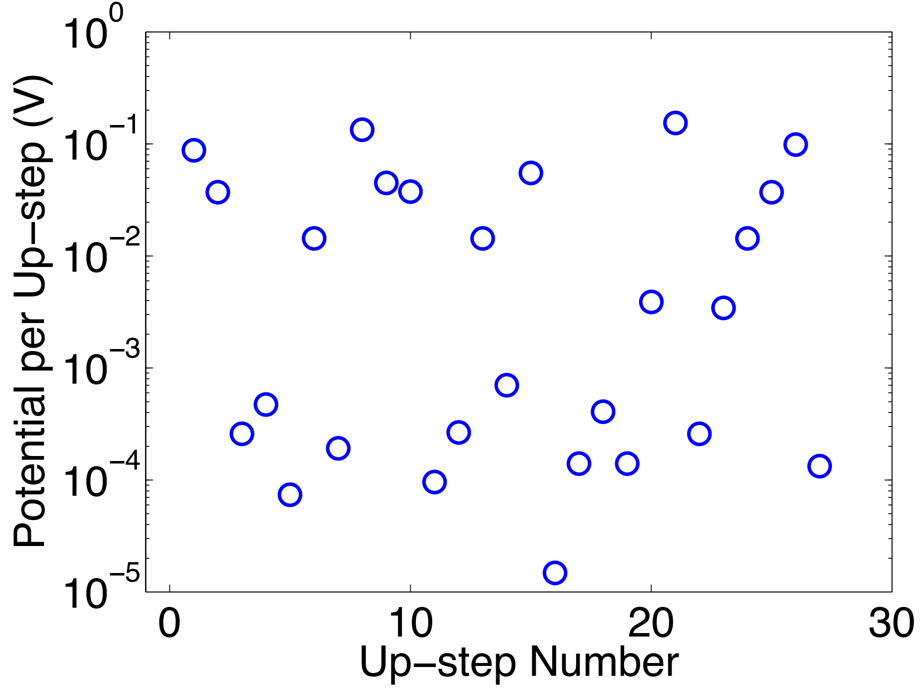


FIG. 4.8 ΔV required to overcome each of the 27 up-steps before the disordered, strongly coupled 25-junction chain reaches the conduction threshold V_{th}. The values vary over a wide range from a minimum of ~14×10^{-6} V to a maximum of ~0.15 V.

actually require less than 7×10^{-6} V to be overcome. During the course of overcoming the 27 up-steps, the charge front advanced only nine times toward the source (Table 4.1). Although it is difficult to establish the relation between the number of up-steps, ΔV and E_c, it is observed that a large number of the up-steps (17 out of the 27) arise when the advancing charge front is halted by large E_c junctions (junctions 13, 15 and 17) especially by those that are further away from the biased drain (junction 17, see Table 4.1). However, it is to be noted that these junctions are not necessarily the junctions having the maximum charging energies (junction 18 has the maximum E_c). Overall, a large fraction of the threshold potential is required to overcome the up-steps when the charge front is halted by large E_c junctions. Overcoming of these "large" up-steps is accompanied by a

considerable increase in the net charge on the device (Table 4.1), and the large build-up of charge helps the electrons to tunnel through large E_c junctions by developing sufficiently large potential drops across these junctions. For example, when the charge front is stuck on island 16 halted by junction 17, the net charge on the device increased by +11*e* from +19*e* to +30*e* (steps 15-25 in Table 4.1). When it finally advances past island 16, the net charge on the system changes from +30*e* to +34*e*. After having overcome all the up-steps at the threshold voltage, the system attains a characteristic background charge state and starts conducting.

The up-steps were also examined at T = 0 K for the 12-junction device by increasing V_{SD} in increments of 140×10^{-6} V from 0 V to the threshold voltage V_{th} = 0.14 V. Altogether, 6 up-steps (Table 4.2) were observed and the value of ΔV required to overcome these up-steps ranged from a minimum of $\sim 140\times10^{-6}$ V to a maximum of $\sim 88\times10^{-3}$ V (Table 4.2 and Fig. 4.9). Overcoming of the first step required the maximum ΔV during which the electron moved from the second island to the drain via the first island. During the course of overcoming all the 6 up-steps, the charge front advanced five times toward the source. Unlike in the 25-junction chain, overcoming of each up-step was accompanied by a change in the net charge on the device and the net charge on the device increased exactly by +*e*, each time an up-step was overcome (Table 4.2).

From the two cases discussed above, it appears that it is difficult to analytically predict the number of up-steps for a given chain length in which the islands are strongly coupled to one another. Unlike in the system studied by Middleton and Wingreen[14], in a disordered system with stronger inter-island coupling, the larger λ limit leads to the potential drops changing as the charge front propagates. The change in potential

Table 4.2 Excess electron count observed on the islands and the electrodes in a 12-junction chain when the system reaches a new static charge state after overcoming an up-step. The vertical axis shows the number of electrons on the islands starting with the drain in the first row and ending with source in the last row. The horizontal axis indicates the up-step number starting with the first up-step on the left and ending with the last up-step on the right. Overcoming of each up-step is accompanied by an addition of one net ($+e$) charge on the system.

ΔV (mV)	87.86	37.00	0.280	0.420	0.140	14.3
Island Number	1	2	3	4	5	6
1	1	2	3	4	5	1672
2	0	0	0	0	0	0
3	-1	-1	-1	-1	-1	-1
4	0	0	0	0	-1	-1
5	0	0	0	0	0	0
6	0	0	-1	-1	-1	-1
7	0	-1	0	0	0	-1
8	0	0	0	-1	-1	0
9	0	0	-1	0	0	-1
10	0	0	0	-1	-1	0
11	0	0	0	0	0	-1
12	0	0	0	0	0	0
13	0	0	0	0	0	-1666

Advancement of the Charge Front

drops along with the distribution of E_c make it difficult to predict from the native structure what the up-steps will be, and therefore, what the threshold voltage will be. The ΔV that is required to overcome the up-steps varies over a wide range that only increases with increasing chain length. Also, it is difficult to identify the specific junction across which the system expends maximum energy to drive ahead the charge front when the charge front stops advancing. Because of the variable voltage drops across the junctions as the charge front advances, that junction need not be the one with the maximum E_c although the results of this analysis indicate that it is typically from among those that have larger charging energies.

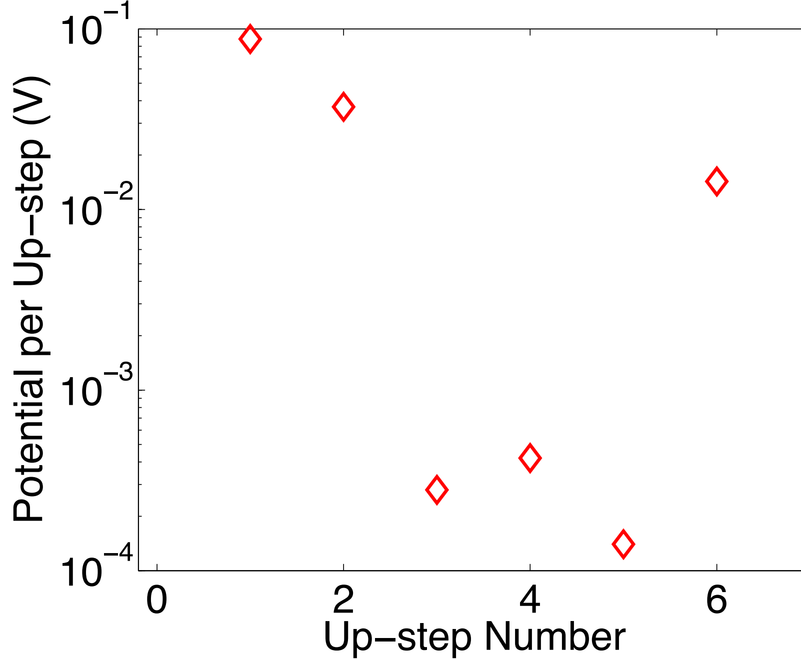


FIG. 4.9 ΔV required per up-step for all the 6 up-steps in a 12-junction long chain device before the device reaches the threshold V_{th}. The values vary over a wide range from a minimum of ~140×10^{-6} V to a maximum of ~88×10^{-3} V.

4.3.2 Mechanism Behind Coulomb Staircase in the *IV* Characteristics at T = 0 K

When the device reaches the threshold voltage V_{th} at T = 0 K, the charge front reaches the grounded source electrode and the device starts conducting. Long 1D chains with sufficient structural disorder exhibit interesting staircase structures in their *IV* characteristics at low V_{SD} that might be used in many applications such as memory devices,[16] sensing[17,18] and information processing. In Chapter 3 we observed that the staircase structures are more pronounced for longer chains. Although much work has been done on single-electron devices exhibiting interesting *IV* characteristics, little effort has been made to explain the exact mechanism behind the origin of staircase structures.

In this section, we explore the exact mechanism behind the charge transport in such devices at low biases that lead to current staircase structures as the bias increases.

When a multi-island device enters the conducting state at $V_{SD} = V_{th}$ after having overcome all the up-steps, it has a unique charge distribution on the islands in its longest lifetime state (LLS). The LLS of the system is defined as the state in which the system spends the longest amount of time (waiting time) before the rate-limiting step (RLS) transition takes place. Once the RLS transition occurs, a series of fast transitions (cascade) takes place that typically leads to a net flow of charge across the device, and ends with the system back again in the LLS. The cascade may not necessarily occur in the sequential order of the junctions. At any particular bias, the microscopic observation of the charge states of the system during its evolution with time shows that the RLS transition takes place across a particular junction as the charge continues to flow across the device, and it is the waiting time for this transition that predominantly determines the current at that particular bias. Therefore, we define the junction across which the RLS transition occurs as the current-limiting junction (CLJ). At $T = 0$ K, the number of Monte Carlo cycles required for the system to come back to its LLS state is observed to be an integral multiple of the number of junctions in the system. During the time the system returns back to the LLS state, one electron is transferred across the device from the source to the drain. As the bias is increased, the transition rate of the RLS transition increases only slowly until the next step in the staircase structure. The transition rates of subsequent transitions across the other junctions following the RLS transition may change drastically as the system periodically (in terms of Monte-Carlo cycles) returns back to the LLS state. However, these fast rates do not have any major effect on the

steady-state device current. Therefore, the device current shows a negligible change until V_{SD} reaches the second step where there is a change in the background charge distribution, the LLS changes, and the device current sharply increases. Since the increase in the device current is often small in between the two consecutive steps as compared to the change in current when the LLS changes at a step, the *IV* curves appears practically flat in the *IV* characteristics in between the steps. At the second threshold, the charge distribution in the LLS state of the system may change considerably. Most frequently, the net charge on the islands that were already charged during the first step increases by one unit and some of the uncharged islands are likely to become charged. This change in the charge distribution along with the increase in the bias V_{SD} alters the transition rates across all the junctions in the system. With the new charge distribution in the LLS state, the RLS transition now typically occurs across a different junction having a larger transition rate. The transition rates of the subsequent cascade of transitions may or may not be altered, although a majority of them show an increase in their values. Hence the device carries a larger current after the second threshold and it continues to do so until it reaches the third threshold. This process continues with the increasing bias at low bias values giving rise to staircase like structures in the device *IV* characteristics as can be seen in Fig. 4.10 for a 12-junction chain. Beyond the first step there are more conduction channels open, each with its own LLS. The dominance of any one LLS diminishes with increasing V_{SD}, and the periodicity in the evolution of charge states breaks down. This mechanism increases the current and eventually washes out the staircase structure as V_{SD} increases. In order to illustrate the mechanism described here in more detail, we have investigated the evolving charge microstates as a function

of increasing bias in the 12-junction device that was earlier described in Section 4.3.1 and Chapter 3.

The *IV* characteristics for a 12-junction chain are shown in Fig. 4.10. When the device first switches on at $V_{th} = 0.14$ V, the system has a characteristic charge distribution in the LLS state of the system that is shown in Fig. 4.11 (magenta circles). It can be seen that five of the eleven islands are charged, each one carrying a net positive charge of $+e$ (a vacancy). The remaining islands are still neutral. At $V_{th} = 0.14$ V, the RLS transition occurs at the rate of $\sim 6.5 \times 10^{7} s^{-1}$ (Fig. 4.12) across the first junction that couples the first island to the drain, thereby limiting the device current at 7.9×10^{-12} A (Fig. 4.10). Therefore the first junction acts as a CLJ at $V_{th} = 0.14$ V. The RLS transition across the first junction is followed by a cascade of transition across the remaining junctions with rates ranging anywhere from 6.8×10^{8} s^{-1} to 5.2×10^{13} s^{-1}. The transition rates across all the junctions at $V_{th} = 0.14$ V are shown in Fig. 4.12, as the steady state system periodically (in terms of Monte Carlo cycles) returns to its LLS while the bias is fixed at $V_{SD} = 0.14$ V. It is observed that the system most frequently returns back to the LLS after 12 cycles. The inset shows a close-in view of the rates at which the system exits the LLS with a specific charge distribution, and the subsequent transitions with different charge distributions occur before the system finally returns back to the LLS again with the same charge distribution. During this time, net one electron flows across the device from the source to the drain. Since the rates are very sensitive to the charge state of the system, it is apparent from the transition rates in Fig. 4.12 that the system nearly periodically visits the same charge state as it evolves through the Monte-Carlo cycles every time it returns

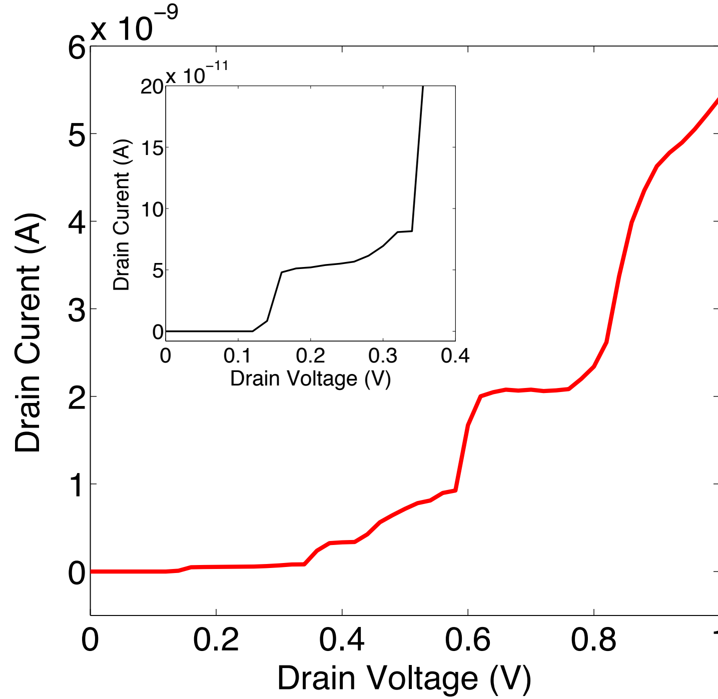


FIG. 4.10 *IV* characteristics of a 12-junction chain at T = 0 K at low V_{SD} bias.[12] The characteristics clearly show a Coulomb staircase structure wherein the steps are neither periodic nor they are uniform. Every step in the staircase is an indication of the fact that one particular current-limiting junction (CLJ) controls the device during that particular bias range. The inset is the close-in view of the *IV* showing a sharp increase in the current at V_{th} giving rise to the first staircase step.

back to its LLS state. As the system evolves through the Monte-Carlo cycles sometimes rare events that have smaller probabilities might occur. But it is observed that the system, by self-correction, immediately returns back to its expected LLS state. During the process the system may take larger number of cycles, which is a higher multiple of 12, before it returns back to the LLS. The periodic process repeats as the constant charge continues to flow across the device unless there is a change in V_{SD}. When V_{SD} is increased to 0.16V, the net charge in the system increases by $+e$ (green diamonds in Fig. 4.11) from +5e to

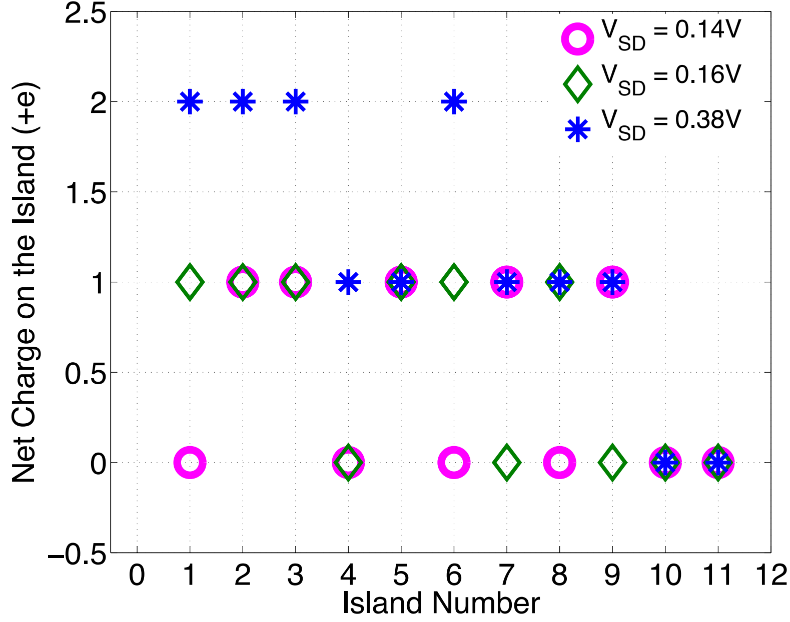


FIG. 4.11 The charge distribution on the islands at three different bias values at $T = 0$ K in a 12-junction chain when the steady state system is in the LLS state. As the bias increases from $V_{SD} = 0.14$ V to $V_{SD} = 0.16$ V, the net charge on the system in its LLS state increases by (+e) from +5e to +6e leading to a change in CLJ from the first junction to the ninth junction and an increase in RLS transition rate. At $V_{SD} = 0.38$ V, the net charge further increases to +13e with the CLJ changing from ninth to the tenth and an increase in RLS transition rate leading to the second step in the *IV*.

+6e and a rearrangement of the charge takes place in the LLS of the system. Due to the rearrangement of the charge and the small increase in V_{SD}, it is observed that the transition rate across the first junction, which earlier controlled the device current, increases substantially from 6.5×10^{7} s^{-1} to 1.9×10^{10} s^{-1}. The first junction does not determine the device current anymore. Rather, the RLS transition now occurs across the ninth junction making ninth junction the CLJ. At $V_{SD} = 0.16$ V, the new CLJ transfers an electron at the rate of 6.9×10^{8} s^{-1}, thereby limiting the device current to 50.4×10^{-12} A.

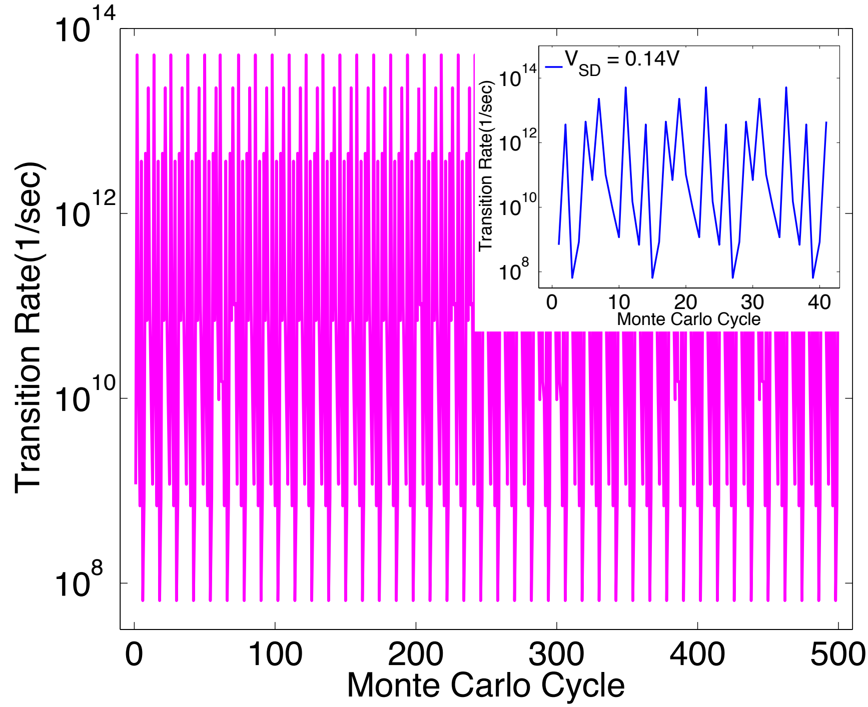


FIG.4.12 The transition rates of the RLS transitions (the minimum value) in a 12-junction chain that occur across a current-limiting junction when the system exits the LLS state and all the rates of other transitions across all the different junctions before the system returns back to its LLS. The system returns to LLS periodically after every 12 Monte Carlo cycles (inset). The inset is a close-in view that shows that the transition rates range anywhere from $6.5\times10^{7}\ s^{-1}$ to $5.2\times10^{13}\ s^{-1}$.

When V_{SD} is increased from 0.14V to 0.16V, since the rate of the RLS transition jumps by a factor of ~ 10, the device current jumps by a factor ~ 6 (see the inset in Fig. 4.10). As the bias is increased further beyond $V_{SD} = 0.16$ V, no appreciable change takes place in the device current up to a bias of $V_{SD} = 0.34$ V. The increase in the current is observed to be negligible, thus giving rise to the first staircase step in the *IV* characteristics. The negligible (on the scale shown) increase observed in the device current as the bias is ramped from $V_{SD} = 0.16$ V to $V_{SD} = 0.34$ V, is due to the increase in the RLS transition

rate across ninth junction, which continues to limit the device current. It is observed that as V_{SD} is increased from 0.16 to 0.34 V, there is a change in the charge distribution in the LLS of the system with a few more islands, either one or two, becoming charged. But that has no major impact on the device current as the RLS transition continues to occur across the ninth junction. As the bias further increases to $V_{SD} = 0.36$ V, there is further increase in the net charge in the device in its LLS and the fourth junction with its higher transition rate momentarily takes over from the ninth junction, and later passes on the control to the tenth junction at $V_{SD} = 0.38$ V. Because of the shifting of the control from ninth to the fourth, and then to the tenth junction, the device current shows a sharp increase as V_{SD} is increased from 0.34 to 0.38 V giving rise to the second step of the staircase in the *IV* characteristics. At $V_{SD} = 0.38$ V, the net charge in the device in its LLS increases to +13e (see Fig. 4.11). Either the net charge on the charged islands increased by one unit charge (+*e*) or some of the neutral islands became charged. As the bias is increased further, the same process continues with every change in the CLJ giving rise to a step in the *IV* that is accompanied by an increase in the net charge in the device. At large biases, since additional conduction channels open up in the charge state space, chances of electronic transitions increase and the periodicity of the system (in terms of Monte Carlo cycles) in returning back to the LLS breaks down. The multiple possibilities of transitions at higher biases and the increasing similarities of lifetimes of the LLS states in each channel lead to the diminishing of the staircase steps in the *IV* characteristics.

4.4 Effect of Temperature on the Device Threshold

After having studied in detail the mechanisms behind the charge build-up leading to the threshold voltage V_{th}, and the mechanisms that produce the Coulomb staircase structure in the *IV* at low V_{SD}, we explore the thermal effects on the Colombo blockade and the threshold voltage V_{th} for a given chain length of the device. Various groups[2, 6, 13, 19-22] have studied the effects of temperature (*T*) on the Coulomb blockade and the device threshold voltage V_{th} either in 1D or multidimensional device structures. In their study of a chain of graphitized nanoparticles, Bezryadin, *et al*.[6] have shown that the V_{th} decreases linearly with the increasing temperature *T*. On the other hand, the investigation done by Xu, *et al*.[13] on the self-assembled ordered close-packed 1D assemblies of quantum dots (QDs) in long SiO_2 nanotrenches show a non-linear variation of V_{th} with *T,* especially at higher *T*. Cordan, *et al.*[21] have observed a similar non-linear behavior in the V_{th} variation with *T* in 2D arrays of Au nano-islands deposited on oxidized silicon. Parthasarathy, *et al*.[2] investigated monolayers of 1-dodecanethiol-ligated gold nanocrystals and proposed a percolation model to explain the observed linear decrease in the Coulomb blockade and V_{th} with increasing temperature. As per their model, for a fairly uniform multidimensional device with no inter-island coupling and where the disorder arises due to the quenched background charges in the substrate, the increase in temperature removes the non-linear threshold-type Coulomb blockade behavior of a fraction of the junctions effectively turning them into linear resistors. They argue that as long as the number of up-steps remains fixed, the increase in *T* does not affect the V_{th}. The V_{th} can be reduced only if there is an actual decrease in the number of up-steps. When the fraction of the linearized

junctions in the system approaches the percolation threshold, a percolating path consisting of a sub-network of linearized junctions is established that bridges the two terminal electrodes and V_{th} becomes zero. We believe that the model may be sufficient to explain the linear variations in V_{th} with decreasing T in multidimensional systems since the linearized junctions that form the percolating path are expected to be those that have small up-step energies and a narrow distribution in the up-step energies. Importantly, in the absence of any inter-island coupling, the step-size does not change with the charge build-up in the system. Using this model, while explaining the non-linear $V_{th}(T)$ behavior observed especially at higher T in long 1D chains of QDs where there is only one conducting path, Xu, *et al.*[13] argue that as the up-step energy increases, it becomes increasingly difficult to overcome the up-steps, especially those having the larger energies. Therefore the system requires a larger increase in temperature for overcoming the same number of up-steps, than it otherwise would require if the up-step energies were smaller. This leads to a sub-linear behavior especially at higher temperatures.

In the backdrop of the observed non-linear behavior of V_{th} with T in the experimental work[13, 21] and our simulation work (see below), and after having broadened the definition of up-steps that is equally valid even in systems having strong inter-island coupling, we believe that the percolation model proposed by Parthasarathy, *et al.*[2] for 2D systems has some limitations in explaining the non-linear behavior of the decrease in V_{th} with the increasing T. We propose that with the change in temperature, the system may follow a different path in the charge-state-V_{SD} space while overcoming the up-steps before reaching the threshold voltage V_{th}. Once a given up-step is thermally overcome, a new charge distribution would exist in the system at the give V_{SD} that ordinarily

would not have at lower temperature at the same V_{SD}. With the change in temperature, and because of non-zero inter-island coupling, the up-steps do not remain the same but are expected to be different with different energies ($e\Delta V$) required for them to be overcome and for the charge to propagate along the chain. For example, the distribution of up-step potentials in Fig. 4.8 and 4.9 is expected to be different at different temperatures. The range of up-step potential distribution may also vary, especially at higher temperatures. The primary reason behind the change in the up-step potential distribution and its range with a sufficient change in temperature is that the system may start with a different static charge state at low V_{SD} with the change in T. A different static charge state at lower V_{SD} is expected to drive the system along a different path in the charge-state space when V_{SD} is increased at a different temperature.

With an increase in T, a thermal broadening of the single-electron charging levels on the islands takes place. Parthasarathy, *et al.*[2] and Elteto, *et al.*[8] argue that this broadening occurs by an amount equal to $2.4k_BT$, wherein the electrons from below the Fermi level E_F get excited thereby creating vacancies down to the $E_F - 1.2k_BT$ level and filling up the levels above the Fermi level up to $E_F + 1.2k_BT$. Any junction having a charging energy $E_{c,ij} < 2.4k_BT$ becomes linearized and will charge the islands in its neighborhood by allowing the electronic transitions even if $\Delta W_{ij} > 0$. At V_{SD} = 0 V, as T is increased and a larger number of junctions are linearized, the static charge state of the system changes, as compared to that at T = 0, with an increased number of islands being charged.[2] Different static charge state at V_{SD} = 0 V will allow the system to traverse along a different path in the charge-state-V_{SD} space as V_{SD} is increased. Also with increasing

temperature, the number of up-steps and the energy per up-step ($e\Delta V$) are expected to decrease, relative to those at $T = 0$, resulting in a decrease in the Coulomb blockade and V_{th}. We believe that the increased chance of electronic transitions especially those with $\Delta W_{ij} > 0$ make the job of identifying *a priori* the up-steps, and determining their sizes difficult especially at higher temperatures. Further investigations are necessary to examine the mechanism behind the decrease in V_{th} with the increase in temperature especially in 1D systems having strong inter-island coupling, and the non-linear behavior observed at higher temperatures.

Figure 4.13 shows the *IV* behavior of a 12-junction QD chain at different temperatures, while the accompanying decrease in V_{th} with the increasing temperature is shown in Fig. 4.14. The device threshold V_{th} with a value of ~0.14V at $T = 0$ K, decreases linearly with the increasing temperature in agreement with the observations made by Parthasarathy, *et al.*[2], and ultimately reaches zero at ~65 K. But considering the small thermal energy at 65 K and the distribution of potentials for the up-steps (ΔV) at $T = 0$ K (Fig. 4.9) of all the up-steps that need to be overcome before conduction starts, it is quite evident that the mechanism must be different or at least modified from that proposed by Parthasarathy, *et al.*[2] ΔV is spread over a large range from $10^{-4} - 10^{-1}$ V (Fig. 4.9) while the thermal potential range over which the V_{th} decreases linearly before reaching zero is 0-5 mV (Fig. 4.14). The system cannot overcome the larger up-steps with such a small increase in temperature. Also, if V_{th} had to decrease only when there is a decrease in the number of up-steps with increasing temperature, and not just with the increase in temperature as proposed by Parthasarathy, *et al.*[2], and considering the distribution in

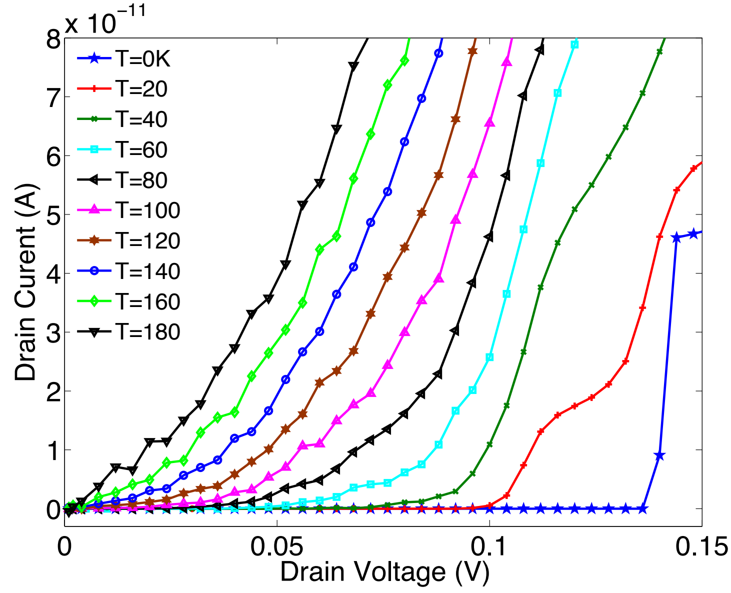


FIG. 4.13 *IV* characteristics of a 12-junction chain device at different temperatures varying from 0-180 K. An increase in temperature decreases the blockade and V_{th} (see Fig. 4.14) and the *IV* characteristics are shifted towards smaller V_{SD} with the decrease in the V_{th}. No appreciable change is observed in the device conductance with increased *T*.

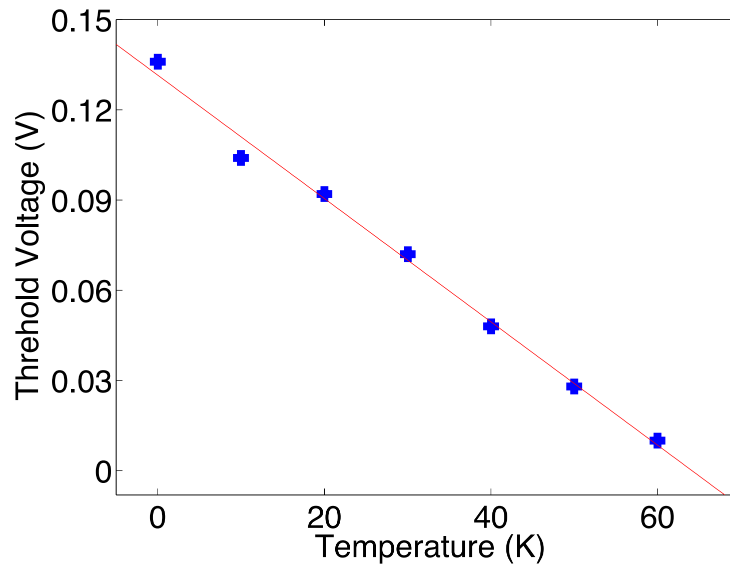


FIG. 4.14 The variation of V_{th} with the temperature of a 12-junction chain device showing a linear decrease with a constant gradient. When the temperature reaches ~ 65 K the blockade and V_{th} reaches zero.

ΔV (Fig. 4.9) and the temperature range in Fig. 4.14, we would anticipate that the decrease in V_{th} will not be smooth and linear with the increasing temperature. This strengthens our argument that with every change in temperature, the system starts with a different charge state at $V_{SD} = 0$ V and traces a different trajectory in the charge-state-V_{SD} space with different up-steps having different step sizes.

With the linear decrease in the threshold voltage V_{th}, the *IV* characteristics are shifted towards smaller V_{SD} values without any appreciable change in the device conductance. Parthasarathy, *et al.*[2] have made similar observations on their large but fairly uniform 2D arrays of Au nanocrystals. The *IV* characteristics in Fig. 4.13, especially at lower temperatures, show staircase steps that are not visible in 2D systems.[2] Any chances of having such steps in uniform 2D systems are minimized by either the potential for multiple conducting paths that may carry the current in 2D systems or the narrow distribution in the junction widths of the narrower junctions that make the dominant conducting path if there exists one (see Chapter 5). Although the big staircase steps in the *IV* disappear with increasing *T*, a few small steps appear at larger *T* even as V_{th} reaches zero at ~65 K. Further investigations are required to ascertain the relation, if there exist any, between the staircase steps at different temperatures. After V_{th} has reached zero at ~65 K, if *T* is increased further, the zero bias conductance (G_0) of the device shows a thermally activated behavior $G_0(T) \sim \exp(-U / k_B T)$ with the increasing *T*. It is to be noted that after doing the curve fitting, the activated behavior is observed to be characterized by an energy barrier (*U*) of ~72meV which is perhaps related to the junction charging energy range of $\sim 44 - 115$ meV, with a mean of 72 ± 22 meV.

The *IV* characteristics at different temperatures for a 25-junction long chain

are shown in Fig. 4.15. Unlike in a 12-junction chain, Fig. 4.16 shows the non-linear variation of V_{th} with T similar to the experimental observations made by Xu, *et al.*[13] on 1D chains. The 25-junction *IV* characteristics show distinct and well-defined Coulomb staircase steps even at relatively higher temperatures up to 140 K. It can be observed in Fig. 4.15 that as the temperature increases from 0 K up to ~40 K, the increase in T does not appear to have any major impact on the *IV* besides the discernible decrease in V_{th}. The device current at the first staircase step does not show any appreciable change as T is increased. In the temperature range ~0 - 40 K, the variation of V_{th} with T shows a larger negative temperature coefficient (Fig. 4.16). In this temperature range V_{th} decreases substantially with the increasing T. When the temperature is increased further from 60 K, no new steps arise in the threshold region and V_{th} decreases by smaller amounts with the increasing T, thereby lowering the negative temperature coefficient (Fig. 4.16). It appears that there exists a critical temperature range between ~ 0-60 K that separates the two regions having different temperature coefficients. When T is increased further from ~ 60 K, the *IV* characteristics for different T are well distinguishable from one another with the appearance of multiple staircase steps. For a given bias, the steps for different temperatures appear to be shifted upward with increasing T with a smoothing or rounding of the sharp step edges. We have observed a similar behavior in the 50-junction long chain with more prominent staircase structure at higher T. The decrease of V_{th} with T shows a non-linear behavior similar to that of the 25-junction chain, but with a much steeper decrease in V_{th} as the temperature is raised from 0 K. The steeper decrease in V_{th} with the increase in the chain length, as T is increased from 0 K, is in agreement with the experimental observations made by Parthasarathy, *et al.*[2]

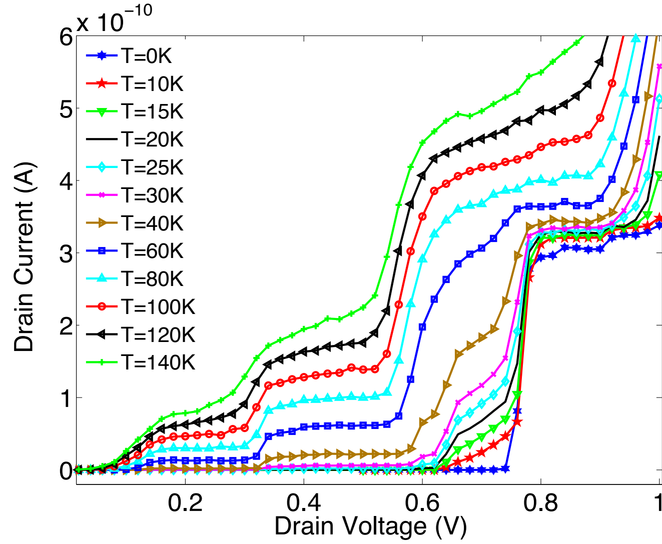


FIG. 4.15 *IV* characteristics of a 25-junction chain device at different temperatures varying from 0-140 K. Increase in temperature decrease the blockade and V_{th} (see Fig. 4.16). The *IV* characteristics show distinct and well-defined staircase steps for $T \sim$ 60-140 K and are well distinguishable from one another at different *T*. For T ~0-40 K, besides the decrease in V_{th}, there is no appreciable change in the *IV* characteristics.

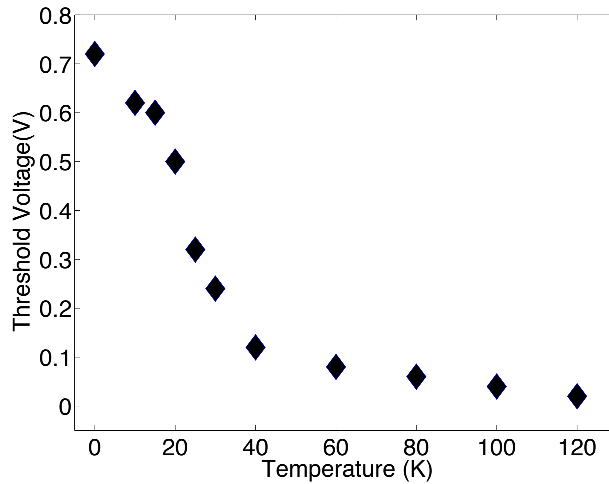


FIG. 4.16 Variation of V_{th} with the temperature of the 25-junction chain device showing a non-linear decrease. The variation shows two different regions with different gradients separated by a critical range T ~40-60 K. The gradient is smaller in the high temperature region, which is in agreement with the observations made by Xu, *et al.*[13] on 1D chains of QDs.

Investigating the microscopic charge states of the system at different temperatures is the next logical step to prove and validate our hypothesis that is proposed earlier in the section to explain the non-linear behavior of $V_{th}(T)$. But the task may not be easy because of the continuous thermal excitations that are expected especially at higher temperatures.

References

[1]R. Parthasarathy, X.-M. Lin, and H. M. Jaeger, Phys. Rev. Lett. 87, 186807 (2001).

[2]R. Parthasarathy, X.-M. Lin, K. Elteto, T. F. Rosenbaum, and H. M. Jaeger, Phys. Rev. Lett. 92, 076801 (2004)

[3]V. Ray, R. Subramanian, P. Bhadrachalam, L. C. Ma, C. Kim, and S. J. Koh, Nat. Nanotechnol. 3, 603 (2008).

[4]A. S. Cordan, A. Goltzene, Y. Herve, M. Mejias, C. Vieu, and H. Launois, J. Appl. Phys. 84, 3756 (1998).

[5]C. H. Lee, S. Qin, M. A. Savaikar, J. Wang, B. Hao, D. Zhang, D. Banyai, J. A. Jaszczak, K. W. Clark, J.-C. Idrobo, A.-P. Li, and Y. K. Yap, Adv. Mater. 25, 4544 (2013).

[6]A. Bezryadin, R. M. Westervelt, and M. Tinkham, Appl. Phys. Lett. 74, 2699 (1999).

[7]P. S. K. Karre, P. L. Bergstrom, G. Mallick, and S. P. Karna, J. Appl. Phys. 102, 024316 (2007).

[8]K. Elteto, E. G. Antonyan, T. T. Nguyen, and H. M. Jaeger, Phys. Rev. B 71, 064206 (2005).

[9]K. K. Likharev, Proc. IEEE 87, 606 (1999).

[10]M. Amman, R. Wilkins, E. Benjacob, P. D. Maker, and R. C. Jaklevic, Phys. Rev. B. 43, 1146 (1991).

[11]D. V. Averin and K. K. Likharev, in *Mesoscopic Phenomena in Solids*, edited by B. Altshuler *et al*. (Elsevier, Amsterdam, 1991), p. 173

[12]M. A. Savaikar, D. Banyai, P. L. Bergstrom, and J. A. Jaszczak, J. Appl. Phys. 114, 114504 (2013)

[13]K. Xu, L. Qin, and J. R. Heath, Nat. Nanotechnol. Lett. 4, 368 (2009).

[14]A. A. Middleton and N. S. Wingreen, Phys. Rev. Lett. 71, 3198 (1993).

[15]K. Elteto, E. G. Antonyan, T. T. Nguyen, and H. M. Jaeger, Phys. Rev. B 71, 064206 (2005).

[16]K. Yano, T. Ishii, T. Hashimoto, T. Kobayashi, F. Murai, and K. Seki, IEEE Trans. Electron Devices 41, 1628 (1994).

[17]R. J. Schoelkopf, P. Wahlgren, A. A. Kozhevnikov, P. Delsing, and D. E. Prober, Science 280, 1238 (1998).

[18]R. G. Knobel and A. N. Cleland, Nature 424, 291 (2003).

[19]C. T. Black, C. B. Murray, R. L. Sandstrom, and S. H. Sun, Science 290, 1131 (2000).

[20]D. D. Cheam, *Integration of Room Temperature Single Electron Transistor with CMOS Subsystem*, PhD dissertation, Michigan Technological University, Houghton, MI, 2009.

[21]A. S. Cordan, Y. Leroy, A. Goltzene, A. Pepin, C. Vieu, M. Mejias, and H. Launois, J. Appl. Phys. 87, 345 (2000).

[22]A. J. Quinn, M. Biancardo, L. Floyd, M. Belloni, P. R. Ashton, J. A. Preece, C. A. Bignozzi, and G. Redmond, J. Mater. Chem. 15, 4403 (2005).

Chapter 5: Simulation of Disordered Two-Dimensional Systems[1]

In Chapter 3, the simulation study of single electron charge transport in multi-island 1D systems investigated the effect of chain length, temperature and the disorder in the chain on the device characteristics. The physics behind the charge build-up leading to the threshold voltage V_{th} and the mechanism of charge transport behind the staircase structure in a disordered 1D system were investigated in detail in Chapter 4 that explained the *IV* characteristics of these 1D devices. After having extensively explored the 1D systems, we now extend the use of MITS to the study of charge transport in multi-island 2D systems and begin to explain some of the interesting device characteristics that are observed in 2D experimental devices.

Experimental studies have been explored for a range of 2D devices that show a rich variety of device properties in different regimes of charge transport. The experimental study explored by Cordan, *et al.*[1] on Au grains has shown that in 2D systems with a distribution in junction widths, there is a wide distribution of tunneling resistances among the junctions. The devices show a reasonable Coulomb blockade at low temperatures. To explain the device characteristics in such 2D devices, Cordan, *et al.*[1] proposed a hypothesis that there exists an optimal path called a dominant conducting path (DCP) that carries a majority of the device current. The existence of such a dominant path turns the device effectively into a quasi-1D device. Although a reasonable hypothesis, the existence of DCPs was not clearly demonstrated by Cordan, *et al.*[1], and to

[1]Much of the work in Chapter 5 is planned for submission for publication in the near future.

our knowledge has not been adequately investigated to date. Furthermore, in their work on the temperature behavior of multiple tunnel junction devices,[2] they demonstrated that the threshold voltage V_{th} decreases with an increase in temperature, and V_{th} increases with the increase in the length of multi-junction arrays. In a study of 1D and 2D arrays consisting of Al islands linked by Al/Al_xO_y/Al tunnel junctions, Rimberg, *et al.*[3] observed that beyond V_{th}, the *IV* characteristics follow a power law behavior $I \propto \left(V_{SD} - V_{th}\right)^{\zeta}$ with the exponent $\zeta = 1.8 \pm 0.16$ in 2D systems. Self-assembled quasi-1D chains of graphitized nanoparticles exhibit power law *IV* behavior with ζ varying over a range from ~1 to 2.3 for different samples.[4] For a given sample characterized at different temperatures, the threshold V_{th} decreases linearly with the temperature without any staircase structures in the *IV* characteristic. Experimental studies done by Kurdak, *et al.*[5] on a 2D square array of Al islands linked by Al/Al_xO_y/Al tunnel junctions showed that for $V_{SD} < V_{th}$ the current is thermally activated with an activation energy that is proportional to $V_{th} - V_{SD}$. Above V_{th}, I scales as $\left(V_{SD} - V_{th}\right)^{\zeta}$ with ζ ranging anywhere between ~1.5 to 2.0 depending on the sample. Black, *et al.*[6] studied spin-dependent tunneling in self-assembled cobalt-nanocrystal superlattices, and demonstrated that the linear *IV* behavior at T = 300 K becomes increasingly nonlinear with decreasing the temperature below T = 70 K, and the resistance increases monotonically with decreasing T at smaller energy scales. The device also demonstrates a power law behavior beyond V_{th} with ζ ranging anywhere between 2.2 and 2.7. Similar observations have been made by Quinn, *et al.*[7] for arrays of nanocrystal gold islands wherein the *IV* characteristic shows a non-linear behavior with the resistance increasing monotonically with

decreasing temperature. They claim that the observations are consistent with the Neugebauer–Webb model[8] for tunneling transport through an array of isolated, monodisperse, metallic islands, where the carrier density is thermally activated. The devices fabricated by Cheam[9] using 2D arrays of larger (~30-50nm) tungsten nanocrystals exhibit a similar behavior but at larger energy scales, wherein the device current increases substantially with increasing temperature. On the other hand, Parthasarathy, *et al.*[10] in a study of monolayers of weakly coupled gold nanocrystals show that the measurements delineate two regimes of charge transport separated by a crossover temperature T^*. Below T^* the *IV* characteristic retains its non-linear behavior with the curves shifting towards zero bias due to the liner decrease in the V_{th} with the increasing *T*. Above T^* the low-bias device conductance increases rapidly with *T,* exhibiting a thermally activated behavior similar to the observations made in our simulation study of 1D systems (Chapter 4). To explain the $V_{th}(T)$ variation, they have extended the idea of up-steps proposed by Middleton and Wingreen[11] to non-zero temperatures, arguing that V_{th} decreases because the number of up-steps decreases with increasing temperature. The increasing temperature removes the non-linear Coulomb blockade behavior of an increasing number of tunnel junctions effectively turning them into linear resistors. At T^* the fraction $p(T)$ of linearized tunnel junctions reaches the percolation threshold for the system, which is a property of the dimensionality and the lattice structure, and V_{th} reaches zero. A continuous percolation path of linearized tunnel junctions without a discernible Coulomb blockade is established across the array between the two electrodes that enables the conduction across the device. For highly ordered

systems beyond the threshold V_{th} for $T < T^*$, the IV characteristic follows a power law behavior with a temperature-independent exponent ζ = 2.25 ± 0.1. For $T > T^*$, the linear zero-bias device conductance exhibits thermally activated behavior with a characteristic energy. In their other work on 2D systems Parthasarathy, *et al.*[12] have shown that in a disordered system with a significant fraction of voids, the exponent ζ in the IV power law behavior changes in the crossover region as V_{SD} is increased. For structurally ordered arrays, the V_{th} increases linearly with the increasing array length between the source and the drain. Some of the experimental device features like the power law IV behavior, V_{th} variation with temperature, and the increase in V_{th} with the increase in the array length have been simulated and discussed in the earlier chapters for 1D systems. In this chapter, we simulate 2D systems using MITS and explain some of the behaviors that are observed in the experimental 2D devices introduced above.

First, we test the hypothesis that was proposed by Cordan, *et al.*[1] that in a multidimensional disordered system, there exists an optimal current path, a DCP that makes the device behave effectively as a quasi-1D device. We show that there may indeed exist a DCP in 2D devices provided there is sufficient disorder in the system. Next, we investigate the effects of temperature and a lateral gate bias on the IV characteristics of a device exhibiting a strong DCP. Finally, we simulate a quasi-1D device consisting of only those junctions and islands that are positioned along the DCP and compare its characteristics with those of the parent 2D device in which the DCP is present.

In order to simulate and study the experimental 2D devices that have disorder in

their inter-island spacings, we first generate, using MITS, a physical model of the device using hard-sphere Metropolis Monte Carlo simulation to generate a configuration of spherical islands confined to a plane with a desired mean areal density and randomized distribution of spacings. A square grid of islands each having a diameter of 6.5 nm, a packing fraction of ~0.68 and a particle density of $\sim 20 \times 10^{-3}$ nm^{-2} was evolved through Monte Carlo cycles to generate a random configuration of islands. After the system has evolved through Monte Carlo cycles, two terminal electrodes, the source and the drain (shown in green circles in Fig. 5.1) each having a radius of ~25nm are deposited, separated from each other by a gap of ~50 nm. The virtual device structure that is generated is similar to the 2D experimental devices fabricated and studied by Parthasarathy, *et al.*[10] having an inter-island spacing of ~1.5-2.6 nm, and the Au nanocrystal core diameter of ~4.5-6.5 nm. In the experimental devices, as discussed earlier in Section 2.2.3, the inter-particle current flow between the Au nanocrystals takes place through the 1-dodecanethiol ligands that act as mechanical spacers between the particles, and which modify the height of the tunneling barrier.[10] The electron effective mass of $0.42m_e$, where m_e is the free electron mass, and the tunneling barrier height of 1.39 eV for the simulated system are chosen from Ref. 13.

As an artifact of using the hard-sphere model to generate random island configurations, some islands are too close to each other as compared to configurations resulting from the physical process discussed in Ref. 10 and Ref. 12. Therefore, before simulating the device, the island size is shrunk by 1.5 nm to 5 nm without affecting the particle density, in order to impose a minimum nearest-neighbor inter-island spacing of ~1.5 nm as observed in the experimental system. The initial island sizes were

chosen to be large enough such that after this shrinking step, the average island size was approximately the mid value of the island size in Ref. 10. This reduces the packing fraction to ~0.40 from ~0.68 in the original system. In all the 2D and 1D devices investigated in the rest of the chapter, the drain electrode positioned on the right is biased positively while the source electrode on the left is always grounded. Whenever the transistor characteristics are studied in any of the devices, the gate electrode is placed laterally above the active device region. The gate length of ~150 nm is sufficiently large that it spans the entire longitudinal length of the active device area. The self-, gate-, and inter-island capacitances in the system were computed using the finite-element-method capacitance solver developed by Banyai, *et al*.[14]

In all the device schematics shown in this chapter, the colored lines connecting any two islands indicate that there is a current flow through that junction of more than 20% of the total device current. A red line indicates that the value of junction current is anywhere from 80-100% of the total device current; likewise, a blue line from 60-80%; a green line from 40-60%; and a yellow line from 20-40%. It must be noted that the nanocrystals in each of the experimental device samples were monodispersed to within 5%[10] as against the uniform islands in the MITS simulated systems. Since the configurations generated using MITS have evolved starting from a square grid rather than a close-packed triangular grid for the initial island positions, we expect a relatively large amount of disorder in inter-island spacings in the simulated devices, possibly more than that in the experimental devices. This large degree of disorder could have an appreciable effect on the device properties. Furthermore, the active device area in the experimental devices consist of an array size of ~ 128×270 islands that is substantially

larger than the simulated device having an array size of $\sim 8 \times 9$ islands. The dielectric constant of 2.1 used in the simulations is that of dodecanethiol that ligates the neighboring islands.[10] While interpreting the results, any comparisons between those of the simulated and the experimental devices should consider the differences in their structures, especially the array sizes.

5.1 *IV* Characteristics of a Device Exhibiting a DCP and the Effect of V_{SD} on the DCP

Unlike in a 1D system where the electron has only one path to traverse between the source and the drain, in a multidimensional system there may exist multiple paths along which the electrons might flow between the two electrodes. The number of effective paths depends on the degree of uniformity in the system. In the disordered 2D system shown in Fig. 5.1, we observe, as hypothesized by Cordan, *et al.*[1], that the majority of the device current flows across one dominant conducting path (DCP). Since there are multiple neighboring islands to which an electron on any island can tunnel, and because the associated tunneling probabilities (rates) depend on multiple factors, the electron on any island is most likely to tunnel to an island at an optimal distance. The optimal distance is determined by the complex interplay at the local level of multiple factors affecting ΔW_{ij}, such as the junction charging energy $E_{c,ij}$, the junction potential drop V_{ij}, system's charge state, and the tunneling resistance across the junctions, R_{ij}. The inter-island electron transfer through junctions of optimal distances ultimately leads to a DCP that carries majority of the device current in the system. We believe that the electron transfer through an optimal distance at the local level in such

disordered 2D systems, consisting of nano-islands that are sufficiently large having a continuous energy spectrum but small enough that charging energies are appreciably large, may be similar to the variable-range hopping (VRH) mechanism studied by Mott[15] and Efros and Shklovskii[16] and later extensively investigated by other groups[17, 18] as well. More research is needed to investigate the similarities and the differences between the two mechanisms. We hypothesize that an increase in temperature is expected to either change the DCP or open additional conducting paths in a multidimensional system, especially in those consisting of bigger islands that can lead to an increase in device current at a given bias. The additional paths that may open with increasing temperature depend on the amount of disorder in the system.

Figure 5.1(a) shows a schematic of device consisting of 67 islands that are randomly positioned in a 2D plane between the source and the drain electrodes. The nearest-neighbor inter-island spacings range anywhere from ~1.5–5 nm with a mean spacing of $\sim 2.7 \pm 1.0$ nm. The nearest-neighbor inter-island capacitances range anywhere from $\sim 1.5 \times 10^{-20} - 10 \times 10^{-20}$ F. Although the islands are all the same size, the island self-capacitances range from $\sim 0.6 \times 10^{-20} - 4 \times 10^{-20}$ F. The islands lying along the periphery of the active device area have large self-capacitances while those lying in the central region of the device have smaller self-capacitances due to shielding effects by the neighboring islands. The lateral gate placed at a distance of ~100 nm from the top of the device is grounded. Because of the lateral position of the gate and due to the shielding effects, the gate capacitances in the system range from $\sim 0.2 \times 10^{-20} - 2 \times 10^{-20}$ F. The islands lying in the central region are observed to have smaller gate capacitances while those lying at the periphery closer to the gate have larger values. Although the

values of junction charging energies in the system lie in the range of ~0.2-0.5 eV, the energies of those junctions that actually take part in the conduction are smaller (~0.2-0.33 eV) with a narrower distribution. As discussed earlier in the case of 1D systems, the junction tunneling resistance increases exponentially with the junction width and the tunneling barrier height. The tunneling barrier heights are not fixed but are taken to vary linearly with the potential drop across the junction. The charges on the neighboring islands also influence the potential drops and hence the tunneling barrier heights across the junctions.

Figure 5.1(a) shows the DCP that exists in a device at $T = 0$ K, $V_G = 0$ V and $V_{SD} = 2$ V consisting of 10 junctions carrying the majority of the device current. The device *IV* characteristics are shown in Fig. 5.2. The local currents flowing through each of the junctions in the DCP are shown in the inset in Fig. 5.2. The strength of the conducting path is measured by the fraction of the total device current being carried by the path. While the robustness of the conducting path is measured by the impact the external factors such as gate voltage, source-drain bias and the temperature have on the path. We define any conduction path in the device as a fairly strong path that carries more than 50% of the total device current. It is observed that the DCP at $V_{SD} = 2$ V is a fairly robust path that partly splits into two weaker paths carrying smaller currents [green and yellow in the inset in Fig. 5.2] closer to the drain. Because of the robust nature of the DCP path as a function of source-drain bias, the device behaves as quasi-1D device consisting of a chain of the DCP junctions and islands. Although the apparent threshold voltage of the device appears to be ~1 V, the actual threshold voltage V_{th} is determined to be 0.78 V. Two small staircase steps are observed in the *IV* around the threshold region. The

device does not appear to exhibit many staircase steps despite the presence of a DCP. Two factors may be responsible for the presence of weak staircase steps in the *IV* characteristics. First, the DCP that carries the majority of the device current is a short path consisting of only 10 junctions. We have already concluded in Chapter 2, and later explained in Chapter 3 that the staircase structure is more prominently observed in longer 1D chains. The other and more important reason is the very narrow distribution in the DCP junction widths with minimal standard deviation (discussed in later sections). Furthermore, the self-capacitances of the DCP islands are expected to have a smaller mean with a smaller standard deviation. When the bias voltage V_{SD} is increased beyond the apparent threshold, device current increases linearly with V_{SD}, exhibiting a constant conductance. The linear increase in the device current indicates that with a small bias of $V_{SD} = 2$ V across a longitudinal array length of 9-10 junctions between the source and the drain, no single junction in the DCP experiences a significantly larger potential drop that may substantially reduce its tunneling barrier height. With no appreciable change in their barrier heights, the DCP junctions are expected to have a constant conductance as V_{SD} is increased [inset in Fig. 5.2]. The linear increase in the device current also indicates that the DCP is a fairly robust path that remains intact at its fixed position [Fig. 5.1(a-e)] in the device thereby retaining the qusi-1D nature of the device as the bias V_{SD} is increased. Figures 5.1(b-e) shows the position of the DCP at four different values of the V_{SD} as it is increased from 0 V to a maximum of 2 V. It is observed that the current flows across the same path as V_{SD} is varied although the strength of the DCP (percent of the total device current that is carried by junctions in the DCP) varies with the changing bias. The DCP is

fairly robust at low bias value of $V_{SD} = 0.98$ V [Fig. 5.1(b)] with majority of the DCP junctions carrying current anywhere between 60-80% of the total device current. As V_{SD} is increased to 1.39 V [Fig. 5.1(c)], the DCP weakens relative to other junctions, especially closer to the drain, with the current through the DCP junctions closer to the drain dropping below 60% of the total current. One additional weaker path opens up closer to the drain that appears to merge with the DCP nearer to the source. When V_{SD} is

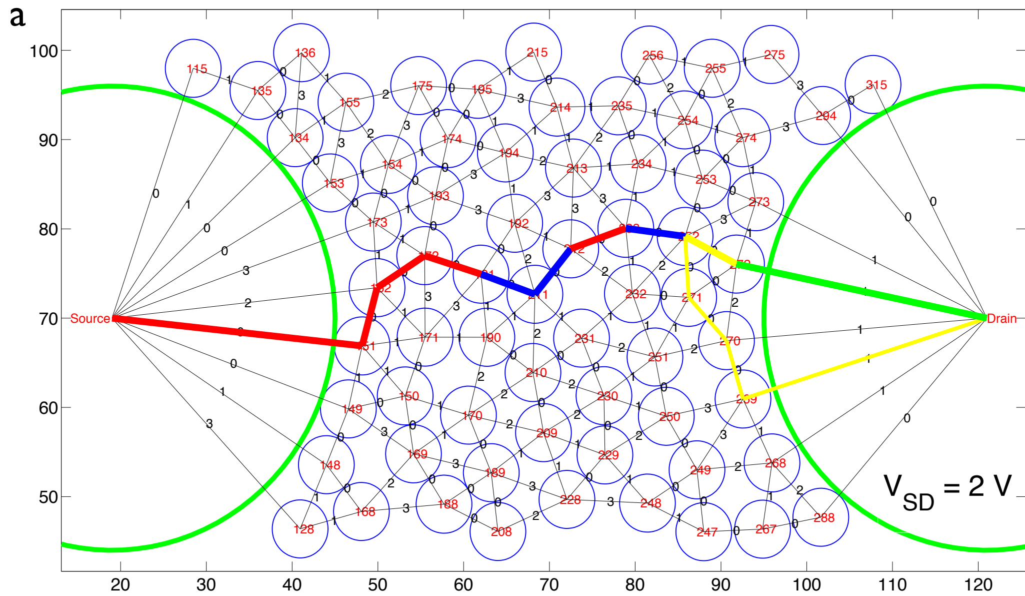
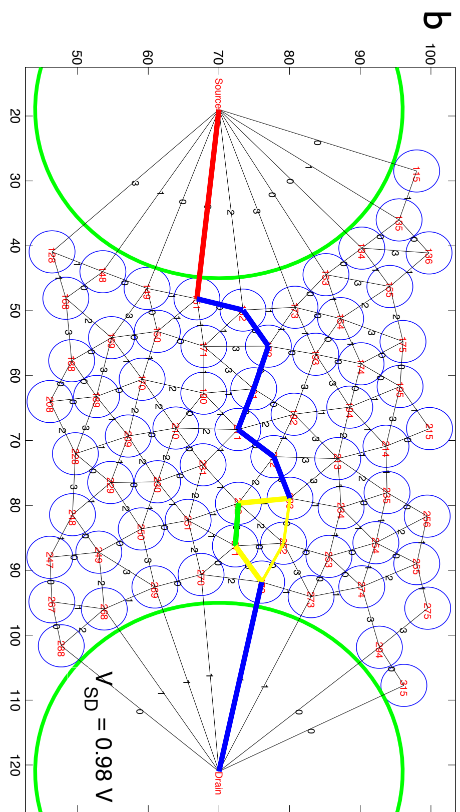
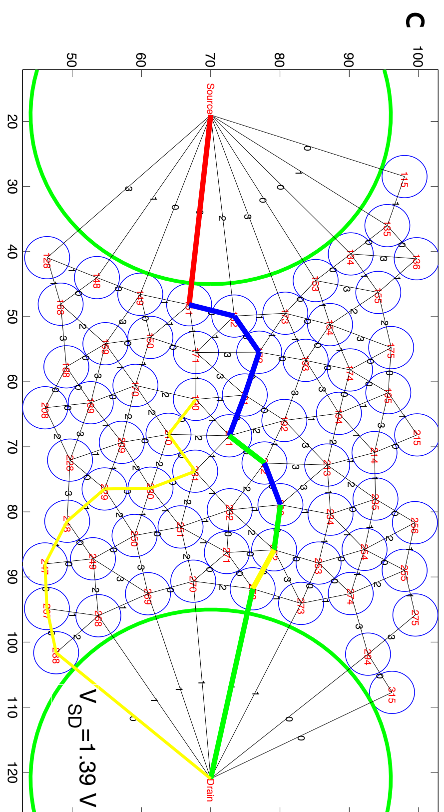
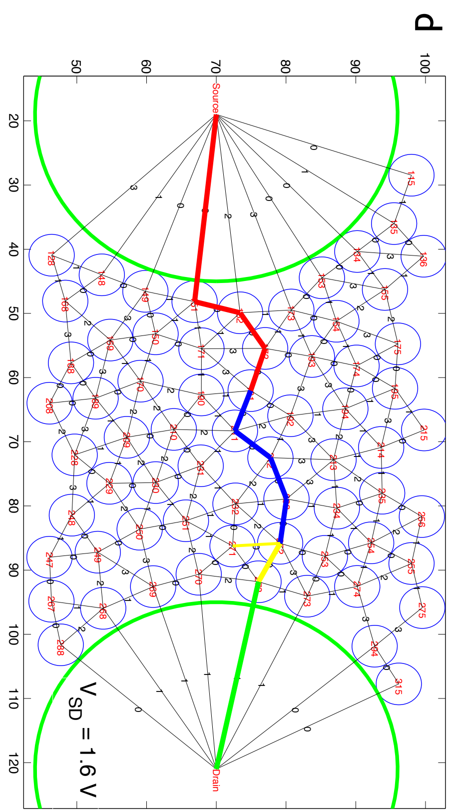
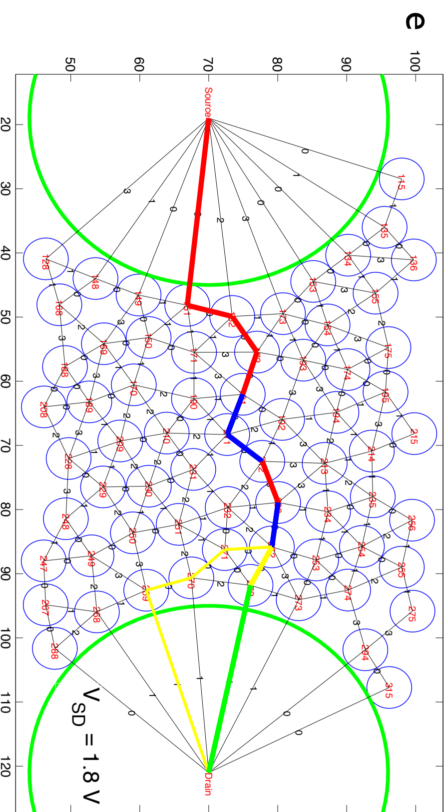


FIG. 5.1 Schematic of a disordered 2D device consisting of 67 uniformly sized nano-islands, each with a radius of 2.5 nm, that are randomly positioned in a 2D plane between the source and the drain after having evolved through Monte Carlo cycles from a square grid. The nearest neighbor inter-island spacings range anywhere from ~1.5-5 nm. (a) DCP observed in the disordered 2D system at $T = 0$ K at $V_{SD} = 2$ V. [b-e (see next page)] As the V_{SD} varies from 0.98 V (b) to 1.8 V (e), the strength of the DCP varies but the DCP retains its dominant conducting nature and its position in the 2D array with the appearance and disappearance of a weaker conducting path (seen in yellow).


b
V_{SD} = 0.98 V


c
V_{SD}=1.39 V


d
V_{SD} = 1.6 V


e
V_{SD} = 1.8 V

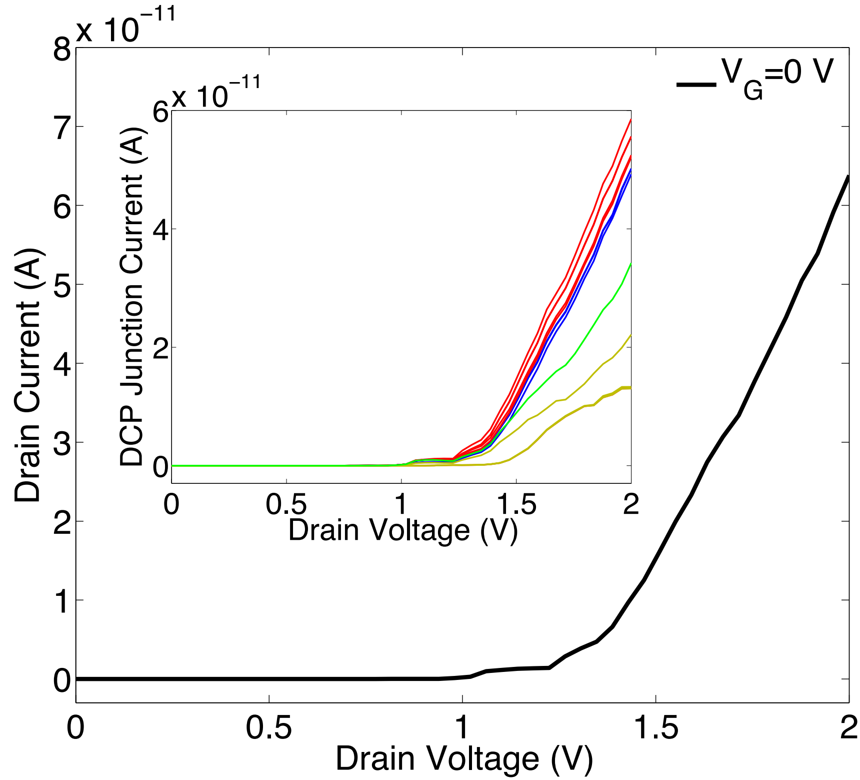


FIG. 5.2 *IV* characteristics of the 2D device shown in Fig. 5.1 at $T = 0$ K and $V_G = 0$ V. The device has a threshold voltage of ~1 V and exhibits a couple of small staircase steps in the neighborhood of the threshold region. In the inset, each curve shows the local current flowing through an individual junction that lies along the DCP. The different colors (as described above) indicate the amount of current, as a percentage of the total device current, being carried through the junction. The linear nature of the device behavior, constant device conductance and the DCP junction current values (in the inset) indicate the robust nature and the strength of the DCP.

raised to 1.6 V [Fig. 5.1(d)], the weaker path disappears, possibly breaking down into still weaker multiple paths, while the DCP strengthens especially in the region closer to the source. At $V_{SD} = 1.8\,\mathrm{V}$ [Fig. 5.1(e)], a different weaker path appears in the neighborhood of the drain carrying less than 40% of the device current. The same path along with the

DCP is observed when the bias is increased to a maximum of 2 V [Fig. 5.1(a)]. The observations do not show any consistent pattern with the weaker paths switching on and off as the bias is increased, but the DCP remains largely intact, although the current carrying strength of the DCP junctions varies. Thus, the device retains its quasi-1D nature with the majority of device current flowing through the DCP as V_{SD} is increased.

The MITS-simulated device current appears to be approximately an order of magnitude higher than that observed in the experimental device.[10] Such a large difference may be expected due to the differences in their structures and because of the smaller size of the simulated device array. Since we wanted to study the physics of the charge transport in 2D, which is not affected by the system size, and a bigger system requires longer simulation time, a smaller system was selected for the simulation study. But to make more quantitative comparisons between the characteristics of an experimental and a simulated device, and to draw the right conclusions from those comparisons, it would be appropriate to simulate a device approximately of a similar size.

5.2. Effect of Gate Bias V_G and Temperature T on the Device Characteristics

5.2.1 Effect of V_G on the Device Characteristics

After having demonstrated the existence of a DCP and having investigated the strength of the DCP, we further study the effect of gate bias and temperature on the DCP and the device characteristics. For the usability of a single electron device as a transistor, the study of gate and thermal effects is very important. A device with a robust DCP may

be better suited for room temperature applications.

The *IV* characteristics of the device at T = 0 K under the influence of gate potential V_G are shown in Fig. 5.3. As explained earlier in the chapter, the asymmetrical side gate is laterally placed above the active device region at a distance of 100 nm from the top edge of the device spanning the longitudinal length of the island array between the source and the drain. In order to study the effects of gate modulation on the device current and the V_{th}, the gate bias V_G is varied in increments of 2 V from -6 to +6 V. Our hypothesis was that a gate electrode placed on only one side of the device conduction

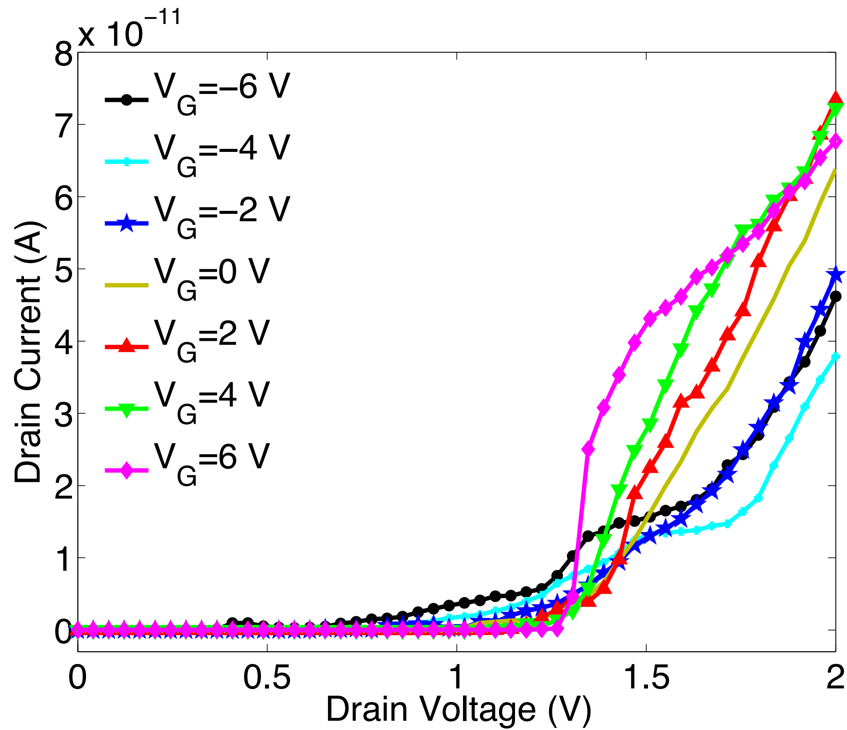


FIG. 5.3. Effect of laterally placed gate bias V_G on the *IV* characteristics of the device. An increase in V_G from -6 V to 4 V increases the Coulomb blockade and the device V_{th}. A further increase in V_G decreases the blockade showing a non-monotonic variation of $V_{th}(V_G)$.

channel (asymmetrical) might be able to move the DCP under sufficiently high gate bias. It is observed that at $V_G = -6$ V the threshold voltage V_{th} is ~ 0.3 V. As V_G is increased the Coulomb blockade increases, thereby increasing V_{th} to a value of ~1.1 V at $V_G = 4$ V. For $V_G = 6$ V, V_{th} appears to be ~1.2 V, but a closer examination demonstrates that the blockade actually decreased to V_{th} ~ 0.75 V. There is a small current flowing through the device between 0.75-1.2 V. The decrease in the blockade and V_{th} may be linked to the weakening of the DCP path shown in Fig. 5.4. and opening of new additional weaker paths. The non-monotonic nature of the variation of absolute blockade and device V_{th} with the increasing gate bias V_G is similar to the $V_{th}(V_G)$ variation observed in the single-island system study in Chapter 4. This observation suggests that the Coulomb blockade shifts with increasing V_G with perhaps one particular junction in the DCP determining the threshold point. At $V_G = 6$ V, when the V_{th} suddenly decreases, a different junction may determine the device V_{th}. A detailed investigation is required to draw any concrete conclusions from such behaviors in 1D and 2D systems, and is left for future studies. Besides modulating V_{th}, the gate bias has an appreciable effect on the device current itself. As V_G is increased from -6 to -4 V, the increase in the blockade appears to shift the *IV* curve towards higher V_{SD} values. But as V_G is increased further from -4 to 0 V, despite the increase in the blockade, the *IV* characteristics shift towards smaller V_{SD} values indicating an increased device conductance for a given V_{SD}. The device current increases sharply after the device has overcome the Coulomb blockade. The change in the

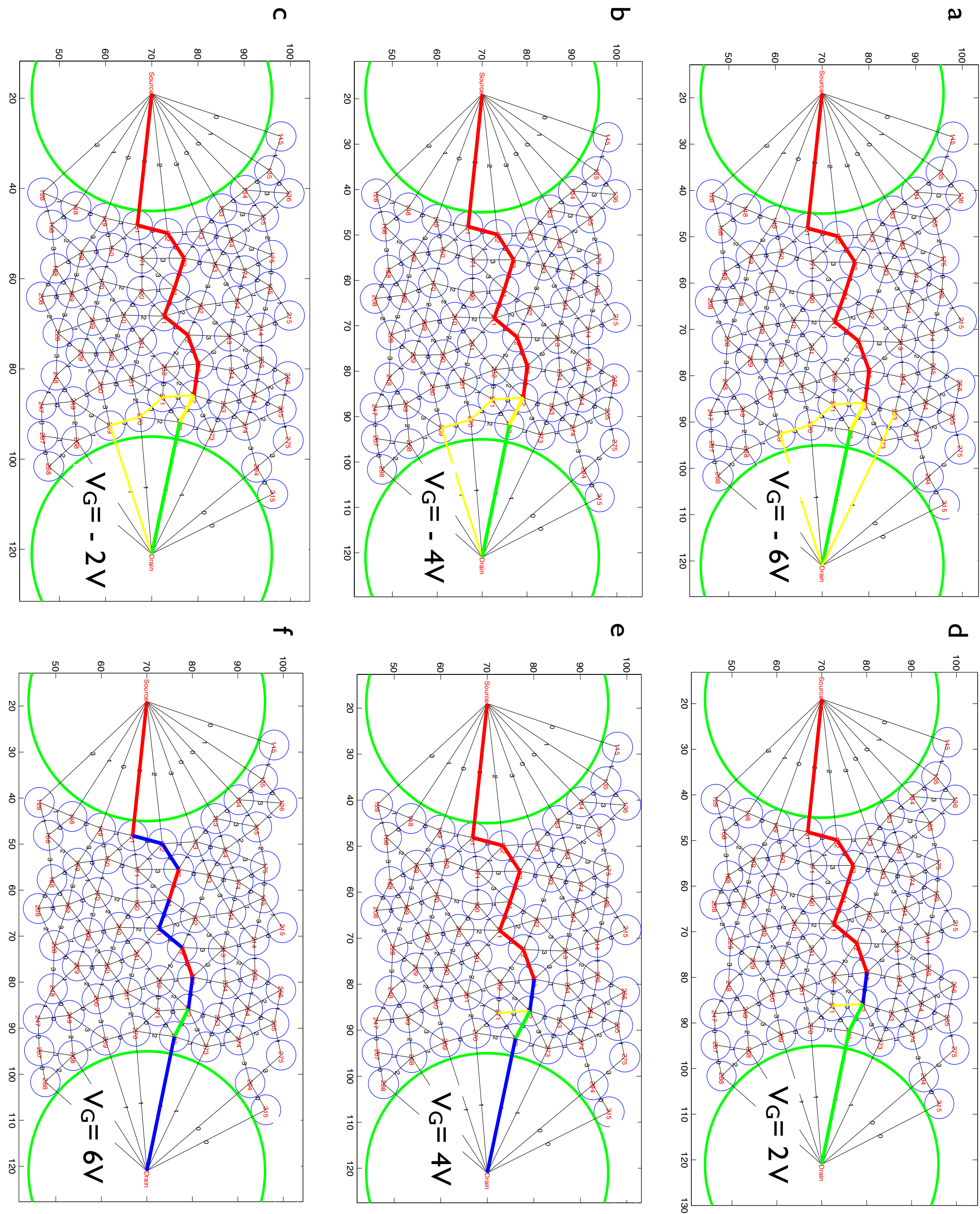


FIG. 5.4. Schematic 2D device geometries showing a DCP in the device at V_{SD}=2 V for different bias values of an asymmetrical side gate placed laterally at 100 nm from the top edge of the device. As V_G increases from -6 V to +6 V, the DCP begins to weaken at the source end while gaining the strength at the drain end. The lower strength of the DCP for V_G = 6 V indicates possible opening of additional weaker paths carrying the device current.

device behavior as V_G crosses -2 V could be linked to the change in the nature of the DCP with the increasing V_G (Fig. 5.4). The figure shows that the DCP at $V_{SD} = 2$ V is strong and robust as V_G increases from -6 to -2 V [Fig. 5.4(a-c)] although it breaks down into multiple paths as it approaches the drain. Nothing substantially changes in the DCP with the DCP still carrying more than 80% of the total device current. But when V_G increses from -2 to 0 V [Fig. 5.4(c) and Fig. 5.1(a)], the currents through a couple of DCP junctions decrease below 80% thereby lowering the DCP strength. This could be the reason behind the change in device behavior (Fig. 5.3) when V_G increses from -2 to 0 V. As the gate bias is increased further towards 6 V [Fig. 5.4(f)], the DCP strengthens at the drain end but begins to weaken near the source terminal, indicating that there are likely additional weaker conducting paths carrying a larger fraction of the device current.

We believe that the gate modulation effects on V_{th} and the device current strongly depend on multiple factors such as the device structure, the amount of disorder, the strength of the DCP, and the position of the gate relative to the tunneling junctions. The investigation indicates that a fairly uniform 2D device with negligible disorder may show stronger gate modulation effects where the multiple conduction paths might be more sensitive to the gate bias.

5.2.2 Effect of Temperature T on the Device Characteristics

The device IV characteristics for the temperature T ranging from 0 - 40 K are shown in Fig. 5.5. At higher temperatures, since a large number of time steps are required for the device current to reach a steady state with satisfactory statistical accuracy, the

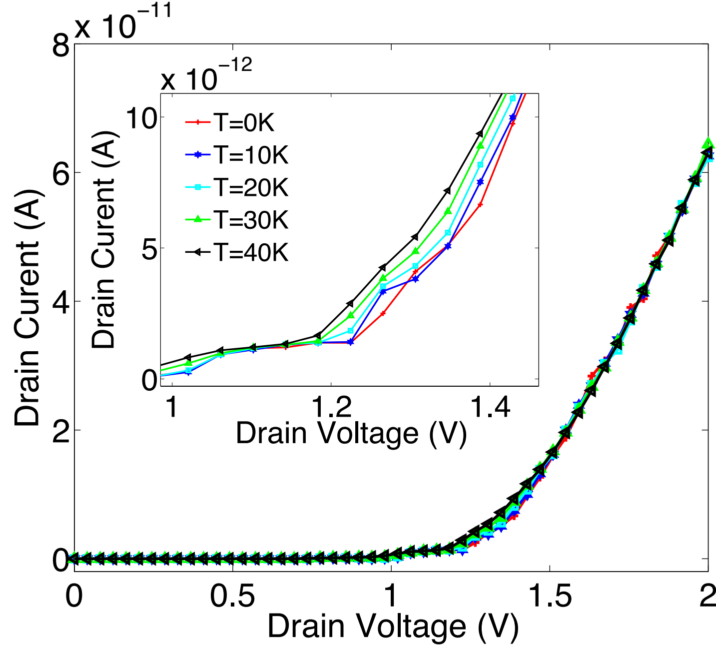


FIG. 5.5 *IV* characteristics of a 2D device at different *T* showing the temperature effects on the *IV*. The temperature has no appreciable effect on the device conductance. The inset shows the shifting of the *IV* characteristics with the increasing *T* that appears to be the sign of decrease in the blockade and the V_{th}.

study was restricted to temperatures up to 40 K. The inset shows the device characteristics at small bias values in the threshold region after the device has overcome the blockade. The DCP paths at two different temperatures, T = 0 K and T = 40 K, are shown in Fig. 5.6. It is observed that the increase in T up to 40 K practically has no effect on the DCP in the device, although it may affect the weaker paths if they exist. Taking into account the junction charging energy range of 0.2-0.5 eV, we believe that 40 K may not be a sufficiently high temperature to observe any major thermal effects on the device characteristics, especially a change in the DCP. Since the DCP does not change, there is no significant change in the device current at T = 40 K at high bias. It will be interesting to investigate in the future work the device characteristics at higher temperatures

going up to ~250K to explore the possibility of observing the negative temperature coefficient of resistance at higher biases observed in the experimental device consisting of tungsten nano-islands in a 2D system.[6, 7, 9]

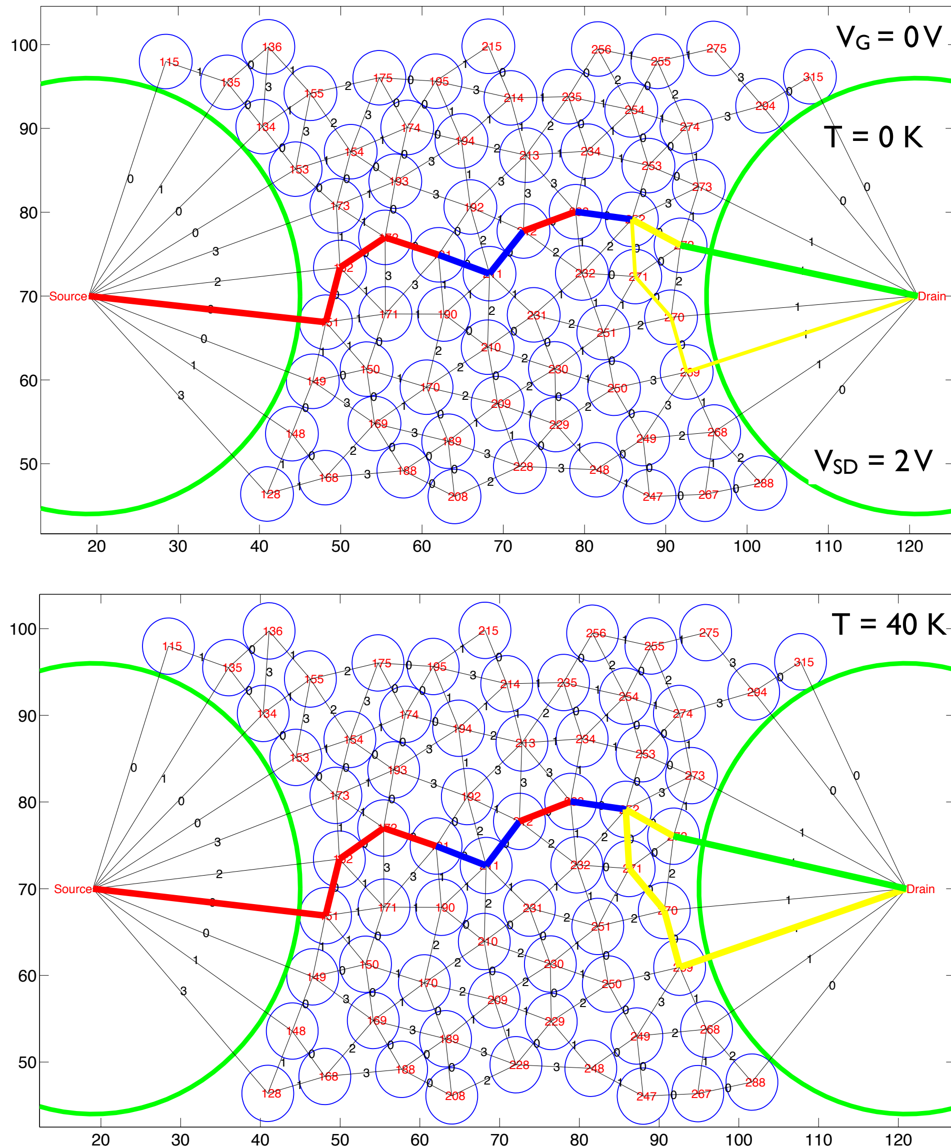


FIG. 5.6 The DCP in the device shown at two different temperatures $T = 0$ K and $T = 40$ K. The 40K rise in temperature does not have any effect on the DCP thereby keeping the device conductance unaffected.

The device current can increase with the increase in T by two possible mechanisms.[8] One, the temperature must be increased to a sufficiently high value to cause thermionic emission from the island that can contribute to the device current. Even if the device characteristics were to be probed at higher T (~250-300 K), the thermionic emission phenomenon is highly unlikely in this particular system since the tunneling barrier height of ~1.4 eV between any two islands is very large compared to a thermal energy of 25 meV at T = 300 K. Also, for the device current to be dominated by thermionic emission current over the tunneling current, the inter-island separations have to be sufficiently large so that the tunneling current is reduced to a negligible value compared to the thermionic current by the large junction widths.[8] The experimental devices[6, 7, 9] do not appear to have such device structures with larger junction widths. Therefore, we believe that the thermionic emission mechanism may not be responsible for the increase in device current with the increasing temperature that is observed in the experimental devices.[6, 7, 9]

In the other mechanism, which is more likely to occur in disordered 2D systems, an increase in temperature may have a two-fold effect. First, an increase in temperature decreases the device V_{th} either in a linear or a non-linear manner similar to what we have observed in 1D systems. Increasing temperature may remove the non-linear Coulomb blockade behavior of the tunneling junction between the two islands thereby linearizing the junction, as proposed by Parthasarathy, *et al.*[10] As the temperature increases, a larger number of junctions in the optimal path are linearized. At a system dependent critical temperature, the fraction of the total number of junctions that is linearized approaches the percolation threshold forming a continuous path of a percolating sub

network of linearized junctions that bridges the source and the drain.[10] With the linearization of every single tunneling junction in the optimal path, the device threshold decreases and reaches 0 V when the percolation threshold is reached.

If the temperature is increased beyond the critical value, the carrier density is thermally activated[8] and the low bias device conductance follows either an Arrhenius or non-Arrhenius behavior with a system dependent characteristic energy.[6, 7, 10, 19] The nature of the behavior depend on the amount of disorder in the system, especially the distribution in the island sizes and the distribution in charging energies.[6, 7, 19, 20] It has been observed that for a system that consists of fairly uniform nano-islands, the low bias device conductance follows an Arrhenius behavior ($\ln(G) \propto T^{-1}$).[10] While in a system consisting of fairly large dispersion in island sizes, the device conductance shows a characteristic non-Arrhenius behavior ($\ln(G) \propto T^{-0.5}$).[6,19] Muller and Yajadda[19] propose that in a highly disordered system with a large distribution in tunneling widths and charging energies, the electrons select different percolation paths at different temperatures that lead to an enhanced conductance in the device at higher temperatures and lower biases. We believe that a change in the percolation path or opening up of additional conducting paths with increased T may lead to increase in the device conductance at higher biases as well. The change in the percolation path or opening up of additional conducting paths may be one of the reasons behind the increase in current with the increasing T observed by Cheam.[9]

In the device characteristics shown in Fig. 5.5, it is observed that with the increase in temperature, the Coulomb blockade decreases, thereby decreasing the V_{th}. This

behavior is similar to the $V_{th}(T)$ behavior that was observed in 1D systems and the behavior observed in 2D systems studied by Parthasarathy, *et al.*[10] In the low bias regime, there is no appreciable change in the device conductance with the increasing temperature. The IV curves appear to be shifting towards lower V_{SD} values due to the decrease in V_{th}. Further investigations may give an insight into relation between exact mechanism of transport in such disordered systems of nano-islands and the system disorder, and the different regimes under which the various transport mechanisms[8, 10, 19, 20] dominate the charge transport.

5.3 *IV* Characteristics of a 1D Device made of the DCP Junctions and Islands

5.3.1 Effect of Gate

After having demonstrated the existence of a DCP in a disordered system that was hypothesized by Cordan, *et al.*[1], we next study the properties of a quasi-1D device that consists of only those junctions and islands that exists in the DCP. The device consists of 10 junctions and 9 identically sized islands of radius 2.5 nm. The junction width varies from ~1.6–2.1 nm (as compared to ~1.5–5 nm in the parent 2D system) with a mean and standard deviation of $\sim 1.75 \pm 0.17$ nm. As the DCP is formed along an optimal path consisting of narrower junctions, it is noted that the mean and the standard deviation of the junction widths in 1D is considerably less than 2.7 ± 1.0 nm in the parent 2D system. All the capacitance values of the junctions and the islands are taken from the parent 2D device. The inter-island capacitances lie in a range between $\sim 7\times10^{-20} - 9\times10^{-20}$ F. The

island self-capacitances range from $\sim 0.6\times10^{-20} - 1\times10^{-20}$ F, while the gate capacitances range from $\sim 0.2\times10^{-20} - 0.34\times10^{-20}$ F. Since the DCP is made of narrower junctions, we observe that the distribution of capacitances is narrower in the quasi-1D device relative to the parent 2D device. The self- and gate-capacitances in the quasi-1D device are at the lower end of the range in the parent 2D device while the inter-island capacitances are observed to be at the upper end of the parent 2D range. For quasi-1D simulations, all the non-DCP islands are removed from the 2D device, although the capacitances of the DCP islands and the DCP junctions in the parent 2D device are retained in the quasi-1D

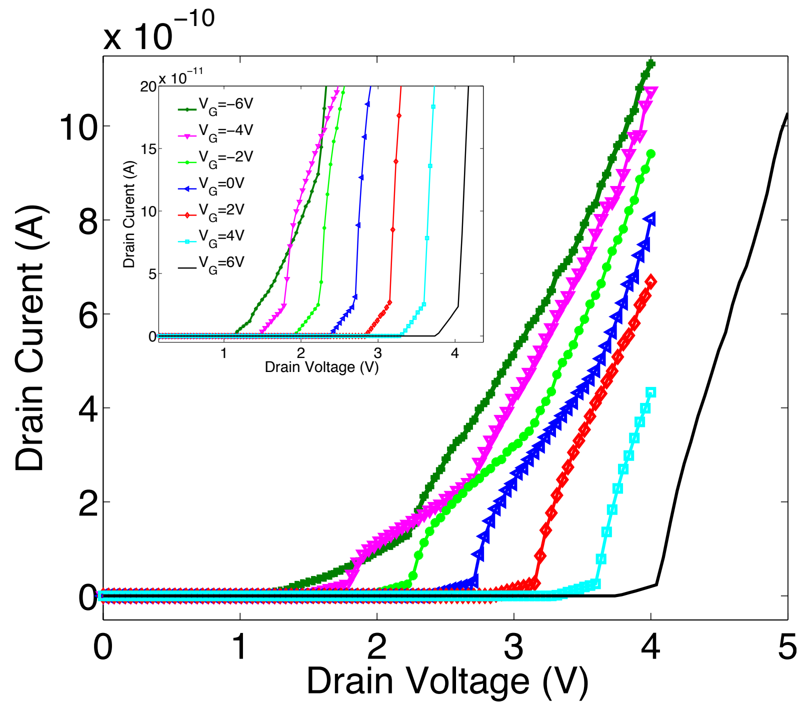


FIG. 5.7 The *IV* characteristics of a 1D device made of only those junctions and islands that are present in the DCP, and the effect of gate on the *IV*. The gate bias V_G modulates the blockade and V_{th}. With the increasing V_G, blockade and V_{th} increase without an appreciable change in the device conductance. DCP junction- and island- capacitance values are retained from the parent 2D system.

device. For an accurate study of the effects of non-participating islands on the device characteristics, further investigations are underway wherein the DCP island- and junction-capacitances in the quasi-1D device are calculated independently. These capacitance values may lower the Coulomb blockade and V_{th} from that observed in Fig. 5.7 but may not have any major impact on the device conductance and the nearly linear *IV* behavior beyond the blockade region.

The device characteristics for the 1D chain under the influence of the varying gate voltage are shown in Fig. 5.7. We observe that the device threshold voltage V_{th} at $V_G = 0$ increases appreciably from ~1 V in the parent 2D system to ~2.5 V in the quasi-1D device. The neighboring islands in the parent 2D system shield the DCP islands. As a result, we expect the junction charging energy of each junction in the DCP to decrease in the 2D plane. Therefore V_{th} in the parent 2D device is smaller than that of the quasi-1D device. Once the device enters the conducting state, despite its linear behavior similar to that of the parent 2D device, the device conductance in the quasi-1D system away from the threshold is observed to be approximately 10 times the device conductance of the parent 2D system. The dominant factor responsible for smaller conductance in 2D could be the charges that are present on the neighboring islands around the DCP. These charged neighboring islands might inhibit the propagation of charge flow along the DCP necessitating increased bias voltage. We also observe that for the case studied here, the quasi-1D device does not exhibit any staircase structure. Since the quasi-1D islands have a narrower distribution of self-capacitances and the DCP junctions have a narrower distribution in junction widths, we expect the quasi-1D system to behave very similar to a single-island device consisting of two uniform junctions. We have already

concluded from observations on the single-island system in Chapter 4 that when the system waits for the RLS transition to take place, if an additional conduction channel does not open in the charge state space, the device will not exhibit any staircase structure. Similar phenomenon is likely to occur in the 1D system having uniformly sized islands with a narrow distribution in self-capacitances and junctions having a relatively narrow distribution of junction widths.

Gate modulation effects are more prominent in the quasi-1D device consisting of the DCP than those taking place in the parent 2D device. As the gate is varied in increments of 2 V from -6 to 6 V, V_{th} increases similarly to that in the 2D structure, and the $V_{th}(V_G)$ variation appears to be smooth and linear in nature (inset in Fig. 5.7). The smooth variation is due to the small degree of disorder in the quasi-1D chain. Although it is not clear from Fig. 5.7 whether the blockade and the V_{th} shift or increase with the increasing V_G, it would be interesting to investigate whether the variation is similar to the $V_{th}(V_G)$ variation observed by Lee, *et al.*[21] In their observations on a quasi-1D chain of gold nano-islands deposited on boron nitride nano tubes, the $V_{th}(V_G)$ variation appears to be smooth and linear accompanied by a change in the blockade and the V_{th} with the change in V_G. We expect the device blockade and the V_{th} to decrease with the increasing V_G beyond a system-dependent critical V_G value, similar to what was observed in the 2D system as well as in the single-island system described in Chapter 4. The critical gate-voltage value in a quasi-1D chain may be larger than that in the 2D and the asymmetric single-island system (Chapter 4) due to the narrower distribution in the capacitances in the quasi-1D chain. That would increase the gate bias range within which the

device shows smooth gate modulation effects on V_{th}, and that could be utilized for transistor switching action in practical devices. Furthermore, as discussed in the previous paragraph, such a 1D chain with a small distribution in junction widths, and uniformly sized islands with a narrow distribution in self-capacitances is expected to behave similarly to a single-island system but with a larger effective charging energy for the whole system. When the device enters the conducting state, the gate does not have an appreciable effect on the device conductance. This is expected in a fairly uniform 1D chain where the chances of having a staircase structure are negligible and there is only one path for the charge to flow between the source and the drain.

5.3.2 Effect of Temperature

Figure 5.8 shows the effects of temperature on the characteristics of the quasi-1D device consisting of the islands and the tunneling junctions in the DCP. In the quasi-1D chain, a step-like feature observed at $T = 0$ K in the device characteristics in the threshold region (at V_{SD} ~2.5-3.5 V) exists even at temperatures up to 240 K. This feature is not observed in the 2D device characteristics, even at $T = 0$ K where the current increase is smooth and linear when the device enters the conducting state above V_{th}. Away from the threshold at larger biases, the temperature has practically no effect on the device conductance. It is observed that the *IV* curves appear to shift towards lower V_{SD} values because of the decrease in the blockade and the apparent V_{th} with increasing T. The device blockade and the V_{th} decrease smoothly with increasing T (inset in Fig. 5.8).

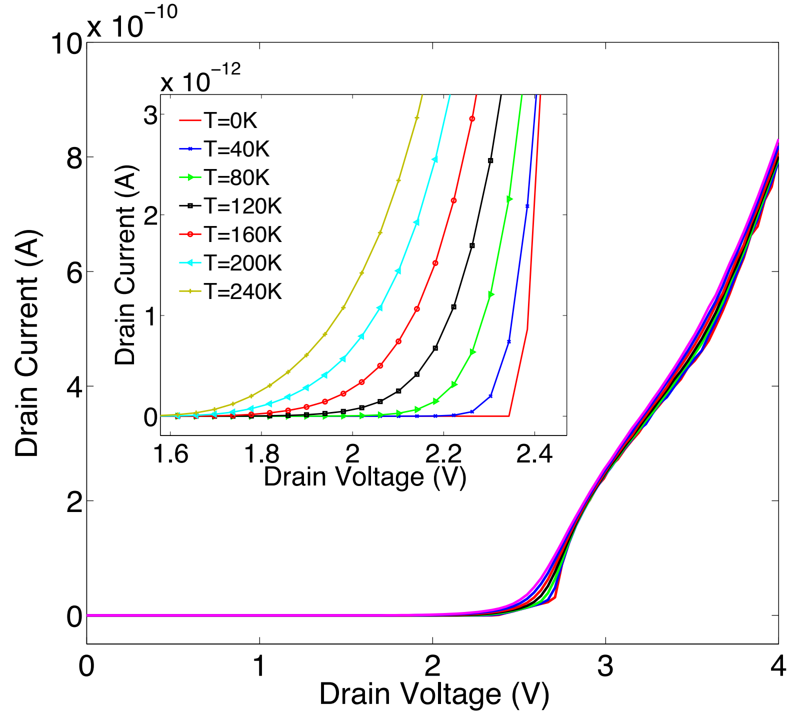


FIG. 5.8 The *IV* characteristics of a 1D device made of only those junctions and islands that are present in the DCP and the effect of temperature T on the *IV*. At large source-drain bias V_{SD}, T has no effect on the device conductance, which indicates that the charge transport is by tunneling. At small V_{SD} (inset), the blockade and V_{th} decrease with the increasing T. The noticeable feature is the apparent translational shift observed in the *IV* characteristics as the T is increased, similar to the experimental observations made by Parthasarathy, *et al.*[10].

A thorough data analysis may reveal the nature of the variation of V_{th} with temperature and the power law *IV* behavior in the quasi-1D chain consisting of the DCP junctions and the islands. Since the disorder in such a chain is small leading to a narrow distribution in junction charging energies, the $V_{th}(T)$ variation may follow a linear behavior similar to the observations made by Parthasarathy, *et al.*[10] At higher temperatures the chances of the device having an absolute blockade are small since an exponentially suppressed current flows through the device. However, the region below the apparent blockade is

clearly distinguishable from the region above the apparent blockade. The inset in Fig. 5.8 shows that as T increases, the IV characteristics that exhibit sharp features at lower T are softened near the apparent threshold point. The most noticeable feature is the translational shift observed in the IV characteristics as the temperature is increased when the device enters the conducting state (inset in Fig. 5.8). Similar observations have been made by Parthasarathy, *et al.*[10] on large 2D arrays of Au nano islands at modestly smaller energy scales. Their observations show that the IV characteristics at different temperatures collapse together when translated by a voltage scale equal to their respective V_{th}. The device resistance in their devices does not change with the changing temperature, and the IV follows a power-law behavior with an exponent of ~2.2. The device characteristics retain their non-linear behavior observed at lower temperatures up to significantly higher values of ~130 K. The self-assembled chains of graphitized carbon nanoparticles ~ 1.2 μm long[4] also appear to show similar behavior up to 72 K with the characteristics shifted by a voltage scale equal to V_{th} at those respective temperatures. In the devices studied by Black, *et al.*[6] increasing temperature rapidly softens any non-linearities that are present in the IV at smaller energy scales. When the critical temperature is reached, the device shows a linear behavior. They argue that small bias device conductance follows an Arrhenius behavior with the characteristic T^{-1} temperature dependence. The experimental devices fabricated by Quinn, *et al.*[7] also show similar temperature effects on the IV with the device conductance following an Arrhenius behavior in temperature. The characteristic activation energy depends on the capacitances in the system. Devices investigated by Cheam [9] show similar temperature effects but at much higher bias energy scales. It would be interesting to see if this model could

address the different device behaviors at higher temperatures that are observed at different energy scales. Further research focused on temperature effects on *IV* especially at lower energy scales might answer this critical question.

References

[1]A. S. Cordan, A. Goltzene, Y. Herve, M. Mejias, C. Vieu, and H. Launois, J. Appl. Phys. 84, 3756 (1998).

[2]A. S. Cordan, Y. Leroy, A. Goltzene, A. Pepin, C. Vieu, M. Mejias, and H. Launois, J. Appl. Phys. 87, 345 (2000).

[3]A. J. Rimberg, T. R. Ho, and J. Clarke, Phys. Rev. Lett. 74, 4714 (1995).

[4]A. Bezryadin, R. M. Westervelt, and M. Tinkham, Appl. Phys. Lett. 74, 2699 (1999).

[5]C. Kurdak, A. J. Rimberg, T. R. Ho, and J. Clarke, Phys. Rev. B 57, R6842 (1998).

[6]C. T. Black, C. B. Murray, R. L. Sandstrom, and S. H. Sun, Science 290, 1131 (2000).

[7]A. J. Quinn, M. Biancardo, L. Floyd, M. Belloni, P. R. Ashton, J. A. Preece, C. A. Bignozzi, and G. Redmond, J. Mater. Chem. 15, 4403 (2005).

[8]C. A. Neugebauer and M. B. Webb, J. Appl. Phys. 33, 74 (1962).

[9]D. D. Cheam, *Integration of Room Temperature Single Electron Transistor with CMOS Subsystem*, PhD dissertation, Michigan Technological University, Houghton, MI, 2009.

[10]R. Parthasarathy, X.-M. Lin, K. Elteto, T. F. Rosenbaum, and H. M. Jaeger, Phys. Rev. Lett. 92, 076801 (2004)

[11]A. A. Middleton and N. S. Wingreen, Phys. Rev. Lett. 71, 3198 (1993).

[12]R. Parthasarathy, X.-M. Lin, and H. M. Jaeger, Phys. Rev. Lett. 87, 186807 (2001).

[13]W. Y. Wang, T. Lee, and M. A. Reed, Phys. Rev. B 68, 035416 (2003).

[14]D. Banyai, M. A. Savaikar, P. L. Bergstrom, and J. A. Jaszczak, (to be published).

[15]N. F. Mott, Philosophical Magazine 22, 7 (1970).

[16]A. L. Efros and B. I. Shklovskii, J. Phys. C : Solid State Phys. 8, L49 (1975).

[17]D. Yu, C. J. Wang, B. L. Wehrenberg, and P. Guyot-Sionnest, Phys. Rev. Lett. 92, 216802 (2004).

[18]P. A. Lee, Phys. Rev. Lett. 53, 2042 (1984).

[19]K. H. Muller and M. M. A. Yajadda, J. Appl. Phys. 111, 123705 (2012).

[20]K. H. Muller, J. Herrmann, B. Raguse, G. Baxter, and T. Reda, Phys. Rev. B 66, 075417 (2002).

[21]C. H. Lee, S. Qin, M. A. Savaikar, J. Wang, B. Hao, D. Zhang, D. Banyai, J. A. Jaszczak, K. W. Clark, J.-C. Idrobo, A.-P. Li, and Y. K. Yap, Adv. Mater. 25, 4544 (2013).

Chapter 6: Conclusions and Future Work

Multi-island Transport Simulator (MITS) is a robust tool that can be used for modeling of one- and multi-dimensional physical systems of metallic nano-meter-sized islands that conduct by means of single-electron tunneling. The physical model employed, in conjunction with a capacitance solver, and the modeling of voltage-dependent tunneling resistances, advances its capabilities beyond those of existing circuit-model simulators, and allows for the investigation of numerous effects such as the spatial disorder of the islands, size distribution of the islands, and source-drain-gate geometries on device characteristics. Unlike in other simulators, MITS has the capability to elucidate key linkages between the physical characteristics of the system and the resulting device characteristics, such as the Coulomb blockade and Coulomb staircase structures. MITS also provides microscopic details that may give insights into the complex interplay among those factors that affect the tunneling rates that are fixed *a priori* (island sizes, island separations, temperature, gate bias, etc.), and the evolving charge state of the system, which changes as a function of the applied source-drain bias and temperature.

Devices of various geometries can be explored to investigate the influence of external factors such as gate bias on the device characteristics, especially in multi-dimensional structures, to study the gate-dependent properties such as Coulomb oscillations, and temperature-dependent properties such as current on/off ratio. In addition, different models of tunneling can be incorporated. For example, using a simple model for the effects of tunneling barrier suppression due to applied biases and charging

effects has allowed for detailed investigation of a 1D system under reasonably high bias conditions where barrier suppression cannot be ignored. The structure of the simulation tool is flexible enough to be able to incorporate refined tunneling models based, for example, on electronic structure calculations specific to materials in a device, more accurate models of the tunneling barriers, or the effects of finite tunneling times as proposed by Korotkov and Nazarov[1] and Nazarov.[2] MITS should be a valuable tool for predictive modeling of prospective devices and for investigating different device geometries to aid in the design and control of device characteristics.

Since the overall 1D device resistance predominantly depends on the wider junctions, and the larger charging energies are associated with the smaller islands, we conclude that in case of 1D structures, those with smaller island sizes and narrower junctions may be better suited for practical applications, especially at room temperature. Devices that consist of smaller islands and narrower junctions are expected to have larger blockade and larger on/off current ratio. Although it is difficult to analytically predict the number of up-steps in a disordered percolating chain, especially wherein the islands are capacitively coupled, the linear behavior of V_{th} as a function of N, even for disordered systems, suggests that longer chain lengths are more suitable for practical applications because of their larger Coulomb blockades and more pronounced staircase structures. Longer 1D-chain devices can also withstand higher temperatures, as they can exhibit Coulomb staircases despite the decrease in V_{th} with increasing temperature. On the other hand, the shorter chains having low V_{th} value have an advantage over longer chains in low power switching applications. With a better control on the fabrication process, it might be possible to switch on the device at a desired source-drain bias without

using a gate electrode. This has been recently demonstrated by Lee, *et al*.[3] wherein the device switch on voltage is modulated by changing the position of the source electrode on a chain of gold nano-islands deposited on boron nitride nanotubes. The likely presence of defects in the experimental devices, due to the limited control on the fabrication process, could result in the experimental devices having larger blockade and larger V_{th} than of those having no defects. Because of the dependence of overall device current on the wider junctions in a long 1D chain, it might be possible to fabricate devices that conduct desired amount of current by artificially etching away specific islands in the chain thereby creating wider junctions. After studying the *IV* power-law behavior, we conclude that in a disordered-chain device operated especially at higher bias energies, it is difficult to predict the device current due to the apparent change in the exponent of the power law behavior with the change in applied bias. To predict the device current, either the device has to be operated at small energy scales or the chain structure has to be uniform so that the power remains fairly constant over a wider bias range. Further investigations are required to ascertain the exact mechanism behind the change of exponent in the power law behavior especially at higher biases and the effects of disorder in the chain on the exponent, in relation to the work in Refs. 4-7.

From the studies done on disordered single-island and 1D-chain devices, we infer that although the *IV* characteristic is symmetric about $V_{SD} = 0$ V in a device with $\lambda \rightarrow 0$ and grounded source, the polarity of the net charge on the charged islands changes with the change in polarity of the drain. The charge transport mechanisms for the two opposite polarities of the drain with grounded source are similar to electron and hole conduction mechanisms in semiconductor devices. Furthermore, a disordered 1D device with

$\lambda \rightarrow 0$, upon exchanging the two electrodes would behave as a different device producing different *IV* characteristics altogether. The exchange of the two electrodes in a disordered 1D device having large λ is likely to produce the same *IV* characteristics. This feature may also be expected in a uniform chain with $\lambda \rightarrow 0$.

In a single-island device whose physical features are well characterized, it is possible to predict the device characteristics by analytically estimating the device current along with V_{th}, the step positions and the height of the steps. For a single-island device to exhibit a staircase structure, a large difference between the two junction transition rates is an essential but not a sufficient condition. It is not enough for the junctions to be asymmetric which may produce a Coulomb blockade but may not produce a staircase structure even if the rates are largely different. The position of the current-limiting junction with respect to biased electrode determines if the device exhibits a staircase structure in its *IV* characteristics. For practical applications, the effects of a gate bias on device behavior are of great importance. In a single-island device, the gate bias shifts the Coulomb blockade and produces *IV* characteristics that are asymmetric about $V_{SD} = 0$. But the range of V_G and V_{SD} in which the blockade and V_{th} shift is limited and well defined by the capacitances in the system, beyond which the blockade and V_{th} decreases with the increasing V_G. After observing similar features in 1D chains and 2D systems, we conclude that the way a gate modulates the device behavior in single-electron devices is different from that of the conventional field effect transistors wherein the gate controls the device behavior by controlling the inversion layer width. Furthermore, for fixed V_{SD} the current in a single-island device shows sharp periodic oscillations as a function of the gate bias whose period is characterized by the gate capacitance. The presence of any

background charge shifts the peaks, which is likely to be observed in experimental devices when tested under different environmental conditions. An increase in temperature does not affect the period of the oscillations in a simulated device, but increases the peak width and decreases the current on/off ratio. However, in a real device increase in the device temperature may shift the peaks if the materials used in the device thermally expand.

After having understood in detail the physical mechanism behind the staircase structure, we conclude that the disordered 1D multi-island chains are always expected to show staircase structures, especially at low V_{SD} and lower temperatures. This is possible due to the large distribution in tunneling transition rates across different junctions in the device. The steps of the staircase are non-uniform with different widths and heights and are difficult to predict. Since the energy required to overcome each up-step is distributed over a large range, it is equally difficult to predict the blockade and V_{th} of a 1D chain device. By devising some smarter methods, it might be possible to engineer the step widths by selective etching of the islands from the fabricated 1D chain device. Like disordered systems, a uniform 1D chain device may also exhibit a staircase structure provided $\lambda \to 0$. In a disordered 1D chain, when the device exhibits a staircase structure at low V_{SD}, one particular junction having the smallest transition rate controls the overall device current, and this junction may change from one staircase step to another. The important observation, that it is the rate limiting process that ultimately leads to the staircase structure in the device characteristics which can be analytically predicted in a single-island system but is unpredictable in a 1D chain device, and establishing the linkage between the device *IV* characteristics and the physical device

features are the main highlights of this dissertation research. Multi-island devices may be expected to show irregularly spaced gate oscillations either due to the disorder in the chain or due to the varying gate influence on the islands. Further research is required to investigate the influence of the gate on the transition rates for a given V_{SD}, that is expected to modulate the blockade and possibly the device current.

The thermal studies done on 1D chain devices demonstrate that temperature has no effect on the device characteristics at higher bias in the asymptotic region. This is expected because the tunneling barrier heights of the typical materials such as tungsten and gold that are used in the devices are large compared to the typical temperature range at which the devices are operated. The increasing temperature decreases the device blockade and the device threshold voltage in either a linear or a non-linear manner. Longer 1D chains may show more prominent non-linear behavior of $V_{th}(T)$. It may be difficult to predict, a *priori*, the number of up-steps and their heights in a device having strong inter-island coupling because of the disorder, and predominantly because the propagating charge front and the change in the charge state modulates the potential drops across the junctions in the device. We believe the system is expected to traverse along different paths in the charge-state-V_{SD} space at different temperatures, and the percolation model proposed by Parthasarathy, *et al.*[7] may have limitations in explaining the $V_{th}(T)$ behavior in devices having strong inter-island coupling especially in disordered 1D chains. Further investigations are underway to study the effects of temperature on the microscopic charge states of the system and the resulting decrease in V_{th} with increasing temperature. But the task may not be easy because of the thermal vibrations in the system that lead to increased possibilities of multiple transitions in the system at any

given bias.

A multi-dimensional device with a sufficient disorder may be expected to behave as a quasi-one-dimensional device exhibiting a single dominant conducting path that carries a majority of the device current. This feature is likely to be observed in experimental devices due to the inherent disorder in such systems unless fairly uniform structures are fabricated using special fabrication methods. Devices having a robust DCP may retain their quasi-1D nature even under varying V_{SD}, V_{G}, or temperature conditions. From an experimental perspective, it would be interesting to fabricate a quasi-1D device made of only the DCP junctions and the DCP islands by etching away the remaining islands in the device plane. Such a device is expected to consist of narrower junctions and larger islands that have a minimum distribution in junction widths and island sizes. The quasi-1D device may have a larger blockade and V_{th}, and may also conduct marginally higher current. But such a device is unlikely to exhibit prominent staircase structure due to the narrow distribution in junction widths and island sizes. The studies conclude that the gate modulation effects in quasi-1D devices are highly smoother than those in 2D devices. Therefore, the quasi-1D structures that are fabricated by etching away the remaining islands from multi-dimensional structures could be a preferred choice over multi-dimensional device structures for transistor operations. Although not investigated here, MITS has the capability of simulating device characteristics as a function of gate bias for different gate geometries.

From the thermal studies performed on a quasi-1D device that has minimum distribution in junction widths, we conclude that in a disordered 2D system that has a robust DCP, the decrease in V_{th} with the increasing temperature is expected to shift

the IV towards lower V_{SD} without any appreciable change in the high bias device conductance. Further increase in temperature, after the threshold voltage has reached zero with the increasing temperature, may lead to an increase in the low bias device conductance due to the thermal activation of charge carrier density. In multi-dimensional devices having bigger islands, larger source-drain bias and higher temperature may also open up additional conducting paths that can increase the high bias device conductance with the increase in temperature. Increase in temperature may also change the DCP. Increase in the number of paths and the change in the DCP with the increase in temperature could be one of the reasons that is responsible for driving higher device current at higher temperatures as has been observed by Cheam.[8] In nearly uniform two-dimensional devices, the Coulomb staircases are likely to be washed out even at $T = 0$ K, as the current is expected to be carried by multiple paths between the source and the drain with each path having a minimum distribution in junction widths and island sizes. These multiple paths would collectively diminish any staircase effects that any one path might exhibit.

There are unlimited opportunities that MITS provide for future work in exploring different aspects of single-electron-device characteristics. Devices with different values of λ should be investigated to study how exactly the self-capacitances and hence the island sizes affect the number of up-steps before the device reaches the threshold. In spite of an unpredictable increase in the number of up-steps with the increasing chain length, and the large distribution in the energy that is required to overcome all of the up-steps up to V_{th}, why does the V_{th} vary linearly with increasing chain length, especially in strongly-coupled-island devices, still remains an open question. In-depth studies are

required to answer that question and probe the limitations of the percolation model proposed by Middleton and Wingreen[6] and Parthasarathy, *et al*.[7] Although our studies on the power law behavior appear to resolve the discrepancies in the exponents predicted by theory[6] as compared to those observed in the experimental work,[7,9] further research is needed to study the effect of chain disorder and the higher bias on the power law behavior. This could be addressed by implementing more refined tunneling models in MITS as discussed earlier.

A systematic study of gate effects is desired if the devices are to be used for transistor applications. The study should probe the effects of gate on the junction charging energies and junction transition rates that modulate the threshold and the device conductance. MITS could be a significant resource to explore the 2D devices especially to study the effect of disorder on the device characteristics. Further studies on different devices of varying disorder may probe the relationship of the structural disorder with the strength of the DCP. Device structures having different particle densities can be made to evolve from different initial grids such as a square grid, a close-packed triangular grid and other different shapes. Different grids will generate device configurations with varying degrees of disorder. Future 1D- and 2D-device studies could further probe and answer some of the most relevant questions that are posed by the experimental works such as the shifting of *IV* without any change in device conductance with the increase in temperature,[7] the change in device conductance with increasing temperatures,[10,11] the linear decrease in V_{th} with the increasing temperature in 2D,[7] and the non-linear decrease in V_{th} with increasing temperature observed in the experimental work performed by Xu, *et al*.[12] on a 1D system and in the simulation study done by Savaikar, *et al*.[13]

and in this dissertation research.

Besides implementing more refined models discussed earlier in MITS, its capabilities can be further strengthened to address other related issues such as the measurement of junction widths and island sizes in the experimental devices in a scientific way. An image-processing tool needs to be developed which can be interfaced with MITS that would read in the physical parameters from the experimental device images that in turn could be fed as inputs to MITS. Such a tool could serve as a valuable resource especially for an experimentalist. Integrating the FEM solver developed by D. R. Banyai [to be published] can expand the application capabilities of MITS. Finally, building a graphical user interface can make MITS an integrated and a standalone tool that would serve as a user-friendly resource for researchers working in the area of single electron devices.

References

[1]A. N. Korotkov and Y. V. Nazarov, Physica B 173, 217 (1991).

[2]Y. V. Nazarov, Phys. Rev. B 43, 6220 (1991).

[3]C. H. Lee, S. Qin, M. A. Savaikar, J. Wang, B. Hao, D. Zhang, D. Banyai, J. A. Jaszczak, K. W. Clark, J.-C. Idrobo, A.-P. Li, and Y. K. Yap, Adv. Mater. 25, 4544 (2013).

[4]K. Elteto, E. G. Antonyan, T. T. Nguyen, and H. M. Jaeger, Phys. Rev. B 71, 064206 (2005).

[5]A. Middleton and S. Jha, Physics Paper 184 (2005), arXiv:cond-mat/ 0511094v1 [cond-mat.dis-nn], see http://surface.syr.edu/phy/184.

[6]A. A. Middleton and N. S. Wingreen, Phys. Rev. Lett. 71, 3198 (1993).

[7]R. Parthasarathy, X.-M. Lin, K. Elteto, T. F. Rosenbaum, and H. M. Jaeger, Phys. Rev. Lett. 92, 076801 (2004)

[8]D. D. Cheam, *Integration of Room Temperature Single Electron Transistor with CMOS Subsystem*, PhD dissertation, Michigan Technological University, Houghton, MI, 2009.

[9]R. Parthasarathy, X.-M. Lin, and H. M. Jaeger, Phys. Rev. Lett. 87, 186807 (2001).

[10]A. J. Quinn, M. Biancardo, L. Floyd, M. Belloni, P. R. Ashton, J. A. Preece, C. A. Bignozzi, and G. Redmond, J. Mater. Chem. 15, 4403 (2005).

[11]C. T. Black, C. B. Murray, R. L. Sandstrom, and S. H. Sun, Science 290, 1131 (2000).

[12]K. Xu, L. Qin, and J. R. Heath, Nat. Nanotechnol. Lett. 4, 368 (2009).

[13]M. A. Savaikar, D. Banyai, P. L. Bergstrom, and J. A. Jaszczak, J. Appl. Phys. 114, 114504 (2013).

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Madhusudan Savaikar <masavaik@mtu.edu> Thu, Nov 28, 2013 at 2:56 PM
To: Raghuveer Parthasarathy <raghu@uoregon.edu>

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R. Parthasarathy, X.-M. Lin, and H. Jaeger, Phys Rev Lett **87,** 186807 (2001).

Fig. 1. (a), (b), (c)

Fig. 2.

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Madhusudan

Raghuveer Parthasarathy <raghu@uoregon.edu> Fri, Nov 29, 2013 at 12:58 PM
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Dear Madhusudhan,

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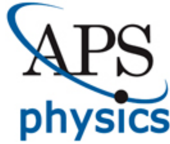

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