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Development of Room Temperature Operating Single Electron Transistor Using FIB Etching and Deposition Technology

By

MANORANJAN ACHARYA

A DISSERTATION

Submitted in partial fulfillment of the requirements

for the degree of

DOCTOR OF PHILOSOPHY

(Electrical Engineering)

MICHIGAN TECHNOLOGICAL UNIVERSITY
2009

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This dissertation, "Development of Room Temperature Operating Single Electron Transistor Using FIB Etching and Deposition Technology", is hereby approved in partial fulfillment of the requirements for the degree of DOCTOR OF PHILOSOPHY in the field of Electrical Engineering.

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Date

Dedicated to

My grandmother Nishamani

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Manoranjan Acharya

Date

ABSTRACT

The single-electron transistor (SET) is one of the best candidates for future nano electronic circuits because of its ultralow power consumption, small size and unique functionality. SET devices operate on the principle of Coulomb blockade, which is more prominent at dimensions of a few nano meters. Typically, the SET device consists of two capacitively coupled ultra small tunnel junctions with a nano island between them. In order to observe the Coulomb blockade effects in a SET device the charging energy of the device has to be greater that the thermal energy. This condition limits the operation of most of the existing SET devices to cryogenic temperatures. Room temperature operation of SET devices requires sub-10nm nano-islands due to the inverse dependence of charging energy on the radius of the conducting nano-island. Fabrication of sub-10nm structures using lithography processes is still a technological challenge. In the present investigation, Focused Ion Beam based etch and deposition technology is used to fabricate single electron transistors devices operating at room temperature. The SET device incorporates an array of tungsten nano-islands with an average diameter of 8nm. The fabricated devices are characterized at room temperature and clear Coulomb blockade and Coulomb oscillations are observed. An improvement in the resolution limitation of the FIB etching process is demonstrated by optimizing the thickness of the active layer. SET devices with structural and topological variation are developed to explore their impact on the behavior of the device. The threshold voltage of the device was minimized to ~500mV by minimizing the source-drain gap of the device to 17nm. Vertical source and drain terminals are fabricated to realize single-dot based SET device. A unique process flow is developed to fabricate Si dot based SET devices for better gate controllability in the device characteristic. The device

parameters of the fabricated devices are extracted by using a conductance model. Finally, characteristic of these devices are validated with the simulated data from theoretical modeling.

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Chapter 1: Introduction

1.1. Background

The new trends in lifestyle in the ubiquitous society, which could be called a "Hi-Tech Style" are widely spreading these days. Progress in ultrafast communication systems, is virtually shrinking the globe every day. Miniaturization in the storage technologies has given the privilege to have terabytes of data, in a wallet, thanks to the progress in micro-electronics.

The genesis of micro electronics can be traced back to the demonstration of the bipolar junction transistor (BJT) in 1947 [1]. This Nobel Prize winning invention eliminated the requirements of massive vacuum tubes with hundreds of terminal voltages even for minimal functionalities. The transistor operation was possible by power consumption in order of milli watts rather than a few hundred watts as for equivalent vacuum tube circuits. The BJT devices became the elemental block for any electronic circuits with various functionalities. However, the real capability of the BJT devices was fully exploited only when many of them can be integrated in a single chip, demonstrated in the invention of the integrated circuit in 1958 [2]. These two discoveries opened the path for high functionality based electronic technology. However, for complex application the power dissipation in the high density BJT based circuits became a major issue. Efforts to resolve the power dissipation issue gave birth

to the third breakthrough, the invention of Complementary Metal-Oxide Semiconductor or CMOS. CMOS based integrated circuits were announced in 1963 [3]. Collectively these three inventions demonstrated the conceptual basis for the modern low power micro-electronics.

Since its birth in 1960s, the tremendous growth in the micro-electronics industry in the last four decades is driven by the need to have portable devices having the capability of better computing coupled with large data storage and ultra low power consumption [1]. These requirements have increased the momentum of research and development efforts in semiconductor industry resulting in better performance and higher component packing density [4]. The development in micro-electronics, such as increased speed, increased complexity in functionalities, and the reduction in power dissipation etc. are made possible by continuously scaling the CMOS device, which is the fundamental block for any electronic circuit [5]. Scaling down the device size increases the number of devices per unit area, thus increasing the number of operations per second. This helps in multiplying the functionalities [6]. The last four decades have evidenced the trend in increasing the number of transistor per chip as per the famous Moore's Law [7]. As shown in Fig. 1.1, the number of transistors per chip doubled in almost every 24 months, doubling the speed and functionalities of operation. Remarkably, the industry has kept pace with this exponential growth for that last four decades. However, the issue with this growth is that when the exponential growth in the device density rapidly approaches infinity, the physical systems generally cannot run to infinity [8]. Even Moore himself pointed out in 2003 that "No exponential change of a physical quantity can, however, continue forever" [9]. This could very well mean reaching a dead end with existing CMOS scaling. This predicted dead end is based on definitive physical laws which need to be understood.

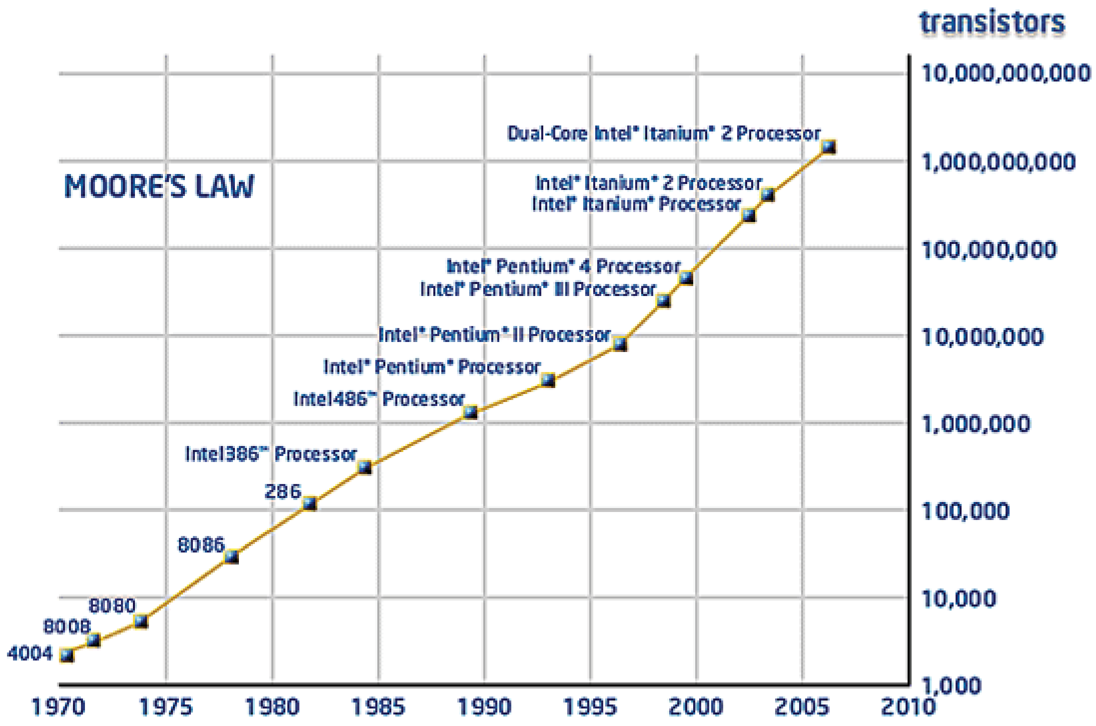


Fig. 1: The increasing rate of the transistors per chip [Source: www.intel.com]

1.2. CMOS Scaling: Issues and Probable Solutions

The basic idea of scaling is to reduce the dimensions of the CMOS transistors and the wires connecting them in integrated circuits [6]. Scaling of CMOS was first proposed by Dennard et. al. [10] to secure the switching characteristic by suppressing the short channel effect. It was recognized that by reducing the dimensional parameters like the gate length (L_g) and gate width (W_g) by a factor K, a decrease in the propagation delay, the drain current, and threshold voltage would result by the same factor (1/K) [11]. This is the basis for CMOS scaling demonstrated by Moore's law over the last four decades [12].

The scaling can be done in two different ways *1. Constant Field Scaling* and *2. Constant Voltage Scaling*. A CMOS device works by modifying the electric field just beneath the surface

of the silicon layer in the gate area to control the flow of current between sources and drain. Constant field scaling achieves the same electric field profile in the smaller transistor by reducing the applied voltage along with all the key dimensions, including the gate oxide thickness (t_{ox})[6]. The constant field scaling can lead to increased number of circuits in a given chip area with no increase in the total power dissipation [13]. During the 1980s the constant field scaling was replaced by constant voltage scaling in order to maintain a constant voltage throughout different generations of chips. The constant voltage scaling has introduced constant increase in the fields and thus in 1990s constant field scaling was reinvented [14]. One of the most important reasons is its positive impact on the power density.

Following constant field scaling, the device size decreased to 0.25 micron without any major issue. But when the device size reached 90nm with 50-60nm gate length, leakage current in the sub-threshold region became an issue [15]. Hence, leakage power became significant to limit the scaling. With further reduction in device size, the scaling is confronted with some fundamental limitations along with limitations based on other factors like process, materials and system. According to Meindl, et al. [15,16] the theoretical and practical limitations in device scaling can be codified into 5 different categories 1. Fundamentals, 2. Materials, 3. Device, 4. Circuits and 5. Systems. The fundamental limits can be derived from the physical principles such as quantum mechanics, thermodynamics and electromagnetism. The material limits are determined by the carrier mobility, carrier saturation velocity, break down field strength, and thermal conductivity. The impact of these parameters on device performance is of great concern when the device size goes below 100nm. [16, 17]. Taking an example, at the 65nm technology node, the thickness of the gate oxide is 1.2nm, which is a

few monolayers of Si-O bonds [18]. Hence further reduction in the gate oxide is almost impossible due to the high tunneling current. It is likely that tunneling currents arising from silicon dioxide (SiO_2) thinner than 0.8 nm cannot be tolerated, even for high-performance systems [12]. Apart from the above material limitations, process related limitations to fabricate a device of channel length below 60nm is always a challenge. With scaling, as the functionalities per chip multiplies, it multiplies the number of devices and hence the total leakage current. This requires efficient and fast dissipation of heat generated by the leakage current, which is still a technological limit at the system level.

These limitations raise the question regarding the existence of CMOS technology in the future. This also drives tremendous effort in research to make the CMOS technology survive for the longest period possible. As discussed above, one of the biggest impediments to the CMOS scaling is the leakage current both from the sub threshold leakage and the gate-dielectric leakage. The effort to overcome these issues can be categorized in two different ways; new materials and new device setups. Gate dielectric leakage current is basically caused by the hot carrier effect and electron tunneling through the gate dielectric. To reduce these currents, high-K based gate dielectrics can be introduced to have a higher physical thickness with same electric field magnitude. However, the benefits of just replacing the SiO_2 with a high-K material for the same electrical field are limited by the presence of two-dimensional electric fringing fields from the drain through the physically thicker gate dielectric [19, 20]. The use of higher-K materials must therefore be combined with a concurrent reduction of the electrical thickness. In addition, other factors like thermal stability, the impact of surface states etc. have to be considered for using high-K materials. Replacement of poly-Si gate electrodes by a metallic gate is another technique to improve the device scaling below the

50nm regime. Its advantages to counteract the gate capacitance degradation and carrier mobility degradation have made it an unique technique for today's sub-50nm CMOS technology. Combination of these two material set-ups can be used for future high performance low power circuits to push the device size even further.

Other than the different material set-ups, new device set-up has been developed to improve the functionality favoring the device scaling. Double/multi-gate MOSFETs [21] or FinFET [22] in which a second gate is added opposite to the traditional gate, have been recognized for their potential to better control the short-channel effects. It is also shown that a Double Gate –FET (DG-FET) can be scaled to a very short channel length (25 to 30 nm) while achieving the expected performance derived from scaling [23]. However, issues in setting up multiple threshold voltage in the same chip along with the fabrication challenges limit its future for future ultra-low power ULSI circuits. Strained Si based devices is also been of great interest for their potential to increase the carrier mobility. In particular combination of strained Si technique with SOI based devices has proven immense potential in the scalability of the devices [24]. Vertical MOSFET configuration provides other new device options for higher levels of functional integration [25].

Advanced techniques in material and device set-ups along with development in the process technology will improve the device performance and will continue the CMOS scaling in the near future till the gate length in a transistor reaches 10nm limit. However, no possible solution is still known to advance the scaling below the 10nm limit. In the sub-10nm regime the materials will lose their bulk properties and the performance of the devices will be dominated by the quantum effects.

Nano-scale devices, which utilize the quantum effects for its operation, are a possible solution for the devices of the next generation. Some of the potential candidates are the, 1D structures (Carbon nanotubes and nano wires), spintronic devices, resonant tunneling devices, single electronics, molecular electronic devices, ferro magnetic logic devices, and devices based on quantum cellular automata [4]. Carbon nanotube based FETs are already demonstrated as a potential device for future logic circuits [26]. However, the difficulties in understanding the detailed physics and the fabrication issue limit their development for future ULSI circuits. Dominance of the Schottky tunneling barrier between the source/drain and the channel, over the carrier transport is another issue that needs to be overcome in these devices [27,28].

1.3. Single Electron Devices: A Successor of CMOS

When the CMOS reaches the ultimate limits of scaling of below 10nm, single electron effects limit the normal transistor action at the smallest length scales and hence some perceive the Single Electron Devices to be a natural successor to the CMOS devices. Single Electron Devices operate on the simple principle of Coulomb blockade, and can manipulate electrons at the level of elementary charge, hence their operation is guaranteed even if the size of the device is reduced to the molecular level. Single Electron Devices not only function as simple switching device but also show immense potential for large scale integration. Single Electron Transistors (SETs) are the most fundamental three terminal single electron devices. Single Electron Transistors are quantum devices in which, instead of working with currents and voltage levels, which are defined by millions of electrons as in today's CMOS technology, one can realize the limit of performing logic operations with

single or small number of electrons [29]. Hence, these devices can work with extremely low power dissipation. The low power consumption and sensitivity to high charge of the SETs makes a potential candidate for sensing and ULSI based applications [30, 31].

The field of single electron devices is developed by several Nobel prizes and Nobel prize winning discoveries and insights. One can argue that the origin of SET devices started in the early 20th century when Robert Milkman showed by his oil drop experiment that charge is discrete and single valued. He achieved localization of a single electron in an oil drop and found out how to measure its elementary charges. For his breakthrough discovery he received the Nobel Prize in 1923. To replicate the same phenomenon in solid state it took several decades. It was in late 1980s when the first manipulation of single electrons realized what is known as single electronics today. But before that could happen, quantum mechanical modeling, explaining the quantum mechanical tunneling of electrons had to be developed. The Coulomb blockade effect, which is the basic working principle for the single electronic devices, was first explained by C. Gorter [32]. In 1951, he explained correctly the current suppression in low bias voltage as the cause of Coulomb repulsion. After ten years the same current suppression effect at low bias was again observed by C. Neugebauer and M. Webb during their study of current conduction in granular films [33]. It took another two decades until 1985 when D. Averin and K. Likharev [34] formulated the popular orthodox theory to explain the single electron tunneling phenomena. This theory quantitatively describes the single electron charging effects such as Coulomb blockade and Coulomb oscillations. The experimental realization of Single Electronic devices started after the invention of the Scanning Tunneling Microscope (STM). The STM was used in several variations to build the single electron devices in nano-scale and opens the possibilities of

manufacturing room temperature operating single electron transistors. However, STM is not the first method of fabricating Single Electron Transistors. Dolan and Fulton [35] used a double shadow evaporation method and fabricated the first Single Electron Transistor showing single electron charging effects. Since then tremendous development has occurred in the field of single electron transistors. The evolution in the design and process technology in the SET devices is detailed in the following chapter.

The most important reason for the increasing interests for Single Electronic Transistor Devices is due to its ultra low power consumption and small size. Table 1 shows the ITRS-2007 report for the comparison in the parameters of different research devices. As it can be observed, the comparative data in Table 1.1 shows that the SET device beat peer devices due to its low power consumption and high device density capability. The only issue retarding the progress of SET devices as for future ULSI systems is its lower fan-out [35]. However, this could be solved by innovative circuit design such as the binary decision diagram [36].

Table 1.1: A comparison study of the next generation emerging devices [Source:ITRS2007]

Device			FET Extension					
		FET [A]	1D structures	Channel replacement	SET	Molecular	Ferromagnetic logic	Spin transistor
Typical example devices		Si CMOS	CNT FET NW FET NW hetero-structures Nanoribbon transistors with graphene	III-V compound semiconductor and Ge channel replacement	SET	Crossbar latch Molecular transistor Molecular QCA	Moving domain wall M: QCA	Spin Gain transistor Spin FET Spin Torque Transistor
Cell Size (spatial pitch) [B]	Projected	100 nm	100 nm [D]	300 nm [I]	40 nm [O]	10 nm [U]	140 nm [Y]	100 nm [C]
	Demonstrated	590 nm	~1.5 μm [E]	1700 nm [J]	~200 nm [K, L]	~2 μm [V]	250 nm [Z, AA]	100 μm [AB]
Density (device/cm^2)	Projected	1E10	4.5E9	6.1E9	6E10	1E12	5E9	4.5E9
	Demonstrated	2.8E8	4E7	3.5E7	~2E9	2E7	1.6E9	1E4
Switch Speed	Projected	12 THz	6.3 THz [F]	>1 THz	10 THz [Q]	1 THz [W]	1 GHz [Y]	40 GHz [AC]
	Demonstrated	1.5 THz	200 MHz [G]	>300 GHz	2 THz [R]	100 Hz [V]	30 Hz [Z, AA]	Not known
Circuit Speed	Projected	61 GHz	61 GHz [C]	61 GHz [C]	1 GHz [O]	1 GHz [U]	10 MHz [Y]	Not known
	Demonstrated	5.6 GHz	220 Hz [H]	Data not available	1 MHz [P]	100 Hz [V]	30 Hz [Z]	Not known
Switching Energy, J	Projected	3E-18	3E-18	3.00E-18	1×10^{-18} [O] [$>1.5\times10^{-17}$] [S]	5E-17 [X]	~1E-17 [Z]	3E-18
	Demonstrated	1E-16	1E-11 [H]	1E-16 [J]	8×10^{-17} [T] [$>1.3\times10^{-14}$] [S]	3E-7 [V]	6E-18 [AA]	Not known
Binary Throughput, GBit/ns/cm^2	Projected	238	238	61	10	1000	5E-2	Not known
	Demonstrated	1.6	1E-8	Data not available	2E-4	2E-9	5E-8	Not known
Operational Temperature		RT	RT	RT	RT [M, N]	RT	RT	RT
Materials System		Si	CNT, Si, Ge, III-V, In_2O_3, ZnO, TiO_2, SiC,	InGaAs, InAs, InSb	III-V, Si, Ge,	Organic molecules	Ferromagnetic alloys	Si, III-V, complex metals oxides
Research Activity [AD]			379	62	91	244	32	122

1.4. Research Objectives

Development of the FIB etch-deposition based SETs and optimization of its fabrication process is the core of the present work. Additional objectives such as characterization of the multi tunnel junction (MTJ) based devices and the impact of design parameters on the device behavior are also set to support the study. In specific the objectives include:

- ✓ Exploring the fabrication of single dot based RT-SET using FIB.
- ✓ Characterizing the FIB etch and deposition process and studying the factors limiting resolution in the nano regime. Studying the impact of beam profile during FIB etching.
- ✓ Optimizing the FIB etching process to maximize the resolution.
- ✓ Development of fabrication process for RT-SETs using FIB etch and deposition technology.
- ✓ Improvement in the performance of the RT-SETs through design.
- ✓ Studying the impact of structural and topological variation in the performance of a RT-SET device.
- ✓ Exploring the realization of semiconductor quantum dot based RT-SETs.
- ✓ Device characterization and demonstration of Coulomb blockade effect and Coulomb oscillation at room temperature.
- ✓ Device modeling and comparison of modeling and experimental results.

1.5. Dissertation Outline

This dissertation details the research carried out for developing Single Electron Transistors operating at room temperature using Focused Ion Beam etch and deposition technology. Chapter 2 describes the theory of SETs , the evolution of technology for fabricating the SET devices and the design of room temperature operating SET devices.

Chapter 3 details the fabrication of the SET devices using FIB etch and deposition processes. The issues in FIB etching process in nano-scale regime and their possible solution is also detailed in this chapter. The characterization process along with the device current

voltage characteristic of the fabricated SET devices are discussed in Chapter 4 and analyzed in Chapter 5. Finally, the conclusion of the work is described in Chapter 6 and the future recommendations are summarized in Chapter 7.

Chapter 2: Theory of Single Electron Transistors and Device Design

The increase in the demand of complex functionalities and unmatched computational ability in present electronic circuits requires higher device density and efficient design. Although new and reliable design technique like DFM (design for manufacturability) and multi-layer routing can enhance the device density by some factor [37], ultimately device size is the key parameter to increase the device density in the demanding ULSI circuits. The reduction of the device dimensions of the CMOS devices by continuous scaling has placed the devices in the length scales of sub 50nm. However, as discussed in the Chapter 1, the device scaling is difficult when the gate length reaches below 30nm. At sub 30nm length scale, the Coulomb blockade and single electron charging effects become dominant, thus impacting the characteristics of the CMOS transistors, in a detrimental way. These effects can be utilized as the basic principles to realize functional devices, which have potential to be used as nano electronic devices. The Single Electron Transistor (SET) is one of such device which has great potential to work in conjunction with CMOS devices for future high speed ULSI circuits.

The SET device works in the principle of Coulomb blockade, which is prominent when the device dimension is scaled down to a few nano-meters [38]. In SET devices, a free electron can be confined in a nano-meter sized island and can tunnel to/from the electrode

terminal by quantum mechanical tunneling. The islands can be made up of any metal or semiconductor material.

2.1. Theory of Operation

The operation of a Single Electron Transistor device can be derived from the charge quantization principle. The charge in any small isolated electron puddle is quantized: it contains only an integer number of electrons. Also this charge can only change in multiples of a single electron [39]. The operation principle of a SET can be explained from this charge quantization effect with a simple example of charging a conducting sphere (representing an island) [40]. Consider a small sphere which is electrically conductive and initially electro neutral. At this point the net charge on the island is zero as the number of protons is equal to number of electrons inside it. Thus the electric field outside the island is zero. Now to charge this island by supplying some electrons to it, the electrons have to expend some energy. For the first electron, a weak external force can do the job as there is no repulsive force from the sphere. Once the sphere is charged by one electron the net charge Q on the sphere is now $-e$. Hence, as shown in Fig 2.1, to move the second electron in to the sphere, a force $F = e\,E$ is the required overcome the repulsion due to the additional electric field E by the existing electron in the sphere. This phenomena repeats every time one additional electron is added to the island. The generated electric field depends on the size of the island, the number of additional electrons in it and the material properties of the island. Though the fundamental charge $e = 1.6 \times 10^{-19}$Coulomb is very small on the human scale of things, the field is inversely proportional to the square of the island size and may become rather strong for nano scaled structures [40]. The energy required to overcome this field is called

the charging energy and for each electron it can be defined as $E_c = {e^2}/{2C_{eff}}$, where C_{eff} is the effective capacitance of the island. The effective capacitance, C_{eff}, is determined by the size of the island and the electrostatics of the ambient.

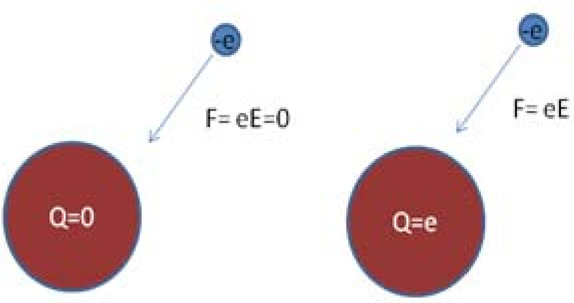


Fig. 2.1: Charging of a metallic sphere with no-charge and charged state

The SET device works in the principle described above where the electron transport to/from the dot takes place by tunneling from the electrode terminals through the tunnel junction. The basic structure of a typical SET device consists of a central island capacitively coupled to the source and drain electrode terminals by two small tunnel junctions. A third gate electrode can be resistively or capacitively coupled to the central island. Electrons can tunnel from the source to the drain electrode through the island. The electron tunneling from the electrodes to/from the nano-island occurs only when the energy supplied by the voltage source is large enough to overcome the charging energy of the system. Hence, in a drain current characteristic of the SETs, the current is suppressed for the lower bias region. This represents the confinement of a single electron, which is only possible when the energy supplied by the voltage is less than the charging energy of the device. The suppression of the current due to this single electron confinement is called Coulomb blockade effect. The

charging energy of the device depends on the effective capacitance of the island with respect to the ambient surrounding and the charge on it. The charge on the island can be controlled by varying voltage on the gate electrodes [39,40,41,42]. Hence, the flow of electron current from the source to drain electrode can be modulated by the voltage in the gate electrode. Figure 2.2 shows the schematic of a SET device along with its electrostatic model.

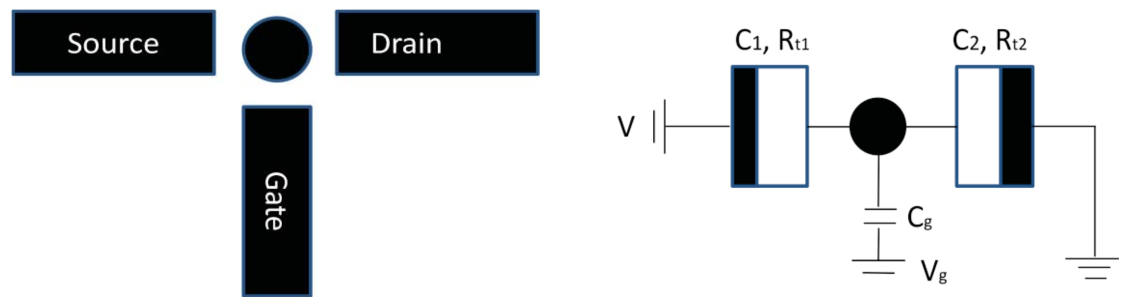


Fig. 2.2: (Left) Basic structure of a SET device. (Right) The electrostatic model of the device.

Throughout the history of the single electronics, a generalized theory has been used to explain the characteristic of the SET devices. This simple and effective theory called the as "orthodox theory" was first developed by Kulik, et al [43]. This theory is based on the following assumptions:

1. The electron energy quantization inside the conductors is ignored, i.e., the electron energy spectrum is treated as continuous;
2. The time for electron tunneling through the barrier is assumed to be negligibly small in comparison with other time scales (including the interval between successive tunneling events);

3. Coherent quantum processes consisting of several simultaneous tunneling events ("co-tunneling") are ignored.

Despite the above assumptions, orthodox theory has very good quantitative agreement with the experimental data [40, 41]. From the outcomes of this theory it is observed that at least two conditions have to be satisfied to make SET devices operable: 1. The charging energy has to be greater than the thermal energy and 2. Tunnel resistance of the junctions has to be greater than the quantum resistance. The first condition has to be satisfied in order to distinguish the Coulomb blockade effect from the thermal agitation of the electrons. At the same time the resistance of the tunnel junction has to be large enough to avoid the band broadening effect which eventually may destroy the electron confinement in the islands [44]. These conditions are quantitatively represented in Eq. 2.1 and 2.2.

$$E_c\left(= e^2/2C_{eff}\right) > k_B T \tag{2.1}$$

$$R_t \gg R_Q \tag{2.2}$$

Where , $E_c = Charging\ Energy\ \left(= {e^2}/{2C_{eff}}\right)$;

$T = Temperature,\quad k_B = Boltzmann\ Constant;$

$R_t = Tunneling\ resistance\ of\ the\ tunnel\ junctions;$

$R_Q = Quantum\ Resistance = {h}/{e^2}\ (= 25.6k\Omega);$

From Eq. 2.1 it can be observed that the effective capacitance, C_{eff}, is the parameter which determines the critical temperature at which the device can operate. From a simple calculation it can be obtained that the effective capacitance, C_{eff}, of the island has to

be in order of 10^{-18}F or lower to make a SET device operable at room temperature (T=300K). The effective capacitance consists of the self capacitance of the quantum dot and its capacitance with respect to the source, drain and gate electrodes. Considering the island to be spherical in shape, it can be calculated that for an effective capacitance to be in order of aF the diameter of the island has to be 10nm or less. This is one of the challenges for progress in the fabrication of the SET operating at room temperature.

Figure 2.3 shows the V-I characteristic of a SET device with different gate voltage V_g. This non linear I-V characteristic of the device shows that for voltages less than e/C the dc current is suppressed due to Coulomb blockade effect. After a threshold voltage V_t the Coulomb blockade is overcome and the current approaches one of its linear asymptotes. For a SET device it can be observed that, the threshold voltage, as well as the source drain current in its vicinity, are a periodic function of the gate voltage.

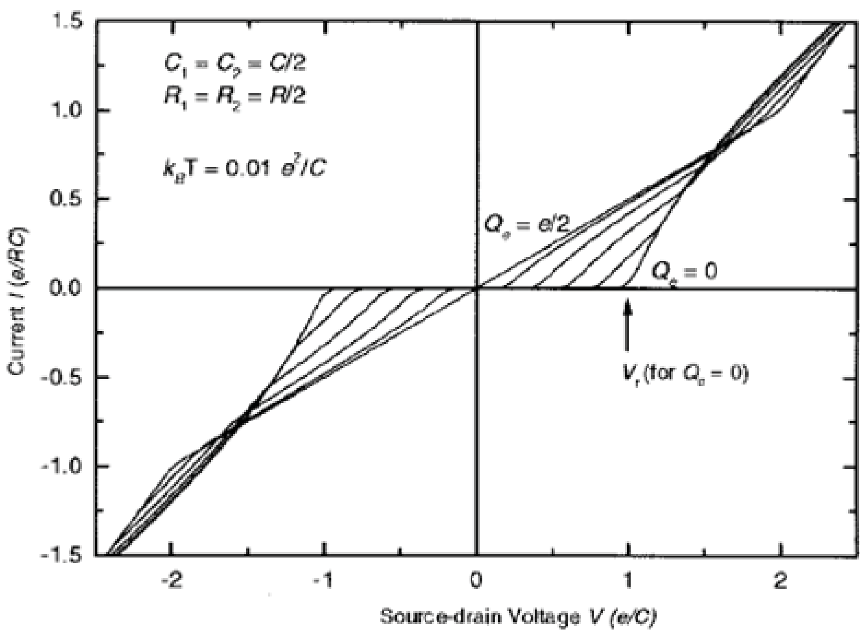


Fig. 2.3: V-I characteristic of a SET device. Where C_1, C_2, and R_1, R_2 represents the junction capacitances and resistances respectively for the two junctions in the SET respectively. Q_0 represents the gate voltage induced charge.[Reprinted with permission from K.K. Likharev, Proceedings of the IEEE, Vol 87 (4), 1999,© 1999 IEEE]

The presence of this oscillation in the drain current with respect to the gate voltage can be explained by the stability diagram as shown in Fig. 2.4 [38]. In the stability diagram the x-axis represents the gate voltage and the y-axis represents the source-drain voltage. The double-hatched rhombic-shaped regions, which are called Coulomb diamonds, are the stable region. Outside the Coulomb diamonds, the number of electrons in the island fluctuates between certain numbers. However inside the Coulomb diamond region, the fluctuation is minimum, i.e., the electron number changes only between two adjacent integers. In the unstable region, the degree of the fluctuation is related to how far the voltage conditions are apart from the Coulomb diamonds. In the stable (Coulomb diamonds) regions, when there

is a finite voltage between the source and drain, electrons are transferred one by one between the two electrodes. And this can be represented as a periodic oscillation in the drain current (or Conductance) with respect to the gate voltage. This is called the Coulomb oscillation and is shown in Fig. 2.4.

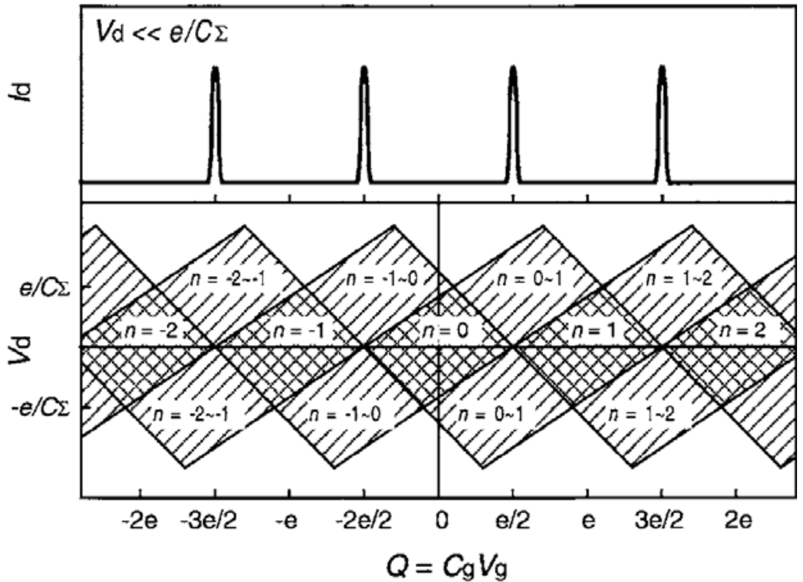


Fig. 2.4: Coulomb Oscillation and stability diagram of a SET. V_d represents the source-drain voltage and C_Σ is the effective capacitance of the device. [Reprinted with permission from Y. Takahashi, Y. Ono, A. Fujiwara and H. Inokawa "Silicon single-electron devices" J. Phys. Condens. Matter Vol. 14, R995, 2002,© 2002 Institute of Physics]

2.2. Single Dot and Multi Dot SETs

The current conduction in a SET device takes place by tunneling of electrons from the source to the drain electrode through the quantum dot. Depending on the number of quantum dots taking part in this conduction process, the SET devices can be divided in two categories: 1.Single Dot based SET where only one dot takes part in the electron transport process; and 2. Multi-Dot based SET, where more than one dot can take part in the electron

transport process. In a single dot based device the electron tunneling occurs only through two tunnel junctions. In the other hand, for a multi dot based device an electron traverses an array of tunnel junctions for its tunneling from the source to the drain electrode. Hence, the multi-dot based SET devices are also called as Multi Tunnel Junction (MTJ) based SETs. Depending on the orientation of the dots, the MTJ devices can also be two dimensional (2D) or one dimensional (1D) devices. In a 1D MTJ base SET, there is just one path for the electron. The electron from the source terminal hops from one dot to another to reach the drain terminal. However, in 2D MTJ based devices, there is more than one parallel path. Theoretical work [45, 46] in 2D MTJ based SET devices shows that the electron will follow a dominant conducting path (DCP) to tunnel from the source to drain electrodes. However, the characteristics of the device can depend on the capacitance presence due to the addition dots other than the DCP. A pictorial view of the electron transport path in a single and 2D multi dot based SET device is shown in Fig. 2.5. For a same size of dots the critical temperature for a MTJ based device is higher than that for a single dot based device. This is because of the reduction in the effective capacitance in the case of MTJ device due to series capacitance by the additional dots. However, this reduction in effective capacitance can lead to a higher threshold voltage, which is undesirable. In this work, MTJ based devices are studied and the impact of this additional capacitance is also investigated.

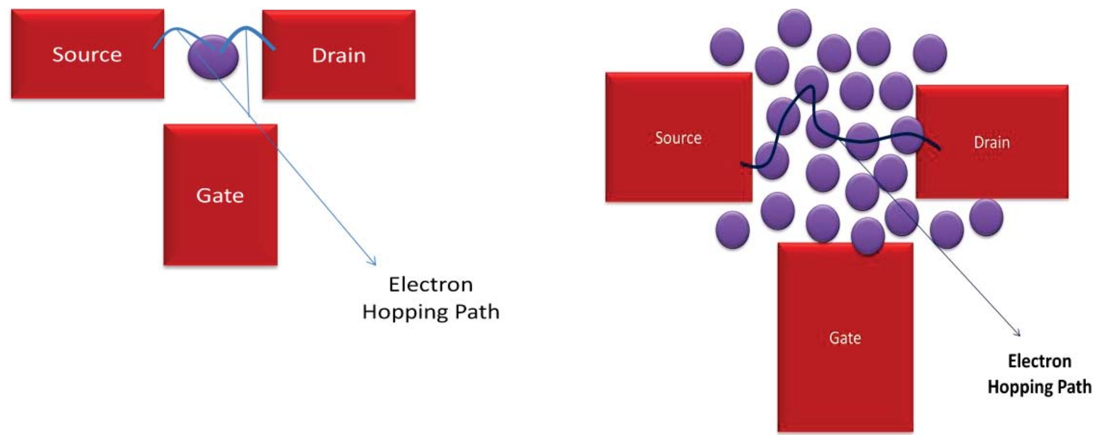


Fig.2. 5: A pictorial view of (Left) Single dot based and (Right) Multi-Dot Based SET devices with possible path of electron transport.

Both the single dot and multi dot based SET requires sub-10nm sized quantum dots to operate at room temperature. Fabrication techniques enabling sub-10 nm feature sizes are indispensable for fabricating SET devices, operable at room temperature. Various structures for SETs have experimentally fabricated. Most of them are developed for low temperature application. From the initial studies on Single Electron systems, mainly metals and III-V compound semiconductors have been used to investigate the basic physics of the transport and to explore possible applications, because of the ease of confinement of electrons possible in the two dimensional electron gas (2DEG) in III-V compounds. The material requirements for the SET are that, the central island can be made of semiconducting material or a metal. Both metallic and semiconducting central islands are studied in the present work.

2.3 Evolution in Technologies for SETs

The first experimental demonstration of the SET devices based on a metallic island was done by Fulton and Dolan in 1987 [35]. The charging effect and Coulomb blockade behavior was observed experimentally by employing the configuration shown in Fig. 2.6 in which three Al-Al junctions with small area and overlap capacitance are formed on a small common electrode. The device is fabricated using e-beam lithography and multiple angle deposition-oxidation-deposition cycle [47]. As the size of the central island is much larger than 10nm, the device could only work in 1.1-4.2K temperature. The V-I characteristic of the device is shown in Fig. 2.7.

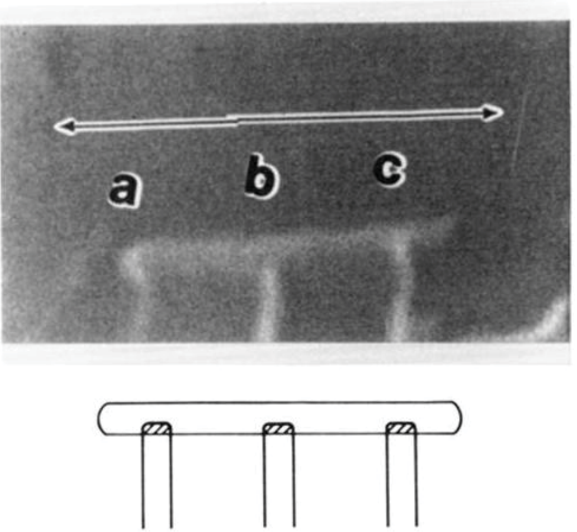


Fig. 2.6: SEM image of the first fabricated SET by Fulton and Dolan. The junctions labeled as a, b and c are formed where the vertical electrodes overlap the contact, the longer horizontal central electrode. [Reprinted with permission from T. Fulton and G. Dolan, Phy. Rev. Lett, Vol. 59, p109 (1987), © 1987 American Physical Society]

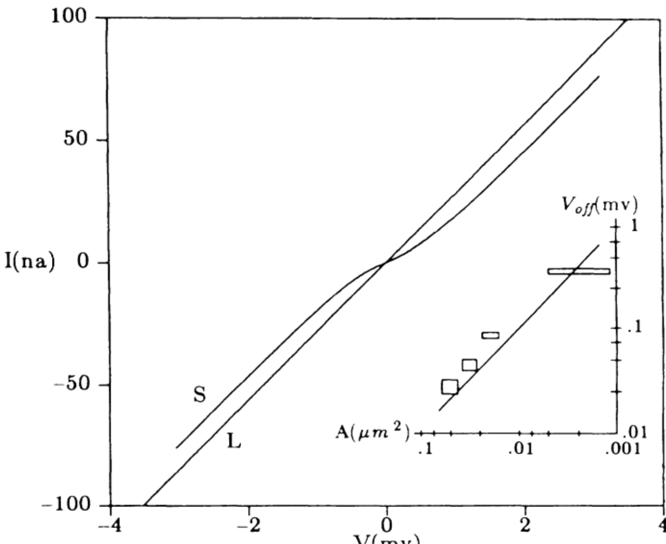
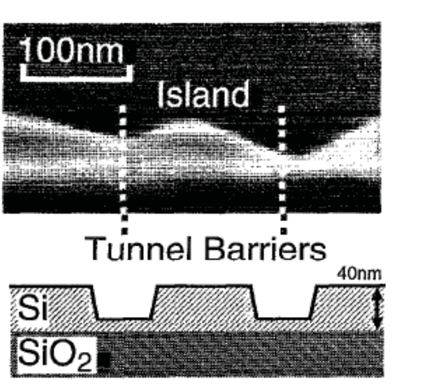


Fig 2.7: The V-I characteristic of the SET device fabricated by Fulton and Dalon. [Reprinted with permission from T. Fulton and G. Dolan, Phy. Rev. Lett, Vol. 59, p109 (1987), © 1987American Physical Society].

In a further investigation, Coulomb oscillations were also observed in a device with a narrow GaAs channel interrupted by two potential barriers. However these devices were only good for low temperature applications [below 4.2K] as the observed effective capacitance is much higher than the critical value of that for room temperature application [48]. A further increase in the charging energy is achieved by using silicon on insulator (SOI) layer of separation by implanted oxygen (SIMOX) process. The first SOI wafer used in SET fabrication was reported by Ali and Ahmed [49] as shown in Fig. 2.8. The E_c reported by this method was 1.6 meV. The island size was still limited by lithography, and the Coulomb blockade (CB) effects observed at few Kelvin temperatures. The operating temperature has

been increased by decreasing the size of the nano-island with the advances in the fabrication technology. In 1996 Nakamura and Chen, et al. [50] reported an aluminum island based SET that can operate at 100K temperature. These devices function and exibit the Coulomb blockade effect with an artificially fabricated 20-nm island electrode by utilizing standard e-beam lithography and three-angle evaporation process. A charging energy of ~12meV and an overall capacitance of ~15aF are reported in these devices. These resultant parameters are also far from the required charging energy for the room temperature operation of the device.



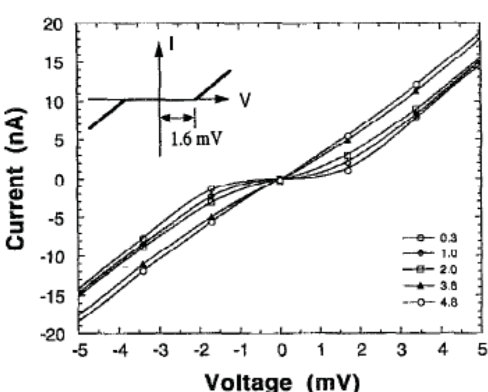


Fig 2.8: SEM image of a 100nm diameter island on a SOI wire as fabricated by Ali et al. and (Right) the V-I characteristic of the device fabricated using this island. [Reprinted with permission from D.Ali and H. Ahmed, Appl. Phys. Lett, Vol.64, p2119, (1994), © 1994 American Institute of Physics]

The first room temperature operating Coulomb oscillation was reported by Matsumoto et al. using scanning tunneling microscopy (STM) as a fabrication process [51]. Using the STM tip as a cathode, the surface of the titanium metal has been oxidized, and a few tens of nanometer wide oxidized titanium line was made to realize the Coulomb

blockade effect in a Ti/TiOx system. The principle of this nano oxidation process for Ti/TiOx system on SiO_2 is shown in Fig. 2.9. The Coulomb staircase of 150 mV period is observed in the current–voltage characteristics of this SET system at room temperature. The oxidation process for forming the tunnel junction is further used in a different way to fabricate silicon based SETs operating at room temperature.

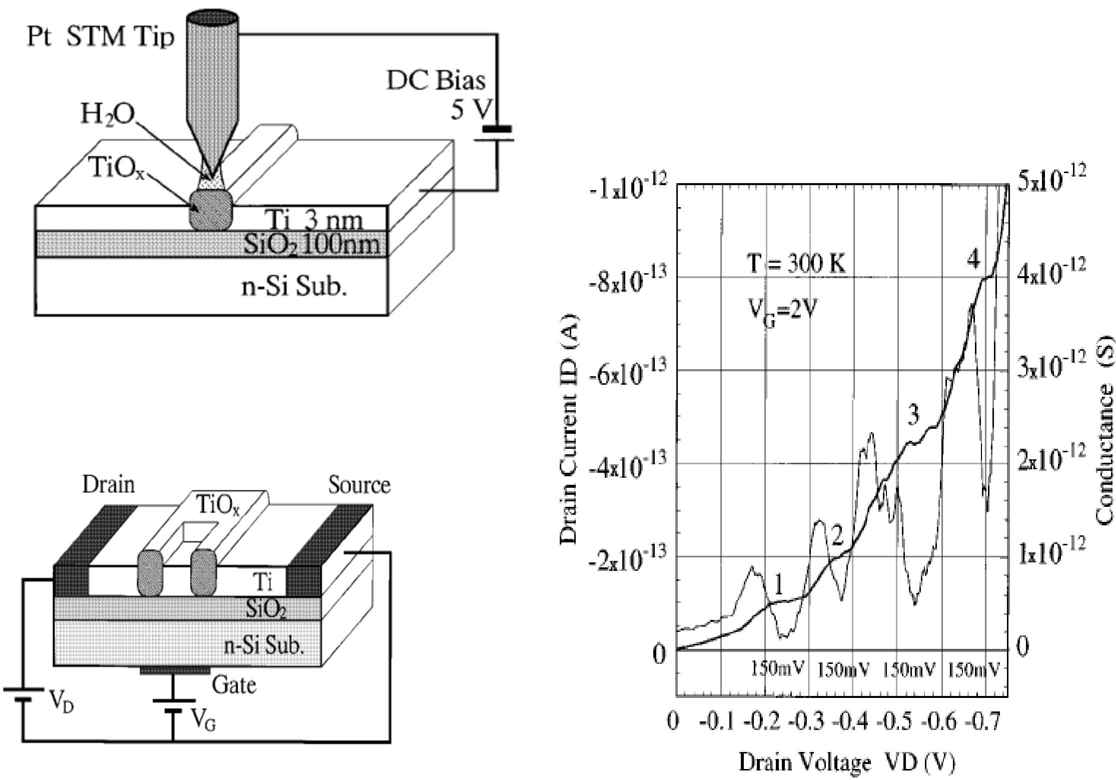


Fig 2.9: The room temperature SET fabricated by STM tip by Matsumoto et al. (left top) Principle of STM nano-oxidation process using STM tip as cathode.(left bottom) Cross-sectional view of single electron transistor fabricated by STM nano-oxidation process.(right) Drain current–voltage characteristics ~thick line and conductance (fine line) of SET at room temperature. Gate bias is set to 2 V. [Reprinted with permission from K. Matsumoto, M. Ishii, K. Segawa, Y. Oka, B. J. Vartanian and J. S. Harris, Appl. Phys. Lett, Vol. 68, p1,(1996), © 1996American Institute of Physics]

Takahashi et al. reported the first room temperature operating Si single electron transistor using pattern dependant oxidation (PADOX) method [52]. In this process, a one-dimensional Si wire was converted into a Si island with tunneling barriers at each end by

means of pattern dependent oxidation of a very thin Si layer on SO_2. Using this technique the total capacitance of the device can be reduced to ~2aF which enable conductance oscillation at room temperature.

An improved version of PADOX is called vertical-PADOX which uses vertical thermal oxidation of a long silicon wire with a thickness modulation resulting in higher charging energy. The fabricated SETs by both PADOX and V-PADOX are recognized to show Coulomb oscillation at room temperature. However, repeatability in the fabrication of the tunnel barrier is the biggest issue in these processes [53, 54]. This issue was further addressed by a controlled formation of the tunnel barrier. Thermal oxidation is used in metal system to improve the device parameters and operating temperature by decreasing the island size. Shirakasi et al. [55] reported a Nb/Nb oxide based SET device fabricated by thermal oxidation and scanning probe microscopy (SPM) based anodization technique. These devices showed extremely high charging energy and are operable at room temperature.

Apart from the conventional technique, in which the fabrication of the nano islands solely rely on the resolution limits of the lithography process, non-conventional bottom-up techniques can be used to fabricate the SET which are more likely to operate at room temperature. Non-lithographical techniques, based on nucleation of silicon are used to produce Si nano crystals which can be used as the quantum islands for a multi dot based SET device. Dutta et al. [56, 57] reported SETs with silicon nano crystals, where the charging energies were in the range of few tens of meV. The nano crystals of size ~8nm were deposited using VHF-plasma CVD technique, on a SOI substrate. The source and drain electrodes were formed with an inter-electrode gap of 30nm. SETs with a charging

energy of a few meV were observed. In a similar investigation for metallic system, clear Coulomb blockade effects have been observed in lateral metal nanostructures with gold nano crystals fabricated by combined electron beam lithography and ionized beam deposition. An overall capacitance of 0.2aF and a charging energy of 0.4eV were observed [58]. Although, the nano crystal based SET showed substantial increase in the charging energy, lack of repeatability in the fabrication of the tunnel junctions and the nano islands is one of the biggest issue in them. In some further efforts one dimensional nano island array based SET were fabricated with improved controllability in the tunnel junction fabrication [59]. However, the obtained charging energies were only good for low temperature operation.

The non-conventional one dimensional nano structure like carbon nano-tubes (CNT) can also be used to realize the SET devices. J. Kong et al. in 2000 reported a SET device operating at 160K temperature, using potassium doped semiconducting single walled CNT as the island [60]. In the very next year W. Henk et. al. reported a room temperature operating SET device showing the charging energy E_c of 120meV. The devices feature a short (down to ~20 nanometers) nanotube section that is created by inducing local barriers into the tube with an atomic force microscope. In a similar work room temperature operation of the SET device is achieved by controllably grown carbon nano tubes by using the patterned chemical catalyst based thermal CVD process[61]. Introduction of the new material and nano structures has potentially increased the operating temperature of the SET devices. However, such approaches have limited ability to reproducibly achieve the positional and dimensional accuracy for the required nano structure to realize the operation of the SET devices. Integration of the SET devices with the conventional CMOS circuits,

which is the prime motivation for researching this device, requires precise positioning of the associate nano structure, which is still a technology challenge with the above mentioned process.

From the above discussion it can be inferred that although different technologies have been explored to fabricate the SET devices, even with elevated operating temperature, repeatability and the compatibility with CMOS technology still needs to be improved. The present work looks at the potential technologies for realizing room temperature operating SET devices which can be fabricated more reliably and much faster than some existing technologies and compatible with the CMOS processing.

2.4. Modeling the V-I current characteristic of a Single Electron Transistor

In a single dot SET device, the current conduction takes place by tunneling of electrons through two capacitive junctions. The non-linear current voltage characteristic of such a device can be explained using orthodox theory [62]. A master equation based model using the orthodox theory can be used to predict the behavior of the device for different device parameters [63]. However, this model cannot predict the characteristic of a device having more than one dot. The device characteristics of a multi-dot SET system can be explained using the charge soliton analysis [64] in which the multi-dot SET system can be analyzed as a linear array of tunnel junctions. In the present work SET devices with different structural and topological configuration have been investigated with the possibility of having both multi dot and single dot behavior in different devices. Hence, both master equation and

a soliton based modeling approaches are made to predict the behavior of different sets of devices.

2.4.1. Master Equation Approach for Modeling a Single Dot SET

A master equation based model as previously studied by Amman et. al.[63] has been developed to predict the behavior of the SET device. A single dot based SET device can be modeled as two capacitive junctions driven by an ideal voltage source across them. The state of these two junctions can be modeled semi classically and characterized by the voltage across the junction. Figure 2.10 shows a representation of a single dot based SET device by a two junction system. If V_1 and V_2 are the voltage drops across the two junctions and N is the extra electron as supplied by the external circuit, the state of the system can be represented by Eq. 2.3.

$$V_1 = \frac{C_2}{C_1 + C_2} V - \frac{Ne}{C_1 + C_2} - V_p \tag{2.3a}$$

$$V_2 = \frac{C_1}{C_1 + C_2} V + \frac{Ne}{C_1 + C_2} + V_p \tag{2.3b}$$

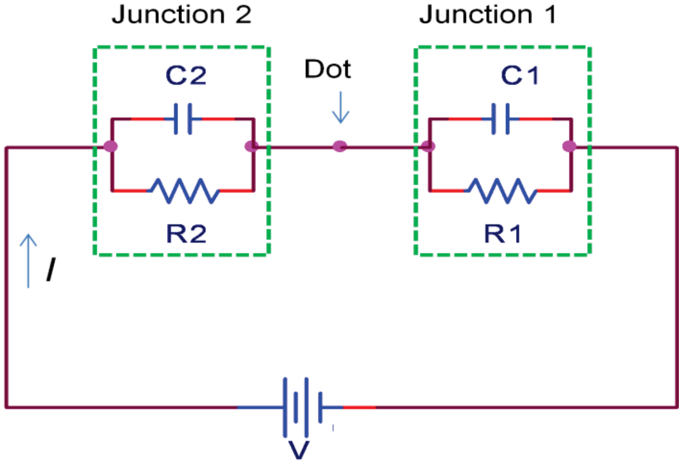


Fig. 2.10: Two junction representation of a single dot SET system. The gate terminal is not shown.

Where C_1 and C_2 are the capacitances of the two junctions respectively and V_p is the additional voltage which represents the misalignment of the Fermi levels in the two consecutive junctions when N and V are zero [65]. The probability $\rho(V, N, t)$, that N electrons are in the middle dot at time t and applied voltage V can be expressed using the master equation as shown in Eq. 2.4 [66,67].

$$\frac{\partial \rho(V,N,t)}{\partial t} = [r_1(N-1,V) + l_2(N-1,V)]\rho(N-1,V,t) + [l_1(N+1,V) + r_2(N+1,V)]\rho(N+1,V,t) - [r_1(N,V) + l_1(N,V) + r_2(N,V) + l_2(N,V)]\rho(N,V,t) \quad (2.4)$$

Where r_i and l_i are the tunneling rates from right and left side respectively for ith junction. To obtain the voltage-current characteristic, a steady state solution of the above Eq. is desired. The steady solution for Eq. 2.4 can be found by assigning the derivative of the probability term as zero which means that for fixed voltage V the probability for

transition to/from a state *N* from/to a sate *N+1* or *N-1* is zero. Further derivation in this approach can lead to express the current as shown in Eq. 2.5 [63].

$$I = \sum_{N=-\infty}^{+\infty} e[r_2(N,V) - l_2(N,V)]\,\rho(N,V)$$
$$= \sum_{N=-\infty}^{+\infty} e[r_1(N,V) - l_2(N,V)]\,\rho(N,V) \tag{2.5}$$

where, $\rho(N,V)$ is the probability of having *N* electrons in the island for a biased voltage of *V*. The tunneling rates r and l for the electron at each junction can be determine from the energy balance equation before and after the tunneling event using orthodox theory as given in Eq. 2.6 [34,39, 40],

$$r_1(N,V) = \frac{1}{e^2 R_1} \frac{E_r - E_m}{1 - e^{-(E_r - E_m)/k_B T}} \tag{2.6}$$

where, E_r is the Fermi energy of the right electrode before the tunneling event and E_m is the Fermi energy of the middle electrode (Quantum dot in our case) after the tunneling event. $E_r - E_m$ is the energy an electron gains during the tunneling event. Assuming that the charge distribution completely relaxes during the tunneling event the energy difference is given by

$$E_r - E_m = -\frac{(2N+1)e^2}{2(C_1 + C_2)} + \frac{eC_2V}{C_1 + C_2} = eV_1(N,V) - E_c \tag{2.7}$$

where, $-\frac{(2N+1)e^2}{2(C_1+C_2)}$ is the change is electrostatic energy of the system and $\frac{eC_2V}{C_1+C_2}$ is the work done by the voltage source. E_c=$\frac{e^2}{2(C_1+C_2)}$ is the charging energy of the system. The above Eq.

can be used to find the tunneling rate in terms of only the applied voltage and the junction parameters. Finally, the characteristic of the device is derived by implementing this tunneling rate in Eq. 2.5. A Matlab code for the model is given in the appendix section. For junction parameters as given in Table 2.1 the V-I plot for the device is shown in Fig 2.11. The junction parameters as given here are derived from the electrostatic analysis of the nano-structure for the device as discussed in Section 2.5 (design section).

Table 2.1 : Parameters used for simulation of a single dot SET device

Device Parameters	Values
C_1	1×10^{-19}F
C_2	1×10^{-19}F
R_1	$2.5 \times 10^{-10}\Omega$
R_2	$2.5 \times 10^{-10}\Omega$
C_g	1×10^{-20}F

The effect of gate voltage can be implemented by evaluating the change in charge distribution with application of the gate voltage. This is incorporated in the model by replacing Eq. 2.3 by Eq. 2.8 as shown below. Here, C_g represents the capacitance associated with the gate electrode and V_g is the gate bias voltage.

$$V_1 = \frac{C_2}{C_1 + C_2 + C_g} V - \frac{Ne}{C_1 + C_2 + C_g} - V_p - \frac{C_g}{C_1 + C_2 + C_g} V_g$$
$$V_2 = \frac{C_1 + C_g}{C_1 + C_2 + C_g} V + \frac{Ne}{C_1 + C_2 + C_g} + V_p + \frac{C_g}{C_1 + C_2 + C_g} V_g \qquad (2.8)$$

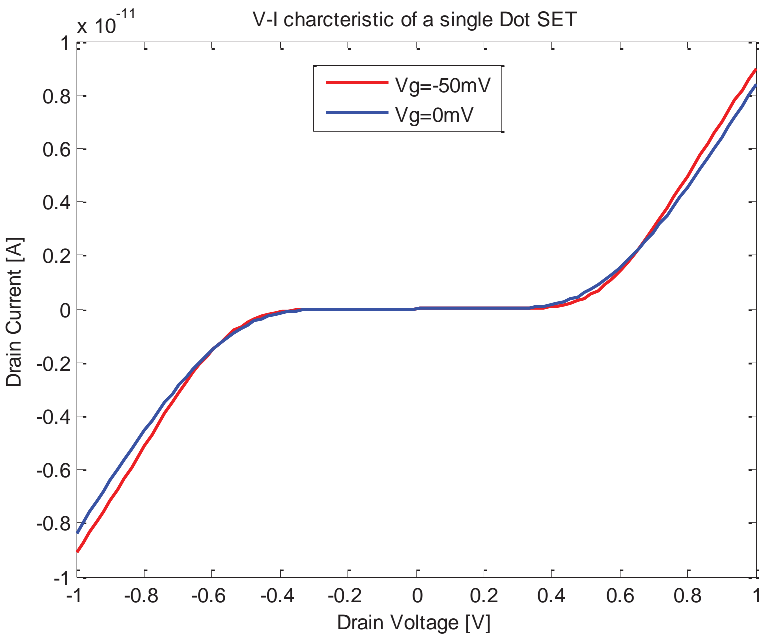


Fig. 2.11: Simulated V-I characteristic for a double junction SET device using master equation model. The parameters for the simulation is input from Table2.1

2.4.2. Soliton Model for Multi Dot SET

In case of a multi-dot device, more than two tunnel junction takes part in the current conduction process. Hence, above mentioned master equation based model cannot predict its behavior. The device characteristic for a multi dot SET can be explained by using a charged soliton model. To implement this model, it is assumed that the electron transport takes place in a one dimensional array of tunnel junctions. This assumption is generally thought to be valid for the investigated device with two dimensional distribution of quantum dots, as the electron transport in such a device takes place in a single dominant conducting path [45,46]. This approach follows the model developed by Karre et. al. [69] with a change

in total current taken directly from any junction instead of adding the current for all the junctions.

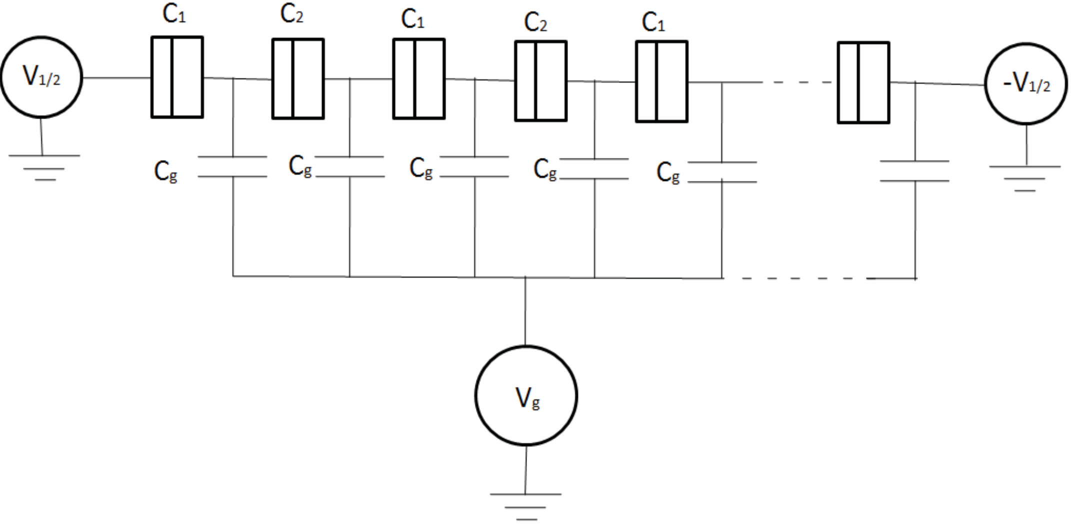


Fig. 2.12: Modeling the multi dot SET with an array of tunnel junctions of capacitance C1 and C2 biased by a voltage V. The gate coupling can be represented by the gate voltage Vg and gate capacitances Cg for each dot.

Considering an array of N tunnel junctions with the capacitance of alternating junctions to be C1 and C2 and the gate capacitance, *Cg*, the schematic of the device can be given as shown in Fig 2.12. The inter-dot capacitance between the next nearest neighbor and further neighboring dots are neglected. The injection of an electron into an array of conducting islands modulates the charge in the system as the electron tunnels from one conducting island to the next. The charge on the conducting island is varied and the neighboring conducting islands are polarized by the presence of the extra charge on the conducting island. The array of the junction is assumed to be homogeneous, which means the tunnel junction and the self capacitance of all the dots are uniform $(C_1=C_2=C)$. The

junction array is driven by a bias voltage V. When one electron is injected in to the junction array it disturbs the electrostatic of the system and creates a potential distribution which can be represented in the form of a charge soliton. The entrance of one soliton in to the array reduces the probability of entering another soliton entering [35,68].The repelling force between the soliton and the biased edge drives the propagation of the charge soliton in to the array and to the other end of the array, thus creating the Coulomb blockade effect [69]. The voltage distribution in the junction array is also driven by this solitary motion of the electron. The potential of an arbitrary island $\boldsymbol{i}$ as function of distance from a charge containing island can be calculated to be Eq. 2.9 [64].

$$V_i = \frac{e}{C_{eff}}\left[exp\left((-|i-k|)\cosh^{-1}\left(1+\frac{C_g}{2C}\right)\right)\right] \tag{2.9}$$

Where, $C_{eff} = \sqrt{C_g^2 + 4CC_g}$. The potential falls off with a characteristic decay length. The above expression for the potential enables the determination of the potential difference in any two islands in the junction array. Hence, knowing the probability of electron tunneling between those islands by the master Eq. method and implanting the potential distribution in the model as described in the previous section, the V-I characteristic of the device can be determined. The Matlab code to simulate the V-I characteristic by this method is given in the appendix section. The simulated V-I characteristic of a multi dot device is shown in Fig 2.13. The parameters used for the device simulation are listed in Table 2.2.These parameters are extracted from the experimental device characteristic as explained in section 5.1.

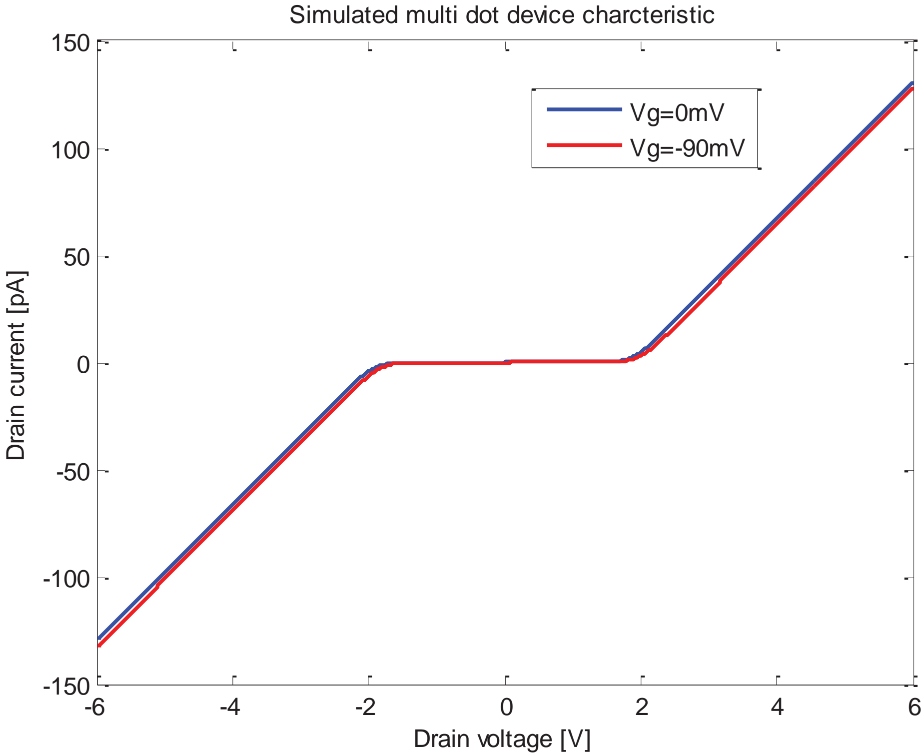


Fig. 2.13: Simulated V-I characteristic of a multi dot SET device with 10 junctions in the dominant conducting path (DCP).

It is seen from the simulated I-V characteristics in 2.13 that a clear Coulomb blockade effect is observable. It can also be observed that the blockade length for the soliton based multi dot SET is larger than for a single dot SET which could be due to the multiple junction's capacitance which adds up in series and hence increases the charging energy and the blockade length. The simulated drain currents are of the order of tens to hundreds of pico amperes (pA). From the simulated source drain characteristics of the multi dot SET system, it can be concluded that the device behavior can be predicted using the soilton

model, although a more realistic model is required to predict the impact of randomness in the position and size of the dots on the device characteristics.

Table 2.2 : Parameters used for simulation of a multi dot SET device

Device Parameters	Values
$\boldsymbol{C_1}$	2.5×10^{-19}F
$\boldsymbol{C_2}$	2.5×10^{-19}F
$\boldsymbol{R_1}$	$2.8 \times 10^{-10}\Omega$
$\boldsymbol{R_2}$	$2.8 \times 10^{-10}\Omega$
$\boldsymbol{C_g}$	2×10^{-20}F
$\boldsymbol{N}$	10

2.5. Design of Single Electron Transistor Device

A single electron transistor consists of one or multiple nano-islands capacitively coupled to the source, drain and gate electrode and/or to each other. The value of the junction capacitance and the tunnel resistance has to satisfy the working conditions as given in Eq. 2.1 and 2.2 to make the SET operable at room temperature. The magnitude of these parameters solely depends on the device design, the size and configuration of the nano structure in the active area of the device. In addition, an optimized design is also important to improve the functionality of the device.

The Single Electron Transistors (SETs), in the present work are fabricated using Focused Ion Beam (FIB) processing. Both FIB etching and FIB deposition methods have been investigated for the fabrication of SET devices. The present section describes the design of SET devices, based on the feature size that can be fabricated using FIB etching and deposition capabilities of the Hitachi FB-2000A FIB instrument. The two important design targets for the current work are:

- ✓ Room temperature operation of the SET device;
- ✓ Improved device functionality.

For room temperature operation of the device, the charging energy $E_c \left(= \frac{e^2}{2C_{eff}}\right)$ has to be greater than the thermal energy at room temperature, which is ~26mV. This requires the effective capacitance, C_{eff}, to be in the order of few aF. The effective capacitance C_{eff} can consist of the junction capacitances and the self capacitance of the nano-island. All these capacitances must be on the same order to make room temperature operation possible. The capacitance of the island is the dominant factor, and hence by reducing the capacitance of the island, the overall capacitance of the device can be minimized. The resistances of these junctions are also important, and have to be more than the quantum resistance, R_Q~ 26kΩ. The design of the device should include all the above factors in order to achieve the room temperature operation of the SET device. The value of the capacitance and the resistances of the devices depend on the dimensions and the structural design of the device. In the current investigation, the nano-islands which are the most critical part for a functional devices have the average size of ~8nm. Also, from the previous study [69] it is observed that the width of the tunneling barrier which can be formed by chemical oxidation of these islands is ~1-2nm.

Considering these parameters, the structure for the SET device is designed as shown in Fig 2.14.

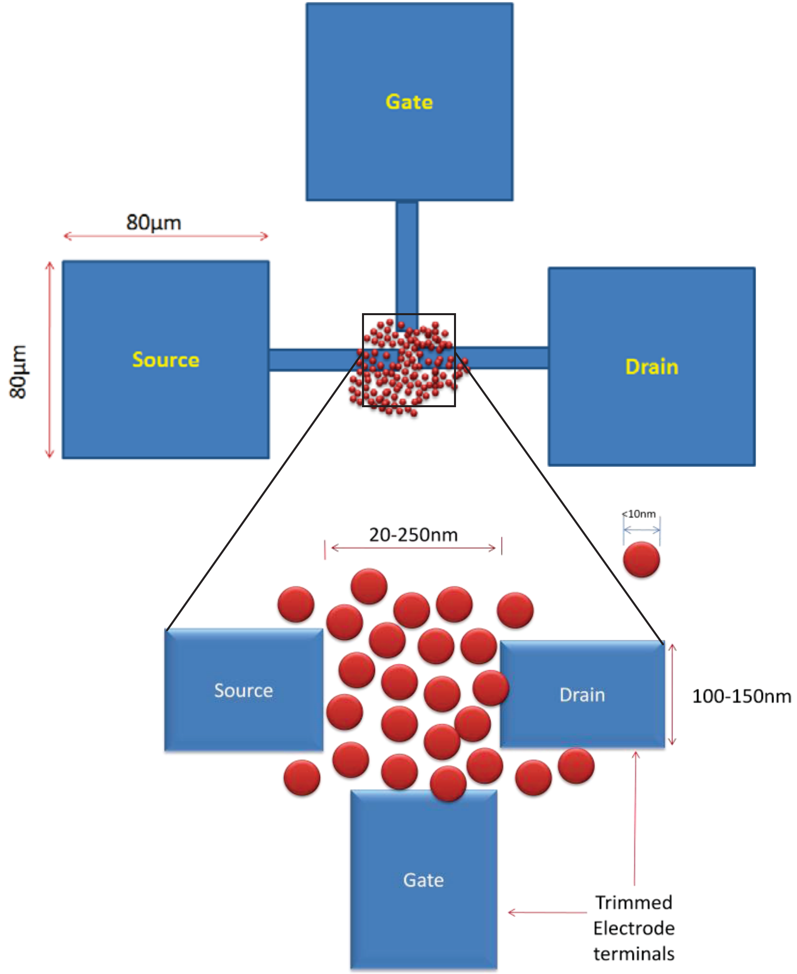


Fig. 2.14: Design of the investigated SET device

The designed devices are multi-dot based SETs, where the electron transport occurs through arrays of tunnel junctions which result in inter-dot capacitances and the capacitances between the electrode terminals and the dots. These capacitances are calculated using electrostatic theory [70] to examine the room temperature operating conditions. This

calculation approximates that the nano-islands are spherical in shape and there is no effect of the surrounding nano structure on the capacitance.

The capacitance between two neighboring dots can be calculated from an approximated structure, as shown in Fig 2.15. Assuming that the nano-islands are spherical in shape, the inter-dot capacitance can be calculated according to Eq. 2.10 [70]:

$$C = \pi\epsilon\sqrt{(d^2 - 4a^2)}\sum_{j=0}^{\infty}\left(\coth\left[(j+1)\cosh^{-1}\left(\frac{d}{2a}\right)\right] - 1\right); \qquad (2.10)$$

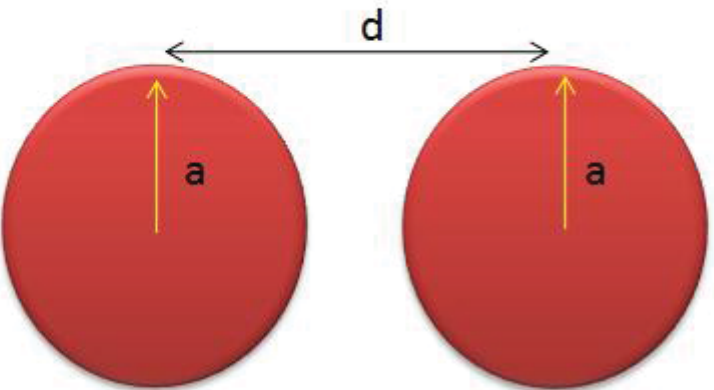


Fig.2.15: Schematic for computation of the capacitance between two neighboring islands in the active area of the SET device.

where, d is the distance between the centers of two dots, a is the radius of each dot, and ϵ is the permittivity for the dielectric media between the two dots. The other capacitance required for the overall device capacitance is the capacitance between the electrode terminals

and the nano islands. The minimum width of the electrode terminal used for the device structure is 100nm and the average diameter of the nano islands is ~8nm. Hence, capacitance between the electrode terminal and the nano islands can be calculated by approximating an arrangement as shown in Fig 2.14. The capacitance for such a structure can expressed as shown in Eq. 2.11 [70]:

$$C = 2\pi\epsilon\sqrt{(d^2 - 4a^2)}\sum_{j=0}^{\infty}\left(\coth\left[(j+1)\cosh^{-1}\left(\frac{d}{2a}\right)\right] - 1\right); \tag{2.11}$$

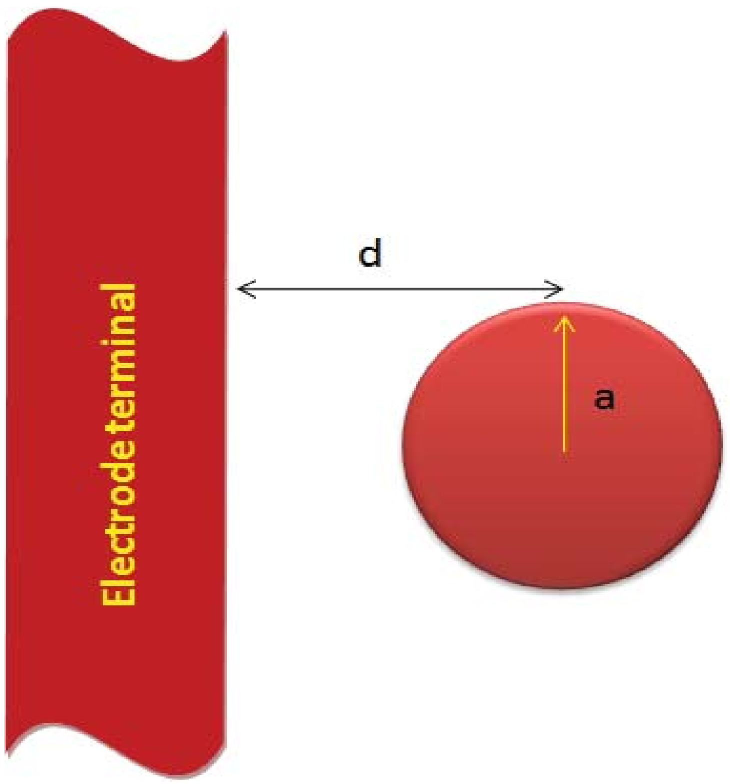


Fig. 2.16: Schematic for computation of the capacitance between island and the electrode terminals

The calculated value of the inter-dot capacitance and the capacitance between the electrode terminals and the nano-islands are given in the appendix section. It can observed that these capacitance below in the order of 10^{-18}F which confirms the room temperature operation.

In addition to room temperature operation, the other requirement of the device design is to improve the functionality of the device. The functionalities of the device to be improved include

- ✓ Reducing the threshold voltage
- ✓ Increasing device density

- ✓ Increasing the gate controllability.

The threshold voltage for a device is basically defined as the voltage at which the device switches from the blockade region to the non-blockade region in the V-I characteristic. A lower threshold voltage is essential for the application of the device in low power electronics. Quantitatively, it is half of the Coulomb blockade length of the device. Hence, a reduction in threshold voltage requires reduction in charging energy and an increase in overall capacitance of the device. In multi dot SET devices like ours, the overall capacitance of the device is composed of the self capacitances of the dots and the junction capacitances of the multiple junctions which are connected in series. An increase in the number of junctions (nano-islands) in the dominant conducting path increases the series capacitances and hence decreases the overall capacitance. Thus, the charging energy and the threshold voltage is increased. Hence, to minimize the threshold voltage, the number of nano-islands has to be reduced. This is achieved by minimizing the gap between source and drain electrode. This minimization of inter-electrode gaps can also help in increasing the device density by decreasing the size of the active area. The gate controllability for the device is improved by using semiconductor nano-islands for the electron tunneling.

Chapter 3: Fabrication of Single Electron Transistor

Focused Ion Beam (FIB) technology is utilized to fabricate Single Electron Transistors (SETs) operating at room temperature. Both FIB etch and deposition technology is used in realization of the room temperature operating Single Electron Transistors (RT-SETs). The limitations due to tail energy overlapping and localized heat generation restricts the FIB etch technology to realize structure below 40nm [71]. This makes the FIB etching process alone unsuitable for fabrication of room temperature operating SETs [69]. Fabrication of sub 10nm quantum dots by FIB deposition process and realization of RT-SETs by this method has been previously demonstrated [69,72]. However, due to resolution limits in the deposition process, devices fabricated by this method are still far from the optimum when functionalities are concerned. Hence, process technology using both FIB etching and deposition process is utilized to fabricate RT-SETs to overcome the limitation in the deposition only process.

This chapter explains the process technology developed for fabricating RT-SETs using FIB etch and deposition process. General previews about the FIB etch and deposition technology is presented in Section 1. Section 2 is dedicated for describing the process

integration for fabricating the RT-SETs. Optimization and development of processes for fabricating devices with different structural and topological variation is described in Section 3 and 4, respectively.

3.1. Focused Ion Beam Technology

The Focused Ion Beam (FIB) technique was developed during the late 1970s and the early 1980s. The first commercial FIB instruments were introduced more than a decade ago [73]. With shrinking device size, positional and dimensional accuracy are critical parameters for suitable fabrication technologies. The FIB technology enables localized milling and deposition of materials with high precision. It is therefore, widely used in device modification, mask repair, process control and failure analysis [73-78]. Apart from its application in circuit modification and failure analysis, FIB technology has proven to be a very useful candidate for nano scaled fabrication [78-81]. This section describes the FIB technology in general and discusses the capability of FIB etching and deposition technology for fabricating nanostructures for various applications.

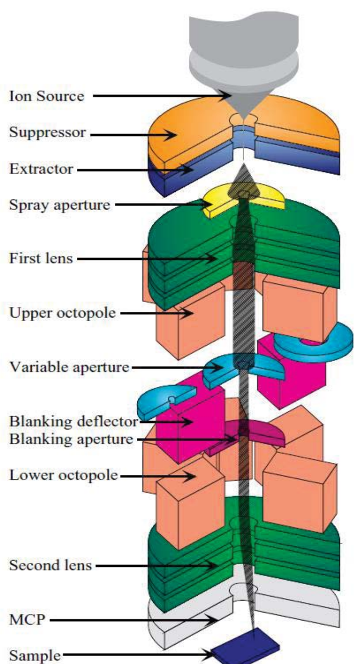


Fig. 3.1: (Left) Hitachi FB-200A FIB system.(Right) The Schematic diagram of FIB Column[The right image is reprinted with permission from S. Reyntjens and R. Puers, J. Micromech. Microeng Vol. 11 p287 (2001), © 2001 Institute of Physics]

The operation of FIB systems is similar to that of Scanning Electron Microscopy (SEM) systems. The primary difference is the use of a highly focused ion beam (commonly Ga+) instead of an electron beam as in a SEM. The FIB system can perform three different applications: Etching, Deposition and Imaging. In modern FIB systems, the spot size of the ion beam can be less than 10nm, which makes this system a suitable candidate for fabricating structures in the sub-100nm regime [82]. This beam can be scanned in a controlled manner to selectively modify the surface of a sample and to image the sample. The basic features of the FIB system are shown in Fig. 3.1 and the principle of its operation in different modes is shown in Fig. 3.2.

The basic FIB tool consists of a vacuum system and chamber, a liquid metal ion source (LMIS), an ion column, a detecting system and a computer based control system [83]. The Ga^+ ions are generated from the LMIS by an extraction voltage. The LMIS has capability to produce an ion source ~5nm in diameter [84]. Once the Ga+ ions are extracted from the LMIS they are accelerated through potential down the ion column. Typically the accelerating voltage ranges from 5-50KeV [83]. The accelerating voltage for the Hitachi FB-2000A system we used for the device fabrication is 30keV. The ion column typically has two lenses; condenser lens for probing the extracted ions, and an objective lens to focus the ions at the sample surface. A set of apertures of various diameters are used to define the probe size of the beam and provide a range of ion currents which can be used for different applications. The alignment of the beam is done by a set of deflectors in the ion column.

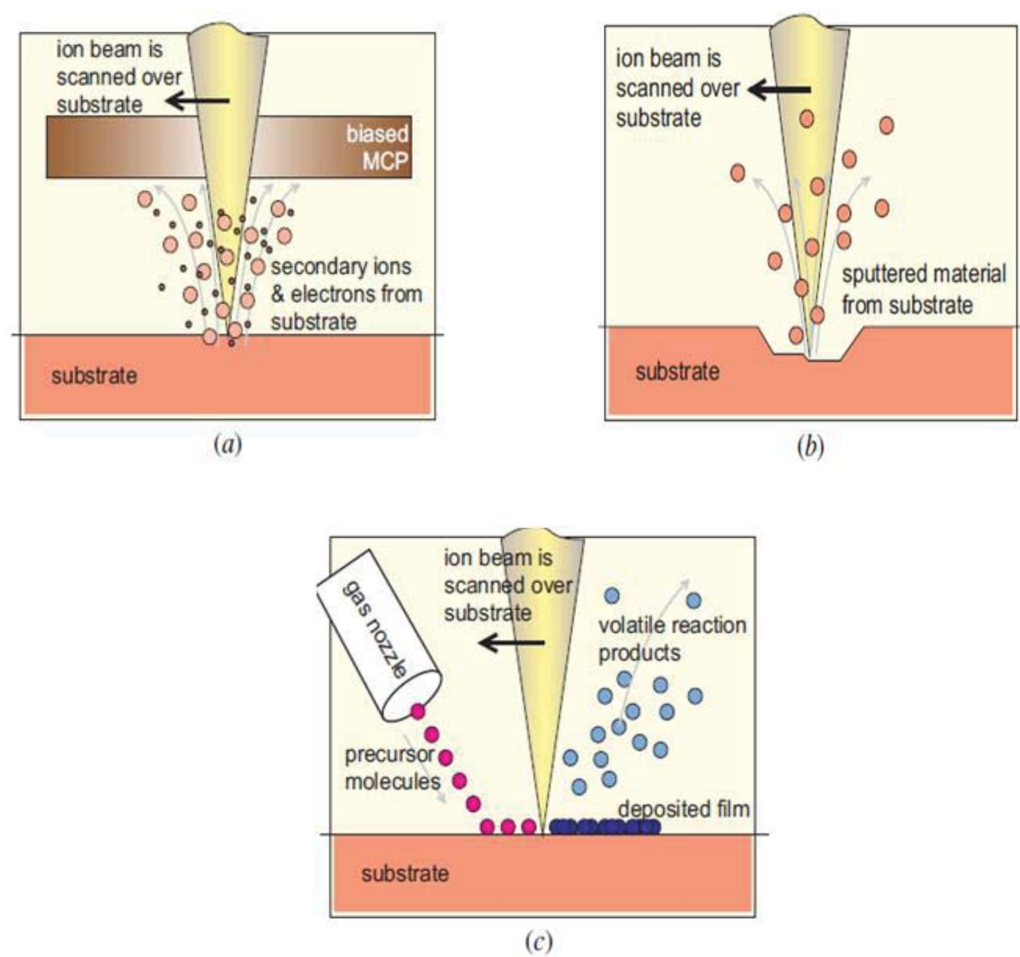


Fig. 3.2: The basic principle of FIB operation (a) Imaging (b) Etching (c) Deposition [Reprinted with permission from S. Reyntjens and R. Puers, J. Micromech. Microeng Vol. 11 p287 (2001), © 2001 Institute of Physics]

The Hitachi FB-2000A FIB system has different beams available for various applications. The beams are defined by the beam number. The higher the beam number, the higher is the current and the diameter of the beam. In Hitachi FB-2000A FIB system, all the beams are divided in two modes; milling mode (MI) and observation mode (MO). The beams in the observation modes have lower current and smaller spot size than those of the beams for milling mode. The milling beams are defined as MI-500 to MI-6 and the

observation beams are MO-50 to MO-6. The beam current range from 1pA to 20nA [85]. For most of the etching related applications, the MI beams are used, with the MO beams used for imaging applications. The variation in the beam parameters for different beams in a Hitachi FB-2000A FIB system is presented in Fig. 3.3.

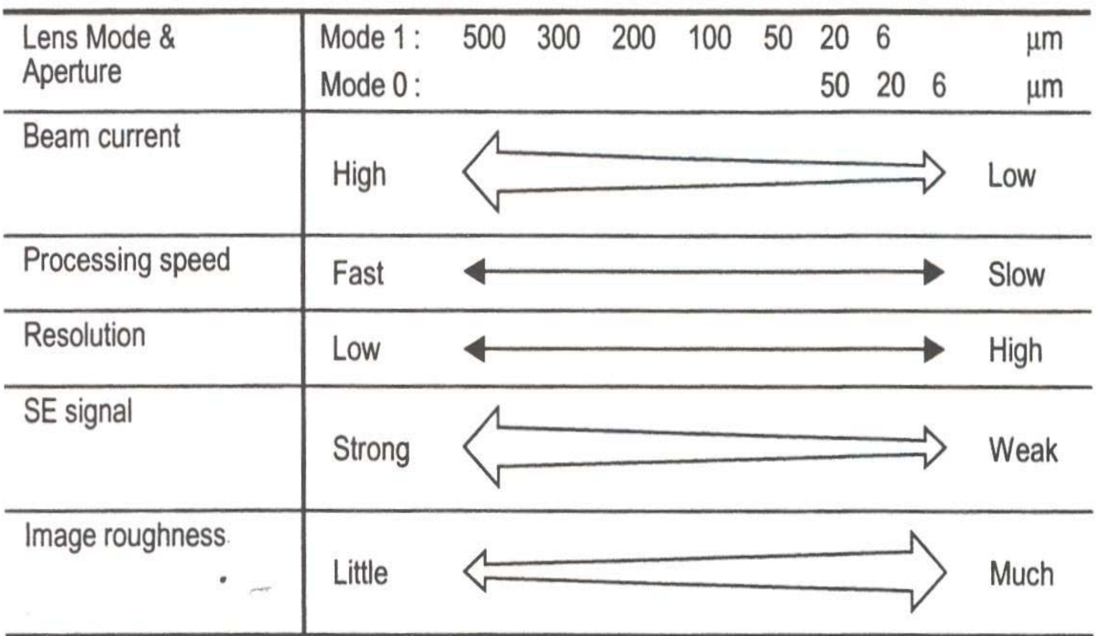


Fig. 3.3: The variation in the beam parameters and capabilities for different beams in the Hitachi FB-2000A FIB System (Source: Hitachi FIB manual).

During FIB processing, different beams are used for fabricating different structures depending upon the dimension of the intended structure. Beams with higher current and larger diameters can be used for fabricating microstructures and beams with lower current and diameter are used for fabricating nano structures. For fabricating the entire device structures for the RT-SETs, both higher and lower beams are used. Table 3.1 gives the details about different beams and their main applications. The present chapter deals with the fabrication technology for RT-SETs using FIB etching and deposition. The limitation of the

FIB etching process is analyzed and an effective optimized process is developed to fabricate sub-20nm nano structure for the RT-SETs. The FIB deposition process is used for fabricating quantum dots and devices with alternative topologies.

Table 3.1: Hitachi FB-2000A Focused Ion Beam System Beam details

Beam Name	Lens Mode	Aperture Diameter	Indicated Beam Current	Main Usage
L.Scan				Low-mag observation
M1-500	Mode 1	500 μm	11.0—15.0 nA	Coarse processing
M1-300	Mode 1	300 μm	4.0—8.0 nA	Coarse processing
M1-200	Mode 1	200 μm	2.0—3.5 nA	Coarse/medium processing
M1-100	Mode 1	100 μm	0.400—0.800 nA	Medium processing
M1-50	Mode 1	50 μm	0.100—0.300 nA	Finish processing
M1-20	Mode 1	20 μm	0.015—0.040 nA	Finish processing
M1-6	Mode 1	6 μm	0.001 —0.005 nA	Observation
M0-50	Mode 0	50 μm	0.020—0.050 nA	Finish processing/observation
M0-20	Mode 0	20 μm	0.004—0.010 nA	Observation
M0-6	Mode 0	6 μm	0.000—0.002 nA	Observation

3.1.1. Focused Ion Beam Etching

The FIB etching process is utilized to fabricate the nano electrodes and micro pads for the RT-SET devices. The resolution limit of the etching process for fabricating the nano structures of desired dimension and the developed technique to address this resolution limit will be discussed in this section.

The etching of a material is achieved when the highly energetic ion beam strikes the sample surface and removes the material atoms from it. The process of removing these material atoms from the sample is called the sputtering process. The rate of etching for a particular material can be characterized by the sputtering yield as defined in Eq. 3.1.

$$Sputtering\ Yield\ (S) = \frac{No\ of\ Target\ atoms\ removed\ from\ the\ sample}{No\ of\ Ions\ impinged\ in\ to\ the\ sample} \quad (3.1)$$

The sputtering yield depends on the target material and the angle of incident of ion beam. The sputtering yield reaches its maximum when the incident angle is between ~75-85 degrees. In addition to the material and incident angle, phenomena like back sputtering and ion channeling also significantly impact the sputtering yield. Although the sputtering yield can give an idea for the rate of material removal from the sample surface, it is not the direct measure of the milling rate for the FIB etching process. Effects like localized heating, sidewall re-deposition, and tail energy overlapping impacts the characteristics of the FIB etching process [83].

The total material removed from a sample depends on the total number of ions impinged on the sample surface. As the number of ions increases with beam current, the rate of material removal is higher for higher beams. Therefore, the fabrication time for beams with higher current is much lower than that for beams of lower current. However, the beam diameter and hence, the spot size of the higher current beams is larger than that of the lower current beam, which makes the higher current beams unsuitable for realizing high resolution structures.

3.1.2. Single Dot Based SET by FIB Direct Writing

The RT-SETs fabricated using FIB deposition process has 8-10 conducting nano islands between the source and drain electrode and gives a threshold voltage of ~1.6V. As discussed in the previous chapter, improvement in the threshold voltage requires minimization of source drain gap to minimize the number of nano-islands participating in the conduction process. This section will explain the utilization of FIB etching process for fabricating nano structures to realize the RT-SETs with minimum number of conducting islands between the source and drain electrodes. The most ideal condition would be to have just one island in between the source and drain electrode. FIB etching based direct writing technique could be utilized for fabricating the nano structure for single dot based SETs [71]. However, room temperature operation of this device requires the conducting island to be less than 10nm in size. In the previous work by Karre et al. [69] it is observed that effects like tail energy overlapping and localized heat generation during FIB etching limits its capability to fabricate structures below 40nm. To address this limitation, a modified method in the FIB direct writing technique is explored to realize a single dot based SETs with a nano island of size below 10nm.

The SET devices are fabricated on a Cr layer on Si/Al_2O_3 samples. The FIB direct writing technique is used to fabricate the nano structure as shown in Fig. 3.4, in the Cr layer to realize the SET device. The active area of the device was made up of a central conducting island separated from the source and drain terminal by very thin tunnel junctions. Targeting a nano island of size below 10nm, a modified patterning approach has been made to overcome the resolution limit due to the energy overlapping effect in the process. The SET device consists of both micro and nano structures. The nano structures are required for the

active area and the microstructures are required for the probing pads and connecting electrodes. The processing time and resolution of the targeted structure in the FIB etching process solely depends on the beam current and the diameter of the beam. In the Hitachi FB-2000A FIB system beams like MI-500, MI-300, etc, which have a larger beam current and diameter are used for fabricating the probing pads and connecting electrodes. The beams like MO-20, MO-06, etc, with lower beam current and smaller diameter are used for fabricating the nanostructures in the active area.

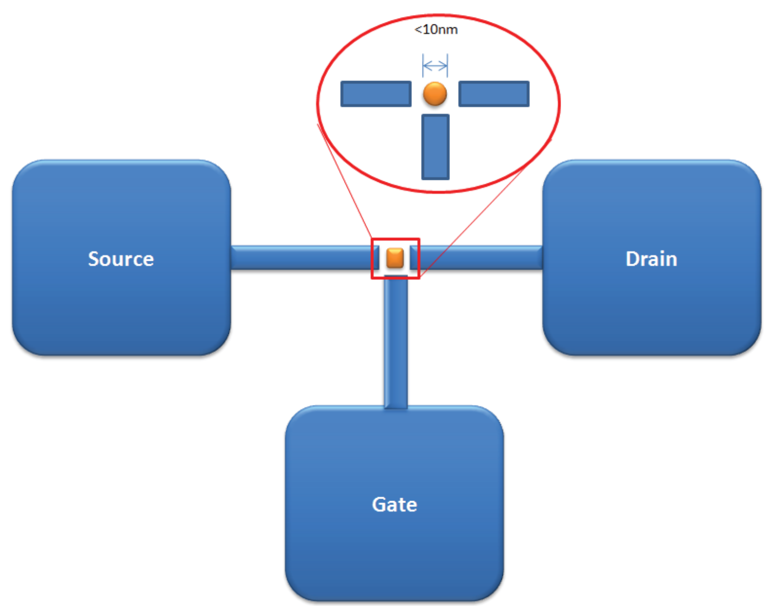


Fig. 3.4: Schematic diagram of the proposed Single dot based SET by FIB direct writing technique.

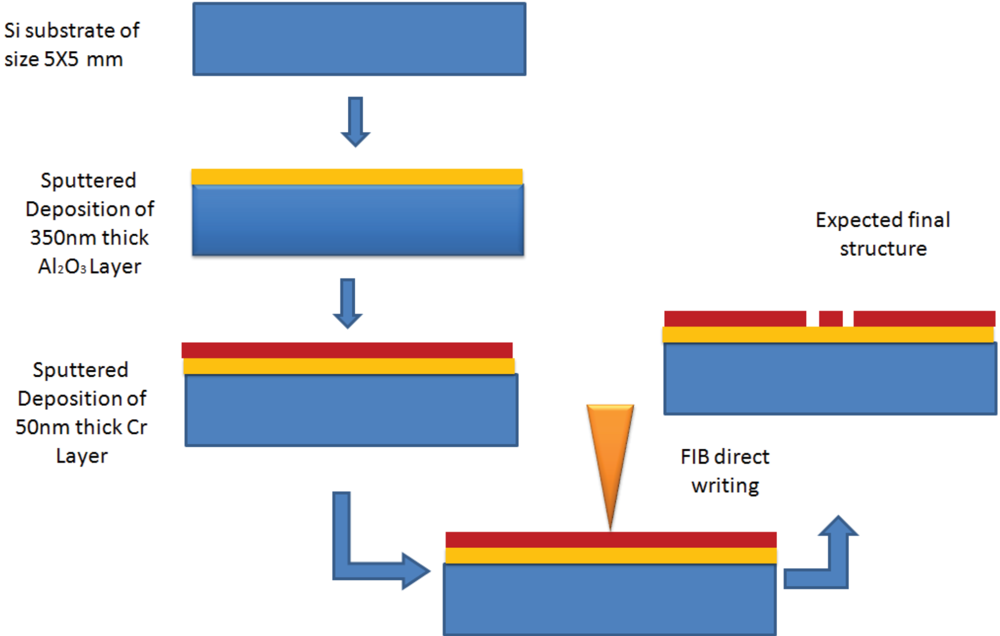


Fig. 3.5: Process Flow for fabricating the nano structure for a single dot based SET by FIB direct writing technique.

The process flow for the single dot based SET device fabrication using FIB direct etching technology is given in Fig. 3.5. In the first step, silicon samples of size 5mm × 5mm are made by dicing a 6" silicon wafer using the Microautomation 1100 dicing saw instrument. The size of the samples are limited to 5mm × 5mm as the maximum size of a sample that will be fit a standard sample holder for the FIB system. The silicon samples are thoroughly cleaned in piranha solution (1:1:1 H_2S_4: H_2O_2:DI water) and then rinsed in de-ionized water. Deposition of the thin film layers on the silicon sample is done by using a physical sputtering process. The samples are introduced to the Perkin Elmer 2400-8J parallel plate RF sputtering system for depositing a 350nm thick Al_2O_3 layer. The deposition process is initiated when the chamber pressure reaches below 10^{-7}Torr. The required time for the deposition was 100min. To avoid overheating the sample and hence to produce uniformity in the deposition rate, the deposition was done in three steps with a certain time interval for cooling the sample holder. The Al_2O_3 layer is used to isolate the device from the silicon substrate. The devices are fabricated in a Cr layer which is deposited on this Al_2O_3 layer. In this step, the samples are introduced into a Perkin Elmer 2400-6J system for depositing a 50nm thick Cr layer. The process parameters for the deposition of Cr and Al_2O_3 layers are given in Table 3.2.

Table 3.2: Parameters for the deposition process of Al_2O_3 and Cr layer

Process Parameters	**Material 1**	**Material 2**
Deposited Material	Chromium (Cr)	Alumina (Al_2O_3)
Process Tool Used	Perkin-Elmore 6" 2400J	Perkin-Elmore 8" 2400J
RF Power	100 W	1000 W
Reflected Power	<10 W	<100 W
DC Bias	-450 V	-465 V
Substrate Bias	0 V	0 V
Process Pressure	6.2 m Torr	14.2 m Torr
Gas Flow	Ar:10SCCM	Ar: 20 SCCM O_2: 4 SCCM
Process Temperature	300^0 K	300^0 K
Deposition Time	5mins	100mins

These samples are then introduced to Hitachi FB-2000A FIB system for fabricating the SET device, the measuring pads and connecting electrodes. The fabrication process of nanostructure for the device in the FIB system can be divided into 3 stages. They are:

- ✓ Pattern Generation
- ✓ Electrode and Pad formation
- ✓ Quantum Island and tunnel junction formation.

The pads and the electrodes for the device are formed in the Cr layer by isolating a patterned area from the rest of the sample as shown in Fig. 3.6. The pattern for the fabrication of these structures can be done either by a CAD input through the Nano Pattern

Generation System (NPGS) or directly by drawing the pattern through the onboard software in the Hitachi FB 2000A FIB system.

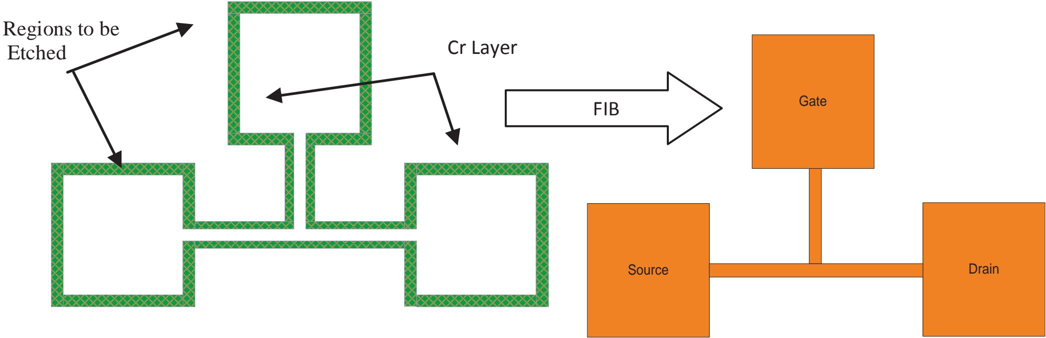


Fig. 3.6: Pictorial view of (Left) generated pattern for Pads and Electrodes fabrication. (Right) Expected Pads and electrodes before the gap formation.

The NPGS-CAD system is very flexible in handling the complexity of the input pattern. However, in nano scale regime the controllability and pattern alignment are major challenges in transferring patterns through the NPGS-CAD system. For the targeted SET device, the structure is very simple but the dimensional accuracy is very important. This motivates us to use the on-board software for pattern transfer rather than the NPGS-CAD system. Two different patterns are generated in the FIB system: one is for forming the device pads and electrodes, and the second is to fabricate the nano island and the tunnel junctions. The etching using the FIB can be done by two different modes of beam scanning: 1.Raster Scan, and 2.Vector Scan. For scanning a particular pattern, the raster scan mode makes the beam to scan all over the area at a time. However, during vector scan mode the beam covers the whole pattern in a line-by-line fashion. Hence, raster scan mode is much faster and efficient, whereas vector scan mode generally gives better resolution since the line width of the pattern

can be controlled. For the pad formation, the raster scan mode was preferred, as the process time and conformity of the fabrication is more important than resolution of these feature. Selection of the desired mode is done before pattern generation. During the pattern generation, a marker is usually fabricated near the nano structures. This helps to find the structure in the sample while doing the characterization through a scanning electron microscope.

Once the pattern is generated, the parameters for the etching process are input to the FIB system to fabricate the pads and the electrodes. Beam MI-500, which is the beam with highest current available in the FIB system is used for fabricating the pads and outlining the electrodes. The width of the electrodes formed by this initial stage of fabrication is around 1-1.5 μm. These are further trimmed to 100~200nm (only at the terminals) in the next stage. Beam MO-50 is used for the trimming process. Again, as resolution is more important here, the vector scan mode is used for this electrode trimming process. Now the sample is ready for the nano structure fabrication of the active part of the device. The parameters used for this fabrication process is listed in the Table 3.3.

In the previous research it was observed that the energy overlapping in the tail region in the FIB etching process limits its ability to fabricate the nano-island of size below 40nm. Considering this fact, a different approach was made by modifying the layout of the desired nano structure for the active area of the device. The old and new layouts for fabricating the SET devices are given in Fig. 3.7.

Table 3.3: FIB process parameters for fabrication of the micro/nano structure for the single electron transistor.

FIB Process Parameters	Structure 1	Structure 2	Structure 3
Fabricated Structures	Probing Pads	Electrodes and Terminals	Nano structure for the Active area
Used Fabrication Mode	Raster Scan	Vector Scan	Vector scan
Beam Used	MI500	MO50	MO06
Beam Current	11-15nA	0.02-0.05nA	~1.5pA
Dwell Time (in µs)	0.5	50	30
Fab Time/Frame Number	~20mins/--	5mins/300	0.6mins/70
Pattern/Line width	10µm/--	--/5	--/2

In the fabrication of the central nano-structure, a T-shaped structure is etched to form the source, drain and the gate electrodes further. This is done by trimming the already fabricated micro electrodes by the MI-50 beam in the Hitachi FB-2000A FIB system. A nano island is intended to form by etching the rectangular pattern on the T-shaped structure as shown in Fig. 3.7(b). The rectangles are etched one by one with an intention to avoid energy overlapping in the tail region. The size of the fabricated nano-island depends on the size of these rectangles. For the targeted nano island of size <10nm, the required size of rectangle must be 20nm (the smaller arm of the rectangle) or less. The expected structure is shown in Fig. 3.7(b). An improvement in the resolution is expected as the energy

overlapping effect is expected to be reduced due to the time gap between the etching of each rectangle. However, it is observed that the resolution did not improve substantially. The minimum diameter of the dot that could be fabricated was ~30nm with a junction width of ~25nm. The reason for this lower resolution can be attributed to the instability in the beam alignment for repeated processing. It was observed that for a lower current beam like MO-06 in the Hitachi FB 2000A FB system the beam loses its alignment each time it runs a process. Hence, exact alignment for all of the four rectangles is difficult to produce. This can be a possible reason for not obtaining substantial improvement in the resolution even in the modified layout approach.

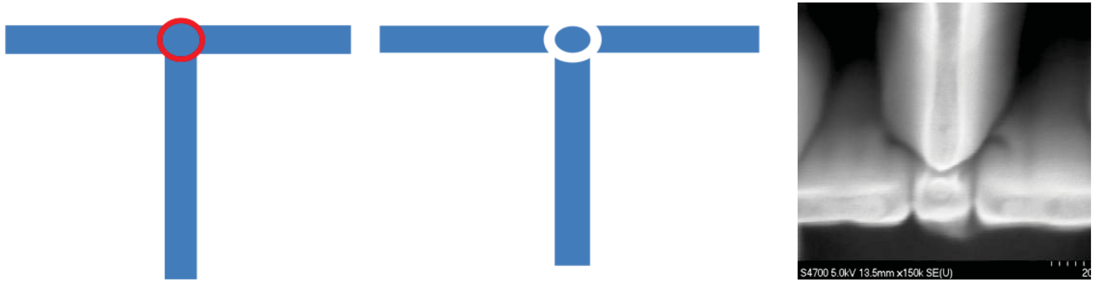


Fig. 3.7(a): Old layout (developed by Karre et al [69]) with the SEM image of the minimum structure possible.

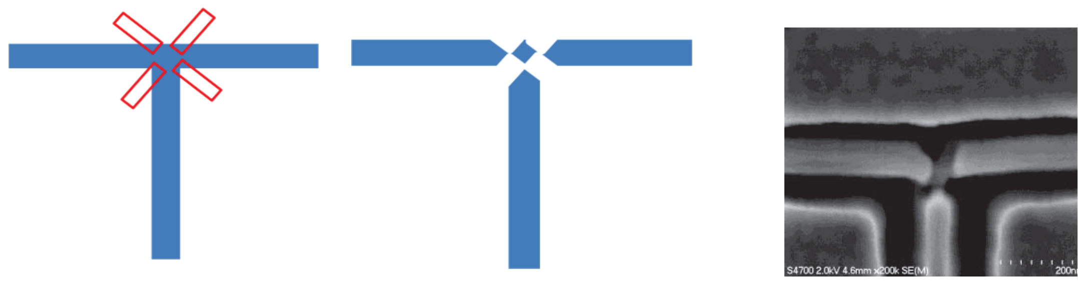


Fig. 3.7(b): New layout with the SEM image of the obtained nano structure.

The failure of FIB direct write technique for fabricating nano structure for the RT-SETs, with a single nano-island motivate the exploration of different approaches for the realization of RT-SETs with minimum possible dots in dominant conducting path. As described in the previous chapter, another efficient way of minimizing the number of participating dots in the RT-SET system is to minimize the gap between the source and drain electrodes and deposit the nano islands between them. In this way, if an inter electrode gap of size comparable to the size of the nano-island can be archived, a SET device with just 1-2 dots participating in the conduction process can be realized. The deposition of the nano islands of size below 10nm can be achieved by FIB deposition process as developed in

previous work by Karre, et al. [69,72]. This deposition process is discussed in the following section.

3.2. Material Deposition and Fabrication of Nano-islands by FIB

FIB enables localized and mask less deposition of both metals and insulator materials [79]. The material deposition process is similar to a gas phase chemical vapor deposition process and the occurring reaction is comparable to, for example, laser induced CVD [86, 87]. However, the resolution for the FIB deposition is much higher than that for the laser induced CVD. In the Hitachi FB-2000A FIB system that is being used in this study, W is the only material that is configured for deposition. The W deposition takes place when the ion beam strikes the $W(CO)_6$ precursor gas adsorbed on the sample surface. The $W(CO)_6$ precursor is generally obtained form a solid source that can be heated to a specific temperature, depending on the process. To optimize the precursor flux available for FIB induced material deposition, the precursor injector must be positioned as close to the deposition area as possible and must be oriented such that the precursor impinging on the area is maximized.

Apart from the position of the precursor injector, the rate of deposition is dependent on parameters like the beam current, dwell time, refresh time, and the deposition area. According to a model developed by *Rüdenauer* and *Semerad* [88], the deposition process can be modeled by the occurrence of the following simultaneous sub-processes:

- ✓ Adsorption of precursor gas from the gas phase onto the growing deposit.
- ✓ Ion beam induced fractionation of adsorbed precursor molecules into a permanently adsorbed metal containing molecule and a volatile component.
- ✓ Ion beam sputtering of adsorbed precursor gas.
- ✓ Ion beam sputtering of previously permanently deposited metal molecules.

However, the net deposition rate is the result of the competition between the deposition and the sputtering process [89]. For fabrication of a continuous film, the deposition has to dominate over the sputtering. For fabrication of a discontinuous film and nano islands, the sputtering process has to dominate the deposition process [69]. The deposition yield (*Y*) for a material during FIB deposition process can be given by Eqn. 3.2 [90].

$$Y = {WLZ}/{I_B t} \tag{3.2}$$

Where, *L, W,* and *Z* are the length, width and height of the deposited film respectively. I_B is the beam current and t is the total time of deposition. From Eq. 3.2 it can be observed that the deposition yield depends on the size of the intended pattern, the beam current and the deposition time. The deposition takes place when the beam scans over the targeted area from pixel to pixel. Hence the total deposition time has two components; the time the beam stays at each pixel, which is called the dwell time (t_d), and the time it takes to move from one pixel to the other (t_{bp}), which is the relaxation time. Considering these two components of the total time for the FIB deposition, a more analytical expression for the deposition yield could be expressed as [69]:

$$Y = \frac{WLZ}{I_B\, n_l[n_1 n_2 t_d + (n_1 - 1)(n_2 - 1)t_{bp}]} \quad (3.3)$$

where; n_l= Number of loops. A loop is said to be completed when the beam starts from one pixel scans around the whole pattern and comes back to the same pixel again. n_1= Number of pixels in the length direction;

n_2=Number of pixels in the width direction;

From Eq. 3.3, it can be observed that the deposition yield can be controlled by controlling the dwell time (t_d) and the relaxation time (t_{bp}).The dwell time can be input to the FIB system directly. The relaxation time can be control by controlling the interlace number. The interlace defines the number of pixels the beam will skip in each step (while going from one pixel to other). Hence, the relaxation time is directly proportional to the interlace number. For a definite size of the deposition pattern and with a constant beam current, the yield of the deposition process depends inversely on the dwell time and the relaxation time. Hence, the deposition yield decreases with increase in dwell times and the deposited films starts to become discontinuous. For higher dwell time, the net deposition yield is mainly dominated by the simultaneous sputtering at the surface of the film. This results in the formation of nano islands instead of a continuous film. An experimental setup to realize this phenomenon was developed by Karre et al. [69]. It was observed that the size of the nano islands can be modulated from 60nm to 6nm by varying the beam current, fabrication area and dwell time. The decrease in size of the nano islands with variation of dwell time from 3μs to 9 μs is shown in Fig. 3.8.

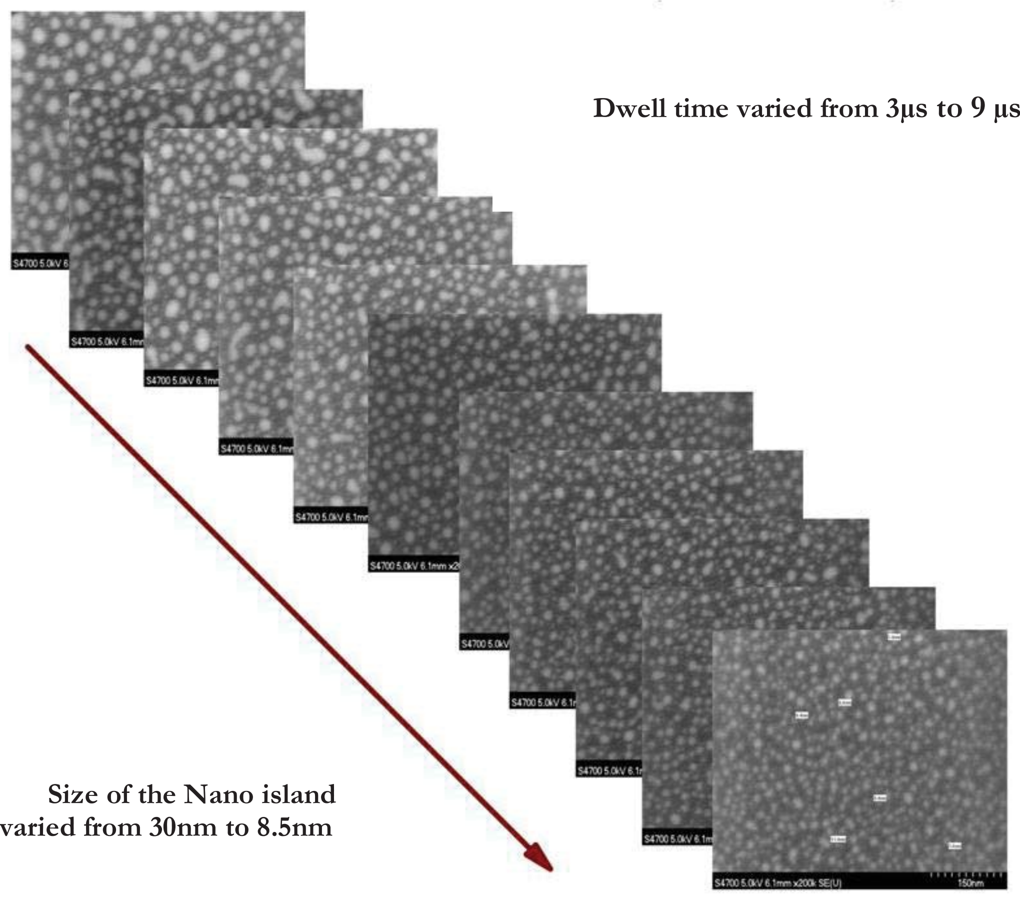


Fig. 3.8: Variation of deposited nano-island size with increase in dwell time of MI200 beam [Reprinted with permission from P. S. Karre, PhD Dissertation, MTU, 2008]

This dependence of the deposition yield with the dwell time is further investigated theoretically and a finite element analysis based model has been developed to validate the experimental results. The net deposition yields for different dwell times is estimated keeping the other parameters like the beam current, pattern area and interlace as constants. The model is based on the assumption that the energy required for the decomposition of the $W(CO)_6$ is attributed from the generated heat energy by the collision cascade in the substrate surface. In other words, the incident ions deposit their energy in the surface of the

sample in the form of phonon scattering and this energy is utilized to decompose the adsorbed gas molecules [91].

The deposition takes place layer by layer with a balance between the deposition and simultaneous sputtering process. Hence, the net deposition yield can be calculated by determining the total deposition and deducting the simultaneous sputtering yield from it as shown in Eq. 3.4.

$$Y_{net} = Y_{Total} - S \tag{3.4}$$

Where,

$Y_{net} = Net\ Deposition\ Yield$;

$Y_{Total} = Total\ Deposition\ if\ there\ is\ no\ sputtering$;

$S = Sputtering\ yield$;

The other parameters affecting the deposition like the precursor flux and the distance between the substrate and gas nozzle can be taken as constant for the calculation process. Then the total deposition yield can be written as

$$Y_{Total} = \frac{N_d}{N_i} \tag{3.5}$$

The number of incident ions *(Ni)* for each pixel can be determined from the beam current I_B and the dwell time t_d as shown in Eq. 3.6.

$$N_i = \frac{I_B}{e} \times t_d \tag{3.6}$$

Where, the electronic charge $e = 1.6 \times 10^{-19} C$. As per the mentioned assumption, the number of W atom deposited or $W(CO)_6$ molecules decomposed can be determined from the energy balance Eq. Knowing the dissociation energy of each $W(CO)_6$ molecule (E_d) and

the available phonon energy from the collision (E_p) at the surface of the substrate, N_d can be calculated as given in Eq. 3.7.

$$N_d = \frac{E_p}{E_d} \tag{3.7}$$

The surface heat energy for each pixel can be obtained by performing a time dependent finite element analysis of the heat conduction. A time dependent study is required to observe the impact of repeated incidence of the ion beam due to multiple scanning during the processes. The partial differential equation based FlexPDE [92] software package was used to study the heat conduction and temperature rise during the deposition process. Considering the nature of the beam profile, a Gaussian heat flux (with respect to x, y) is taken as the heat source which attributes the heat energy generated due to the phonons. The magnitude of the heat energy is primarily the fraction of the ion energy which is being dissipated as phonon scattering in the sample surface. The Monte Carlo simulation based SRIM/TRIM [93] package has been used to obtain this energy value. The parameters used in the SRIM/TRIM calculation and the FlexPDE code for evaluating heat conduction at the surface are listed in the appendix section.

In the FEA analysis for heat conduction, the boundary conditions are defined by assigning all the surface temperatures to 300K before the beam strikes. The time dependency is implemented by introducing periodicity in the heat source to realize the deposition process in which the ion beam strikes each pixel periodically. The ON time for the heat flux is same as the dwell time (the time for which the beam stays over each pixel) and each period is taken as the loop time (time taken for the beam to come back to the same pixel) which is 0.59sec. in this case. The temperature distribution and the maximum rise in

surface temperature are calculated for different dwell times. It has been observed that the maximum surface temperature increases with dwell time but doesn't go beyond 900˚C. This implies that the maximum part of the generated heat transfer is to the alumina layer and the silicon substrate. From the time dependent study it is observed that the relaxation time (the time required to reach room temperature) is much less than the loop time. In other words the surface temperature at each pixel comes back to its original value (300K) before the beam strikes the pixel for the next scan. Figure 3.9 shows the change in maximum temperature with dwell time.

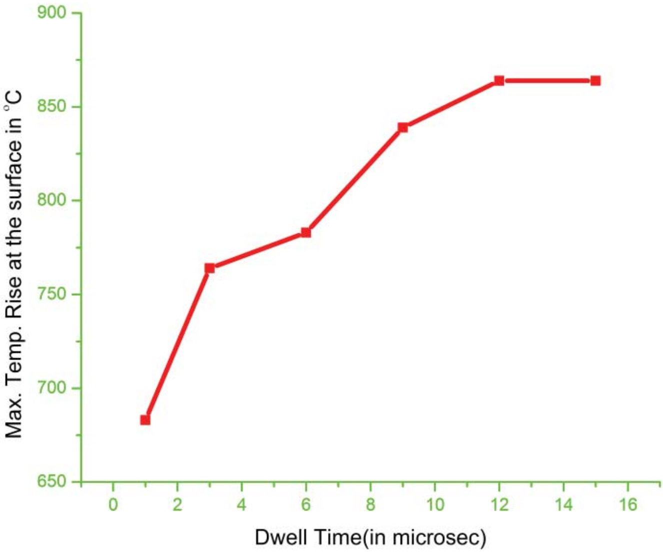


Fig. 3.9: Increase in surface temperature with respect to the dwell time during FIB deposition process

From the temperature distribution data, the amount of heat content in a collision volume is determined using simple heat conduction theory [94]. This heat energy is being

used to decompose the adsorbed $W(CO)_6$ molecules. Hence, the total deposition yield (Y_{total}) can be determined by using Eq. 3.4, 3.5 and 3.6.

The sputtering yield for each dwell is determined by Monte Carlo simulation for the ion-solid interaction using SRIM/TRIM package. Finally the net deposition yield (Y_{net}) is determined by using Eq. 3.2. The above process is repeated for different dwell times (t_d) and the variation of the net deposition yield with the dwell time is determined. As shown in Fig. 3.10, it can be observed that the net deposition yield decreases with dwell time. The deposition yield is less than 100 for dwell times of 5μs or more, which is just one order higher than the sputtering yield. This validates the fact that as the dwell time increases we get discontinuous film and finally when the dwell time is too high we will deposit nano-islands instead of continuous films. This outcome qualitatively agrees with the obtained experimental results.

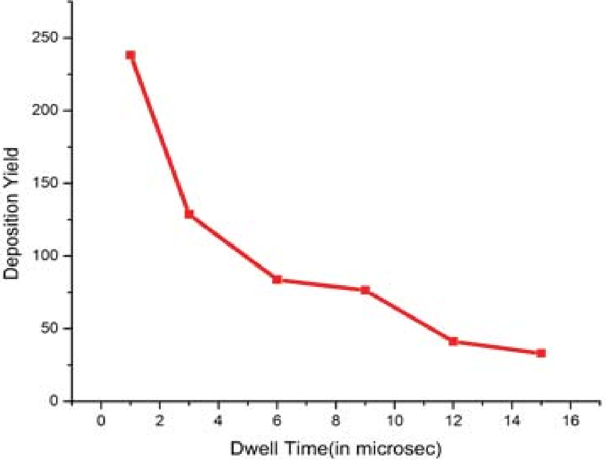


Fig. 3.10: Variation of deposition yield with respect to dwell time as obtained from the FEA based calculation.

For room temperature operation the SET devices, the capacitances of the nano islands need to be in the order of aF range [40], which requires the size of the islands to be smaller than 10nm in diameter. The FIB deposition technique described above is used to fabricate the nano islands of size below 10nm. The parameters for this fabrication process are given in the appendix section. These parameters are used to deposit the sub-10nm nano islands between the source drain gap to realize the RT-SET.

3.3. Fabrication of Tunnel Junction for RT-SET

The operation of the SET is based on the controlled transport of electrons from the source to drain terminal through the dominant conducting path. The electron transport is possible by tunneling in the junction between the terminals and the nano islands and between the nano-island themselves. To realize the localization of these electrons in the individual dots the resistance of these tunnel junctions must be greater than that of the quantum resistance which is $\frac{h}{e^2} = 26k\Omega$. Hence, fabricating this tunnel junction is one of the critical steps in the fabrication process.

The tunnel junctions for the SET devices are fabricated by oxidizing the quantum dots deposited using FIB deposition technology. The formation of an oxide layer over the W nano islands can be achieved either by thermal oxidation or by chemical oxidation of these nano dots. However, it has been observed that during the thermal oxidation at a process temperature of 900^0C the size of the nano islands increases due to the internal thermodynamics of the process [69]. As for a room temperature operation of the SETs the size of the nano-islands has to be smaller than 10nm, and thermal oxidation is not suitable

for fabricating the tunnel junction for the RT-SETs. The chemical oxidation method is considered to be a suitable method for fabricating the tunnel junctions for the W nano islands. Peracetic acid is used for oxidizing the W nano islands. Peracetic acid is a mixture of acetic acid and hydrogen peroxide at a ratio of 1:1 by volume. In the oxidation process, samples are thoroughly cleaned in piranha solution before putting them in the peracetic acid solution. Peracetic acid as a strong oxidizing agent, forms a thin layer of tungsten oxide over the nano-islands surface. It was observed that the thickness of the oxide layer depends on the time of oxidation [69] as shown in Fig. 3.12. A longer time results in the nano-structures being etched away due to the dissolution of the grown oxide in H_2O_2. The thickness of the oxide layer with respect to the oxidation time is shown in Fig.3.11. For the current work, different oxidation times were used for different device configurations which are summarized in the appendix section. The property of this oxidation process to etch out all the W dots when oxidized for a long time is further used for the process development of fabricating Si quantum dot based devices. This will be discussed in the subsequent section.

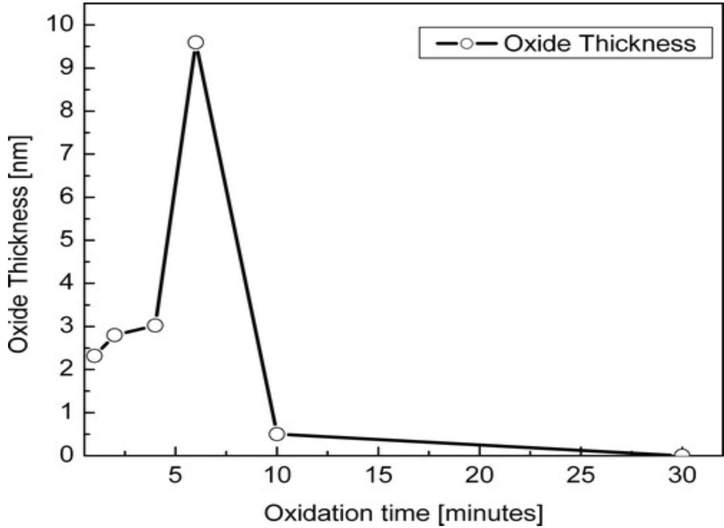


Fig. 3.11: Thickness of the tungsten oxide with respect to the oxidation time [Reprinted with permission from P. S. Karre, PhD Dissertation, MTU, 2008].

3.4. Process Integration

The processes for fabricating the individual elements of the device are developed. The functional devices with different configurations are realized by integrating all these processes. To improve the functionalities of the devices, like threshold voltage (V_{th}), gate controllability and critical dimension, studying parameters impacting the device characteristic is very important. In this effort, devices with structural and topological variation are fabricated. In a further investigation, SETs with semiconductor quantum dots are also studied. The different devices fabricated are listed below.

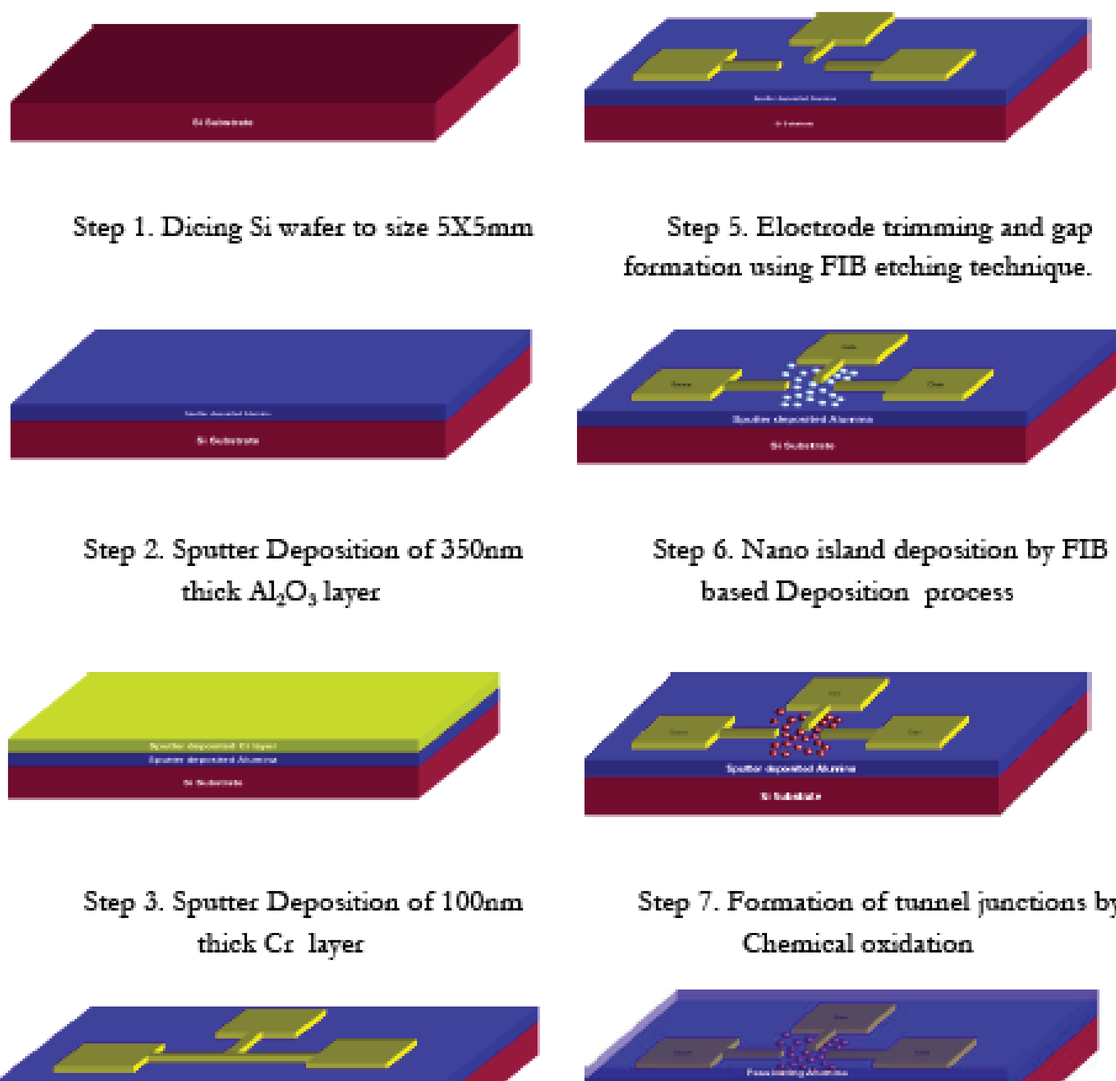
- ✓ Sub-20nm Source-Drain gap based SETs.
- ✓ Devices with varying source drain gaps.
- ✓ Vertical SET devices.

- ✓ Silicon quantum dot based devices.

This section will explain the integration of different processes to fabricate the above devices. Optimization in the process parameters required for achieving the targeted nano features of the device is also done in the individual process flow.

3.4.1. Sub-20nm Source-Drain(S-D) Based SET Devices

From the discussion in the design chapter it is known that one efficient way of improving the threshold voltage (V_{th}) in multi-dot based SETs is to reduce the series capacitances associated with the Dominant Conducting Path (DCP). This can be done by reducing the number of dots participating in the DCP, the most ideal case being just one dot in the DCP. A FIB based direct writing technique with different pattern layouts has been approached for achieving the nano-structure for a SET with a single island of size below 10nm. However, the tail energy overlapping issue in the FIB etching process limits its ability to fabricate such structure in sub-30nm regime. Hence a different approach is pursued to decrease the number of participating dots in the DCP by decreasing the source to drain gap. The nano electrodes with a very small inter-electrode gaps can be fabricated by the FIB etching technique and the conducting nano-islands can be deposited in the gaps by the FIB deposition technique. The fabrication process flow for such a device is given in Fig.3.12. Considering the average size of the deposited dots to be ~8nm [79], a source drain gap of less than 20nm is required to obtain a device having 1-2 dots in the DCP.



Step 1. Dicing Si wafer to size 5X5mm

Step 2. Sputter Deposition of 350nm thick Al_2O_3 layer

Step 3. Sputter Deposition of 100nm thick Cr layer

Step 4. Formation of probing pads and electrodes by FIB etching process.

Step 5. Electrode trimming and gap formation using FIB etching technique.

Step 6. Nano island deposition by FIB based Deposition process

Step 7. Formation of tunnel junctions by Chemical oxidation

Step 8. Device passivation by sputter deposition of 30nm thick Al_2O_3 layer.

Fig. 3.12: Process flow for FIB etch deposition based RT-SET fabrication.

Silicon samples of size 5mm× 5mm are used as the substrate for the devices. After a thorough cleaning by piranha solution, a 350nm thick Al_2O_3 layer is deposited on the Si substrate as an isolating layer between the Si and the devices. The Al_2O_3 deposition is done by physical sputtering process using a Perkin-Elmer 2400-8J RF sputtering tool. After the isolation layer, a thin layer of Cr film of thickness 100nm is deposited. This will act as the active layer for the device. Another RF-sputtering process is used for Cr layer deposition. The detail about the film deposition and the parameters for these processes are discussed in the previous section.

Once the active layer is deposited, the samples are introduced to the Hitachi FB-2000A FIB system to fabricate the micro/nano structure for the device. The device fabrication in the FIB system is done in 4 steps: 1. Pattern generation, 2.Fabrication of the device pad and electrodes, 3. Fabrication of inter-electrode gaps, and 4. Deposition of the nano-islands.

The pattern generation and the pad and electrode fabrication steps are achieved following exactly the same procedure as that for the single dot based devices as mentioned in the previous section (3.1). The electrodes are trimmed to 100-500nm in thickness using the vector scan mode. The SEM micrograph of the micro pads and the active area with the electrodes are shown in Fig. 3.13.

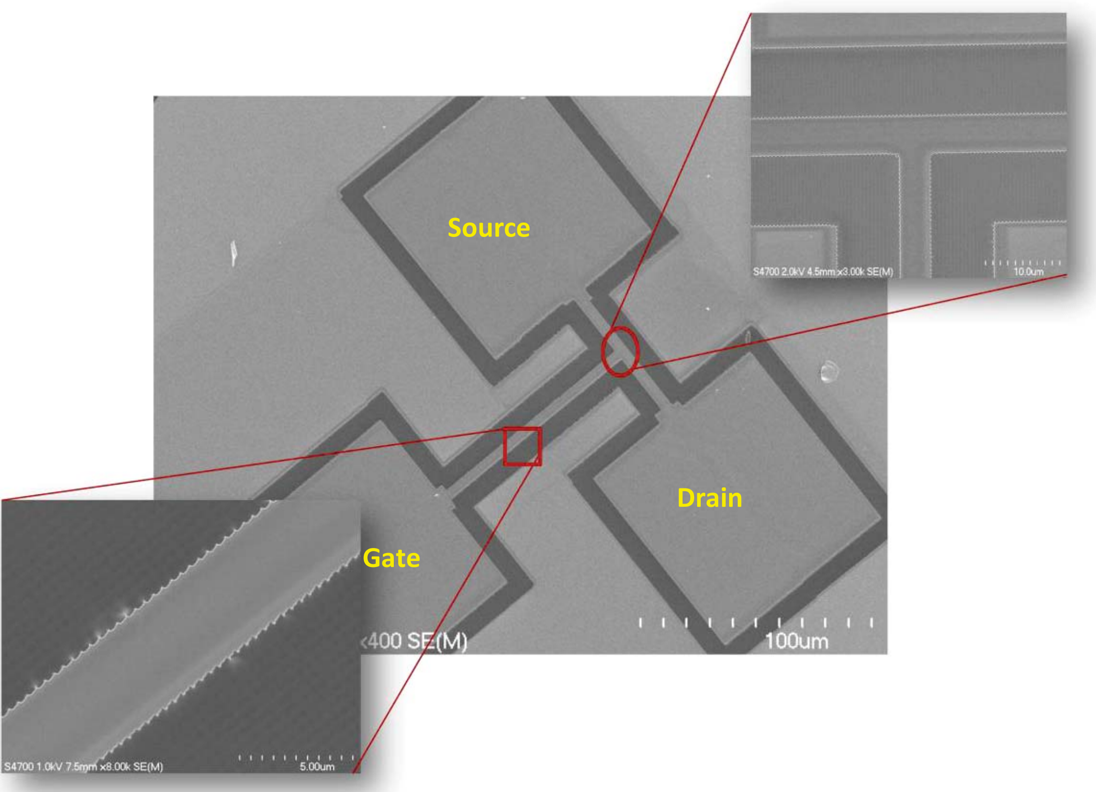


Fig. 3.13: Scanning electron micrograph of the micro-pads and electrodes. The top inset shows the magnified view of the active area before electrode trimming. The bottom inset shows the magnified view of an electrode.

Once the electrodes are trimmed to 100-200nm, the next step is to fabricate the nano gap between the electrode terminals. The FIB etching process is used for fabricating these gaps. As resolution is of highest priority during fabrication of these nano-gaps, the vector scan mode is used. The gap between the source and drain electrode is targeted to <20nm and the gap between the gate electrode is targeted <50nm. As the beam current has great impact on the resolution of the etched structure, observation beams are used for this

process. The lowest beam current available in the FIB system is the MO-06 beam which is 1pA. However, it is observed that perfect alignment and control of this beam is very difficult, and this decreases the repeatability. Hence, the next higher current beam MO-20 is used for fabricating the nano-gaps between the electrodes. The MO-20 beam has a beam current of 1-4pA and the beam radius of 20nm. The layout for the gap formation is drawn on the onboard CAD system in the FIB system. The mode of fabrication (Raster scan or Vector scan) has to be specified during the pattern generation stage. The resolution of the desired structure is affected on the different parameters. The description of parameters and their impact on the resolution is described below.

Pattern Line Width: - As discussed in the previous section, during the vector scan etching process the beam scans the desired area in a line-by-line fashion. Therefore, the width of the line is a controlling factor for desired resolution. When the beam scans any pattern, it divides the pattern into number of pixels and moves from one to another. Thus, line width in a pattern can be described as the measure of number of pixels in the line in a lateral direction. Two different pattern lines having line width of 1 and 2 respectively is shown in Fig. 3.14. From this, it is very obvious that the beam covers more area in the sample when the line width is higher. The area covered in every scan is also depends on the pixel size which again depends on the beam diameter (beam type).

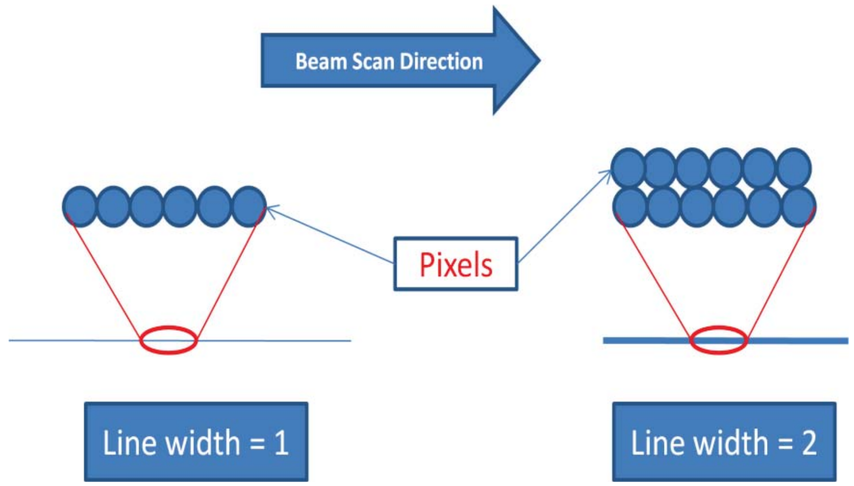


Fig. 3.14: Illustration of pattern line width and the pixel arrangement

Frame Number: - Unlike the raster scan mode where we can input the total time of etching, in vector scan mode the etch time is determined by a parameter called frame number. Frame number determines how many times the beam will scan the whole line in each run. The total time of etching is directly dependent on the frame number along with other parameters like dwell time and zoom area. For high resolution nano structure fabrication, it is observed that multiple runs with lower frame numbers works better than a single run with a higher frame number. This may be due to the extra time between each run, which helps in dissipating the heat in the sample, generated during the ion-sample interaction process.

Dwell Time: - Dwell time is the time the beam stays in each pixel during every scan. It is the most important parameter for the fabrication process as it has the highest impact on the resolution of the desired structure. In the vector scan mode, the dwell time can vary from 1μs to 128 μs. This also determines the total time of etching in a particular run.

Magnification: - The area of the fabrication window or the magnification, which is determined by the zooming option in the FIB system, is also a deciding factor for the resolution. Especially in vector scan mode fabrication, the process pixel size directly depends on this parameter. As the pixel size gets smaller when the area is small, high-resolution structures are easy to fabricate at minimum area of the fabrication window or at the highest zoom. The minimum area of the fabrication window that can be achieved in our FIB system is 1 μm x 1 μm. However, it is observed that it is very difficult to achieve the desired resolution of the targeted structure at this area. This is because the pixel size at this area is almost equal to or smaller that the beam diameter itself and hence, controlling the beam is really difficult.

All the parameters discussed above are optimized to obtained the desired resolution of the inter electrode gap. The parameters used for fabricating the nano inter-electrode gaps are shown in Table 3.4. The SEM image of the fabricated structure is shown in Fig. 3.15. From Fig.3.15 it can be observed that the resulting gap width is ~37nm which is much higher than the desired value of <20nm.

Table 3.4: Fabrication parameters for 17nm source drain gap formation

Parameter	Value
Beam Type	MO20
Scanning Mode	Vector scan
Dwell Time	30 μs
Number of runs	1 to 2
Frame Number	70
Fabrication Area (Zoom)	2x2 μm (Zoom=4x2)
Pattern Line Width	1pixel

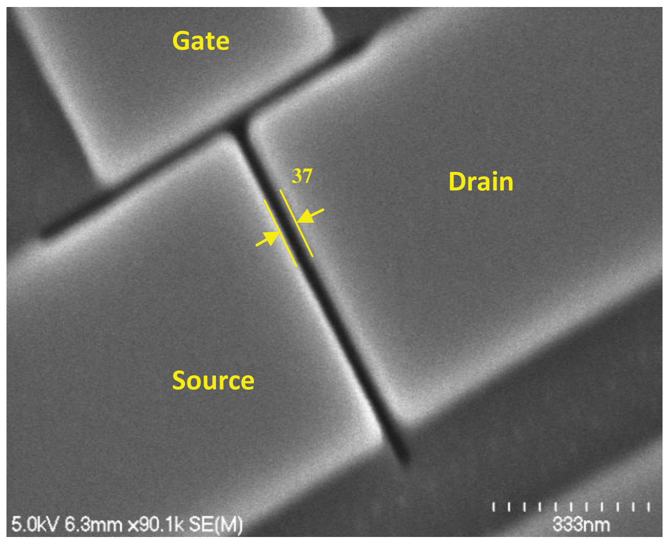


Fig. 3.15: Scanning Electron Microscope image of the inter electrode nano gap for the targeted RT-SET (Before The process optimization).

It is expected that the FIB etching generated secondary effects like localized heat generation and tail region etching that might be the reasons for the deviation of the resultant gap width from the targeted value [95]. Hence, an optimized process must be designed to minimize the impact of these effects on the resolution of the fabricated nano structures. The process optimization requires characterization of the FIB etching process considering additional effects like the profile dependant etching and localized heat generation. In the further investigation, the phenomena occurring during the ion-solid interaction for FIB etching process is studied.

3.4.1(a). FIB Etching Characterization

To characterize the FIB etching process and the other effects associated with it during fabrication in nano meter regime, it is very important to study the ion solid interaction phenomenon. From the ion-solid interaction phenomenon, the dissipation of the ion energy in different events can be evaluated and hence the localized generated heat can be estimated. In this section the different events occurring during the ion solid interaction process for the FIB etching will be discussed. The energy dissipation on different events is calculated and their impact on the desired structure is estimated. Impact of the beam profile on the etched structure is described with a suitable experimental set-up.

Ion Solid Interaction: The ability to mill, image and deposit materials using a Focused Ion Beam (FIB) system depends critically on the ion beam- solid interaction [83]. Figure 3.17 shows a schematic diagram illustrating the possible ion beam-material interactions that can result from ion bombardment of a solid. The impinged ion may come to rest inside the material after a series of elastic and non-elastic collision or can back sputter with some energy after going through a few collisions. During the collision between the energetic ions and solid atoms, the ion dissipates its energy in three major events. They are

- ✓ Ionization
- ✓ Phonon Generation
- ✓ Vacancy Creation (which may lead to sputtering)

These three events can occur individually or simultaneously for each ion. Ionization occurs when the ion strikes a target atom and removes one or more electrons from it. These

electrons can be emitted out from the target surface or can neutralize any already ionized atom inside the target material. In addition to that, the moving atoms recoiled by the impinged ion can collide and transfer some of its energy to a stationary or another moving neutral atom to ionize them. The emitted electrons are called as secondary electrons (SE). The SEs can be collected by a detector producing a current which is further processed to image the surface of the sample. The ionization process is a result of an inelastic collision of the impinging ions as there is no momentum transfer involved in it.

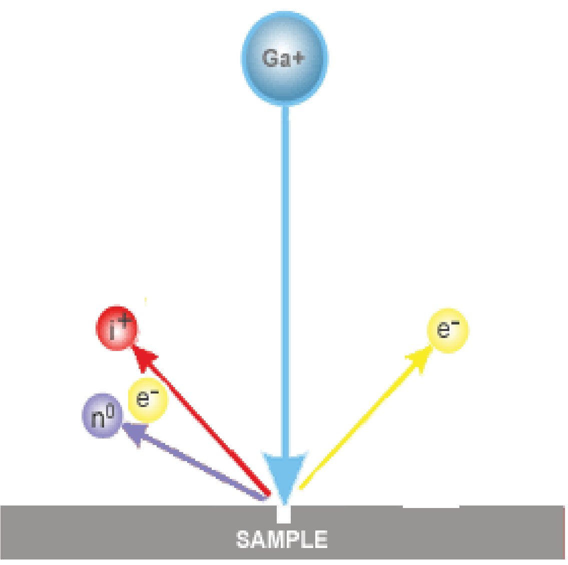


Fig. 3.16: Pictorial view of ion-solid interaction

When the energetic ion impinges the target substrate, it can lose its kinetic energy by colliding with several target atoms. This displaces the stationary atoms from their lattice position and creates vacancies. The displaced atom can create a cascade of secondary collisions before coming to rest by losing all its kinetic energy. After a cascade of collisions the moving atom (the ion) can either take a vacancy position and hence decrease net vacancy

or can take an interstitial position. During the collision cascade, if a moving atom has enough energy to overcome the surface binding energy of the material, the atom can exit out of the surface, creating a permanent vacant site. This phenomenon is known as physical sputtering. The FIB based etching process is a result of a series of sputtering events. The sputtering process is a surface phenomenon, as the probability of a recoiled atom at the surface having energy greater than the surface binding energy of the material is much higher than that for an atom underneath the surface.

Apart from the sputtering and ionization process, the impinged ion generated collision cascade can result in phonon generation due to the transfer of energy as lattice vibration. When the transferred energy to an atom is less than the threshold energy to create a vacancy, a phonon is generated [96]. The phonon generation can lead to localized heating and hence enhances the lateral etching.

To characterize the sputtering generated etching phenomenon during the FIB processing, evaluation of the fractional distribution of the ion energy dissipated in the above three events is important. Monte Carlo simulation based SRIM computer simulation package [97] was used to analyze the ion energy distribution in the material for different events. During this calculation the impact of the Guassian profile of the FIB beam is taken into account, by varying the dose and the energy of the ions as a Gaussian function. For the current experiment, Cr is taken as the target material and Ga is taken as the impinging ion. The peak energy of the ions at the center of the beam is defined to be 30keV. The SRIM package takes number of ions as the input parameter instead of the ion dose. The total number of ions for a particular beam in the FIB system is calculated from the beam as given in Eq. 3.5.

The simulation results from the SRIM/TRIM package show the percentage distribution of energy dissipated in the three different events (lattice vibration (phonons), ionization, and vacancy creation). A snap shot of the input and output window of the SRIM tool is shown in the appendix section. The SRIM tool uses the Monte Carlo simulation technique and analyses the stopping power in each collision. Finally, the percentage of energy dissipated in different events is evaluated statistically [97]. It is observed that 50-60 % of the energy goes into phonon generation, 40-45 % of the energy dissipates for the ionization of the atoms in substrate, and only 4-8% of the energy goes for removing the atoms. Following the same simulation technique, a set of output data is obtained for different positions in the Gaussian beam. The input parameters like the energy and the number of ions for these points are calculated considering a Gaussian distribution with a peak at the center of the beam. Figure 3.17 shows the distribution of fractional energy distribution in different events with respect to the position in the beam profile. The trajectory of the displaced atoms and impinged ions is shown in Fig.3.18.

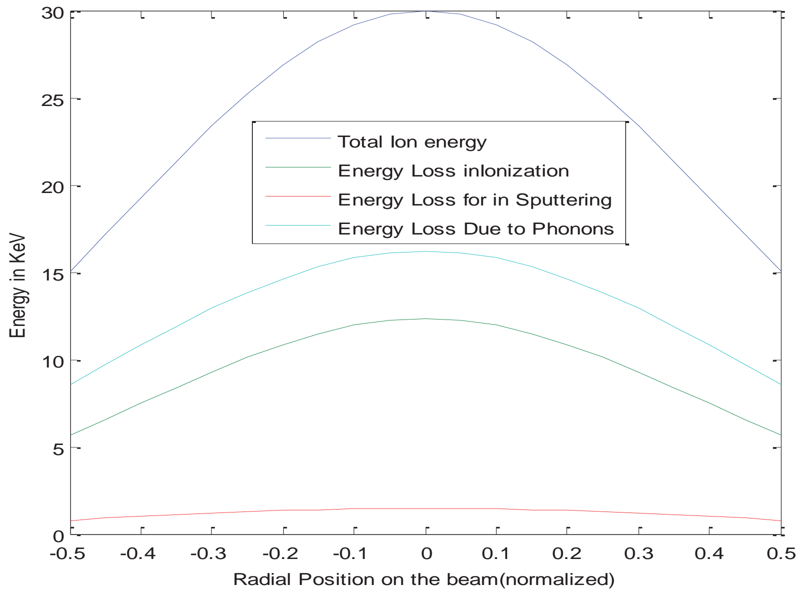


Fig. 3.17: Dissipation of ion energy for different events in sample surface.

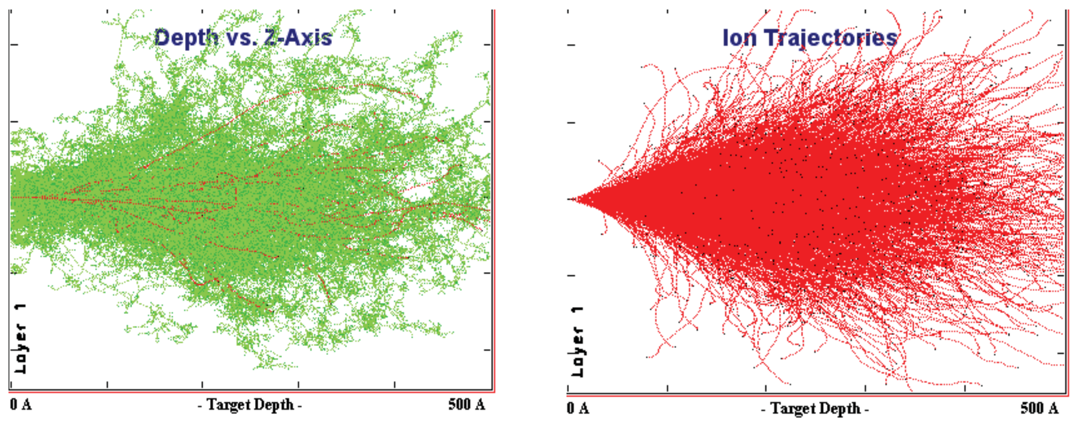


Fig. 3.18: Trajectories of the displaced atoms (Left) and the incident ions (Right)

From this simulation, it is observed that more than 50-60% of ion energy is going only for phonon generation and ultimately surface heating. In a further investigation the distribution of the phonon energy inside the sample surface is obtained. Figure 3.19 shows the distribution of the phonon energy with respect to depth from the sample surface. It was observed that the phonon energy distributed with a nearly Gaussian distribution up to ~50nm beneath the sample surface, with a peak at ~23nm. The phonon generated heat is localized inside the collision volume [83]. This localized heat can impact the resolution of the desired structure by providing additional energy to the surface atoms.

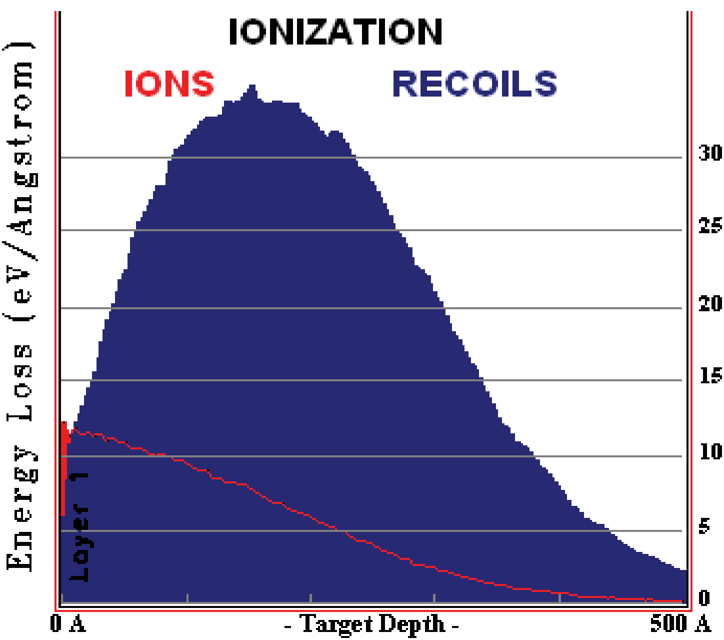


Fig. 3.19: Distribution of the phonon energy beneath the sample surface

Apart from the localized heat generation, the etching profile during FIB etching process also depends on the etching taking place at the tail region of the Gaussian beam.

Efficient and reliable fabrication process of nano structure below 100nm is achievable by engineering the beam. This requires a complete understanding of the etch rate at different position of the beam profile. Hence, as an effort to characterize the etch rate with respect to the beam profile, the sputtering rates for the target material (here it is Cr) is evaluated at different points in the beam. With the capability of the SRIM tool the distribution of the displaced atom reaching at the surface can be obtained with respect to the amount of kinetic energy contained by them.

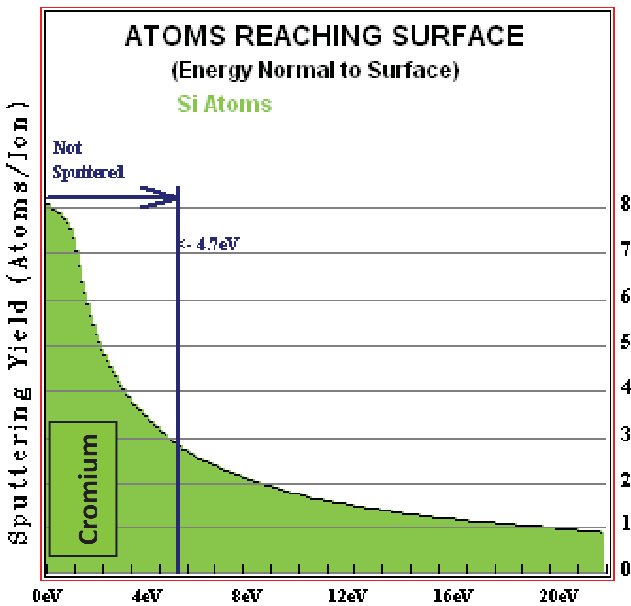


Fig. 3.20: Distribution of moving atoms reaching at the surface. The atoms having energy more than the surface binding energy will be sputtered out.

Figure 3.20 shows the distribution of the displaced ions with respect to the kinetic energy contained by them. Sputtering occurs if the contained energy of these atoms exceeds the surface binding energy. Hence, the sputtering yield can be evaluated from this plot by

determining the average number of atoms having energy more than the surface binding energy. The numerical value of the sputtering yield can also be extracted from the SRIM output file directly. The sputtering yield is calculated at different position in the beam and plotted in Fig.3.21. It can be observed that the sputtering yield decreases from the center of the beam towards the tail. Although the numerical value of the sputtering yield is not that different throughout the profile, the final etch rate has its impact as it counts for the total ion impinged.

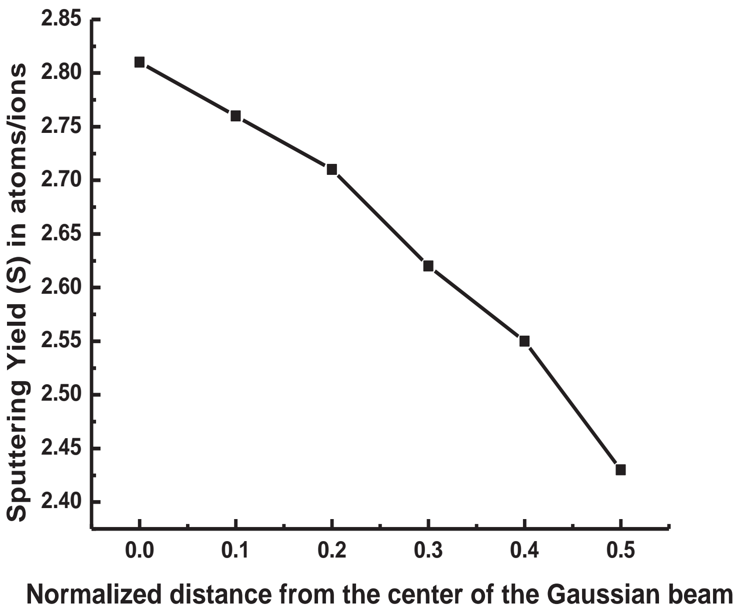


Fig. 3.21: Variation of the sputtering yield with respect to the position in beam profile

In a further investigation, an experimental setup was designed to determine the profile dependency of the etched structure for an FIB etching and validate the modeling result. Figure 3.22 shows the design of the experimental setup. The basic idea is to find out the material removal rate when etched by different parts of the beam (say tip and tail).In the

designed experiment, a thin strip of tungsten is fabricated by FIB deposition process and then it is etched by the FIB in an oblique direction.

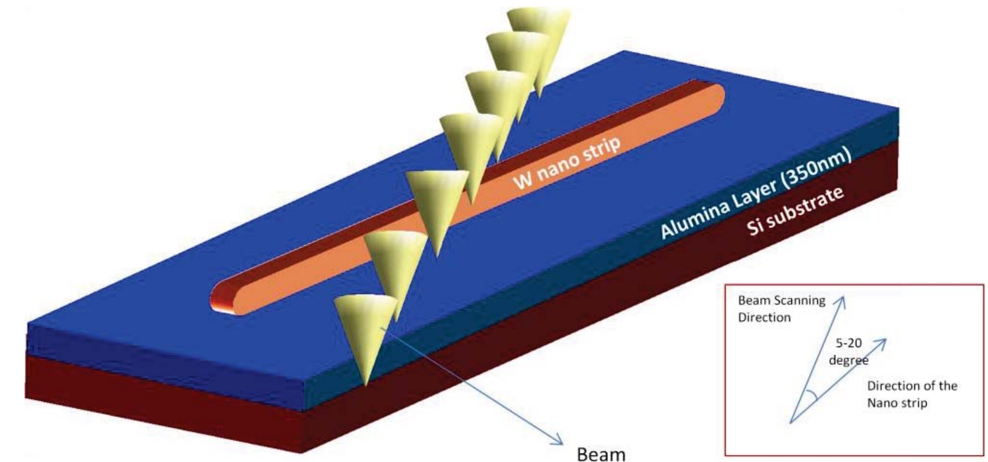


Fig. 3.22: Pictorial view of the experimental set-up to study the beam profile dependency in the FIB etching process.

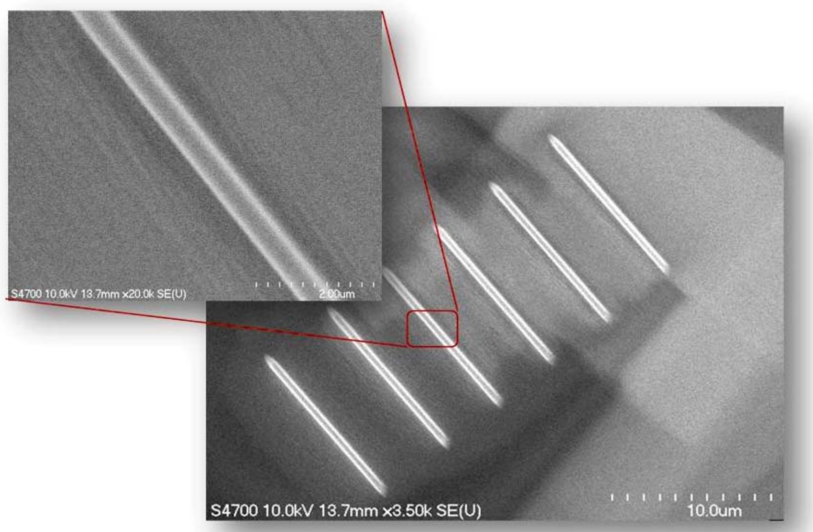


Fig. 3.23: SEM image of the Tungsten Nano strip deposited by FIB deposition process (at different magnification).

The FIB process parameters for the nano strip deposition and etching is given in the appendix section**.** The SEM image of such nano strips is shown in Fig. 3.23. The angle between the beam scanning direction during etching and length of the nano strips are varied from 5^0, 10^0 and 20^0. The objective was to gradually expose the strip to the different portions of the beam profile as the milling continues. This allows the beam to etch the nano strip with a different rate at different positions.

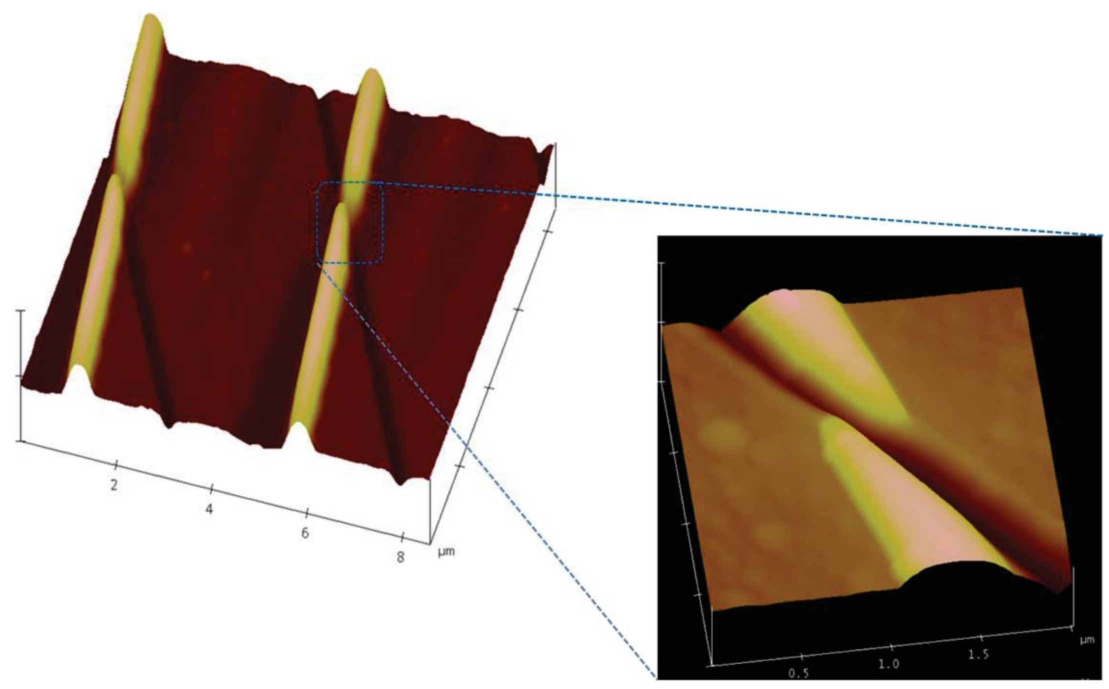


Fig. 3.24: AFM image of W nano strips at different magnification, after being etched by FIB in an oblique direction.

Finally, the etched profile of structure is characterized by using an Atomic Force Microscope (AFM). It is expected that the material removal rate increases as the beam comes closer to the strip. The images obtained from the AFM are shown in Fig. 3.24. From the

cross sectional analysis of the AFM images, it can be observed that the material removal from the portion of the nano strip where it is etched by the tail region of the beam is much less than that for the portion where it is etched by the center of the beam. This result validates the modeling outcome as described above.

3.4.1(b). Process Optimization for Nano-gap Fabrication

From the modeling and experimental data in the FIB etching characterization study as described above, it can be observed that two key parameters are affecting the resolution of the inter-electrode gap:

- ✓ Phonon generated localized heating
- ✓ Etching in the tail region.

To maximize the resolution, the impact of the above two phenomena must be minimized. The generated heat has to be dissipated efficiently and in the mean time the optimization in the process parameters is needed to minimize the impact of the tail region of the beam. A novel technique is developed to improve the resolution of the desired nano structure by controlling the thickness of the active Cr layer. The sputtering process is limited to the surface of the material [83]. Hence, if the phonon generated heat can be efficiently dissipated far from the surface of the Cr, the resolution of the desired structure is expected to improve. This can be achieved by controlling the thickness of the Cr layer. For a thinner Cr layer the part of the collision cascade can shift to the underlying Al_2O_3 layer during FIB etching. As the density of the Cr is twice that of Al_2O_3, the straggle of the ions is greater in the Al_2O_3 film, which aids in achieving higher resolution of the desired structure in the Cr layer. Also, the higher heat capacity of the alumina layer helps to take the heat out from the

Cr layer to give a controlled etching with better resolution of the desired structure. On the other hand, the desired structure in the ultra thin ultra thin Cr layer may be more greatly impacted by the tail region etching. Hence, a trade up between these two effects has to be obtained to achieve the desired resolution in the nano structure.

To experimentally demonstrate this modeling result, the desired nano structure (inter-electrode gaps) for the SET devices are fabricated on samples having different thickness of Cr layer. The probing pads and connecting electrodes are fabricated by the process as mentioned before on Si/Al_2O_3 sample with a Cr layer of different thickness. The thickness of the Cr layer is varied from 100nm to 10nm. The inter electrode gaps are fabricated using the MO-20 beam in the Hitachi FB-2000A FIB system. The beam parameters as given in appendix section, are kept constant for all the samples. The SEM micrograph of the inter-electrode gap for different thickness of the Cr film is shown in Fig. 3.25.

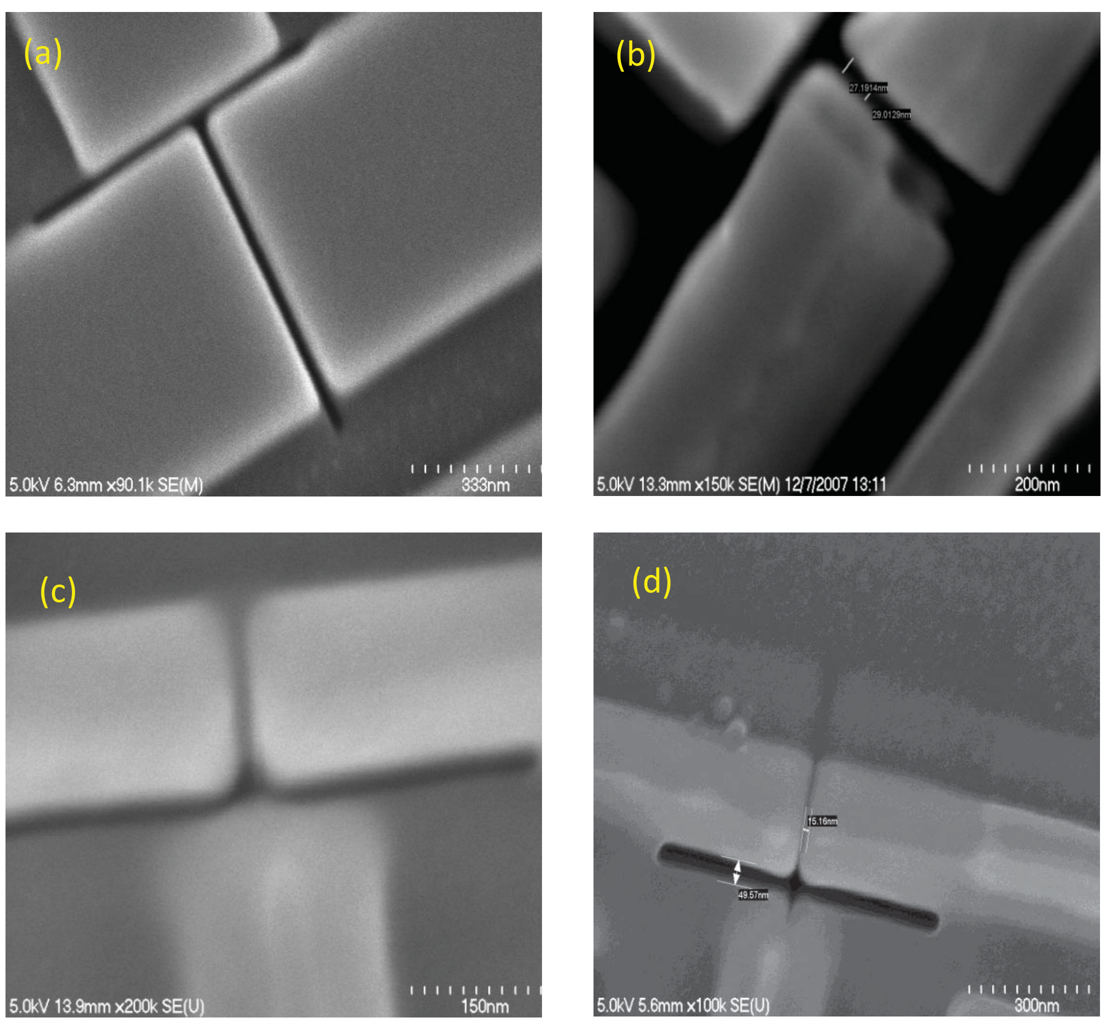


Fig. 3.25: SEM images (the s are not in the same scale) of the inter electrode gaps fabricated in Cr films of different thickness (a)100nm,(b)50nm,(c)20nm,(d)15nm

Figure 3.26 shows the variation in the experimental gap length with the variation in the thickness of the Cr film. As the thickness of the Cr film increases, the majority of the ion interactions occurs in the Cr thin film and hence, does not result in a high resolution of

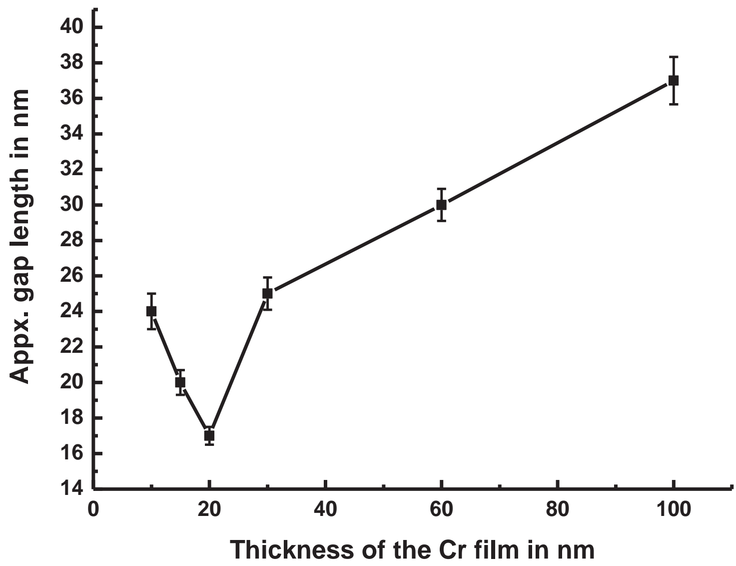


Fig. 3.26: Experimental inter-electrode gap length vs thickness of the Cr Layer

the etched nanostructure. When the thickness of the Cr approached below 30nm which is close to the required resolution of the nanostructure, it was observed that, the majority of the ion interactions did not occur in the Cr thin film, thus improving the resolution of the fabricated nanostructure. From the experiment it is concluded that the possible resolution of the nano structure is highest when the thickness of Cr is between 15-20 nm. This is supported by the modeling results. As obtained from the TRIM simulation, the ion and displaced atom trajectories during the etching process for our system with a Cr film of 15nm and 20nm are shown in Fig. 3.27, which confirms the occurrence of maximum collisions in

the Al_2O_3 film rather than the Cr film. In Fig. 3.27(b) and 3.27(d) the green (light) color represents the displaced atoms in Cr and the red (dark) in Fig.3.27(a) and 3.27(c) and violet (light gray) color shows the displacement of Al and O atoms respectively.

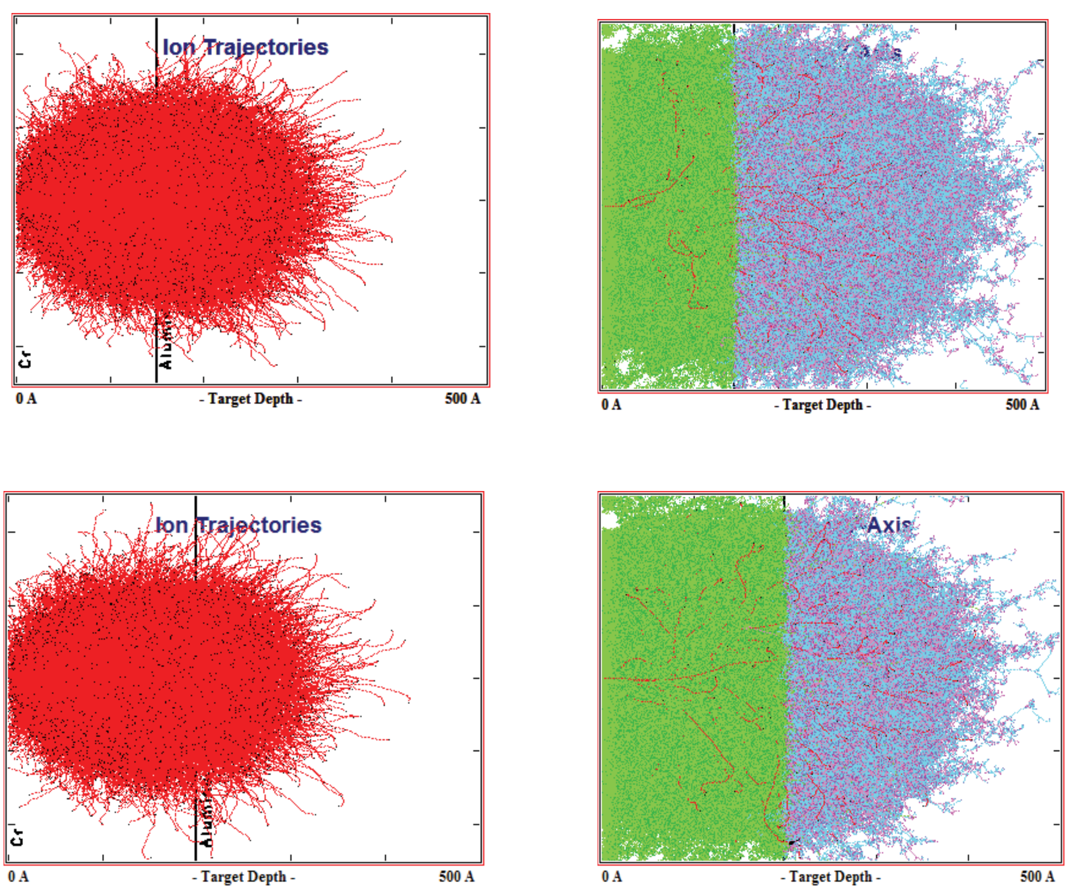


Fig. 3.27: Ion and displaced atom trajectories and collision cascades for Cr film of (top) 15nm and (bottom) 20nm over 350nm thick Alumina film as obtained from the TRIM model.

After obtaining the optimized value of the Cr thickness, the SET devices are fabricated using the optimized process parameters. A sample with 20nm Cr layer is processed by FIB etching as mentioned above and a source-drain gap of ~17nm and gate gap of ~30nm is achieved.

The nano-islands are deposited using the previously mentioned FIB deposition process. The deposition parameter for the nano-islands is given in the appendix section. The tunnel junctions for the devices are fabricated using the chemical oxidation method using peracetic acid. The oxidation was performed for 2 mins expecting an oxide of thickness 2-3nm. Device passivation was done by depositing a 30nm thick Al_2O_3 layer using the RF sputter deposition technique. And finally the device pads are exposed using FIB etching technique for probing purpose during the device characterization. The process parameters for depositing the passivation layer and the exposing the probing pads are given in the appendix section. The SEM micrograph of such a device before the passivation is presented in Fig. 3.28 with different magnification.

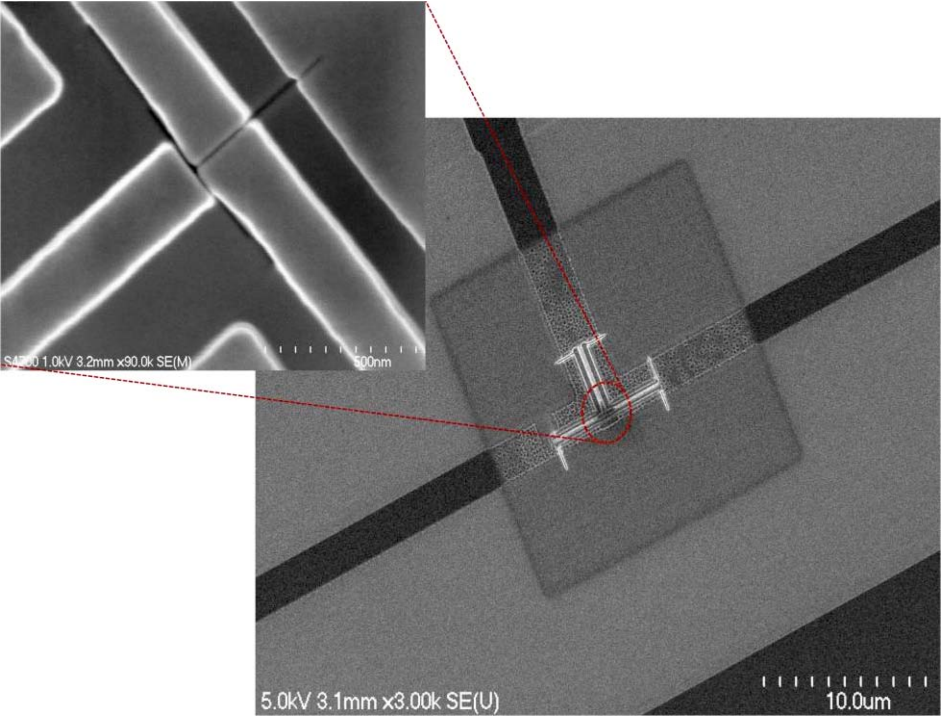


Fig. 3.28: The SEM micrograph of a Sub-20nm source-drain gap based SET. The inset shows the electrode terminals and the nano gap before the dot deposition.

3.4.2. SETs with Varying Inter-Electrode Gaps

The sub-20nm source drain gap based devices are fabricated with an effort to improve the threshold voltage of the SET devices. In a further effort to study the impact structural variation on the device behavior, devices with varied source drain gap are fabricated. The source drain gap is taken as the structural parameter for investigation as it has a direct relationship with the total effective capacitance of the device [45, 46].

The FIB etch and deposition technique is used to fabricate the devices. Similar process flow as that for the sub-20nm based device is followed to fabricate the probing pads, the connecting electrodes and the nano terminals. The final inter electrode gaps for the devices are different for different devices. In the fabrication process, the width of the nano gaps can be varied either by varying the frame number and dwell time or by varying the line width of the pattern. As the process with line width variation is faster and more controllable, it is used to pattern the different widths of the nano gaps. The FIB parameters for different width of the nano gaps are given in the appendix section. The nano islands are deposited by the FIB deposition process and the tunnel junctions were fabricated using the chemical oxidation technique. The oxidation time was kept constant for all the devices to maintain a uniform junction width for all of them. The device passivation and the exposure of the probing pads are done by following the process as mentioned for the sub-20nm devices.

3.4.3. Vertical SETs

Utilizing the FIB based etch and deposition technique, SET devices with source drain gaps of 17nm are successfully fabricated. Considering the average size of FIB

deposited nano-island to be 6-10nm, it is expected that at most 2 dots are in the dominant conducting path depending upon the exact size of the dot in the DCP. Hence, single dot behavior from such a device cannot be expected always. Electron transport through a single dot in the dominant conducting path can be possible for such devices only if a source drain gap of ≤12nm is achieved. However, from the analysis of the FIB etching process it is observed that fabricating a nano gap of that size is extremely difficult due to the secondary effects during FIB processing. An alternative approach has been made to realize a SET device with a single quantum dot participating in the dominant conducting path.

A device with vertical source and drain electrode configuration has been fabricated. The idea is to sandwich the nano islands between the two electrodes and realize a single dot based SET device. This also explores the possibility of 3-D fabrication of the future ultra large scale nano-electronic circuit to achieve higher device density. The pictorial view of the device configuration is shown in Fig. 3.29. As shown in Fig. 3.29, there is just one layer of dots in between the source and drain electrode. As in multi dot based SET device the current transport must take place through just one dominant conducting path. It is obvious that out of several parallel paths, the electron will be transported through just one dot. Hence, the realization of a single dot based SET device is possible.

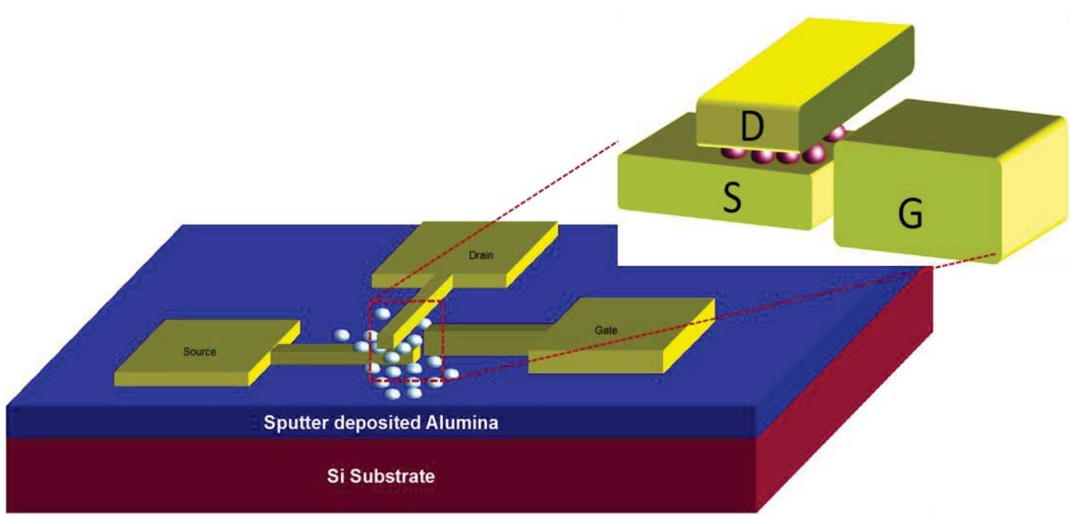


Fig. 3.29: Pictorial view of the device configuration for a vertical SET.

The vertical device needs multiple layers of nano structure to be fabricated one over the other with precise positioning. The fabrication of such a device using FIB etch and deposition method is difficult as it needs additional lithography steps with precise alignment at each layer of fabrication. Hence, the FIB based deposition process is used to fabricate such devices. Si/Al_2O_3 samples of size 5x5 mm were used for fabricating the vertical SET devices. After a thorough cleaning by piranha solution, the samples are introduced to the Hitachi-FB 2000A FIB system. The devices were fabricated in steps. In the first step, the source and gate electrodes are fabricated by the FIB deposition process. The deposition parameters for the electrode fabrication are given in the appendix section. It was noticed that during these deposition processes for continuous film fabrication, the dwell time and beam current are kept much lower than that for nano-island fabrication. Once the electrodes are fabricated, the probing pads of size 100×100um are deposited. The fabrication time for the gate electrode double that for the source electrode to increase thickness of the gate electrode

with respect to the channel location. This will help in uniform distribution of the gate electric field in the active part of the device.

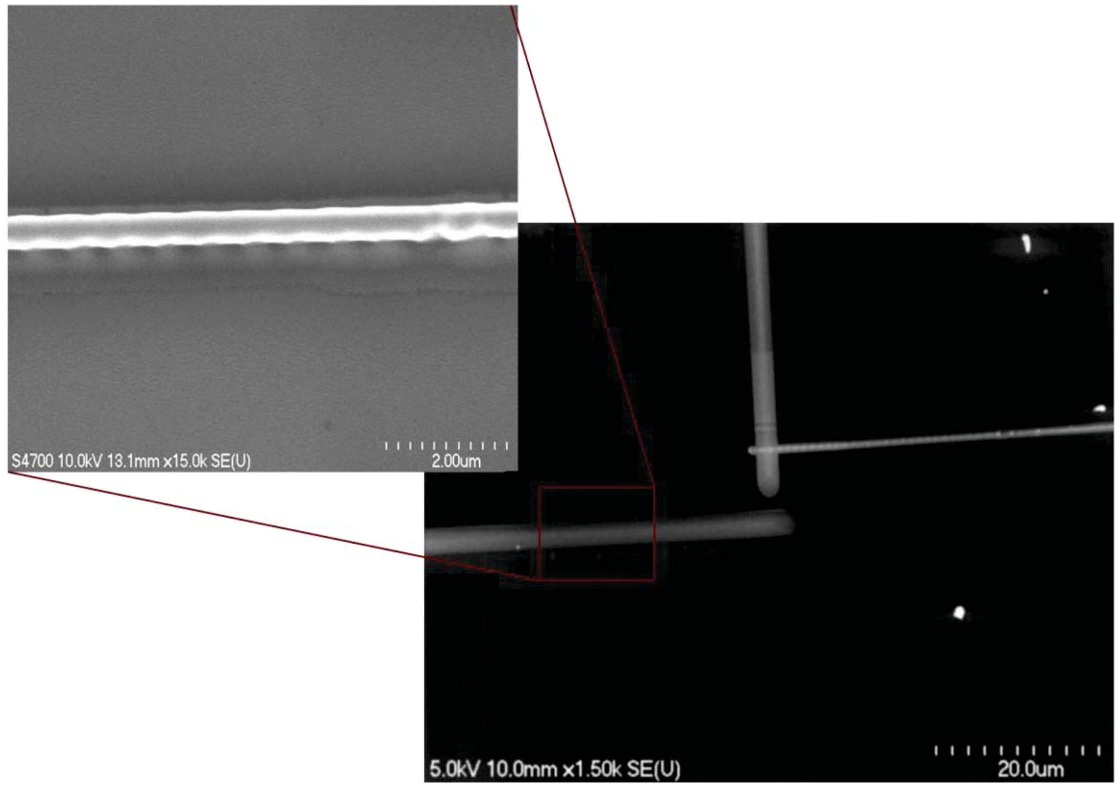


Fig. 3.30: SEM image of a vertical device. The extended figure shows the magnified view of an FIB deposited electrode.

The SEM image of the fabricated gate and source electrodes with the probing pads are shown in Fig. 3.30. It was observed that the minimum achievable distance between the gate and source electrode is ~300nm which is basically due to the resolution limit in the FIB deposition process. Once the source and gate electrodes are fabricated, the first layer of the tunnel junction must be fabricated. The samples are taken from the FIB system and a chemical oxidation process is done to produce the first layer of tunnel junction. As previously mentioned, peracetic acid, a mixture of H_2O_2 and acetic acid in the ratio 1:1, is

used for fabricating the tunnel junction layer. In the initial experiment the oxidation time for the electrodes are taken as 2mins which is same as that for the planar devices. However, it was observed that the FIB processing for depositing dots in the subsequent step etches out the entire oxide layer which results in the device electrically shorting. Therefore, the oxidation time for the gate and source electrodes is taken to be 4-5min. As the oxide thickness depends on the oxidation time, the resulted oxide thickness is thicker than that for an oxidation time of 2mins. The yielded oxide is expected to withstand the etching resulting from the subsequent FIB deposition process for the nano-island fabrication.

After the fabrication of the 1st layer of tunnel junctions, the samples are introduced again to the FIB system for deposition of the quantum dots. The quantum dots are deposited using the MI-200 beam in the Hitachi FB-2000A system with the same parameters as used for the sub-20nm based devices. The quantum dots are then oxidized for 3 mins by peracetic acid to form the second layer of tunnel junction. In the final step of FIB processing, the sample is further introduced to the FIB system for depositing the drain electrode and drain pad. This is again done using Beam-01. During the fabrication of the drain electrode, the deposition time is decreased to 2 mins from 3.5 mins (which was the deposition time for source electrode) to decreases the lateral overlapping. This helps in obtaining a narrower electrode hence the number of dots in the common overlap area can be decreased. As the background charges due to additional random dots can impact the gate controllability of the device [40], decreasing the number of dots in the common area for the source and drain electrode can potentially reduce this effect.

The passivation for the device is done by depositing a ~30nm thick Al_2O_3 layer. A physical vapor deposition process using a Perkin Elmer RF 2400-6J sputtering system is used

for depositing the Al_2O_3 layer using the parameters as described in the appendix section. In the subsequent step the source, drain and gate pads for the device are exposed for probing purposes by selectively etching the passivating alumina layer by FIB etching process. The FIB parameter for the etching process is detailed in the appendix section.

3.4.4 Silicon Quantum Dot Based SETs

All the devices and technologies described are based on a metallic island. Tungsten nano islands of size below 10nm are deposited using FIB deposition process and used as the conducting dots for the current transport in the SET device. Metallic quantum dots have continuous energy levels and the electron transport takes place only when the voltage given by the supply is more than the effective charging energy of the SETs. The controllability in the investigated SET device is expected to be poor, due to the random background charges in the additional dots and the randomness in the orientation and the size of the dots. One way to improve the gate controllability is to use semiconductor quantum dots instead of metallic dots. In semiconductor quantum dots as the energy levels are discontinuous, in addition to charging energy, alignment of the energy levels is required during the electron tunneling from the source to drain through the dots [98,99]. In a further investigation semiconductor quantum dot based fabrication was explored to improve the gate controllability in the RT-SETs. Silicon quantum dots of size below 10nm are fabricated to realize the semiconductor SETs.

In the fabrication of Si dot based SET devices, the greatest challenge is to fabricate the Si quantum dots of size below 10nm. In this effort, a novel method using FIB deposition technology has been used to fabricate sub-10nm sized Si quantum dots between source and

drain electrodes. As mentioned in the previous section, during FIB deposition process when the dwell time increases with the other parameters as constants, the deposition yield decreases due to the domination of the sputtering effect. For a higher beam currents like in the MI-200 beam, this sputtering dominant deposition can yield in depositing sub-10nm sized tungsten nano-islands for a dwell time of 9us or higher. However, it is observed that for intermediate values of dwell time (1-5μs) a discontinuous film of tungsten is deposited as shown in Fig. 3.31. Again, during the chemical oxidation process of the W dots in peracetic acid, it was observed that for a oxidation time of 20 mins or higher all the material can be oxidized and etched out by peracetic acid. Hence, the deposited discontinuous film can be used as a mask for the formation of Si quantum dots and can be further removed by etching it through peracetic acid.

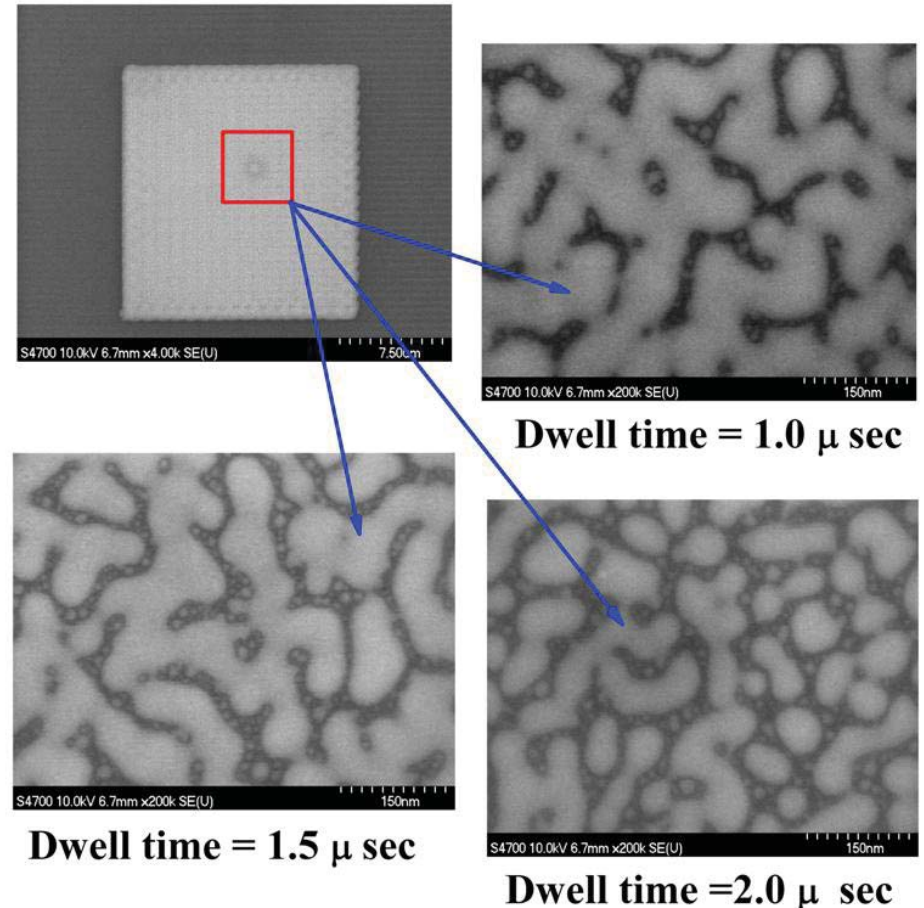


Fig. 3.31: SEM image of the discontinuous fabricated using FIB deposition technique [Reprinted with permission from P. S. Karre, PhD Dissertation, 2008].

This method was used for fabricating the Si quantum dots. A discontinuous W film of size 16x16um is deposited using FIB deposition technique. The parameters used for depositing the W film are given in Table-3.7. The SEM image of such discontinues film is given in Fig. 3.31. In the next step, a ~6nm thick poly-silicon film is deposited by physical vapor deposition process using a Perkin Elmer 2400-8J RF-Sputtering tool. In the following step the samples are dipped again in a peracetic acid solution for 30mins to oxidize and

remove the W film. Hence, the silicon remains as Si quantum dots. Ambient oxidation is used to form the oxide layers on the Si dots for the tunnel junction of the devices.

In further step, the source drain and gate electrodes are fabricated using FIB deposition technology using the parameters as mention for the vertical devices. Prior to the electrode fabrication, the area in the sample other than the active area (where quantum dots are present) was flashed by the MI-500 beam for 30sec to remove any additional Si layers which might short the electrodes during testing. The 100x100μm sized probing pads for the device were fabricated using the FIB deposition technology. And finally the devices were passivated by depositing a 30nm thick Al_2O_3 layer by the sputter deposition process. The exposure of the probing pads is achieved by etching the pad area by the FIB etching process. The process for fabricating this Si dot based device is shown in Fig. 3.32.

This technique used to fabricate the Si islands can also be used for fabricating other types of quantum islands. In an additional investigation, Cr islands of size below 10nm were also demonstrated using this technique.

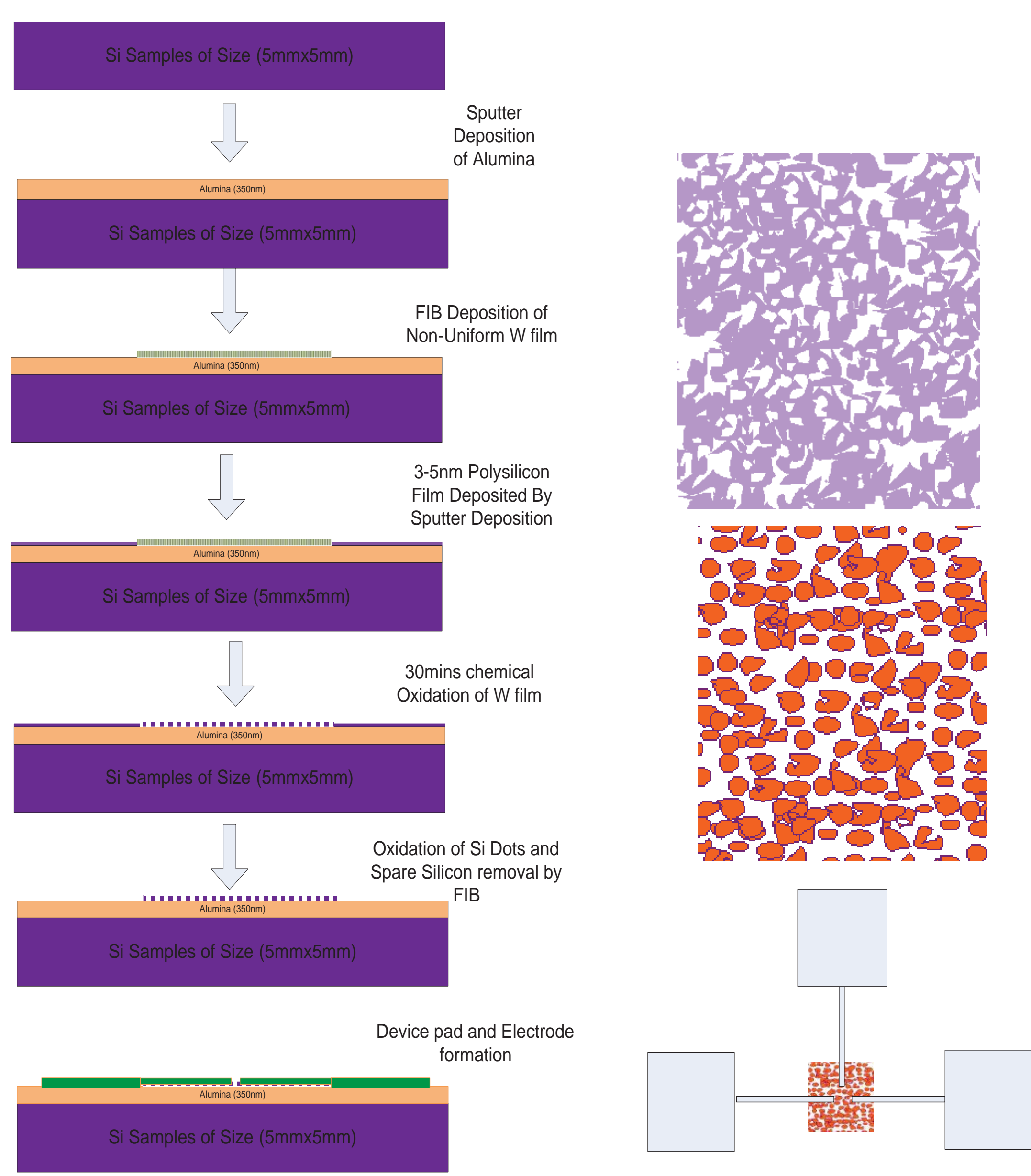


Fig.3.32: Process flow for fabricating Si dot based SET device.

Chapter 4: Device Characterization

Room temperature characteristics of the SET devices with different configurations are discussed in this chapter. The measurement set up and the method for characterization of the devices is described in Section 4.1. The characteristics of the devices fabricated using FIB etch and deposition technology is discussed in Section 4.2. Following these the results, the characteristics of the device with vertical source and drain configuration is discussed in Section 4.3. In Section 4.4, the characteristic of the SET devices with Si dots are discussed.

4.1. Experimental Set-Up for Device Characterization

From the modeling output of the studied SETs as discussed in Chapter 2, it can be observed that the expected output current range for the SET devices can be in the order of 1 to few hundred pA. Hence, characterization of these devices with such low output currents requires high a precision measurement set-up with proper impedance matching. The Keithley 4200-SCS Semiconductor Parametric Analyzer (SPA) with a current measuring capability of 0.1fA, has been used to characterize the SET devices. A Micromanipulator 8400 probe station has been used to probe the device pads and transfer the measuring signals

(voltage and current) between the device and the SPA. A pictorial view of the experimental set-up for the device characterization is shown in Fig. 4.1.

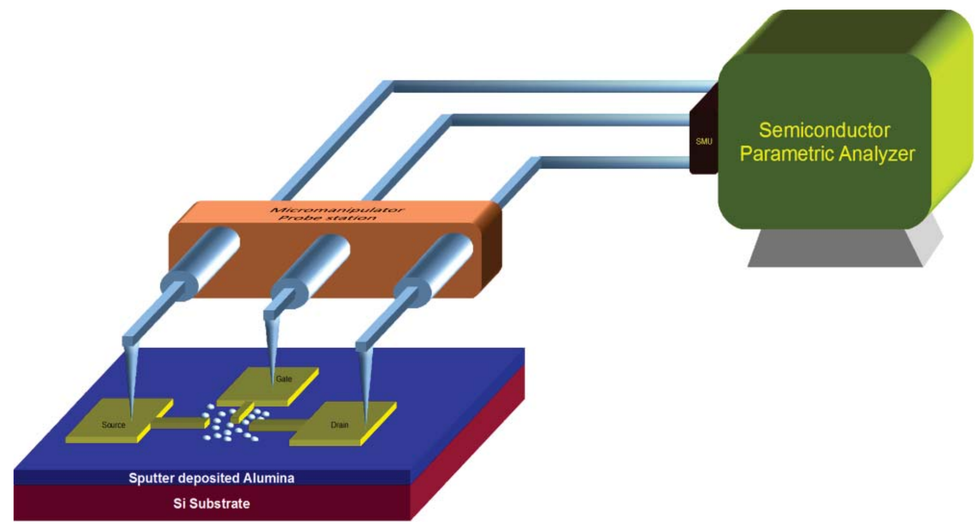


Fig. 4.1: A pictorial view of the measurement set-up for characterizing the SET devices.

Three probes with tip size of approximately 20-30μm were used for probing the source, drain and gate pads of the devices. Movement of these probes in x, y and z direction can be controlled by Micromanipulator 450/550 manipulators, with a one micron precision. The probes are arranged on the devices by using an optical microscope on the micromanipulator probe station. The individual probes are connected to the Source Measuring Units (SMU) of the SPA system through triaxial cables. The extra shielding in the triaxial cable protects the measuring signal from the ambient noise. To further avoid the ambient noise from interfering the measured signal, grounded pads and hand bands are used during the experiment. A digital image of the measurement set-up is shown in Fig. 4.2.

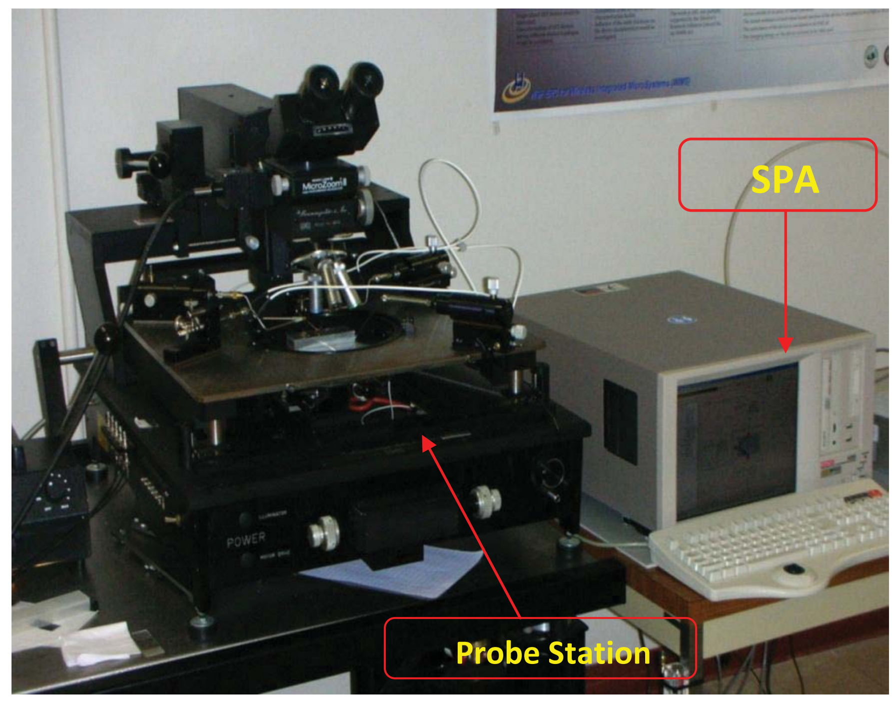


Fig. 4.2: Digital picture of the measurement set-up used for characterizing the SET devices.

After the probes are arranged on the device pads, the Keithley SPA system is set-up for the measurement. In the SPA system, a Visual C++ based software framework named Keithley Interactive Test Environment (KITE) has been used to obtain the measured data from the devices. The input parameters for the measurement are summarized in the appendix section.

In a SET device, the important characteristics required to verify the single electron charging effects are the Coulomb blockade effect and Coulomb oscillations. The Coulomb blockade effect can be observed in the Source-drain characteristic with different gate voltages. The Coloumb oscillation effect can be observed in the characteristic curve showing

the change in drain current with respect to the gate voltage for a fixed source to drain voltage.

To obtain the Coulomb blockade effect in source-drain characteristic, the voltage between source and drain terminal is swept from a negative value to a positive value for different gate voltages. This can be done in the SPA system by assigning the voltage parameters to the source pad connected SMU, as a voltage sweep and assigning the SMU drain pad connected as a ground terminal. The SMU connected to the gate terminal is assigned a voltage step. The sweeping of the voltage is possible by incrementing the voltage with constant incremental step. Depending on the start and stop point of the voltage sweep the step value determines the number of data point for the measurement. For the Keithley 4200 SPA system, the maximum number of data points available for any measurement is limited to 1000. Hence, the value of the incremental step must be defined in such a way that the total number of data points is always less than the maximum limit. Similarly, the voltage step in the gate terminal is defined by assigning a start and stop point along with the step value. This arrangement helps in sweeping the source drain voltage for different gate voltages.

In the gate-drain characteristic to obtain the Coulomb oscillation effect, the variation in the source-drain current with respect to the gate voltage needs to be measured. The measurement is performed by sweeping the gate voltage from a negative to a positive value for a fixed source to drain voltage. Measurement for different source to drain voltages can be performed by assigning a voltage step for the source to drain terminal.

Depending on the time taken for the measurement 4 different sampling modes are available in the Keithley 4200 SPA system. They are

- ✓ Fast mode
- ✓ Normal mode
- ✓ Quiet Mode
- ✓ Custom Mode

The total time required for the measurement is maximum in the quiet mode and minimum in the fast mode. However, the accuracy of measurement is better in the quiet mode compared to the fast and normal mode. The custom mode allows the user to set up the measurement time. For characterizing the SET devices quiet mode is used as accuracy is more important than the measurement time.

Another important parameter to be set up during the measurement is the compliance current. Compliance current is defined as the maximum current a voltage source is allowed to reach in its attempt to source the programmed voltage [100]. The set value of the compliance current must be greater than the measured value of the current to have accurate measurement. Considering the expected output current range to be in the order of few pA the value of the compliance current is set to be 0.1 to 1μA.

Once the measurement is configured, the V-I curve for both source-drain and gate–drain characteristic are obtained. In the source drain characteristic, clear Coulomb blockade is obtained. The characteristics of the Coulomb blockade are that, when the electrostatics of the system is not favorable for electron transfer, there is no increase in the drain current for an increase in the source-drain voltage, this is referred as Coulomb blockade. This measurement is repeated for different gate voltages and for different devices. Coulomb

oscillation is also observed in the gate-drain characteristic by sweeping the gate voltage for different fixed source drain voltages. Origin 7.5 plotting software package is used to obtain the required plot from the measured data [101].

4.2. Room Temperature Characterization of the FIB Etch Deposition based SET:

The SET devices are fabricated in a Cr layer deposited over a Si/Al_2O_3 sample using FIB etch and deposition technology. The nano structures for the device such as the electrode terminal, inter-electrode gaps and the probing pads are fabricated using FIB etching technology and the quantum islands are formed by FIB deposition technique. Chemical oxidation process is used to fabricate the tunnel junction for the device. The fabricated devices are Multi tunnel junction based SETs as more than one dots are involved in the current conduction. The number of dots participating in the in the dominant conduction path for the electron transport depends on the inter electrode gap between the source and drain electrode and the size of the dots.

For room temperature operation of the SETs the effective capacitance of the device has to be in the order of aF. The size of average diameter of the deposited dots is ~8nm and the width of the chemically formed tunnel junction is ~2nm. This makes the effective capacitance low enough for room temperature operation of the SETs. The total number of dots participating in the dominant conducting path for the electron transport also impacts on the total effective capacitance. Devices with variation in the source to drain gaps are fabricated to understand the impact of number of islands in the dominant conducting path

on the device behavior. The minimum gap achieved was ~17nm having ~1 to 2 dots taking part in the conduction process.

4.2.1. SET with 17nm Source-Drain gap:

SET devices with a minimum source drain gap of 17nm and a gate gap of 50nm are fabricated by optimizing the thickness of the active Cr layer. The width of the source drain and gate terminals are ~150nm. SEM image of the active area of such a device prior to the dot deposition is shown in Fig. 4.3. .Assuming the mean diameter of the nano-islands to be 8nm and the width of the tunnel junction to be ~2nm, it is expected that more than one parallel path are available for the electron to travel from the source to drain electrodes. However, the electron tunneling will take place through only one array of dots which is energetically most favorable. As described previously, this array is called the dominant conducting path (DCP). In this particular device, it is expected that only 1-2 dots are participating in the dominant conducting path.

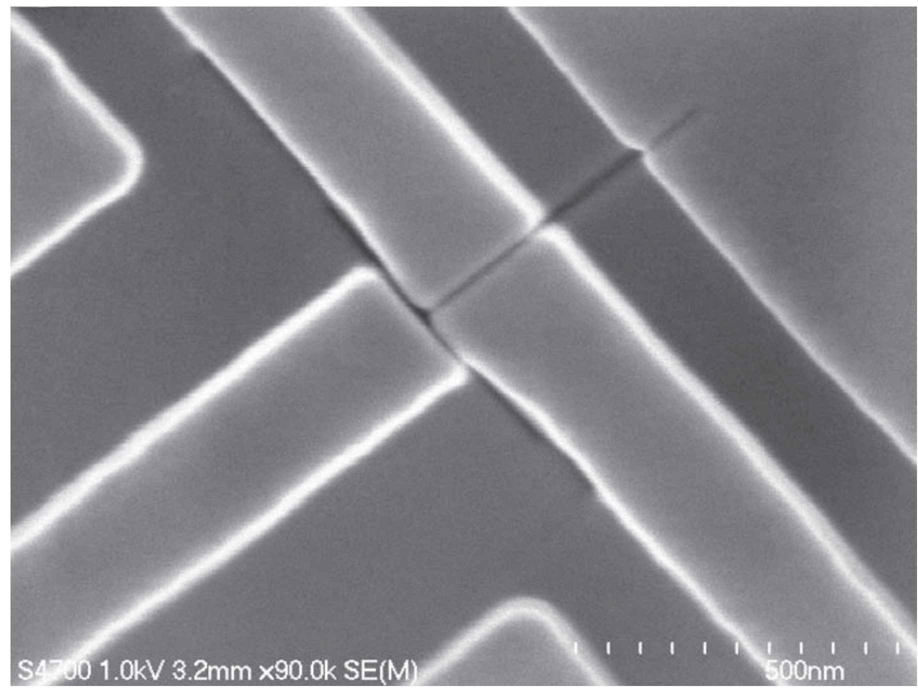


Fig. 4.3: SEM image of the nano structure for the SET with 17nm Source-drain gap.

The source drain characteristic of the 17nm device is shown in Fig. 4.4. The change in drain current is recorded by sweeping the voltage between the source and drain terminal from -5V to +5V. It can be observed that the experimental drain current is on the order of a few hundred pA in range. To observe the impact of the gate voltage, the measurement was done for different gate voltages. The Coulomb blockade region is defined as the "off" state of the device where the drain current reaches to zero for a non-zero value of the source-drain voltage. The blockade length can be calculated as the period of voltage for which the current is in ±7% of its minimum value [39]. As shown in Fig. 4.4 clear Coulomb blockade effect is observed at room temperature for different gate voltages. The length of the Coulomb blockade is ~1.1V for a gate voltage of 10mV, yielding a threshold voltage ~550mV. The observed threshold voltage is much lower than that for a deposition based

device reported previously by Karre, et al. which was on the order of ~2V. Also, a substantial improvement in the gate controllability of the device is observed.

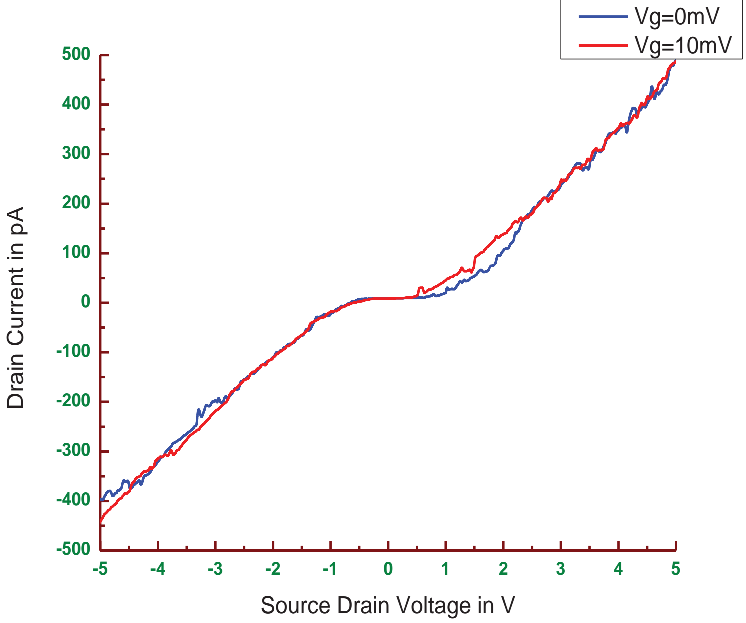


Fig. 4.4: Coulomb blockade characteristic of a 17nm source-drain gap based SET device.

The drain current vs gate voltage characteristic of the device is obtained by sweeping the gate voltage for different source drain voltage. The magnitude of the source drain voltage was chosen within the blockade voltage range so that the Coulomb oscillations can be observed due to charge quantization effects in the nano-island. Coulomb oscillation in the drain current and the conductance with respect to the gate voltage is observed as shown in Fig. 4.5. Each oscillation represents the charging and discharging of the quantum island by one electron or packet of electrons resulting from the Coulomb blockade effect. For a single dot based SET device, the Coulomb oscillations are periodic, but for a multi-dot based SET

device non periodic Coulomb oscillations are observed due to inter-dot electron-electron interactions [102]. For the fabricated device, the aperiodicity and the appearance of the multiple peaks in the Coulomb oscillations can be attributed to the randomness in the size and positional distribution of the nano islands. The gate voltage is swept from -300mV to 300mV and it can be observed from Fig. 4.5 that the drain current oscillates with an average period of ~90mV.

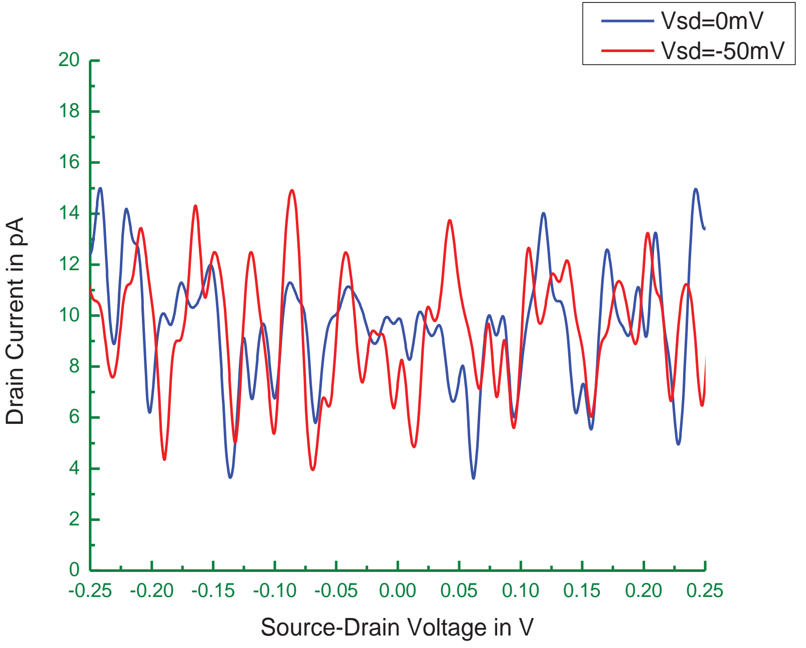


Fig. 4.5: Coulomb oscillation for a device with 17nm source-drain gap.

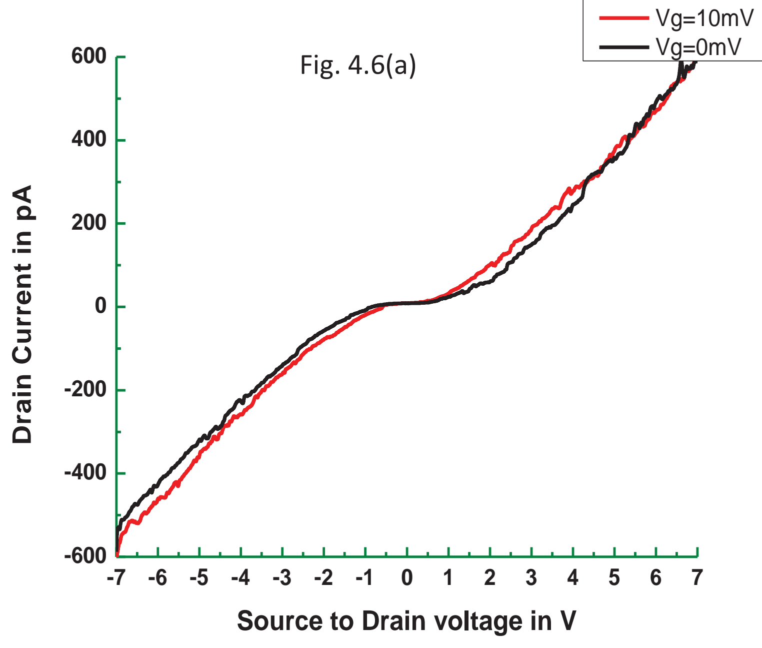
4.2.2. SETs with variable Source to drain gap

SET devices with varied inter-electrode gaps between source and drain are fabricated to study the impact of geometrical variation on the device behavior. In the fabrication process the variation in the source to drain gap is achieved by varying the dwell time and the

number of runs during FIB etching process. Source drain gaps are varied from a minimum of 17nm to a maximum of 250nm. The maximum value of the gap is taken to be 250nm to compare the behavior of the resultant device with the previously developed deposition based device by Karre, et al. [69] which had a source drain gap of the same order.

The Coloumb blockade characteristic of the devices is obtained by sweeping the source drain voltage from a negative to a positive value for different gate voltages. Drain current suppression for lower source-drain voltages representing the Coulomb blockade region is observed in each of the devices. It is also observed that the length of the blockade varies with the source drain gap in the devices. The details about the variation in the behavior of such devices are discussed in the following chapter (Chapter-5). Figures 4.6(a) and 4.6(b) represent the source-drain characteristic of devices with the source drain gap of 35nm and 150nm.

The Coulomb oscillation characteristic the devices are obtained by sweeping the gate voltage for different source drain voltages. The magnitude of the source drain voltage was chosen within the blockade voltage range so that the Coulomb oscillations can be observed due to charge quantization effects in the nano-island. Coulomb oscillation in the drain current and the conductance with respect to the gate voltage is observed for devices with source drain gap of 50nm and 100nm as shown in Fig. 4.7.



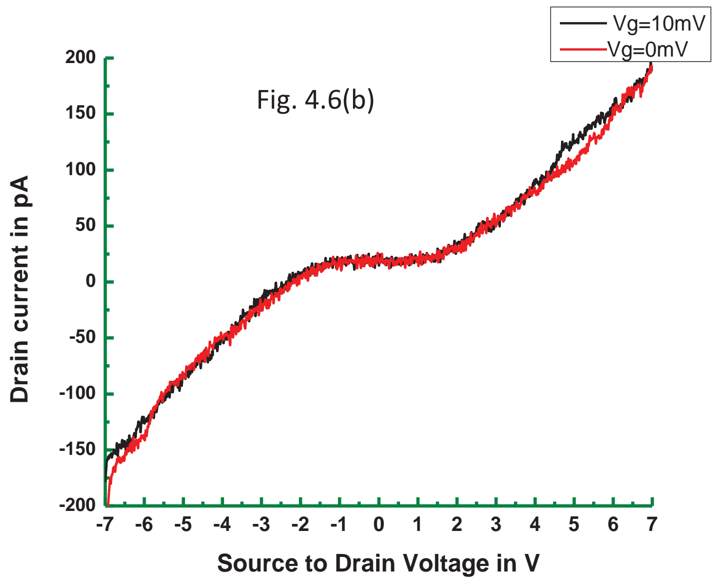


Fig. 4.6: Coulomb blockade characteristic of SET devices with different source to drain gap (a) S-D gap=35nm (b) S-D gap=150nm.

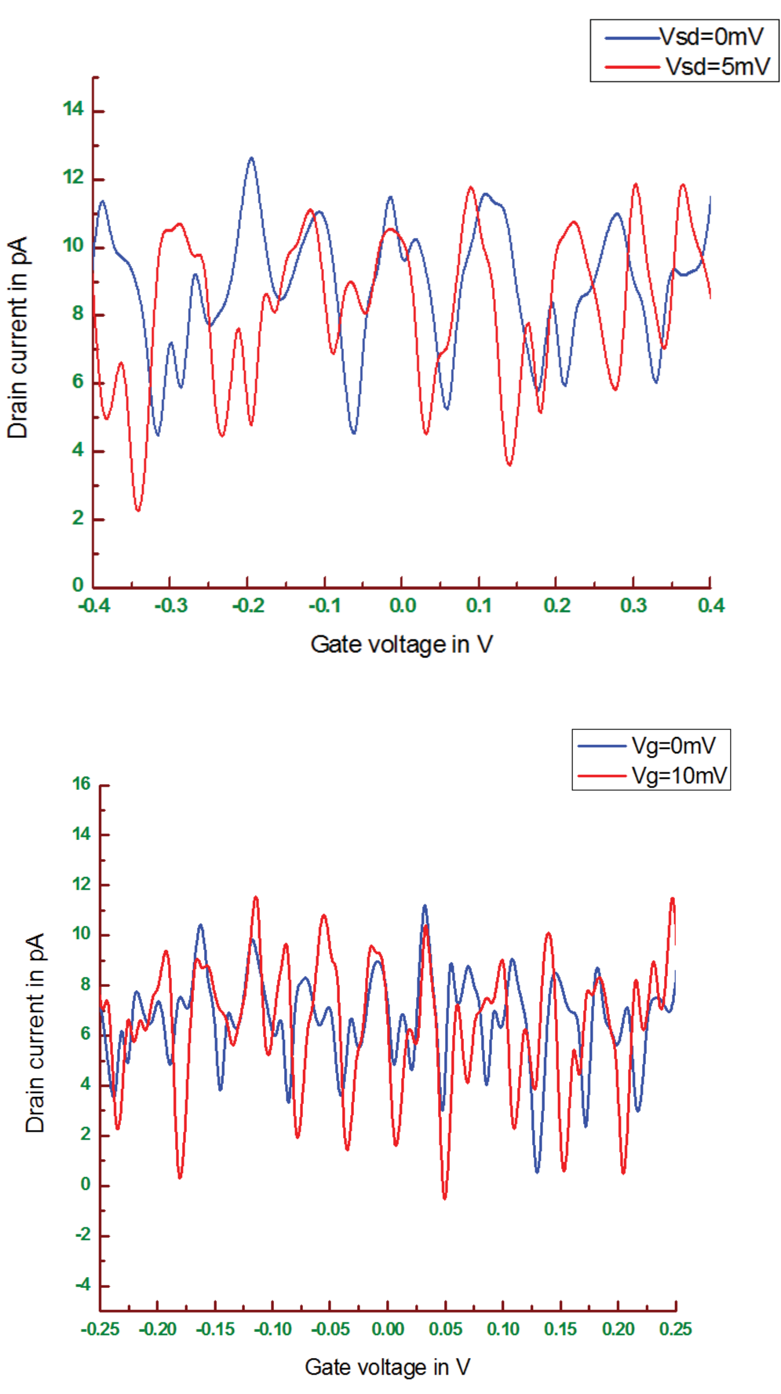


Fig. 4.7: Coulomb oscillation characteristic of FIB etch deposition based SET device with (a) 35nm source-drain gap and (b) 150nm source-drain gap.

4.3. Characterization of Vertical SET devices:-

The devices fabricated by FIB etch and deposition processes are planar devices having multiple numbers of quantum islands taking part in the dominant conducting path for the electron transport. The vertical device is fabricated using FIB deposition technology to realize a single dot behavior in the SET. The FIB deposited nano islands are sandwiched between the source and drain electrodes. This configuration ensures the existence of only one dot taking part in the dominant conducting path for the electron transport process. The configuration for this device is shown in Fig. 4.8.

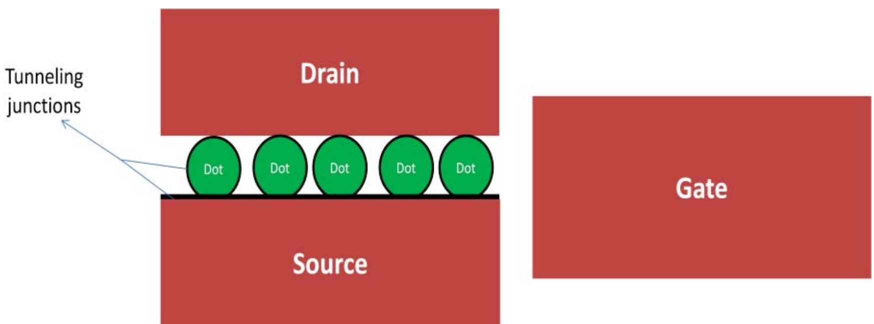
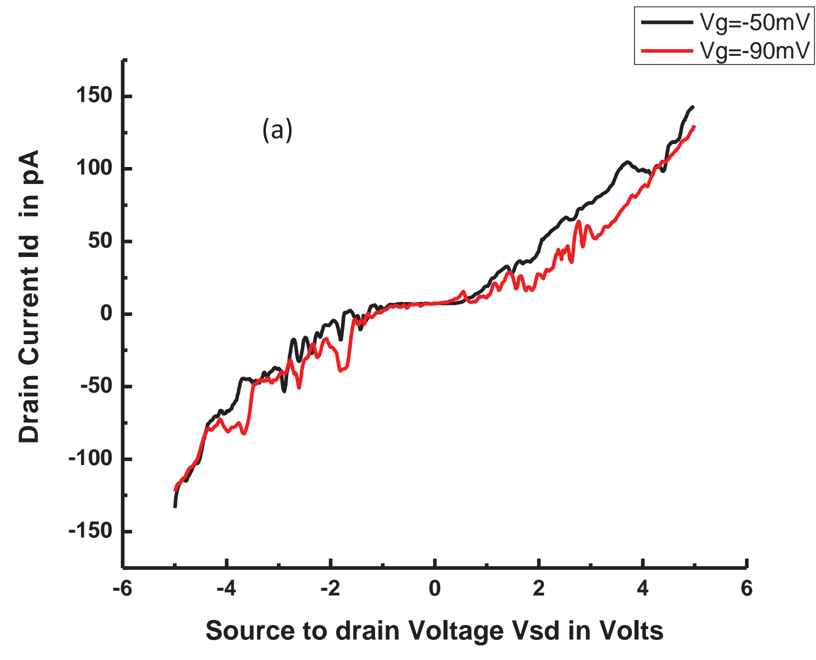


Fig. 4.8: Configuration of a Vertical SET device.

The source drain characteristic of the vertical SET device is shown in Fig. 4.9. The change in drain current is obtained by sweeping the voltage between the source and drain terminal from -5V to +5V. It can be observed that the obtained drain current is on order of a few hundred pA in range. To observe the impact of the gate voltage, the measurement was done for different gate voltages. As shown in Fig. 4.9(a), a clear Coulomb blockade effect is observed at room temperature for different gate voltages.



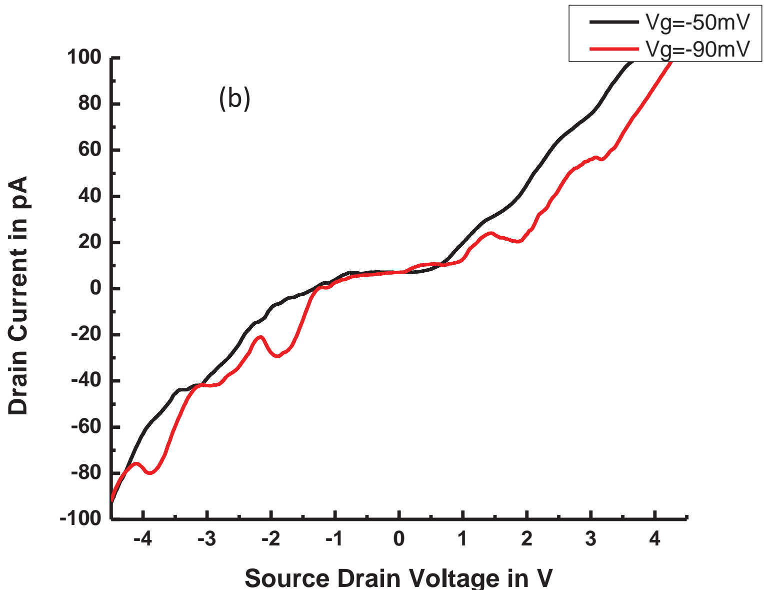


Fig. 4.9: Source-drain V-I characteristic of a Vertical SET device for two different gate voltages (a) Original Data (b) Smoothen by averaging 30adjacent points.

The length of the Coulomb blockade is ~1.2V, hence the threshold voltage ~600mV. It can be observed that the drain current fluctuates for higher source-drain voltage. In further investigation to study these fluctuation, a plot with averaging of 30 adjacent points is obtained and shown in Fig. 4.9(b). Clear Coulomb stair case behavior is observed in this smoothened curve. The length of the stair case decreases with higher gate voltage. Hence, the filtered out noise could be attributed to multi tunneling generated short noise [46]. For this particular configuration, the possibility of having multiple tunneling is higher as there is just one dot in parallel paths for current conduction between source and the drain terminals [103].

The gate terminal for the vertical SET device is placed laterally to the source and drain terminal. The height of the gate electrode is intentionally made higher than that for the source /drain electrode to minimize the fringing effect in the gate electric field. The drain current vs gate voltage characteristic of the device is obtained by sweeping the gate voltage for different source drain voltage. The magnitude of the source drain voltage was chosen within the blockade voltage range so that the Coulomb oscillations can be observed due to charge quantization effects in the nano-island. Coulomb oscillation in the drain current and the conductance with respect to the gate voltage is observed as shown in Fig. 4.10. Each oscillation represents the charging and discharging of the quantum island by one electron or packet of electrons resulting from the Coulomb blockade effect. Multiple peaks and non-periodic oscillation was also observed in this device due to the multiple dots surrounding the dominant conducting path with randomness in size and positional distribution. The gate voltage is swept from -40mV to 0 mV and it can be observed from Fig. 4.5 that the drain current oscillates with an average period of ~10mV.

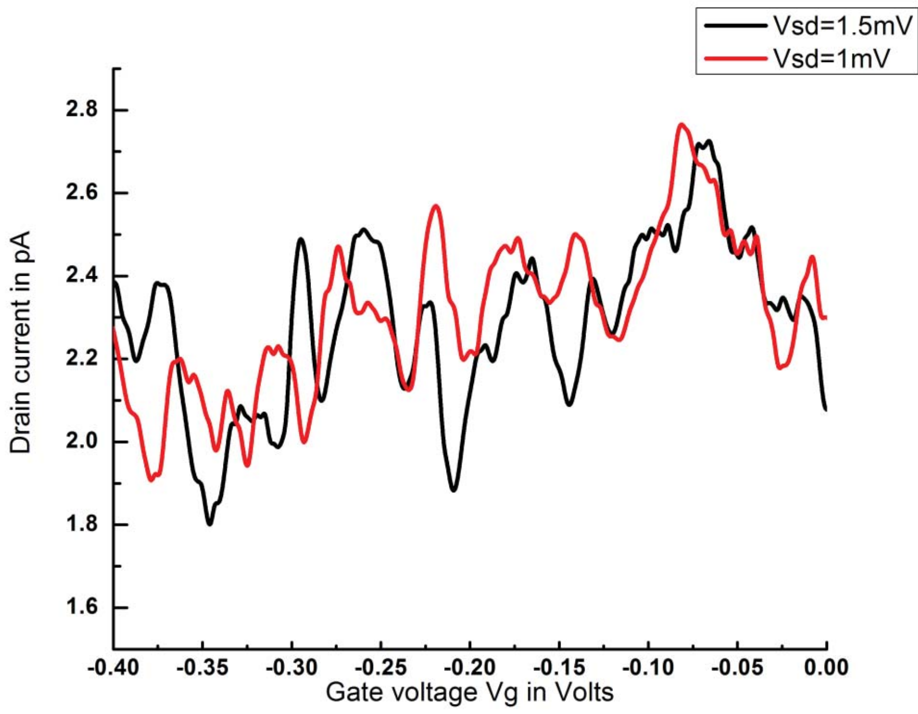


Fig.4.10: Coulomb oscillation for a vertical SET device

4.4. SET with Silicon Quantum Dots:

The SET devices studied so far use the FIB deposited tungsten nano islands as the central islands for the electron transport. Being metallic quantum dots, the tungsten nano islands have continuous energy states and an equilibrium position in the chemical potential is required for tunneling of electron from the source to the dot and from one dot to the other. On the other hand, for semiconductor quantum dots the energy levels are discontinuous. Hence, energy level alignment along with chemical potential equilibrium conditions must be satisfied for any tunneling event. This makes the semiconductor dots to be more preferred for SET devices when the gate controllability is a concern.

In the fabricated tungsten quantum dot based SET devices, Coulomb blockade is demonstrated at room temperature. With design enhancement the devices also shows room temperature characteristic with improved threshold voltage. However, gate controllability of the drain current in the W dot device is still far from a satisfactory level. Also, the appearance of multiple peaks in the Coulomb oscillation plot due to the randomly oriented dots raises questions regarding the functionality of the device.

Hence, in an effort to improve the device functionality regarding the gate controllability and the periodicity of the Coulomb oscillations, Si quantum dot based SET devices are fabricated and characterized at room temperature. For the Si dot based device the Si quantum dots are fabricated by using a FIB deposited discontinuous tungsten film as a masking layer. The FIB deposition technique is used for depositing the source, drain and gate electrodes and probing pads. A native SiO_2 is used as the tunneling junction for the device.

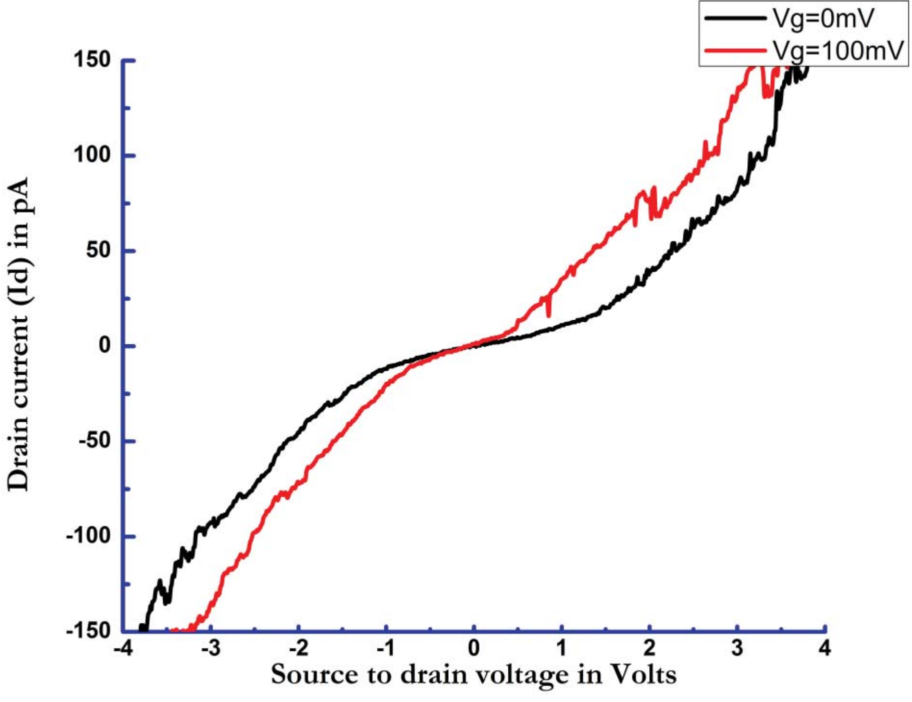


Fig. 4.11: V-I characteristic of a Si quantum dot based SET device at room temperature.

The room temperature Coulomb blockade characteristics of such a Si quantum dot based SET is shown in Fig. 4.11.The change in drain current is recorded by sweeping the voltage between the source and drain terminal from -5V to +5V. It can be observed that the obtained drain current is also on the order of a few hundred pA, similar to the tungsten dot based devices. To observe the impact of the gate voltage, the measurement was done for different gate voltages. The Coulomb blockade region is defined as the "off" state of the device where the drain current reaches to zero for a non-zero value of the source-drain voltage. As shown in Fig. 4.11, clear Coulomb blockade effect is observed at room temperature for different gate voltages. It can also be observed that the length of the

Coulomb blockade and hence the "Off" state for the device decreases with increase in the gate voltage. This behavior portrays the improvement in the gate controllability effect by using semiconductor quantum dots. From Fig. 4.11 it can be observed that by increasing the gate voltage from 0mV to 100mV the threshold voltage changes from 1V to 500mV.

The drain current vs. gate voltage characteristic of the Si dot based device is obtained by sweeping the gate voltage for different source drain voltage. The magnitude of the source drain voltage was chosen within the blockade voltage range so that the Coulomb oscillations can be observed due to charge quantization effects in the nano-island. Coulomb oscillation in the drain current and the conductance with respect to the gate voltage is observed as shown in Fig. 4.12. Each oscillation represents the charging and discharging of the quantum island by one electron or packet of electrons resulting from the Coulomb blockade effect. For a single dot based SET device, the Coulomb oscillations are periodic, but for a multi-dot based SET device, a non periodic Coulomb oscillation is observed due to multiple charging effect [102]. However, the periodicity for this semiconductor based device is improved compared to the tungsten dot based device. The existent aperiodicity and the appearance of the multiple peaks in the Coulomb oscillation can be attributed to the randomness in the size and positional distribution of the nano islands. The gate voltage is swept from -300mV to 300mV and it can be observed from Fig. 4.12 that the drain current oscillates with an average period of ~90mV.

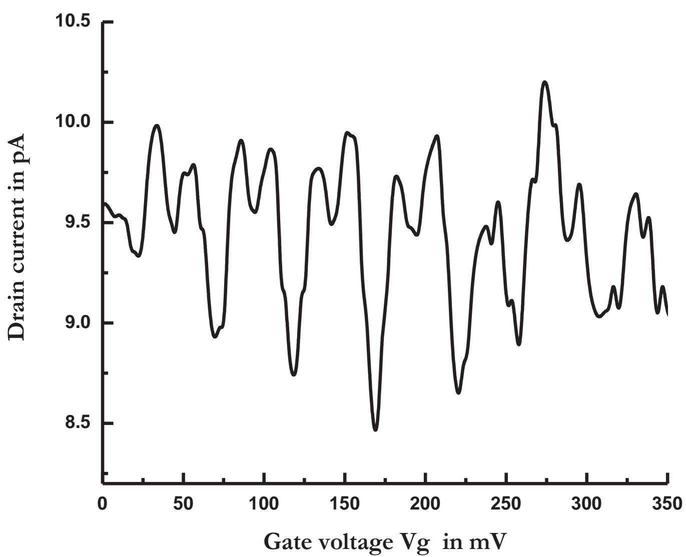


Fig. 4.12: Coulomb oscillation for a Si dot based SET.

Chapter 5: Analysis and Discussion

5.1. Extraction of Device Parameters

In a SET device the charging energy, junction capacitance and the tunnel resistance are the key parameters on which the characteristic of the device depends. For a single dot based SET device, these parameters can be easily calculated by electro statically analyzing the nano structures for the device. But for the SET devices fabricated with multiple dots, an indirect method must be used for extracting the device parameters. Knowing the number of quantum islands taking part in the Dominant Conducting Path (DCP), the device parameters can be estimated from the measured data by using orthodox theory [104]. Hirvi and Pekola, et al. derived analytically, the relationship between the dip in conductance and the device parameters for multiple tunnel junction based SETs as expressed in Eq. 5.1. Assuming that the tunnel junctions within the SET device have uniform tunnel resistance and junction capacitance, the relation between the conductance G and the charging energy E_c can be represented as shown in Eq. 5.1[105].

$$\frac{G}{G_T} = 1 - 2\sum_{i=1}^{N} \frac{R_{T,i}}{R_\Sigma} \frac{\Delta_i}{k_B T} g\left(\frac{R_{T,i}}{R_\Sigma} eV / k_B T\right) \tag{5.1}$$

Where,

$$g(x) = \left[x \sinh x - 4\left(\sinh\left({}^{x}/_{2}\right)\right)^{2}\right]/8\left(\sinh\left({}^{x}/_{2}\right)\right)^{4};$$

$$N = Number\ of\ junctions\ inthe\ DCP\ for\ the\ device;$$

$$G = Conductance\ of\ the\ device;$$

$$G_T = Asymptotic\ conductance\ for\ higher\ \ drain\ voltage;$$

$$R_T = Tunnel\ resistance\ for\ each\ junction;$$

$$R_\Sigma = \sum_{i=0}^{N} R_{T,i};$$

Rigorous computation is required to solve the expression in Eq. 5.1 for non-uniform junctions in the DCP. However, assuming that the junction resistance and the capacitance are uniform in each junction, the expression can be simplified and expressed as given in Eq. 5.2 [69,105].

$$\frac{\Delta G}{G_T} = \frac{E_c}{3k_B T}\frac{(N-1)}{N} \tag{5.2}$$

where, ΔG is the dip in the conductance; k_B Boltzmann's constant; and T is the temperature in K. The charging energy E_C can be expressed as $E_c = \frac{e^2}{2C'}$, where $C'$is the capacitance of the array of N junctions. Considering the average size of the dots to be ~8nm the number of junction N can be determined by knowing the source-drain gap of the device. The capacitance of the individual junction C can be related to the total capacitance of the array as shown in Eq. 5.3 [69].

$$C' = \frac{NC}{2(N-1)} \tag{5.3}$$

A plot between the normalized conductance and the source drain voltage is obtained and shown in Fig. 5.1 using the measured data from the device characterization. The dip in the conductance $\frac{\Delta G}{G_T}$ is derived from this plot. The dip in conductance value can further be used to find out the charging energy and the junction capacitance using Eq. 5.2 and 5.3. The resistance of the tunnel junctions, which is related to the charging energy, the temperature of operation and the number of tunnel junctions in an array, is also calculated.

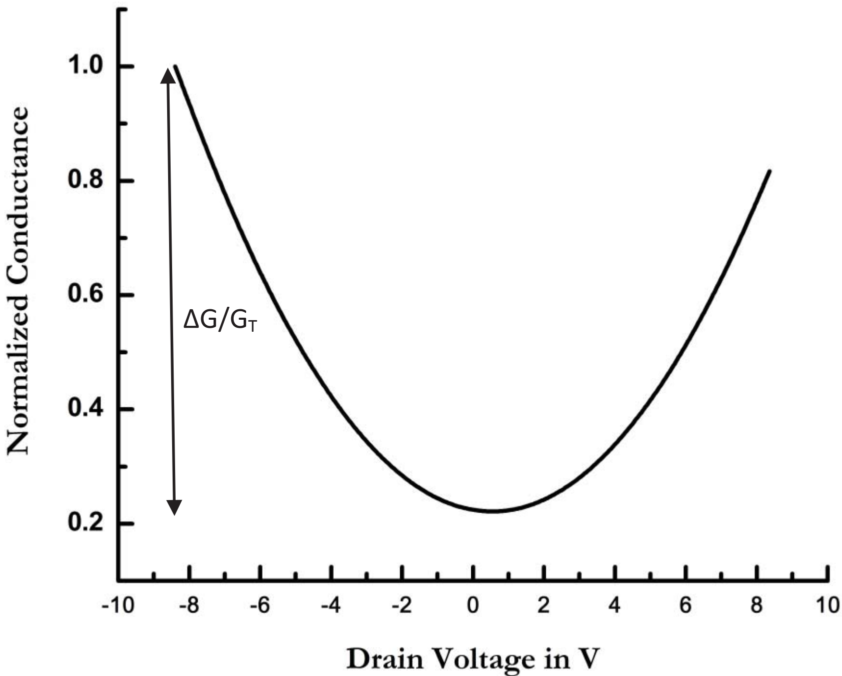


Fig. 5.1: Normalized conductance with respect to drain voltage.

The device parameters for the different device configurations are extracted utilizing the Coulomb blockade characteristic of the devices. To obtain the dip in conductance the differential conductance is calculated from the source-drain characteristic of the device and then the normalized value of the conductance is plotted against the source drain voltage.

From this calculation it is observed that the charging energy for all the devices is more than 130meV, which is almost 5 times higher than the thermal energy at room temperature. This makes it possible for the devices to demonstrate Coulomb blockade effect at room temperature. The obtained capacitance for each junction is also in the range of 10^{-19} or smaller which is much less than the critical value for room temperature operation. The error margin in this calculation is obtained simply by the maximum and minimum value of the obtained data for particular device.

5.2. Impact of Structural Variation on the Device Behavior

SET devices with different structural configurations are fabricated to study the impact of structural parameters on the device behavior. The different device configurations and fabrication methods are discussed in detail in the fabrication chapter (Chapter 3). Comparing the V-I characteristics of different devices it can be observed that the blockade length changes for different configurations. Therefore, it is important to study the effect of structural variation on the device output characteristics to optimize the structural parameters for a SET device operating at room temperature.

5.2.1. Impact of Source-Drain Gap

The inter-electrode gap between the source and drain terminals has a direct impact on the device characteristics and device parameters. For the fabricated multi dot based devices, the source to drain gap determines the length of the dominant conducting path (DCP) and the number of dots taking part in the DCP. Hence, the source drain gap has direct impact on

the electron transport process. The overall capacitance of the device is also related to the source drain gap as it determines the number of series capacitances associated with the current transport process.

To study the impact of source drain gap, Cr electrode and W dot based devices are fabricated using FIB etch and deposition technology with varying source drain gaps. The width of the source, drain and gate electrode terminals are kept constant at 150nm. The source-drain (S-D) gap is varied from 17nm to 250nm, with a fixed gate gap of 50nm. The maximum gap is taken as 250nm to compare device characteristics with the deposition based RT-SET devices developed by Karre, et al. [69]. The rest of the process parameters, such as the oxidation time and thickness of the passivation, are layer kept constant for all the devices. The V-I characteristic of the devices at room teperature with different source drain gap, starting from 17nm to 250nm is shown in Fig. 5.2.

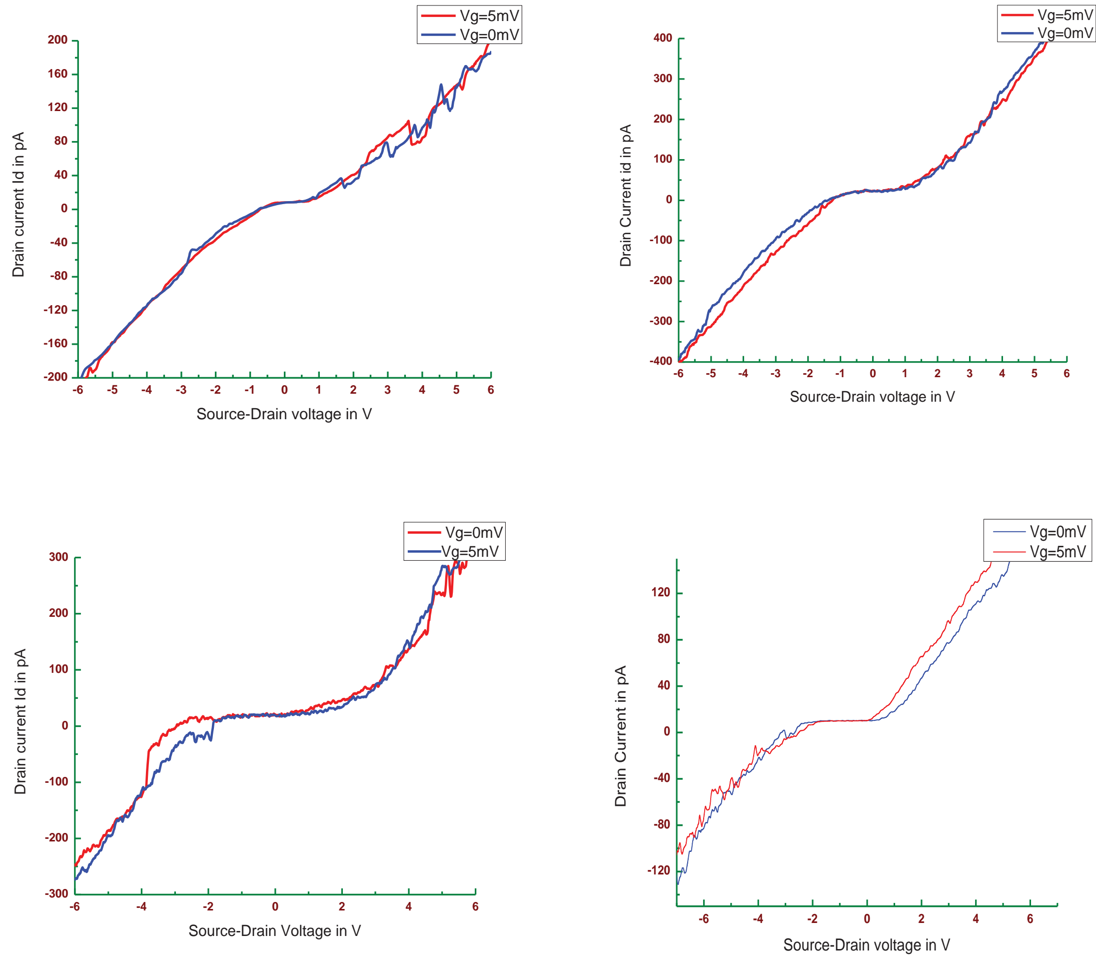


Fig. 5.2: Room temperature V-I characteristic of the SET devices with different source drain gaps (top left) ~ 17nm (top right) ~37nm (bottom left) ~50nm (bottom right) 150nm. The electrode width and the gate gap for all the devices are kept constant as 100nm and 50nm respectively.

From Fig. 5.2 it can be observed that the source drain gap has significant impact on the current suppression region in V-I plot for the devices. The length of the Coulomb blockade region increases with increase in the source-drain inter-electrode gap. Hence, the threshold voltage V_t which is half of the Coulomb blockade length can be reduced by decreasing the

source drain gap. This result agrees with the previously reported device at 4.2K temperature operation by Cordon et al.[46]. However, room temperature observation of this Coulomb blockade modulation effect by controlling the source-drain gap makes this effort unique and novel. The variation in threshold voltage with respect to the source to drain gap is shown in Fig. 5.3. The vertical error bars represents the maximum and minimum value of the threshold voltage for the particular SD gap.

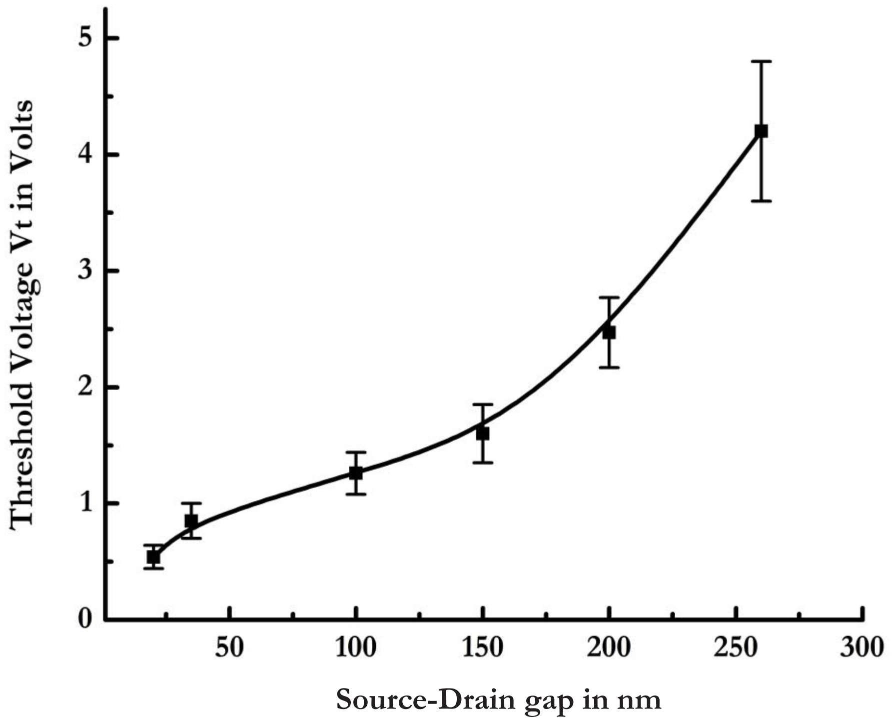


Fig. 5.3: Variation of the Threshold voltage with respect to the Source-Drain gaps

Other than the Coulomb blockade length and the threshold voltage, another important parameter studied is the charging energy. It is expected that the charging energy is directly proportional to the source-drain gap. This is because with an increase in source-drain gap,

the number of series capacitances associated with the DCP increases and hence the total effective capacitance decreases. As the charging energy is inversely proportional to the overall capacitance, it increases with an increase in the source-drain gap. To observe this effect, the charging energy and the overall capacitance for SET devices with varying source-drain gap are extracted as explained in Section 5.1. The variation of these two parameters with respect to the source-drain gap is shown in Fig. 5.4. As expected, an increasing trend in the charging energy and a decreasing trend in overall capacitance with respect to the source drain gap is observed as shown in Fig. 5.4.

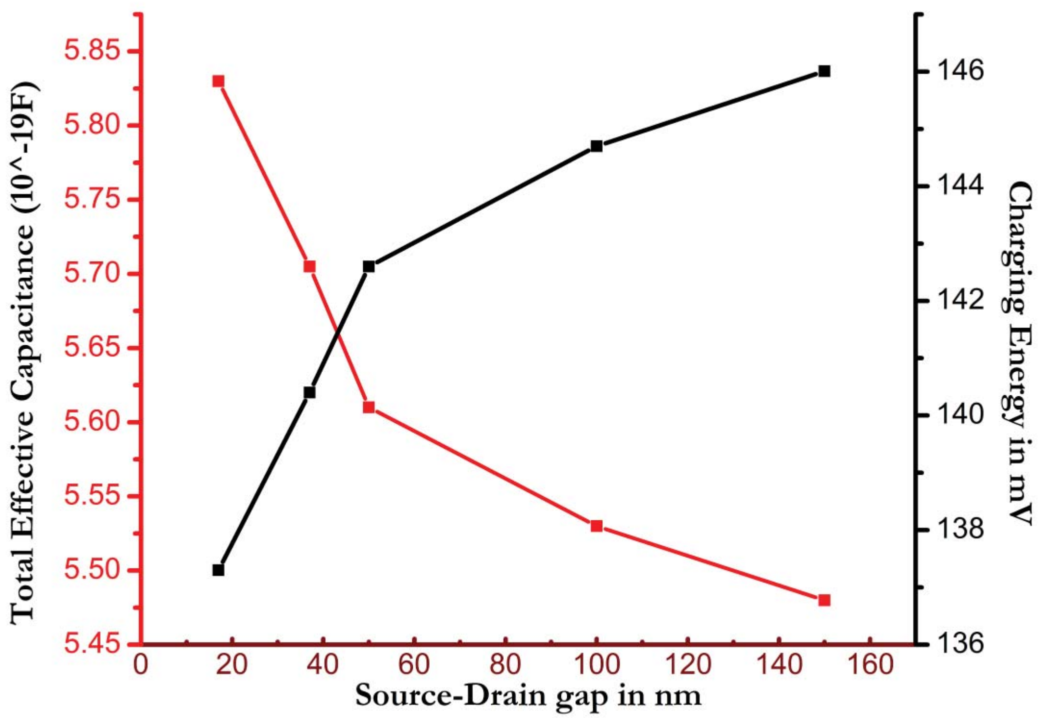
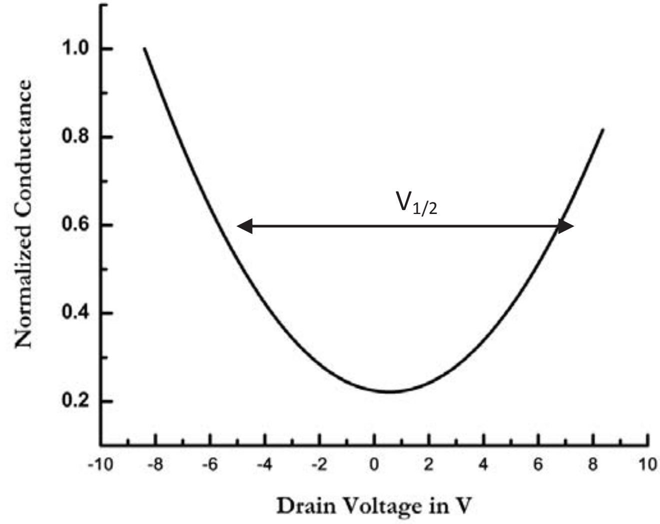


Fig. 5.4: The variation of charging energy and total effective capacitance with respect to the source drain gap.

The dependence of the device behavior on the source-drain gap can also be traced from the differential conductance plot as shown in Fig. 5.1. Theoretically, it can be predicted that full width half maximum voltage ($V_{1/2}$) in a conductance plot is directly proportional to the number of tunnel junction N taking part in the current conduction process for a multi dot SET devices [104,105]. To validate the above relationship for the fabricated devices at room temperature, the $V_{1/2}$ for each device is calculated from the conductance plot. As the number of junctions in the DCP depends on the source drain gap, an increasing trend in the $V_{1/2}$ is

observed with respect to the source drain gap. Figure 5.5 shows the dependency of $V_{1/2}$ in the normalized conductance plot with respect to the number of junctions and/or source drain gap as obtained from the experimental data. The red line shows the fitted linear curve of the experimental data. The variation of $V_{1/2}$ with respect to the number of junctions is close to linear with a slope of 0.326. This behavior validates the theoretical prediction of the model derived by Pakola, et al. [104]. A small non linearity in dependency can be attributed to the non-uniform tunnel resistance and junction area for various tunnel junctions. This fact is also experimentally demonstrated by the same group in a different work [104,105].



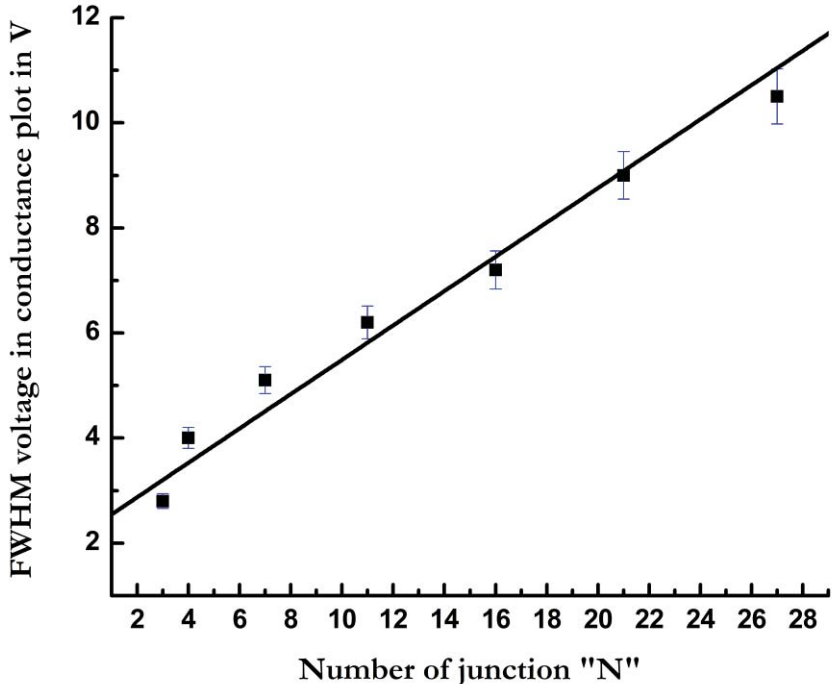


Fig. 5.5 (Top) Representation of $V_{1/2}$ in a conductance plot. (Bottom) The dependency of FWHM voltage $V_{1/2}$ in the conductance plot with respect to the number junction in the DCP (source-drain gap) for room temperature operating SET devices.

5.3 Impact of Topological Variation on the Device Behavior

5.3.1: 3-Dimensional Devices

Studying the impact of the device topology on the characteristic of the device is important to optimize the device configuration and design for improved functionality. This study is carried out by fabricating and characterizing SETs with different topological configuration. Along with the already discussed side-gated planar devices, three other devices with vertical configurations are fabricated as discussed below.

1. **Vertical Source Drain devices**- The source and drain electrodes are fabricated in two different plains sandwiching the nano-islands. The FIB deposition technique is used to fabricate this device.
2. **Top Gate device** - The source, drain and the nano-islands are fabricated in one plain and the gate electrode is fabricated above this plain on a 50nm thick Al_2O_3 dielectric layer. The fabrication of the gate electrode is done using the FIB deposition process. The source and drain electrodes are fabricated by FIB etching whereas the gate electrode is fabricated by FIB deposition.
3. **Bottom Gate device** – First, the gate electrode is fabricated on the Si/Al_2O_3 sample and then the source and drain electrode and the nano-islands are deposited over a 50nm thick Al_2O_3 dielectric layer. The source, drain and gate are fabricated using the FIB deposition technique.

The pictorial views of such devices are shown in Fig. 5.6. The dimensions of the device terminals are given in Table 5.1.

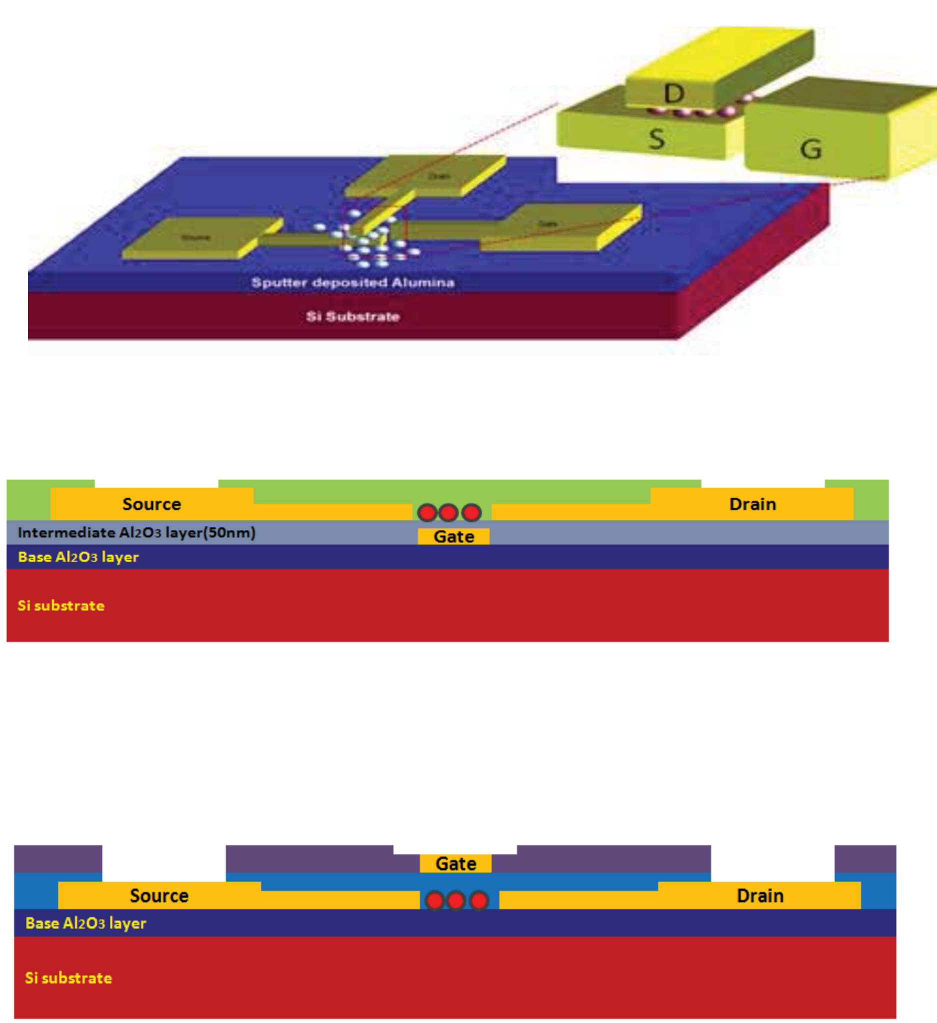
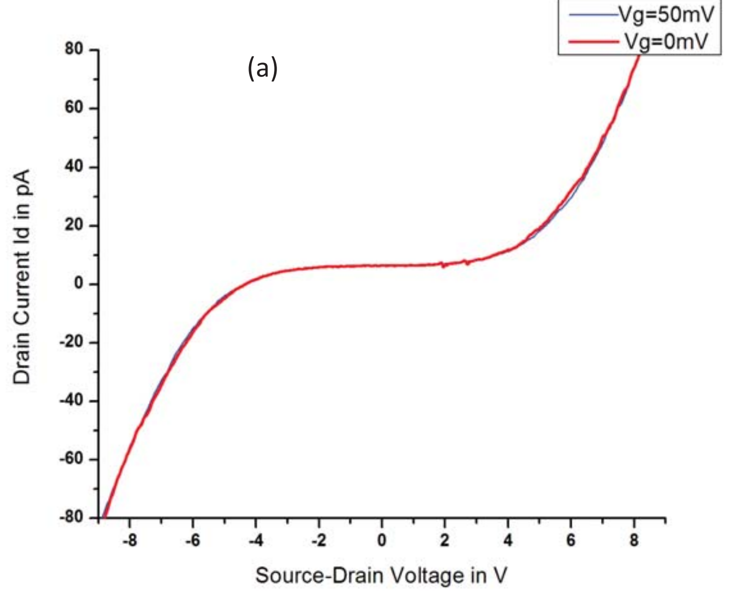


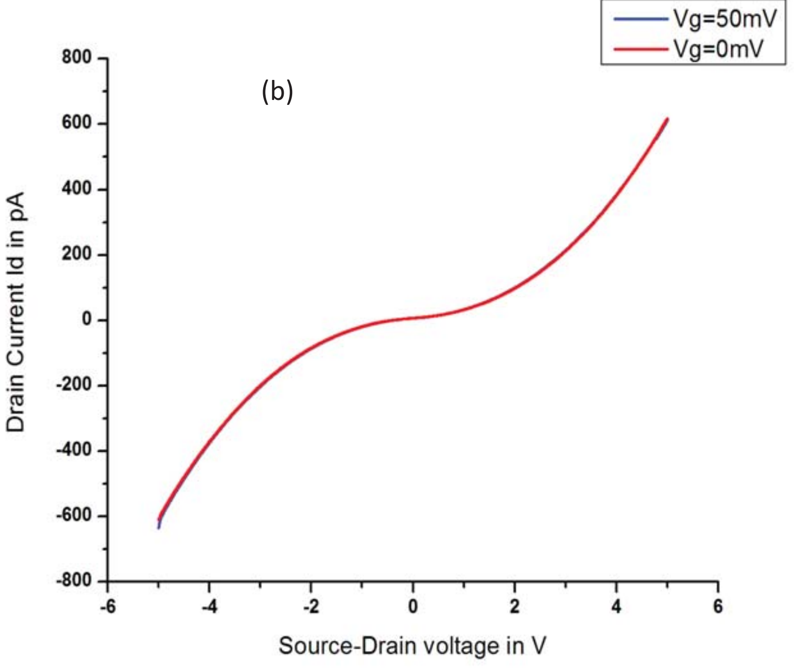
Fig. 5.6: Pictorial view of SET devices with different topology (top) Vertical Source and drain, (middle) Bottom Gate device (bottom) Top gate device.

Table 5.1 Dimensional Parameters of SET with Different Topology

Device Type	Vertical Source-Drain	Top gate	Bottom Gate
Width of Source and drain terminal	~300nm	~100nm	~300nm
Width of gate terminal	~300nm	~300nm	~300nm
Source-drain gap	depends on the dot size and oxidation time	~25nm	~250nm
Gate gap	~1um	50nm	50nm

The Coulomb blockade characteristics of such devices are shown in Fig. 5.7. Clear Coulomb blockade is observed in all the devices at room temperature. However, it can be observed that the length of the Coulomb blockade is different for each configuration. The device parameters can be extracted from the V-I characteristic as explained in Section 5.1. The charging energy and the total effective capacitance of the devices are graphed in Fig. 5.8.


Vg=50mV
Vg=0mV
(a)
Drain Current Id in pA
80
60
40
20
0
-20
-40
-60
-80
-8
-6
-4
-2
0
2
4
6
8
Source-Drain Voltage in V


Vg=50mV
Vg=0mV
(b)
Drain Current Id in pA
800
600
400
200
0
-200
-400
-600
-800
-6
-4
-2
0
2
4
6
Source-Drain voltage in V

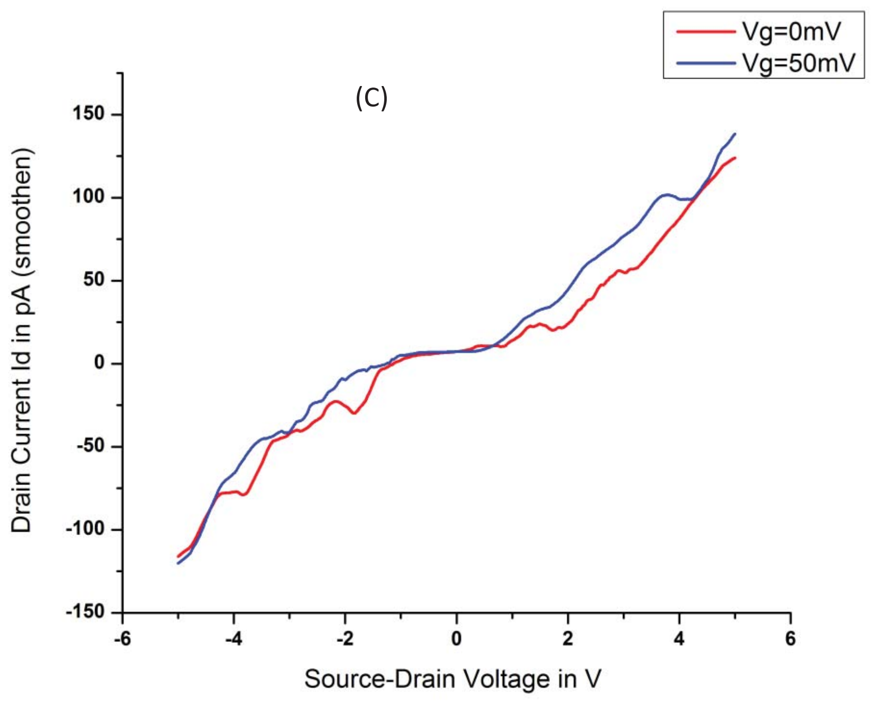


Fig. 5.7: Coulomb blockade characteristic of the SET devices of different topology (a) Bottom gate (b) Top gate (c) Vertical Source and Drain.

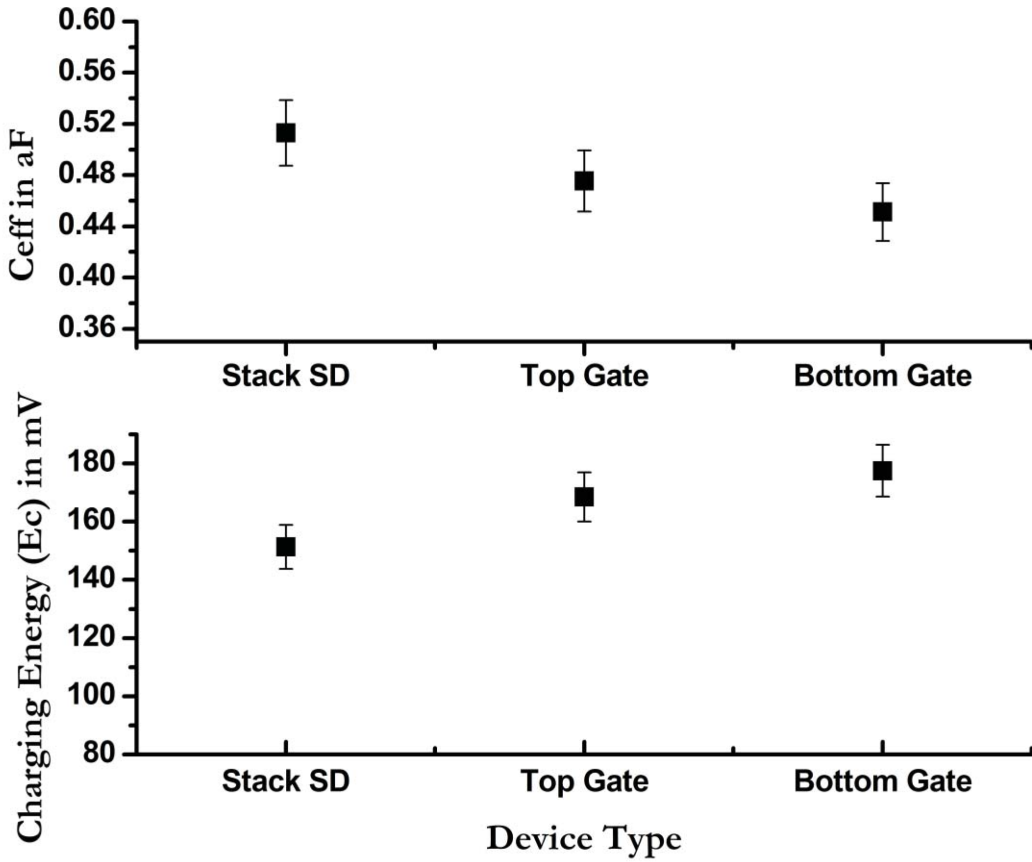


Fig. 5.8: Plots showing the charging energy and the effective capacitance for SET with different topology as extracted from the experimental V-I characteristic.

From Fig. 5.8, it can be observed that the device with vertical source and drain terminal has higher effective capacitance and lower charging energy than the other configurations. This attributes to the lower Coulomb blockade length than the other two devices. In case of a vertical source-drain device the dominant conducting path is expected to have only one participating dots. Hence, the electron transport is expected to take place only through two tunnel junctions. Therefore, single dot based device behavior is expected from this device.

The top gate and bottom gate devices have planar source and drain terminal hence more than one dots forms the dominant conducting path for the current transport. This results in lower effective capacitance due to higher number of series capacitance in the DCP than that for a vertical source-drain device. The charging energy and the C_{eff} are expected to be the same for the top and bottom gate devices, as the thickness of the intermediate Al_2O_3 layer is kept constant for both devices. A small variation in these parameters as observed in Fig. 5.8 can be attributed to the variation in the source drain gap of the devices.

5.3.2. Comparison between Vertical S-D and Planar S-D Device

In a fabricated SET device with 17nm source drain gap it is expected that only 1 or 2 quantum dots take part in electron transport process. Likely in case of vertical source drain based device as the layer of the nano-islands are sandwiched between the sources and drain terminals only one dot is expected to be in the DCP. Hence, comparing the behavior of these devices can explore the key effect of device topology. Figure 5.9 shows the Coulomb blockade characteristic of these two devices.

From Fig. 5.9 it can be observed that the length of the Coulomb blockade for both the devices is almost equal. In a vertical source drain device with a single dot in the DCP, no additional series capacitances are associated in the overall capacitance of the device. Hence, the effective capacitance is expected to be higher than that of the 17nm S-D gap based planer device and the blockade voltage should be smaller. But as is shown in Table 5.1, the gate gap for the vertical source-drain device is much higher than that of a planar device. It is expected that the larger gate gaps in the case of the vertical source-drain device can decrease the gate capacitance by adding the series capacitances due to additional dots between the

gate terminal and the DCP. This results in a lower effective capacitance which makes the blockade length similar rather than larger than that of a 17nm S-D gap based device. A capacitive model showing the series capacitance for both the devices is shown in Fig. 5.10. The value of the extracted charging energy (mean value for 9 data of each device) and the effective capacitance from the V-I curve of the devices is given in Table 5.2.

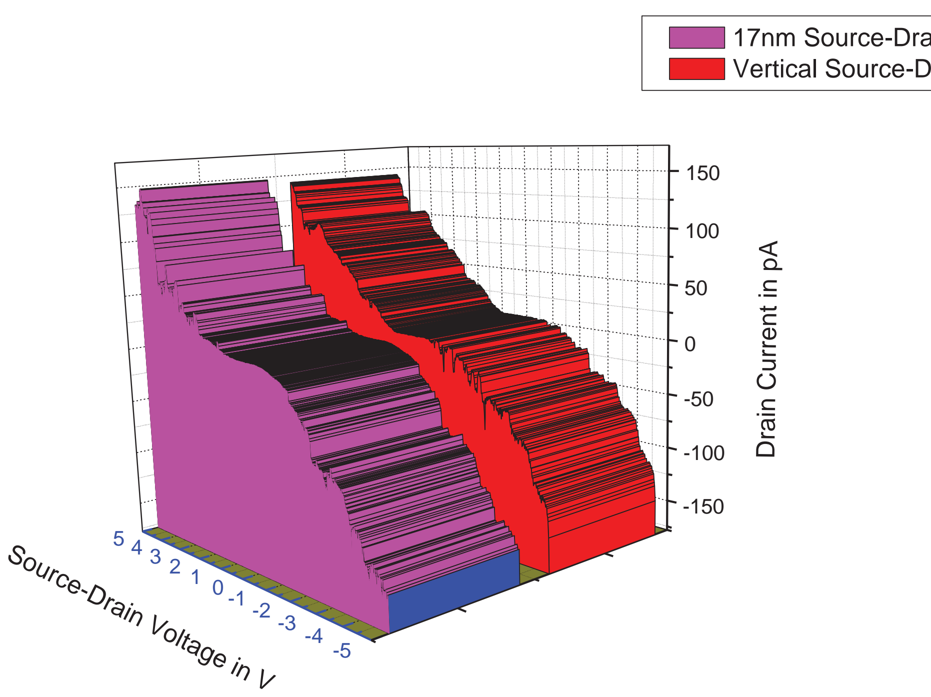


Fig. 5.9: Comparison of the Coulomb blockade characteristic of a 17nm source drain device and a vertical source-drain device.

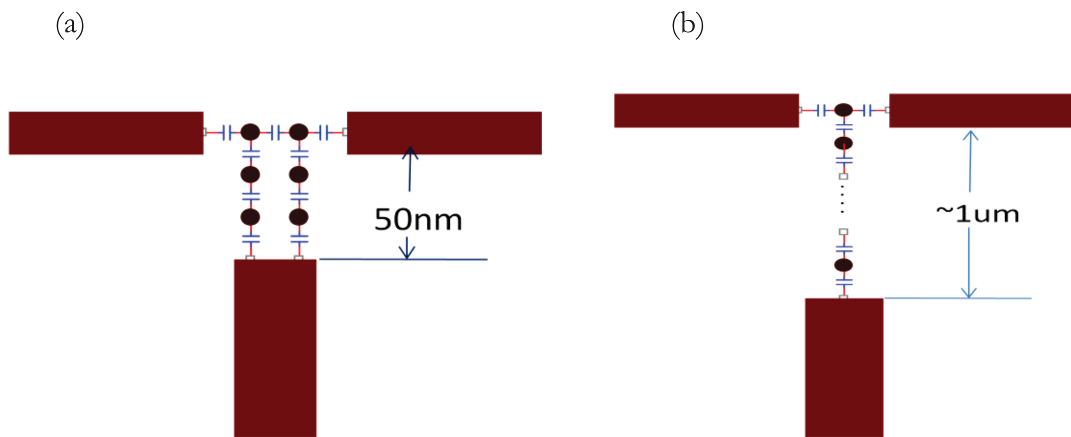


Fig. 5.10: Capacitive model of the SET devices (a) Device with 17nm S-D gap (b) Device with vertical S-D terminals [The electrodes for device (b) are in different planes which is not shown in this picture].

Table 5.2: Device parameters for vertical device and 17nm S-D gap based device

Device Type	Charging energy in mV	Ceff in aF
Vertical S-D SET	151.3	0.513
17nm S-D gap based SET	137.3	0.583

5.4: Impact of additional Non-participating dots

In a multi dot based SET device as explained in this work, the current conduction takes place by tunneling of the electron through an array of junctions in a single dominant conducting path (DCP). The current voltage characteristic and the performance parameters like threshold voltage (V_t) of the device depends on the capacitances associated with DCP. In this section, the impact of additional series capacitances due to the nonparticipating nano-

islands is reported. A novel method to improve the threshold voltage and to reduce the gate leakage current is also presented.

To study the impact of these non-participating dots in the planar device characteristics, two different sets of devices are fabricated. For one of these two sets of devices the additional dots are removed by FIB etching process. On the other hand, for the other SET device the additional dots are present. The removal of these dots is done using the MO-50 beam in the FIB system using the raster scan mode. From the V-I characteristic of our fabricated device in Fig. 5.11, it can be observed that the threshold voltage and hence the Coulomb blockade length for a device without any non-participating dots is smaller than that of a device with non-participating dots. In other words, the blockade length of the SET device decreases if the non-participating dots are removed from the active area. This fact could be explained by using capacitance analysis.

For a multi-dot based SET device, the total effective capacitance C_{eff} could consist of the intra dot capacitance in the DCP (dominant conducting path), capacitances associated due to the electrode terminals, and finally the additional capacitances associated due to non-participating dots. Figure 5.12 shows the pictorial view of the SET devices, with the capacitance associated due to various structures. It could be observed that, for a device with additional non-participating dots, the number of series capacitances associated with the DCP is higher than that for a device without any non-participating dots. These series capacitances decrease the total effective capacitance of the device and hence increase the threshold voltage. Therefore, by removing the non-participating dots, these series capacitance could be eliminated and hence the threshold voltage could be improved. This could be observed from

the capacitance model of the device as shown in Fig. 5.12. The decrease in the threshold voltage could be observed in Fig. 5.11.

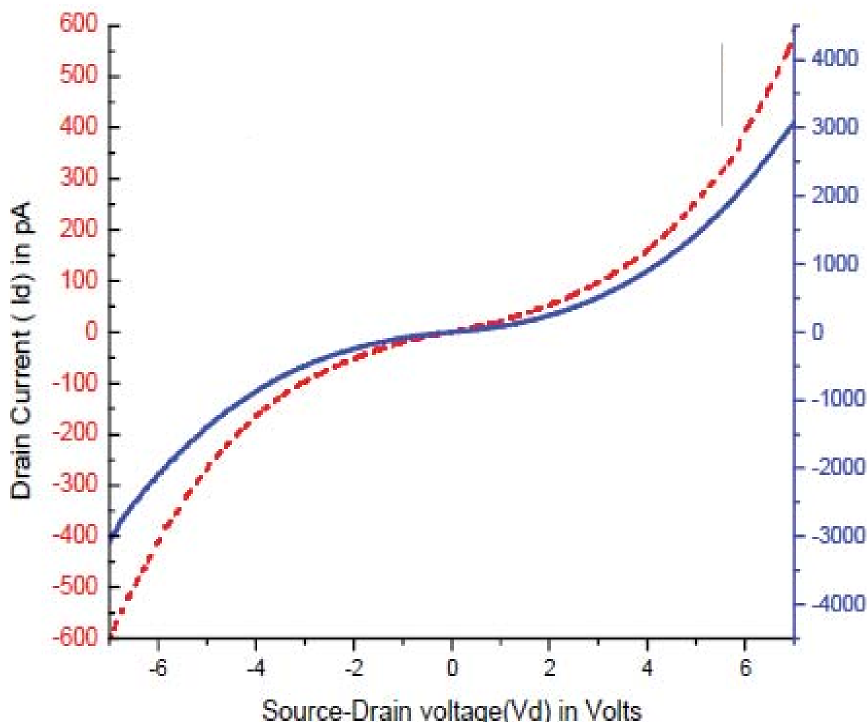


Fig. 5.11: Room temperature V-I characteristics of the SET devices with (blue line) and without (red dash) the non-participating dots.

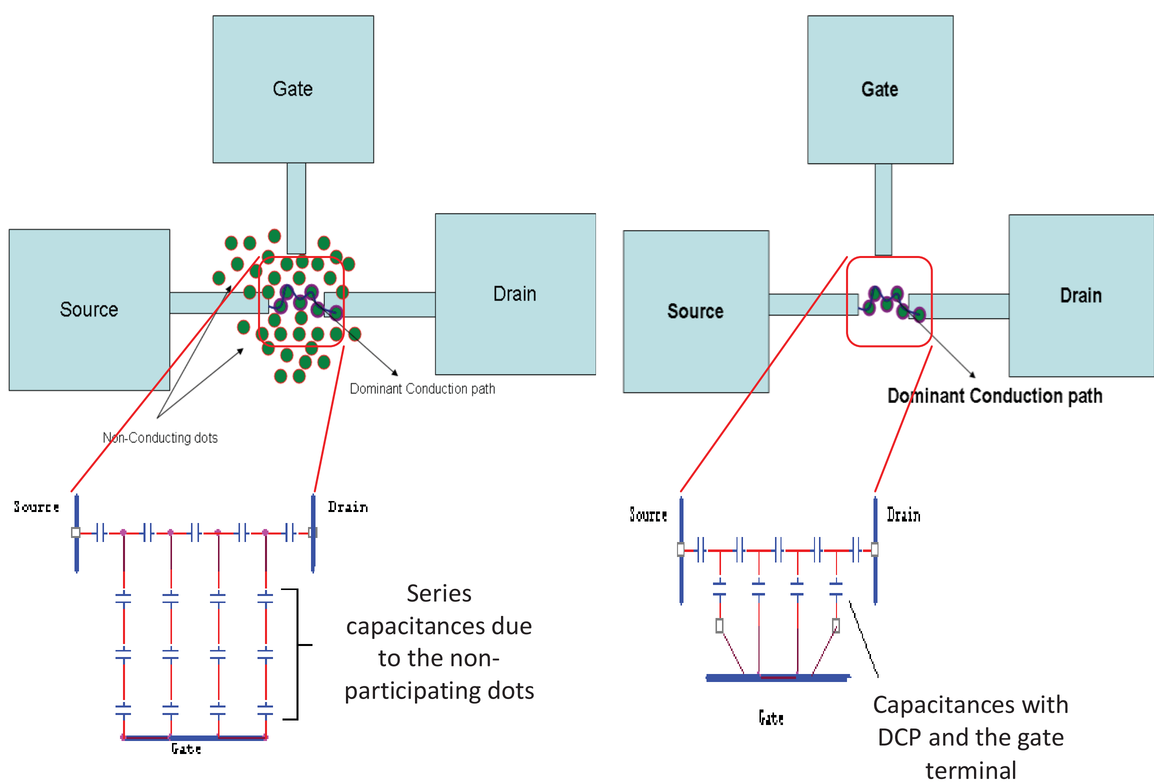
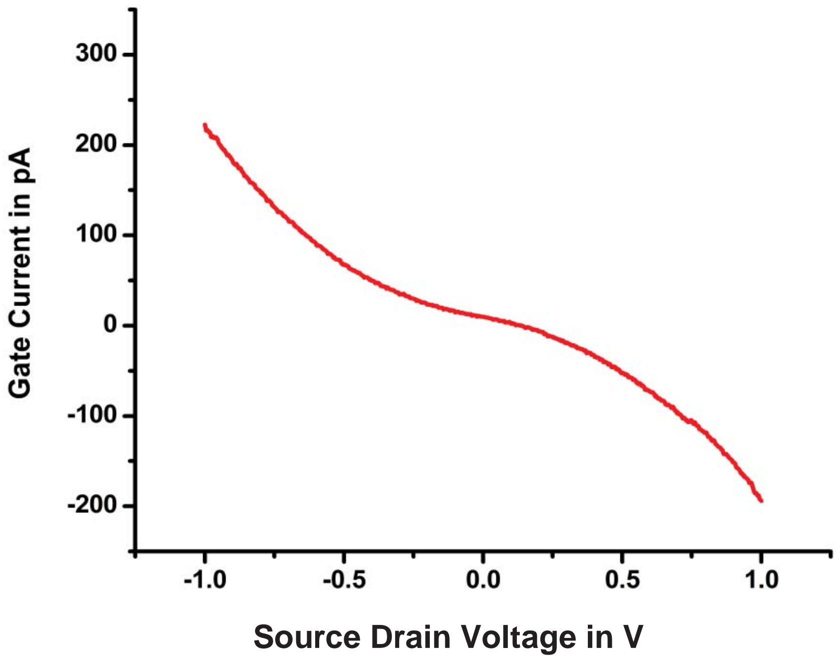


Fig. 5.12: Pictorial view of a SET device (left) with and (right) without additional non-participating dots. The inset represents an approximated capacitance model of such devices.

In addition to the threshold voltage improvement, removal of these non-participating dots from the active area also has impact on the gate leakage current. The gate leakage current with respect to the source drain voltage for the devices with non-participating dots are shown in Fig. 5.13 . From the blockade nature of the gate current characteristic as shown in Fig. 5.13(a), it could be expected that the gate leakage current is primarily from the unintended tunneling from the source terminal to the gate terminal through the non-participating dots. Therefore, removing these dots could minimize the gate leakage current. This is validated by measuring the gate current for a device in which the

non-participating dots are removed and plotted in Fig. 5.13b. Comparing these two characteristics, it can be observed that the gate leakage current is decreased by two orders of magnitude in a device without the additional non-participating dots. Removing the non-participating dots blocks the path for tunneling and hence decreases the leakage current. The removal of gate leakage current is important as it complicates the understanding of the V-I output characteristics of the device by adding an offset current. This can also have negative effect in the applicability of the device especially for sensing applications [69].



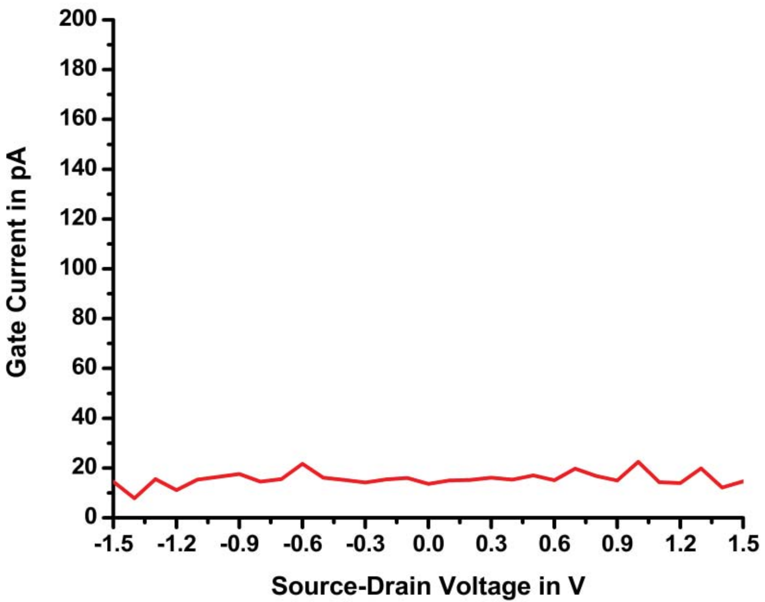


Fig. 5.13: Plot showing the gate current with respect to the source-drain voltage in a multi dot RT-SET (left) with and (right) without non-participating additional dots.

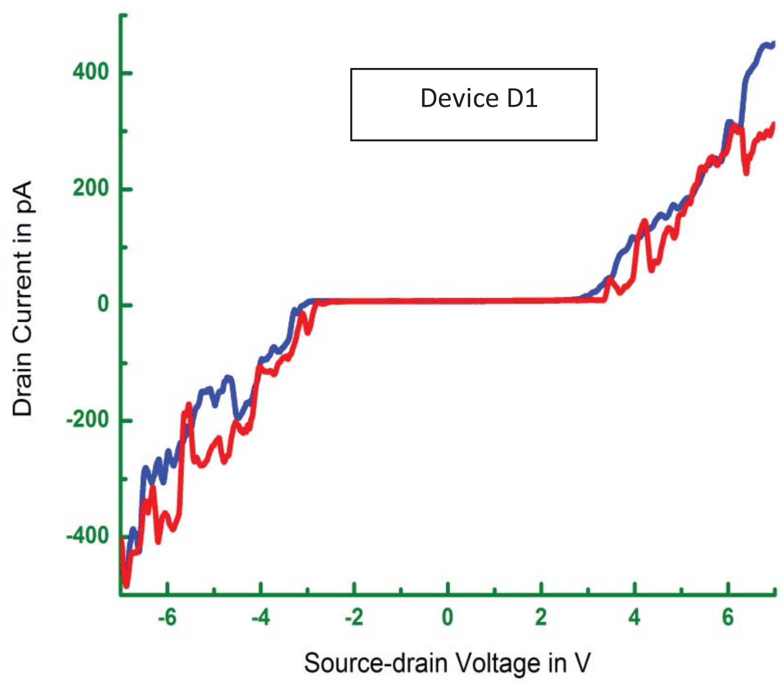
5.5: Impact of Material Properties

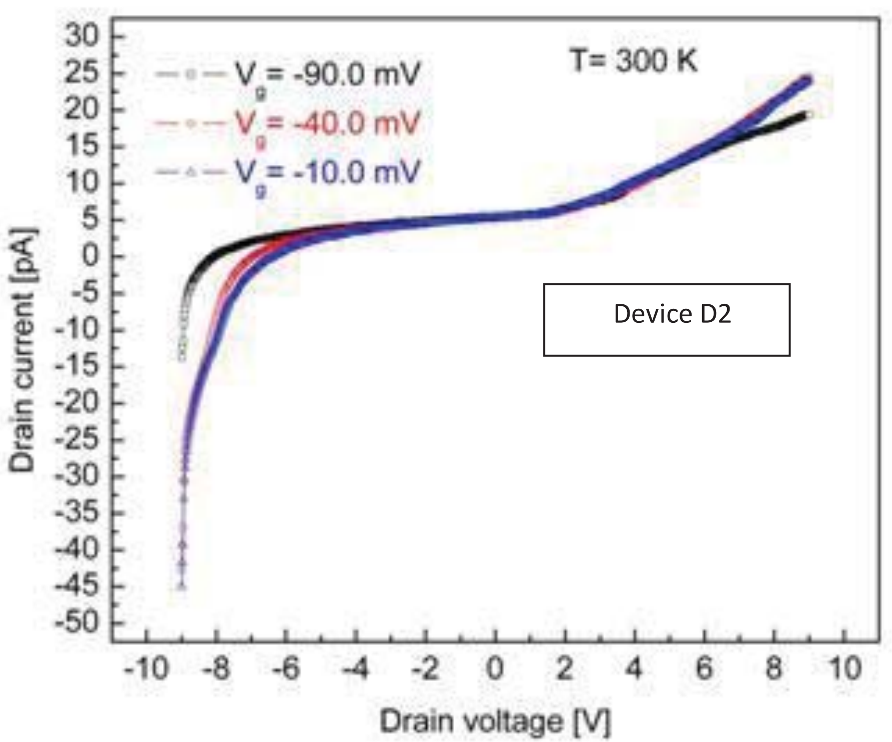
Apart from the impact of topology and device structure on the device characteristic, the behavior of the device can also depend on the materials. The electronic properties of material for the electrodes and the quantum dots has a direct impact on the electron tunneling from the source to drain terminal. To study this effect, SET devices with similar structural and topological configuration are characterized and compared. Three sets of devices are formed for the comparison study of different material set-ups. The description of the three devices are shown in Table 5.3.

Table 5.3: Description of the SET devices with different material set-ups

Device Name	Material used for Source, Drain and Gate terminal	Material used for the Quantum Dots	Tunnel Junction	Source drain gap	Device Structure
D1	Tungsten (W)	Tungsten	WO_2	250nm	Planar
D2	Chromium (Cr)	Tungsten	WO_2	250nm	Planar
D3	Tungsten (W)	Silicon	SiO_2	250nm	Planar

The device D1 represents a FIB deposition based as developed by Karre, et al. The D_2 is basically formed by FIB etch and deposition process with higher dwell time and/or line width at the nano-gap formation step to achieve a source-drain gap of 250nm. Device D3 represents one of the silicon dot based devices as discussed in the fabrication and result chapters. The room temperature V-I characteristic of such devices as obtained by the Keithley 4200 SPA system are shown in Fig. 5.14.


Device D1
Drain Current in pA
Source-drain Voltage in V
400
200
0
-200
-400
-6
-4
-2
0
2
4
6


T= 300 K
V g = -90.0 mV
V g = -40.0 mV
V g = -10.0 mV
Device D2
Drain current [pA]
Drain voltage [V]

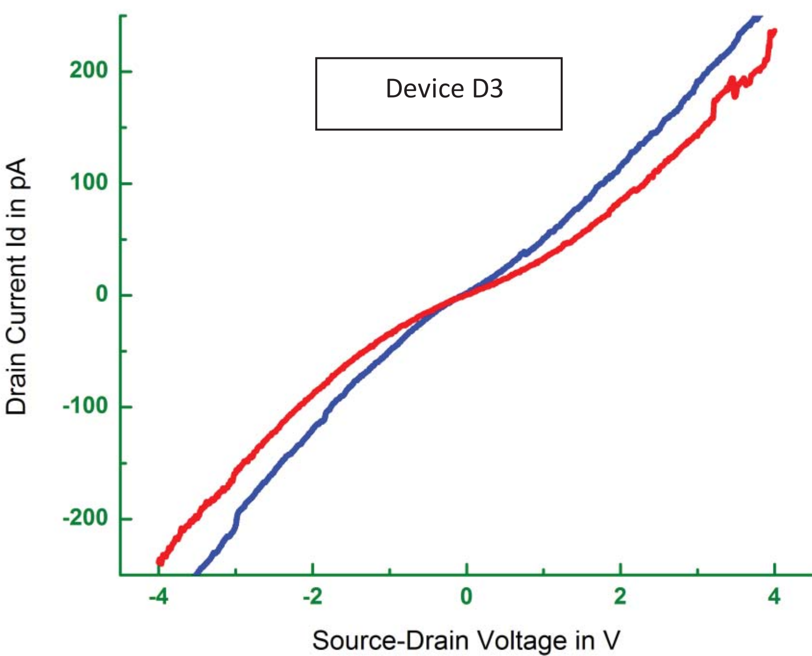


Fig. 5.14: The V-I characteristic of the devices with different material setups showing the Coulomb blockade for different gate voltages. The buttom plot is reprinted from Ref-69 with kind permission from the author].

Comparing the Coulomb blockade characteristic of the devices as shown in Fig. 5.14 it can be observed that the length of the Coulomb blockade is approximately same for devices D1 and D2. The blockade length in a device characteristic represents the effective charging energy of the device at room temperature. The charging energy directly depends on the effective capacitance of the device.

The device D1 and D2 have the same material for the quantum dots and the tunnel junction with similar junction width and source drain gap. Hence, the overall capacitance for the dominant conduction path for both the device is almost the same. This makes the charging energy of the two devices to be equal which results in equal blockade length and

threshold voltage. The Coulomb blockade length can also be represented by the difference between the chemical potential of the electrode material and that of the nano-island. In this case as the chemical potential of Cr is approximately equal to that of W, the devices D1 and D2 gives the equal blockade length.

Comparing the characteristic of device D3 with other two devices it can be observed that the blockade length is much smaller than that of the others for a equal gate voltage Vg=0mV. This could be attributed to the lower charging energy and higher effective capacitance of the device. The effective capacitance consists of the individual junction capacitance and the self capacitance of each dot. For device D3 the dots are made up of Si with a permittivity higher than that of tungsten. This makes the self capacitance of the dots and hence the effective capacitance of the devices higher than that of device D1 and D2. An increase in the effective capacitance decreases the blockade length and the threshold voltage.

Gate controllability is another aspect of these devices which is compared in this study. This is the measure of modulating the drain current by changing the gate voltage. From Fig. 5.14 it is clear that the gate controllability of the device is much better for Si nano-dot based devices than that of the devices with W nano-islands. This behavior can be attributed to the arrangement of the energy levels in the band structure of the nano-island.

The arrangement of the nano-islands in our device configuration can be treated as a random array of 3-dimentional quantum wells separated from each other by the tunnel barriers. The electron transport from the source terminal to the drain terminal occurs by tunneling through a dominant conducting path in this array. For metallic nano-islands, as in case of the device D1 and D2, the energy levels in the quantum well are continuous. Hence the current conduction through the single electron tunneling takes place only when the

energy supplied by the source-drain voltage is large enough to overcome the charging energy due to difference in the chemical potentials. The gate voltage can change the chemical potential in the dots to control the tunneling event. However, any background charges in the additional non-participating dots can nullify this controllability [39].

On the other hand, in case of a device with semiconductor quantum dots as in case of D3, the energy levels in the quantum well are expected to be discontinuous. Hence to make a possible tunneling event, the alignment of the energy levels in the DCP condition has to be satisfied in addition to the charging energy condition [98,99]. This requirement for energy level alignment hopefully reduces the impact of background charges and increases the gate controllability in a Si dot based device (D3) as shown in Fig. 5.14. This reasoning can also explain the improved periodicity in the Coulomb oscillation of a Si dot based device as discussed in Chapter-4.

5.6. Multiple Peaks and Non-periodicity in the Coulomb Oscillation

Coulomb oscillation in the drain current or in the conductance represents the charging and discharging events in the device controlled by the gate voltage. In case of a single dot double junction SET device, the oscillation peaks are periodic and uniform. In the current research, all the devices fabricated shows Coulomb oscillation at room temperature. However, from the drain current vs. gate voltage characteristic of such devices as discussed in Chapter-4, it can be observed that these oscillations are non-periodic in nature with the existence of multiple level of peaks.

In a multiple-dot based SET device the charging and discharging and hence the Coulomb oscillation events depend on inter-dot interactions. According to theoretical study [103], the peak and periodicity of the Coulomb oscillation depends on the parameters like inter-dot Columbic repulsion and multiple electron hopping. Prada, et al. [103] in his analysis shows that this effect can generate additional peaks in the Coulomb oscillation. The spacing between these additional peaks depends on the Coulomb repulsion parameter 'w' and the number of electrons in the occupied quantum dots in the DCP. The periodicity and the uniformity of these peaks can be impacted directly with the size and distance between the quantum dots in the DCP. In the present device as the quantum dots are random in size and position. Non-periodic multiple peaks are visible in the Coulomb oscillation characteristics.

Another effects that can impact the Coulomb oscillation behavior is the thermal noise and the background charges. These two effects can create a giant fluctuation in current [106] which can appear in the Coulomb oscillation in terms of multiple peaks.

The above effects generated multiple peaks and the non-periodicity in the Coulomb oscillation can be represented statistically. A previous work in this area suggests that the spacing between the peaks in oscillation at mK temperature is dispersed in a Gaussian profile, although a theoretical explanation for this fact is not yet known [107]. To verify this trend in the FIB fabricated devices, the spacing between the peaks in the Coulomb oscillation is noted for each device and their distribution is calculated. The distribution curve of these data for a etch-deposition based device is shown in Fig. 5.18.

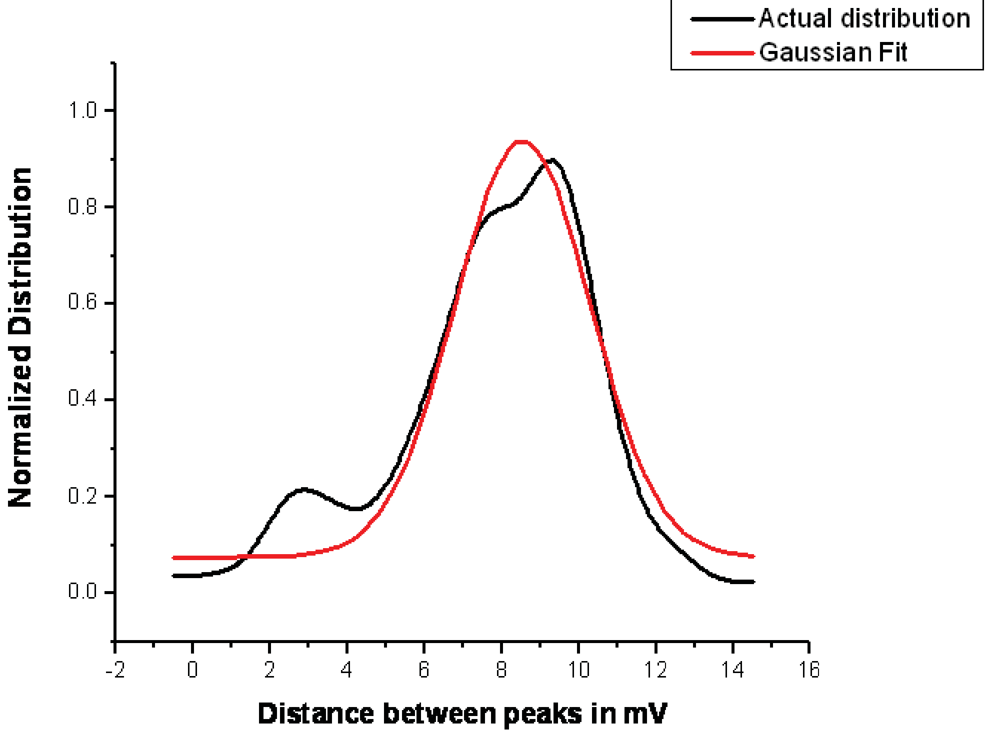


Fig. 5.15: The distribution of the spacing between the multiple peaks in the Coulomb oscillation of a 17nm based SET device.

5.7. Model Verification

The non-linear Coulomb blockade characteristics of the SET devices with different configurations can be explained using the models as discussed in Chapter-2. Depending on the topology of the device, two different theoretical modeling approaches are made to explain the behavior.

Vertical Device

In case of a vertical source-drain device, it is expected that only a single dot is taking part in the dominant conducting path. The behavior of the device can be approximated to that of a single dot based device. Hence a single dot based master-equation. approach is performed to model the behavior of these devices. The impact of the additional parallel dots is included by iterating the program for all the possible DCP. The randomness in the size and position of the dots is attributed by setting a parameter which can assign random values to the junction capacitance and tunnel resistance. The order of the capacitance and resistance value is decided from the theoretically calculated data as explained in Chapter-2.The mean value of these parameters (best fitted value) are input through a data structure as given in Table 5.3. The capacitance and resistance of the two junctions are calculated uniquely to represent variation in the junction width for source and drain. The Matlab code for the model is included in the appendix section.

With the data used in simulations, it was observed that the shape of the device characteristics along with the Coulomb blockade length of the device was captured by the present model. Figure 5.16 shows the simulated V-I plot for the vertical device with and without considering the parallel paths.

Table 5.4: Device parameters for simulating the V-I characteristic of a vertical device

Device Parameters	mean values
1st junction capacitance (C_1)	$1 \times 10^{-19} F$
2nd junction capacitance (C_2)	$1 \times 10^{-19} F$
1st junction Resistance (R_1)	$5 \times 10^{10} \Omega$
2nd junction Resistance (R_2)	$5 \times 10^{10} \Omega$
Gate Capacitance (C_g)	$1 \times 10^{-20} F$

The mean value for gate capacitance is taken one order of magnitude lower than that of the junction capacitance to properly consider additional series capacitances associated with the non participating dots present between the gate terminal and source-drain gap.

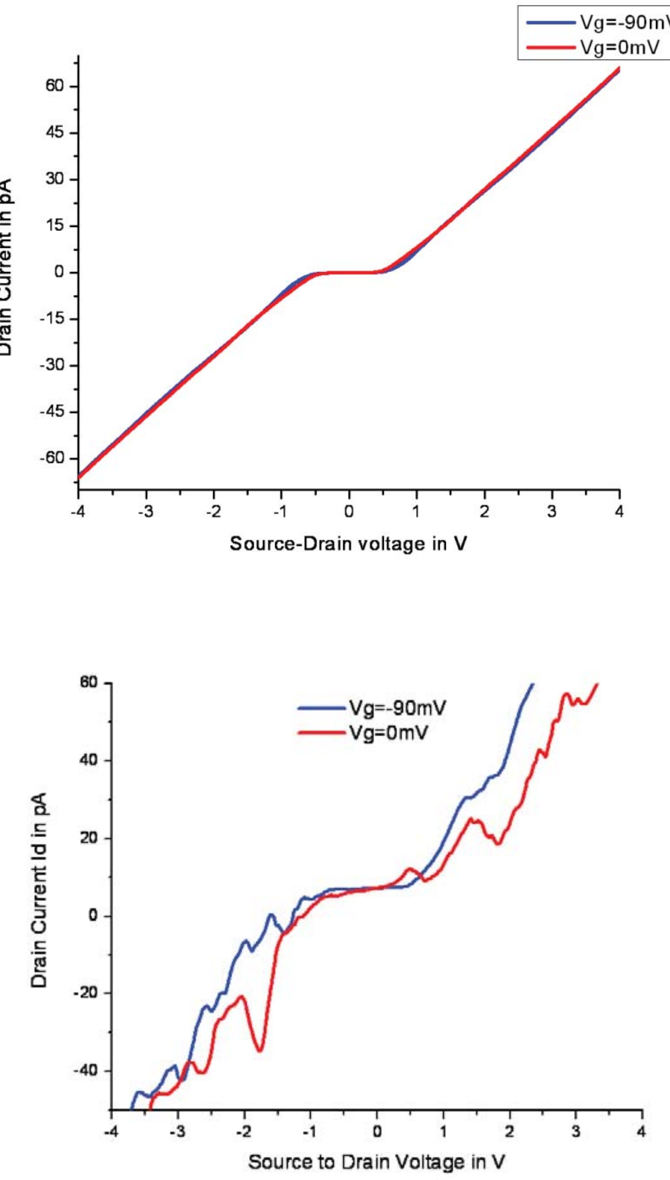


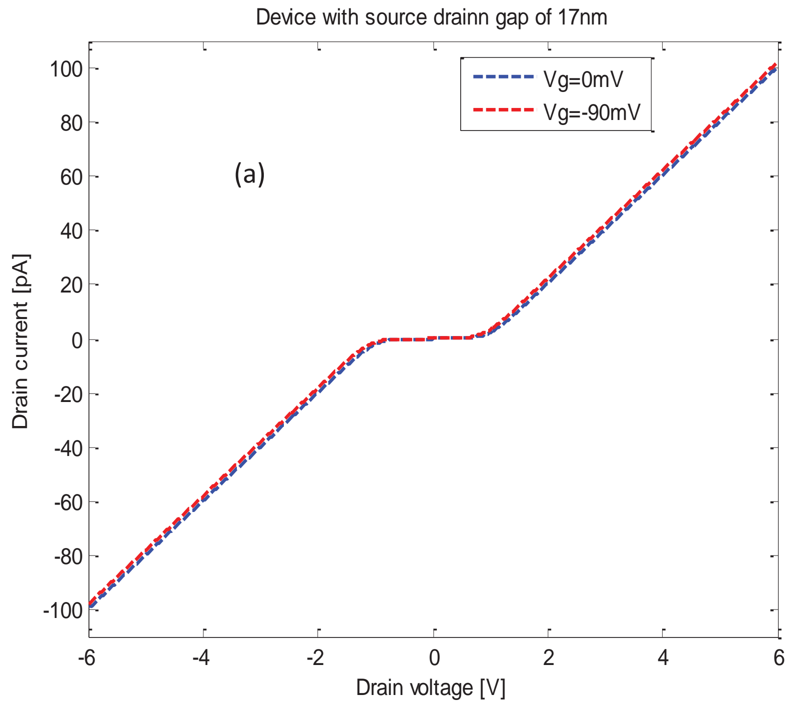
Fig. 5.16: Theoretical (top) and experimental (bottom) non-linear characteristic of a SET device with vertical source and drain terminal.

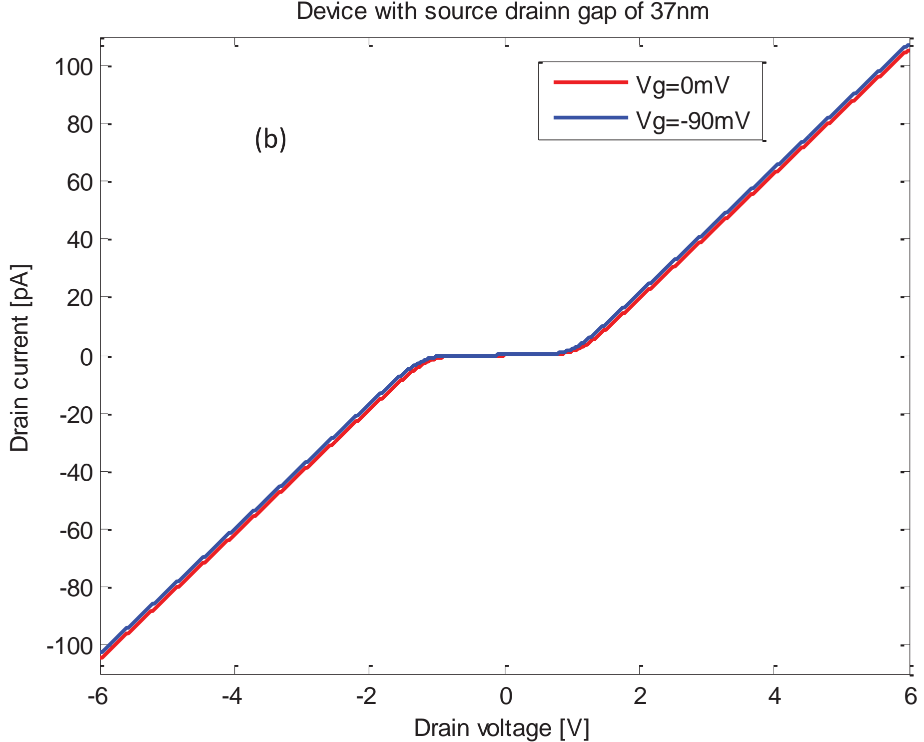
Comparing the experimental and simulated non-linear V-I characteristic for the vertical device it can be observed that the order of the obtained drain current is in agreement with the experimental data. The length of the Coulomb blockade in the simulated V-I

characteristic is slightly smaller than that of the experimental data. The possible reason for this fact can be lower charging energy in the model data as the model does not include the inter dot capacitance which can increase the charging energy in case of the real device. The current fluctuation in the experimental data which could be due to multiple tunneling paths in a real device is not captured in the simulated plot. This could be a result of averaging the currents for multiple DCP in the vertical device.

Planar Devices

Unlike the vertical device, the dominant conducting path in a planar device consists of more than one nano-island participating in the current conduction process. The master equation model cannot be used to model the V-I characteristic of this device as there are more than two junctions in the DCP. The non-linear Coulomb blockade characteristics of the multi dot SET device can be explained using the Soliton model as explained in Chapter 2. The source drain non linear characteristics for different device structures have been simulated. The device parameters used in the simulation are obtained from the experiment, which are extracted using the device parameter extraction, as explained in Section 5.1.


Device with source drainn gap of 17nm
Vg=0mV
Vg=-90mV
(a)
Drain current [pA]
Drain voltage [V]
100
80
60
40
20
0
-20
-40
-60
-80
-100
-6
-4
-2
0
2
4
6


Device with source drainn gap of 37nm
Vg=0mV
Vg=-90mV
(b)
Drain current [pA]
Drain voltage [V]
100
80
60
40
20
0
-20
-40
-60
-80
-100
-6
-4
-2
0
2
4
6

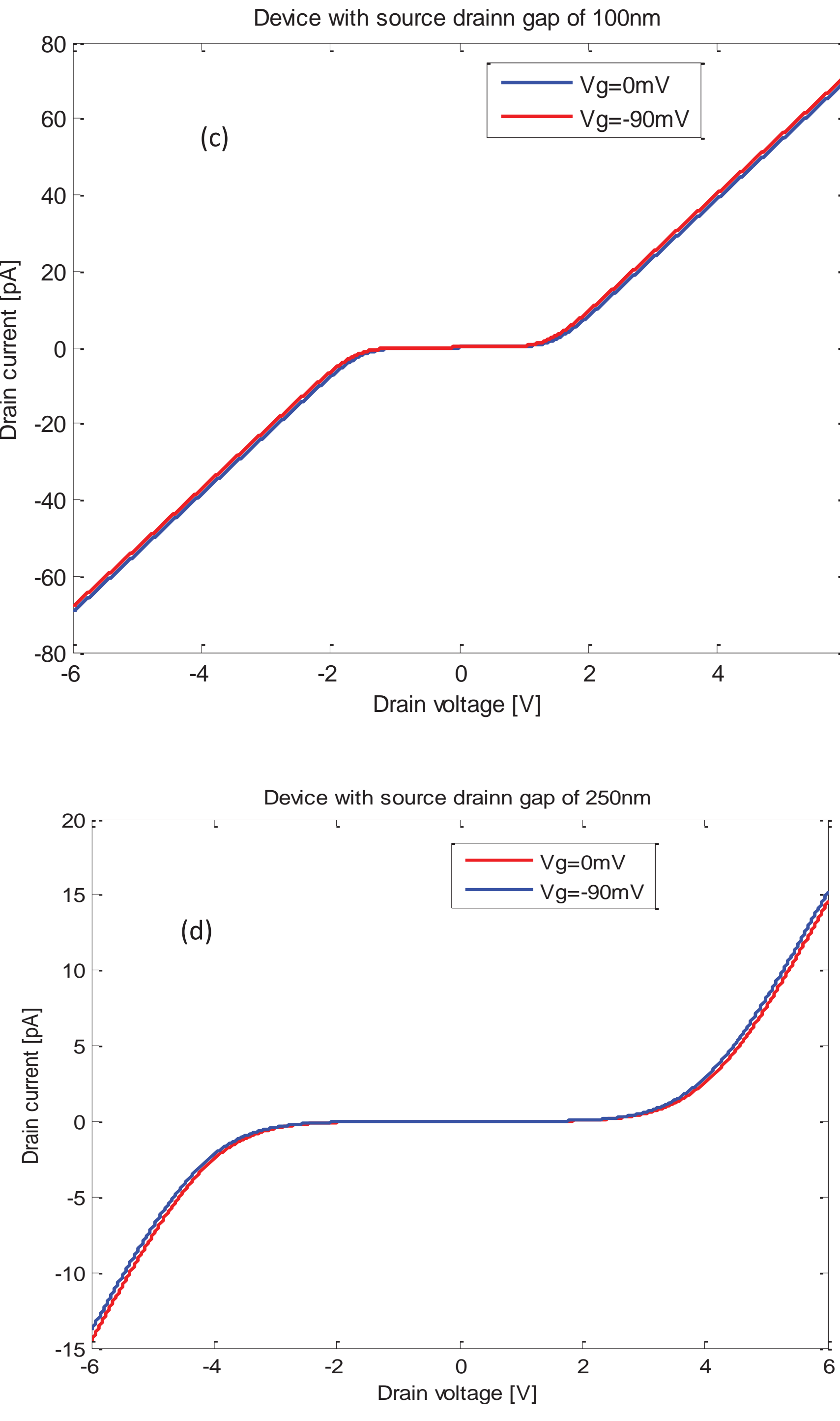


Fig. 5.17: Simulated V-I charcetristic of planar devices fabricated by FIB etch and deposition process with different source and drain gaps (a)17nm, (b) 37nm, (c) 100nm (d) 250nm

Comparing the experimental data with the modeling result it can be observed that the current in the simulated non-linear V-I characteristic of the planar device is in the same order with the experimental data. Also the length of the Coulomb blockade in the simulated V-I plots is in agreement with the experimental results. Figure 5.18 shows a comparison of these two parameters for modeling and the experimental curve.

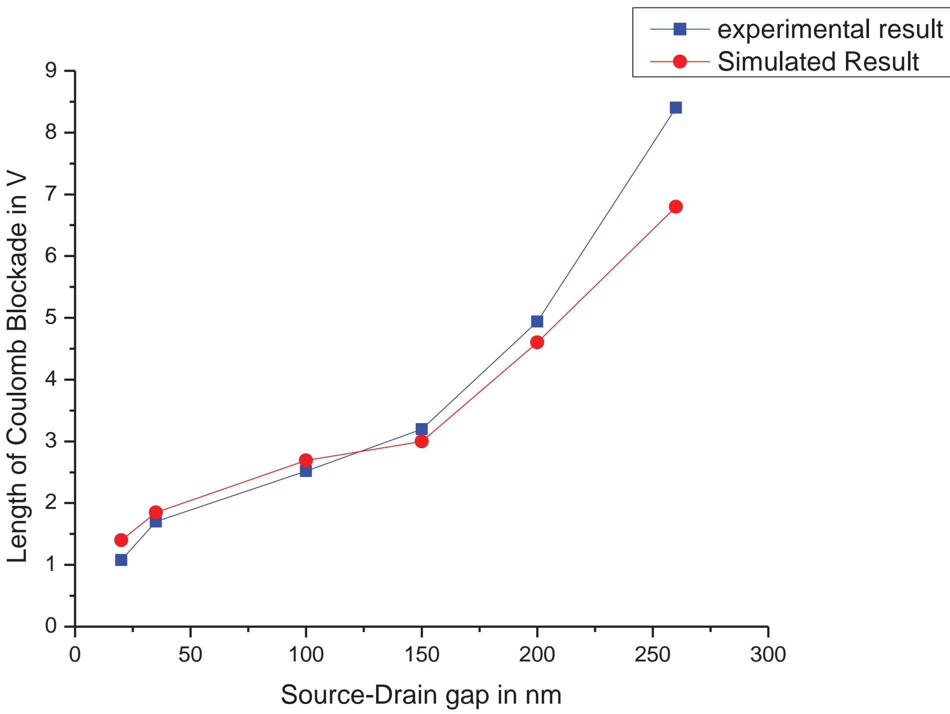


Fig. 5.18: Coulomb blockade length with respect to source-drain gap. Comparison between simulated results with the experimental data.

The Soliton theory model assumes the junction capacitance and the tunnel resistance is uniform, which is not true for the real devices. Again, this model is valid only for devices with one dimensional arrays of nano-islands. The two dimensional random distribution of

the tungsten nano-islands in case of the real device is not considered in the model. Hence, this model gives least understanding about the non-ohmic and fluctuating behavior of the drain current in the non-blockade region of the Coulomb blockade characteristic. This model also simulates the drain current characteristic and is not capable of capturing the Coulomb oscillation. Hence, an improved and more realistic model is required to fully understand the behaviors of these multi dot based devices.

Chapter 6: Conclusion

This dissertation work has led to significant progress in understanding the behavior of room temperature operating single electron transistor devices and the impact of structural and topological parameters on it. It also helped to achieved some of the milestones to optimize the fabrication process of these device for enhanced functionality. The research also explored some of the limitations of the FIB etching process and developed optimized process parameters to overcome these limitations. The major contribution of this work is summarized below.

- ✓ The capability of FIB etching and deposition process along with their limitation in the nano scale regime is more clearly understood.
- ✓ The dissipation of ion energy during ion solid interaction for a FIB etching processing is studied and its impact on the resolution of the FIB etching process is predicted.
- ✓ The impact of Gaussian beam profile on the FIB fabricated nano structure is investigated experimentally.
- ✓ An optimized process flow is developed to overcome the resolution limits in the FIB etching process. This is performed by optimizing the thickness of the active

layer. In this particular work, the nano-structure of minimum line width at a 17nm has been fabricated on a Cr layer with an optimized thickness of 20nm.

- ✓ Previously developed FIB deposition processing is used to fabricate sub-10nm sized nano island using higher dwell time for deposition. An heat conduction analysis based model is developed to predict the deposition yield with respect to the dwell time and to validate the experimental data.
- ✓ Single electron transistor devices are fabricated using these nano islands and nano structures fabricated by FIB technology. These devices are characterized by SPA system and all of them show Coulomb blockade effect at room temperature.
- ✓ Devices with different structure and topology are fabricated to investigate the impact of structural and topological variation on the device behavior. It was observed that the threshold voltage of the device can be modulated by varying the source drain gap in the device. A minimum threshold voltage of ~500mV is achieved for a device with 17nm source-drain gap.
- ✓ Realization of single dot based SET device is demonstrated by the vertical source drain based device. Clear Coulomb stair case conduction is observed in such a device and this also explores the possibility of 3-D fabrication of the devices for future nano-electronics.
- ✓ The experimental characteristic of the devices are validated by theoretical modeling. A master equation based model is developed to validate the characteristic of the vertical device and a Soliton based model is developed to validate the planar devices.

- ✓ SET with Si quantum dots are fabricated using a unique technique by FIB deposited discontinuous W thin film. Clear Coulomb blockade behavior with better gate controllability is demonstrated in such devices.
- ✓ The impact of additional non-participating dots on the device behavior is investigated. It was observed the gate leakage current can be reduced by removing the additional non-participating dots surrounding the dominant conducting path for the device.

Chapter 7: Future Work

The present work explored the behavior of the device at room temperature and developed Focused Ion Beam based technology to enhance the functionality of these devices. However, further investigation is required to understand the current fluctuation in the non-blockade region of the device. Low temperature characterization of these devices can be a good approach in that effort. Technology needs to be developed to minimize the non-periodicity in the Coulomb oscillation. Continuing efforts are needed for the realization of single dot SET systems.

The current model for the planar device assumes the system to be a 1-D array of quantum dots. An improved and more realistic model needs to be developed to predict the behavior of such multi dot based SET devices. The inter-islands capacitance needs to be considered while predicting the V-I characteristic of the device. A model using Monte Carlo simulation can be approached to consider the randomness in the size and position of the island. In order to fully understand the device behavior, a quantum mechanical model exploring the tunneling events between the islands and their neighbors, and the inter-island interaction effects needs to be investigated. For the vertical device, a modified model considering the impact of non-participating parallel dots needs to be developed.

Along with the development of the fabrication technology and the theoretical understanding of the device, possible application of these devices needs to be explored. Effort is needed to integrate these SET devices with existing CMOS devices for logic application. Other applications like displacement sensing and thermometry using these devices can be investigated. Mass fabrication of these devices is another future aspect which should be explored.

Chapter 8: Appendix

8.1. Fabrication Process Parameters

Table 8.1: Parameters for nano-islands oxidation process

Device Type	Oxidation Process	Oxidation Time	Apprx. Oxide Thickness
Etch deposition based Planar SETs	Chemical Oxidation by Peracetic Acid	2mins	1-2nm
Vertical S-D Based Device	Chemical Oxidation by Peracetic Acid	3mins	2-3nm
Top/Bottom Gate devices	Chemical Oxidation by Peracetic Acid	2mins	1-2nm
Silicon Dot based SETs	Native oxidation by atmospheric exposure	-	1-2nm

Table 8.2: Fabrication parameters for source drain gap formation of different widths

Intended Gap Width	20nm	35nm	100nm	150nm	250nm
Beam Type	MO20	MO20	MO20	MO20	MO20
Scanning Mode	Vector scan	Vector scan	Vector scan	Vector scan	Vector scan
Dwell Time	30 μs	30 μs	30 μs	30 μs	30 μs
Number of runs	1 to 2	3	5	5	8
Frame Number	70	70	100	100	100
Fabrication Area (Zoom)	2x2 μm (Zoom=4x2)	2x2 μm (Zoom=4x2)	2x2 μm (Zoom=4x2)	2x2 μm (Zoom=4x2)	2x2 μm (Zoom=4x2)
Pattern Line Width	1pixel	2pixel	5pixel	8pixel	20pixel

Table 8.3: Fabrication Parameters for Deposition the Passivation Layer for the Device

Deposited Material	Alumina (Al_2O_3)
Process Tool Used	Perkin-Elmore 8” 2400J
RF Power	1000 W
Reflected Power	<100 W
DC Bias	-465 V
Substrate Bias	0 V
Process Pressure	14.2 m Torr
Gas Flow	Ar: 20 SCCM O_2: 4 SCCM
Process Temperature	300^0 K
Deposition Time	10mins

Table 8.4: FIB Etching Parameters for Exposing the Probing Pads

Beam Used	MI300
Beam Current	4.8nA
Dwell Time (in µs)	100
Fab Time	10mins
Pattern Dimension	80X80µm
Interlace	2

Table 8.5 FIB Deposition Parameters For Fabricating Different Nano/Micro Structure

FIB Parameters	Structure 1	Structure 2	Structure 3	Structure 4	Structure 5	Structure 6
For use in Device/Experiment	Vertical SET/Si dot based SET	Vertical SET	Vertical SET	FIB Characterization Experiment	All SETs	All SETs
Fabricated Structures	Source Electrode	Drain electrode	Gate Electrode	Nano-Strip	Probing Pad	Nano-isalnds
Beam Used	Beam 01	Beam 01	Beam 01	Beam 01	Beam 01	MI200
Beam Current	0.112nA	0.112nA	0.112nA	0.117nA	0.112nA	2.231nA
Dwell Time (in µs)	0.5	0.5	0.5	0.5	0.5	9
Fab Time	3.5mins	2mins	5mins	3mins	18mins	6-12sec
Pattern Dimension	0.25µm x 50 µm	0.25µm x 50 µm	0.25µm x 50 µm	0.25µm x 40 µm	80µm x 40 µm	16µm x 16 µm
Interlace	2	2	2	2	2	8

8.2 Code for Simulation

8.2.1. Matlab Code for Device Modeling

Default

```
   SETisland = struct( 'R1', 25E9, 'R2', 25E9, 'C1', 1.0E-19, 'C2',
1.0E-19, 'Cg', 1.0E-20 );
   SETparameters = struct( 'Vg', 0, 'VMax', 1, 'VSamp', 100, 'NMax', 5,
'NWarningTol', 1.0E-05, 'BlockadeThreshold', 0.07, 'T', 300 );
   VERTisland = struct( 'R10', 25E9, 'R20', 25E9, 'C10', 1.0E-19,
'C20', 1.0E-19, 'Cg0', 1.0E-20, 'NIslands', 10, 'CRandExp', 0.5,
'RRandExp', 0.1, 'RComp', true );
```

```
VERTparameters = struct( 'Vg', 0, 'VMax', 1, 'VSamp', 100, 'NMax',
5, 'NWarningTol', 1.0E-05, 'BlockadeThreshold', 0.07, 'T', 300 );
```

Vertical Device

```
function [I V blockade] = VERT(island, parameters)
% vert.m
% Matlab program to calculate the IVC of a "vertical SET" modeled as
many
% non-interacting single island SET devices in parallel.
%
% Adapted from David Berman's single island SET code
% http://electron.mit.edu/theses/David_Berman.pdf
%
% Inputs:
%    island: Struct defining the capacitances and resistances of the
island
%       .R10: First junction mean resistance
%       .R20: Second junction mean resistance
%       .C10: First junction mean capacitance
%       .C20: Second junction mean capacitance
%       .Cg0: Gate mean capacitance
%       .CRandExp: Orders of magnitude by which the capacitance
varies
%       .RRandExp: Orders of magnitude by which the resistance
varies
%       .RComp: Wether to compensate so the total resistance of the
device is
%               not reduced when increasing the number of islands.
%               R = R0*NIslands so the effective resistance of the
device is
%               Reff =  R/NIslands =  (R0*NIslands)/NIslands = R0
%
%    parameters: Struct defining the parameters
%       .Vg:                Gate voltage
%       .VMax:              Maximum source-drain voltage (Vsd)
%       .VSamp:             Number of samples of Vsd
%       .NMax:              Maximum number of excess electrons to
consider
%       .T:                 Temperature
%       .NWarningTol:       Warn if rho is non-negligable for rho(+-
NMax)
%       .BlockadeThreshold: Current threshold to define the edges of
the
%                           Coulomb blockade (very rough measure)
%
% Output:
%    I:        Current array
%    V:        Voltage array
%    blockade: Approximate blockade length
%
```

```
   % % This Matlab program calculates the current through an SET as a
function
   % % of source-drain voltage, V, for a given gate voltage, Vg. The
gate
   % % Voltage, Vg, is defined in the Matlab environment before calling
the
   % % program. The first few lines of the program define the operating
   % % temperature (in K), and both capacitances and resistances of the
SET.
   % % These parameters can be changed by simply editing the file and
saving it.
   % % The capacitances are defined in Farads, and resistances in ohms.
This
   % % program outputs a plot which is generated by the command
'plot(V,I)'.
   % % Both V and I are vectors. The current is calculated from the
tunneling
   % % rate equations.



   % Distribute the capacitances exponentially about C0
   RandomArr=rand(5,island.NIslands);
   C1 = (10^island.CRandExp).^RandomArr(1,:)/(10^(island.CRandExp/2));
   C2 = (10^island.CRandExp).^RandomArr(2,:)/(10^(island.CRandExp/2));
   Cg = (10^island.CRandExp).^RandomArr(3,:)/(10^(island.CRandExp/2));
   R1 = (10^island.RRandExp).^RandomArr(4,:)/(10^(island.RRandExp/2));
   R2 = (10^island.RRandExp).^RandomArr(5,:)/(10^(island.RRandExp/2));
   C1 = C1*island.C10;
   C2 = C2*island.C20;
   Cg = Cg*island.Cg0;
   R1 = R1*island.R10;
   R2 = R2*island.R20;

   % Compensate so changing NIslands doesn't change the effective
resistance
   % of the device
   if island.RComp
      R1 = R1*island.NIslands;
      R2 = R2*island.NIslands;
   end

   I = 0;
   B = zeros(1,island.NIslands);
   for i=1:island.NIslands
      singleIsland.R1 = R1(i);
      singleIsland.R2 = R2(i);
      singleIsland.C1 = C1(i);
      singleIsland.C2 = C2(i);
      singleIsland.Cg = Cg(i);
      [I1 V] = SETIV(singleIsland, parameters);
      I = I + I1;
   end
```

```
% Define the blockade as the lenght of the region for which the
conductance
% is less than parameters.BlockadeThreshold times the conductance at
% parameters.VMax
g               = I(length(I))./V(length(V));
blockadeIndices = find( I./V < parameters.BlockadeThreshold * g );
blockade        = V( max(blockadeIndices) ) - V(
min(blockadeIndices) );
```

Planar Device

```
% multidotblockadesolitonPreislandDT3.m
% This Matlab program calculates the current through an SET as a
function of
% source- drain voltage, V, for a given gate voltage, Vg. The gate
Voltage,
%Vg, is defined in the Matlab
% environment before calling the program. The first few lines of the
program
% define the operating temperature (in K), and both capacitances and
resistances of
% the SET. These parameters can be changed by simply editing the
file and saving
% it. The capacitances are defined in Farads, and resistances in
ohms. This
% program outputs a plot which is generated by the command
'plot(V,I)'. Both
% V and I are vectors. The current is calculated from the tunneling
rate equations.
%The original single dot SET program is modified for the multi dot
SET.

       %                                                !
% This is for multi dot SET with device configuration DT3: - -


k=1.380662e-23; % Boltzmann's constant

T=300.0; % Temperature in Kelvin
e=1.602e-19; % Charge of an electron in Coulombs
C1=input('\n C1= \n');%C1=1.2478e-18; % Capacitance of tunnel
junction 1 in farads
C2=input('\n C2= \n');%C2=2.85947e-19;
Cg=input('\n 5Cg= \n');%2.59e-20;
   %C2=50e-18; % Capacitance of tunnel junction 2 in farads
   %Cg=40e-18; % Gate capacitance in farads
%  Csum=C1+C2+Cg; % Total capacitance of the central island


%Csum=num*(C1);
```

```
Csum=sqrt(Cg*Cg+4*(C1)*Cg); %Deisling model

num=input('\n Number of islands\n');
Vg=input('\n Array containing values of Vg \n');



Ec=(e^2)/(2*Csum); % Charging energy
R1=2.8e10;%R1=25.13e14; % Resistance of tunnel junction 1 in ohms
R2=9.213e9; % Resistance of tunnel junction 2 in ohms
V=[-10000:10000]; % Vector for the source-drain voltage
V=V*600e-6; % V goes from -10V to +10V
V=V+eps; % Avoid dividing by zero
N=[-8:8];
n=length(N);
Nt=N'*ones(size(V));
Vt=ones(size(N))'*V;


Inew=0;
Inew1=0;

for Vg=Vg %-0.01;
    %for Vg=-3.0:2.5:0.033
for i=1:num



     %PHYSICAL REVIEW B 73, 035331 _2006_ reference

  %  V1=(e*(num-1)*(Vt+Vg)/(2*num*Csum))+(Vg*(Cg/(Csum)));
   % V2=(e*(num-1)*(Vt+Vg)/(2*num*Csum))-(Vg*(Cg/(Csum)));

  % Deisling model

V1=(e*(Vt+Vg)/Csum)*exp(-i*(acosh(1+(Cg/(2*(C1+C2))))));
+(Vg*(Cg/(Csum)));

V2=(e*(Vt-Vg)/Csum)*exp(-(i+1)*acosh(1+(Cg/(2*(C1+C2)))));
-(Vg*(Cg/(Csum)));

p1=1/(e^2*R1);
p2=1/(e^2*R2);
DEr1=(V1*e)-Ec;
DEl1=(-V1*e)-Ec;
DEr2=(V2*e)-Ec;
DEl2=(-V2*e)-Ec;
r1=p1*DEr1./(1-exp(-DEr1/(k*T)));
l1=p1*DEl1./(1-exp(-DEl1/(k*T)));
l2=p2*DEl2./(1-exp(-DEl2/(k*T)));
r2=p2*DEr2./(1-exp(-DEr2/(k*T)));
x=r1+l2;
y=l1+r2;
prodxl=x;
```

```
prodyu=y;
prodxl(1,:)=ones(size(V));
prodyu(n,:)=ones(size(V));
for i=1:n-1,
prodxl(i+1,:)=prodxl(i,:).*x(i,:);
prodyu(n-i,:)=prodyu(n-i+1,:).*y(n-i+1,:);
end
ro=prodxl.*prodyu;
sro=sum(ro);
for i=1:length(V),
ro(:,i)=ro(:,i)/sro(i);
end

I=-e*sum(((l2-r2).*ro)); % Total current through the SET
I=I*10^12;%Inew1=(Inew1)+I;



end
%Inew=Inew1;
plot(V,I,'r','LineWidth',1.5)
hold on;

xlabel('Drain voltage [V]');
ylabel('Drain current [pA]');
title('Simulated device charcteristic');
end
```

8.2.2. Matlab Code for Device Parameters Extraction

```
%Device parameter calculations of SET multi dot system


N=input('\Input n: Number of Junctions\n');

%N=num+1;

dip=input('\Input d: Dip in the normalized Differential
conductance\n');
d=dip;
e= 1.602*10^(-19);
KbT=26*10^(-3);
R0=0.25105*10^(12);
Ec1=d*(6*KbT)*(N/(N-1));
Ec=Ec1*e;
%Ec in ev
Ceff=(e*e)/(2*Ec);
c=(Ceff*2*(N-1))/N;
RRtot1=((N/(N-1))*((3*KbT)/Ec1))-2/5;
R1=RRtot1/(RRtot1+1);
R=abs(R1*R0);
```

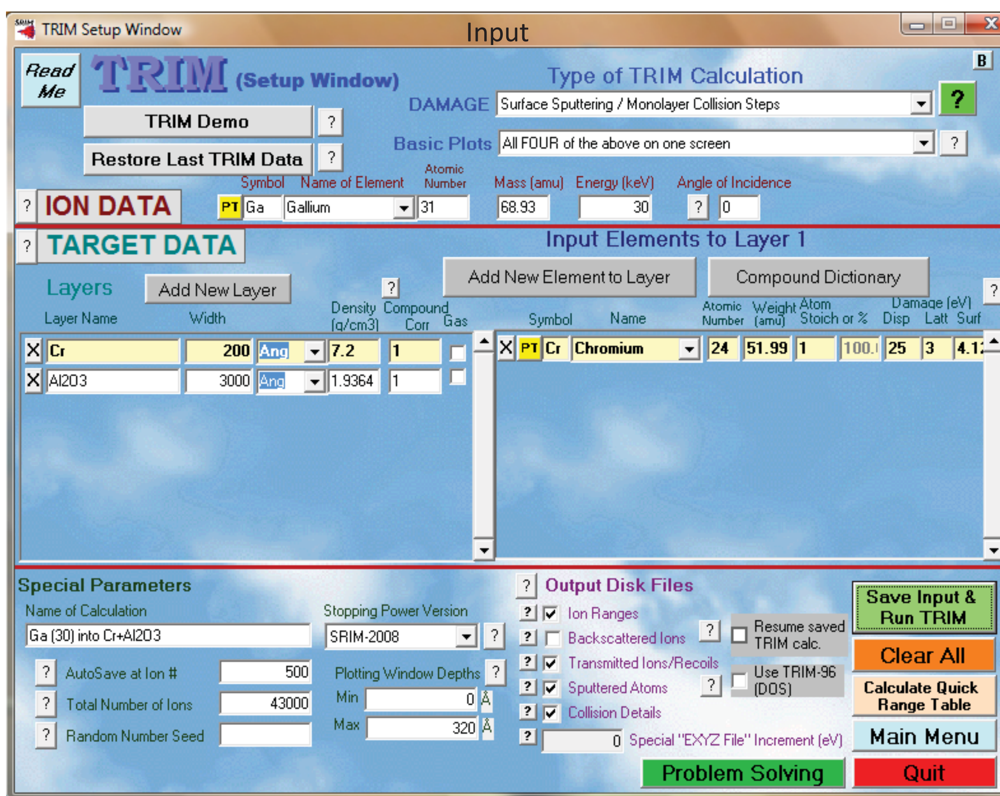
8.2.3. FlexPDE Code for Heat Conduction Calculation for Predicting the Deposition Yield

```
{ FIB based heat eneration in a stack of thin filme
 *************************************** }

title 'time-dependent 3D heat conduction'

select
   regrid=off { use fixed grid }
   ngrid=1       { smaller grid for quicker run }

coordinates
   cartesian3

variables
   Tp(threshold=300)        { the temperature variable, with approximate size}

definitions
   long = 10
   wide = 10
   K                          { thermal conductivity -- values supplied later }

  A=cos(pi*0.000003/0.6)


  Pulse=USTEP(cos(2*pi*t/0.6)-A)

   Q =  Pulse*1.247e9!*exp(-x^2-y^2-(z-9.95)^2)


 { Thermal source }
   tmax =6      { plot range control }

initial values
   Tp = 300.

equations
   div(k*19868*grad(Tp)) + Q = dt(Tp)        { the heat equation }

extrusion z = -long,9.934432,9.99404,long      { divide Z into two layers }

boundaries
```

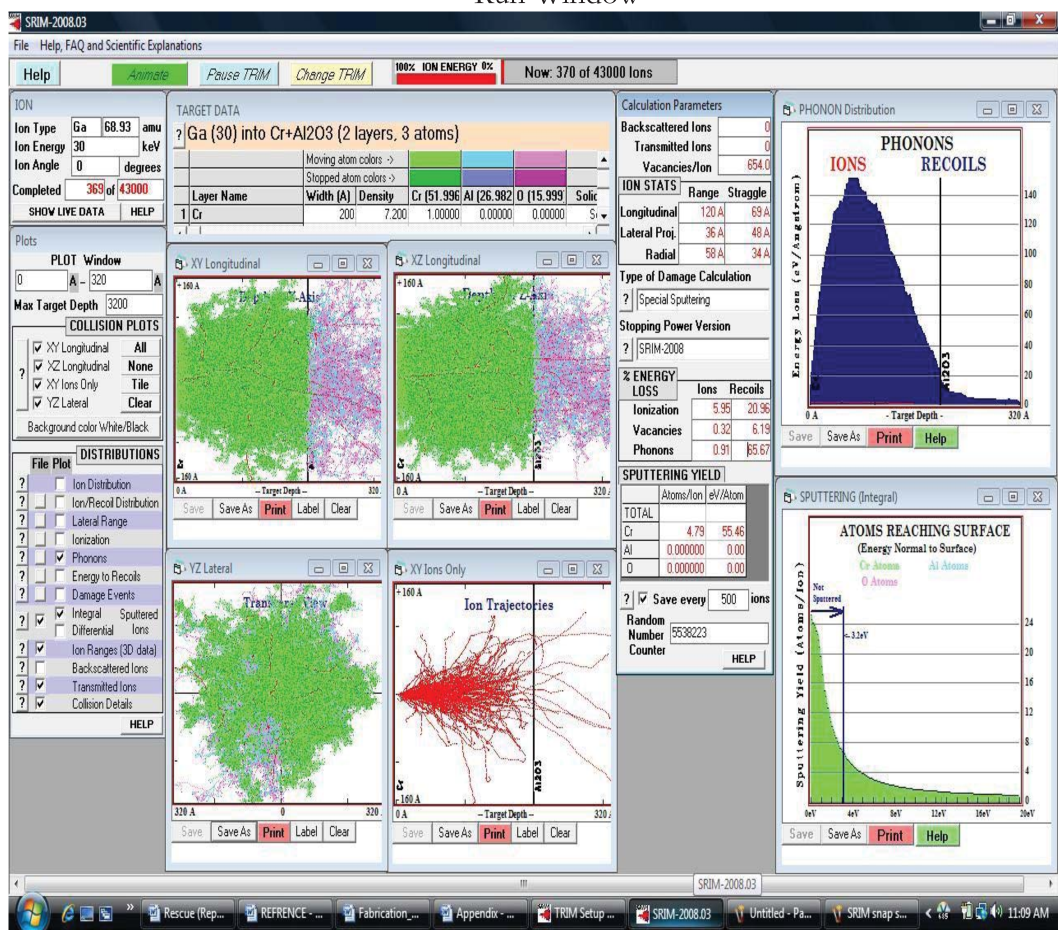
```
   surface 1 value(Tp)=300       { fix bottom surface temp }
   !surface 3 value(Tp)=0       { fix top surface temp }
{ boundaries
LIMITED REGION "Patch"
SURFACE 3
NATURAL(Tp)=Q !Pulse*1.247e9*exp(-x^2-y^2)

START(4,0) ARC(CENTER=0,0) ANGLE=360
 }
   Region 1            { define full domain boundary in base plane }
      layer 1 k=149              {Silicon}
      layer 2 k=18            { Alumina }
     layer 3 k=173
      start(-wide,-wide)
        value(Tp) = 300          { fix all side temps }
        line to (wide,-wide)   { walk outer boundary in base plane }
          to (wide,wide)
          to (-wide,wide)
          to close

{    Region 2            { overlay a second region in left half }
      layer 1 k=0.2           { bottom left brick }
      layer 2 k=0.4           { top left brick }
      start(-wide,-wide)
        line to (0,-wide)              { walk left half boundary in base plane }
          to (0,wide)
          to (-wide,wide)
          to close}

time 0 to 6 by 1e-9           { establish time range and initial timestep }

monitors
   for cycle=1
     contour(Tp) on z=0  as "XY Temp" range=(0,tmax)
     contour(Tp) on x=0  as "YZ Temp" range=(0,tmax)
     contour(Tp) on y=0  as "XZ Temp" range=(0,tmax)
     elevation(Tp) from (-wide,0,0) to (wide,0,0)  as "X-Axis Temp" range=(0,tmax)
     elevation(Tp) from (0,-wide,0) to (0,wide,0)  as "Y-Axis Temp" range=(0,tmax)
     elevation(Tp) from (0,0,-long) to (0,0,long)  as "Z-Axis Temp" range=(0,tmax)

plots
   for t = 0 by 0.59 to .6
     contour(Tp) on z=0  as "XY Temp" range=(0,tmax)
     contour(Tp) on x=0  as "YZ Temp" range=(0,tmax)
     contour(Tp) on y=0  as "XZ Temp" range=(0,tmax)
```

```
histories
    history(Tp) at  (0,0,long*0.975)
!(wide/2,-wide/2,-long/2)
               { (wide/2,wide/2,-long/2)
                (-wide/2,wide/2,-long/2)
                (-wide/2,-wide/2,-long/2)
                (wide/2,-wide/2,long/2)
                (wide/2,wide/2,long/2)
                (-wide/2,wide/2,long/2)
                (0,0,0)}
 range=(0,tmax)


histories
    history(Tp) at  (0,0,long*0.975)
(wide/2,-wide/2,-long/2)
                (wide/2,wide/2,-long/2)
                (-wide/2,wide/2,-long/2)
                (-wide/2,-wide/2,-long/2)
                (wide/2,-wide/2,long/2)
                (wide/2,wide/2,long/2)
                (-wide/2,wide/2,long/2)
                (0,0,0)
 range=(0,.6)
end
```

8.2.4. SRIM/TRIM Input for Calculating the Energy Dissipation



Run Window



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