Current Spike Reduction Technique for High Power Laser Diode Driver with Pulse Current Output

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***Abstract*-A Vertical-Cavity Surface-Emitting Laser (VCSEL) has attracted a strong interest as a pump source of diode pumped solid state (DPSS) lasers for many applications, such as welding, cutting and marking, in recent years. In the past, a series dropper has been typically used as a laser driver. However, the power loss of series dropper which adopts several kW class high power laser is very large, and the cooling system becomes much larger and whole driver is also much larger. In order to solve these problems, switch mode power supply (SMPS) is adopted as a laser driver. However, switch device breakdown problem occurs in this case. This paper clarifies the mechanism of mentioned above problem and proposes the solution technique.**

I. INTRODUCTION

A Vertical-Cavity Surface-Emitting Laser (VCSEL) has attracted a strong interest as high power laser source for many applications, such as medical, industrial and military field. In industrial applications, this laser is indirectly as pumping sources for other lasers, such as diode-pumped solid-state (DPSS) lasers or fiber-lasers used for cutting, welding and marking. The high-power solid-state laser has a two pumped methods. One is the flash-lamp pumped, and the other is the laser diode (LD) pumped. The flash-lamp pumped method is worse efficiency, because the flash-lamp had a broad spectrum, so the absorbed energy of the gain-medium becomes decrease. On the other hand, the LD pumped method is 10 times more efficient than the flash-lamp excitation, since the spectrum of the LD is overlap to the absorption spectrum of the gain-medium.

High power LDs as pumped source for DPSS lasers are Edge-emitting lasers and VCSEL. A VCSEL have more advantages than Edge-emitting lasers, such as low cost, high reliability [1].

A passively Q-switched laser is one of DPSS lasers. The gain-medium is pumped a pulse laser (Quasi–continuous-wave: QCW) from VCSEL through optical fiber. The gain-medium emits the high brightness short pulse (Q-Switched laser) when exceeding threshold of a saturable absorber, as shown in Fig. 1 [2, 3]. In this laser system, the noise and ripple current from LD driver don't affect pulse laser characteristics, so adopting of the switch mode power supply (SMPS) becomes easy.

So far, a series dropper type regulator has been typically used as a LD driver because a laser diode dislikes the noise and ripple current from the driver. However, the power loss of series dropper type regulator which adopts several kW class high power LD is very large such around 70% of input power in several 100s Amps case, and the cooling system becomes much larger and whole driver is also much larger. These drawbacks make it difficult to practical realization of the driver for high power LD.

To overcome these drawbacks, SMPS is adopted as a LD driver. Moreover, in order to realize higher efficiency, the synchronous rectification technique is introduced. However, the breakdown of switching devices due to the spike current becomes severe problem in this case.

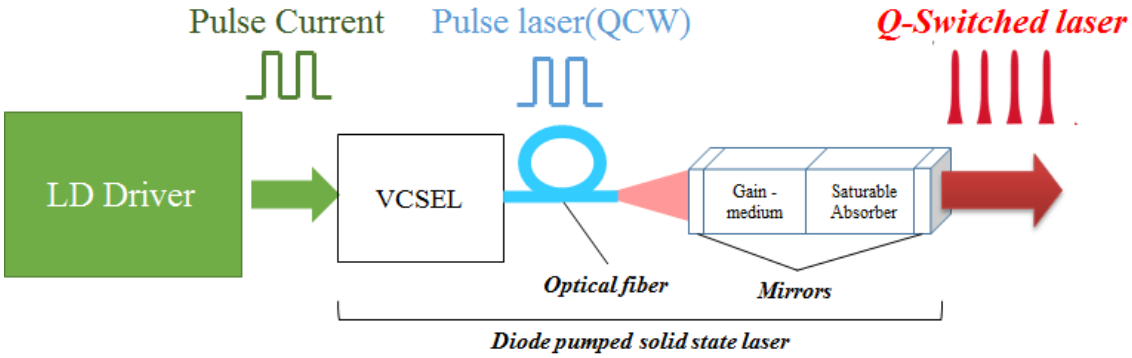


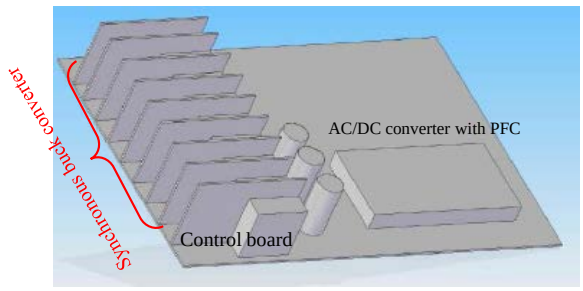
Fig. 1. Schematic configuration of laser system.

This paper investigates the steady state characteristics in order to design the controller. Moreover, the mechanism of spike current occurrence clarifies and proposes the current spike reduction technique for SMPS VCSEL driver with synchronous rectification.

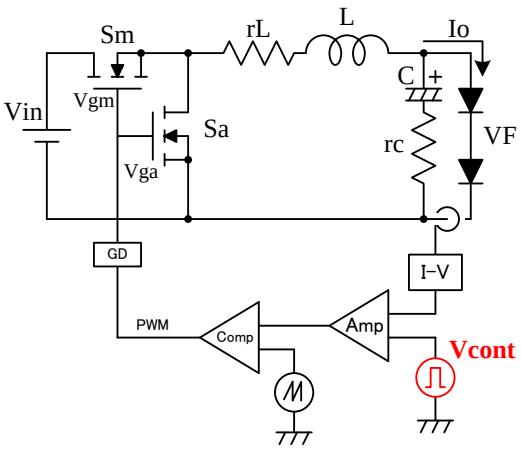
II. CIRCUIT CONFIGURATION

Figure 2 shows the system and circuit configuration of VCSELs driver. The magnetic component of buck converter become much larger in several 100s amps case. Moreover, the parallel connected power devices are needed in order to reduce power loss at power devices. Therefore, it is difficult to realize downsizing and high efficiency with only one large current converter.

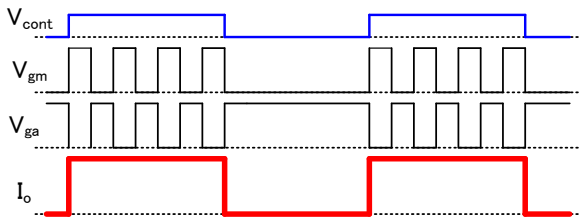
In order to reduce the system volume and power loss, the parallel connected buck converter system is proposed as shown in Fig. 2 (a). In this case, the power capacity of one buck converter is several 10s watts, and the size of magnetic component and power loss at power devices become smaller.



(a) Parallel connected system



(b) Synchronous buck converter



(c) Control waveforms

Fig. 2. System and circuit configuration.

The synchronous buck converter is used as shown in Fig. 2 (b), and the switching sequence for the output pulse current generation is shown in Fig. 2 (c). The amplitude of the output pulse current can be a by changing the reference voltage "Vcont" of error amplifier. When the output pulse becomes high, the switching devices of Sm and Sa switch again and again with high frequency as shown in Fig. 2 (c).

III. STEADY STATE CHARACTERISTICS

The operation of the synchronous buck converter can be divided into 2 states without dead time interval. Figure 3 shows the analytical model. The inductor current and capacitor voltage which are state variables treat as current source and voltage source, respectively. Moreover, the diode as a load represents a voltage source (forward voltage) and resistance.

Applying the stage space averaging method can derive the steady state characteristics as following equation [4, 5].

State 1. Sm : ON, Sa : OFF

$$\begin{cases} V_i = r_L \hat{i}_L + L\dfrac{d\hat{i}_L}{dt} + \hat{v}_c + r_c C\dfrac{d\hat{v}_c}{dt} \\ \hat{i}_L = C\dfrac{d\hat{v}_c}{dt} + i_o \\ v_F = \hat{v}_c + r_c C\dfrac{d\hat{v}_c}{dt} = r_d i_o + V_{Fo} \end{cases} \quad (1)$$

State 2. Sm : OFF, Sa : ON

$$\begin{cases} 0 = r_L \hat{i}_L + L\dfrac{d\hat{i}_L}{dt} + \hat{v}_c + r_c C\dfrac{d\hat{v}_c}{dt} \\ \hat{i}_L = C\dfrac{d\hat{v}_c}{dt} + i_o \\ v_F = \hat{v}_c + r_c C\dfrac{d\hat{v}_c}{dt} = r_d i_o + V_{Fo} \end{cases} \quad (2)$$

From Eq. (1), (2), the averaging state equation and output equation are given as Eq. (3).

$$\begin{cases} \dfrac{d\bar{\mathbf{x}}}{dt} = \mathbf{A}\bar{\mathbf{x}} + \mathbf{b}V_i + \mathbf{c}V_{Fo} \\ \bar{i}_o = \mathbf{d}\bar{\mathbf{x}} + \mathbf{e}V_{F0} \end{cases} \quad (3)$$

where,

$$\bar{\mathbf{x}} = \begin{bmatrix} \bar{i}_L & \bar{v}_c \end{bmatrix}^T \quad (4)$$

$$\mathbf{A}=\begin{bmatrix} -\frac{1}{L}\left(r_L+\frac{r_d r_c}{r_d+r_c}\right) & -\frac{1}{L}\frac{r_d}{r_d+r_c} \\ \frac{1}{C}\frac{r_d}{r_d+r_c} & -\frac{1}{C}\frac{1}{r_d+r_c} \end{bmatrix} \quad (5)$$

$$\mathbf{b}=\begin{bmatrix} \frac{D}{L} \\ 0 \end{bmatrix} \quad (6)$$

$$\mathbf{c}=\begin{bmatrix} -\frac{1}{L}\frac{r_c}{r_d+r_c} \\ \frac{1}{C}\frac{1}{r_d+r_c} \end{bmatrix} \quad (7)$$

$$\mathbf{d}=\begin{bmatrix} \frac{r_c}{r_d+r_c} & \frac{1}{r_d+r_c} \end{bmatrix} \quad (8)$$

$$\mathbf{e}=\begin{bmatrix} -\frac{1}{r_d+r_c} \end{bmatrix} \quad (9)$$

From Eq. (3), (10), the output current and voltage on steady state is given as Eq. (10).

$$\begin{cases} I_o=\frac{1}{r_L+r_d}\left(DV_i-V_{F0}\right) \\ V_F=\frac{1}{r_L+r_d}\left(r_d DV_i+r_L V_{F0}\right) \end{cases} \quad (10)$$

The parameter “VF0” in the Eq. (1) is the forward voltage at zero ampere, and “VF0” can estimate from I-V characteristic of the load diode. Moreover, the internal resistance “rd” can also estimate from I-V characteristic. Figure 4 shows the experimental I-V characteristics of the load diode. The SiC-SBDs (C3D16060D) are used as the load diode (3 series – 2 parallel). As shown in Fig. 4, the “VF0” is around 1.81V, and the “rd” is around 0.14 ohm.

Figure 5 shows analytical and experimental results of the relationship between duty ratio and output current. The load current increases in proportion to the duty ratio.

Moreover, there is the minimum duty ratio for flowing the current to the load, and when the duty ratio is lower than the minimum duty ratio the current does not flow to the load. Figure 6 show the experimental results of the efficiency characteristics. The efficiency is kept high (around 85%) for all range.

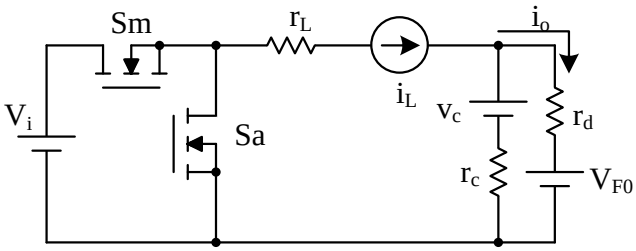


Fig. 3. Analytical model of synchronous buck converter.

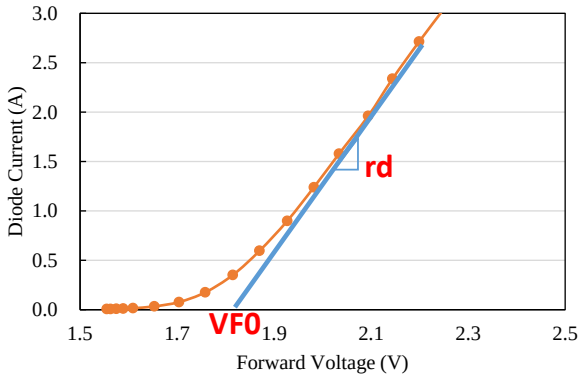


Fig. 4. I-V characteristic of load diode.

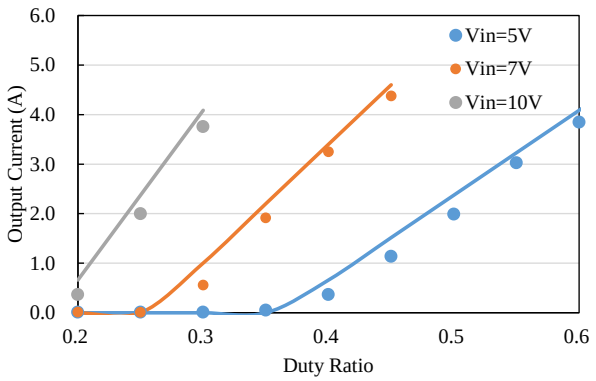


Fig. 5. Steady state characteristics.

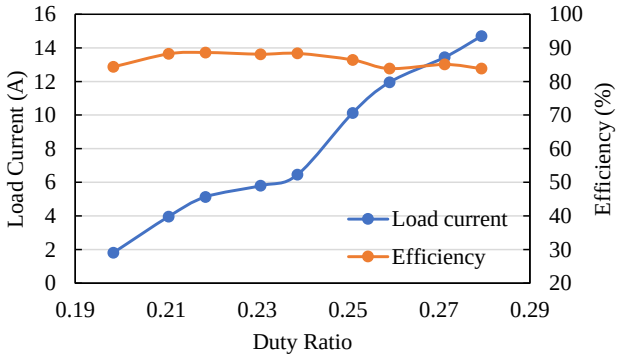
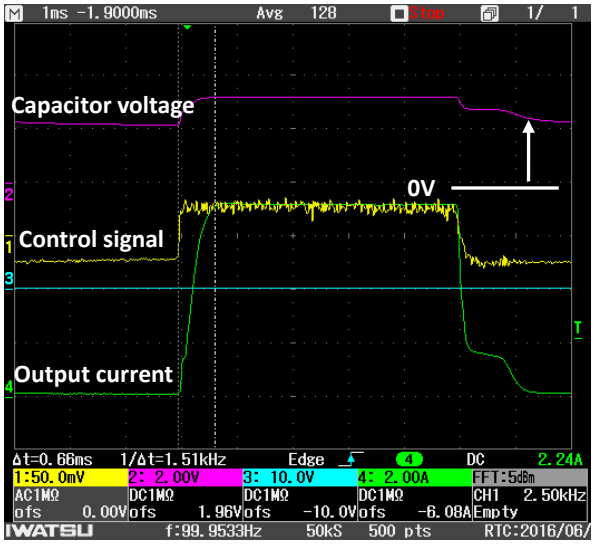


Fig. 6. Efficiency Characteristics.

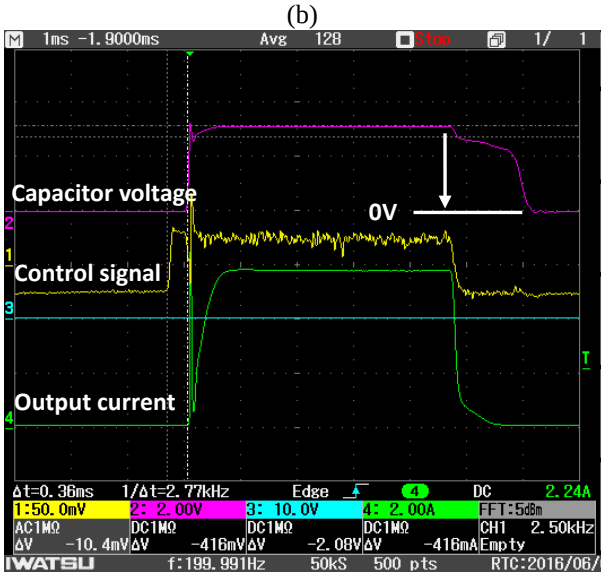
IV. CURRENT SPIKE PROBLEM AND REDUCTION TECHNIQUE

The spike current is generated when the output current switches to High from Low. This spike current leads to switching devices breakdown. Figure 7 shows the experimental key waveforms. As shown in Fig. 7 (a), the output current follows up the control signal variation and the current increases smoothly in diode rectification case. On the other hand, the output current has large spike at restart time in synchronous rectification case, as shown in Fig. 7 (b). In order to clarify the mechanism of spike current occurrence, the output capacitor voltage is paid attention. In diode rectification case, when main switch Sm is off the electric charge of the output capacitor is discharged, and the output voltage and the current flown through LD is gradually decreased.



(a) Diode rectification

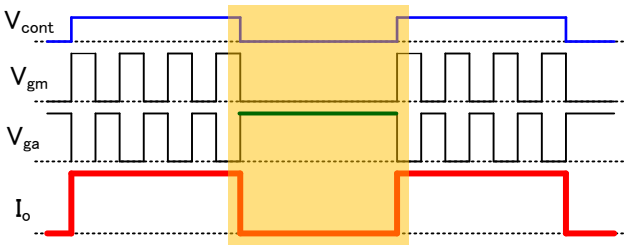
(b)



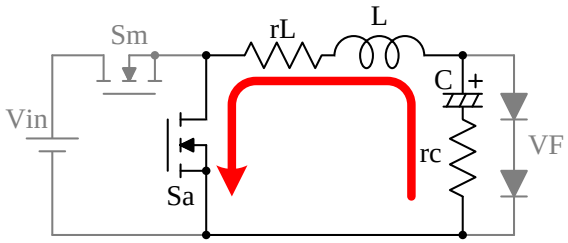
(b) Synchronous rectification

Fig. 7. Experimental key waveforms.

After that, the output voltage reaches forward voltage Vfo of LD then the rectification diode is turned off by the reverse voltage from output capacitor. Therefore, the output capacitor voltage is maintained by Vfo as shown in Fig. 7 (a). However, the output capacitor voltage reaches zero in synchronous rectification case as shown in Fig. 7 (b). This is because, the synchronous rectification switch Sa is full-on when the main switch is full-off as shown in Fig. 8 (a). In this case, the capacitor voltage is completely discharged through the synchronous rectification switch Sa as shown in Fig. 8 (b). As a result, the spike current is generated when the output current switches to High from Low, and the spike current is inrush current for output capacitor charge.

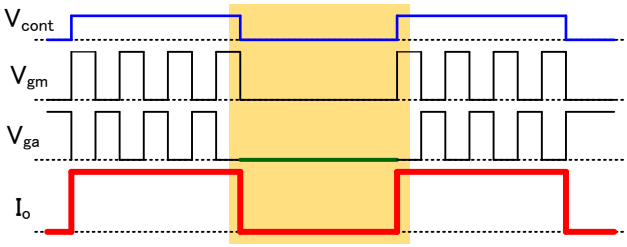


(a) Switching waveforms

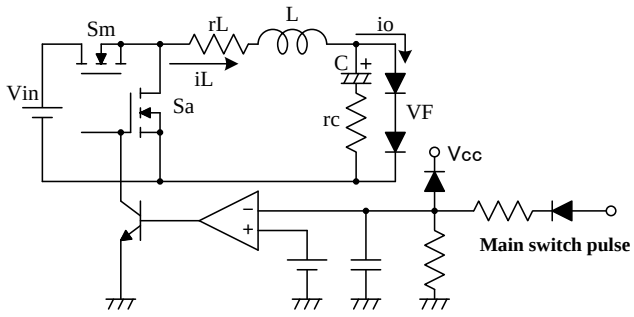


(b) Equivalent circuit when Sm off

Fig. 8. Mechanism of spike current occurrence.



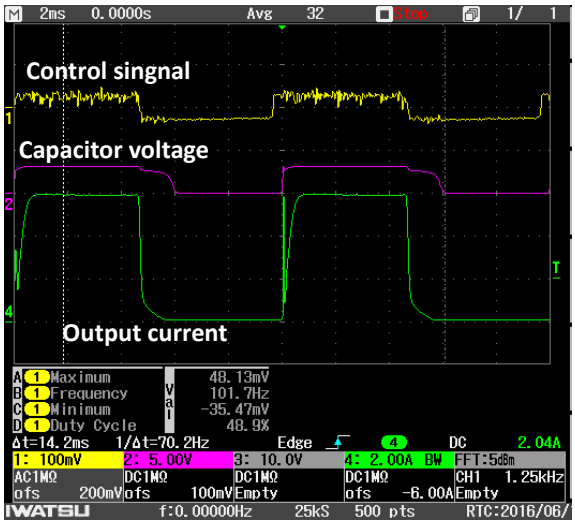
(a) Switching waveforms



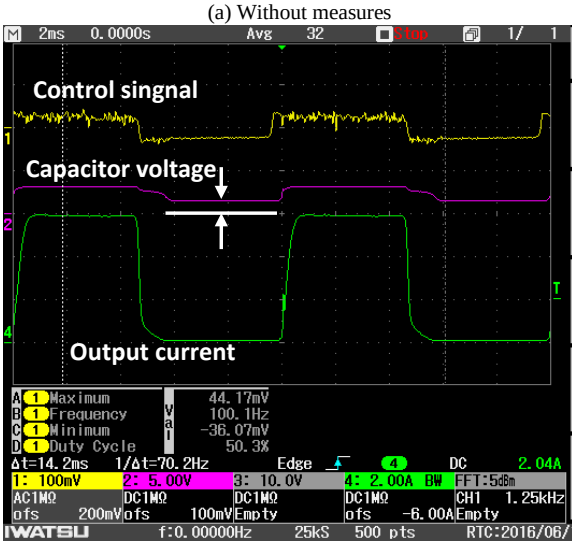
(b) Proposed turn-off circuit

Fig. 9. Proposed spike current reduction technique

In order to solve this problem, the synchronous rectification switch is forced full-off when the main switch is full-off as shown in Fig. 9 (a). When average value of the detected gate signal of the main switch Sm is smaller than the reference voltage, the transistor which is connected in gate terminal of synchronous rectification switch Sa is on. In this case, the electric charge of the input capacitance is discharged, and the n the synchronous rectification switch Sa is forced turn-off as shown in Fig. 9 (b). Figure 10 shows the experimental key waveforms with proposed technique. As shown in Fig. 10 (b), the spike current is dramatically reduced. Moreover, the output capacitor voltage is maintained forward voltage VF0 of the load diode.



(a) Without measures



(b) With proposed technique

Fig. 10. Experimental key waveforms with proposed technique.

V. CONCLUSIONS

The switch mode power supply was applied to VCSEL driver instead of series dropper type regulator. Adopting the synchronous rectification technique for more efficient caused the breakdown of the power devices due to the spike current.

This paper investigated the spike current occurrence mechanism in VCSELs driver with synchronous rectification, and the reduction technique of spike current was also proposed.

As a result, the mechanism of spike current occurrence was clarified. The complete discharge of the output capacitor through synchronous rectification switch caused spike current occurrence. Moreover, the spike current was dramatically reduced by the proposed technique.

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