Efficient Spectrum Sensing for Aeronautical LDACS Using Low-Power Correlators

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***Abstract*—Air traffic has seen tremendous growth over the last decade pushing the need for enhanced air traffic management schemes. L-band Digital Aeronautical Communication System (LDACS) is gaining traction as a scheme of choice, and aims to exploit the capabilities of modern digital communication techniques and computing architectures. Cognitive radio based approaches have also been proposed for LDACS to improve spectrum efficiency and communication capacity; however, these require intelligent compute capability in aircrafts that enforce limited space and power budgets. This paper proposes the use of multiplierless correlation to enable spectrum sensing in LDACS air-to-ground links, and its integration into the on-board LDACS system. The proposed architecture offers improved performance over traditional energy detection even at low signal to noise ratio (SNR) with lower energy consumption than a multiplier-based correlator, while also assisting in receiver synchronisation. We evaluate the proposed architecture on a Xilinx Zynq FPGA and show that our approach results in 28.3% reduction in energy consumption over the multiplier-based approach. Our results also show that the proposed architecture offers 100% accuracy in detection even at -12 dB SNR without requiring additional circuitry for noise estimation, which are an integral part of energy detection based approaches.**

I. Introduction

The sustained growth of air traffic over the past decade is pushing the limits of global air traffic management (ATM) systems, and it is expected that current systems will reach peak capacity by 2020. To address this challenge, the International Civil Aviation Organisation (ICAO) has recommended the Future Communications Infrastructure that will integrate optimal datalink protocols for enhancing air-to-air, air-to-ground, and satellite-based links. For air-to-ground links, L-band Digital Aeronautical Communications System (LDACS) is gaining traction as the preferred system for final deployment [1], [2]. LDACS is proposed as an inlay approach with legacy L-band systems like Distance Measuring Equipment, and hence has stringent requirements on transmission and reception [2]. LDACS uses modern digital modulation schemes like Orthogonal Frequency Division Multiplexing (OFDM) for improved performance and spectral efficiency over the traditional analog techniques employed by current systems.

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The introduction of digital processing blocks can also enable intelligent and on-demand spectrum allocation in LDACS, further enhancing its appeal in aeronautical systems [3]. Use of cognitive radio (CR) based dynamic spectrum access has been proposed for LDACS, which would enable opportunistic and on-demand access to the L-band channel(s) while meeting the reliability and safety requirements imposed by the standard [4]–[6]. This allows an aircraft to identify vacant spectral bands in the air-to-ground spectrum and choose a suitable channel to initiate an LDACS air-to-ground transmission. However, introducing dynamic spectrum access for LDACS presents unique challenges over terrestrial CR systems; aircraft in the range of the system are in constant motion resulting in an evolving network structure, while the channel conditions between communicating entities can change very rapidly, requiring more effective sensing compared to terrestrial CR systems. Furthermore, while ground-based systems can employ powerful computational systems to support the processing demands, implementations for aircraft must be compact and power efficient to satisfy weight, space, and power budgets.

In this paper, we present an approach for spectrum sensing using low power correlators that also serve as the receiver synchroniser for the OFDM baseband. The multiplierless correlator architecture presented for IEEE 802.16d in [7] is enhanced to cater to the longer preamble structure of LDACS air-to-ground transmissions. Further, we enhance the computational precision to improving performance in very low signal-to-noise ratio (SNR) conditions, which are likely in the LDACS scenario due to diverse channel conditions, limited transmission power, and the mobile nature of the aircraft. We show that the proposed approach outperforms traditional energy detection (ED) as well as feature detection (FD) based spectrum sensing schemes even when the ED technique incorporates highly accurate noise prediction. The multiplierless approach also results in improved power consumption, making it an ideal choice for on-board implementation. The proposed correlator is implemented on a Xilinx Zynq FPGA to evaluate the performance in hardware.

The remainder of this paper is organised as follows. Section II discusses related work in spectrum sensing, correlators, and FPGA-based cognitive radio architectures. Section III provides an overview of the LDACS standard and the data frame format used to exchange information in air-to-ground links. Section IV presents the architecture of the proposed multiplierless correlator tailored to the LDACS frame and its integration into our radio platform. In Section V, we evaluate the proposed architecture and compare it against the ED

and FD techniques for LDACS under multiple signal quality conditions. Finally, we conclude the paper in Section VI.

II. Related Works

A. Spectrum Sensing

CR based communication systems aim to make use of vacant areas of allocated spectrum by providing mechanisms to dynamically access these spectrum holes. By allowing devices to opportunistically time-share slices of spectrum, CR improves available communication bandwidth and spectral efficiency. A key requirement of a CR system is the ability to efficiently detect spectral holes. The literature describes several techniques to detect spectrum holes with varying efficiency (in terms of probability of detection and false alarm) and computational complexity. These include simple techniques like energy detection (ED) [8], as well as computationally intensive methods like matched filter detection [9], cyclostationary feature detection [10], and eigenvalue detection [11], among others. ED has generally been the most popular and widely deployed scheme due to its incoherent nature and low computational complexity. However, the accuracy of ED based spectrum sensing is significantly affected by the accuracy of noise variance estimation. ED based techniques are also unable to distinguish between licensed and malicious users, while also suffering from a lower SNR threshold for accurate detection [12]. In [5], the authors enhance traditional ED using an energy-difference based detection algorithm within the context of LDACS communication, however it is still vulnerable to errors in noise estimation.

Eigenvalue detection [11] is also an incoherent detection technique in which the maximum to minimum ratio of eigenvalues of the covariance matrix of the received signal is compared with a threshold to determine the presence/absence of communication in the current channel. Eigenvalue detection, however, requires computation of a covariance matrix and eigenvalue decomposition of the received signal, which are computationally complex tasks. Furthermore, the threshold selection for eigenvalue detection is a challenging problem, limiting the application of this approach in low power systems.

Coherent detection techniques such as cyclostationary feature detection [10] and matched filter detection, have the ability to differentiate noise (or unlicensed user transmissions) from licensed user communication. Cyclostationary feature detection exploits the cyclostationary properties of received signals to detect the presence/absence of communication in a given channel. However, decomposition of the cyclostationary features is also computationally intensive, and the technique requires relatively long observation times for high detection accuracy. Matched-filters also rely on knowledge of the transmitted signal properties such as frame structure, pilot symbol structure, and sampling frequency to provide optimal detection. As with cyclostationary feature detection, matched filter sensing is also computationally intensive as the received signals must be demodulated prior to applying the matched filtering process.

B. Multiplierless Correlators in OFDM Systems

OFDM is a widely used modulation technique in high throughput wireless systems that offers resilience to multi-path fading and methods to allocate communication spectrum in a flexible manner. This makes OFDM a key scheme in CR systems by supporting techniques like spectrum pooling, which allows temporary access of licensed (idle) spectrum to unlicensed users, thus natively enabling dynamic spectrum access [13]. A key challenge in efficient OFDM systems is receiver synchronisation, since minor errors can lead to inter-carrier or inter-symbol interference [14].

Various approaches have been proposed in the literature to achieve accurate synchronisation. They either rely on auto-correlation based techniques [15]–[17], which offers a low complexity implementation and performance that severely degrades at low signal power (low SNR), or on cross-correlation based techniques [18], which offer better performance at low SNR rates with very high implementation complexity or a combination of the two as cascaded stages [19], [20] that offers the best of both worlds. Though efficient implementations of cross-correlators were proposed [21], these are still over $5\times$ more complex than efficient implementation of classic auto-correlators. Multiplierless correlators address this challenge by replacing the multiplication operation with shift-add blocks and representing the known preamble as a sum of powers-of-2 [7], [22]. It has been shown that they can maintain the same synchronization accuracy as multiplier-based correlators, while consuming significantly fewer resources [7].

In this work, we improve the multiplierless correlator approach described in [7] and employ these correlators to perform spectrum sensing in the LDACS air-to-ground band. The correlator is enhanced to cater for the very low SNR conditions that may be encountered in aeronautical systems and also to support the larger preamble of LDACS communication. The proposed correlator can also synchronise the OFDM receiver in the LDACS ground-to-air link, thus reducing overall resource consumption. The structure mimics a matched filter detector using a-prioi knowledge of the LDACS air-to-ground and ground-to-air frame structures for receiver synchronisation and spectrum sensing in time domain.

C. FPGAs as Radio Platforms

FPGAs have been widely used in CR research owing to their hardware level adaptability, processing capabilities and parallelism. While platforms like CRUSH [23] and CRKIT [24] aimed to leverage the computational capabilities of FPGAs for implementing complex baseband modules, platforms like WARP [25] and Iris [26] used hardware-level flexibility to adapt properties of baseband modules based on channel conditions. Recent hybrid FPGA platforms have renewed interest in building adaptive radios on FPGAs as they offer close coupling of a processor for high-level cognitive software and hardware fabric for high throughput baseband processing. Software APIs can enable detailed reconfiguration of the hardware (the entire baseband or parts of it) from within the cognitive layer [27]. Such architectures have been demonstrated for LDACS [6]. We integrate the proposed correlator into this platform and

evaluate the performance in actual hardware in addition to software simulations.

III. LDACS Air-to-ground communication

LDACS is a cellular communication system involving a network of Ground Stations (GS) and Airborne Stations (AS). As mentioned, LDACS uses OFDM as the modulation scheme with FFT length 64 and a total bandwidth of 0.5 MHz for each channel. It uses 50 sub-carriers for transmission with a spacing of 9.8 KHz. These are further separated into two banks of 25 subcarriers each, which are used for ground-to-air and air-to-ground communication. LDACS defines these links as the Forward Link (FL) and Reverse Link (RL) respectively. In this work, we explore the case for opportunistic spectrum access by aircraft in the RL segment. This allows aircraft to sense spectrum usage in the RL band, determine the optimal segment, and request permission to use this spectrum from the ground station. The ground station has a global view of spectrum usage and can allow a requested channel to be used if there are no potential conflicts. Dynamic spectrum access in this manner enables more efficient use of the limited RL spectrum, especially in congested airspaces.

The RL transmission in LDACS is based on OFDM-TDMA bursts that adapt to the demands of multiple users. The transmitter design mimics a typical OFDM transmitter design, with support for adaptive coding and modulation schemes to cater to environments with strong interference, support high-priority messages, and maintain reception quality. The Inverse Fast Fourier Transform (IFFT) operation distributes the modulated data into different sub-carriers.

The receiver block also resembles a typical OFDM receiver with enhancements to eliminate interference with adjacent distance measuring equipment (DME) channels (*blanking non-linearity* block). The synchronization logic determines the starting point of a multi-frame, the Fast Fourier Transform (FFT) block demodulates the signal followed by equalization, demodulation and decoding to extract the received information.

A hierarchical arrangement of the communication in the RL is shown in Fig. 1. Communication is organised into a cyclic structure of *super frames*, each having a duration of 240 ms. Each *super frame* has one *random access* slot, used by the aircraft to request cell entry, and 4 multi-frames. Each multi-frame is composed of a variable-sized Dedicated Control (DC) segment and a data segment. Our aim is to enable dynamic access in the multi-frame segment, which would otherwise be manually allocated to different aircraft by the respective ground station.

The detailed frame structure of an RL DC segment with 4 tiles is shown in Fig. 2. The format follows a tiled structure, each tile corresponding to 720 µs, organised as 6 rows (time domain) and 25 columns (frequency domain). In time-domain, each row also has a cyclic prefix (CP) that marks the start of each row (not shown in Fig. 2). The first tile is called the synchronization tile that contains a fixed structure of AGC preamble, two synchronization symbols, and two pilot symbols, followed by a repetition of the AGC preamble, which

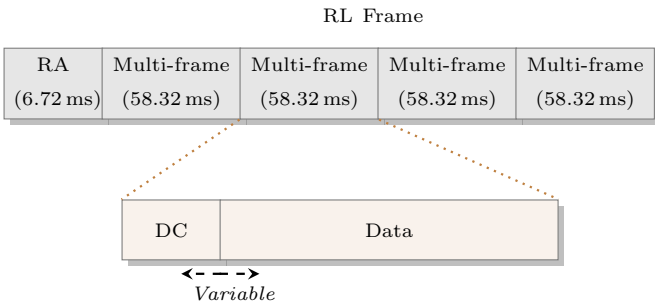


Fig. 1: Framing structure of LDACS RL communication.

aids in synchronising the LDACS receive chain at the ground station. Since the synchronization tile must be present in each RL segment, detecting its presence or absence at fixed time intervals can confirm whether the segment is currently in use or not. The remaining tiles are filled with information transmitted to the ground segment, with pilot symbols inserted at regular intervals.

The FL frame also uses a similar structure for the synchronization tile, but only uses the synchronization symbols instead of a full tile. While receiving a frame from the ground station, the aircraft must detect the synchronization symbol to detect the start of frame, and to adapt the sample timing window to reduce inter-symbol interference at the aircraft receiver. Since transmission and reception occurs at distinct time intervals, the same synchronizer block within the aircraft receiver can be used to sense the presence of communication in the RL DC segment (when the aircraft wants to transmit), and to perform accurate reception (when the aircraft receives information from the ground station).

The time duration of each OFDM symbol in LDACS is 120 µs; this, when combined with the FFT length of 64, results in 375 samples (time domain) of synchronisation information in a multi-frame (excluding the repetitive AGC preamble, and including the 11 sample CP for each row). The synchronisation elements are known (or can be calculated) a priori, allowing the use of cross-correlation for synchronisation and spectrum sensing. The complex cross-correlator structure could be built efficiently in hardware which can perform the computation at line rate to ensure on-the-fly detection. For our experimental setup, we use the minimum allowed RL DC size of two tiles (including the synchronisation tile) followed by eight data tiles as the multi-frame data, with a total frame size of 4950 samples in the time domain (including the CP for each row).

IV. Multiplierless Correlator for Spectrum Sensing in LDACS

A. Architecture of Multiplierless Correlator

Implementing such a complex cross-correlator on an modern FPGA without architecture optimisations would result in a high DSP Block requirement of 1500 blocks and registers, requiring a very large device and hence increasing static and dynamic power consumption. An optimised design can make use of the internal pipeline registers within the DSP block to absorb the delay stages, reducing the resource consumption

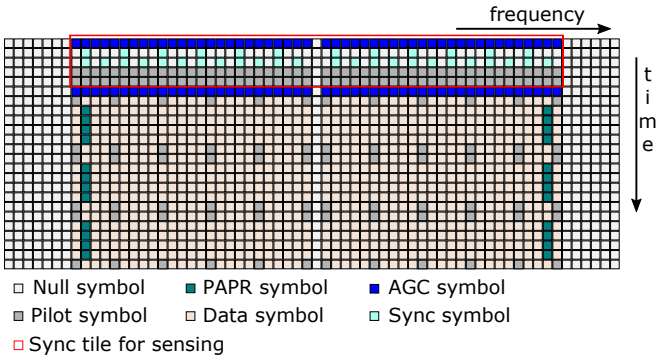


Fig. 2: Organisation of RL DC Segment, reproduced from [2].

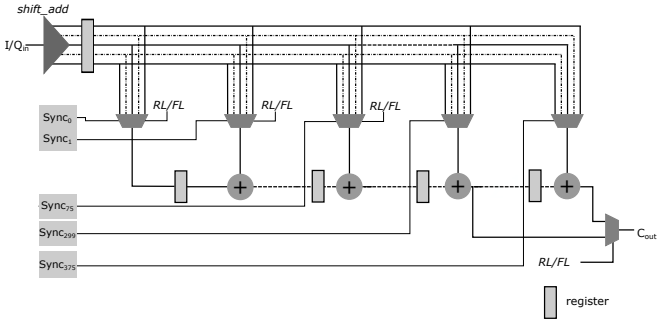


Fig. 3: Architecture of the multiplierless correlator.

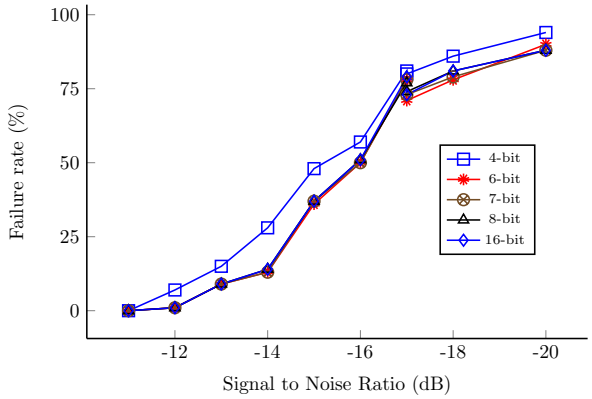


Fig. 4: Variation of detection accuracy with quantisation levels of mulitplierless correlator for LDACS-1 frame.

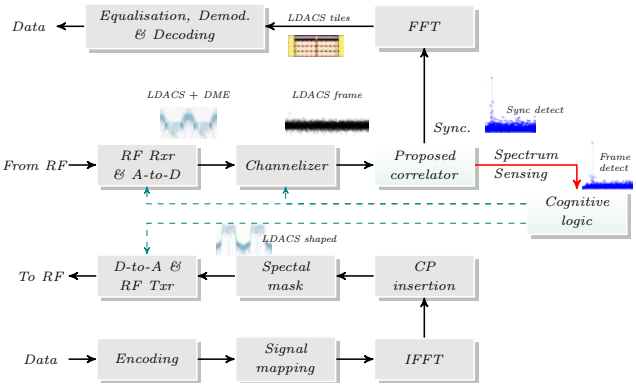


Fig. 5: Integrating the multiplierless correlator into the LDACS processing chain.

of fine-grained elements (registers/LUTs) and at the same time, increasing the overall performance of the system (clock speeds). For resource constrained implementation, the same DSP block could be reused over two computations to reduce the utilisation by half; however, this would result in an increase of latency by 4× at each node, while still consuming higher power. Multi-pumping could also be used to time-multiplex the DSP blocks [28], but this would require a higher clock rate, consuming more power. Multiplierless correlation reduces this complexity by replacing the multiplier(s) with a series of shift-adds, requiring fewer computational resources, at a cost of reduced accuracy.

The high-level architecture of the multiplierless correlator is shown in Fig. 3, which extends the correlator used in [7] for the IEEE 802.16d standard. The structure mimics a transpose-direct form filter where the multiplication operation at each tap is replaced by a multiplexer, that selects one among its many inputs based on the synchronisation symbol value at that tap (Sync[n]). Like in [7], our architecture uses a single shared *shift-add* block to optimise resource consumption; however, our design supports higher quantization levels to improve performance under very low SNR conditions. This shared *shift-add* block receives the **I** and **Q** components from the RF front-end and computes all possible multiples of the input sample corresponding to the 375 synchronisation samples. While the design in [7] uses a 64 sample preamble structure, the long synchronisation tile in LDACS creates a long critical path through the multiplexers. To mitigate this, we introduce a pipeline stage at the output of the tap multiplexers to increase the operating frequency of the design. Finally, to re-use the correlator for synchronisation of the FL frames (unique to our application), which rely on the synchronisation symbols alone instead of a full tile, the input multiplexers of taps 1–75 have an additional select line, which can bypass the *shift-add* inputs for '0'. In this case, the output of tap 225 is used for synchronisation purposes.

To optimise the quantisation level for the design, we simulated the multiplierless correlator in MATLAB using different quantisation levels and observed that there is no appreciable gain beyond 6-bit quantisation (2^{-5}), as shown in Fig. 4. Hence during implementation, the quantised values of the synchronisation tile (Sync[n]) were hard-coded with 6-bit quantization and I and Q sample wordlength of 16 bits. This allows the tools to optimize most of the multiplexers (except 1–75) into fixed logic during the implementation process, reducing the resource consumption further. The multiplexers corresponding to taps 1–75 were optimized to 2-to-1 multiplexers, also lowering resource consumption. Though this results in an inflexible design, the contents of the synchronisation tile are fixed in LDACS, allowing them to be computed off-line and loaded into the system at design time.

B. Proposed Correlator in the LDACS Processing Chain

Fig. 5 shows a simplified block diagram of the LDACS baseband, with our proposed multiplierless correlator inte-

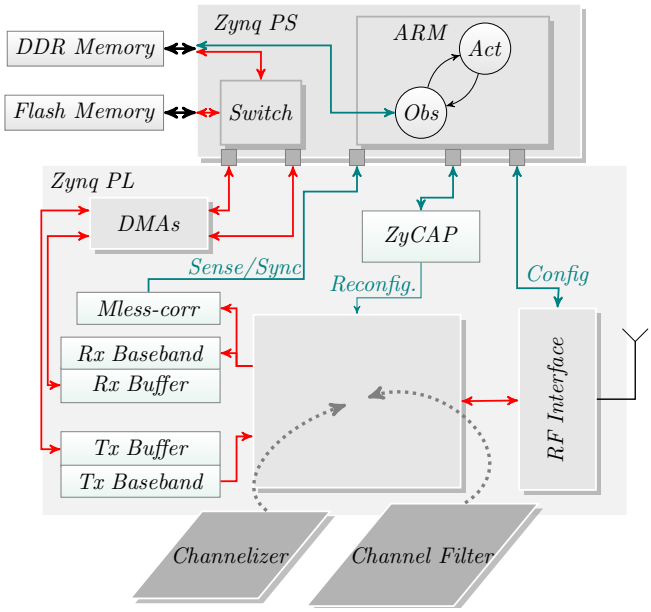


Fig. 6: Integrating multiplierless correlator into the radio platform on Zynq.

grated into the datapath. In the receive direction, the digitised signals are passed through a programmable channeliser that can extract and isolate the LDACS channels from the adjacent DME pulses. The binary data from the selected channel is fed to the correlator (part of receiver synchroniser), which attempts to estimate the symbol timing offset by detecting the start of a ground-to-air frame (signal cross correlation approach). The remainder of the receive channel baseband mimics a typical OFDM receiver – the FFT module transforms the received frame to the frequency domain, which is then equalised, demodulated and decoded to obtain the actual transmitted information. The LDACS standard also suggests the use of time- and frequency-domain interference mitigation techniques and adaptive equalisation to ensure robust and reliable reception.

When the station needs to transmit information, the spectrum sensing chain is activated and the cognitive logic configures the channeliser to scan the LDACS RL bandwidth. In this configuration, the correlator tries to detect the presence of a synchronisation tile in the data received from the channeliser output, and the information is relayed to the cognitive logic. Once a suitable channel is detected, the transmit chain is activated and the cognitive logic configures the RF modules to use the selected channel for transmission. The baseband modules map the information using QPSK modulation, applies the IFFT, and inserts the cyclic prefix to form the LDACS frame. The spectral masking filter transforms the signal to maintain the stringent LDACS specification, before feeding it to the Digital to Analog conversion and RF modules.

C. Integration into LDACS Radio Platform

The simplified diagram in Fig. 6 shows the architecture of our radio platform for LDACS [6] on a Xilinx Zynq device. The Zynq architecture integrates a dual core ARM processor and a programmable fabric on the same chip, enabling tight coupling between software and hardware processing blocks. The baseband functionality (LDACS channelizers and filters) and interfaces to the antenna are implemented in the programmable logic (PL) region of the Zynq with dedicated interfaces to interact with the cognitive software tasks running on the ARM core. Dedicated direct memory access (DMA) controllers offer high speed data movement between the baseband modules and software (or external interfaces). The platform offers high speed dynamic adaptability through parametric reconfiguration (for tuning parameters) and high-speed partial reconfiguration, which can be initiated through simple software APIs. An Analog Devices AD-FMCOMMS4-EBZ board (based on the AD9364) connects to the antenna interface to complete the RF front-end (see [6] for more details on our LDACS radio platform).

The LDACS standard allows transmission of air-to-ground information over 23 channels and places stringent requirements on the pulse shape of the transmitted signal. This results in the use of complex filters for channelization during reception and pulse shaping during transmission. We implement this non-concurrent functionality using partial reconfiguration to reduce the area overheads and power consumption; the channelization module is loaded on the fly during spectrum sensing, while the channel filter module is loaded during actual transmission. The PR approach optimises resource utilisation, leaving behind enough resources to implement other complex baseband modules, like the correlator in this case.

As shown in Fig. 6, the correlator module (marked as Mless-corr) interfaces with the output of the partially reconfigurable region (PRR) that holds either the channelizer or the channel filter (depending on the operating mode). We have replaced the filter-bank based spectrum sensing scheme in [6] with an optimal channelizer for LDACS and the channel filter with the work proposed in [29] to reduce multiplication complexity. During a sensing operation, the channelizer output is also read by the correlator module which then determines if there is an LDACS air-to-ground frame transmitted in the channel. Four such channels are available simultaneously through the channelizer, and are sequentially fed into the correlator module under software control. The result of sensing is read by the cognitive software to determine the best channel for transmission. During a normal receive operation, the software configures a register bit in the correlator module allowing it to be reused as a receiver synchroniser for the OFDM demodulator stage. The parametric configuration changes as well as the mode switch through reconfiguration are all performed using simple function calls from the cognitive software, such as `set_basesband(spectrum_sense)`. Our framework handles all the low-level steps need to manage the change in parameters or physical reconfiguration operation in response to these function calls.

V. Results

A. Implementation Results

To evaluate the resource requirements of the proposed correlator and to estimate its power consumption, we implement the

TABLE I: Detailed resource consumption of the multiplierless correlator on a Zynq XC7Z045 device as a standalone module.

Sub-module	FFs	LUTs	Slices	DSPs
shift_add	242	180	67	0
tap mux	0	5,961	1,766	0
add–delay chain	23,726	23,754	5,957	0
Total Utilisation (%)	24,000	29,895	7,806	0
% Utilisation	5.5	13.7	14.2	0
Frequency		195 MHz		

TABLE II: Resource comparison of proposed correlator on the Zynq XC7Z045 and the multiplier-based correlator on the Zynq XC7Z100 device.

Design	FFs	LUTs	Slices	DSPs	% Util.	F_{Max}
Multiplierless	24,000	29,895	7,806	0	13.67 (LUTs)	195
Multiplier-based	11,968	6,112	1,528	1,500	74.25 (DSP)	406

correlator in isolation on a Xilinx Zynq XC7Z045 FPGA. The detailed resource consumption of the sub-modules of the multiplierless correlator is shown in Table I. The design achieves an operating frequency of 190 MHz on the moderate-grade fabric of the XC7Z045, and the complete design consumes only 14% of the resources on the Zynq design allowing the rest of the baseband modules to be integrated on the same device.

For comparison, we also implemented an optimised multiplier-based correlator design (in isolation, transpose direct form), which could only fit on the larger XC7Z100 device (same architecture, but offers more resources) due to the large number of DSP blocks required. The optimised structure maps the delay elements using the internal pipeline registers within the DSP block to maximize performance with minimal fine-grained resource usage. The results of the different implementations are shown in Table II. The multiplier-based design consumes nearly 2% of LUTs and Flip-flops (FFs) and 76% of the DSP blocks available on the larger XC7Z100 device. The lower resource utilisation of the multiplierless approach enables a more compact implementation (and a smaller device with less static power consumption), making our architecture better suited for on-board systems, while also leaving sufficient resources available for the rest of the baseband functions. The pipelined structure ensures that both designs offer similar compute throughput (one output per clock cycle) and latency (376 cycles); however, the higher operating frequency achievable using multiplier-based correlators make them suited for use in LDACS ground stations for managing/monitoring spectrum allocation across all aircraft.

We also evaluate the power consumption of the design using the XPower Analyser tool from Xilinx. A post place-and-route simulation dump was used to generate the activity rates with actual LDACS frame data as the input to the correlator in each clock cycle. The simulation was performed at the design clock frequency of 125 MHz. The tool computed the total power consumption of the multiplierless correlator as 1,160 mW, with 1,038 mW contributed by the correlator operation (dynamic power) on the XC7Z045 device. The power analysis of the multiplier-based correlator at the same operating frequency resulted in an estimated consumption of 3,166 mW of dynamic power (contributed by the correlator in operation). The proposed design thus achieves a 3× advantage in dynamic power consumption. The larger device requirement for the multiplier-based design also contributes to a much higher total power, further highlighting the advantage of the proposed approach.

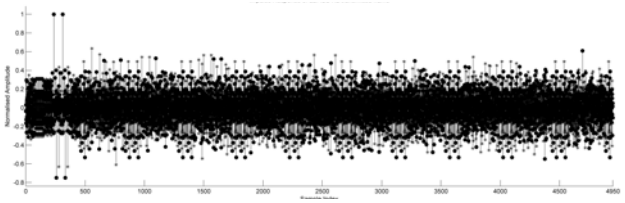
TABLE III: Resource utilisation of the Zynq radio platform after integrating the proposed correlator.

Sub-module	FFs	LUTs	BRAMs(36/18)	DSPs
Channel Filter	1,336	1,397	0/0	23
Channelizer	1,581	2,161	4/0	46
Mless-corr	24,000	29,895	0	0
RF I/F	22,781	21,970	6/4	77
Reconfig	697	767	1/1	0
Total Utilisation	49,913	55,594	11/5	123
% Utilisation	11.4	25.4	2.57	13.67

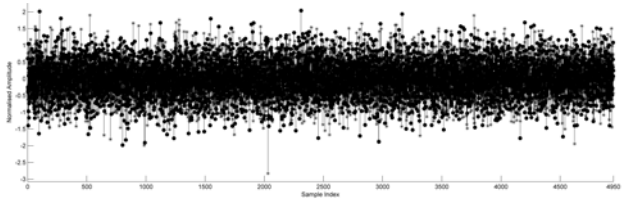
Finally, we evaluate the resource overheads of the design when integrated into our radio platform on the XC7Z045 device. The results of the implementation are shown in Table III. It can be observed that the proposed correlator is logic intensive and contributes nearly 65% of the total LUT consumption of the system (without considering the baseband modules that are not integrated here). However, our correlator doubles up as the receiver synchroniser in the LDACS OFDM baseband, a key functionality that is required to ensure accurate decoding of the received information (over the critical LDACS ground-to-air link). A standalone multiplierless cross-correlator to assist with receiver synchronisation would otherwise consume 9215 registers and 9574 LUTs more, and our proposed correlator effectively reducing the resource consumption by 16%. The overall design consumes less than 26% of resources on the device, leaving considerable general (LUTs, FFs) and specialised (DSP Blocks, BRAMs) resources for implementing baseband modules and other compute intensive processing for on-board LDACS systems.

B. Spectrum Sensing Effectiveness

To determine the effectiveness of the proposed correlator approach in detecting the presence/absence of transmissions under different SNR conditions, we generate LDACS frames in MATLAB and emulate different received conditions by adding Additive White Gaussian Noise (AWGN) components. For the proposed correlator-based approach and the multiplier-based approach, we use a single frame size (4950 samples) as the detection window. This frame size corresponds to the minimal RL frame recommended by the standard. The frequency response plot of our test input frames are shown in Fig. 7; sub-plot 7a shows the actual LDACS RL frame when it was transmitted (zero noise condition), while sub-plot 7b shows



(a) Actual LDACS RL frame with no noise.



(b) Received LDACS RL frame at -10 dB SNR.

Fig. 7: Frequency plots of generated LDACS RL frames under different SNR conditions.

the case when the frames are received at SNR conditions of -10 dB. It can be observed that the noise significantly affects the frequency response signature and noise power level of the transmitted LDACS frame, limiting the scope of simple energy detection-based techniques. An effective spectrum sensing scheme should be able to accurately determine the presence of LDACS transmission under such diverse conditions.

For our evaluation, these received frames are used as inputs to the hardware implementation (as preloaded RAM contents), simulation model of the proposed multiplier-less correlator (MATLAB simulation), and the multiplier-based model (in hardware). The inputs are quantized to 16-bit signed-magnitude fixed-precision format for hardware implementation while the MATLAB simulation model is tested with MATLAB's native accuracy (double precision floating point). The output of the proposed correlator (hardware evaluation) corresponding to received LDACS frames at different noise conditions ($SNR = 0$dB, $SNR = -10$dB) is plotted in Fig. 8. The presence of frame is determined by detection of a significant peak (more than $1.33\times$ all others in the current frame) at sample index 375, corresponding to the LDACS RL preamble. Though the plots vary significantly due to the difference in input noise levels, the proposed correlator achieves significant peaks at index 375 most of the time, resulting in positive frame detection.

We also evaluate the detection accuracy of the proposed correlator under different noise conditions with SNRs ranging from 0dB to -20dB in hardware, by loading the test frames into BlockRAMs on the FPGA. The performance is averaged over 1000 LDACS frames (4950 samples each) for each SNR condition, with each frame having a different noise signature at the same SNR. We also compare against the performance of a simulation model of the proposed correlator in MATLAB and a multiplier-based correlator in hardware (at 16-bit precision), to compare against the proposed correlator with the same input frames. The results are plotted in Fig. 9. The hardware model achieves almost identical accuracy to the multiplier-based equivalent (same truncation mechanism) and the simulation model in MATLAB (minor deviations due to rounding), with 100% positive frame detection in conditions up to -12dB.

We also compare the approach against the traditional ED based technique (in MATLAB) under different noise variance estimation conditions. The performance of ED based detection is largely determined by the noise variance estimation, which is complex to compute and is often assumed to be a known parameter while evaluating the algorithm. For our evaluation, we consider three cases of noise variance estimation: with no error (ideal condition), with 1% error and with 5% error (practical condition); the error detection techniques that can achieve these conditions are beyond the scope of this paper. We have used a 4950 sample observation window and 1% probability of false alarm as the parameters for determining the decision threshold in ED. With perfect noise estimation, it can be observed that the percentage detection of ED reduces rapidly beyond an SNR of -11dB, while the proposed approach can achieve close to 90% positive detection even at an SNR of -15dB. As the quality of noise estimation deteriorates to 1% and 5% error, the performance of ED deteriorates significantly compared to the proposed approach. The results show that the proposed correlator based technique offers better detection accuracy over the ED technique without incurring the computational complexities associated with highly accurate noise estimation.

Finally, we also compare the proposed technique against cyclostationary feature detection (CFD) and autocorrelation based schemes from the literature. A low-complexity cyclostationary technique was proposed for sensing spectrum in a femtocell design for LTE networks [30], while the work in [31] explores a cooperative cyclostationary technique for spectrum sensing in low SNR conditions in generic OFDM systems (which we have adapted to a single-cycle CFD scheme for LDACS). The autocorrelation technique described in [32] relies on the detection of autocorrelation coefficient for spectrum sensing in generic OFDM systems. For our experiments, we adapt these algorithms to the properties of LDACS RL-DC frame and simulate the performance in MATLAB, under different noise conditions with SNRs ranging from 0dB to -20dB. The results, shown in Fig. 9, clearly shows that the proposed technique offers higher detection accuracy, even while running at lower computational precision. It should be noted that the detection accuracy of techniques which rely on periodic properties of the signal will improve further as the detection window is increased, which requires detection across multiple timeslots in the LDACS RL-DC segment.

VI. Conclusion

Legacy communication systems in the aeronautical domain have been unable to keep pace with the ever increasing volume of information being exchanged between aircraft and ground stations. New standards like LDACS aim to improve air-traffic management, offering new pathways for communicating between air and ground stations while ensuring coexistence with legacy L-band systems. While techniques like dynamic spectrum access can enable efficient use of the spectrum

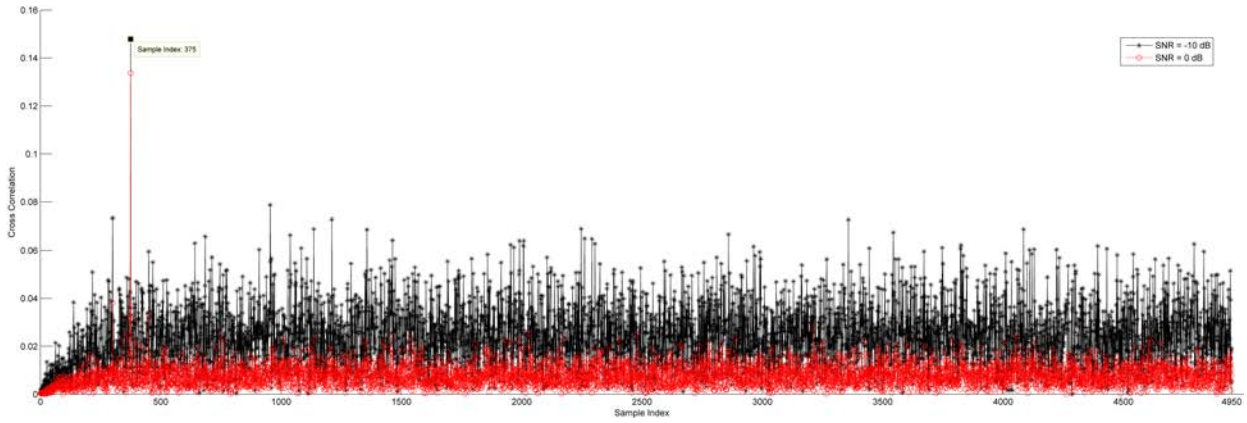


Fig. 8: Correlator output at SNR of 0dB and −10dB.

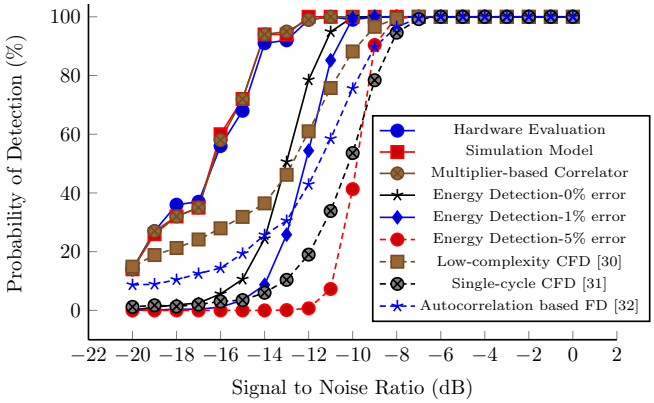


Fig. 9: Comparison of detection accuracy of RL DC frames using different detection techniques.

in LDACS, the associated operations are computationally intensive, requiring efficient techniques to implement them on on-board systems that operate under tight constraints.

In this paper, we proposed the use of multiplierless correlation for spectrum sensing in the LDACS digital front-end, with the added benefit of the same hardware being used for timing synchronization in the LDACS OFDM receiver. We show that the proposed architecture offers 3× energy reduction over multiplier-based correlators and better detection of LDACS RL frames in air-to-ground channels even at low SNR values, compared to traditional ED systems and other feature detection techniques. Moreover, the observation window for spectrum sensing can be as small as the minimal RL frame structure, enabling faster turn-around from sensing to start of transmission. Our results show that the proposed correlator based spectrum sensing offers 100% detection accuracy even −12dB SNR without requiring noise estimation, reducing the computational complexity in on-board implementation.

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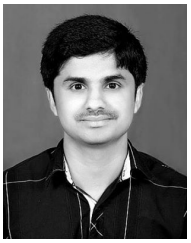

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