Adaptive Stabilization of Uncontrolled Rectifier Based AC–DC Power Systems Feeding Constant Power Loads

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***Abstract*—It is known that, when tightly regulated, actively controlled power converters behave as constant power loads (CPLs). These loads can significantly degrade the stability of their feeder system. The loop-cancelation technique has been established as an appropriate methodology to mitigate this issue within dc–dc converters that feed CPLs. However, this has not yet been applied to uncontrolled rectifier based ac–dc converters. This paper therefore details a new methodology that allows the loop-cancelation technique to be applied to uncontrolled rectifier based ac–dc converters in order to mitigate instability when supplying CPLs. This technique could be used in both new applications and easily retrofitted into existing applications. Furthermore, the key contribution of this paper is a novel adaptive stabilization technique, which eliminates the destabilizing effect of CPLs for the studied ac–dc power system. An equation, derived from the average system model, is introduced and utilized to calculate the adaptable gain required by the loop-cancelation technique. As a result, the uncontrolled rectifier based ac–dc feeder system is always stable for any level of CPL. The effectiveness of the proposed adaptive mitigation has been verified by small-signal and large-signal stability analysis, simulation, and experimental results.**

***Index Terms*—AC–DC converters, constant power load (CPL), loop-cancelation technique, negative impedance instability.**

I. Introduction

ACTIVELY controlled power converters are widely used in many applications. Unfortunately, when tightly regulated, actively controlled power converters behave as constant power loads (CPLs) [1], [2]. These CPLs can significantly degrade the stability of their feeder system [3]–[5]. It can be seen from previous publications [6]–[10], that unstable system operation can be predicted from dynamic mathematical models via control theory. In order to derive models in such a way as to be suitable for stability analysis the averaging technique [9], [10] can be utilized. However, mathematical prediction only states when the system will become unstable. In order to eliminate the destabilizing effect, mitigation techniques are required.

In terms of mitigation techniques, there are three possible ways to apply a compensating signal for eliminating the destabilizing effect. The first is to generate the mitigating signal on the feeder side [11]–[20]. In this case, the system can be stabilized without conciliating the load performance. However, this way cannot be applied to a feeder system that utilizes an uncontrolled rectifier based ac–dc rectifier due to the absence of the control loop in the feeder subsystem. In this situation, a second mitigation technique can be used in which the compensating signal is injected into the CPL control loop to modify the load impedance for stable operation [21]–[27]. The drawback of mitigation on the CPL side is that the additional compensating signal may deteriorate the load performance. The final way to eliminate the destabilizing effect is by connecting an auxiliary circuit between the feeder and load subsystems [28]–[30]. This method is suitable for power systems having existing feeder and load subsystems that are impossible to modify. In this paper, the feeder system includes an uncontrolled rectifier in which the output voltage cannot be adjusted. Hence, the additional auxiliary circuit approach for mitigation is selected.

In terms of the control techniques to create the compensating signal, there are two well-known approaches. The first is the active damping method [11], [15]–[30]. In this case, a virtual resistance is used to increase the damping of the filter circuit. However, the power level of the CPL (P_{CPL}) that can be mitigated is limited [12], [14]. Therefore, a second approach was introduced, namely the loop-cancelation technique [12], [14]. This technique can mitigate system instability at higher values of P_{CPL} than those compensated by active damping. However, this technique has only been applied to dc–dc converters, as described in [12]. The application of the loop-cancelation technique to uncontrolled rectifier based ac–dc power systems via an auxiliary circuit has not been reported in previous publications, e.g., [12]. Hence, in this paper, instability mitigation for uncontrolled rectifier based ac–dc power systems via the loop-cancelation technique is presented. Moreover, this paper also presents a novel adaptive stabilization technique based on an equation that can be derived from the average system model. The equation is used to determine the adaptable gain required

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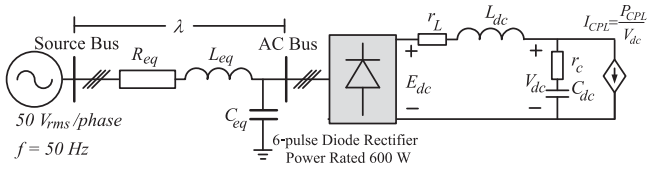

Fig. 1. AC–DC power system feeding an ideal CPL.

for loop cancelation. This gain depends on the power level of the CPL, which can be calculated from voltage and current sensors on the dc bus. As a result of this methodology, the system can automatically ensure stability under all operating conditions. The stability study presented in this paper, using small-signal and large-signal stability analysis, confirms that the mitigated system is always stable. In addition, simulation and experimental results are also presented to verify the proposed adaptive stabilization technique that eliminates the destabilizing effect of the CPL.

The paper is structured as follows. In Section II, an ac–dc power system feeding an ideal CPL is introduced to illustrate the effect of CPLs. In Section III, the loop-cancelation technique for ac–dc power systems feeding ideal CPLs is explained. An explanation of how to apply the loop-cancelation technique to the ac–dc power system, the derivation of mathematical model, the system stability analysis via the eigenvalue theorem and the phase-plane plot, the concept of the adaptive stabilization, and the simulation results are all addressed in Section III. A realistic ac–dc power system is then analyzed in Section IV. In this case, parallel controlled buck converters are used as CPLs instead of the ideal CPLs. Simulation and experimental results are also presented in Section IV to confirm that the proposed mitigation technique can eliminate the destabilizing effect of the CPL. Finally; Section V concludes and discusses the benefits of the adaptive stabilization technique for the ac–dc power system.

II. AC–DC Power System Feeding an Ideal CPL

The ac–dc power system investigated in this study is depicted in Fig. 1. An ac–dc power system including an uncontrolled rectifier is considered in this paper because it is still widely used in many applications. It consists of a balanced three-phase voltage source, a transmission line represented by R_{eq}, L_{eq}, and C_{eq}, a six-pulse diode rectifier, dc-link filters represented by r_L, $L_{\rm dc}$, r_c, and $C_{\rm dc}$, and an ideal CPL represented by a dependent current source. The parameters of the system in Fig. 1 are given in Table I. Note that the inductance value has been chosen in order for stability to occur at a power level that is able to be verified experimentally.

It is known that CPLs can degrade the stability of their feeder systems via the dc-link filter [3]–[5]. Many research works have already presented how to predict unstable operation using a mathematical model of the system. For three-phase systems with six-pulse diode rectifiers, the DQ method [6]–[8] can be applied in order to analyze the three-phase rectifier circuit and obtain a dynamic model suitable for stability study. The eigenvalue theorem [8] can then be applied to the linearized model for stability analysis. Based on the procedure in [9], the eigenvalue plot of the system shown in Fig. 1, with the parameters in Table I, is depicted in Fig. 2. It can be seen from Fig. 2 that the system will be unstable when the value of $P_{\rm CPL}$ reaches 320 W. In this paper, it will be shown that as a result of the techniques used, the ac–dc system shown in Fig. 1 can provide power exceeding 320 W, in this case up to 600 W (rated power), without instability occurring. The details of the technique used for the stabilization of the uncontrolled rectifier based ac–dc power system will be explained in Section III. Moreover, the novel adaptive stabilization for ac–dc power systems feeding the CPLs is also explained.

TABLE I
Parameters of the System in Fig. 1

Parameters	Value
V_s	50 $V_{\rm rms/phase}$
ω	$2\pi \times 50$ rad/s
R_{eq}	0.1 Ω
L_{eq}	0.21 mH
C_{eq}	2 nF
r_L	0.57 Ω
r_c	2.97 Ω
$L_{\rm dc}(\Delta I_{\rm dc} \leq 0.5$ A)	37.7 mH
$C_{\rm dc}(\Delta V_{\rm dc} \leq 5$ V)	237.35 μF

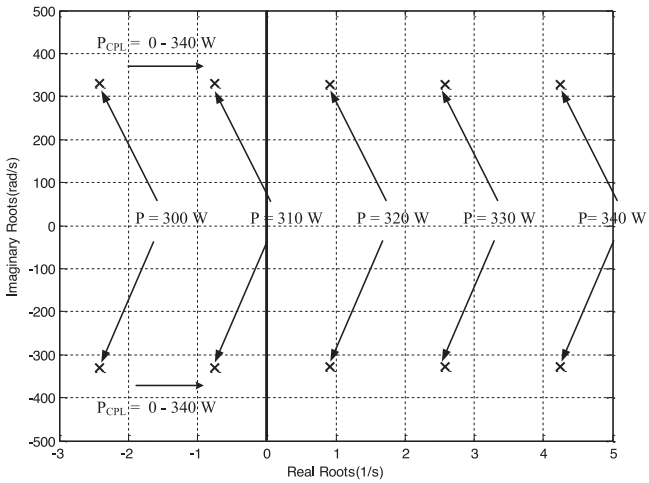

Fig. 2. Eigenvalue plot of the system before applied the proposed mitigation technique.

III. Loop-Cancelation Stabilization of an AC–DC Power System Feeding an Ideal CPL

Within this section, the new methodology for the application of the loop-cancelation technique to uncontrolled rectifier based ac–dc converters will be detailed. The established ac–dc converters will be detailed. The established ac–dc power system, on which this study is based, is shown in Fig. 1. The newly proposed ac–dc power system, including the loop-cancelation technique, is depicted in Fig. 3. An ideal CPL is considered initially in order to facilitate the calculation of the adaptable gain, as will be described later in this section.

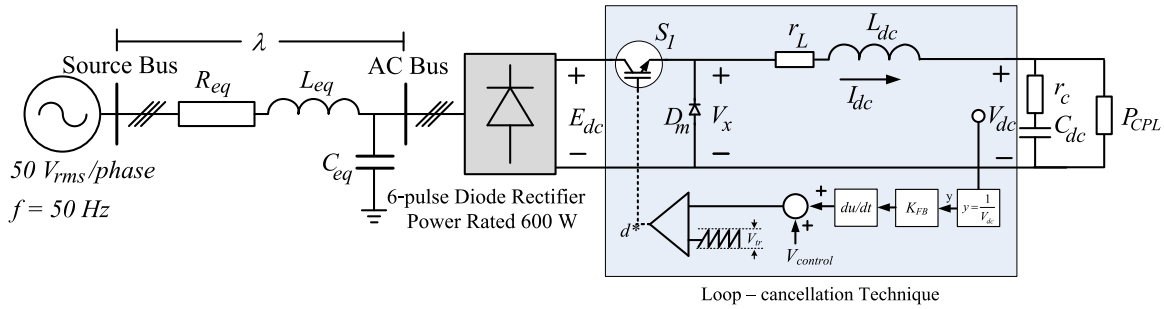

Fig. 3. AC–DC power system with the loop-cancelation technique.

Within dc–dc converters, the control of output dc voltage is a natural feature. The loop-cancelation method [12] can therefore be conveniently applied to introduce a corrective action by adjusting the converter duty cycle. In contrast, the ac–dc power system in this study employs an uncontrolled rectifier in which the output voltage cannot be adjusted and is defined by the ac voltage magnitude only. Therefore, this study proposes a new approach by introducing into the dc link a controlled switch S_1 to both control the output voltage and introduce the proposed loop-cancelation technique. Only switch S_1 and diode D_m are added into the system, whereas r_L, $L_{\rm dc}$, r_c, and $C_{\rm dc}$ are the existing dc-link filter of the rectifier circuit. Therefore, the effect of S_1 and D_m on the overall system power loss and cost is very small. The duty cycle d^* is used to control the switch S_1. d^* can be calculated using

$$d^* = \frac{1}{V_{\rm tr}}\left(V_{\rm control} + K_{\rm FB}\frac{d}{dt}\left(\frac{1}{V_{\rm dc}}\right)\right) \tag{1}$$

where $V_{\rm tr}$ is the amplitude of a triangular signal that can be set by the user. Based on the loop-cancelation technique reported in [12] for dc–dc converters, it is known that the feedback gain $K_{\rm FB}$ is a vital parameter that enables the designer to determine the characteristic of output dc-link filter damping. Moreover, if the designer can determine the appropriate value for $K_{\rm FB}$, the desired time-domain response can be obtained and the destabilizing effect can be completely eliminated.

First, for the proposed uncontrolled rectifier based ac–dc power system, the mathematical model will be derived. From this, the equation for calculating $K_{\rm FB}$ can be obtained. As detailed in previous publications [6]–[10], feeder systems with three-phase rectifiers can be analyzed using the DQ method, while the behavior of S_1 can be eliminated by using the generalized state-space averaging (GSSA) method [6]. The equivalent circuit of the system in Fig. 3, represented in the *dq*-frame, is shown in Fig. 4. After applying the DQ method, the three-phase diode rectifier can be treated as a transformer in the *dq*-frame [10]. The GSSA is then used to eliminate the switching behavior of S_1. Applying Kirchhoff's voltage law and Kirchhoff's current law to the circuit shown in Fig. 4, with d^* given by (1), the mathematical model of the proposed ac–dc power system under continuous conduction mode, using the loop-cancelation technique, is defined by the following equation:

$$\begin{cases}
\dot{I}_{ds} = -\frac{R_{eq}}{L_{eq}}I_{ds} + \omega I_{qs} - \frac{1}{L_{eq}}V_{{\rm bus},d} + \frac{1}{L_{eq}}V_{sd} \\
\dot{I}_{qs} = -\omega I_{ds} - \frac{R_{eq}}{L_{eq}}I_{qs} - \frac{1}{L_{eq}}V_{{\rm bus},q} + \frac{1}{L_{eq}}V_{sq} \\
\dot{V}_{{\rm bus},d} = \frac{1}{C_{eq}}I_{ds} + \omega V_{{\rm bus},q} \\
\qquad\qquad -\sqrt{\frac{3}{2}}\cdot\frac{2\sqrt{3}V_{\rm tr}}{\pi C_{eq}\left(V_{\rm control}+K_{\rm FB}\frac{d}{dt}\left(\frac{1}{V_{\rm dc}}\right)\right)}I_{\rm dc} \\
\dot{V}_{{\rm bus},q} = -\omega V_{{\rm bus},d} + \frac{1}{C_{eq}}I_{qs} \\
\dot{I}_{\rm dc} = \sqrt{\frac{3}{2}}\cdot\frac{2\sqrt{3}V_{\rm control}}{\pi L_{\rm dc}V_{\rm tr}}V_{{\rm bus},d} - \frac{(r_\mu+r_L+r_c)}{L_{\rm dc}}I_{\rm dc} - \frac{1}{L_{\rm dc}}V_{\rm dc} \\
\qquad +\frac{r_c P_{\rm CPL}}{L_{\rm dc}V_{\rm dc}} + \sqrt{\frac{3}{2}}\cdot\frac{2\sqrt{3}}{\pi L_{\rm dc}C_{\rm dc}}\frac{K_{\rm FB}V_{{\rm bus},d}}{V_{\rm tr}}\frac{d}{dt}\left(\frac{1}{V_{\rm dc}}\right) \\
\dot{V}_{\rm dc} = \frac{1}{C_{\rm dc}}I_{\rm dc} - \frac{P_{\rm CPL}}{C_{\rm dc}V_{\rm dc}}
\end{cases} \tag{2}$$

A new variable $I_{\rm dc1}$, as given by (3), can be used to simplify the system model

$$\dot{I}_{\rm dc1} = \dot{I}_{\rm dc} - \sqrt{\frac{3}{2}}\cdot\frac{2\sqrt{3}}{\pi L_{\rm dc}}\frac{K_{\rm FB}V_{{\rm bus},d}}{V_{\rm tr}}\frac{d}{dt}\left(\frac{1}{V_{\rm dc}}\right). \tag{3}$$

Hence, (2) can be written as the following equation:

$$\begin{cases}
\dot{I}_{ds} = -\frac{R_{eq}}{L_{eq}}I_{ds} + \omega I_{qs} - \frac{1}{L_{eq}}V_{{\rm bus},d} + \frac{1}{L_{eq}}V_{sd} \\
\dot{I}_{qs} = -\omega I_{ds} - \frac{R_{eq}}{L_{eq}}I_{qs} - \frac{1}{L_{eq}}V_{{\rm bus},q} + \frac{1}{L_{eq}}V_{sq} \\
\dot{V}_{{\rm bus},d} = \frac{1}{C_{eq}}I_{ds} + \omega V_{{\rm bus},q} - \sqrt{\frac{3}{2}}\cdot\frac{2\sqrt{3}V_{\rm tr}}{\pi C_{eq}V_{\rm control}}I_{\rm dc1} \\
\qquad +\frac{18K_{\rm FB}}{\pi^2 C_{eq}L_{\rm dc}V_{\rm control}}\frac{V_{{\rm bus},d}}{V_{\rm dc}} \\
\dot{V}_{{\rm bus},q} = -\omega V_{{\rm bus},d} + \frac{1}{C_{eq}}I_{qs} \\
\dot{I}_{\rm dc1} = \sqrt{\frac{3}{2}}\cdot\frac{2\sqrt{3}V_{\rm control}}{\pi L_{\rm dc}V_{\rm tr}}V_{{\rm bus},d} - \frac{(r_\mu+r_L+r_c)}{L_{\rm dc}}I_{\rm dc1} - \frac{1}{L_{\rm dc}}V_{\rm dc} \\
\qquad -\sqrt{\frac{3}{2}}\cdot\frac{2\sqrt{3}(r_\mu+r_L+r_c)K_{\rm FB}}{\pi L_{\rm dc}^2 V_{\rm tr}}\frac{V_{{\rm bus},d}}{V_{\rm dc}} + \frac{r_c P_{\rm CPL}}{L_{\rm dc}V_{\rm dc}} \\
\dot{V}_{\rm dc} = \frac{1}{C_{\rm dc}}I_{\rm dc1} - \frac{P_{\rm CPL}}{C_{\rm dc}V_{\rm dc}} + \sqrt{\frac{3}{2}}\cdot\frac{2\sqrt{3}}{\pi L_{\rm dc}C_{\rm dc}}\left(\frac{K_{\rm FB}}{V_{\rm dc}V_{\rm tr}}\right)V_{{\rm bus},d}
\end{cases} \tag{4}$$

It can be seen from (4) that $K_{\rm FB}$ is presented in the system model. The effect of $K_{\rm FB}$ can be assessed via a plot of the dominant eigenvalues. These eigenvalues were calculated from the linearization of (4). The system parameters for this plot are given in Table I with $V_{\rm control} = 2.9\,{\rm V}$, $V_{\rm tr} = 3\,{\rm V}$, and $P_{\rm CPL} = 320\,{\rm W}$. The dominant eigenvalue plot when gain $K_{\rm FB}$ is varied from 0 to 2.45 is shown in Fig. 5. The plot within Fig. 5 can be used to determine the best value of $K_{\rm FB}$ to avoid unstable operation with the desired time-domain response depending on

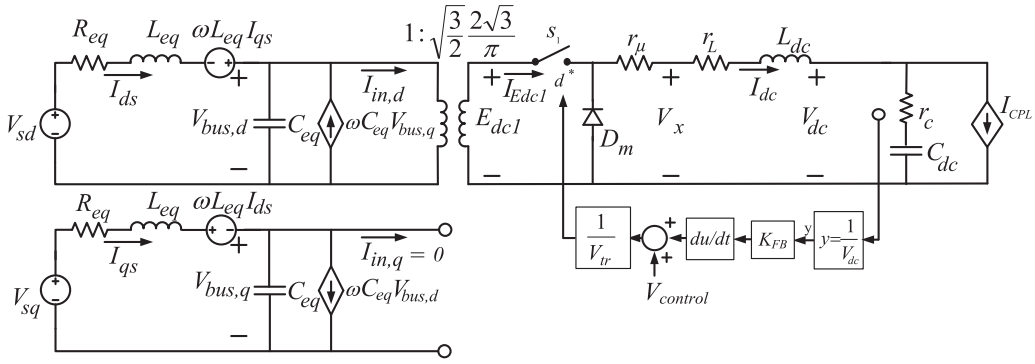

Fig. 4. Equivalent circuit of the ac–dc power system with the loop-cancelation technique in the *dq*-frame.

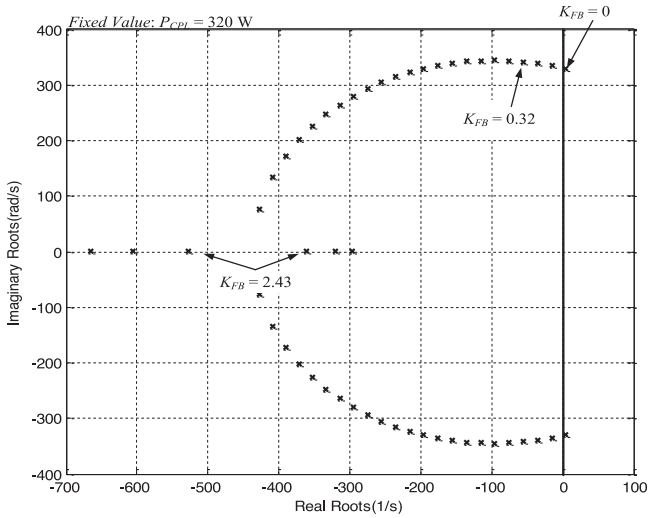

Fig. 5. Eigenvalue plot for the ac–dc power system with the loop-cancelation technique by varying K_{FB}.

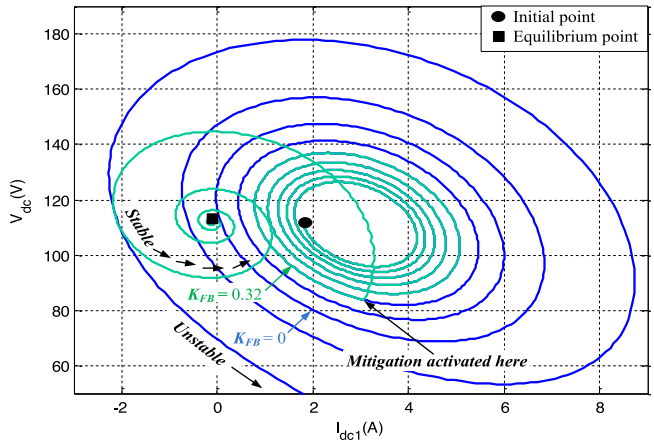

Fig. 6. Phase-plane plot of the ac–dc power system.

the location of dominant poles. However, the plot will change when P_{CPL} changes. Therefore, the appropriate value of K_{FB} to mitigate the instability problem should be adapted according to the variation of P_{CPL}.

Large-signal stability analysis of the example system is shown in Fig. 6 via a phase-plane plot. Initially, P_{CPL} is set at 200 W. Subsequently, P_{CPL} is increased to 320 W. If $K_{\mathrm{FB}} = 0$ (without mitigation), huge oscillation occurs, as shown by the blue line in Fig. 6. Conversely, if the proposed mitigation is applied with $K_{\mathrm{FB}} = 0.32$, the system can regain stability as depicted by the green line in Fig. 6. It can be seen from Figs. 5 and 6 that there is good agreement between the eigenvalue plot and phase-plane plot. Both methodologies confirm that stability is achieved when $K_{\mathrm{FB}} = 0.32$. However, $K_{\mathrm{FB}} = 0.32$ is for $P_{\mathrm{CPL}} = 320$ W. If P_{CPL} is increased, K_{FB} should be increased to ensure that the system maintains stable operation. Hence, K_{FB} must be adaptable depending on the level of P_{CPL}. In this paper, a novel equation is used to calculate the adaptable gain. The derivation of this equation is detailed as follows.

Considering only the characteristics of output dc-link filter damping, the differential equations $\dot{I}_{\mathrm{dc1}}$ and $\dot{V}_{\mathrm{dc}}$ in (4) will now be analyzed. It can be seen that the nonlinear terms of K_{FB} occur in both $\dot{I}_{\mathrm{dc1}}$ and $\dot{V}_{\mathrm{dc}}$. However, normally $(r_\mu + r_L + r) << L_{\mathrm{dc}}$, therefore only the nonlinear terms of K_{FB} within $\dot{V}_{\mathrm{dc}}$ are required. If parameter P_1 is defined as

$$P_1 = \sqrt{\frac{3}{2}}\frac{2\sqrt{3}V_{\mathrm{bus},d}}{\pi L_{\mathrm{dc}} C_{\mathrm{dc}} V_{\mathrm{tr}}}\left(K_{\mathrm{FB}} - \frac{1}{2\sqrt{3}}\cdot\sqrt{\frac{2}{3}}\frac{\pi L_{\mathrm{dc}} V_{\mathrm{tr}} P_{\mathrm{CPL}}}{V_{\mathrm{bus},d}}\right) \tag{5}$$

then $\dot{V}_{\mathrm{dc}}$ in (4) can be written as

$$\dot{V}_{\mathrm{dc}} = \frac{1}{C_{\mathrm{dc}}} I_{\mathrm{dc1}} + \frac{P_1}{V_{\mathrm{dc}}}. \tag{6}$$

According to (6), if $P_1 = 0$, the nonlinear term P_1/V_{dc} can be canceled. Therefore, K_{FB} in order to guarantee that $P_1 = 0$ can be defined from (5). The adaptable value of K_{FB} can then be calculated in order to stabilize the system according to

$$K_{\mathrm{FB}} = \frac{1}{2\sqrt{3}}\cdot\sqrt{\frac{2}{3}}\frac{\pi L_{\mathrm{dc}} V_{\mathrm{tr}} P_{\mathrm{CPL}}}{V_{\mathrm{bus},d}}. \tag{7}$$

The final system, with adaptive stabilization based on the loop-cancelation technique, is shown in Fig. 7. It can be seen in Fig. 7 that the loop cancelation gain K_{FB} is calculated as in (7). K_{FB} will be adapted depending on the value of the system operating point defined by P_{CPL}. From (7), the adaptable K_{FB} depends on the values of $L_{\mathrm{dc}}, V_{\mathrm{tr}}, V_{\mathrm{bus},d}$, and P_{CPL}. In the

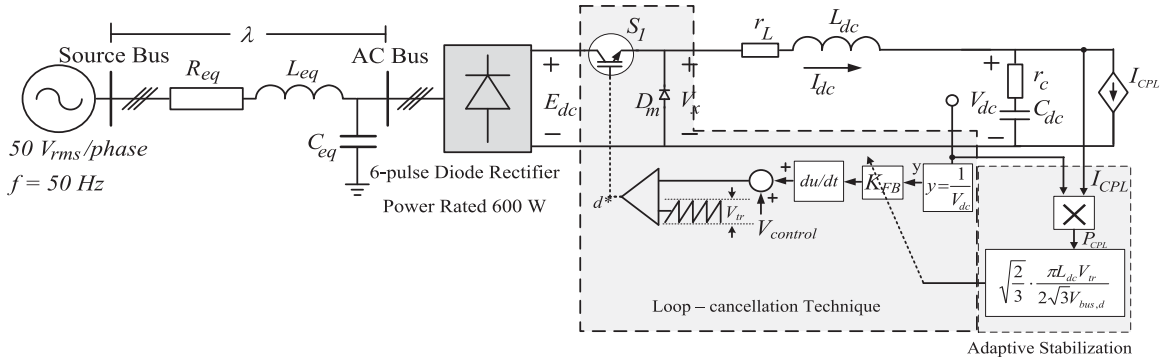

Fig. 7. System with the adaptive stabilization based on the loop-cancelation technique.

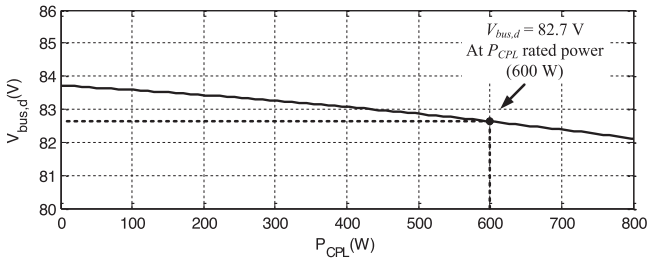

Fig. 8. $V_{\mathrm{bus},d}$ values for P_{CPL} when varied from 0 to 800 W.

example system used in this paper, $L_{\mathrm{dc}} = 37.7$ mH; however, in other systems this can be determined by the measurement or identified by artificial intelligence techniques [31]. The value of $V_{\mathrm{bus},d}$ can be determined by using the power flow equation [9] based on the ac side. The $V_{\mathrm{bus},d}$ values of the example system in Fig. 1, when the P_{CPL} is varied from 0 to 800 W (the rated power is 600 W), are shown in Fig. 8.

According to Fig. 8 at the rated power of 600 W, the value of $V_{\mathrm{bus},d}$ for the example system is 82.7 V. It can be seen from Fig. 8 that the higher the value of P_{CPL}, the lower the value of $V_{\mathrm{bus},d}$. This in turn results in a higher value of K_{FB}. Finally, P_{CPL} can be determined according to (8). The required values of I_{CPL} and V_{dc} can be obtained from current and voltage sensors, respectively

$$P_{\mathrm{CPL}} = V_{\mathrm{dc}} I_{\mathrm{CPL}}. \tag{8}$$

To ensure that condition (7) can provide the appropriate value of K_{FB}, a phase-plane analysis of the system in Fig. 7 was performed. The phase-plane plots for $P_{\mathrm{CPL}} = 400$, 500, and 600 W are shown in Fig. 9(a)–(c), respectively. It can be seen that if the P_{CPL} is increased, the value of K_{FB} is also automatically increased based on (7). It can be seen from Fig. 9(a) that the system without the proposed mitigation technique ($K_{\mathrm{FB}} = 0$) is unstable; this is represented by the blue line. However, when the mitigation is activated at $t = 0.1$ s, with $K_{\mathrm{FB}} = 0.405$, the system settles to a new stable operating point. This stabilization trajectory is represented by the green line in Fig. 9(a). Similarly, as shown in Fig. 9(b) and (c), the system with $P_{\mathrm{CPL}} = 500$ W and 600 W becomes stable with $K_{\mathrm{FB}} = 0.506$ and 0.607, respectively. These analytical results, via phase-plane analysis,

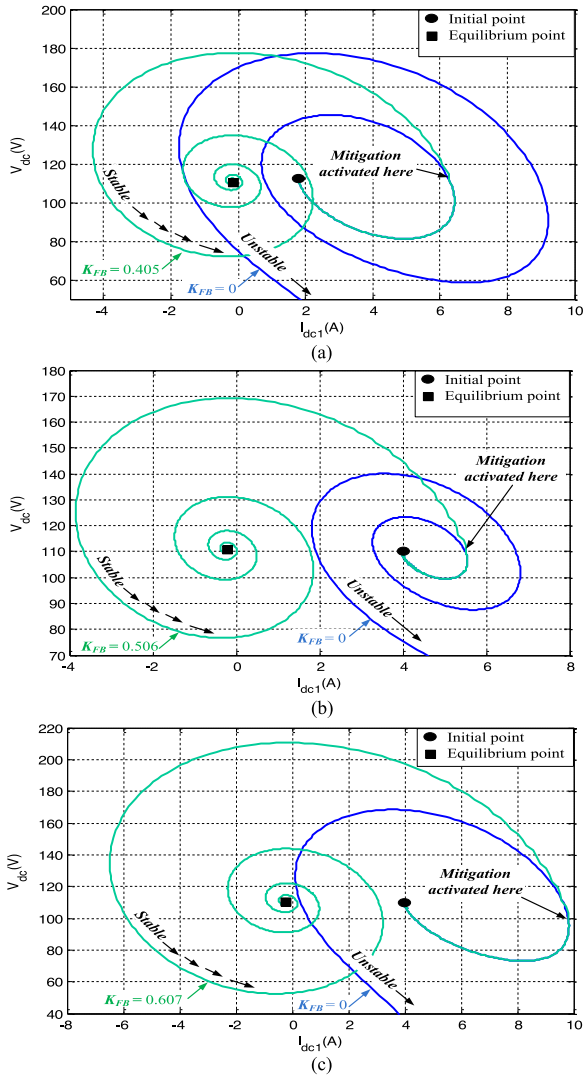

Fig. 9. Phase-plane plots of the system with the proposed adaptive stabilization. (a) $P_{\mathrm{CPL}} = 400$ W. (b) $P_{\mathrm{CPL}} = 500$ W. (c) $P_{\mathrm{CPL}} = 600$ W.

confirm that the adaptable K_{FB} calculated from (7) ensures stable operation.

Time-domain simulation results when P_{CPL} is varied from 200 W to the rated power of 600 W are depicted in Fig. 10. It

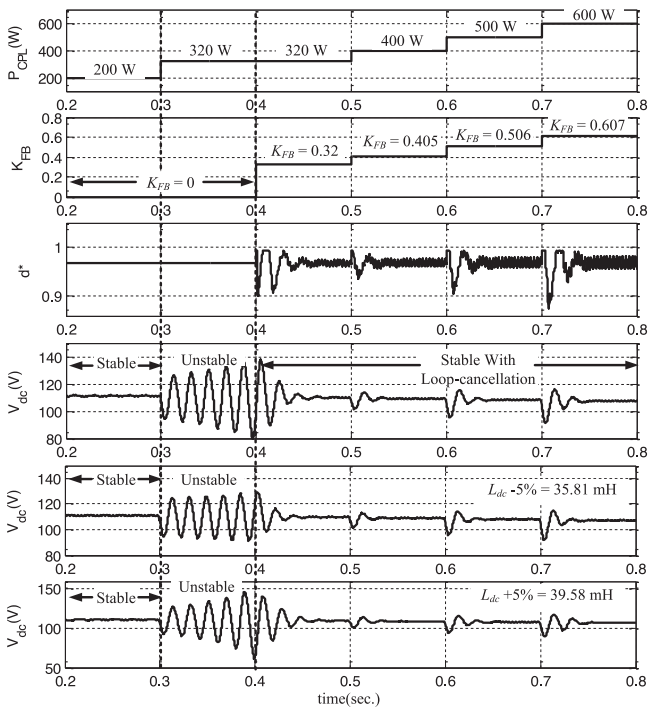

Fig. 10. Time-domain simulation results with adaptive stabilization based on the loop-cancelation technique.

can be seen from Fig. 10 that the system is initially unstable between 0.3 and 0.4 s when $K_{\rm FB} = 0$. However, once the loop-cancelation technique is activated at 0.4 s the system becomes stable and remains stable under all subsequent values of $P_{\rm CPL}$. After 0.4 s, current and voltage sensors are used to continuously monitor the value of $P_{\rm CPL}$ in order to recalculate the appropriate $K_{\rm FB}$. This can be seen in Fig. 10. The duty cycle of S_1 is also included in Fig. 10. This value cannot exceed one for practical implementation. Hence, this limitation has already been added in the simulation, as can be seen in Fig. 10. The simulation results using the same value of $K_{\rm FB}$ for $L_{\rm dc} - 5\% = 35.81$ mH and $L_{\rm dc} + 5\% = 39.58$ mH are also shown. It can be seen that even though $L_{\rm dc}$ is changed to 35.81 or 39.58 mH, the system can remain stable by using the $K_{\rm FB}$ calculated from fixed $L_{\rm dc} = 37.7$ mH. It means that the parameter robustness of the proposed control method does not affect the mitigation result.

IV. Experimental Verification

It has been established in the previous sections that the proposed ac–dc power system shown in Fig. 1 becomes unstable when $P_{\rm CPL}$ is equal to 320 W. Adaptive loop cancelation has been analytically proven to mitigate the instability, as shown in Fig. 7. The simulation results shown in Fig. 10 have also confirmed that the system is always stable with adaptable $K_{\rm FB}$. In this section, experimental verification is reported in order to support the proposed adaptive stabilization concept. The same ac–dc system is used as shown in Fig. 7. However, within the experimental rig, two parallel tightly controlled buck converters are used to represent the ideal CPL. More details on these converters can be found in [9]. In addition, as the time-domain simulation results presented in the previous section were performed with an ideal CPL, they were repeated also using two paralleled buck converters. A diagrammatic representation of the ac–dc power system examined in this section, with the proposed adaptive stabilization, is shown in Fig. 11.

The experimental rig is shown in Fig. 12. The MOSFET IRFP250N and the diode MUR1560G were added into the system to represent the S_1 and D_m, respectively. Moreover, the low-pass filter was already embedded to eliminate the noise generated from the derivative term. The bandwidth of the low-pass filter is set equal to ten times the resonance frequency [12]. In this paper, the resonance frequency is equal to 343.3 rad/s, calculated from the $L_{\rm dc}$ and $C_{\rm dc}$ values shown in Table I. The proposed adaptive stabilization, based on the loop-cancelation technique, was implemented using an Atmaga1280 microcontroller with analog circuits. This is highlighted by the number 3 in Fig. 12. As for both controlled buck converters highlighted by the number 5 and 7, a damping ratio (ζ) and a natural frequency (ω_n) for a voltage loop were set to 0.7 and $2\pi(400)$ rad/s, respectively. For a current loop, these values were equal to 0.7 and $2\pi(4000)$ rad/s. Hence, following on these damping ratios and natural frequencies, K_{pv}, K_{iv}, K_{pi}, and K_{ii} are equal to 0.05, 20, 0.6819, and 1948, respectively. In addition, the switching frequencies for switch S_1 and switches inside the controlled buck converters were equal to 10 kHz.

Both the simulation model and the experimental rig were subjected to the same test scenario. The resulting $V_{\rm dc}$ waveforms are shown in Fig. 13. The test scenario can be summarized as follows.

1) Initially, the total load power was set to 250 W; CPL1 = 250 W, CPL2 = 0 W.
2) At $t = 0.11$ s, an additional load of 24.2 W is introduced by the second converter CPL2, as a result the total CPL becomes 274.2 W. From the experimental results, it can be seen that the system response is now poorly damped indicating that the stability margin is approaching. The simulation also shows a very oscillatory response, however of a much smaller magnitude. This discrepancy can be explained by unaccounted parasitic effects and modeling assumptions. Hence, both the simulation model and the experimental setup indicate that the system is close to instability.
3) At $t = 0.43$ s, CPL2 is increased to 80 W. As predicted from the analytical analysis presented in the previous section, at a total load power of 330 W, the system becomes unstable. It can be seen from Fig. 13 that in both simulation and experimental results, the dc voltage exhibits an expanding oscillatory behavior.
4) At $t = 1.05$ s, the proposed algorithm is activated and the system stabilizes.
5) At $t = 1.15$ s, the load power is further increased (CPL total power becomes 380 W). The system maintains stable operation due to the stabilizing effect of proposed adaptive stabilization technique.
6) Finally, to confirm that the system maintains stability even with higher loads, two further CPL step increases are introduced at $t = 1.27$ s (total load power becomes 430 W)

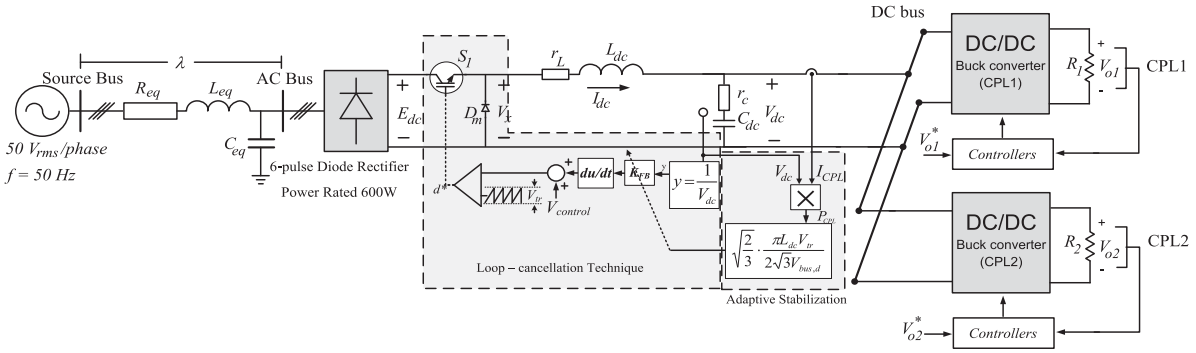

Fig. 11. AC–DC power system with the proposed adaptive stabilization feeding paralleled controlled buck converters.

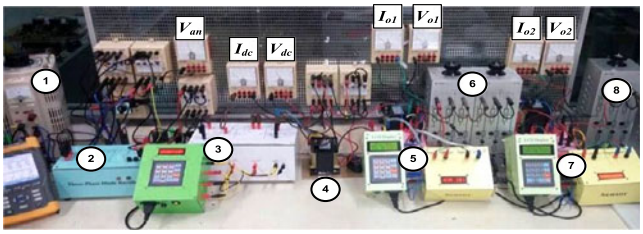

Fig. 12. Testing rig based on the system in Fig. 11.

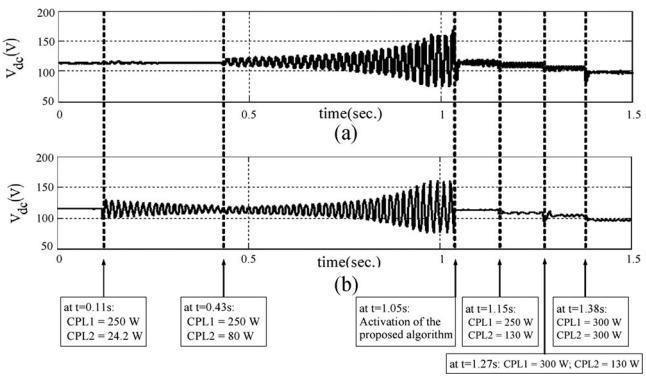

Fig. 13. (a) Simulation and (b) experimental results.

and at $t = 1.38$ s (600 W total). It is clearly seen from Fig. 13 that the dc bus voltage responses are stable and that the voltage drops at each load step according to the system's internal resistance.

Overall, it can be concluded that there is a very good match between the simulation and experiment results during the test scenario. The capability of the system to return to stable operation using the proposed technique is clearly shown. Furthermore, once the proposed mitigation has been activated, the results in Fig. 13 confirm that the system is always stable even when the total CPL is equal to 600 W (the rated power of feeder system). The experimental results confirm that the proposed adaptive stabilization algorithm, based on the loop-cancelation technique, fully mitigates the ac–dc feeder system instability caused by CPLs. In addition, Fig. 13 validates the developed system model and the assumptions made during the development of this effective technique.

V. Conclusion

In this paper, adaptive stabilization of an uncontrolled rectifier based ac–dc converter has been introduced. The proposed mitigation technique has been used to eliminate the destabilizing effect of CPLs. As a result, the ac–dc feeder system is always stable for any level of CPL. The theoretical results from the eigenvalue theorem and the phase-plane analysis confirm that the uncontrolled rectifier based ac–dc power system, with the proposed adaptive stabilization, is always stable. Moreover, simulations and experimental results have been used to verify the theoretical results. Agreement between theoretical, simulation, and experimental results has been shown. The proposed adaptive mitigation is therefore a very powerful and flexible technique, which can be used to guarantee the stable operation of uncontrolled rectifier based ac–dc feeder systems when supplying CPLs.

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Adaptive Stabilization of Uncontrolled Rectifier Based AC–DC Power Systems Feeding Constant Power Loads

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***Abstract*—It is known that, when tightly regulated, actively controlled power converters behave as constant power loads (CPLs). These loads can significantly degrade the stability of their feeder system. The loop-cancelation technique has been established as an appropriate methodology to mitigate this issue within dc–dc converters that feed CPLs. However, this has not yet been applied to uncontrolled rectifier based ac–dc converters. This paper therefore details a new methodology that allows the loop-cancelation technique to be applied to uncontrolled rectifier based ac–dc converters in order to mitigate instability when supplying CPLs. This technique could be used in both new applications and easily retrofitted into existing applications. Furthermore, the key contribution of this paper is a novel adaptive stabilization technique, which eliminates the destabilizing effect of CPLs for the studied ac–dc power system. An equation, derived from the average system model, is introduced and utilized to calculate the adaptable gain required by the loop-cancelation technique. As a result, the uncontrolled rectifier based ac–dc feeder system is always stable for any level of CPL. The effectiveness of the proposed adaptive mitigation has been verified by small-signal and large-signal stability analysis, simulation, and experimental results.**

***Index Terms*—AC–DC converters, constant power load (CPL), loop-cancelation technique, negative impedance instability.**

I. Introduction

ACTIVELY controlled power converters are widely used in many applications. Unfortunately, when tightly regulated, actively controlled power converters behave as constant power loads (CPLs) [1], [2]. These CPLs can significantly degrade the stability of their feeder system [3]–[5]. It can be seen from previous publications [6]–[10], that unstable system operation can be predicted from dynamic mathematical models via control theory. In order to derive models in such a way as to be suitable for stability analysis the averaging technique [9], [10] can be utilized. However, mathematical prediction only states when the system will become unstable. In order to eliminate the destabilizing effect, mitigation techniques are required.

In terms of mitigation techniques, there are three possible ways to apply a compensating signal for eliminating the destabilizing effect. The first is to generate the mitigating signal on the feeder side [11]–[20]. In this case, the system can be stabilized without conciliating the load performance. However, this way cannot be applied to a feeder system that utilizes an uncontrolled rectifier based ac–dc rectifier due to the absence of the control loop in the feeder subsystem. In this situation, a second mitigation technique can be used in which the compensating signal is injected into the CPL control loop to modify the load impedance for stable operation [21]–[27]. The drawback of mitigation on the CPL side is that the additional compensating signal may deteriorate the load performance. The final way to eliminate the destabilizing effect is by connecting an auxiliary circuit between the feeder and load subsystems [28]–[30]. This method is suitable for power systems having existing feeder and load subsystems that are impossible to modify. In this paper, the feeder system includes an uncontrolled rectifier in which the output voltage cannot be adjusted. Hence, the additional auxiliary circuit approach for mitigation is selected.

In terms of the control techniques to create the compensating signal, there are two well-known approaches. The first is the active damping method [11], [15]–[30]. In this case, a virtual resistance is used to increase the damping of the filter circuit. However, the power level of the CPL (P_{CPL}) that can be mitigated is limited [12], [14]. Therefore, a second approach was introduced, namely the loop-cancelation technique [12], [14]. This technique can mitigate system instability at higher values of P_{CPL} than those compensated by active damping. However, this technique has only been applied to dc–dc converters, as described in [12]. The application of the loop-cancelation technique to uncontrolled rectifier based ac–dc power systems via an auxiliary circuit has not been reported in previous publications, e.g., [12]. Hence, in this paper, instability mitigation for uncontrolled rectifier based ac–dc power systems via the loop-cancelation technique is presented. Moreover, this paper also presents a novel adaptive stabilization technique based on an equation that can be derived from the average system model. The equation is used to determine the adaptable gain required

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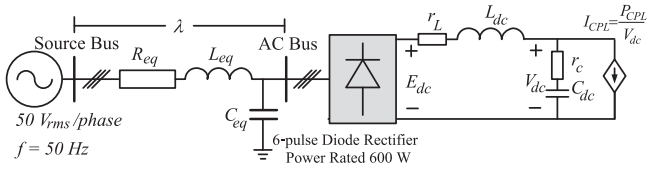

Fig. 1. AC–DC power system feeding an ideal CPL.

for loop cancelation. This gain depends on the power level of the CPL, which can be calculated from voltage and current sensors on the dc bus. As a result of this methodology, the system can automatically ensure stability under all operating conditions. The stability study presented in this paper, using small-signal and large-signal stability analysis, confirms that the mitigated system is always stable. In addition, simulation and experimental results are also presented to verify the proposed adaptive stabilization technique that eliminates the destabilizing effect of the CPL.

The paper is structured as follows. In Section II, an ac–dc power system feeding an ideal CPL is introduced to illustrate the effect of CPLs. In Section III, the loop-cancelation technique for ac–dc power systems feeding ideal CPLs is explained. An explanation of how to apply the loop-cancelation technique to the ac–dc power system, the derivation of mathematical model, the system stability analysis via the eigenvalue theorem and the phase-plane plot, the concept of the adaptive stabilization, and the simulation results are all addressed in Section III. A realistic ac–dc power system is then analyzed in Section IV. In this case, parallel controlled buck converters are used as CPLs instead of the ideal CPLs. Simulation and experimental results are also presented in Section IV to confirm that the proposed mitigation technique can eliminate the destabilizing effect of the CPL. Finally; Section V concludes and discusses the benefits of the adaptive stabilization technique for the ac–dc power system.

II. AC–DC Power System Feeding an Ideal CPL

The ac–dc power system investigated in this study is depicted in Fig. 1. An ac–dc power system including an uncontrolled rectifier is considered in this paper because it is still widely used in many applications. It consists of a balanced three-phase voltage source, a transmission line represented by R_{eq}, L_{eq}, and C_{eq}, a six-pulse diode rectifier, dc-link filters represented by r_L, $L_{\rm dc}$, r_c, and $C_{\rm dc}$, and an ideal CPL represented by a dependent current source. The parameters of the system in Fig. 1 are given in Table I. Note that the inductance value has been chosen in order for stability to occur at a power level that is able to be verified experimentally.

It is known that CPLs can degrade the stability of their feeder systems via the dc-link filter [3]–[5]. Many research works have already presented how to predict unstable operation using a mathematical model of the system. For three-phase systems with six-pulse diode rectifiers, the DQ method [6]–[8] can be applied in order to analyze the three-phase rectifier circuit and obtain a dynamic model suitable for stability study. The eigenvalue theorem [8] can then be applied to the linearized model for stability analysis. Based on the procedure in [9], the eigenvalue plot of the system shown in Fig. 1, with the parameters in Table I, is depicted in Fig. 2. It can be seen from Fig. 2 that the system will be unstable when the value of $P_{\rm CPL}$ reaches 320 W. In this paper, it will be shown that as a result of the techniques used, the ac–dc system shown in Fig. 1 can provide power exceeding 320 W, in this case up to 600 W (rated power), without instability occurring. The details of the technique used for the stabilization of the uncontrolled rectifier based ac–dc power system will be explained in Section III. Moreover, the novel adaptive stabilization for ac–dc power systems feeding the CPLs is also explained.

TABLE I
Parameters of the System in Fig. 1

Parameters	Value
V_s	50 $V_{\rm rms/phase}$
ω	$2\pi \times 50$ rad/s
R_{eq}	0.1 Ω
L_{eq}	0.21 mH
C_{eq}	2 nF
r_L	0.57 Ω
r_c	2.97 Ω
$L_{\rm dc}(\Delta I_{\rm dc} \leq 0.5$ A)	37.7 mH
$C_{\rm dc}(\Delta V_{\rm dc} \leq 5$ V)	237.35 μF

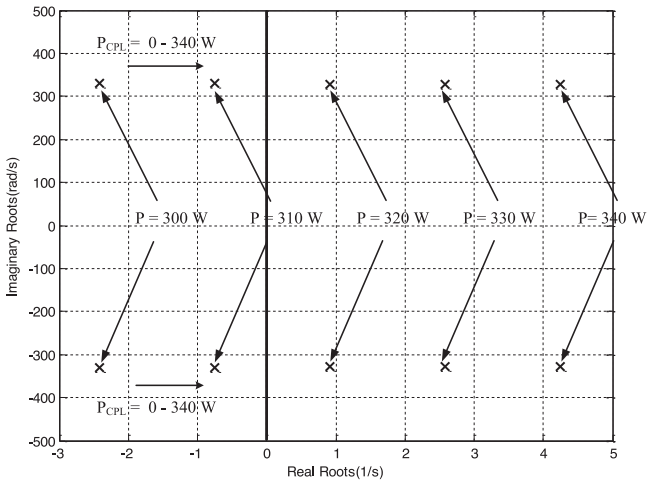

Fig. 2. Eigenvalue plot of the system before applied the proposed mitigation technique.

III. Loop-Cancelation Stabilization of an AC–DC Power System Feeding an Ideal CPL

Within this section, the new methodology for the application of the loop-cancelation technique to uncontrolled rectifier based ac–dc converters will be detailed. The established ac–dc converters will be detailed. The established ac–dc power system, on which this study is based, is shown in Fig. 1. The newly proposed ac–dc power system, including the loop-cancelation technique, is depicted in Fig. 3. An ideal CPL is considered initially in order to facilitate the calculation of the adaptable gain, as will be described later in this section.

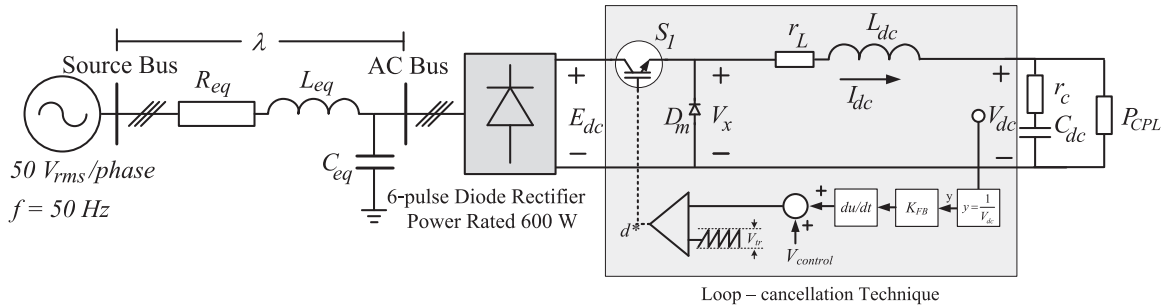

Fig. 3. AC–DC power system with the loop-cancelation technique.

Within dc–dc converters, the control of output dc voltage is a natural feature. The loop-cancelation method [12] can therefore be conveniently applied to introduce a corrective action by adjusting the converter duty cycle. In contrast, the ac–dc power system in this study employs an uncontrolled rectifier in which the output voltage cannot be adjusted and is defined by the ac voltage magnitude only. Therefore, this study proposes a new approach by introducing into the dc link a controlled switch S_1 to both control the output voltage and introduce the proposed loop-cancelation technique. Only switch S_1 and diode D_m are added into the system, whereas r_L, $L_{\rm dc}$, r_c, and $C_{\rm dc}$ are the existing dc-link filter of the rectifier circuit. Therefore, the effect of S_1 and D_m on the overall system power loss and cost is very small. The duty cycle d^* is used to control the switch S_1. d^* can be calculated using

$$d^* = \frac{1}{V_{\rm tr}}\left(V_{\rm control} + K_{\rm FB}\frac{d}{dt}\left(\frac{1}{V_{\rm dc}}\right)\right) \tag{1}$$

where $V_{\rm tr}$ is the amplitude of a triangular signal that can be set by the user. Based on the loop-cancelation technique reported in [12] for dc–dc converters, it is known that the feedback gain $K_{\rm FB}$ is a vital parameter that enables the designer to determine the characteristic of output dc-link filter damping. Moreover, if the designer can determine the appropriate value for $K_{\rm FB}$, the desired time-domain response can be obtained and the destabilizing effect can be completely eliminated.

First, for the proposed uncontrolled rectifier based ac–dc power system, the mathematical model will be derived. From this, the equation for calculating $K_{\rm FB}$ can be obtained. As detailed in previous publications [6]–[10], feeder systems with three-phase rectifiers can be analyzed using the DQ method, while the behavior of S_1 can be eliminated by using the generalized state-space averaging (GSSA) method [6]. The equivalent circuit of the system in Fig. 3, represented in the *dq*-frame, is shown in Fig. 4. After applying the DQ method, the three-phase diode rectifier can be treated as a transformer in the *dq*-frame [10]. The GSSA is then used to eliminate the switching behavior of S_1. Applying Kirchhoff's voltage law and Kirchhoff's current law to the circuit shown in Fig. 4, with d^* given by (1), the mathematical model of the proposed ac–dc power system under continuous conduction mode, using the loop-cancelation technique, is defined by the following equation:

$$\begin{cases}
\dot{I}_{ds} = -\frac{R_{eq}}{L_{eq}}I_{ds} + \omega I_{qs} - \frac{1}{L_{eq}}V_{{\rm bus},d} + \frac{1}{L_{eq}}V_{sd} \\
\dot{I}_{qs} = -\omega I_{ds} - \frac{R_{eq}}{L_{eq}}I_{qs} - \frac{1}{L_{eq}}V_{{\rm bus},q} + \frac{1}{L_{eq}}V_{sq} \\
\dot{V}_{{\rm bus},d} = \frac{1}{C_{eq}}I_{ds} + \omega V_{{\rm bus},q} \\
\qquad\qquad -\sqrt{\frac{3}{2}}\cdot\frac{2\sqrt{3}V_{\rm tr}}{\pi C_{eq}\left(V_{\rm control}+K_{\rm FB}\frac{d}{dt}\left(\frac{1}{V_{\rm dc}}\right)\right)}I_{\rm dc} \\
\dot{V}_{{\rm bus},q} = -\omega V_{{\rm bus},d} + \frac{1}{C_{eq}}I_{qs} \\
\dot{I}_{\rm dc} = \sqrt{\frac{3}{2}}\cdot\frac{2\sqrt{3}V_{\rm control}}{\pi L_{\rm dc}V_{\rm tr}}V_{{\rm bus},d} - \frac{(r_\mu+r_L+r_c)}{L_{\rm dc}}I_{\rm dc} - \frac{1}{L_{\rm dc}}V_{\rm dc} \\
\qquad + \frac{r_c P_{\rm CPL}}{L_{\rm dc}V_{\rm dc}} + \sqrt{\frac{3}{2}}\cdot\frac{2\sqrt{3}}{\pi L_{\rm dc}C_{\rm dc}}\frac{K_{\rm FB}V_{{\rm bus},d}}{V_{\rm tr}}\frac{d}{dt}\left(\frac{1}{V_{\rm dc}}\right) \\
\dot{V}_{\rm dc} = \frac{1}{C_{\rm dc}}I_{\rm dc} - \frac{P_{\rm CPL}}{C_{\rm dc}V_{\rm dc}}
\end{cases} \tag{2}$$

A new variable $I_{\rm dc1}$, as given by (3), can be used to simplify the system model

$$\dot{I}_{\rm dc1} = \dot{I}_{\rm dc} - \sqrt{\frac{3}{2}}\cdot\frac{2\sqrt{3}}{\pi L_{\rm dc}}\frac{K_{\rm FB}V_{{\rm bus},d}}{V_{\rm tr}}\frac{d}{dt}\left(\frac{1}{V_{\rm dc}}\right). \tag{3}$$

Hence, (2) can be written as the following equation:

$$\begin{cases}
\dot{I}_{ds} = -\frac{R_{eq}}{L_{eq}}I_{ds} + \omega I_{qs} - \frac{1}{L_{eq}}V_{{\rm bus},d} + \frac{1}{L_{eq}}V_{sd} \\
\dot{I}_{qs} = -\omega I_{ds} - \frac{R_{eq}}{L_{eq}}I_{qs} - \frac{1}{L_{eq}}V_{{\rm bus},q} + \frac{1}{L_{eq}}V_{sq} \\
\dot{V}_{{\rm bus},d} = \frac{1}{C_{eq}}I_{ds} + \omega V_{{\rm bus},q} - \sqrt{\frac{3}{2}}\cdot\frac{2\sqrt{3}V_{\rm tr}}{\pi C_{eq}V_{\rm control}}I_{\rm dc1} \\
\qquad + \frac{18K_{\rm FB}}{\pi^2 C_{eq}L_{\rm dc}V_{\rm control}}\frac{V_{{\rm bus},d}}{V_{\rm dc}} \\
\dot{V}_{{\rm bus},q} = -\omega V_{{\rm bus},d} + \frac{1}{C_{eq}}I_{qs} \\
\dot{I}_{\rm dc1} = \sqrt{\frac{3}{2}}\cdot\frac{2\sqrt{3}V_{\rm control}}{\pi L_{\rm dc}V_{\rm tr}}V_{{\rm bus},d} - \frac{(r_\mu+r_L+r_c)}{L_{\rm dc}}I_{\rm dc1} - \frac{1}{L_{\rm dc}}V_{\rm dc} \\
\qquad - \sqrt{\frac{3}{2}}\cdot\frac{2\sqrt{3}(r_\mu+r_L+r_c)K_{\rm FB}}{\pi L_{\rm dc}^2 V_{\rm tr}}\frac{V_{{\rm bus},d}}{V_{\rm dc}} + \frac{r_c P_{\rm CPL}}{L_{\rm dc}V_{\rm dc}} \\
\dot{V}_{\rm dc} = \frac{1}{C_{\rm dc}}I_{\rm dc1} - \frac{P_{\rm CPL}}{C_{\rm dc}V_{\rm dc}} + \sqrt{\frac{3}{2}}\cdot\frac{2\sqrt{3}}{\pi L_{\rm dc}C_{\rm dc}}\left(\frac{K_{\rm FB}}{V_{\rm dc}V_{\rm tr}}\right)V_{{\rm bus},d}
\end{cases} \tag{4}$$

It can be seen from (4) that $K_{\rm FB}$ is presented in the system model. The effect of $K_{\rm FB}$ can be assessed via a plot of the dominant eigenvalues. These eigenvalues were calculated from the linearization of (4). The system parameters for this plot are given in Table I with $V_{\rm control} = 2.9\,{\rm V}$, $V_{\rm tr} = 3\,{\rm V}$, and $P_{\rm CPL} = 320\,{\rm W}$. The dominant eigenvalue plot when gain $K_{\rm FB}$ is varied from 0 to 2.45 is shown in Fig. 5. The plot within Fig. 5 can be used to determine the best value of $K_{\rm FB}$ to avoid unstable operation with the desired time-domain response depending on

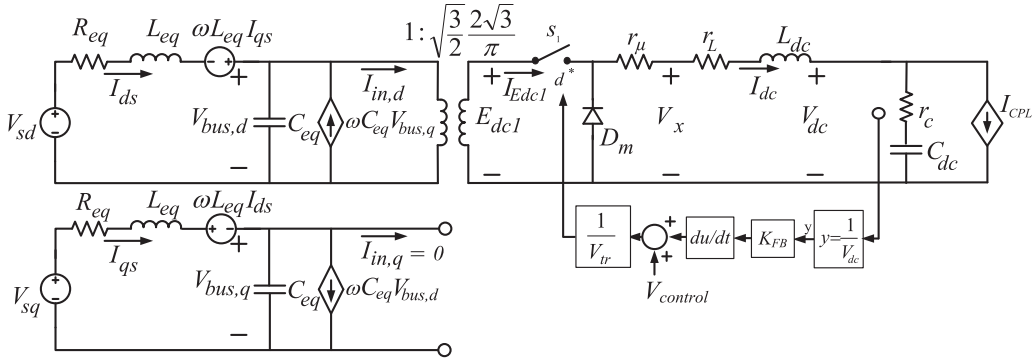

Fig. 4. Equivalent circuit of the ac–dc power system with the loop-cancelation technique in the *dq*-frame.

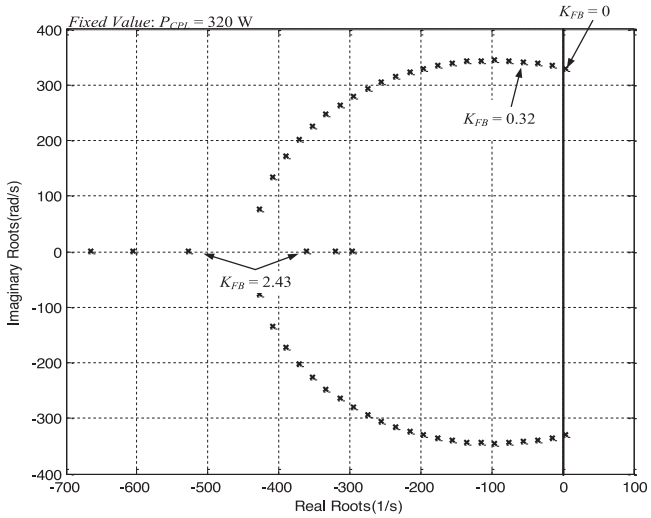

Fig. 5. Eigenvalue plot for the ac–dc power system with the loop-cancelation technique by varying $K_{\rm FB}$.

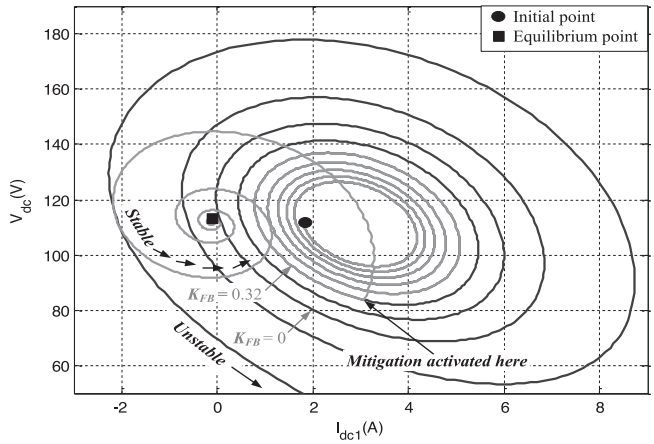

Fig. 6. Phase-plane plot of the ac–dc power system.

the location of dominant poles. However, the plot will change when $P_{\rm CPL}$ changes. Therefore, the appropriate value of $K_{\rm FB}$ to mitigate the instability problem should be adapted according to the variation of $P_{\rm CPL}$.

Large-signal stability analysis of the example system is shown in Fig. 6 via a phase-plane plot. Initially, $P_{\rm CPL}$ is set at 200 W. Subsequently, $P_{\rm CPL}$ is increased to 320 W. If $K_{\rm FB} = 0$ (without mitigation), huge oscillation occurs, as shown by the blue line in Fig. 6. Conversely, if the proposed mitigation is applied with $K_{\rm FB} = 0.32$, the system can regain stability as depicted by the green line in Fig. 6. It can be seen from Figs. 5 and 6 that there is good agreement between the eigenvalue plot and phase-plane plot. Both methodologies confirm that stability is achieved when $K_{\rm FB} = 0.32$. However, $K_{\rm FB} = 0.32$ is for $P_{\rm CPL} = 320$ W. If $P_{\rm CPL}$ is increased, $K_{\rm FB}$ should be increased to ensure that the system maintains stable operation. Hence, $K_{\rm FB}$ must be adaptable depending on the level of $P_{\rm CPL}$. In this paper, a novel equation is used to calculate the adaptable gain. The derivation of this equation is detailed as follows.

Considering only the characteristics of output dc-link filter damping, the differential equations $\dot{I}_{\rm dc1}$ and $\dot{V}_{\rm dc}$ in (4) will now be analyzed. It can be seen that the nonlinear terms of $K_{\rm FB}$ occur in both $\dot{I}_{\rm dc1}$ and $\dot{V}_{\rm dc}$. However, normally $(r_\mu + r_L + r) << L_{\rm dc}$, therefore only the nonlinear terms of $K_{\rm FB}$ within $\dot{V}_{\rm dc}$ are required. If parameter P_1 is defined as

$$P_1 = \sqrt{\frac{3}{2}}\frac{2\sqrt{3}V_{{\rm bus},d}}{\pi L_{\rm dc} C_{\rm dc} V_{\rm tr}}\left(K_{\rm FB} - \frac{1}{2\sqrt{3}}\cdot\sqrt{\frac{2}{3}}\frac{\pi L_{\rm dc} V_{\rm tr} P_{\rm CPL}}{V_{{\rm bus},d}}\right) \tag{5}$$

then $\dot{V}_{\rm dc}$ in (4) can be written as

$$\dot{V}_{\rm dc} = \frac{1}{C_{\rm dc}} I_{\rm dc1} + \frac{P_1}{V_{\rm dc}}. \tag{6}$$

According to (6), if $P_1 = 0$, the nonlinear term $P_1/V_{\rm dc}$ can be canceled. Therefore, $K_{\rm FB}$ in order to guarantee that $P_1 = 0$ can be defined from (5). The adaptable value of $K_{\rm FB}$ can then be calculated in order to stabilize the system according to

$$K_{\rm FB} = \frac{1}{2\sqrt{3}}\cdot\sqrt{\frac{2}{3}}\frac{\pi L_{\rm dc} V_{\rm tr} P_{\rm CPL}}{V_{{\rm bus},d}}. \tag{7}$$

The final system, with adaptive stabilization based on the loop-cancelation technique, is shown in Fig. 7. It can be seen in Fig. 7 that the loop cancelation gain $K_{\rm FB}$ is calculated as in (7). $K_{\rm FB}$ will be adapted depending on the value of the system operating point defined by $P_{\rm CPL}$. From (7), the adaptable $K_{\rm FB}$ depends on the values of $L_{\rm dc}, V_{\rm tr}, V_{{\rm bus},d}$, and $P_{\rm CPL}$. In the

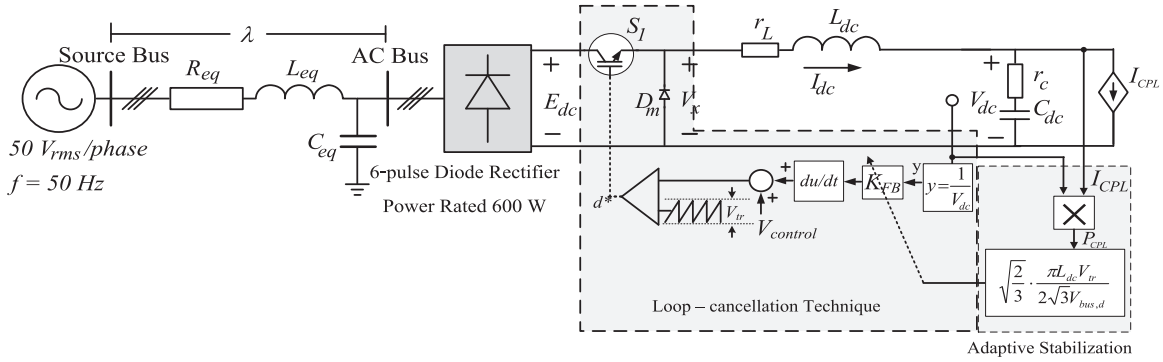

Fig. 7. System with the adaptive stabilization based on the loop-cancelation technique.

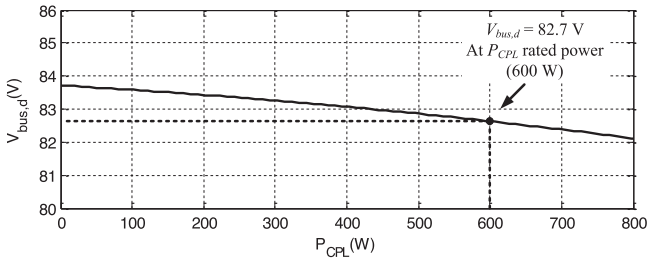

Fig. 8. $V_{\mathrm{bus},d}$ values for P_{CPL} when varied from 0 to 800 W.

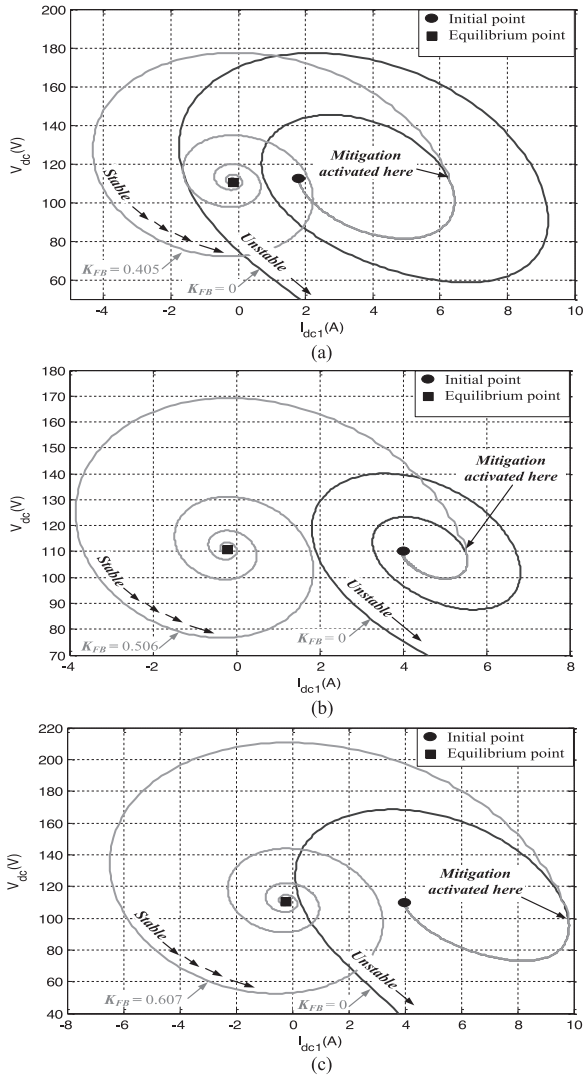

Fig. 9. Phase-plane plots of the system with the proposed adaptive stabilization. (a) $P_{\mathrm{CPL}} = 400$ W. (b) $P_{\mathrm{CPL}} = 500$ W. (c) $P_{\mathrm{CPL}} = 600$ W.

example system used in this paper, $L_{\mathrm{dc}} = 37.7$ mH; however, in other systems this can be determined by the measurement or identified by artificial intelligence techniques [31]. The value of $V_{\mathrm{bus},d}$ can be determined by using the power flow equation [9] based on the ac side. The $V_{\mathrm{bus},d}$ values of the example system in Fig. 1, when the P_{CPL} is varied from 0 to 800 W (the rated power is 600 W), are shown in Fig. 8.

According to Fig. 8 at the rated power of 600 W, the value of $V_{\mathrm{bus},d}$ for the example system is 82.7 V. It can be seen from Fig. 8 that the higher the value of P_{CPL}, the lower the value of $V_{\mathrm{bus},d}$. This in turn results in a higher value of K_{FB}. Finally, P_{CPL} can be determined according to (8). The required values of I_{CPL} and V_{dc} can be obtained from current and voltage sensors, respectively

$$P_{\mathrm{CPL}} = V_{\mathrm{dc}} I_{\mathrm{CPL}}. \tag{8}$$

To ensure that condition (7) can provide the appropriate value of K_{FB}, a phase-plane analysis of the system in Fig. 7 was performed. The phase-plane plots for $P_{\mathrm{CPL}} = 400$, 500, and 600 W are shown in Fig. 9(a)–(c), respectively. It can be seen that if the P_{CPL} is increased, the value of K_{FB} is also automatically increased based on (7). It can be seen from Fig. 9(a) that the system without the proposed mitigation technique ($K_{\mathrm{FB}} = 0$) is unstable; this is represented by the blue line. However, when the mitigation is activated at $t = 0.1$ s, with $K_{\mathrm{FB}} = 0.405$, the system settles to a new stable operating point. This stabilization trajectory is represented by the green line in Fig. 9(a). Similarly, as shown in Fig. 9(b) and (c), the system with $P_{\mathrm{CPL}} = 500$ W and 600 W becomes stable with $K_{\mathrm{FB}} = 0.506$ and 0.607, respectively. These analytical results, via phase-plane analysis, confirm that the adaptable K_{FB} calculated from (7) ensures stable operation.

Time-domain simulation results when P_{CPL} is varied from 200 W to the rated power of 600 W are depicted in Fig. 10. It

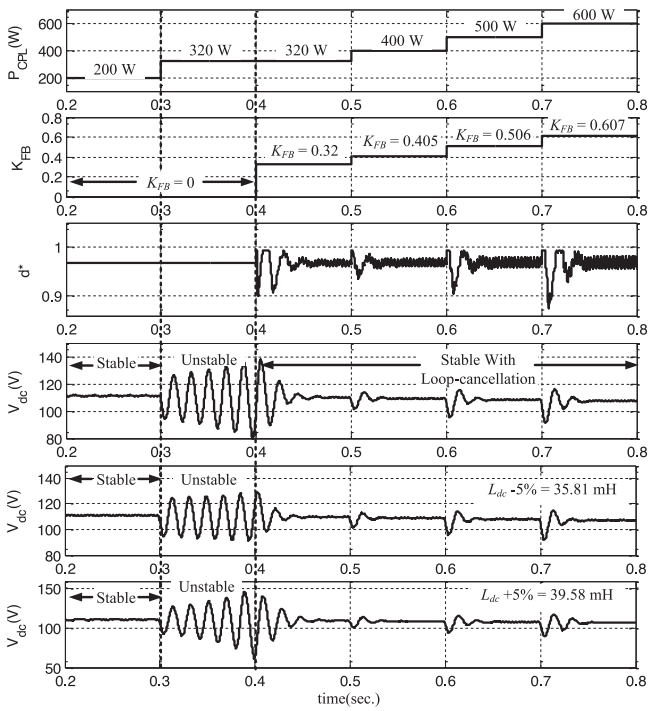

Fig. 10. Time-domain simulation results with adaptive stabilization based on the loop-cancelation technique.

can be seen from Fig. 10 that the system is initially unstable between 0.3 and 0.4 s when $K_{\rm FB} = 0$. However, once the loop-cancelation technique is activated at 0.4 s the system becomes stable and remains stable under all subsequent values of $P_{\rm CPL}$. After 0.4 s, current and voltage sensors are used to continuously monitor the value of $P_{\rm CPL}$ in order to recalculate the appropriate $K_{\rm FB}$. This can be seen in Fig. 10. The duty cycle of S_1 is also included in Fig. 10. This value cannot exceed one for practical implementation. Hence, this limitation has already been added in the simulation, as can be seen in Fig. 10. The simulation results using the same value of $K_{\rm FB}$ for $L_{\rm dc} - 5\% = 35.81$ mH and $L_{\rm dc} + 5\% = 39.58$ mH are also shown. It can be seen that even though $L_{\rm dc}$ is changed to 35.81 or 39.58 mH, the system can remain stable by using the $K_{\rm FB}$ calculated from fixed $L_{\rm dc} = 37.7$ mH. It means that the parameter robustness of the proposed control method does not affect the mitigation result.

IV. Experimental Verification

It has been established in the previous sections that the proposed ac–dc power system shown in Fig. 1 becomes unstable when $P_{\rm CPL}$ is equal to 320 W. Adaptive loop cancelation has been analytically proven to mitigate the instability, as shown in Fig. 7. The simulation results shown in Fig. 10 have also confirmed that the system is always stable with adaptable $K_{\rm FB}$. In this section, experimental verification is reported in order to support the proposed adaptive stabilization concept. The same ac–dc system is used as shown in Fig. 7. However, within the experimental rig, two parallel tightly controlled buck converters are used to represent the ideal CPL. More details on these converters can be found in [9]. In addition, as the time-domain simulation results presented in the previous section were performed with an ideal CPL, they were repeated also using two paralleled buck converters. A diagrammatic representation of the ac–dc power system examined in this section, with the proposed adaptive stabilization, is shown in Fig. 11.

The experimental rig is shown in Fig. 12. The MOSFET IRFP250N and the diode MUR1560G were added into the system to represent the S_1 and D_m, respectively. Moreover, the low-pass filter was already embedded to eliminate the noise generated from the derivative term. The bandwidth of the low-pass filter is set equal to ten times the resonance frequency [12]. In this paper, the resonance frequency is equal to 343.3 rad/s, calculated from the $L_{\rm dc}$ and $C_{\rm dc}$ values shown in Table I. The proposed adaptive stabilization, based on the loop-cancelation technique, was implemented using an Atmaga1280 microcontroller with analog circuits. This is highlighted by the number 3 in Fig. 12. As for both controlled buck converters highlighted by the number 5 and 7, a damping ratio (ζ) and a natural frequency (ω_n) for a voltage loop were set to 0.7 and $2\pi(400)$ rad/s, respectively. For a current loop, these values were equal to 0.7 and $2\pi(4000)$ rad/s. Hence, following on these damping ratios and natural frequencies, K_{pv}, K_{iv}, K_{pi}, and K_{ii} are equal to 0.05, 20, 0.6819, and 1948, respectively. In addition, the switching frequencies for switch S_1 and switches inside the controlled buck converters were equal to 10 kHz.

Both the simulation model and the experimental rig were subjected to the same test scenario. The resulting $V_{\rm dc}$ waveforms are shown in Fig. 13. The test scenario can be summarized as follows.

1) Initially, the total load power was set to 250 W; CPL1 = 250 W, CPL2 = 0 W.
2) At $t = 0.11$ s, an additional load of 24.2 W is introduced by the second converter CPL2, as a result the total CPL becomes 274.2 W. From the experimental results, it can be seen that the system response is now poorly damped indicating that the stability margin is approaching. The simulation also shows a very oscillatory response, however of a much smaller magnitude. This discrepancy can be explained by unaccounted parasitic effects and modeling assumptions. Hence, both the simulation model and the experimental setup indicate that the system is close to instability.
3) At $t = 0.43$ s, CPL2 is increased to 80 W. As predicted from the analytical analysis presented in the previous section, at a total load power of 330 W, the system becomes unstable. It can be seen from Fig. 13 that in both simulation and experimental results, the dc voltage exhibits an expanding oscillatory behavior.
4) At $t = 1.05$ s, the proposed algorithm is activated and the system stabilizes.
5) At $t = 1.15$ s, the load power is further increased (CPL total power becomes 380 W). The system maintains stable operation due to the stabilizing effect of proposed adaptive stabilization technique.
6) Finally, to confirm that the system maintains stability even with higher loads, two further CPL step increases are introduced at $t = 1.27$ s (total load power becomes 430 W)

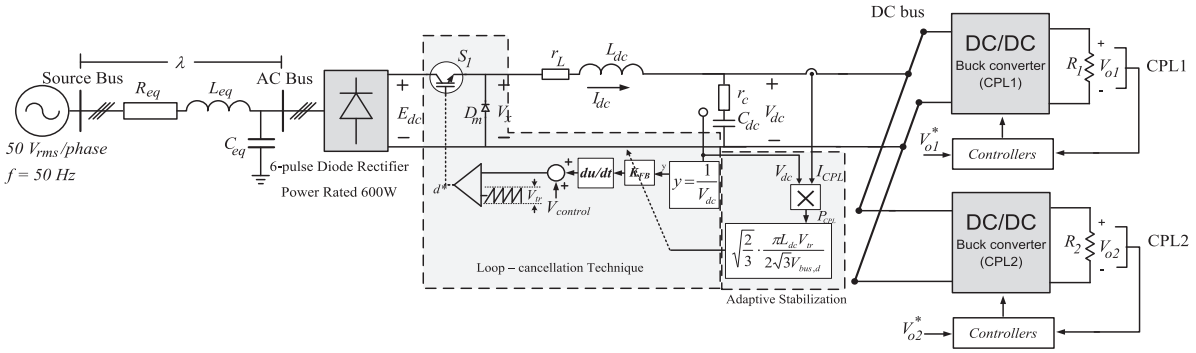

Fig. 11. AC–DC power system with the proposed adaptive stabilization feeding paralleled controlled buck converters.

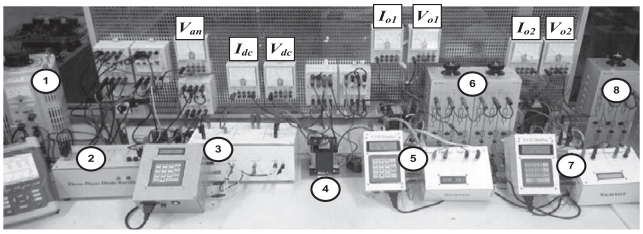

Fig. 12. Testing rig based on the system in Fig. 11.

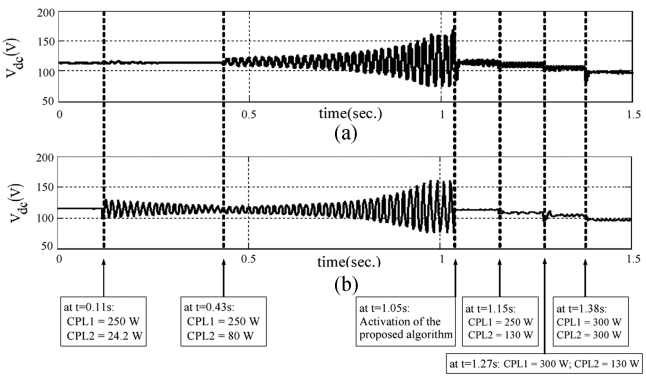

Fig. 13. (a) Simulation and (b) experimental results.

and at $t = 1.38$ s (600 W total). It is clearly seen from Fig. 13 that the dc bus voltage responses are stable and that the voltage drops at each load step according to the system's internal resistance.

Overall, it can be concluded that there is a very good match between the simulation and experiment results during the test scenario. The capability of the system to return to stable operation using the proposed technique is clearly shown. Furthermore, once the proposed mitigation has been activated, the results in Fig. 13 confirm that the system is always stable even when the total CPL is equal to 600 W (the rated power of feeder system). The experimental results confirm that the proposed adaptive stabilization algorithm, based on the loop-cancelation technique, fully mitigates the ac–dc feeder system instability caused by CPLs. In addition, Fig. 13 validates the developed system model and the assumptions made during the development of this effective technique.

V. Conclusion

In this paper, adaptive stabilization of an uncontrolled rectifier based ac–dc converter has been introduced. The proposed mitigation technique has been used to eliminate the destabilizing effect of CPLs. As a result, the ac–dc feeder system is always stable for any level of CPL. The theoretical results from the eigenvalue theorem and the phase-plane analysis confirm that the uncontrolled rectifier based ac–dc power system, with the proposed adaptive stabilization, is always stable. Moreover, simulations and experimental results have been used to verify the theoretical results. Agreement between theoretical, simulation, and experimental results has been shown. The proposed adaptive mitigation is therefore a very powerful and flexible technique, which can be used to guarantee the stable operation of uncontrolled rectifier based ac–dc feeder systems when supplying CPLs.

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