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# New Efficient Sub-module for Modular Multilevel Converter in Multi-terminal HVDC Networks

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**Abstract**— In high-voltage applications, the magnitude of total semiconductor losses (on-state and switching) determines the viability of modular type multilevel converters. Therefore, this paper presents a new cell arrangement that aims to lower total semiconductor loss of the modular multilevel converter (MMC) to less than that of the half-bridge modular multilevel converter (HB-MMC). Additional attributes of the proposed cell are: it eliminates the protective thyristors used in conventional half-bridge cells that deviate part of the dc fault current away from the anti-parallel diode of the main switch when the converter is blocked during a dc short circuit fault; and it can facilitate continued operation of the MMC during cell failures without the need for a mechanical bypass switch. Thus; the MMC that uses the proposed cell retains all advantages of the HB-MMC such as full modularity of the power circuit and internal fault management. The claimed attributes of the proposed cell are verified using illustrative simulations and reduced scale experimentations. Additionally, this paper provides brief and critical discussions that highlight the attributes and limitations of popular MMC control methods and different MMC cells structures proposed in the literature, considering the power electronic system perspective.

**Keywords**—flying capacitor cell; half and full bridge modular multilevel converter; mixed-cell commutation cells; and voltage source converter high-voltage direct current transmission systems;

## I. INTRODUCTION

Rapid developments of voltage source converter high-voltage direct current (VSC-HVDC) transmission systems in recent years have attracted significant research interest in high-voltage high-power converters, dc switchgear and dc protection systems[1, 2]. At present, half-bridge modular multilevel converters (HB-MMC) and optimized full-bridge modular multilevel (OFB-MMC) converters are the preferred choice for industry when designing VSC-HVDC transmission systems with power rating up to 1000MW per converter[3-7]. The reasons are: their modularity permits easy incorporation of redundant cells into each arm to facilitate continued operation should a (limited) number of cell capacitors and switching devices fail; offer the best trade-off between semiconductor loss and performance; and seamless current commutation between converter arms, unlike many of the hybrid converter topologies discussed in [8-11].

Figure 1 summarises some of the cell arrangements being used, or proposed for use, in modular and hybrid multilevel converters. These cells could be categorised into unipolar cells with two-level or three-level output voltage ( $V_c$  and 0, and  $2V_c$ ,  $V_c$  and 0 respectively); asymmetrical bipolar cell with four-level output voltage ( $2V_c$ ,  $V_c$ , 0 and  $-V_c$ ) and symmetrical bipolar cells with three-level and five-level output voltage ( $V_c$ , 0 and  $-V_c$ , and  $2V_c$ ,  $V_c$ , 0,  $-V_c$  and  $-2V_c$  respectively), assuming that all cell capacitors are well balanced  $V_{c1}=V_{c2}=V_c$ . Unipolar cells such as in Figure 1 (a), (c), (d) and (e) limit the number of semiconductor switches in the conduction path to one or two per cell, and this makes these cells attractive from semiconductor loss point of view. However, the use of unipolar cells limit the operating range of modular converters to unipolar dc link voltages, with the output phase voltage and voltages developed across the upper and lower arms restricted within the envelope defined by  $+1/2V_{dc0}$  and  $-1/2V_{dc0}$ , and  $V_{dc0}$  and 0 respectively, where,  $V_{dc0}$  represents the nominal dc link voltage, see Figure 2 (a) and (b). These restrictions make MMCs that employ unipolar cells unable to deal with dc faults because their upper and lower arms are unable to produce voltages with opposite polarities to counter or balance the reduced input dc link voltage as it collapses during dc faults. Recently, there are several attempts to further lower MMC switching loss by adopting three-level unipolar cells such as flying capacitor (FC), T-type and active neutral-point clamped (ANPC) cells[1, 12]. These three-level cells also reduce the number of dc-dc converters required to supply the IGBTs' gate-drives by 50%; thus, leading to overall reduction in the cost and weight of the MMC control circuit. However, the use of FC cells in MMC is not attractive because it compromises the modularity of the power circuit and reliability (each cell contains two floating capacitors with different rated voltages). T-type and ANPC cells require

complex capacitor voltage balancing and suffer from high capacitor voltage ripple due to the lack of redundant switch states that can be used to balance the cell capacitor voltages at the cell level (each voltage level can be generated by only one state, and upper capacitor of the cell in Figure 1 (c) and (d) cannot be selected or inserted into the power path unless the lower capacitor is already inserted into power path).

Each asymmetric bipolar cell in Figure 1 (f) and (g) inserts three semiconductor switches in the conduction path per cell during normal operation, and can exploit the negative voltage level it generates to allow MMC upper and lower arm voltages to be varied between  $V_{dc0}$  and 0 during normal operation, and  $\frac{1}{2}V_{dc0}$  and  $-\frac{1}{2}V_{dc0}$  during operation with zero dc link voltage, see Figure 2 (a) and (c). Such operation permits MMC cell capacitor voltages to be regulated independent of the dc link voltage ( $V_{dc}$ ), and enables MMC upper and lower arms to generate bipolar voltages that can be used to counter the dc link voltage ( $V_{dc}$ ) as it varies between 0 and  $V_{dc0}$  (including during dc short circuit fault). As a result, the MMCs that employ the asymmetrical cells in Figure 1 (f) and (g) are able to deal with dc faults better than those using unipolar cells, while retaining full control over the active and reactive power they exchange with the ac grid [4, 5, 13]. Among the asymmetrical bipolar cells, the hybrid cell in Figure 1 (f) is attractive and has sufficient redundant switch states that allow the cell capacitor voltage of the MMC to be balanced at local or global levels, and does not lead to a significant compromise of the power circuit modularity nor its internal fault management (which is necessary for continued operation when limited number of cells fail).

Figure 1 (b) and (i) show symmetrical bipolar cells that insert two and four semiconductor switches in conduction path during normal operation, and generate three and five voltage levels ( $V_c, 0$  and  $-V_c$ ) and ( $2V_c, V_c, 0, -V_c$  and  $-2V_c$ ) respectively. These symmetrical bipolar cells permit the voltages across MMC upper and lower arms to be modulated between  $V_{dc0}$  and 0, 0 and  $-V_{dc0}$  during normal operation with rated positive and negative dc link voltage, and between  $\frac{1}{2}V_{dc0}$  and  $-\frac{1}{2}V_{dc0}$  during operation with 0 dc link voltage, see Figure 2 (a) and (d). Such operational flexibility allows MMCs that employ symmetrical bipolar cells to generate peak output phase voltage  $V_m > \frac{1}{2}m_{max}V_{dc0}$  (over-modulation), without reappearance of the low-order harmonics in the baseband as in traditional voltage source converters; where,  $m_{max}$  represents the maximum modulation index. The aforesaid attributes allow MMCs that use symmetrical bipolar cells to have the largest control range (see Figure 2 (d)), tolerance to dc faults, and bipolar dc link voltage operation. But these attributes are achieved at the expense of increased semiconductor losses compared to their counterparts that employ unipolar and asymmetrical bipolar cells [5, 13, 14].

Figure 1(h) shows an example of three-level unipolar cell that offers a dc fault reverse blocking capability, while it remains subject to many of the aforesaid limitation of the unipolar cells such as operation with the unipolar dc link voltage. Additionally, it has higher semiconductor losses compared to its counterparts in Figure 1(c), (d) and (e) because it inserts three semiconductor switches into conduction path compared to two in flying capacitor and T-type cells.

The authors in [15] proposed a new type of symmetrical bipolar cell that can generate seven voltage levels to be used in modular ac/ac and dc/ac converters. The modular converter that uses the proposed cell can generate more voltage levels per phase using reduced number of switching devices compared to full-bridge MMCs; thus, the proposed cell is expected to be attractive for applications that demand high quality output voltage and current waveforms. Additionally, the operating envelope of the MMC that uses the proposed cell is expected to be similar to that of the full-bridge MMC, including operation with positive and negative dc link voltage and dc fault reverse blocking. The proposed cell inserts two fewer IGBTs in the conduction path compared to the equivalent full-bridge cells; hence, its semiconductor losses is expected to be lower than the full-bridge cell. The main limitations of the proposed cell is lack of modularity as the rated voltage of the upper capacitor is three times that of the lower capacitor, and rated voltage of the middle switch devices is twice that of the upper and lower switches.

In recent years, several methods have emerged that can be used to control modular multilevel converters, with some methods offer maximum control range and flexibility [12, 16, 17]. Some of the popular methods to control half-bridge modular converter is the standard decoupled current controller in synchronous reference frame that rotates at fundamental frequency ( $\omega$ ), with a dedicated supplementary controller for suppression of the 2<sup>nd</sup> order harmonic current in the phase variables or the synchronous reference frame at twice the fundamental frequency[7, 13, 18-20]. In this control method, the controller that suppresses the 2<sup>nd</sup> order harmonic current in each MMC phase leg injects the necessary harmonics into modulation functions of the upper and lower

arms in order to suppress the parasitic component of the common-mode current (both ac and dc components of modulation functions are modified). Although this control approach is relatively slow and cell capacitor voltages are highly coupled to dc link voltage, its ability to suppress 2<sup>nd</sup> order harmonic current in converter arms to virtually zero makes it well suited for HVDC applications, where converter semiconductor losses (on-state and switching) are paramount.

An improved version of the method discussed in [7, 13, 18-20], which includes two additional cascaded control loops that regulate the average cell capacitor voltage per phase leg and common-mode current[21-23]. This control method could be used with MMCs that employ half or full-bridge cells and other symmetrical and asymmetrical bipolar cells in Figure 1 in order to decouple the control of cell capacitor voltages from the dc link voltage. In this manner, active and reactive powers could be controlled independent of the dc link voltage in asymmetrical and symmetrical bipolar cells, and over a limited range in unipolar cells such as the half-bridge cell. The main shortcoming of this control method when it is used with half-bridge and other unipolar cells is that the MMC arms experience relatively high currents during reduced dc link voltage operation, should the cell capacitor voltages to be controlled independent of the dc link voltage (fixed at nominal dc link voltage  $V_{dc0}$ ).

The authors in [24-31] presented several control methods for half and full-bridge modular converters that employ phase-shifted carriers pulse width modulation. The refined version of this control method is presented in [26], which includes a number of dedicated controllers for common-mode voltage per phase (average capacitor voltage per phase leg), upper and lower arm voltage balancing and individual cell capacitor voltage balancing (these controllers ensure vertical balancing); and controller that ensures the dc link current is evenly distributed between the phase leg (the average common-mode current in each phase leg must be equal to one third of the dc link current, and this controller is for ensuring horizontal balancing). Additionally, basic converter controllers such as dc link voltage and active and reactive powers could be included. The main attributes of this control approach are: fixed switching frequency per device, independent of operating condition (this makes thermal management and heatsink design simpler); and no need for time consuming capacitor voltage sorting (which is extremely useful should MMC adopted in dc transformers, with relatively high fundamental frequency). But increased reliance on the control system at the modulation level may raise concern regarding the reliability of this control method; especially, during operation in harsh power system environments.

Several methods for controlling MMCs using energy manipulation have been proposed in [16, 32-34]. For example, the method presented in [16] uses the zero sequence (dc) and negative sequence (2<sup>nd</sup> order harmonic current) component of the common-mode current of each phase leg to regulate the total energy stored per converter to be constant and to suppress the cell capacitor energy fluctuations to virtually zero in an attempt to drastically reduce capacitor voltage ripple. Whilst the positive sequence of the common-mode current at fundamental frequency is used to ensure energy balance between the upper and lower arms of each phase leg. Although this approach is interesting, the choice of capacitor voltage ripple instead of the suppression of the 2<sup>nd</sup> order harmonic currents in MMC arms is not appropriate for HVDC applications, where the semiconductor losses supersede the capacitor voltage ripple; especially, as all the above control methods are able to keep the capacitor voltage ripples well within the tolerable limits. Additionally, the use of arm energy balancing in the practical MMC (where the cell capacitances may have large tolerances) may lead to substantial voltage difference between upper and lower arms of the same phase leg; thus, leading to appearance of even harmonic voltages and currents in the baseband.

This paper presents a new cell arrangement that can reduce MMC semiconductor losses beyond that of the HB-MMC; eliminate the need for the protective thyristor used in HB-MMC to deviate part of the fault current from the freewheeling diodes of the main switches which bypass the cell capacitors when the converter is blocked during dc fault; and facilitate continued operation of the MMC during internal cell failure, without the need for mechanical bypass switches. The viability of the proposed cell is demonstrated using simulations and experimentations. In these demonstrations, a switching model of the MMC with 16 cells and 32 capacitors per arm is used to illustrate device (modulation, capacitor voltage balancing and semiconductor losses) and system aspects (pole-to-pole dc short circuit, unbalanced operation and internal fault management), and two prototypes of the single-phase MMC with HB and proposed cells for loss and performance comparison. It has been shown that the proposed MMC is

promising as it has lower semiconductor loss compared to HB-MMC, and its unique cell structure enables dc short circuit survival over an extended period, without the need for protective thyristor as in the HB-MMC.

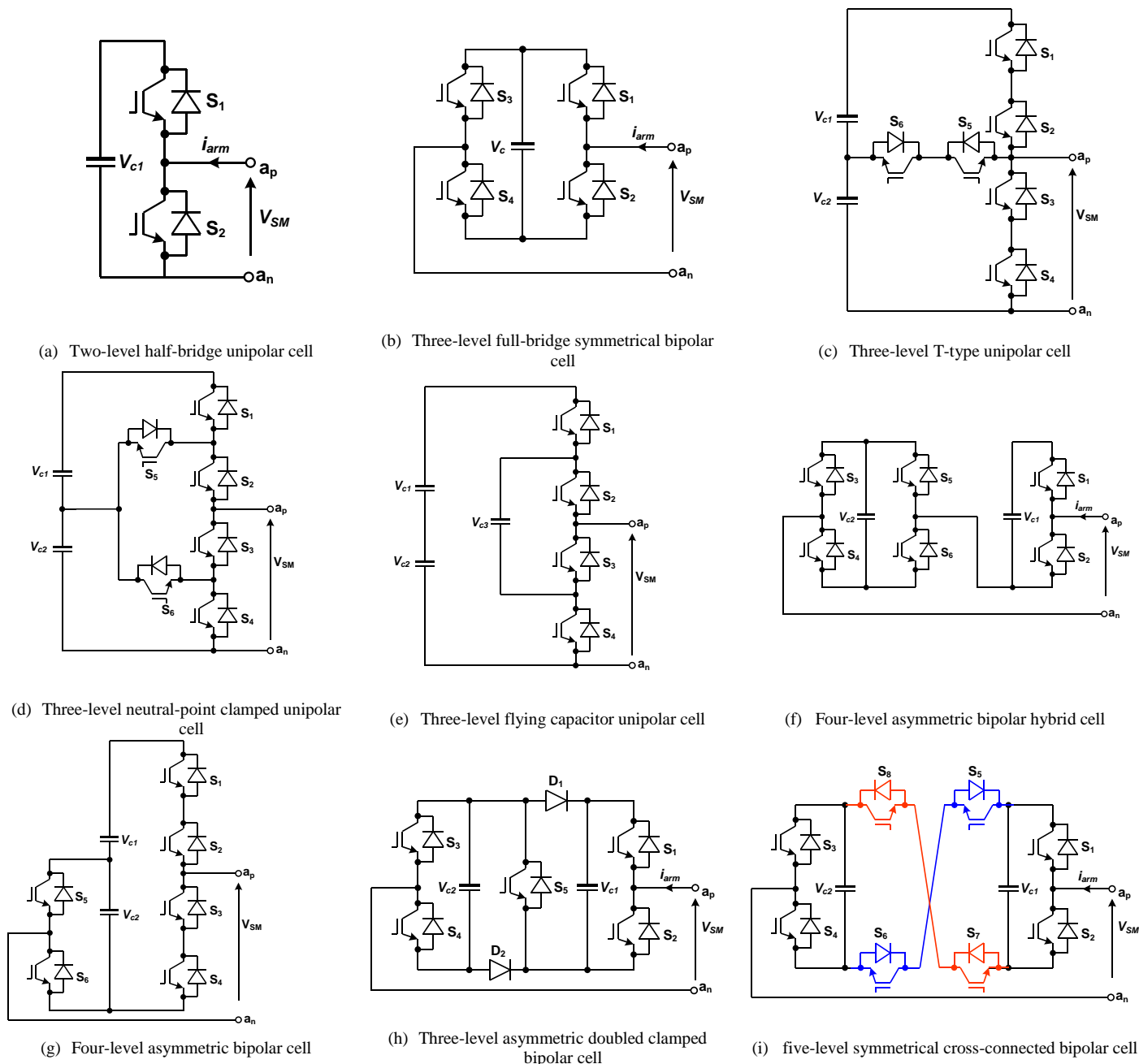
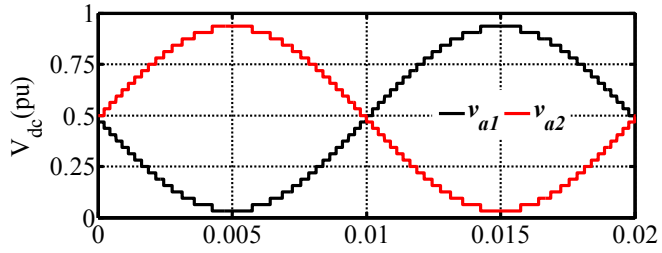
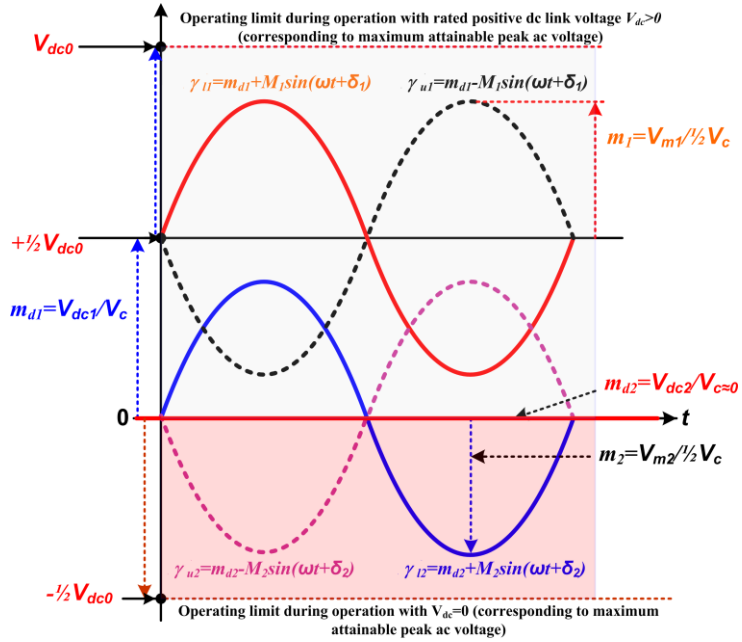


Figure 1: Some of the known cell configurations for modular and hybrid multilevel converters' submodules

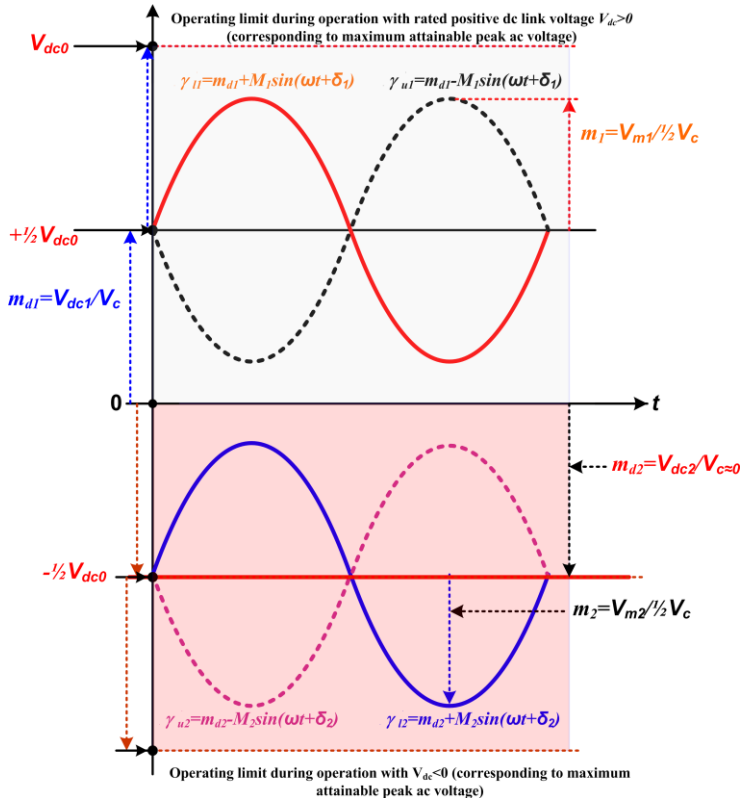


b) Operational limits of MMCs that employ unipolar cells such as in Figure 1 (a), (c), (d) and (e)



c) Operational limits of MMCs that employ asymmetric bipolar cells such as in Figure 1 (f), (g) and

(h)



d) Operational limits of MMCs that employ symmetric bipolar cells such as in Figure 1 (b) and (i), including possibility of over-modulation

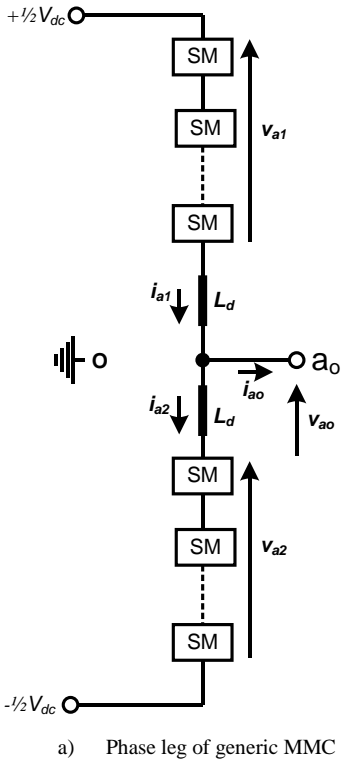


Figure 2: Illustration of different operating limits of MMCs that employ unipolar, and symmetrical and asymmetrical bipolar cells (vertical axis is normalized by  $\frac{1}{2}V_{dc}$ )

## II. THE PROPOSED MODULAR MULTILEVEL CONVERTER

Figure 3 presents two types of cells that can be used in MMCs to reduce the number of isolated dc/dc converters required to supply the driving circuits of the semiconductor switches. Figure 3(a) shows a basic cell arrangement which is formed by back-to-back connection of two versions of the HB cells and it can generate three voltage levels between ‘ $a+$ ’ and ‘ $a-$ ’,  $V_{sm}=‘0’$ , ‘ $V_c$ ’ and ‘ $2V_c$ ’ should both cell capacitor voltages  $V_{c1}$  and  $V_{c2}$  be regulated at  $V_c$ . In this cell arrangement, the voltage level ‘ $V_c$ ’ represents the redundant switch state that can be generated by two switch combinations, and can be used in conjunction with the arm current polarity to balance the cell capacitor voltages globally or locally at the cell level. This approach can be extended to the MMC with hundreds of cells per arm, where ‘ $n$ ’ cells in each MMC arm could be divided into ‘ $m$ ’ subgroups, with each subgroup consists of ‘ $r$ ’ cells and capable of generating ‘ $r+1$ ’ voltage levels; and  $\{n, m, r\} \in \mathbb{N}$  and  $n = m \times r$ .

Apart from the aforesaid attributes, an MMC that uses the cells in Figure 3(a) has the same number of cell capacitors, switching devices in conduction path and loss distribution as in conventional HB cells in Figure 3(c), including the efficiency. Figure 3(b) presents an alternative sub-module arrangement that inherits all the attributes of the cell arrangement in Figure 3(a), and offers new set of features such as reduced semiconductors losses and improved utilization of semiconductor switches. Table 1 summarises the switch states of the sub-modules in Figure 3(b). Voltage level ‘ $V_c$ ’ offers redundant switch states that can be exploited to balance capacitors  $C_1$  and  $C_2$  within each sub-module at the cell level, without increasing capacitor voltage ripple. Notice that a zero voltage level, which is used to bypass the cell capacitors  $C_1$  and  $C_2$  could be achieved by turning on switches  $S_2$ ,  $S_3$ ,  $S_5$  and  $S_6$  simultaneously. This leads to distribution of the arm current ‘ $i_a$ ’ between two parallel paths,  $S_2S_3$  and  $S_5S_6$ , each carries half of the arm current ( $\frac{1}{2}i_a$ ); thus, leading to reduced conduction loss per cell compared to conventional HB cell. Additionally, the protective thyristor ‘T’ being used to deviate part of the dc fault current from the freewheeling diodes of the switches  $S_2$  and  $S_3$  in conventional HB cell in Figure 3(c) or in the cell arrangement in Figure 3(a) are no longer required, because the freewheeling diodes of switches  $S_2S_3$  and  $S_5S_6$  will be sufficient to handle dc fault current over extended period of time. Also, the mechanical bypass switch in each HB cell in Figure 3(c) could be eliminated as the semiconductor switches  $S_2$  and  $S_3$  could be used to bypass the damaged cell.

When the cell arrangement in Figure 3(b) is used in a generic MMC in Figure 3(d), its modulation and control remain the same as in HB-MMC case. Therefore for phase ‘ $a$ ’, the upper and lower arm modulation functions are:  $\gamma_{a1} = \frac{1}{2}[\alpha_a - m_a \sin(\omega t + \delta)]$  and  $\gamma_{a2} = \frac{1}{2}[\alpha_a + m_a \sin(\omega t + \delta)]$ , where, dc modulation index  $\alpha_a = V_{dc} / \bar{V}_c \approx 1$  during normal operation; ac modulation index  $m_a = V_m / \frac{1}{2}\bar{V}_c$  ( $V_m$  and  $V_{dc}$  are peak phase and pole-to-pole dc voltages); and  $\bar{V}_c$  represents the average voltage across cell capacitors of each arm.

Amplitude modulation and cell capacitor voltage balancing of the MMC that uses the submodule in Figure 3(b) can be performed using one of the following methods:

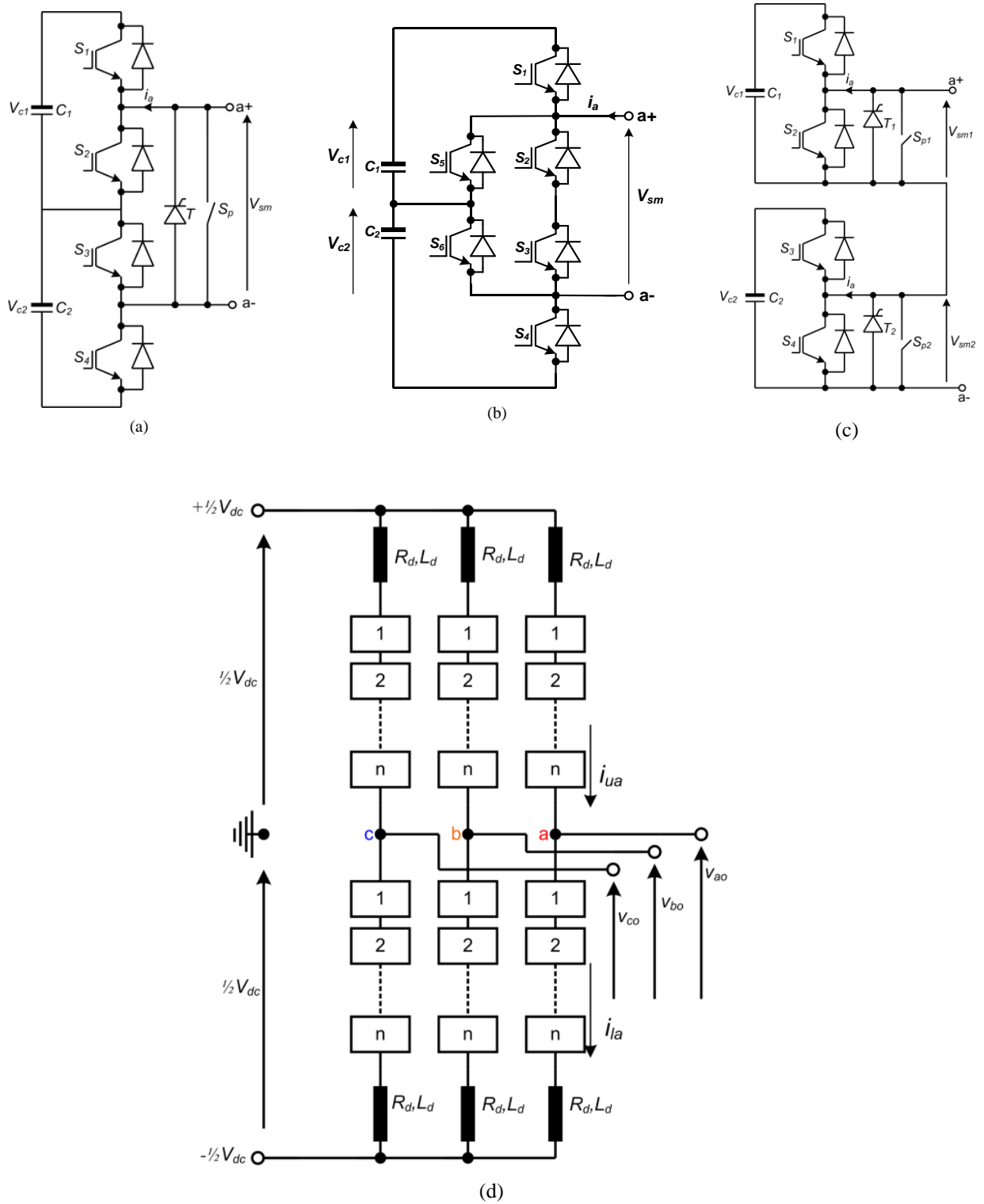


Figure 3: (a) and (b) represent types 1 and 2 cell arrangements for modular multilevel converter in (d), and (c) represents conventional half-bridge cell connection

Table 1: Summary of switch states of the sub-module arrangement in Figure 3(b); switches S1 to S6 represent composite switching devices that comprise of IGBT plus anti-parallel diodes and  $\rightarrow, \uparrow$  and  $\downarrow$  stand for states of charge of the cell capacitors (unchanged, charge and discharge) for different arm current polarity

Voltage levels	Switching states		current polarity	Impact on capacitors
	ON	OFF		
0	$S_2, S_3, S_5, S_6$	$S_1$ and $S_4$	$i_a > 0$	$C_1 \rightarrow C_2 \rightarrow$
			$i_a < 0$	
$V_c$	$S_4, S_5$	$S_1, S_2, S_3, S_6$	$i_a > 0$	$C_1 \rightarrow C_2 \uparrow$
			$i_a < 0$	$C_1 \rightarrow C_2 \downarrow$
	$S_1, S_6$	$S_2, S_3, S_4, S_5$	$i_a > 0$	$C_1 \uparrow C_2 \rightarrow$
			$i_a < 0$	$C_1 \downarrow C_2 \rightarrow$
$2V_c$	$S_1, S_4$	$S_2, S_3, S_5, S_6$	$i_a > 0$	$C_1 \uparrow C_2 \uparrow$



			$i_a < 0$	$C_1 \downarrow C_2 \downarrow$
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A) **Method I:** this method is summarised as follows:

- 1) All cell capacitor voltages are indexed as  $V_{cij}$ , where ‘ $i$ ’ identifies the location of individual cell in each arm ( $i \in \mathbb{N}$  and it varies from 1 to  $n$ ); and ‘ $j$ ’ points to the location of individual capacitor within each submodule ( $j \in \mathbb{N}$  and it varies from 1 to 2).
- 2) Marquardt’s capacitor voltage balancing method that sorts the capacitor voltages of each arm in ascending or descending order could be applied to select the number of cell capacitors to be switched in and out the power path, taking into account the voltage level to be synthesized in each sampling period, cell capacitor voltage magnitudes and arm current polarities. Insertion functions that determine the number of submodules to be inserted and bypassed from the upper and lower arms for phase ‘ $a$ ’ are:  $n_{ui} = n \times \gamma_{a1}$  and  $n_{ub} = n - n_{ui}$ , and  $n_{ii} = n \times \gamma_{a2}$  and  $n_{ib} = n - n_{ii}$  respectively (where,  $n$  stands for number of cell capacitors per arm).
- 3) Since the precise locations of the submodule capacitors to be inserted into power path and that to be bypassed are known from step 2), the mapping summarized in Table 1 can be directly used to generate the gating signals for individual switches  $S_{ik}$ , where ‘ $k$ ’ varies from 1 to 6 and  $k \in \mathbb{N}$ .

B) **Method II:** This method is summarised as follows:

- 1) Vector ( $V_c$ ) of capacitor voltages of each arm is created.
- 2) Submodule capacitors to be inserted into power path from each arm are determined using sorting of the capacitor voltages [ $A_I$   $IX$ ]=sort( $V_c$ , 'ascend') and [ $B_I$   $IY$ ]=sort( $V_c$ , 'descend'), where  $IX$  and  $IY$  are index vectors that hold locations of the cells to be switched in and out of the power path, and  $A_I$  and  $B_I$  are sorted versions of the cell capacitor voltages  $V_c$  in ascending and descending orders. A vector of status signals  $\lambda[i]=1$  and 0 are assigned to the submodule capacitors to be inserted into the power path and those to be bypassed, taking into account the arm current polarity and voltage level to be synthesized (where, ‘ $i$ ’ is a positive integer that varies from 1 to  $n$ ).
- 3) The status vector  $\lambda$  that was created in step 2) will be used to determine the number of capacitors to be inserted into power path from each submodule using  $\sigma[k]=\lambda_1[k]+\lambda_2[k]$ ; where  $\lambda_1[k]=\lambda[2k-1]$  and  $\lambda_2[k]=\lambda[2k]$ ,  $k$  is a positive integer that varies from 1 to  $\frac{1}{2}n$ , and  $\lambda_1$  and  $\lambda_2$  are vectors that represent status of the capacitors  $C_{1k}$  and  $C_{2k}$ . Notice that  $\sigma[k]=0, 1$  and 2 stand for the following cases: when both capacitors of  $k^{th}$  submodule are bypassed; one of the submodule capacitors is inserted into the power path and other is bypassed; and both capacitors of  $k^{th}$  submodule are inserted into power path.
- 4) Using information provided by vector  $\sigma$  and mapping in Table 1, the gating signals of individual switches are generated and voltage across the cell capacitors  $C_{1k}$  and  $C_{2k}$  of each  $k^{th}$  submodule are balanced locally, taking into account arm current polarity.

Notice that in method I, the cell capacitor voltage balancing in step 2) is performed in similar manner as that in conventional HB-MMC, while in the method II, the cell capacitor voltage balancing is performed at cell level, which is simpler and faster. A flow chart that depicts implementation steps of method II is provided in the appendix, Figure 14.

Figure 4 shows basic waveforms of three-phase MMC that employs 16 of the proposed cell in Figure 3(b) in its arms and being controlled using amplitude modulation and the cell capacitor voltage balancing method II. The following parameters are assumed in this illustration:  $V_{dc}=80\text{kV}$ ;  $C_m=10\text{mH}$ ; number of cells per arm is 16 (two capacitors per cell); arm reactor inductance and internal resistance are  $L_d=10\text{mH}$  and  $R_d=0.25\Omega$ ; load resistance and inductance are  $20\Omega$  and  $40\text{mH}$  (equivalent to three-phase power of  $66.8\text{MW}$  and  $42.1\text{MVar}$ ); and 0.90 modulation index. In this example, the 2<sup>nd</sup> harmonic current component of the common-mode in each phase is suppressed using a resonant controller. The plots for the pre-filter output phase voltage, three-phase output currents, phase ‘ $a$ ’ upper and lower arm currents and phase ‘ $a$ ’ cell capacitor voltages in Figure 4 (a), (b), (c) and (f) show that the MMC which uses the proposed cell operates satisfactorily, retains seamless current commutation between upper and lower arms as with the HB-MMC, and the voltages across the cell capacitors are well regulated around  $\frac{1}{2}V_{dc}/n$  ( $\frac{1}{2} \times 80/16 \approx 2.5\text{kV}$ ). Figure 4 (d) and (e) shows that phase ‘ $a$ ’ common-mode current is practically dc with its parasitic component (2<sup>nd</sup> harmonic current) is successfully suppressed to nearly zero. Figure 4 (g) shows the common and differential-mode ac powers the upper and lower arm cell capacitors of phase ‘ $a$ ’ exchange with the dc and ac sides. Observe that the common and differential-mode ac powers oscillate at 2<sup>nd</sup> harmonic and fundamental frequencies and adhere to the following analytical expressions:

$p_{com}(t)=p_{ac1}(t)+p_{ac2}(t)=\frac{1}{4}mV_{dc}I_m\cos(2\omega t+\varphi)=\frac{1}{3}P\cos 2\omega t-\frac{1}{3}Q\sin 2\omega t$  and  $p_{dif}(t)=p_{ac1}(t)-p_{ac2}(t)=\frac{1}{3}P(2-m)/m\times\sin\omega t-\frac{2}{3}Q/m\times\cos\omega t$ ; which are identical to that of the HB-MMC; where,  $p_{ac1}=v_{a1}i_{a1}$  and  $p_{ac2}=v_{a2}i_{a2}$ , and P and Q are the average active and reactive powers the converter exchanges with the ac side or load. The absence of dc components in both ac power components confirm that the upper and lower arm cell capacitors exchange zero average active power with the dc and dc sides; thus, natural balancing of the cell capacitor voltages could be ensured with simple cell rotation as suggested originally [35]. The differential and common-mode energies displayed in Figure 4 (h) and (i) indicate that the converter being studied has constant average common-mode energy and zero average differential-mode energy; and the latter indicates that the energy balance between the upper and lower arm cell capacitors is ensured (vertical balancing). These common and differential mode energies are described analytically as follows:

$$p_{ac1}(t) = v_{a1}i_{a1} = \frac{1}{4}I_m V_{dc} \sin(\omega t + \varphi) - \frac{1}{2}mI_d V_{dc} \sin \omega t + \frac{1}{8}mI_m V_{dc} \cos(2\omega t + \varphi) \quad (1)$$

$$p_{ac2}(t) = v_{a2}i_{a2} = -\frac{1}{4}I_m V_{dc} \sin(\omega t + \varphi) + \frac{1}{2}mI_d V_{dc} \sin \omega t + \frac{1}{8}mI_m V_{dc} \cos(2\omega t + \varphi) \quad (2)$$

The upper and lower arm cell capacitors energies are:

$$\frac{dE_1(t)}{dt} = p_{ac1}(t) \Rightarrow E_1(t) = E_1(0) - \frac{1}{4}\frac{I_m V_{dc}}{\omega} \cos(\omega t + \varphi) + \frac{1}{2}\frac{mI_d V_{dc}}{\omega} \cos \omega t + \frac{1}{16}mI_m V_{dc} \sin(2\omega t + \varphi) \quad (3)$$

$$\frac{dE_2(t)}{dt} = p_{ac2}(t) \Rightarrow E_2(t) = E_2(0) + \frac{1}{4}\frac{I_m V_{dc}}{\omega} \cos(\omega t + \varphi) - \frac{1}{2}\frac{mI_d V_{dc}}{\omega} \cos \omega t + \frac{1}{16}mI_m V_{dc} \sin(2\omega t + \varphi) \quad (4)$$

Where,  $E_1(0) = E_2(0) = E(0) \approx N_c \times \frac{1}{2}C_m \left[ \frac{V_c}{N_c} \right]^2 = \frac{1}{2}\frac{C_m V_c^2}{N_c}$ , and  $V_c \approx V_{dc} - 2R_d I_d - 2N_c V_{device}$  ( $V_{device}$  represents dc voltage drop per device).

per device).

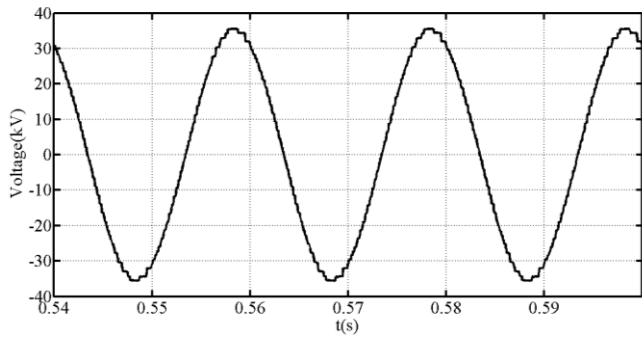
From (3) and (4), common and differential mode energies are:

$$E_{com}(t) = \frac{C_m V_c^2}{N_c} + \frac{1}{6\omega} [P \sin 2\omega t + Q \cos 2\omega t] \quad (5)$$

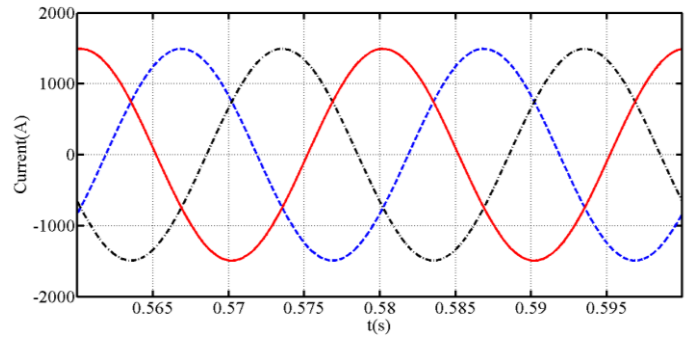
$$E_{dif}(t) = \frac{1}{6\omega} [P(m-1/m) \cos \omega t + 2Q/m \sin \omega t] \quad (6)$$

Observe that equations (5) and (6) agree with the simulation waveforms for the common and differential-mode energies presented in Figure 4 (h) and (i). Equations (5) and (6) indicate that the common and differential mode energies could be manipulated through the 2<sup>nd</sup> and 1<sup>st</sup> harmonic currents. Whilst Figure 4 (d) shows the common-mode currents of the three phase legs have the same magnitude, which indicates that the horizontal balancing or even distribution of dc link current between the three phases is ensured.

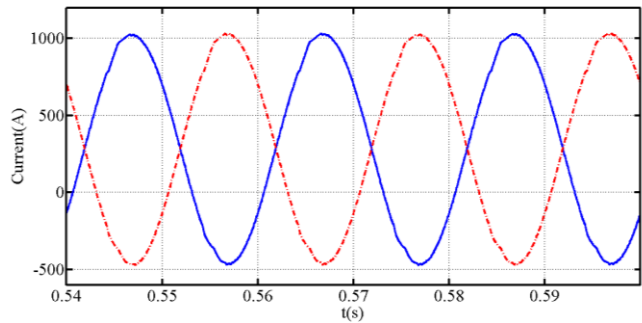
The voltage waveforms across the switching devices  $S_1$ ,  $S_2$  and  $S_3$  and  $S_5$  in Figure 4 (j), (k) and (l) indicate that the switching devices of the MMC which employs the proposed cell operate at reduced average switching frequency as in HB-MMC. Since the composite switch  $S_2S_3$  in Figure 3(b) is exposed to multilevel voltage waveform as in Figure 4 (f) with one voltage level switched at each instant, the composite switch  $S_2S_3$  can be formed without the need for stringent requirement of typical series device connection. The voltage waveforms in Figure 4 (j), (k) and (l) show that the conduction periods of switches  $S_1$  and  $S_5$  in the proposed cell are not significantly different as that between the main and auxiliary switches  $S_1$  and  $S_2$  of the half-bridge cell, see Figure 3 (b) and (c), with the composite switch  $S_2S_3$  being used to halve the currents in  $S_5$  and  $S_6$  (thus, better loss distribution is expected).



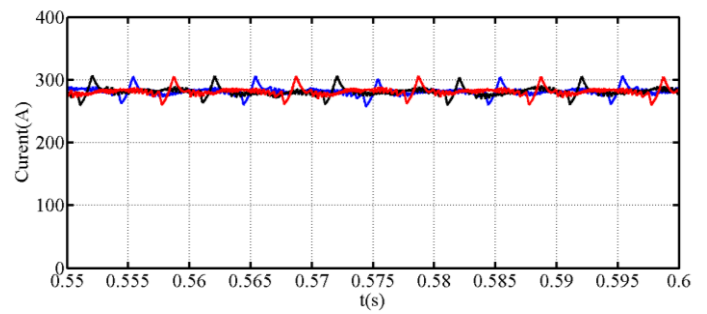
(a) Phase voltage ( $v_{ao}$ )



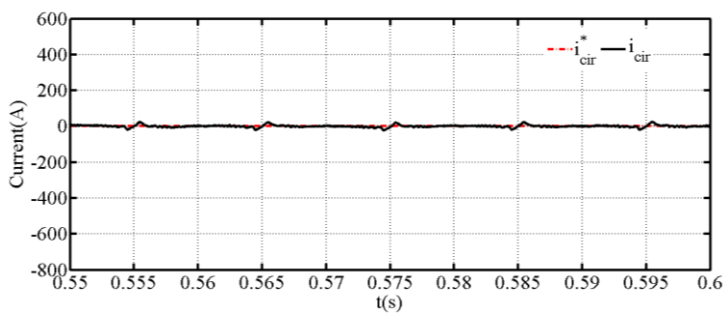
(b) Three-phase output currents



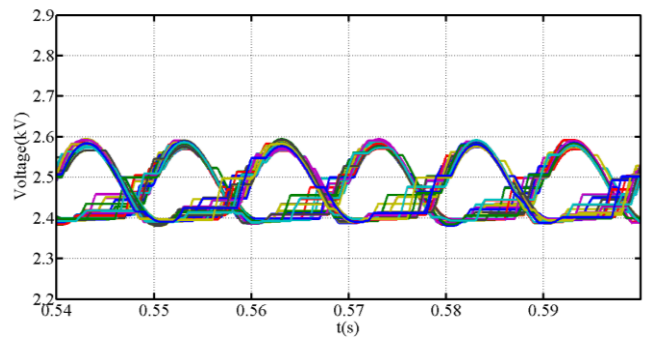
(c) Phase 'a' upper and lower arms currents



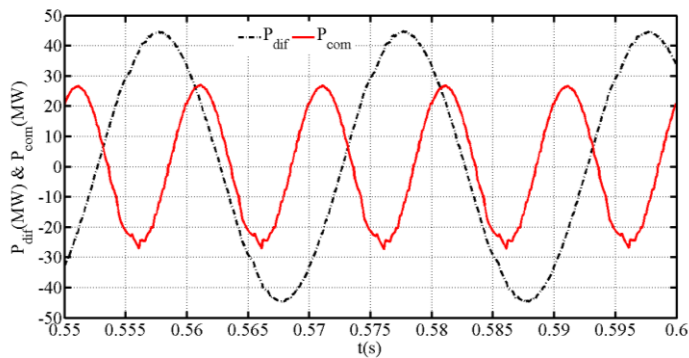
(d) Common-mode currents of the three phases



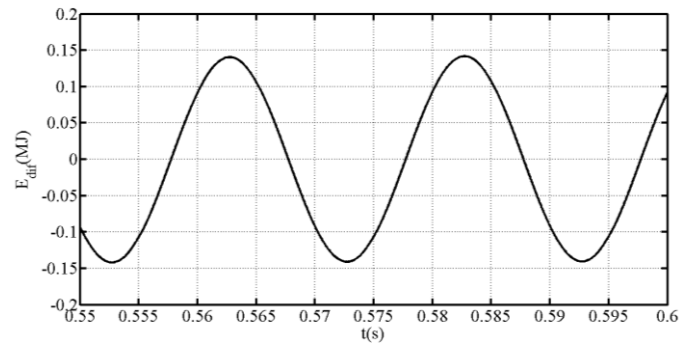
(e) Phase 'a' circulating current



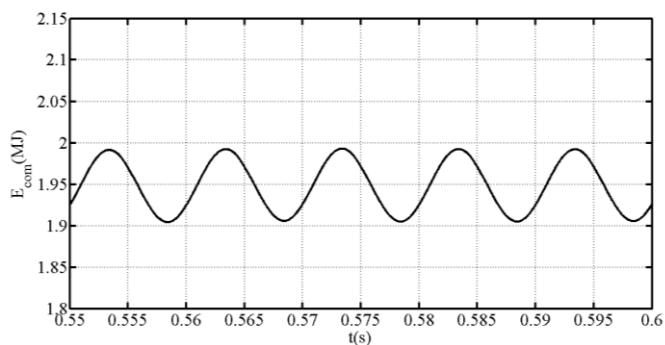
(f) Phase 'a' upper and lower arm cell capacitor voltages



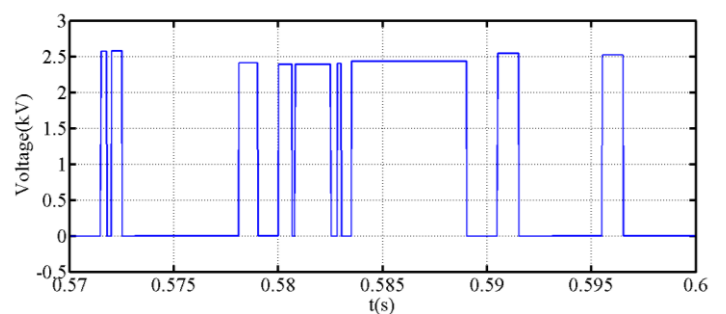
(g) Phase 'a' differential and common-mode ac powers



(h) Phase 'a' differential-mode energy



(i) Phase 'a' common-mode energy



(j) Voltage across switch  $S_{a1}$

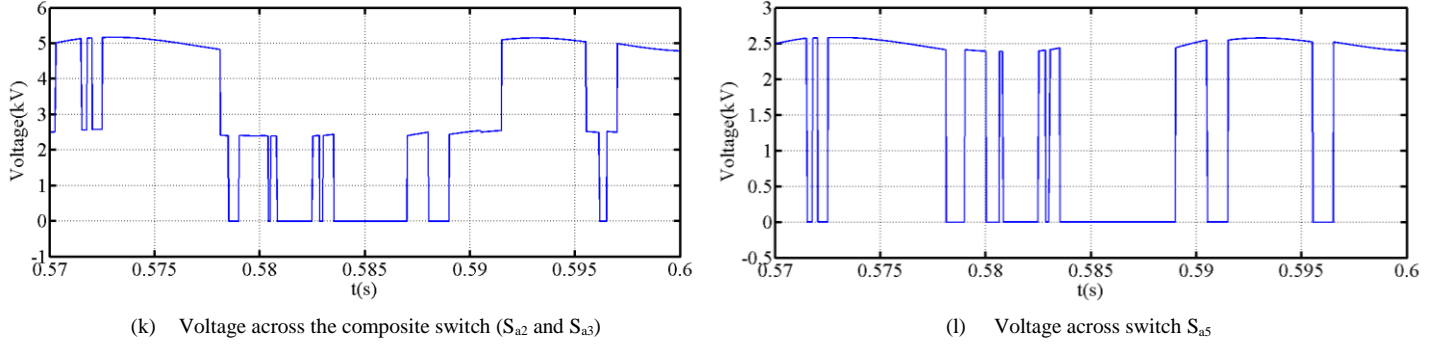


Figure 4: Simulation waveforms for the MMC that employs the proposed cell in Figure 3(b)

### III. ANALYTICAL SEMICONDUCTOR LOSS ESTIMATION

Since semiconductor loss is a decisive factor that determines successful adoption or abandonment of the modular type converters in practical systems, this section presents an approximate method for loss calculations, and this method is used in this paper to compare the semiconductor loss of the MMC that employs the proposed cell against that uses conventional half-bridge cell. Notice that the MMC with half-bridge cell and proposed cell present a fixed number of switching devices in conduction path for a given voltage stress per device and dc link voltage, irrespective of modulation strategy. For an example, out of ‘ $2n$ ’ cell capacitors available for selection in each phase leg at any instant, ‘ $2n$ ’ switches must be used to insert ‘ $n$ ’ cell capacitors into conduction path, and ‘ $2n$ ’ switches for bypassing of the ‘ $n$ ’ remaining cell capacitors. During bypass of the ‘ $n$ ’ cell capacitors using switches  $S_2S_3S_5S_6$  in each cell, the current conduction path is through diodes ( $D_2D_3D_5D_6$ ) for  $i_a < 0$ , and through IGBTs ( $T_2T_3T_5T_6$ ) for  $i_a \geq 0$ . During insertion of the cell capacitors into conduction path, the current flow through the IGBT or diode depends on the individual switch location within each cell, see Table 2. Figure 5 depicts MMC upper and lower arm currents, and their corresponding insertion functions. Observe that the conduction period of diodes ( $D_2D_3D_5D_6$ ) and IGBTs ( $T_2T_3T_5T_6$ ) of the switches  $S_2S_3S_5S_6$ , which are used to bypass cell capacitors, vary significantly with the magnitude and polarity of the dc component of the arm current  $I_d$  ( $I_d$  varies strongly with dc power being exchanged), see Figure 5(a). The current conduction between  $\beta$  and  $\pi - \beta$  in Figure 5(a) represents conduction period of diodes ( $D_2D_3D_5D_6$ ) during bypass of the cell capacitor of individual cells, where  $I_0$  represents the peak fundamental components of the arm currents; and  $\beta = \sin^{-1} I_d / I_0$ . Recall that  $I_d = \frac{1}{3} I_{dc}$  ( $I_{dc}$  is the dc link current) and  $I_0 = \frac{1}{2} I_m$  (where,  $I_m$  represent peak of the output phase current). From Figure 3 (b) and Figure 5(a) and Table 2, currents in the IGBTs and diodes of the switches being used to bypass the cell capacitors in each phase leg are  $i_{Tb}(t) = i_a$  for  $\pi - \beta < \omega t \leq 2\pi + \beta$  and  $i_{Db}(t) = -i_a$ ,  $\beta < \omega t \leq \pi - \beta$ .

Using these definitions of  $i_{Tb}(t)$  and  $i_{Db}(t)$ , the equivalent average and root mean square currents in the IGBTs and diodes of the switches being employed to bypass ‘ $n$ ’ cell capacitors are approximated by:

$$\bar{I}_{Tb} = \left[ \frac{1}{2} I_d (\pi + 2\beta) + \sqrt{I_0^2 - I_d^2} \right] / \pi \quad (7)$$

$$\bar{I}_{Db} = \left[ \left[ \frac{1}{2} I_d (\pi - 2\beta) - \sqrt{I_0^2 - I_d^2} \right] / \pi \right] \quad (8)$$

$$I_{rms\_Tb}^2 = \left[ \left( I_d^2 + \frac{1}{2} I_0^2 \right) (\pi + 2\beta) + 3 I_d \sqrt{I_0^2 - I_d^2} \right] / 2\pi \quad (9)$$

$$I_{rms\_Db}^2 = \left[ \left( I_d^2 + \frac{1}{2} I_0^2 \right) (\pi - 2\beta) - 3 I_d \sqrt{I_0^2 - I_d^2} \right] / 2\pi \quad (10)$$

Using expressions (7) to (10), the on-state losses of the switches  $S_2S_3$  and  $S_5S_6$  being used to bypass ‘ $n$ ’ cell capacitors from each phase leg are computed using:

$$P_{Tb} = n \left[ V_{T0} \bar{I}_{Tb} + \frac{1}{2} R_{Ton} I_{rms\_Tb}^2 \right] \quad (11)$$

$$P_{Db} = n \left[ V_{D0} \bar{I}_{Db} + \frac{1}{2} R_{Don} I_{rms\_Db}^2 \right] \quad (12)$$

where,  $R_{Don}$  and  $R_{Ton}$ , and  $V_{Do}$  and  $V_{To}$  are on-state resistances and threshold voltages of the diode and IGBT that form a single composite switch  $S_2S_3$  and  $S_5S_6$ . However, insertion of ‘ $n$ ’ cell capacitors using switch states that generate ‘ $V_c$ ’ and ‘ $2V_c$ ’ from each arm insert ‘ $n$ ’ switches of mixed combinations (diodes and IGBTs) into conduction path, see Table 2 and Figure 3(b). This introduces some imperfections, which are handled in this paper using average on-state resistance and threshold voltage of the IGBT and diode ( $R_{on}=\frac{1}{2}(R_{Don}+R_{Ton})$  and  $V_T=\frac{1}{2}(V_{Do}+V_{To})$ ), and their equivalent average and root mean square currents are approximated by:

$$\bar{I}_{Ti} = \frac{1}{2\pi} \left[ \int_{\beta}^{\pi-\beta} i_{ia} dt + \int_{\pi-\beta}^{2\pi+\beta} i_{ia} dt \right] = \bar{I}_{Db} + \bar{I}_{Tb} \quad (13)$$

$$I_{rms\_Ti}^2 = \frac{1}{2\pi} \int_{\beta}^{2\pi+\beta} i_{ia}^2 dt = \left( I_d^2 + \frac{1}{2} I_0^2 \right) \quad (14)$$

Using expressions (7) to (10), the on-state losses of the switches  $S_2S_3$  and  $S_5S_6$  being used to bypass ‘ $n$ ’ cell capacitors from each phase leg are computed using:

$$P_{Ti} = n \left[ V_{T0} \bar{I}_{Ti} + R_{Ton} I_{rms\_Ti}^2 \right] \quad (15)$$

Notice that equations (7) to (15) could be applied to HB-MMC (see cell in Figure 3(c)) should ‘ $\frac{1}{2}$ ’ in (11) and (12) is omitted.

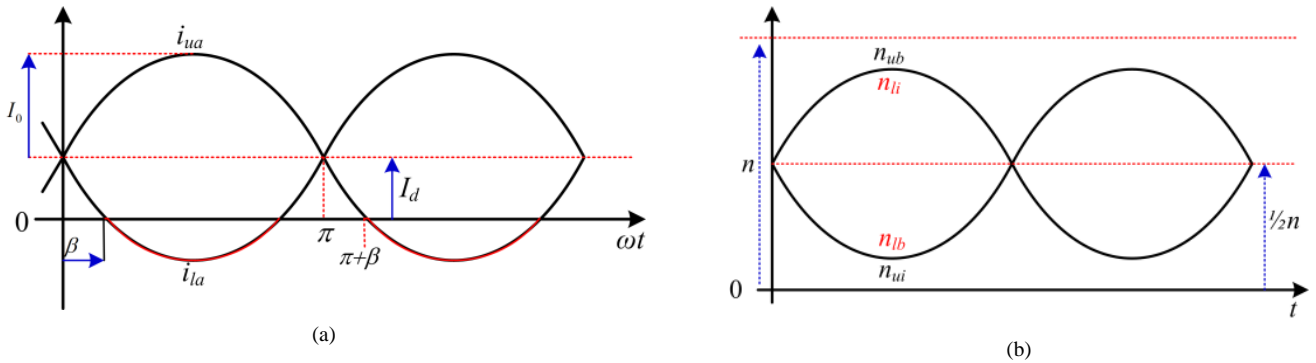


Figure 5: (a) and (b) are MMC upper and lower arm currents ( $i_u$  and  $i_l$ ) and their corresponding insertion functions

Table 2: Detailed current path of the proposed submodule in Figure 3 (b)

Voltage levels	Conduction path	Switch states	current polarity
0	$T_2, T_3, T_5, T_6$	$S_2, S_3, S_5, S_6$	$i_a > 0$
	$D_2, D_3, D_5, D_6$		$i_a < 0$
$V_c$	$D_4 T_5$	$S_4 S_5$	$i_a > 0$
	$T_4 D_5$		$i_a < 0$
	$D_1 T_6$	$S_1 S_6$	$i_a > 0$
	$T_1 D_6$		$i_a < 0$
$2V_c$	$D_1, D_4$	$S_1 S_4$	$i_a > 0$
	$T_1, T_4$		$i_a < 0$

To demonstrate the improved efficiency of the MMC that uses proposed cell in Figure 3(b) compared to that uses HB cell, the on-state losses of MMCs that employ these two cells are presented in Table 3. The on-state loss estimated in Table 3 are computed, assuming the following rated parameters: 1052MVA converter with 640kV ( $\pm 320$ kV) dc link voltage; 352kV line-to-line ac voltage, which is corresponding to 0.9 modulation index; and considering three operating points shown in Table 3. In this study, 4.5kV IGBT(T1800GB45A) from Westcode is assumed, with a voltage stress per switch of 2.0kV. Analytical and simulation on-state losses summarized in Table 3 indicate that the MMC with the proposed cell arrangement has lower on-state loss than the conventional HB-MMC. It has been found that presented analytical method overestimates the on-state losses of both converters being compared by a maximum of 6% with respect to that being computed using detailed simulation (on-state loss of individual device is calculated using measured currents and then added together), considering three operating points in Table 3.

Table 3: Validation of analytical estimated on-state loss against that obtained using simulation (MMC with the proposed cell arrangement versus that uses half-bridge cell)

MMC	$\text{Cos}\phi=1$	$\text{Cos}\phi=0.8$	$\text{Cos}\phi=0$	
Proposed cell	4.99MW	4.72MW	4.27MW	Analytical
	4.7MW	4.50MW	4.01	Simulation
Half-bridge cell	5.59MW	5.25MW	4.68MW	Analytical
	5.51MW	5.00MW	4.50MW	Simulation

For calculations of switching loss, IGBT turn-on and turn-off energy losses ( $E_{on}$  and  $E_{off}$ ) from datasheet are approximated as:  $E_{on} = -270.7 \times 10^{-12} i_{on}^4 + 1.812 \times 10^{-6} i_{on}^3 - 2.744 \times 10^{-3} i_{on}^2 + 4.953 i_{on}$  and  $E_{off} = -3.11 \times 10^{-9} i_{off}^4 + 11.57 \times 10^{-6} i_{off}^3 - 13.65 \times 10^{-3} i_{off}^2 + 8.921 i_{off}$ ; where  $i_{on}$  and  $i_{off}$  are currents at the turn-on and turn-off instances. IGBT switching loss is obtained from:  $P_{sw} = (f_{on} \bar{E}_{on} + f_{off} \bar{E}_{off})$ , where  $\bar{E}_{on}$  and  $\bar{E}_{off}$  are average turn-on and turn-off energy losses over one fundamental cycle, and  $f_{on}$  and  $f_{off}$  are switching frequencies. With freewheeling diodes recovery losses being neglected, Table 4 and Table 5 show that the switching losses and total semiconductor losses of the MMC with the proposed cell arrangement are lower than that of the HB-MMC. The results in Table 3, Table 4 and Table 5 all indicate that the MMC that uses the proposed cell arrangement outperforms the HB-MMC from semiconductor loss point of view. Please refer to [36, 37] for more detailed method for semiconductor loss calculations, where diode recovery losses are taken into account. With power loss cost assumed to be 3M€/MW per year [38], the savings over project lifetime of 30 years between the two converters are displayed in Table 5.

Table 4: Summary of estimated switching losses of both MMCs (simulation)

	$\text{Cos}\phi=1$	$\text{Cos}\phi=0.8$	$\text{Cos}\phi=0$
<b>Proposed cell</b>	2.30MW	2.18MW	2.99MW
<b>Half-bridge cell</b>	3.39MW	3.11MW	3.75MW

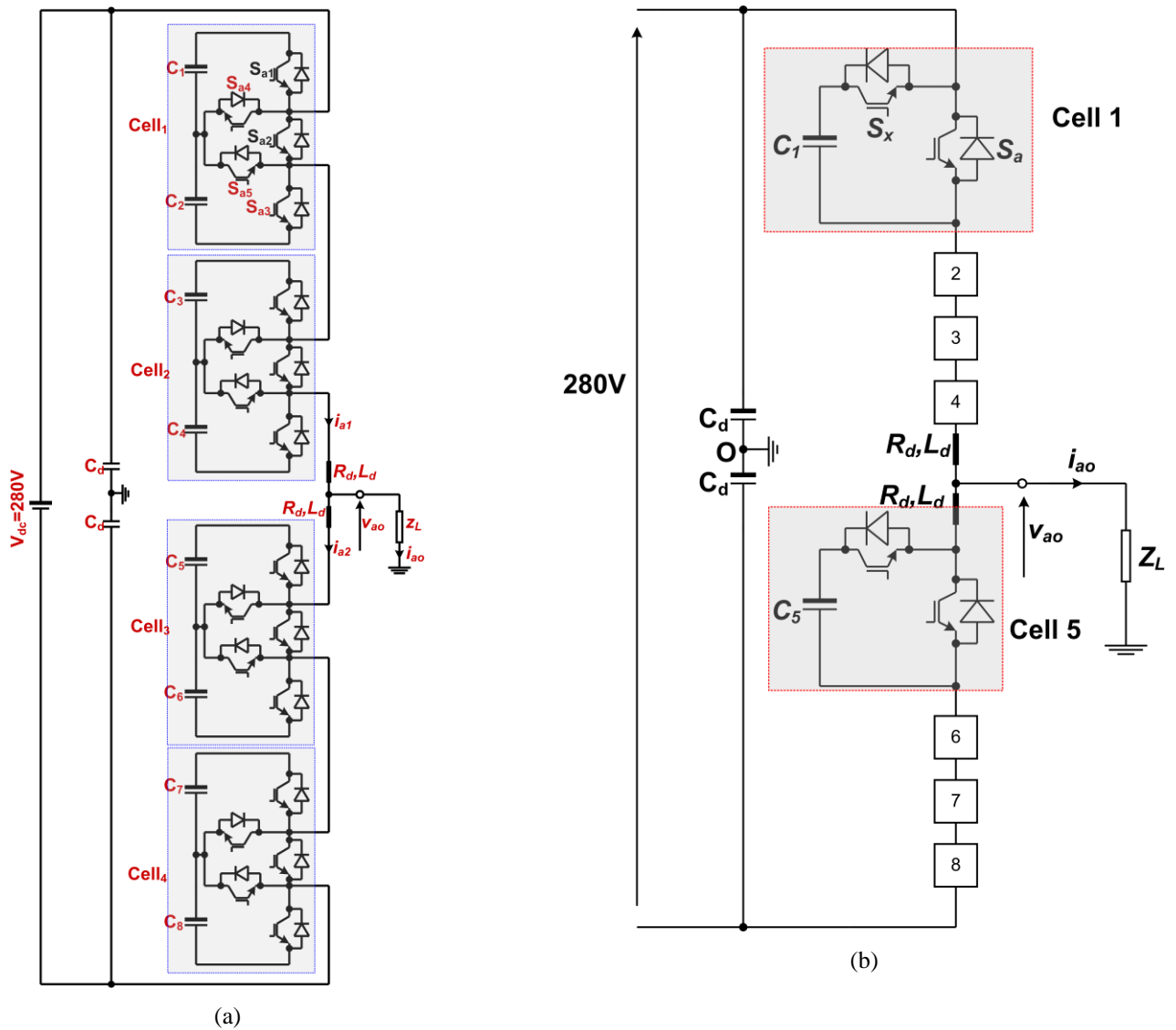
Table 5: Summary of total semiconductor losses (on-state plus switching) converter of the proposed MMC against half-bridge MMC

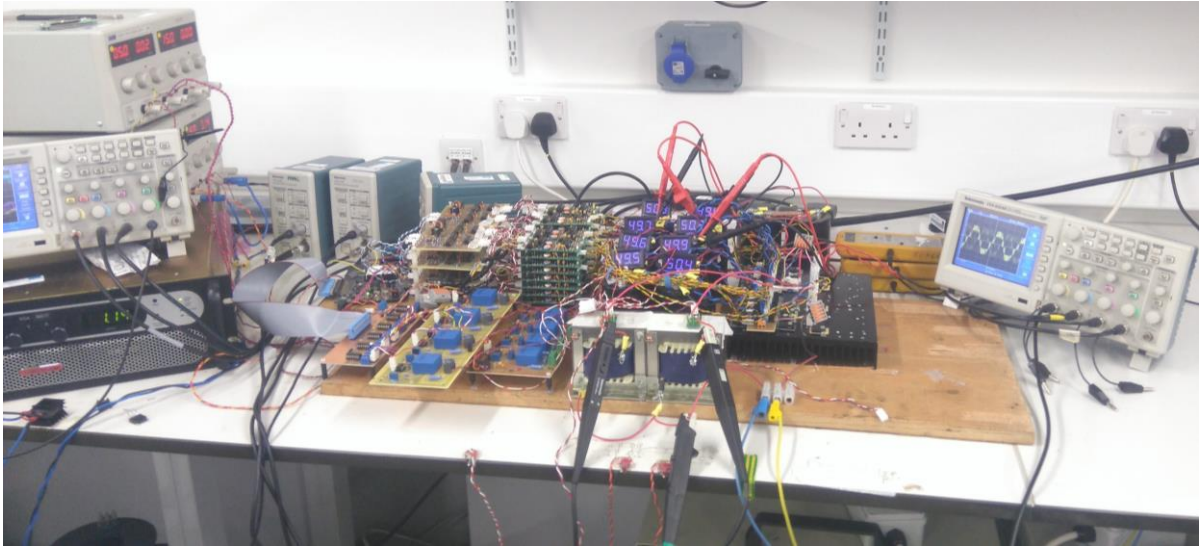
	$\text{Cos}\phi=1$	$\text{Cos}\phi=0.8$	$\text{Cos}\phi=0$
<b>Proposed cell</b>	7.29MW(0.69%)	6.90MW(0.66%)	7.26MW(0.69%)
<b>Half-bridge cell</b>	8.98MW (0.85%)	8.36MW(0.80%)	8.05MW(0.77%)
<b>Cost saving</b>	152.1M€	131.4M€	71.1M€

#### IV. REDUCED SCALE EXPERIMENTATIONS

This section uses reduced scale experimentations to compare the performance of the MMC that employs the presented cell in Figure 3(b) against that uses the conventional HB cell. Figure 6 shows schematic diagrams and prototypes of both converters, with test rig parameters listed in Table 6. Modulation and capacitor voltage balancing are programmed on low-cost 32-bit Cypress microcontroller (CY8CKIT-050 PSoc® 5LP). Due to the reduced number of cells per arm (4 cells), pulse width modulation with 2.4kHz carrier frequency is used (carriers are arranged in phase disposition fashion). Experimental waveforms presented in Figure 7 (a) to (e) and Figure 8 (a) to (e) show that both MMCs produce similar output voltages and currents, upper and lower arm currents and cell capacitor voltages. However, samples of the gating signals in Figure 7 (f) and Figure 8 (f) indicate that the proposed cell is expected to have better loss distribution as the arm current will be evenly shared between  $S_{a2}$ ,  $S_{a3}$ ,  $S_{a5}$  and  $S_{a6}$  when the cell generates zero voltage level (when gating signals of  $S_{a2}$  and  $S_{a4}$  in Figure 7f are both high). Summary of the overall semiconductor losses (on-state plus switching) of both converters obtained from experiments in Table 7 confirm that the improved loss performance of the proposed cell. But the figures for the semiconductor losses displayed are extremely high due to the use of low cost IGBTs with high on-state voltage drop employed (30A, 1200V IGBT, STGW30NC120HD, while the actual average voltage stress per cell capacitor and IGBT is 70V). Because of the IGBTs over-rating, it is observed that the peak fundamental voltages obtained from both prototypes are 102.1V and 100.9V for the proposed and HB cells respectively, compared to theoretical peak voltage  $V_m = 1/2 m V_{dc} = 1/2 \times 0.8 \times 280 = 112V$ . Notice that with the measured dc link current = 1.89A and output active

power=481.6W (proposed cell), the effective dc voltage, excluding the total devices voltage drop and losses in the switching devices could be approximated by  $V_{dc}=P_{dc}/I_{dc}=481.6/1.89\approx 254.8V\approx V_c$ , assuming switching losses in the reduced scale prototype is negligible. This discussion indicates that the total dc voltage drop in the switching devices is  $280-254.8=25.2V$ , power loss= $25.2\times 1.89\approx 47.6W$ , and peak phase voltage  $V_m=\frac{1}{2}mV_c=\frac{1}{2}\times 0.8\times 254.8=101.92V$ , which are in line with the measured loss and peak phase voltage in Table 7 and Figure 7(b). Similarly, for the prototype of the HB-MM, the effective dc voltage  $V_{dc}=V_c=477.1/1.89\approx 252.4V$ , peak phase voltage  $V_m=\frac{1}{2}mV_c=\frac{1}{2}\times 0.8\times 252.4=100.96V$ , and power loss= $(280-252.4)\times 1.89\approx 52.17W$ . These results also agree with experimental results summarised in Table 7 and Figure 8(b). Although on a per unit basis the magnitudes of the experimental losses are out of step with that expected in full-scale HVDC converter, it does not invalidate the superiority of the proposed cell over the HB cell in term of semiconductor loss.





(c)

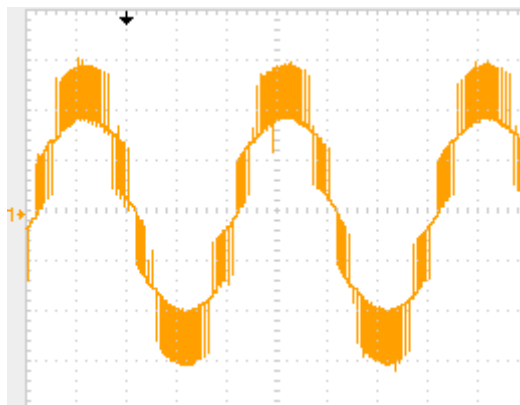
Figure 6: (a) and (b) are schematic diagrams of the simulated and practical MMCs that employ the proposed cells and conventional half-bridge cells, and (c) photograph of the prototypes of both MMCs

Table 6: Simulation and test rig parameters

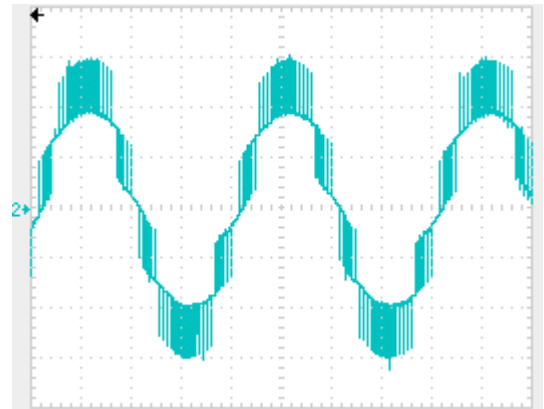
DC link voltage(Vdc)	280V
Number of cells (proposed)	2
Number of cells (half-bridge)	4
Arm reactor inductance ( $L_d$ )	3mH
Arm reactor internal resistance ( $R_d$ )	0.1
Cell capacitance ( $C_m$ )	2.2mF
Load resistance	9.5 $\Omega$
Load inductance	6mH
Switching frequency	2.4kHz
Average voltage per capacitor	70V

Table 7: Summary of the experimental loss

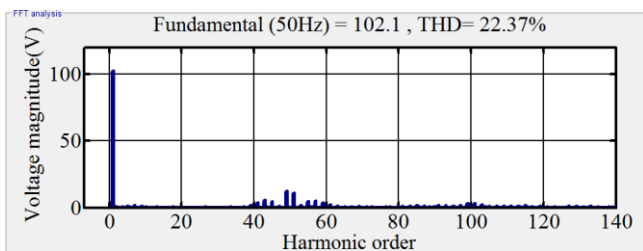
	Proposed MMC	HB-MMC
Input dc power ( $P_{dc}$ )	529.2W	529.2W
Average output ac power ( $P_{ac}$ )	481.6W	477.05W
Power loss ( $P_L=P_{dc}-P_{ac}$ )	47.6W	52.15W



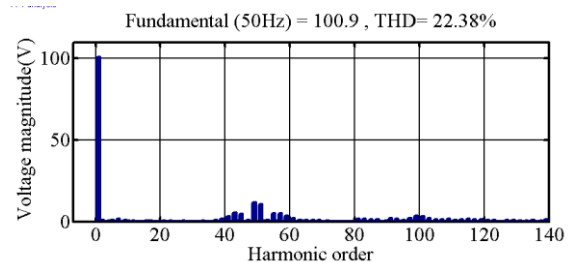
(a) Pre-filter output voltage (5ms/div and 40V/div)



(a) Pre-filter output voltage (5ms/div and 40V/div)

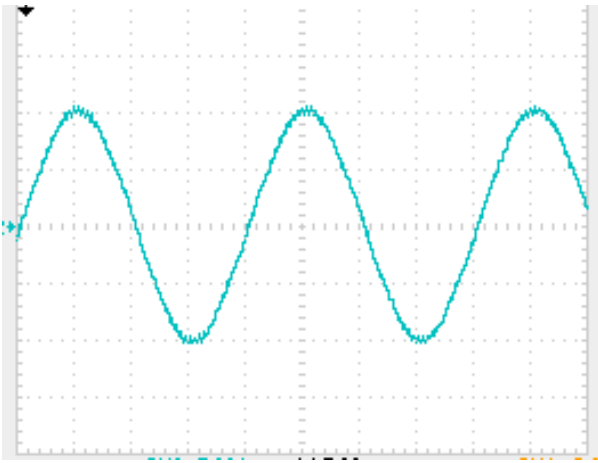


(b) Phase voltage spectrum

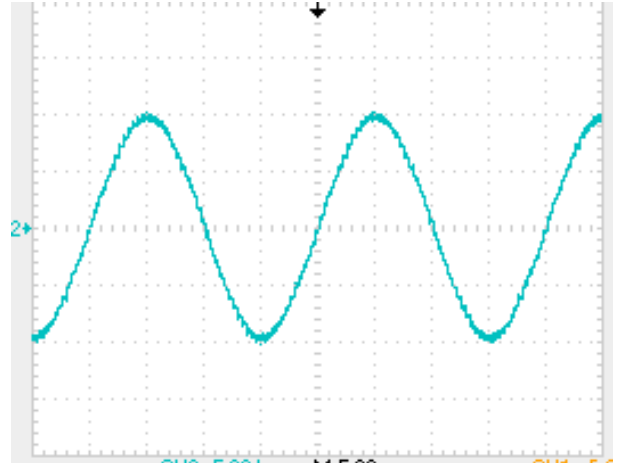


(b) Phase voltage spectrum

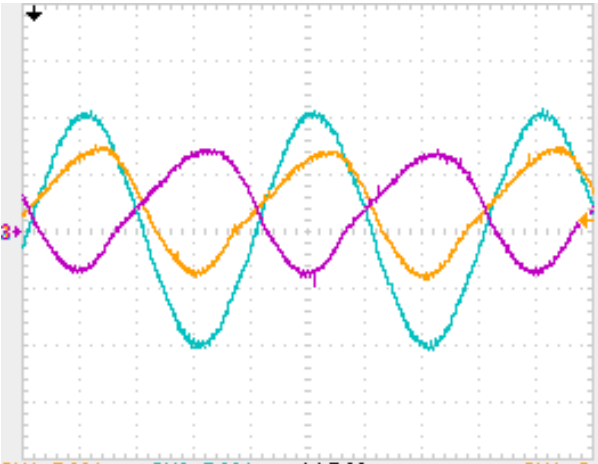




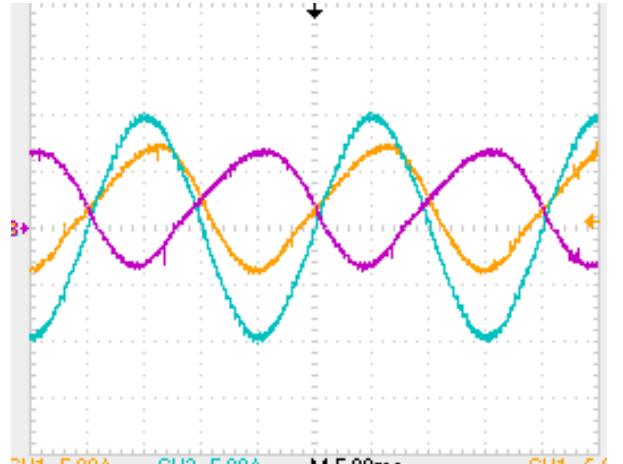
(c) Output phase current(5ms/div and 5A/div)



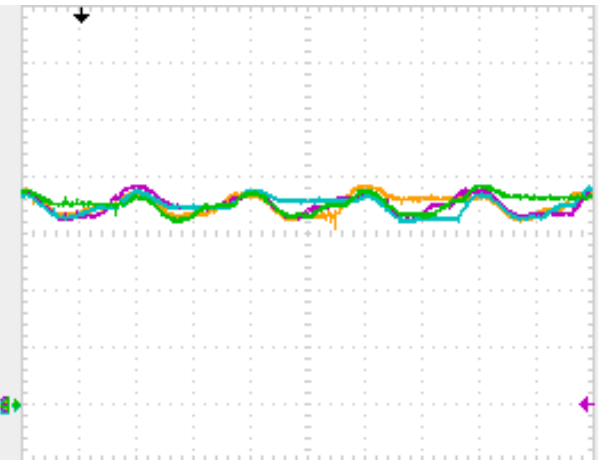
(c) Output phase current(5ms/div and 5A/div)



(d) Upper and lower arm current and output phase or load current (5ms/div and 5A/div).



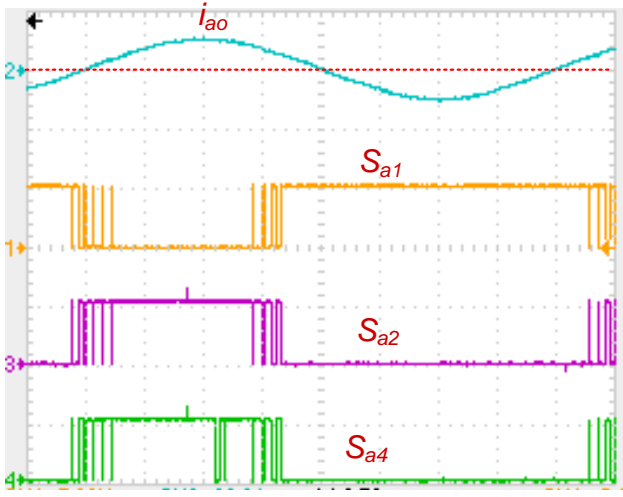
(d) Upper and lower arm current and output phase or load current (5ms/div and 5A/div).



(e) Upper arm cell capacitor voltages (10ms/div and 20V/div)

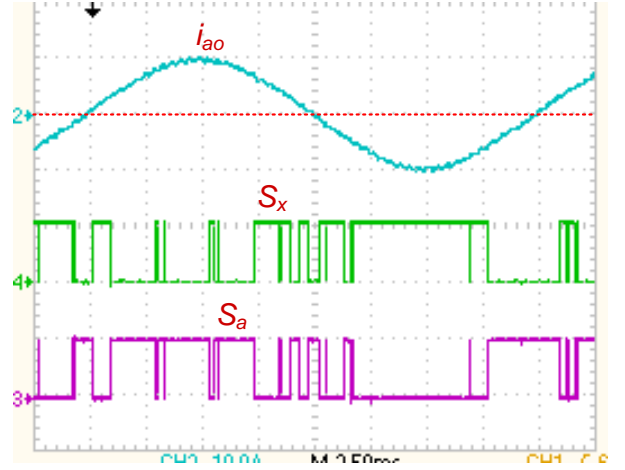


(e) per arm cell capacitor voltages (10ms/div and 20V/div)



f) Output phase current and samples of gating signals of the one cell during converter operation (2.5ms/div, 5V/div for  $S_{a1}$ ,  $S_{a2}$  and  $S_{a4}$  and 20A/div for  $i_{ao}$ )

Figure 7: Experimental results from scaled down prototype of the MMC with the proposed cell as shown in Figure 6 (a) and (c)



f) Output phase current and samples of gating signals of the one cell during converter operation (2.5ms/div, 5V/div for  $S_x$  and  $S_a$  and 10A/div for  $i_{ao}$ )

Figure 8: Experimental results from scaled down prototype of the MMC with the conventional half-bridge cell as shown in Figure 6 (b) and (c)

## V. SYSTEM SIMULATIONS

This section presents system simulations of the MMC that adopts the proposed cell, considering dc short circuit fault and continued operation when some cells fail. Figure 9 shows the test system that represents 84MVA converter terminal of symmetrical monopole HVDC link, with  $\pm 40\text{kV}$  dc link voltage, connected to 66kV ac grid through 80MVA, 40kV/66kV ac transformer with 20% per unit reactance. The proposed MMC is modelled using a detailed switch model, with 16 cells (32 cell capacitors) per arm, arm inductance  $L_d=10\text{mH}$ , and each cell capacitance is rated at 2.5kV and 8mF. DC cable parameters are given in Figure 9, with ac side high impedance grounding adopted as suggested in [39, 40] to define the insulation level for the dc side. In this example, the MMC being studied is equipped with active and reactive power controllers, a fundamental current controller in  $d-q$  frame, circulating current controller and cell capacitor voltage balancing (overall control system is similar to that in [41]). At startup, the converter station is commanded to inject active power of 64MW into ac grid, at bus B at unity power factor. A permanent pole-to-pole dc short circuit fault is applied in the middle of the dc line at time  $t=0.5\text{s}$ , and active power injection into B is reduced to zero immediately, with gating signals to converter switches inhibited after  $50\mu\text{s}$  from fault initiation.

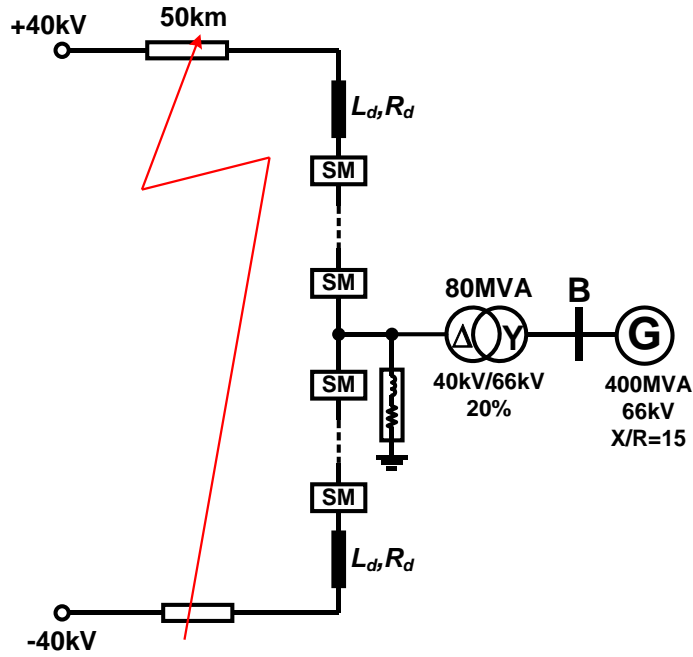
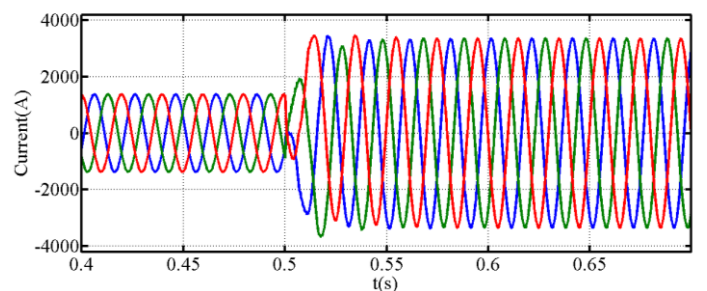
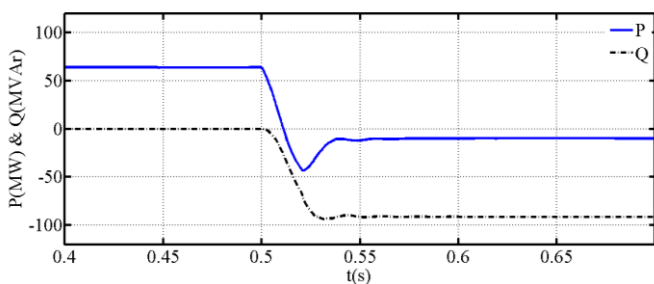


Figure 9: Converter terminal of monopole HVDC link ( $R_{dc}=9m\Omega/km$ ,  $L_{dc}=1.35mH/km$  and  $C_{dc}=0.23\mu F/km$ )

### A) Pole-to-pole dc short circuit fault

Figure 10 presents selected waveforms that illustrate the behaviour of the MMC that employs the proposed cell when it is subjected to a pole-to-pole dc short circuit fault. Figure 10(a) and (b) display active and reactive power converter exchanges with the ac grid ‘G’, measured at bus B, and ac currents in the low-voltage side of the interfacing transformer. Figure 10(c) shows phase ‘a’ upper and lower arm currents are well controlled during normal operation, with 2<sup>nd</sup> order harmonic currents in the converter arms suppressed. During the dc short circuit fault, significant overlap is observed between the upper and lower arm, which is caused by large arm inductances and transformer leakage inductances (these overlaps indicate short periods of simultaneous conduction of the upper and lower arms of the same phase-leg). Figure 10(d) shows current waveforms in the switches  $S_2$  and  $S_6$ , which are exploited for generation of zero voltage level at each cell during normal operation, and to share the current stress when the converter is blocked during pole-to-pole dc short circuit fault. In this illustration, the on-state resistance for the diodes of the composite switches  $S_2$  and  $S_3$  are deliberately set to be 90% of that of the  $S_5$  and  $S_6$  to mimic the potential mismatch in the typical semiconductor switches may be employed (see data sheet of IGBT T1800GB45A for on-state resistance). Observe that the arm current is shared well between the parallel paths provided by the diodes of the switches  $S_2$  and  $S_3$ , and  $S_5$  and  $S_6$ . This clearly supports the case for elimination of the thyristors being used in HB cell in Figure 3(c) to relieve diodes of the main switches that bypass the cell capacitors from excessive overcurrent during dc short circuit fault. Figure 10(e) presents current waveform in the switch  $S_1$ , which is in series with capacitors  $C_1$  of each cell. Observe that the current in this switch has dropped to zero when the converter is blocked as expected (no discharge of the cell capacitor). Figure 10(f) shows phase ‘a’ cell capacitor voltages remain balanced in the pre-fault condition and **flat** when the converter is blocked during a fault period. The above discussions show that the MMC that uses the proposed cell retains all the attributes and adheres to the same fundamental equations that describes the steady-state and dynamic operation of the HB-MMC, while offering higher efficiency than HB-MMC and eliminates the unidirectional current sharing thyristor being used in the HB-MMC.



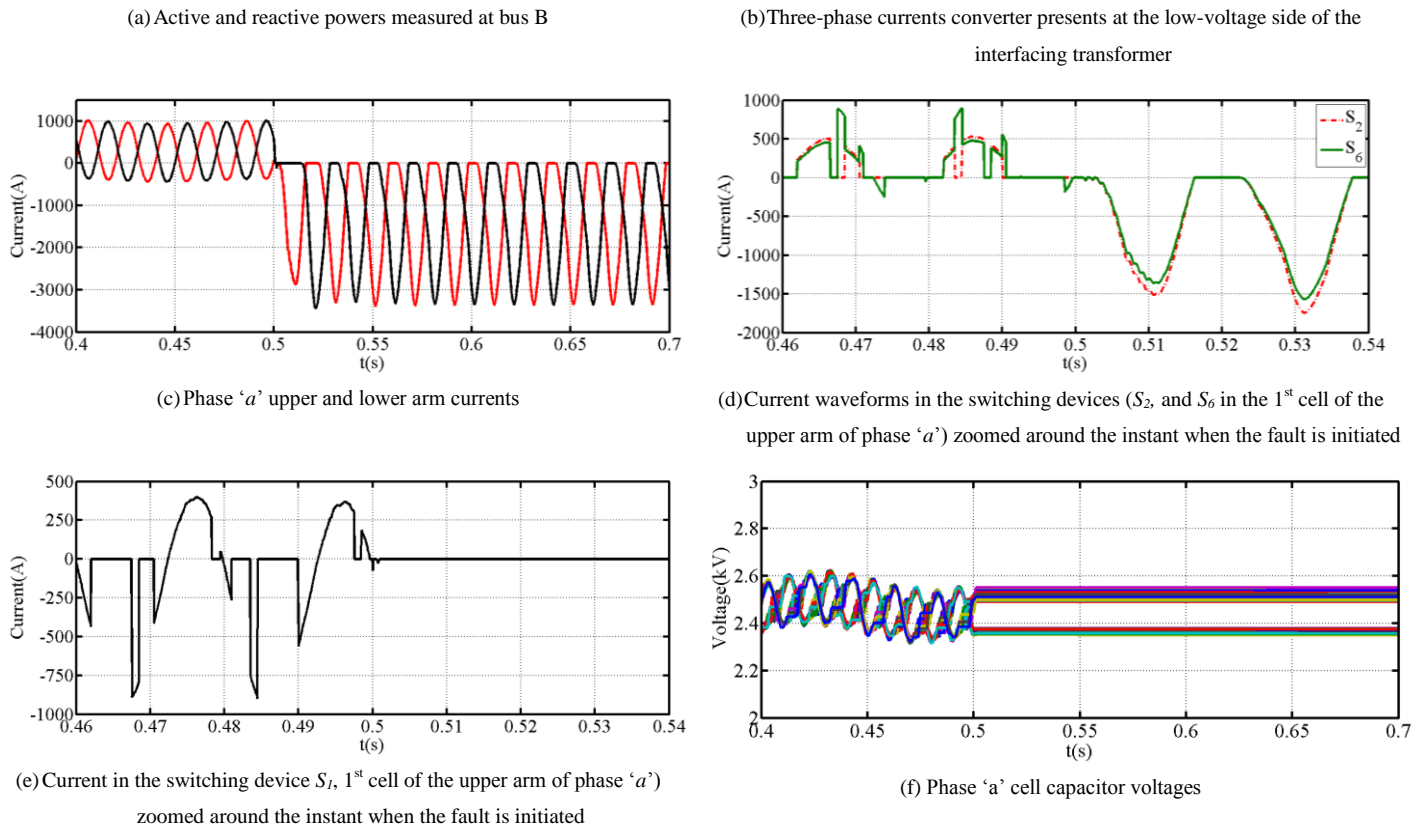


Figure 10: Selected waveforms illustrate behavior of the proposed MMC during a pole-to-pole dc short circuit fault

### B) Continued operation with multiple cell faults

Figure 11 shows some of the possible switching restrictions that would be applied to facilitate continued converter operation during cell capacitors failure or switching devices open circuit faults, depending on the exact fault location. For example, the fault scenario depicted in Figure 11(a) necessitates full bypass of the presented cell (two voltage levels will be lost per affected cell), while any of the other fault scenarios in Figure 11(b) and (c) could restrict the number of voltage levels to be generated to two ( $V_c$  and 0, should  $V_{c2}=V_{c1}=V_c$ ), with one switch state available for generation of each voltage level (loss of one voltage level per affected cell). In these two fault scenarios, the switch state in Figure 11(a) could be used to generate zero voltage at reduced semiconductor loss. Figure 11(d) and (e) summarise examples of switch open-circuit faults that do not affect the number of voltage level each cell could generate, and limit number of possible ways to generate voltage level ' $V_c$ ' to one. Additionally, these fault scenarios' do not permit generation of '0' voltage level at reduced losses. Figure 11(f) displays simultaneous fault scenario in the switches  $S_5$  and  $S_6$  that will make the faulty cell incapable of generating voltage level ' $V_c$ ', and as a result the affected cell could be reconfigured to operate as two-level unipolar cell capable of generating 0 and  $2V_c$ . When large numbers of cells suffer from this type of simultaneous fault, all cells in the affected phase leg could be reconfigured as stated above, without any sacrifice to maximum fundamental output voltage that could be generated. For illustration of internal fault management of the proposed cell, a hypothetical case that assumes cells 6 and 7 in the upper arm of phase 'a' of the test system in Figure 9 are subjected to open circuit fault scenarios depicted in Figure 11(c) and (b) at  $t=0.25s$ , and at  $t=0.5s$ , cell 4 in the lower arm of phase 'b' is subjected to simultaneous open circuit fault scenario in Figure 11(a). In the pre-fault condition, the test system being studied injects 64MW into the ac grid at unity power factor, with its power set-point unchanged when some of its cells fail as stated earlier. The following simplifications are assumed during implementation of the internal fault management, which are summarised as follows:

- 1) Fault location and type are detected instantly; thus, a fault management scheme for affected arm is enabled immediately.
- 2) Information of fault location is used to identify the affected and unaffected cell capacitors; hence, status vector ( $\Psi$ ) for the affected arm that contains zeros and ones is generated, with zeros and ones pointing to the locations of the unaffected and affected capacitors within each cell in the faulty arm. For an MMC with  $n$  cell capacitors, and  $M$

faulty cell, status vector is  $\Psi_i = \delta(i-k)$ ; where,  $\delta$  is Dirac function and it is defined as  $\delta(i-k) = 0 \forall i \neq k$  and  $\delta(i-k) = 1 \forall i = k$ ;  $i = 1$  to  $n$ ; and  $k$  is natural number stands for location of faulty cell.

- Each affected capacitor ( $C_i$ ) is omitted from the group of capacitors to be selected to synthesize different output voltages by setting its corresponding capacitor voltage  $V_{ci} = 2 \times \max(V_c)$  for  $i_{arm} \geq 0$  and  $V_{ci} = 0.5 \times \min(V_c)$  for  $i_{arm} < 0$ ; where,  $V_c = \{V_{c1}, V_{c2}, \dots, V_{cn}\}$ .

Based on the outlined points, the gating signals for the switching devices of the faulty cells are modified.

Figure 12 shows simulation waveforms for the fault scenarios described above. These waveforms indicate that the MMC which uses the proposed cell can manage its internal cell faults safely as that in the HB-MMC case. Simulation waveforms for the hypothetical case presented in Figure 12 (time for fault detection and needed for activation of the fault management are assumed to be infinitesimal) show no evidence of transients in the arm or output phase currents when partial bypass of cells 6 and 7 are initiated at  $t = 0.25$ s, and complete bypass of the cell 4 is activated at  $t = 0.5$ s, see Figure 12 (a), (b) and (f). Current waveforms measured in the switches of the cell 6 and 7 in the upper arm of phase 'a' and of the cell 4 in the lower arm of phase 'b' in Figure 12 (c), (d) and (e) show seamless partial or complete exclusion of the faulty section of the cells, with the voltage across the affected capacitors remaining unchanged, avoiding any catastrophic outcome that may result from incorrect switching of the affected cells. The above discussions show that the MMC that uses the proposed cell is able to fully or partially bypass the faulty cells, without the need for mechanical bypass switches to be installed in each cell required as in the conventional HB cell.

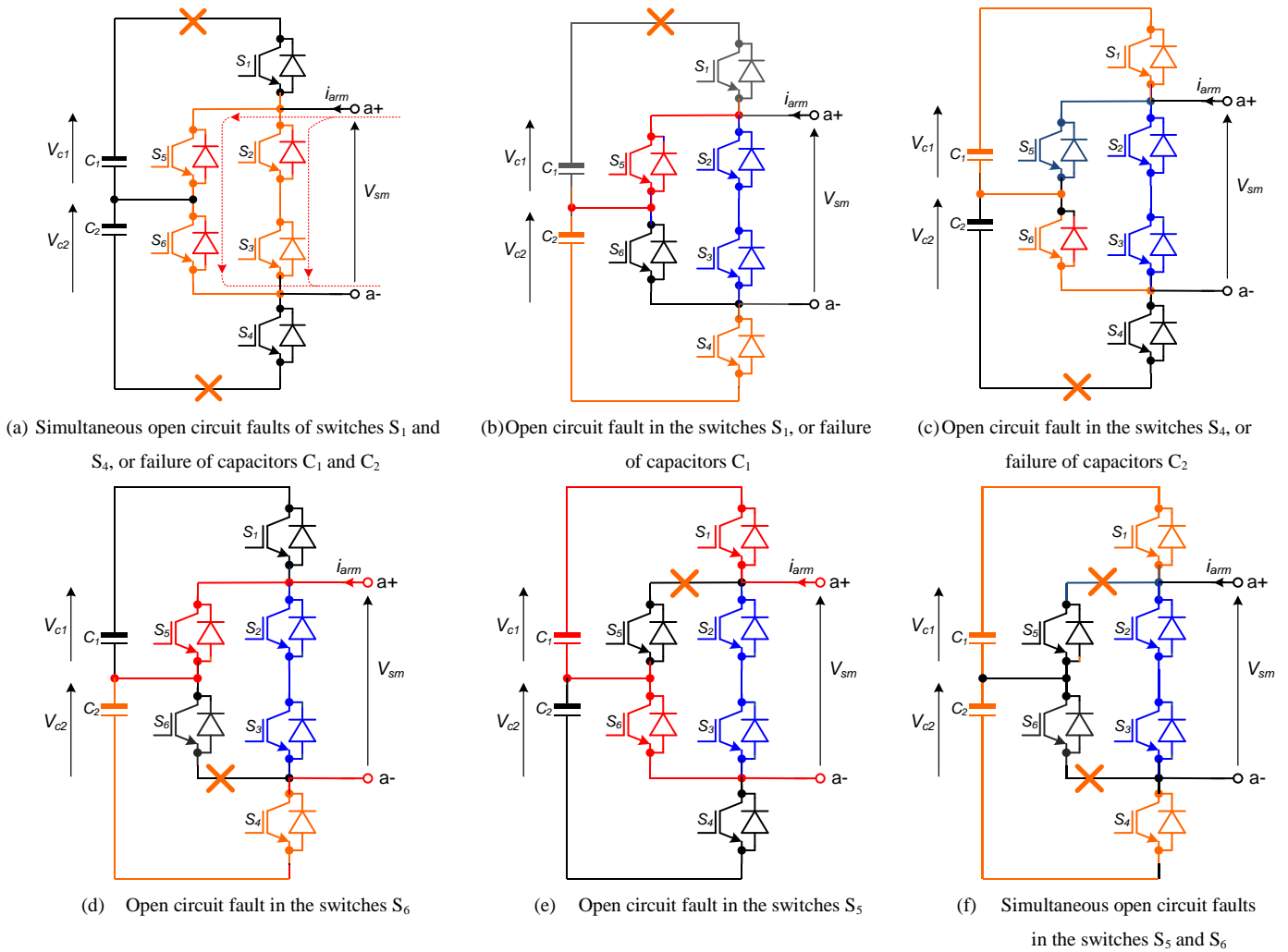
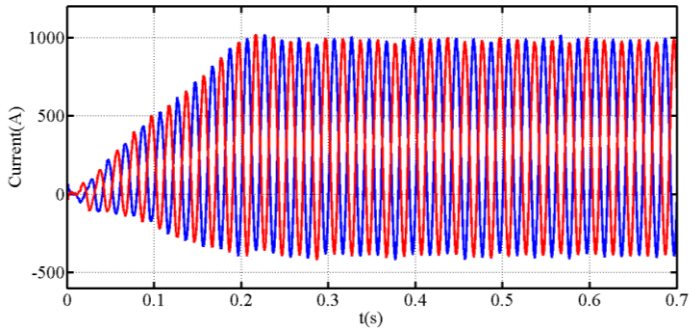
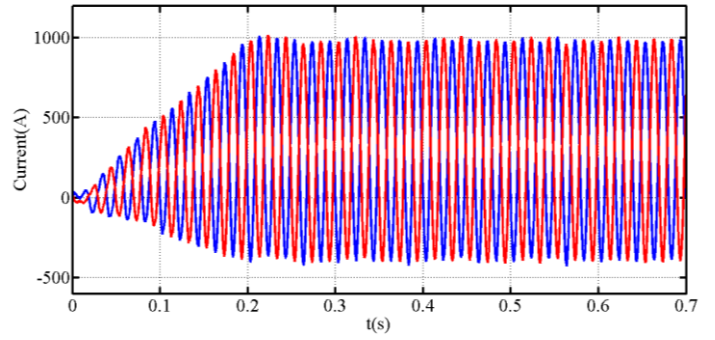


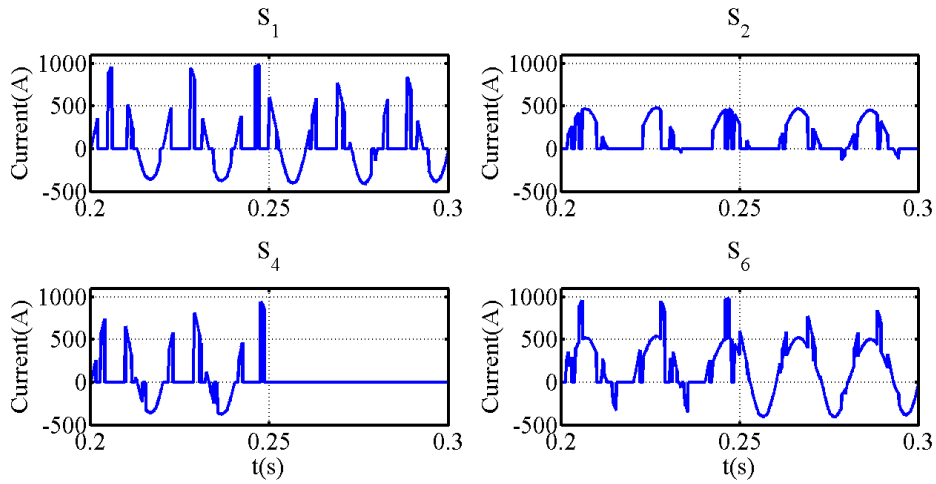
Figure 11: Examples of exploitable switch states to facilitate partial or full bypass of the faulty cells and continued converter operation during switch devices open-circuit faults or cell capacitor failures



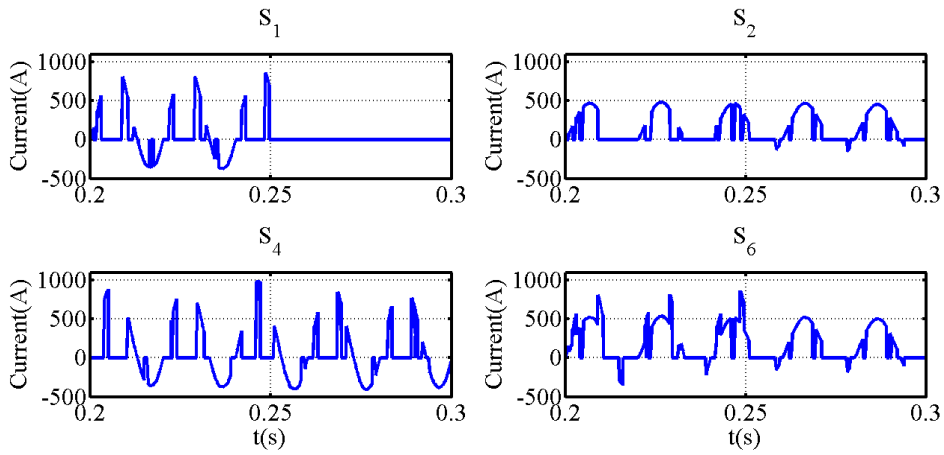
(a)Phase 'a' upper and lower arm currents



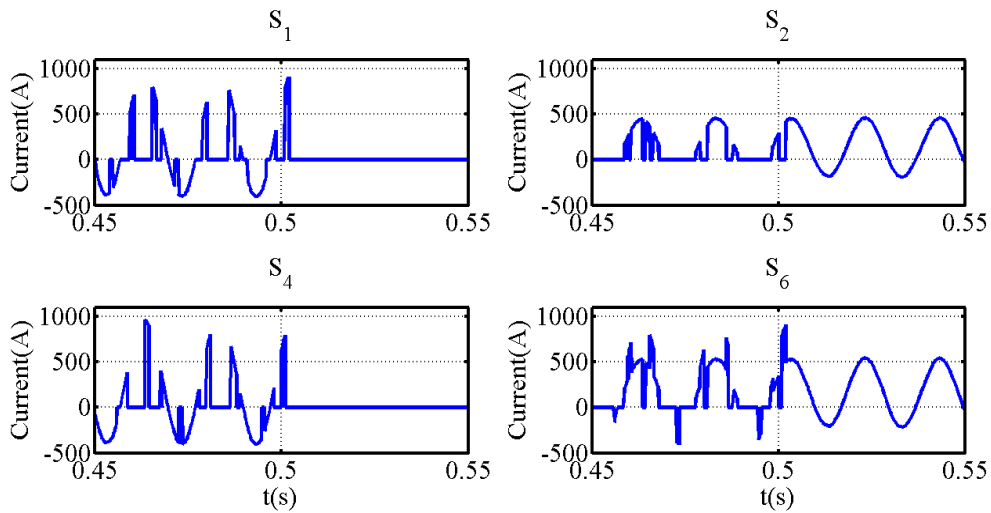
(b)Phase 'b' upper and lower arm currents



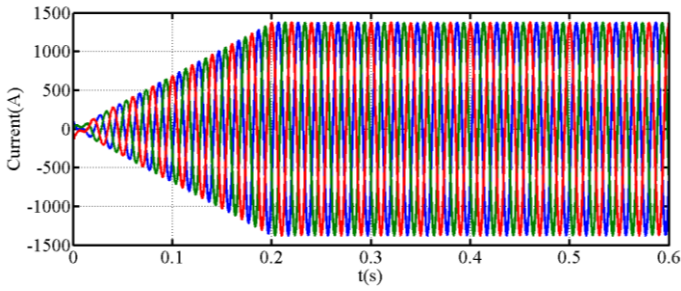
(c)Current waveforms for the Cell 6 in phase 'a' upper arm (Switches  $S_1, S_2, S_4$  and  $S_6$ )



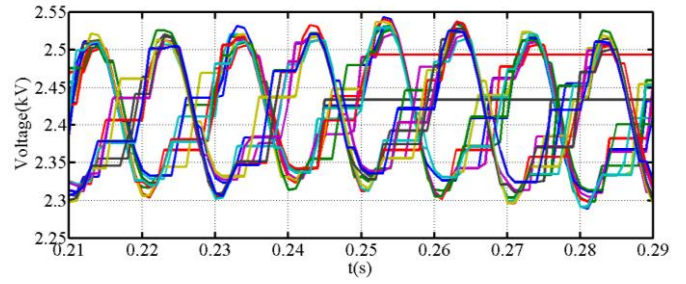
(d)Current waveforms for the Cell 7 in phase 'a' upper arm (Switches  $S_1, S_2, S_4$  and  $S_6$ )



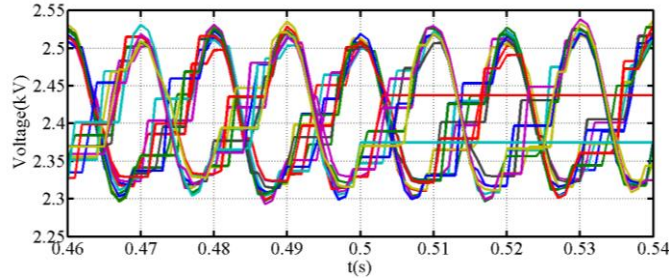
(e)Current waveforms for the Cell 4 in phase 'b' lower arm (Switches  $S_1, S_2, S_4$  and  $S_6$ )



(f) Three-phase output current



(g) Samples of phase 'a' upper and lower arm cell capacitors

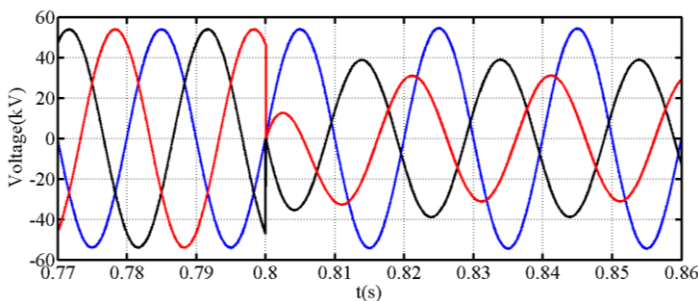


(h) Samples of phase 'b' upper and lower arm cell capacitors

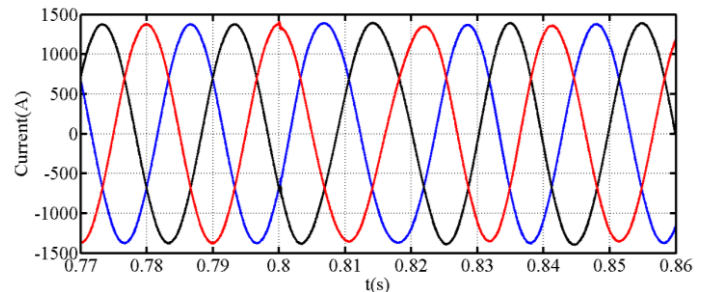
Figure 12: Waveforms illustrate easy of internal fault handling in the proposed cell

### C) Unbalanced operation

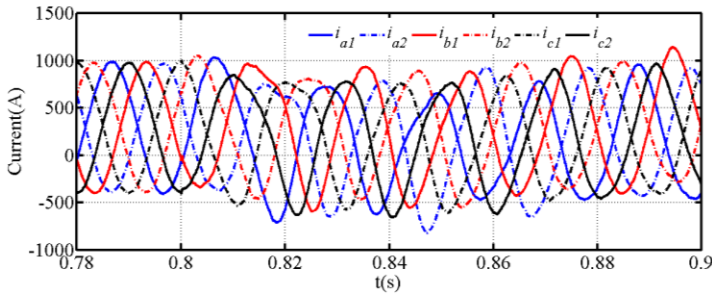
This section examines the performance of the MMC that adopts the proposed cell during unbalanced operation initiated by deliberate connection of  $1.2\Omega$  and  $0.8\Omega$  resistors between phase b and ground and c and ground at  $t=0.8s$ , and results for this case are displayed in Figure 13. Figure 13(a) and (b) display three-phase voltages measured at bus B and currents at converter terminal (measured at the low-voltage side of the interfacing transformer). Observe that although three-phase voltages at the grid side are severely unbalanced, the currents the converter injects exhibit limited unbalance as expected. The plots for upper and lower arm currents in Figure 13 (c) and (d), common-mode currents in Figure 13(e) and dc link currents in Figure 13(f) show no penetration of 2<sup>nd</sup> order harmonic into the dc positive and negative dc link currents, with the 2<sup>nd</sup> harmonic currents in converter arms suppressed. These are achieved with the conventional decoupled controller of the positive sequence currents in frame, and resonance based controller for 2<sup>nd</sup> harmonic suppression in converter arms. The plot for the common-mode currents in Figure 13 (e) indicates that each converter phase contributes unequal dc currents to the dc link current ( $I_{dc}$ ), and this in contrary to some of the control methods in the literature that advocate dc current balancing, which may lead to overcurrent of the phases that experience larger voltage depressions. The above discussions indicate that the MMC with the proposed cell could operate satisfactory under unbalanced condition as HB-MMC.



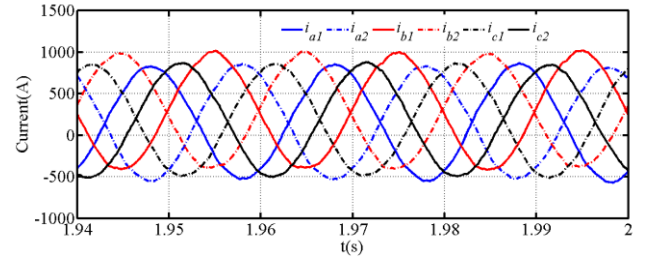
(a) Three-phase voltages measured at B



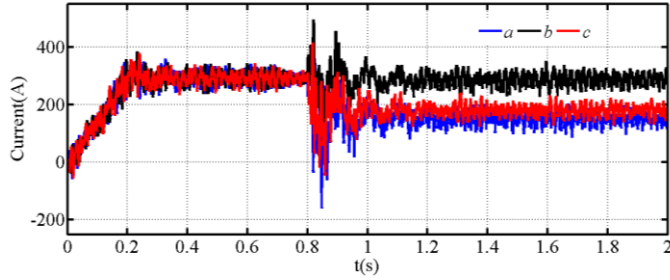
(b) Three-phase currents at converter terminal, measured at the low-voltage side of the interfacing transformer



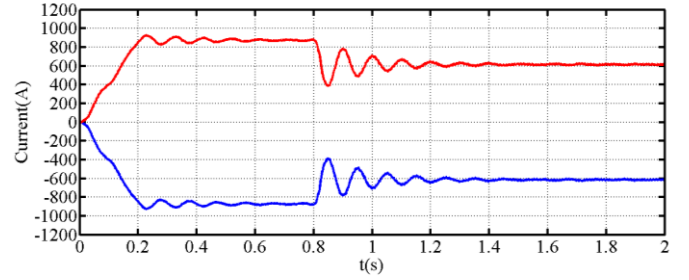
(c) Upper and lower arm currents of the three phases, zoomed around transition between balanced to unbalanced condition



(d) Upper and lower arm currents of the three phases during new steady-state when system operates under unbalanced condition



(e) Common-mode currents of the three phases,  $\frac{1}{2}(i_{a1} + i_{a2} + i_{b1} + i_{b2} + i_{c1} + i_{c2})$



(f) Positive and negative dc link currents

Figure 13: Waveforms that illustrate the performance the MMC that employs the proposed cell during unbalanced condition

## VI. BRIEF COMPARISON HALF-BRIDGE AND PROPOSED CELL

Table 8 summarizes the main similarities and differences between the HB and the proposed cell in Figure 3 (c) and (b), assuming that both cells use semiconductor switches with similar voltage and current ratings, and two HB cells are equivalent to one of the proposed cell in Figure 3 (b). Table 8 shows that both cells being compared have similar semiconductor areas, with the proposed cell in Figure 3 (b) offering the best overall performance and utilization of these semiconductor devices.

Table 8: Global comparison between the proposed cell in Figure 3(b) and equivalent half-bridge cells in Figure 3(c)

	Half-bridge cell	Proposed cell
Number of IGBTs	4 (per two cells)	6 (per cell)
Number of protective thyristors	2 (per two cells)	0
Number of bypass switches	2 (per two cells)	0
Number cell capacitors	2 (per two cells)	2 (per cells)
Devices dedicated for handling dc fault current converter is blocked during dc short circuit	Freewheeling diodes of switches $S_2$ and $S_4$ , and thyristors $T_1$ and $T_2$	Freewheeling diodes of switches $S_2$ , $S_3$ , $S_5$ and $S_6$
Internal fault management should one or limited number of cells fail	Bypass switches	Switches $S_2$ , $S_3$ , $S_5$ and $S_6$
Power loss distribution	Switching devices $S_2$ and $S_4$ that generate zero voltage states dissipate more losses than $S_1$ and $S_3$	Better than HB cell as the semiconductor losses in the main switches that generate '0' voltage level are distributed between $S_2$ and $S_3$ , and $S_5$ and $S_6$ .
Semiconductor loss	low	Lower than HB cell, see Table 5
Number of isolated dc-dc converter for gate drives	2 (per two cells)	1 (per cell)
Dynamic response	good	The same as HB-MMC

## VII. CONCLUSIONS

This paper presents an alternative cell arrangement that uses its zero voltage level to reduce semiconductor losses of modular type converters to less than that of the HB-MMC, should the two additional IGBTs incorporated into the propose cell (instead of two protective thyristors in equivalent HB cells) are utilized as described above. The same IGBTs being used to reduce



semiconductor losses could be exploited to bypass the faulty cells during internal converter faults; thus, making the use of mechanical bypass switch redundant. The presented simulation and experimental results show that the MMC which uses the proposed cell inherit all the attributes of the HB-MMC, including internal fault management; scalability to high-voltage applications; and transient performance during ac and dc network faults. The viability of the proposed cell arrangement at device and system levels is confirmed using simulations.

## VIII. APPENDIX

This appendix presents a flow chart that summarises implementation of the method II, which is employed to perform capacitor voltage balancing in this paper.

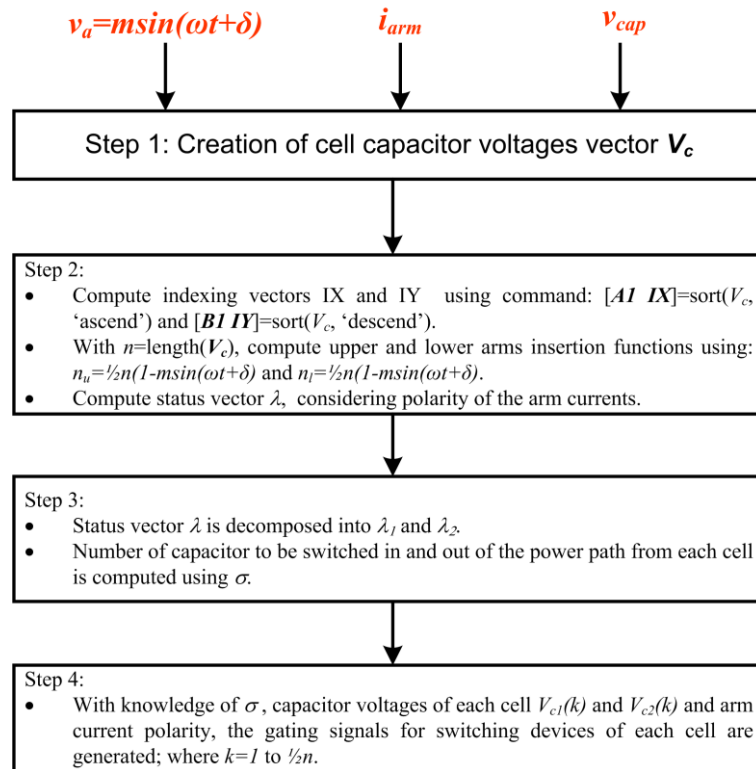


Figure 14: Flow chart that summarises implementation of method II of the capacitor voltage balancing which is employed in this paper

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