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Precise Multi-Channel Timing Analysis System for Multi-Stop LIDAR Correlation

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***Abstract*—The development of single photon applications has led to significant research into high-precision timing analysis systems. The requirement of precise time-of-flight measurements, as well as the removal of ambient/dark photon noise has been a driving force in the development of systems which provide a precise timing resolution. The proposed system aims to compute time-of-flight single photon measurements for a Multi-stop Light Detection and Ranging (LIDAR) experiment. This involves precisely computing time-of-flight between an emitted START signal and multiple photon reflections corresponding to STOP signals within a Field Programmable Gate Array (FPGA). The aim of this system is to time-tag photon counts from multiple single photon detectors with a resolution in the tens of picoseconds, where correlation computations are performed in hardware to determine time-of-flight between START and STOP signals. The developed system showed an 8-channel multi-stop timing analysis system and achieved an average resolution of 21.5 ps, with a measurement error of 20 ps FWHM. The number of STOPs that can be detected by the system is determined by the deadtime and dynamic range of the TDC. In our design the dynamic range is 2.14 s and the deadtime for each TDC block is 8 ns. From the tests conducted on the time-tag correlator, the capability to record 120 STOPs has been observed.**

***Index Terms*—Timing Measurement, Multi-Stop Measurement, Time-to-Digital Converters, Light Detection and Ranging**

I. Introduction

Precise timing measurement tools are essential to many science and engineering applications. Time-to-digital converters (TDC) are commonly used in fields such as robotics, automotive, physics and medicine. TDCs are essential timing measurement tools which provide a digital representation of time, where time is represented by a system clock period.

TDCs are commonly employed as correlation tools in applications such as LIDAR. In a single stop LIDAR, a START signal corresponds to the time when the laser transmitter starts to emit photons to the target and the STOP signal determines the detection of reflected photons from the target by the receiver. The photon time-of-flight can be used as a measure for range-finding. However, in applications such as ranging through fog, many noise photons return from the environment and weak returns from more distant objects would be suppressed in a single stop system - thus, potentially leading to errors in measurement. In order to overcome this problem, multi-stop measurements are preferable.

Asynchronous logic elements, such as carry chains located in CMOS chips, are commonly used for high resolution TDC implementations. Carry chains are used to create a delay-line structure to divide a clock period into sub-divisions for fine timing measurement. This allows for measurements at a higher resolution than that of a system clock period. This type of TDC would provide a time stamp for the event with respect to reference clock. TDCs which digitise events with respect to reference clocks are called flash TDCs. Picosecond resolution can be achieved with this type of implementation as described in [2],[6],[9]. The explanatory diagram for the tapped delay line based TDC is shown in figure 1.

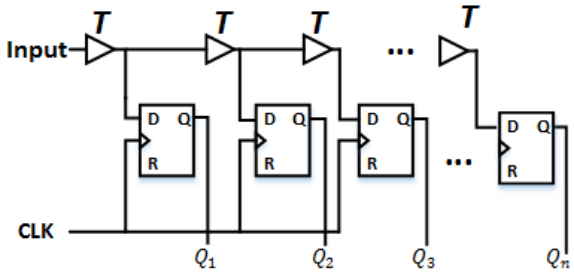

Fig. 1: *An example of an n-stage Tapped Delay Line*

The illustration of waveforms for the tapped delay line can be seen in figure 2.

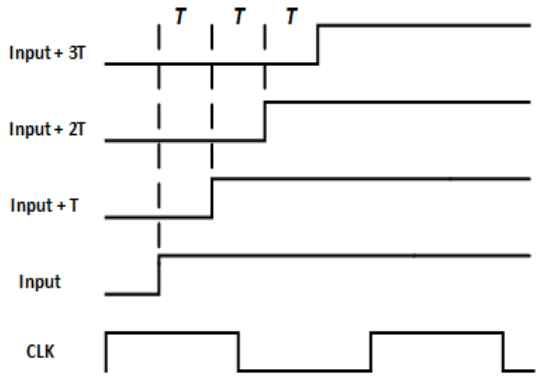

Fig. 2: *Illustration of input at each delay element in a delay line*

In multi-stop measurements, the transmitter sends photons to the target many times and the hits of both correlated and uncorrelated photons are detected by the receiver. Over many runs the histogram of time stamps for photon hits is accumulated, and from this the distribution of correlated photons will be distinguished from the background noise. For

such implementation schemes, a Multi-Stop TDC which can generate time stamps for many STOP signals with respect to one START signal is required.

Although fine interpolation improves the resolution of the TDC, it has limited dynamic range. In order to improve the dynamic range whilst keeping the timing resolution high, the hybrid interpolation scheme, Nutt Interpolation, as described in [8] is commonly used. In this method, the sequencing of events is characterised with the coarse counter, while the measurements respective to the clock period are measured by the fine interpolation scheme. An illustrative diagram for such a scheme is shown in figure 3; where the time interval between T_{Start} and T_{Stop} is computed from coarse and fine timing measurements.

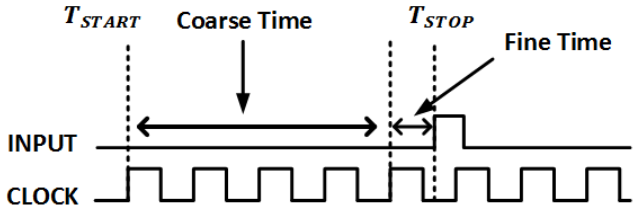

Fig. 3: *Illustration of Nutt Interpolation*

In an ideal time-to-digital converter, each delay element that is used for time quantisation should have equal bin widths. However, due to the internal routing of the FPGA chip, temperature and power fluctuations, delay-line based TDCs suffer from non-constant bin widths. This non-linearity across the TDC leads to missing codes at the output of the TDC. In order to improve the linearity, calibration schemes such as the sliding scale technique [7], code density testing calibration [3] and wave union launcher [10] can be used.

In brief, we developed a 8-channel multi-stop TDC for multi-stop LIDAR applications which is implemented within a field-programmable gate array (FPGA). The TDC is based on a 512-bin tapped delay line structure with hardware based calibration to improve linearity. Details about the implementation can be found in Section II. The results achieved from testing can be found in Section III. Finally, section IV concludes this paper.

II. System Architecture

Previously, a CMOS based TDC has been designed for LIDAR sensors system-on-chip (SOC) as described in [1]. This implementation was using the sliding scale calibration technique and achieved 52 ps resolution. However, the linearity and resolution could be improved further with different calibration schemes such as code density testing [3] and some high-speed field programming gate array (FPGA) fabric to provide a finer quantisation of time.

Another similar Multi-Stop TDC has been designed by RoentDek Handels GmbH[4]. Their design consists of 4 high resolution Multi-Stop TDC channels. The resolution of the least significant bit resolution is set to 13 ps while the average resolution is at 30 ps also design provides 5 ns dead-time. Additionally, the software based TDC calibration is available on the design. The one of the drawbacks of this design is usage of Xilinx Virtex 6 which increases the cost of the product. Also better resolution could be achieved with a cheaper chip such as Xilinx Spartan 6. Another disadvantage of this design is it only provides 4-channels but, 8 to 32 channel TDC designs are commonly needed in many applications. Software based calibration is also a limitation since on the fly calibration is needed in cases where TDC is needed to be adaptive to change in temperature without long calibration times.

In addition, a commercial TDC chip TDC7200 has been designed by Texas Instruments to achieve similar multi-stop TDC operation [5]. This design provides 2 channel Multi-Stop TDC that provides an average resolution of 55 ps whilst dynamic range is up to 8ms. This product aims to provide cheaper solution to needs of time of flight applications. However, only having 2-channels and limited resolution seem to be the main drawbacks of this design.

The proposed architecture consists of an array of 8 TDCs, each with a unique hardware calibration block, and one multi-channel tag correlator block which calculates the absolute difference between the time-stamps of START and STOP signals. The pre-defined channel 1 is assigned as the reference channel whose tags are designated as START events.

A. Time-to-Digital Converter

A TDC based on a 512-stage delay-line structure has been implemented with primitive carry chains structures, which are commonly used for arithmetic operations in the FPGA. This implementation has been done on a Xilinx Spartan 6 LX150 FPGA which was located on an Opal Kelly XEM6310 board. The coarse counter is run by a 125 MHz clock generated by using the Xilinx Clocking Wizard. These coarse counters provide a timing resolution of 8 ns. For the coarse counter, 28 bits are assigned within the time-tag for sequencing. The clock period of 8 ns spanned over 372 delay-elements within the TDC, thus, providing an average TDC bin width of 21.5 ps, whilst the least significant bit resolution of a tag was set to 1.95 ps.

The least significant bit (LSB) of the code can be expressed as below :

$$LSB = \frac{T_{Clock}}{2^N} \tag{1}$$

where T_{Clock} is the clock period and N is the number of bits reserved for fine quantisation. When the 8 ns clock period and the 12 bit is substituted into the formula given above the LSB of the TDCs code can be calculated as below:

$$LSB = \frac{8 \times 10^{-9} s}{2^{12}} = 1.95\ ps \tag{2}$$

The 512-bit thermometer code generated from the delay-line is transformed by the priority encoder into 9-bit raw code. Later this 9-bit is used to address a linear fine-time within the calibration block. A 28 bit coarse counter value, 12 bit fine time value and 8 bit channel identification tag are concatenated to form the final time stamp. This is done by subtracting the

fine tag from the next clock edges coarse counter value. In total, a 48 bit time tag is generated by the TDC. The diagram for the tag formation can be found in figure 4.

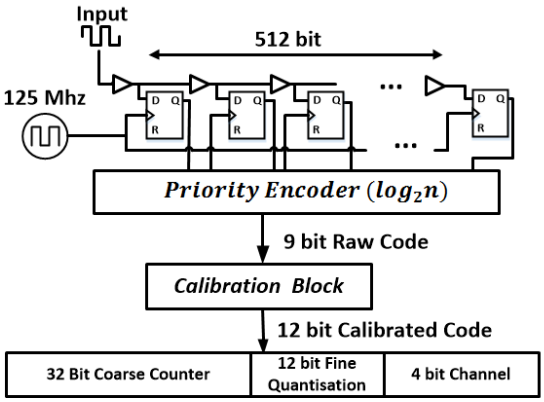

Fig. 4: *Illustration of tag formation from TDC scheme*

B. Calibration of Time-to-Digital Converter

The use of a delay-line structure for fine timing measurements leads to issues with non-linearity between delay elements. This is caused by the mapping of the structure into FPGA hardware, as well as variations in propagation delay characteristics caused by temperature. This results in non-linear sub-divisions of the system clock period represented per delay-element.

The issue of non-linearity is primarily due to the layout of carry elements within the FPGA fabric. The delay-line structure is designed by utilising Carry4 hardware primitives, which consist of 4 carry elements that are instantiated using fast logic per FPGA slice. Figure 5 shows a high-level overview of how a logical hardware design is mapped into the FPGA fabric where designs are routed through the FPGA interconnect, with logical designs mapped into logic blocks.

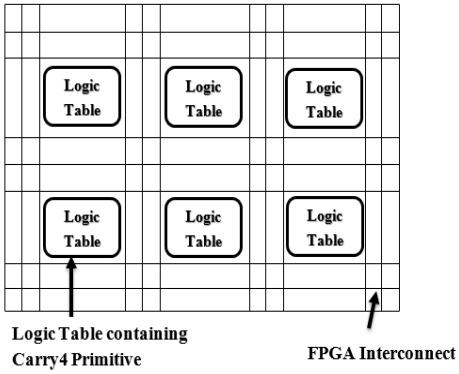

Fig. 5: *High-level overview of logical design layout within FPGA fabric*

The issue arising in the design of delay-line structures is the interconnect between each delay element. Typically, Carry4 elements are mapped into a logic block with all interconnections being mapped within the logic block. However, the output of each Carry4 primitive is routed through the FPGA interconnect to the next Carry4 element which resides in a different logic block. This leads to non-linear propagation delays represented per carry element, resulting in non-linear sub-divisions of the system clock period, as shown in Figure 6.

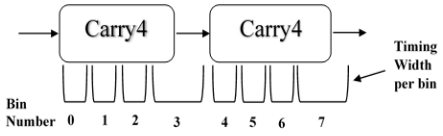

Fig. 6: *Non-linearity within delay-line structure*

To mitigate the effects of this linearity, we introduce some form of calibration at system start-up. This involves utilising a signal input to the system which is orthogonal to the system clock. Assuming a perfectly linear delay-line structure, we would expect an even distribution of counts amongst bins (white Gaussian noise). However, the experiment highlights the result of this non-linearity where we see specific bins having a larger propagation delay, and therefore counts having a higher probability of landing currently in specific bins, as shown below in Figure 7.

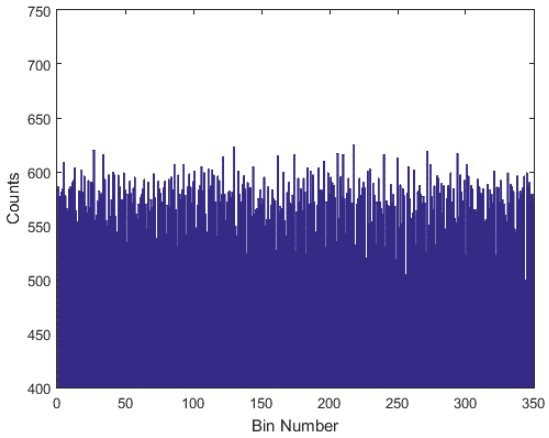

Fig. 7: *Distribution of counts across delay-line*

To calibrate the system, we can input a set number of counts with a trigger orthogonal to the system clock, and statistically analyse the distribution of counts amongst bins. The system utilises an FPGA Block RAM (BRAM) to store the statistical distribution of counts across the delay-line per TDC channel. The system cumulatively sums the distributed counts across the delay-line, and stores the cumulated statistics within FPGA BRAM, as shown below in figure 8.

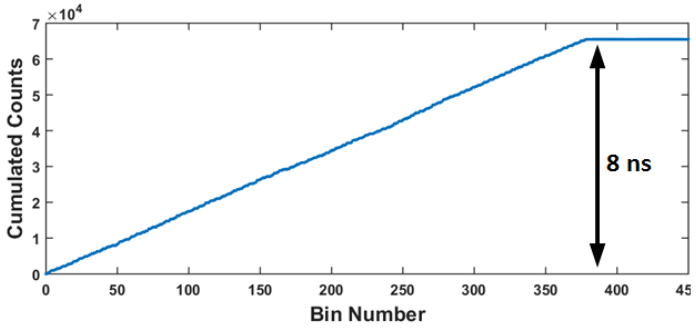

Fig. 8: *Cumulative distribution of counts across delay-line structure*

The fine-time represented as a sub-division of the system clock period can then be computed, by computing what sub-division of the system clock is represented by the cumulated counts of a specific bin in comparison to the total number of counts distributed across the delay line. This is shown by the following equation:

$$Bin\ Width = T_{clk} \times \frac{N_{cumulative}}{N_{Total}} \tag{3}$$

The resultant fine-time measurements per bin can then be stored as a look-up table in the FPGA Block RAM; therefore, when a count is incident on the system, the bin number is used to index the Block RAM to return a calibrated value of fine-time. This process is repeated at system start-up, as both the FPGA-mapped design layout and surrounding temperatures affect the propagation delay.

C. Multi-Channel Tag Correlator

The Multi-channel tag correlator is a required module for calculating the delta time between a START signal and multiple STOP signals. In this module, concurrently generated tags across the 8 channels are serialised, and time differences between one START and multiple STOPs are calculated.

The design consisted of 8 Flash TDC blocks which run concurrently. Since all Flash TDCs share the same system clock (and hence synchronized coarse counter), subtracting time-tags of START and STOP signals, gives the absolute timing difference corresponding to time-of-flight.

The block diagram of the system is shown in figure 9.

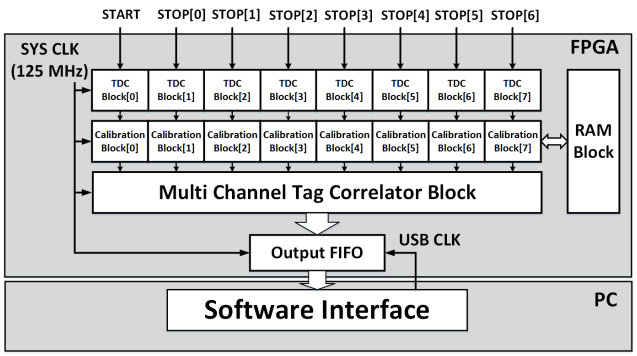

Fig. 9: *The block diagram of the system*

When finding the delta time between the START and STOP signals, one channel is chosen as a reference channel whose tags are used as START signals. When a tag is eived from a STOP channel, it is subtracted from the START signal and the difference is stored as the delta time and sent to the PC for processing.

This operation consists of five different stages. These stages are initialisation, idle, set, calculation and send. Initialisation of the system is required to prevent any calculation that could be done until the TDC block is completely calibrated. During this stage no result is calculated and the FPGA does not output anything to the PC.

After the calibration of the TDC has completed successfully, the system stays idle and waits to process any subsequent time tags received from the TDC modules. The reference channel is predefined in the design, thus it does not change during the operation. When a new tag is received, the tag is checked to determine the source channel. According to the channel identifier bits of the tag, the correlator decides about the next operation. If a tag for a START signal is received, the next operation changes the reference tag with the recently received tag. Once the reference tag is updated, the system becomes idle again. If a STOP signal is received, then the systems proceeds to a calculation as the next operation.

Since each reference signal is constant, the delta time calculation can be expressed like below:

$$\Delta_n = (T_{STOP_n} - T_{START}) \tag{4}$$

The explanatory diagram for the delta time calculations of the tag correlator can be seen in figure 10.

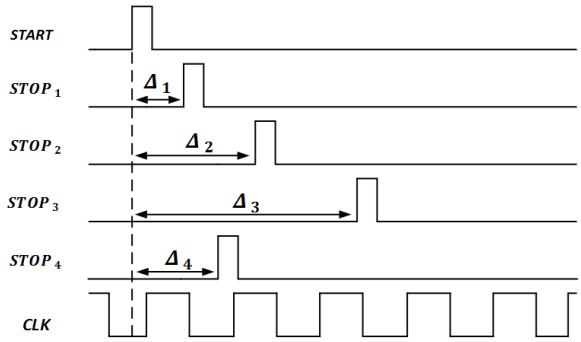

Fig. 10: *Illustration of delta time measurement for multiple stops by the tag correlator*

The delta time between the START and STOP signals is computed in the calculation step. This is done by subtracting the tag corresponding to STOP from the reference tag, which is the most recent START tag. Since tags are generated with a flash TDC, each input signals tag is generated relative to their position according to system clock edge and common coarse counter which continuously counts at the rising edge of the system clock. Thus, subtracting the tags at the START and STOP signals will compute the absolute time difference between them. Also, the overflow of the coarse counter is checked during the operation and required modifications have been implemented to produce the correct absolute value.

When the calculation is finished, the final stage of operation is sending the calculated results to the PC through first in first out (FIFO) buffer inside the FPGA via USB 3.0 port. The design enables writing of all calculated values into the FIFO buffer to then be transferred to the PC.

III. Results

By using the architecture discussed in section 3, a multi-stop TDC for multi-stop LIDAR sensors was successfully implemented. The LSB resolution for the TDC was set to 1.95 ps and the average resolution of the delay-line was 21.5 ps. Each TDC block can process one tag every clock period, thus the dead time for this design is 8 ns.

The timing jitter measurement has been conducted; and is calculated by subtracting of the tags generated by two separate TDC blocks fed with an identical trigger signal. The input trigger feeding the TDC blocks was set to approximately 1.057 MHz and the number of time-tags generated was approximately 140,000. From accumulating and forming the histogram from the output of the differences, the timing jitter graph has been plotted. From this test, the Full Width Half Maximum (FWHM) timing jitter has been computed to be approximately 20 picoseconds.

The results from the timing jitter measurements can be found in figure 11.

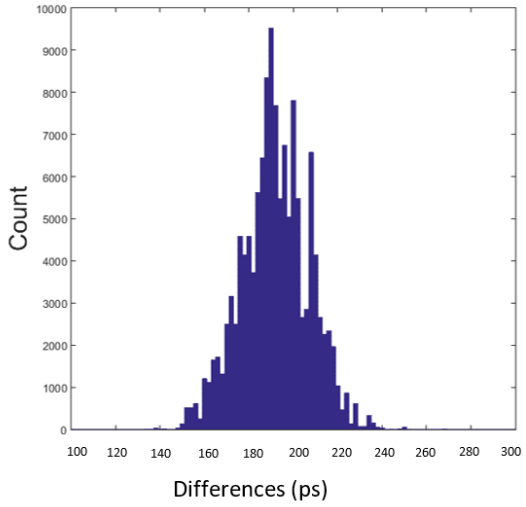

Fig. 11: *Timing jitter measurement between TDCs with identical trigger stimulus*

In order to test the performance of the multi-channel tag correlator module, an experiment setup which provides one START and a multiple number of STOPs was created. This setup provides a similar environment for multi-stop LIDAR sensors which receives a multiple number of photon hits between each START signal.

The test setup consisted of two synchronised signal generators. One generator was assigned to emulate a START signal, and the other as the STOP signal. For the first two tests, the STOP signal generator was set to 1 MHz and the START signal generator was set to 1MHz/N, where N is the required number of STOPs. For the third test, the STOP signal generator was set to 275 kHz whilst the START generator was set to 2.3kHz. The START signal was assigned a lower frequency, so when the system receives a STOP signal, the delta time between the START and the most recent STOP can be computed and sent to be accumulated on a PC for computing a histogram. Each histogram was formed from approximately 100,000 data samples.

The first test was conducted for 5 STOPs. Thus, the START signal was at 200 KHz while STOPs are generated at 1 MHz. The results for this test can be seen in figure 12.

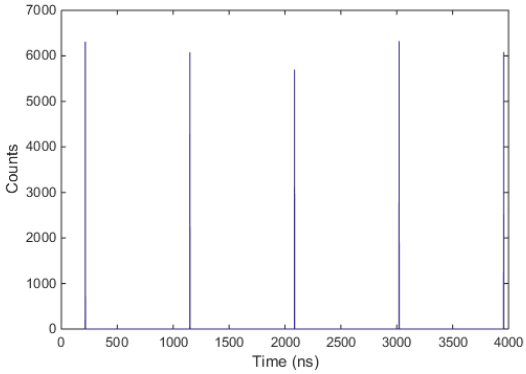

Fig. 12: *Histogram of 5 STOPs computed by the correlator*

The second test consisted of 43 STOP signals. This test also had 1 MHz clock for each STOP while START signals were given every 23.3 kHz. The results observed from this test can be seen in figure 13.

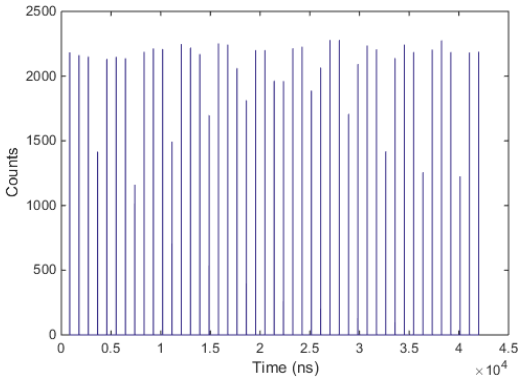

Fig. 13: *Histogram of 43 STOPs computed by the correlator*

The third test was aimed to record 120 STOP signals. The STOP signals generated at 275 kHz while the STOP signal frequency was at 2.3 kHz. Thus, the results are obtained as in figure 14.

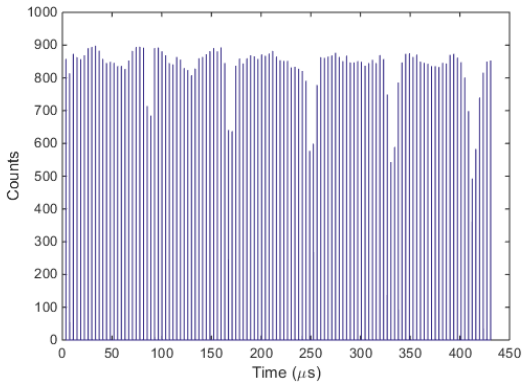

Fig. 14: *Histogram of 120 STOPs computed by the correlator*

These tests show that the multi-stop TDC is capable of registering the events clicking arbitrary times between two START signals. The number of STOP signals that can be detected from one channel is limited to the dynamic range of the design and the dead time of each channel. It should be noted that since the largest number that can be represented by the coarse counter is 28-bit, the longest dynamic range that this design can provide is 2.14 seconds, which exceeds the time-of-flight of any emitted single photon. This range should be sufficient for any LIDAR applications and timing analysis system would not be the limiting factor for the measurements.

IV. Conclusion

This experiment showed the development of a multi-channel timing analysis system to be used for time-of-flight measurements for LIDAR systems. The resultant self-calibrating timing analyser showed an average TDC resolution of 21.5 ps, with a single stop timing measurement error of approximately 20 ps FWHM. The system integrates a hardware-based correlation module to compute time-of-flight measurements between emitted and reflected incident photons, allowing for precise distance measurements based on photon time-of-flight.

The system was designed to be scalable in terms of handling multiple channels operating in parallel. The limitations of the number of parallel timing analysis channels is inherently limited by the FPGA area. The maximum number of channels tested within this experiment was 8, however the system could theoretically scale up to a maximum of 16 channels within the Spartan-6 LX150 FPGA.

The tag correlator module has been implemented for recording the multiple STOP events needed for the multi-stop LIDAR. The tag correlator has been tested with various number of STOP events and the largest number of test sets consisted of 120 STOPs. During these tests, the delta time between START and STOP signals has been successfully recorded by the module and a histogram of the recorded data is formed on the PC. The maximum number of events that could be recorded was determined by the dynamic range of the TDC - which is 2.14s. The system can continuously process incident photons within the dynamic range with a deadtime of 8 ns per detection.

The developed system showed successful precise time-of-flight measurement instrumentation implemented within FPGA hardware. The system is designed to be integrated into a LIDAR system, where time-of-flight measurements can be directly output from the FPGA module. The integrated hardware design eliminated the requirement for additional timing analysis software for calibrating the system and computing differences between time-stamped photon detections.

The future work of the design involves the adaptation into multiple experimental LIDAR systems and improvements in design in order to achieve better dead time. The improvement of dead time would be possible if a single delay line could be used to tag multiple trigger events within a clock period. Potential implementation would involve more complex priority encoder design which could detect the thermometer code patterns generated by the delay line when multiple hits occur within in a clock period.

V. Acknowledgments

We thank Mr. Steve Buckley from Sensl for technical email exchanges, and his comments have improved this work. We would also like to thank to Colston Research Society for the travel scholarship, they are providing.

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