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High Performance Resistance Switching Memory Devices Using Spin-on Silicon Oxide

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***Abstract*—In this paper, we present high performance resistance switching memory devices (RRAM) with an SiO_2-like active layer formed from spin-on hydrogen silsesquioxane (HSQ). Our metal-insulator-metal (MIM) devices exhibit switching voltages of less than 1 V, cycling endurances of more than 10^7 cycles without failure, electroforming below 2 V at room temperature, and retention time of resistance states of more than 10^4 seconds at temperatures up to 120 ºC. We also report arrays of nanoscale HSQ-based RRAM devices in the form of multilayer nanopillars with switching performance comparable to that of our thin film devices. We are able to address and program individual RRAM nanopillars using conductive atomic force microscopy. These promising results, coupled with a much easier fabrication method than traditional ultra-high vacuum based deposition techniques, make HSQ a strong candidate material for the next generation memory devices.**

***Index Terms*— Analog memory, atomic force microscopy, dielectric films, nanofabrication, resistive RAM, silicon compounds.**

I. Introduction

Resistance switching random access memory (RRAM) has attracted a lot of attention in recent years due to its excellent electronic properties, such as nanosecond switching time [1], high degree of scalability and low operating voltages [2]. These qualities make RRAM a good candidate for the next generation of memory devices as conventional NAND Flash technology reaches the end of the roadmap and as new classes of so-called storage class memory are developed. There have been numerous reports in the literature of materials that exhibit resistance switching, the most extensively studied of which include transition metal oxides such as HfO_2 [3], TiO_2 [4], and TaO_{2-x} [5]. Recently, however, silicon oxide (SiO_x) has also demonstrated excellent resistance switching performance [6-8]. The main advantages of using SiO_x are two-fold: first, the material is very abundant and readily available; second, it is fully compatible with CMOS manufacturing processes and materials. The most common methods for depositing SiO_x as thin film materials are sputtering, Chemical Vapour Deposition (CVD) and Atomic Layer Deposition (ALD). While these techniques are well established and the layer thicknesses are extremely controllable, they require deposition in a high vacuum environment and are multi-step processes. In this paper, we propose using a spin-on SiO_2-like hydrogen silsesquioxane (HSQ) as the active switching material, and we demonstrate fabrication of high performance non-volatile micro- and nanoscale RRAM devices using this material.

The main advantage of using HSQ from a fabrication prospective is that it can be applied onto most metallic and semiconductor surfaces by spin-coating alone at ambient conditions, hence it simplifies the fabrication process. The layer thickness can be controlled precisely by a combination of solution concentration, spin speed and spin duration. While there have been several previous reports of using HSQ in RRAM devices, the HSQ layer used in these reported works were doped with either nanoparticles or metal ions [9]. Our work is distinctively different from these previous reports as we demonstrate switching that is intrinsic to the HSQ thin film; no metal doping is required.

II. Hydrogen silsesquioxane

Since its discovery in the 1970s [10], HSQ has been commonly used in the semiconductor industry as a spin-on insulator for microelectronic devices due to its excellent planarisation performance and gap-filling properties. In the 1990s, Namatsu et. al., demonstrated that HSQ can be used as a negative tone resist for electron beam lithography [11], with feature sizes of the order of a few nanometres patterned routinely [12, 13].

The HSQ molecule has a cage structure which consists of silicon, oxygen, and hydrogen networks, and has a general formula of $(HSiO_{3/2})_{2n}$. Upon spin-coating and annealing, these cage structures open up and cross-link to form a networked structure of amorphous silicon oxide [14]. We performed X-ray Photoelectron Spectroscopy (XPS) scans on two spin-coated HSQ thin films on Si substrates to demonstrate the effect of thermal annealing. The XPS spectra

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were taken a few nanometres below the surface to ensure we measured the bulk material rather than the surface. Fig. 1(a) shows the XPS spectra in the range corresponding to the Si2p region; spectra were normalised to the same intensity. The Si2p peak for the sample annealed at 160 ºC for 2 minutes shifts to a higher energy (104 eV) compared to that of the non-annealed sample, indicating that the crosslinked (annealed) film is more SiO_2-like compared to the non-crosslinked (un-annealed) film. The XPS spectra for the same samples in the O1s region (Fig. 1(b)) shows a binding energy shift to higher energy for the annealed film. The O1s spectra were normalised to the Si peak at 99 eV, and by analysing the area under each peak, we were able to estimate the oxygen content in the annealed (crosslinked) HSQ film to be around 40% higher than in the non-annealed film.

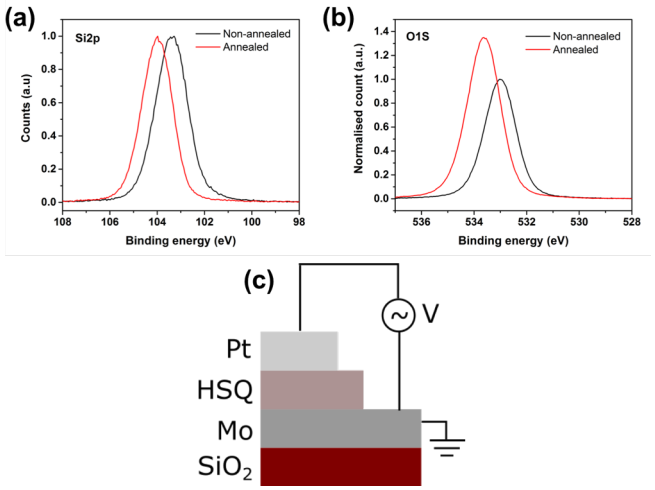

Fig. 1. HSQ thin film XPS spectra and MIM device schematic. (a) Normalised XPS spectra for the non-annealed and annealed HSQ film on Si substrate in the Si2p peak region. (b) XPS depth profile spectra for the same non-annealed and annealed HSQ film in the O1s region. These spectra were normalised to the Si peak at 99 eV. (c) Cross-section schematic of our HSQ based MIM RRAM device.

III. HSQ THIN FILM RRAM DEVICES

After establishing that the annealed HSQ film is SiO_2-like, we fabricated our RRAM devices in a two-terminal metal-insulator-metal (MIM) configuration. Fig. 1(c) is the schematic of the device structure. Devices were fabricated on a Si chip with a thermally grown SiO_2 layer on top to electrically insulate the bottom electrode of the device from the Si substrate. First, 200 nm of Mo was deposited onto the SiO_2 surface by sputtering to serve as the bottom electrode. A 35 nm thick HSQ layer was then spin-coated on top of the Mo and annealed at 160 ºC for 2 minutes. A top Pt electrode was deposited by electron beam evaporation, the size of individual devices defined using a shadow mask with device sizes ranging from 200 µm × 200 µm to 800 µm × 800 µm.

Current-voltage (IV) measurements were preformed using a Keithley 4200 Semiconductor Characterisation System, a Signatone probe station and tungsten probes.

Fig. 2(a) shows typical current-voltage (IV) characteristics of our Mo-HSQ-Pt RRAM devices. We were able to electroform the devices at voltages as low as -1.6 V. Subsequently we could tailor the low resistance state (LRS) and high resistance state (HRS) through a combination of applied bias and current compliance. For example, after setting the device to the LRS at -1.8 V with a current compliance of 1 mA, we could reset the device with +1.3 V to the HRS (Set 1 and Reset 1 in Fig. 2(a)). This gave us over 4 orders of magnitude of contrast between the LRS and HRS.

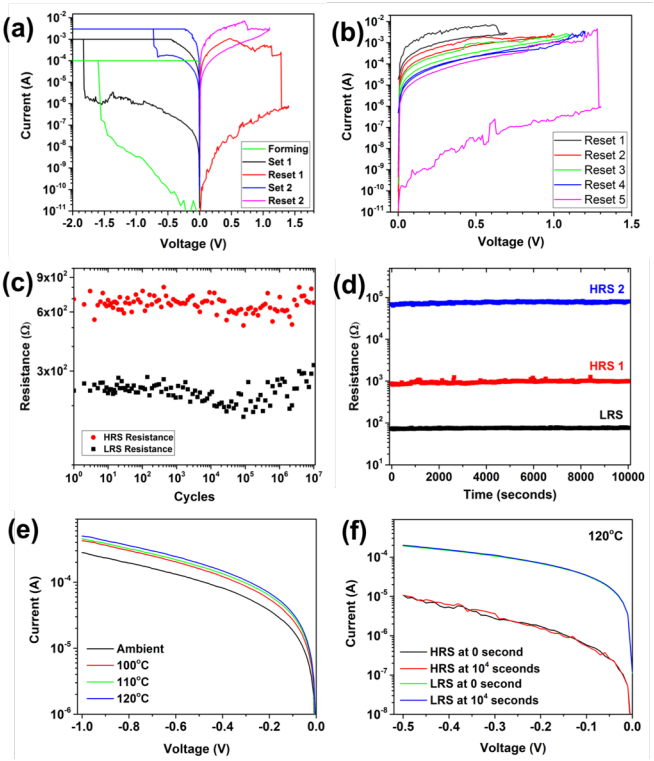

Fig. 2. Current-Voltage, cycling and retention performance of our Mo-HSQ-Pt thin film RRAM devices. (a) Current-Voltage (IV) sweep for our Mo-HSQ-Pt RRAM devices showing forming and two sets of set/reset cycles to demonstrate controllable set and reset resistance levels. (b) Gradual reset of the RRAM device with increasing reset voltage. (c) Cycling performing between LRS and HRS states showing our devices is capable of more than 10^7 switching cycles. (d) Retention performance of 3 different resistance states of our device (Read voltage 0.2V). (e) Temperature dependent IV characteristics of the LRS. (f) IV characteristics of the LRS and HRS at 120 ºC at 0 seconds (first reading after the temperature has been stabilised) and 10^4 seconds. Demonstrating the state retention at high temperature.

Note, a stronger reset process, achieved by sweeping the device to the higher positive voltages, results in higher set voltages, which could be in some cases greater than the initial electroforming voltage. Furthermore, the large drop in current for high reset voltage suggested that the device could be reset to a (near) pristine state, indicating that almost total destruction of the conductive path in the HSQ layer. However, we could lower the set and reset voltages to -0.7 V and +1.1 V, respectively, by adjusting the compliance current and still obtain over one order of magnitude contrast between LRS and HRS (Set 2 and Reset 2 in Fig. 2(a)). Fig. 2(b) shows multiple resistance states, which we could programme by performing gradual resets (gradually increasing the reset

voltage). These results demonstrate that our HSQ RRAM devices are potentially capable of multilevel bipolar switching.

We fitted the IV curves with a number of possible current transport mechanisms – trap assisted tunnelling, Fowler-Nordheim tunnelling, Poole-Frenkel hopping and thermionic (Schottky) emission. We found that the dominant transport mechanisms in our HSQ RRAM devices is trap assisted tunnelling, which is consistent with our previous reports of SiO_x RRAM [2].

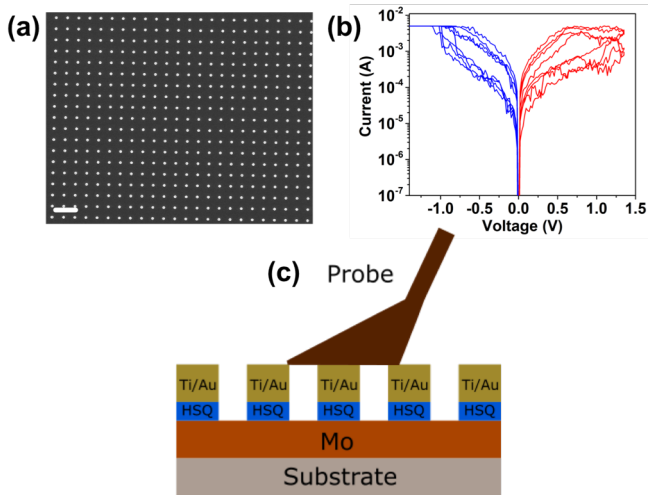

Fig. 3. HSQ nanopillar RRAM array. (a) Scanning electron microscope image of the nanopillar RRAM array showing excellent uniformity. Scale bar 3 µm. (b) Current-voltage (IV) sweeps of our Mo-HSQ-Au RRAM nanopillar array showing multiple set and reset cycles. (c) schematic of the probe needle probing the IV of a group of nanopillars.

We performed temperature dependent IV measurements for our devices (Fig. 2(e)) and our results showed that as we increase the device temperature, the LRS resistance decreases. This suggests that the switching mechanism is likely to be filamentary. We also observed no device size dependence of LRS current and this also indicates filamentary the switching. These observations are consistent with our previous reports on SiO_x based devices [15]. We are able to electroform and set our devices under negative bias (i.e. negative bias applied to top electrode), which indicates that mobile oxygen ions are pushed towards the bottom electrode (Mo) during the set process, leaving a silicon-rich channel behind. The subsequent reset under positive bias reintroduces the oxygen ions into the system, leaving the system in a higher resistance state [16].

Apart from changes in the bulk HSQ layer, chemical and structural changes at the insulator-metal (HSQ-Mo) interface under applied bias could also contribute to the switching mechanism. We are planning further work to investigate interfacial changes such as proton exchange [17, 18] and the formation of molybdenum oxide [19, 20] at the interface in order to gain a deeper understanding of the switching mechanisms in our devices.

Our HSQ-based RRAM devices showed excellent cycling performance as shown in Fig. 2(c), achieving more than 10^7 switching cycles. Note that the contrast between the two resistance states during the endurance test is lower than that shown in Fig. 2(a). This is because we used short and low-amplitude pulses for the endurance test (set pulse: -1.05 V, 150 ns; reset pulse: +1.1 V, 5 µs) to prevent significant current overshoots, as we did not use controller transistors in our set-up. We anticipate that the integration of controller transistors would allow us to use higher voltage pulses that would increase the resistance state contrast while preventing hard breakdown of devices. We have performed retention measurements for multiple resistance states at room temperature (Fig. 2(d)), and at 120 ºC (Fig. 2(f)); our devices showed excellent retention performance – up to 10^4 seconds at both ambient and elevated temperatures. These IV, cycling and retention characteristics are comparable with those we have previously reported for sputtered silicon oxide based RRAM [21].

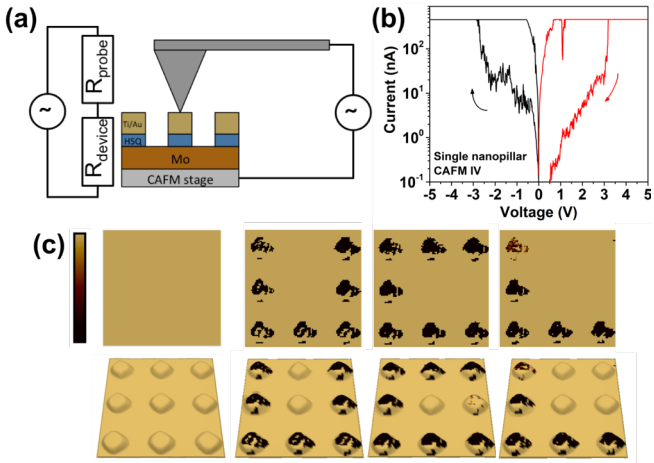

Fig. 4. Addressing individual HSQ RRAM nanopillars. (a) Schematic diagram showing the addressing of individual RRAM nanopillars (300 nm in diameter and 150 nm in height) using conductive atomic force microscopy (CAFM) technique. (b) IV sweep of an individual nanopillar, showing the set and reset cycle. (c) Demonstration of programming a 3 × 3 nanopillar array by addressing each pillar individually. Top: 2D conductivity map of the CAFM scan over a 3 × 3 nanopillar array. The far left one represents pristine state. By addressing individual nanopillars (i.e. either switching the pillar on or off), we can form the letter "U", "C" and "L" in sequence on the same array. Darker colour represents higher negative current. Bottom: 3D topography scan in contact mode after addressing the array and overlaying the image with the CAFM one. This shows there is no deformation of pillars after addressing the array. The top and bottom limits (lighter and darker colours) of the scale bar is -2 pA and -3 pA respectively.

IV. HSQ RRAM NANOPILLARS

From a technological point of view, it is important to shrink the individual device size to the nanoscale in order to achieve high density memory modules. In order to show that our devices work in the nanoscale regime, we fabricated MIM devices in the form of nanopillar arrays by single shot electron beam lithography. We have demonstrated in our previous work that we could fabricate nanoarrays over millimetre areas within only a few hours using this technique [22]. The HSQ nanopillar devices were fabricated on a Si wafer with a 4 µm thermal oxide layer, on top of which was

150 nm of Mo, which served as the bottom device electrode. The HSQ active switching layer and Ti/Au top contact were patterned using electron beam lithography and reactive ion etching (RIE).

Fig. 3(a) shows a scanning electron microscope (SEM) plan view image of a section of the nanopillar RRAM sample. The nanopillars are 150 nm high (35 nm of HSQ plus 115 nm of Ti/Au), 300 nm in diameter and their spacing is 2 μm. The sample has excellent uniformity in individual pillar size and inter-pillar spacing.

Fig. 3(b) shows IV sweeps of an HSQ nanopillar array using a probe needle to make contact. The schematic of the measurement set-up is shown in Fig. 3(c). Because the needle probe tip was much larger than an individual nanopillar, we were probing several nanopillars at once, and the switching process might involve more than one nanopillar. Nevertheless, the voltages required to set and reset are comparable to those of our MIM thin film devices (in the region of 1 V). We may also cycle the pillars many times between the LRS and HRS with over 1 order of magnitude of resistance contrast.

We probed the electrical characteristics of individual RRAM nanopillars by conductive atomic force microscopy (CAFM), landing a conductive probe on top of single pillars to measure their IV characteristics. In our preliminary work, we found that metal-coated silicon probes were too prone to wear on the rough, pillared surface; we therefore used boron-doped diamond probes on nickel cantilevers. These have a relatively high impedance of 10^5 to 10^6 Ω and a large radius of curvature, typically between 50 – 100 nm.

It is important to note that in our previous work we have made the diameter of the nanopillar of the order of tens of nanometres. However, devices of this size were unstable when addressed with diamond probes, due to the hardness of the diamond compared to the softness of the top electrode. Therefore, larger lateral size devices were fabricated for this work so that the contact between the probe tip and the pillar could be made more stable. For all measurements, the CAFM probe was grounded and the bias voltage was applied to the stage.

An example of the IV sweeps using the CAFM on an individual nanopillar is shown in Fig. 4(b). The voltage applied to form the device is in the region of -2.8 V, and a subsequent read voltage of 0.5 V was applied, which showed that the device stayed in the LRS. We were able to reset the device in the opposite polarity at around +3.1 V, demonstrating bipolar switching. Note, the voltages required to form (and set) and reset are higher than those demonstrated in the thin film devices. However, this may be due to the impedance mismatch between the device and the CAFM instrumentation and/or poor contact between the nanopillar and probe tip.

In order to demonstrate that we could address multiple individual pillars to demonstrate programming capability, we used a 3 × 3 pillar array onto which write letters of our choice. For each write/erase operation, the CAFM probe was lifted, positioned above the required nanopillar and then brought into close contact with the top electrode, meaning that there was no tunnelling gap. When reading the 3 × 3 array, the probe was lifted from close contact to prevent wear of the pillars. This reduced the measured currents and made them somewhat variable (ranging from 5 pA to 12 nA with a mean of 2 nA and standard deviation of 4 nA) and increased the effective noise level. Current maps were therefore thresholded from -2 pA to remove the noise floor and cut off at -3 pA to best distinguish the state of each device in a binary manner (i.e. all current levels below -2 pA represent "off' and the pillar is "switched on" for current levels above -3 pA). Fig. 4(c) shows a CAFM image of the 3 × 3 pillar area scanned with 0.5 V bias to show all pillars were initially in the HRS (off state). Subsequently, we wrote the letters "U", "C" and "L" in the same array using form and reset operations to switch on and off individual nanopillars. This demonstrates that we are able to programme individual nanopillars to write an area using CAFM.

V. Conclusion

In summary, we have demonstrated that HSQ is an excellent material for resistance switching applications. We can achieve bipolar intrinsic resistance switching by controlling the thin film thickness in our MIM devices. We could achieve one magnitude of LRS and HRS contrast with set and reset voltages of 1 V or less. Higher state contrast can easily be achieved with set and reset voltages of less than 2 V. The switching voltages are typically less than 1V, with excellent cycling (>10^7 cycles) and retention performance (10^4 seconds) at temperatures up to 120 ºC. One of the advantages of HSQ is ease of fabrication and processing compared with traditional UHV based techniques, such as sputtering and atomic layer deposition. We have demonstrated that highly uniform nanoscale RRAM arrays could be fabricated by single shot electron beam lithography, and we can address and programme individual nanopillars using CAFM.

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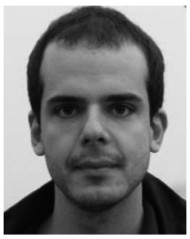

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