Symbolic Analysis of the Tau Cell Log-Domain Filter using Affine MOSFET Models

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***Abstract*— This paper analyses a filter known as the Tau Cell using symbolic methods and shows that the operation of this filter is independent of the magnitude of the input DC offset. This means that the circuit places no restrictions on whether the input DC offset is a sub-threshold current or not. The circuit behaviour predicted from symbolic analysis was observed in similar circuits on a chip fabricated using MOSIS AMI 1.6µm technology. This paper highlights the utility of symbolic analysis and shows that it is a powerful tool for circuit analysis and design.**

***Keywords*—Symbolic Circuit Analysis, Log Domain Filters, Small-Signal Modelling**

I. Introduction

Symbolic analysis is used to aid the design and analysis of analog integrated circuits because it provides a more intuitive understanding of circuit behaviour than numerical analysis. The symbolic simulator plays an important role, especially in the design of novel circuits, by providing direct insight into the qualitative influence of each circuit parameter on the desired circuit behaviour. In this paper we use a symbolic circuit analysis toolbox, developed in Matlab to analyse a log-domain filter known as the Tau Cell [1], shown in Fig. 1.

Log-domain filters take advantage of the exponential relationship between current and voltage when the transistors that make up the circuit are in the weak inversion (sub-threshold) region. The requirement that the transistors in a log-domain filter are in weak inversion places limitations on these circuits. Circuits in weak inversion can suffer from difficulties with matching and hence, the precision of the circuit can be compromised.

Restriction of the DC offset to a low current level can also restrict the allowable signal swing in the circuit and hence the gain of the circuit. This is of particular concern when dealing with second order filters with high Q values.

The Tau Cell [1] is a log-domain building block for creating a number of different filters. This paper shows, using symbolic circuit analysis, that this building block is virtually unaffected by the magnitude of the DC offset and hence, that it can be used to create filters which enjoy many of the benefits of log-domain devices without some of the drawbacks. The main advantage will be that the DC offset can be adapted to accommodate the amplitude of the input signal over several orders of magnitude without degrading the performance of the filter.

The circuit behaviour predicted from our symbolic analysis of the Tau Cell is verified in numerical simulation and observed in the behaviour of similar circuits on a fabricated integrated circuit.

II. Background

A. Symbolic Circuit Analysis

Symbolic analysis is a method of analysis in which some or all of the circuit parameters are retained as symbols. Therefore it provides an opportunity for interactive design of novel circuits and allows further exploration into the behaviour of existing circuits. The symbolic circuit analysis tool complements numerical analysis tools by providing additional intuitive understanding of the circuit behaviour. The usefulness of symbolic analysis in varied fields of circuit analysis, design and testing is widely demonstrated [2]. The main problem with the existing symbolic analysis tools is that the size of the symbolic expressions is large, even for small circuits, making them difficult to read and hard to interpret. Moreover, the expressions obtained from a low accuracy analysis do not correlate well with the expressions obtained from high accuracy analysis. In other words, it is hard to keep track of the errors between a low accuracy and high accuracy analysis.

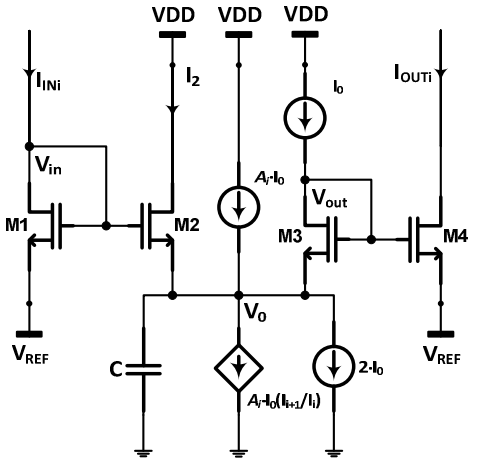

Fig. 1. The Tau Cell

The symbolic analysis toolbox we developed and used to analyse the Tau Cell is based on affine arithmetic concepts and overcomes the difficulties mentioned above. An affine arithmetic number can be defined as,

$$\tilde{x} = x_0 + x_1 \cdot \varepsilon_1 + x_2 \cdot \varepsilon_2 + \ldots + x_m \varepsilon_m \quad (1)$$

where, x_0 is defined as the central value, $\{x_1, x_2, .. x_m\}$ are the partial deviations or errors which, when added to central value, result in increased accuracy, and ε_i is the noise symbol whose value is assumed to be in the range {-1,+1}.

The symbolic analysis toolbox used in the analysis presented in this paper contains MOSFET small signal affine models of different levels of complexity, shown in Fig. 2. These models were built from conventional device models by redistributing and regrouping the circuit elements using the concept of affine arithmetic numbers as illustrated in equation (1). The details of the transformation and equations governing the elements in the affine MOSFET models can be found in [3].

B. Log Domain Circuits

The exponential relationship between voltage and current, when a transistor is in weak inversion, has led to the foundation of a group of analog circuits classified as log-domain or current-mode circuits. The relationship between terminal voltages and drain current in weak inversion [4] is given in by,

$$I_D = I_S \cdot e^{(V_G - V_{T0})/nU_T} \cdot \left[e^{-V_S/U_T} - e^{-V_D/U_T} \right] \quad (2)$$

where, V_G is the gate voltage, V_D is the drain voltage, V_S is the source voltage (all referred to the bulk voltage), V_{T0} is the zero source threshold voltage, U_T is the thermal voltage, and n is the gate reduction factor. Equation (2) gives the weak inversion drain current (I_D) when it is small, i.e., much less than the specific current (I_S). The specific current is dependent on the physical characteristics of the transistor such as its width and length, carrier mobility, gate oxide capacitance and thermal voltage. The drain current reaches saturation when the drain voltage becomes larger than $4U_T$. In log-domain circuits current, rather than voltage, is the main signal carrier. As a result, they have a wider dynamic range to exploit than voltage domain circuits [5]. Research into log-domain circuits has revealed that issues with noise and matching make it very difficult for these circuits to fulfil their potential [6]. Some of these issues are made worse by the need for sub-threshold bias currents in these circuits.

C. Translinear Loops

Many current-mode circuits use translinear loops. Translinear loops exist where transistors create closed loops of gate-source junctions [7]. The translinear principle can be summarized as follows for MOS transistors operating in weak inversion: *in a closed loop containing an equal number of gate-source junctions of one polarity and an equal number of gate-source junctions of the opposite polarity, the product of the currents of one polarity is equal to the product of currents of the opposite polarity* [7].

D. The Tau Cell

The Tau Cell [1] is a type of log-domain filter designed for complete programmability via two parameters: the time constant, τ, and the current feedback gain, A_i. The Tau Cell is designed to be a building block to create much more complicated filters. The Tau Cell is shown in Fig. 1. Its transfer function is given by,

$$T_i(s) = \frac{1}{\left[\tau_i \cdot s + 1 - A_i\right] + A_i \cdot T_{i+1}} \quad (3)$$

where, $\tau_i = C \cdot U_T / I_0$

The Tau Cell utilizes the principle of translinear loops. In Fig. 1 the closed loop of gate-source junctions is created by transistors M1 to M4. Hence, by the translinear principle,

$$I_{IN} \cdot I_0 = I_2 \cdot I_{OUT} \quad (4)$$

This relationship has become a convenient way of analysing and representing current-mode circuits. The principle of translinear loops is also used to create the current feedback gain, A_i, however, for a first order log-domain filter, A_i is equal to 0, so no multiplier is needed for these.

In this paper we analyse the first order Tau Cell using symbolic small signal analysis and show that it allows us to deduce more about the circuit than standard analysis with translinear loops.

III. Symbolic Small Signal Analysis using Affine MOSFET Models

Small signal analysis is a valid method of analysing log-domain filters since the voltage signal swing is normally small in these circuits, independent of the region of operation (strong or weak inversion) and the transistors can be approximated with a linear transconductance. When the small signal condition is not met the analysis presented here is not valid.

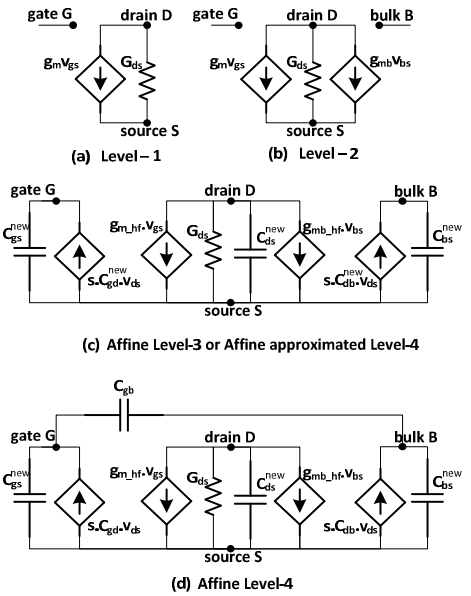

Fig 2. Affine MOSFET small-signal model at different accuracy levels

The Matlab toolbox used for this analysis directly reads the circuit netlist and DC operating point parameters from SPICE simulation results. Using this toolbox, the transfer function for small and medium size circuits can be derived using the Determinant technique or the Sequence-of-Expressions technique as shown in [2]. The Tau Cell was designed using 1.6µm technology and simulated using ELDO SPICE to obtain the circuit parameter values from the DC operating point results. The transfer function, I_{OUT}/I_{IN}, for the Tau Cell was derived using Determinant technique.

The symbolic transfer functions were computed after substituting the MOSFETs with affine level-2 and affine level-4 models respectively, as shown in Fig. 2. The numerator and denominator of the transfer function obtained from our Matlab toolbox in the case of level-2 model is shown in equations (5) and (6).

$$num = g_{mN4} \times g_{mN2} \times G_{dsN3} \tag{5}$$

$$den = G_{dsN3} \times G_{dsN1} \times (s \cdot C + G_{dsN2} + g_{mN2}) \tag{6}$$

As can be seen from the equations (5) and (6), the drain conductance of M3 cancels out and the (trans) conductance of M2 influences the time constant in transfer function. The transfer function can be represented in the simplified form as,

$$T_i(s) = \frac{g_{mN4}}{G_{dsN1}} \times \frac{g_{mN2}}{\left(s \cdot C + G_{dsN2} + g_{mN2}\right)} \tag{7}$$

As can be seen from equation (7) the parameters of transistors M4 and M1 contribute only to the gain in the expression and do not affect the time constant in the transfer function. This simplified analysis provides a quick insight into the circuit operation of the Tau Cell with transistors M1 and M4 determining the current gain and transistor M2 dominating the time constant.

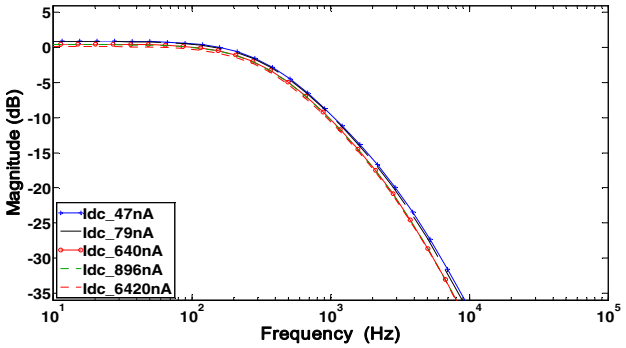

Fig 3. First Order Tau Cell Bode Plot from Symbolic Analysis Toolbox

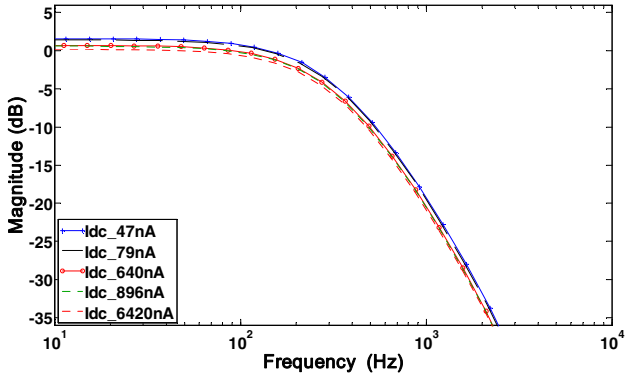

Fig 4. Second Order Tau Cell Bode Plot from Symbolic Analysis Toolbox

A thorough analysis including the parasitic capacitances can be performed using the affine level-4 model for all the transistors, shown in Fig. 2 (d). It is expected that the parameters of the transistors M1 and M4 will dominate the gain while M2 will dominate the time constant. Transistor M3 may not cancel out, but remain equally present in both numerator and denominator. The numerator and denominator of the transfer function obtained from the Matlab toolbox using the level-4 model is shown in equations (8) and (9).

$$\begin{aligned} num = &\left(g_{mN4} - s \cdot C_{gdN4}\right) \times \left(G_{dsN3} + s \cdot C_{dsN3}^{new}\right) \\ &\times \left(g_{mN2} - s \cdot C_{gdN2} + s \cdot C_{gsN2}^{new}\right) \end{aligned} \tag{8}$$

$$\begin{aligned} den = &sub_1 \times \left(G_{dsN3} + s \cdot C_{dsN3}^{new} + C_{gsN4}^{new}\right) \\ &+ sub_2 \times \left(G_{dsN3} + s \cdot C_{dsN3}^{new}\right) \end{aligned} \tag{9}$$

where,

$$sub_1 = \left\{ \begin{array}{l} \left(G_{dsN2} + s \cdot C_{dsN2}^{new} + s \cdot C\right) \times \left(G_{dsN1} + s \cdot C_{dsN1}^{new} + s \cdot C_{gsN2}^{new}\right) \\ + \left(g_{mN2} + s \cdot C_{gsN2}^{new} - 2 \times s \cdot C_{gdN2}\right) \times \left(G_{dsN1} + s \cdot C_{dsN1}^{new}\right) \\ - s \cdot C_{gdN2} \times \left(g_{mN2} - s \cdot C_{gdN2}\right) \end{array} \right\} \tag{10}$$

$$sub_2 = s \cdot C_{gsN4}^{new} \times \left(G_{dsN1} + s \cdot C_{dsN1}^{new} + s \cdot C_{gsN4}^{new}\right) \tag{11}$$

Equations (8) and (9) show that, the parameters of M3 are equally present in both the numerator and the denominator. Therefore changing the parameters of M3 will not significantly influence the frequency response characteristics of the filter. The "sub"-expressions, sub_1 and sub_2, are dominated by (G_{dsN1}+s·C_{dsN1}), in other words by transistor M1, while (g_{mN4}-s·C_{gdN4}) is a factor in the numerator. Therefore the gain is still strongly dependent on M1 and M4, despite the fact that their parameters cannot be completely extracted out as common expressions. The denominator expression, sub_1, shows that the parameters of transistor M2 continue to dominate the time constant.

The expectation about the circuit behaviour from the low accuracy symbolic analysis (equation (7)) correlates well with the results obtained from the high accuracy symbolic analysis (equations (8) – (11)). This is because the use of affine arithmetic models for symbolic simulation helps keep track of errors as the level of accuracy improves. Therefore, our analysis provides a more intuitive understanding of circuit behaviour when compared with analysis using the conventional MOSFET small signal models.

The results from the symbolic analysis of the Tau Cell using the level-4 affine MOSFET model were validated with numerical computation using 1.6µm transistor BSIM3v3 parameters. Fig. 3 shows the frequency response of the first order Tau Cell shown in Fig. 1. The input DC current was varied over two orders of magnitude from 47nA to 6.42uA.

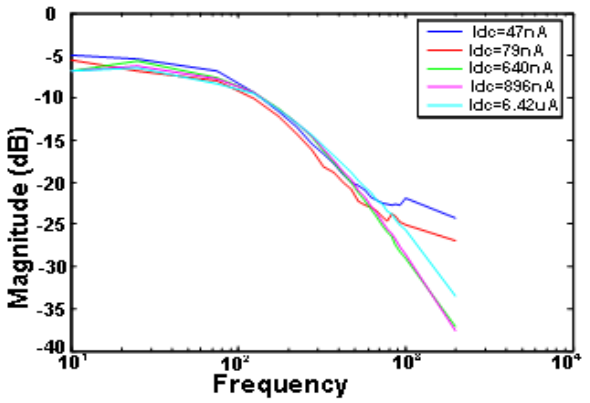

Fig 5. Tau Cell frequency response measured from a fabricated chip

The Bode plot obtained from Matlab shows that the gain changes by 2-3dB between the lowest and highest DC currents. This is expected from the symbolic expressions (8) – (11) since transistors M1 and M4 were shown to dominate the gain. Neglecting the gain, the shape of the frequency response curve remains constant across the 4 decade input current range. This is also expected from our symbolic analysis as only transistor M2 was shown to dominate the time constant of the circuit.

IV. Experimental Results

To confirm our theoretical analysis of the Tau Cell a test chip was used. The chip was fabricated using MOSIS AMI 1.6µm technology. The chip was originally designed to test matching in second order Tau Cell filters in the audio frequency range [8], however, it did allow us to vary the input DC current over a limited range. Each chip contained six filters that were configured as second order low pass filters. Given the structure of the second order filter, however, which consists of a cascade of first order filters [1], the DC independence hypothesized in section III still holds. This can be seen in simulation in Fig. 4.

Our experimental set up allowed us to vary the input DC current reliably from 47 nA to 6.4 µA. The frequency response of the filter was measured by injecting a current with a constant DC-to-signal amplitude ratio of 11.5% into the filter and measuring the output amplitude as the frequency was swept from 10 Hz to 2 kHz. Over the two orders of magnitude of DC currents that we measured only slight differences in the frequency response of the filter were observed, as shown in Fig. 5. There was a change of about 2 dB in gain between the highest DC current, 6.4 µA, and the lowest current, 47 nA.

V. Conclusions

The behaviour of the Tau Cell log-domain filter has been analysed in detail in this paper. The intuitive understanding of the filter's behaviour developed using symbolic circuit expressions has been corroborated with measurements from a fabricated chip. This, to the best of our knowledge, is the first time that the conclusions and predictions from the symbolic analysis of a novel circuit have been verified with fabricated chip results.

According to symbolic analysis, the frequency response of the Tau Cell is independent of the DC offset. This was demonstrated over a two decade range on a fabricated chip. The symbolic analysis also predicted a gain dependant on the transconductance of input and output transistors. This was measured to be 2dB over the two decade DC offset range and matched well with the numerical simulation result.

We can therefore conclude that the Tau Cell is not restricted to sub-threshold input DC offset currents. This means that matching may improve and the signal swing can be large. These are very important features for filters used in audio applications with potentially high Q values, illustrating the utility of analysis using symbolic methods even for the most simple of circuits.

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