Switched Capacitor DC-DC Converter for Miniaturised Wearable Systems

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***Abstract*— Motivated by the demands of the integrated power system in the modern wearable electronics, this paper presents a new method of inductor-less switched-capacitor (SC) based DC-DC converter designed to produce two simultaneous boost and buck outputs by using a 4-phases logic switch mode regulation. While the existing SC converters missing their reconfigurability during needed spontaneous multi-outputs at the load ends, this work overcomes this limitation by being able to reconfigure higher gain mode at dual outputs. From an input voltage of 2.5 V, the proposed converter achieves step-up and step-down voltage conversions of 3.74 V and 1.233 V for Normal mode, and 4.872 V and 2.48 V for High mode, with the ripple variation of 20-60 mV. The proposed converter has been designed in a standard 0.35 µm CMOS technology and with conversion efficiencies up to 97-98% is in agreement with state-of-the-art SC converter designs. It produces the maximum load currents of 0.18 mA and 0.36 mA for Normal and High modes respectively. Due to the flexible gain accessibility and fast response time with only two clock cycles required for steady state outputs, this converter can be applicable for multi-function wearable devices, comprised of various integrated electronic modules.**

Keywords*— *Wearable electronics, Switched Capacitor, DC-DC converter, Simultaneous outputs, Single-Input Dual-Outputs.

I. INTRODUCTION

There is a growth of applications in wearable technology to enhance the quality of life through incorporated into healthcare, education, security and many more [1-3]. While wearable designs growing fast, yet battery life is the major discomfort point in wearables right now. The power and battery management are becoming one of the crucial functions in wearable and portable systems, as it considerably extends the battery life of a wearable design by employing energy efficient and boost circuit blocks. Increasing different loads in the miniaturised wearable devices, require different operating voltages and load currents which powered by battery through DC-DC converters. Reliable and efficient DC-DC conversion provides steady regulated DC output voltage from unregulated battery source to attain longer system run-time at smaller size wearable designs. Thereby miniaturised integrated power system supply required regulated voltages at the sufficient current at high efficiency and improve system's power conversion efficiency with advanced circuit topologies.

This paper will introduce switched-capacitor (SC) approach for an integrated on-chip power system which can be used for

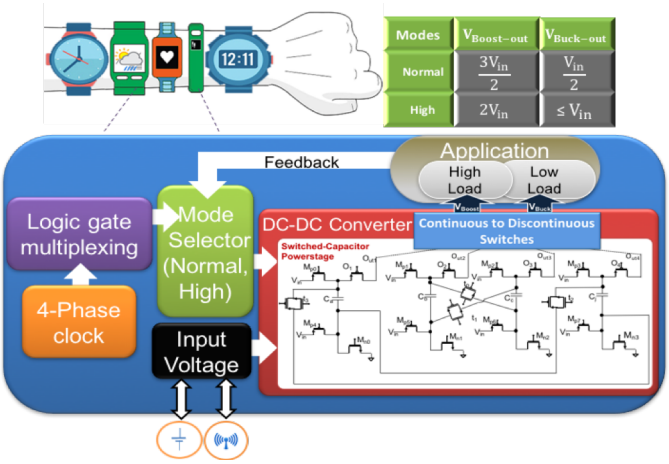

Fig. 1. *Overall system of wearable power system*

wearable electronics and systems. This is mainly due to eliminating the needs of bulky inductors and can fabricate on silicon surface for various applications [4] with high conversion efficiency. The Fig. 1 illustrates the high-level concept of the proposed power device. Power management operates in power stage network and is controlled by digital modules. Depending on the load conditions, mode selector will choose the appropriate gain modes. The primary source of input is taken from the use of an integrated battery or a remote powering. This input voltage will process DC-DC conversions in the power stage by using a novel 4-phases rotation scheme. Hence non-overlapping 4-phases clock generator is integrated. The proposed technique in this paper will introduce SC approach single-input simultaneous dual-outputs with each output lines comprised of two different gain modes (Normal, High), enhance the 3-phases rotation topology reconfigurable SC converter with the single-input single-output (SISO) [5]. In generating of two spontaneous outputs from single input by traditional SC converters, which can configure one gain at a time [6], will require two independent converters or use of a capacitor bank [7]. By integrating only four capacitors and novel switch mode regulation, this converter enables both boosting and bucking conversions simultaneously without doubling the operation mechanisms.

II. METHODOLOGY AND SYSTEM DESCRIPTION

Using a switch mode regulation, the proposed converter is designed to configure into two different gain modes, each with two different simultaneous regulated stable dual outputs

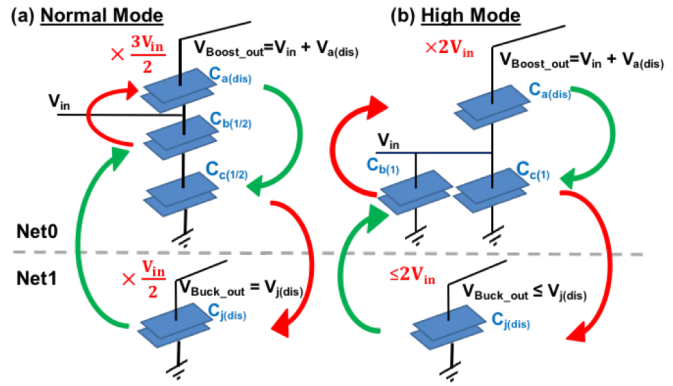

Fig. 2. *Proposed Methodology of (a) Normal and (b) High modes with arrows indicating charging(green) and discharging(red) directions*

(V_{Boost_out}, V_{Buck_out}). Power stage network is divided into two conceptual internal networks (Net0, Net1) as shown in Fig. 2, and boost operation will perform in Net0 whilst buck output produces at Net1. Therefore, in every clock cycles, there will be two active corresponding internal outputs at (O_{ut1}-O_{ut4}). These internal outputs will then connect to High and Low loads through continuous to discontinuous switches.

A. Normal and High modes Operations

The Fig. 2(a) explains the construction of 3/2 gain Normal mode configuration at Net0 and 1/2 gain at Net1. The capacitors C_b and C_c are charged in series to $V_{in}/2$ as all the capacitors have equal capacitances. Considering a continuous sequence of a 4-phases rotation, previously charged C_a is now discharged to Net0 boost output in a series with V_{in}. Therefore, Net0 load is discharged at:

$$V_{boost\_Norm} = V_{in} + V_{Ca} = \frac{3V_{in}}{2} \quad (1)$$

While in Net1, a capacitor C_j, which was initially charged to $V_{in}/2$ from Net0 in the previous clock cycle, is now discharged to buck output of Net1:

$$V_{buck\_Norm} = V_{Cj} = \frac{V_{in}}{2} \quad (2)$$

The proposed converter can reconfigure into relatively even higher gain ratios for both boost and buck outputs than Normal mode. This will improve power stage SC converter design flexibility for single-input dual-outputs (SIDO). As suggested by the Fig. 2(b), the following derivation is achieved for High mode operation:

$$V_{boost\_High} = V_{in} + V_{Cc} = 2\,V_{in} \quad (3)$$

The voltage of equal or less than source voltage can be achieved by controlling the switching frequency of capacitor discharge at buck conversion:

$$V_{buck\_High} \leq V_{in} \quad (4)$$

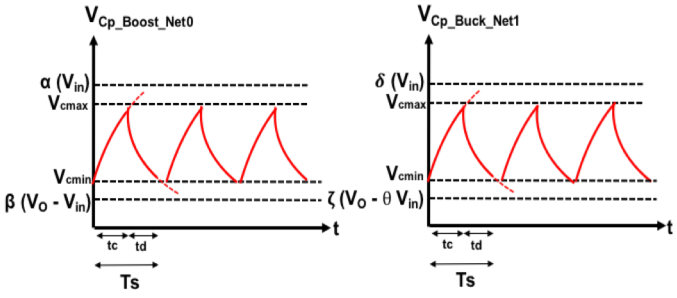

Fig. 3. *Charging discharging characteristic graph of flying capacitors in two internal networks (a)* Net0 and (*b*) Net1.

B. Output Voltages and Power Looses

The first order differential equation of charging and discharging part of RC circuit in Laplace and convert it back to time domain in Inverse Laplace, a final voltage $V_c(t)$ is the sum of the initial charging voltage $V_c(0)$ and the input voltage V_{in}. The total switching time (t) with RC time characteristic in Eq. (5).

$$V_c(t) = V_c(0)e^{-\frac{t}{RC}} + V_{in}(1 - e^{-\frac{t}{RC}}) \quad (5)$$

According to the circuit configuration of Normal and High modes, the coefficient of voltage values for each charged pump capacitors tends to charge-discharge to and actual voltages of capacitors (V_{max}, V_{min}) in Fig. 3 varies and defined in Table I.

TABLE I. Variable values for Fig. 3.

Normal mode	High mode
α=1/2, β=1, δ=1/2, ζ=1, θ=0	α=1, β=1, δ=1, ζ=1, θ=0

For a Normal mode, in charging phase, a final voltage $V_c(t)$ is equal to V_{cmax} and initial voltage $V_c(0)$ will be V_{cmin}. Since it is charged towards ½V_{in}, produces the Eq. (6). Likewise, a final voltage for a discharge phase is V_{cmin}, the initial voltage is V_{cmax} and V_{in} from Eq. (5) can be replaced with $V_o - V_{in}$ to get Eq. (7).

$$V_{cmax} = V_{cmin}e^{-\frac{t_c}{T_c}} + \left[\frac{1}{2}V_{in}\left(1 - e^{-\frac{t_c}{T_c}}\right)\right] \quad (6)$$

$$V_{cmin} = V_{cmax}e^{-\frac{t_d}{T_d}} + [(V_o)\left(1 - e^{-\frac{t_d}{T_d}}\right)] \quad (7)$$

The output current is denoted as I_o. The total amount of charge for steady state charging and discharging voltage-time for Normal mode ΔQ_{Normal} is $\frac{I_0}{2\,f_s}$ and solve together with Eq. (6) and (7) give:

$$V_{boost\_Norm} = \frac{3}{2}V_{in} - \frac{Io\_boost}{2\,f_sC_p}\left(\frac{1}{1-e^{-\frac{t_d}{T_d}}} + \frac{1}{1-e^{-\frac{t_c}{T_c}}} - 1\right) \quad (8)$$

$$V_{buck\_Norm} = \frac{1}{2}V_{in} - \frac{Io\_buck}{2\,f_sC_p}\left(\frac{1}{1-e^{-\frac{t_d}{T_d}}} + \frac{1}{1-e^{-\frac{t_c}{T_c}}} - 1\right) \quad (9)$$

Correspondingly ΔQ_{High} is $\frac{I_0}{3\,f_s}$ for High mode and solve in Eq. (6) and (7) produce:

$$V_{boost\_High} = 2V_{in} - \frac{Io\_boost}{3\,f_sC_p}\left(\frac{1}{1-e^{-\frac{t_d}{T_d}}} + \frac{1}{1-e^{-\frac{t_c}{T_c}}} - 1\right) \quad (10)$$

$$V_{buck\_High} = V_{in} - \frac{Io\_buck}{3\,f_sC_p}\left(\frac{1}{1-e^{-\frac{t_d}{T_d}}} + \frac{1}{1-e^{-\frac{t_c}{T_c}}} - 1\right) \quad (11)$$

The conduction power loss can deviate from the V_{out} and V_{in} relation of (8-11) are described as

$$P_{conduct\_Norm} = \frac{I^2_{o\_boost,buck}}{2\,f_sC_p}\left(\frac{1}{1-e^{-\frac{t_d}{T_d}}} + \frac{1}{1-e^{-\frac{t_c}{T_c}}} - 1\right) \quad (12)$$

$$P_{conduct\_High} = \frac{I^2_{o\_boost,buck}}{3\,f_sC_p}\left(\frac{1}{1-e^{-\frac{t_d}{T_d}}} + \frac{1}{1-e^{-\frac{t_c}{T_c}}} - 1\right) \quad (13)$$

whereas (t_d and t_c) are the total switching time of charging and discharging. Moreover, RC time constant (T_d and T_c) are dominated by on-resistance along the path of charging-discharging R_{on}, and flying capacitor C_p, as it is larger than the

capacitance of individual switches. Furthermore, charge-discharge mechanisms of a gate-source parasitic capacitance of MOSFET transistors (C_{gs}), the frequency of switching (f_s) and the gate-source voltages (V_{gs}) of individual switches along the path dominate the switching power losses [8] and for this proposed methodology-

$$P_{sw\_Norm(boost,buck)} = f_s \sum_i C_{GSi} V_{GSi}^2 \cong f_s C_{OX} \sum_i W_i L_i V_{GSi}^2 \quad (14)$$

$$P_{sw\_High(boost,buck)} = f_s \sum_i C_{GSi} V_{GSi}^2 \cong f_s C_{OX} \sum_i W_i L_i V_{GSi}^2 \quad (15)$$

where (W_i, L_i) are width and length of individual transistors along the path of operations and (C_{ox}) is the gate-oxide capacitor of the transistor.

C. *Efficiency*

The efficiencies of Normal and High modes are calculated individually for boost and buck outputs. This is done by taking the percentage of simulated output power divided by the sum of simulated output power and the total power losses. The simulated voltages and currents from the boost and buck outputs produce ($P_{Norm_{boost}}$, $P_{Norm_{buck}}$) for a Normal mode, and ($P_{High_{boost}}$, $P_{High_{buck}}$) for a High mode. The total power losses are the sum of Eq. (12) and (14) for a Normal mode and, (13) and (15) for a High mode. The efficiencies of the boost and buck outputs are ($\eta_{Norm_{boost}}$, $\eta_{Norm_{buck}}$) for a Normal mode, and ($\eta_{High_{boost}}$, $\eta_{High_{buck}}$) for High mode are calculated through the generalised Eq. (16) and (17) respectively:

$$\eta_{Norm_{boost,buck}} = \frac{P_{Norm_{boost,buck}} \times 100\%}{P_{Norm_{boost,buck}} + P_{conduct\_norm} + P_{sw\_Norm}} \quad (16)$$

$$\eta_{High_{boost,buck}} = \frac{P_{High_{boost,buck}} \times 100\%}{P_{High_{boost,buck}} + P_{conduct\_High} + P_{sw\_High}} \quad (17)$$

III. Design and Implementation

The work is implemented in a standard 0.35 µm CMOS technology. The operating frequency of 1.1 MHz is used to ensure that 1 nF charge pump capacitors are fully charged/discharged over MOSFET switches. The series of four D-flip flops are constructed to produce 90-degree phase shift for four different phases at every rising edge of input clock signal and is further enhanced by passing it through ring oscillators. Thereby, the power stage's transistor switches benefit non-overlapping 0.1 ns dead time intervals between clock phase changes.

The selection of the mode or a pair of gains changes when load demands higher voltages at the output. The supply voltages to loads are monitored by the analog to digital converter and gain selection is done by a digital router module programmed with Verilog-A. In which, all the transistor addresses for four different phases logics are registered and automatically reconfigure the power stage network in accordance with proposed methodology when the selection of Normal or High mode is changed.

The configuration of four integrated 1 nF capacitors in power stage is controlled through 20 switches (4 Transmission Gate, 4 nMOS, 12 pMOS). However, only 7 switches for Normal mode and 8 switches in total for High mode are used in every clock phases. The power switches protocols are carefully designed to make sure that all internal outputs of power stage (O_{ut1}-O_{ut4}) are regulated at all 4-phases for both gain modes. This is due to multiple ways to route for the same logic and each offers the different resistance path along the switches. The different resistances across the path leads to small variations in ΔV at outputs. Through simulations, the obtained design ensures the optimum route with minimum on-resistance and maintains the symmetric R_{on} values for all 4-phases are accessible for consistency of outputs level. This can be further improved by introducing adaptive pulsing unit in between gain selector and power stage network since fast switching energy delivery for low and high loads can vary, and hence is noted as a future plan.

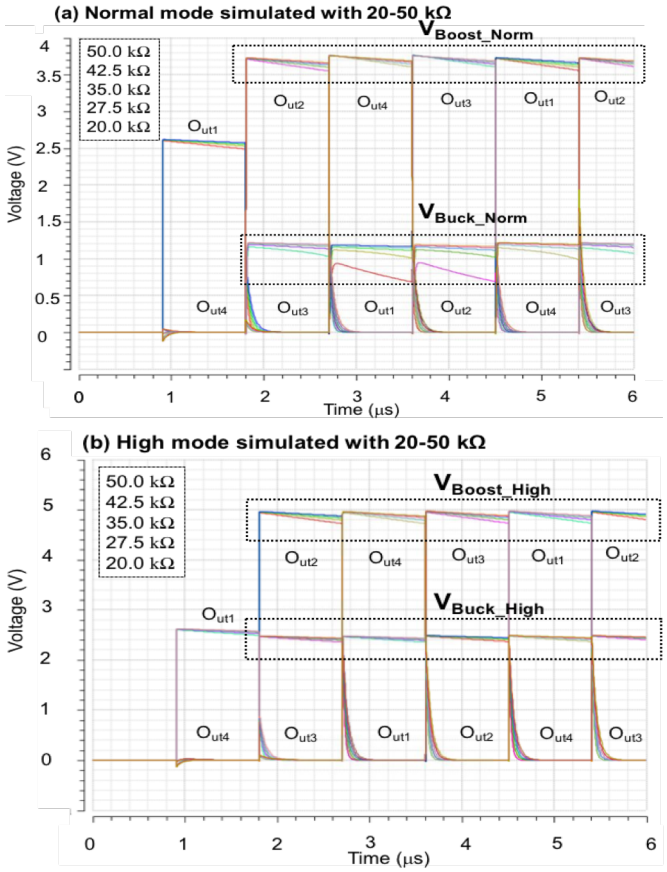

Fig. 4. *Output Voltages of (a) Normal mode and (b) High mode simulated with 20-50 kΩ load resistors and 1pF filter capacitor.*

There can be multiple ways to route and the optimal one has been selected to offer the same output level of the same gain at all 4-phases. Due to the different resistances R_{on} across the path, there can be slightly different in ΔV at outputs. Therefore, it is important to minimise the ripple variations through the tests.

IV. Results and Discussion

The proposed converter is simulated in a Cadence software. The results in Fig. 4 are tested with 2.5 V input voltage and different loads vary from 20-50 kΩ. It demonstrated that the conversion efficiencies can perform up to 97-98%. At best, Boost output mode produces 3.752 V (at 180.8 µA) and the Buck being 1.171 V (at 29.08 µA) Normal mode. Likewise, for the High mode, The Boost output produces 4.98 V (at 241.125 µA) and 2.49 V (at 120.45 µA) for the Buck output. The output ripples are recorded between 20-60 mV. It is observed in Fig. 4(a) that some internal outputs of V_{Buck} suffer high ripple at low load. This is due to unequal R_{on} across charging-discharging path during the routing as discussed earlier and it can be fixed by introducing adaptive pulsing to adjust the frequency of switching. The converter average output power varies across the different load of 20-50 kΩ as shown in

Fig. 5. It demonstrates the average power output range from 1.5-0.6 mW and 0.7-0.3 mW, for High and Normal modes, respectively. Assuming input integrated battery degrades over time, line regulation with varying inputs of 2.5-2 V, simulated with a fixed load of 40 kΩ and the results shown in Fig. 6. Although the output voltages reduce from targeted values due to input changes, the linear line indicates that converter still maintains correct gain operation relative to a given input.

The recent state-of-the-art single-input multi-output (SIMO) SC designs summarised in Table II can only produce fixed gain ratios. For example, an integrated battery-powered system-on-chip with the SC converter in [9], the conversion efficiency significantly dropped due to cascading 2:1 converter twice to get 2:1 and 4:1 outputs. In contrary, with the technique proposed in this paper, the conversion efficiencies for both outputs maintain fairly high. Furthermore, the SIMO SC converters are also presented in [10] where the output gain ratios are rather fixed. However, using the proposed a 4-phases topology gives an ability to reconfigure the converter into higher gain ratios for both boost and buck outputs, and improves the design flexibility of SIDO converters design.

V. CONCLUSION

This paper demonstrates the novel topology of switched-capacitor approach a 4-phases rotation scheme to yield simultaneous boost and buck conversion. This new topology ensures optimum use of integrated capacitors as there is no idle capacitor in every phase of operations. This improves the overall conversion efficiency in contrary to reconfigurable SISO converters which run at the optimum voltage at the output SIDO converter not only provide simultaneous outputs but also produce larger output voltage range which will be beneficial for multi-functional wearable applications with internally integrated electronic modules.

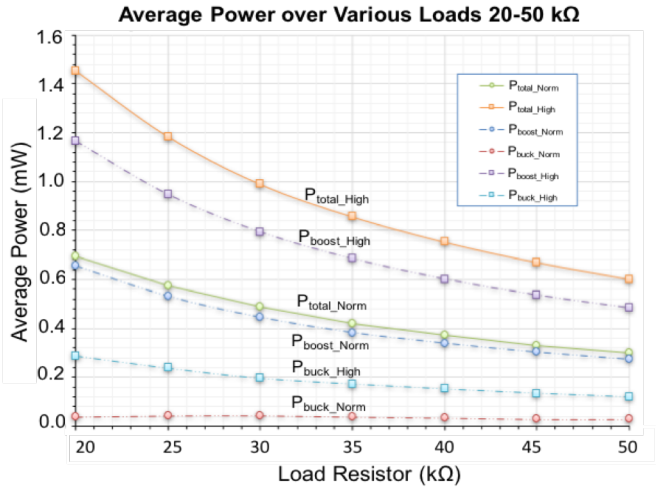

Fig. 5. *Average Output power for varying loads tested with 20-50 kΩ.*

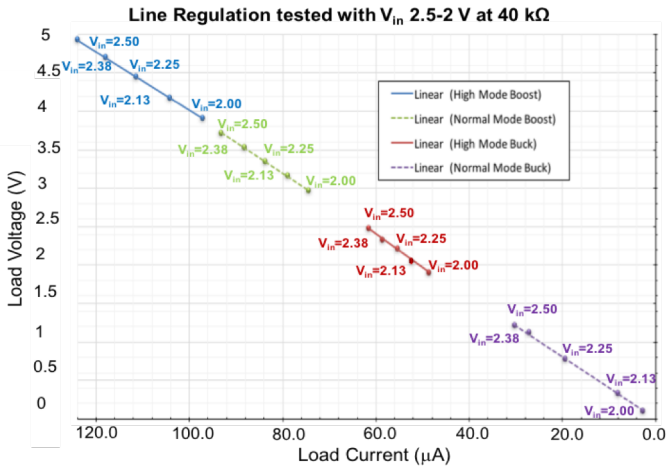

Fig. 6. *Line regulation tested with the changing input of 2.5-2 V at 40 kΩ.*

TABLE II. Performance Summary and comparison with state-of-the-arts.

Specification	This work	[6]	[7]	[8]
Input (V)	2.5	3.7	1	1.2
Output (V)	3.74, 1.233	1.8, 0.8	0.66, 0.33,1	0.76, 0.32
	4.979, 2.48	-	-	-
I_{load} (mA)	0.36, 0.18	0.4, - 1	-	0.4, 0.9
Conversion Ratios	×3/2, ×1/2 or ×2, ×1	×1/2, ×1/4	×2/3, ×1/3, ×1	×1/2, ×2/3
$P_{out\ max}$(mW)	1.5	1.3	1.3	1
Ripple (mV)	20-60	60	9.6	19.5-40.6
Efficiency (%)	97-98	70	90	68
$C_{Integrated}$ (F)	1n ×4	2.24n ×≥2	3.7n× ≥4	5n×2 6n×2

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REFERENCES

[1] S. Vallurupalli, *et al.* "Wearable technology to improve education and patient outcomes in a cardiology fellowship program-a feasibility study," *Health and Technology,* vol.3, pp.267-270, 2013.

[2] S. Park and S. Jayaraman, "Enhancing the quality of life through wearable technology," *IEEE Engineering in medicine and biology magazine,* vol. 22, pp. 41-48, 2003.

[3] A. Pantelopoulos *et al.*, "A survey on wearable sensor-based systems for health monitoring and prognosis," *IEEE Trans. Systems, Man, and Cybernetics, Part C,* vol. 40, pp. 1-12, 2010.

[4] H. Heidari, *et al.* "A CMOS current-mode magnetic hall sensor with integrated front-end," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 62, pp. 1270-1278, 2015.

[5] I. Chowdhury and D. Ma, "Design of reconfigurable and robust integrated SC power converter for self-powered energy-efficient devices," *IEEE Trans. Industrial Electronics,* pp. 4018-4028, 2009.

[6] Y. Wang, P. Luo, X. Zheng, and B. Zhang, "A 0.3 V–1.2 V ultra-low input voltage, reconfigurable switched-capacitor DC-DC converter for energy harvesting system," in *Solid-State and Integrated Circuit Technology (ICSICT)*, 2016, pp. 1333-1335.

[7] T. Tong, S. K. Lee, X. Zhang, D. Brooks, and G.-Y. Wei, "A fully integrated reconfigurable switched-capacitor DC-DC converter with four stacked output channels for voltage stacking applications," *IEEE J. Solid-State Circs,* pp. 2142-2152, 2016.

[8] D. Ma and R. Bondade, "Power Loss in Switched-Capacitor Power Converters: Causes and Analysis," in *Reconfigurable Switched-Capacitor Power Converters*, ed: Springer, 2013, pp. 59-69.

[9] X. Zhang, *et al.*, "A Fully Integrated Battery-Powered System-on-Chip in 40-nm CMOS for Closed-Loop Control of Insect-Scale Pico-Aerial Vehicle," *IEEE J. Solid-State Circuits,* vol. 52, pp. 2374-2387, 2017.

[10]Y. Yang, Y. Zhao, and G. Dong, "A Multi-Output on-Chip Switched-Capacitor DC–DC Converter with Unequal Flying Capacitors for Different Power Modes," *Journal of Circuits, Systems and Computers,* vol. 24, p. 1550051, 2015.