High Linearity SAR ADC for Smart Sensor Applications

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***Abstract*—This paper presents a capacitive array optimization technique capable to improve the Spurious Free Dynamic Range (SFDR) and Signal-to-Noise-and-Distortion Ratio (SNDR) of Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) for smart sensor specifications. Monte Carlo simulation results show that the proposed optimization technique makes the SFDR, SNDR and (Signal-to-Noise Ratio) SNR better definitely concentrated, which means with a spread between maximum and minimum value much smaller than the one obtained by conventional calibration techniques. This gives rise to more stable and better performances. The averaged SFDR improves from 72.9 dB to 91.1 dB with $\sigma_u = 0.4\%$, the 18.2 dB improvement required an off-line processing and a small digital logic circuits.**

***Index Terms*—Analog-to-Digital Converter, Successive Approximation Register(SAR) ADC, Capacitive digital-to-analog converter(DAC), Capacitor Mismatch Calibration, Smart Sensor Systems.**

I. Introduction

Smart sensors are devices which integrate transducers, signal conditioning and processing electronics, have played an important role in changing our society and lifestyle. The merit goes to the explosive growth of embedded applications for smart sensors [1]. Table I includes some applications described on top journals in diverse fields.

Fig. 1 shows the block diagram of a smart sensor node: the sensor detects a physical, chemical or biological quantity, then small signal at the output of the sensor is amplified and filtered, after that, an analog-to-digital converter (ADC) converts the analog sensing signal into digital codes. Since the ADC is an important block in smart sensor node, the designer must optimize performance of ADC, more specifically, high resolution, to satisfy the demands of low power and small silicon area at the same time as required by multi-functional smart sensor nodes.

Mainstream ADC architectures include Flash ADC, Successive approximation register (SAR) ADC, pipeline ADC and Sigma-Delta ADC. Flash ADC can only be applied for low resolution and high sampling rate application, pipeline and Sigma-Delta ADC are not appropriate for the low power sensor design as they require using op-amps.

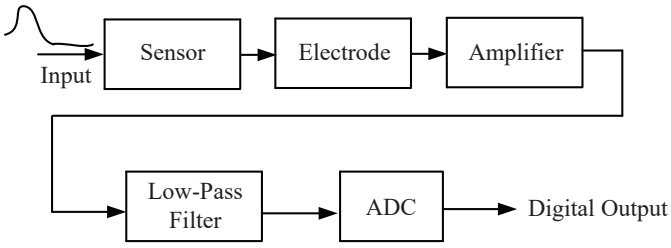

Fig. 1. Basic architectural components of smart sensor node.

As known the successive approximation register (SAR) converter obtains the analog-to-digital conversion using a binary search algorithm. As shown in Fig. 2, it consists of a sample-and-hold (S/H) stage, a digital-to-analog converter (DAC), a voltage comparator, and a successive approximation register. The simple architecture and the low power blocks make the SAR the optimal choice for medium speed sensor applications. However, the capacitive array mismatch limits the performance of the converter. For high resolution SAR ADC, the limits require using large unity capacitors and calibration circuits which normally operate off-line. This paper presents a method that allows using the minimum capacitance imposed by the kT/C limit and requires a limited digital control to reach high Spurious Free Dynamic Range (SFDR) and Signal-to-Noise-and-Distortion Ratio (SNDR). The method significantly reduces the mismatch error by optimizing the use of the capacitive array. The used technique sorts, groups and alternates the capacitive elements for an optimal linearity for a given set of elements.

The remainder of this paper is organized as follows. Section II describes previous work on performance enhancement methods, section III gives detailed description of the technique proposed, then section IV compares performance between

TABLE I
CONCLUSION OF SMART SENSOR IN RECENT YEARS

Ref	Source	Technology	Type	Function	Platform	Calibration
[2]	Nature 2016	Plastic substrate	Bio Sensor	Measure sweat	FPCB	yes
[3]	Nature 2016	Nanoporous silicon substrate	Bioresorbable pressure sensor	Monitor intracranial pressure	Programmable NFC	N/A
[4]	Nature 2016	Polyimide /Glass substrate	Biochemical sensor	Monitor alcohol consumption	DSP functionalization	yes
[5]	Nature 2015	Acrylic sheet	Active sensor	Monitor vibration	Digital oscilloscope	N/A
[6]	Nature 2014	CMOS	Electrochemical sensor	Detection of metabolites	Chip	yes

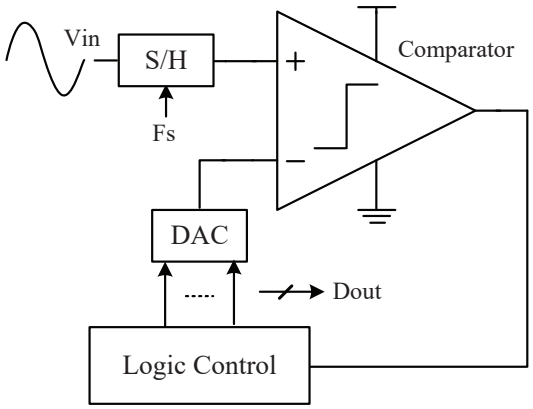

Fig. 2. Typical architecture of SAR ADC.

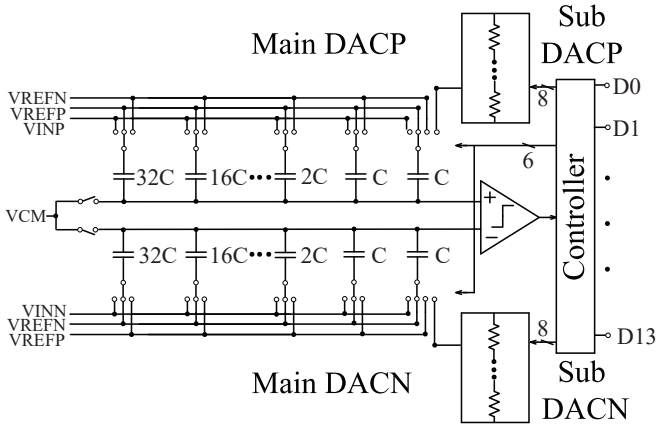

Fig. 3. A capacitor-resistor combined 14-bit SAR ADC architecture [7].

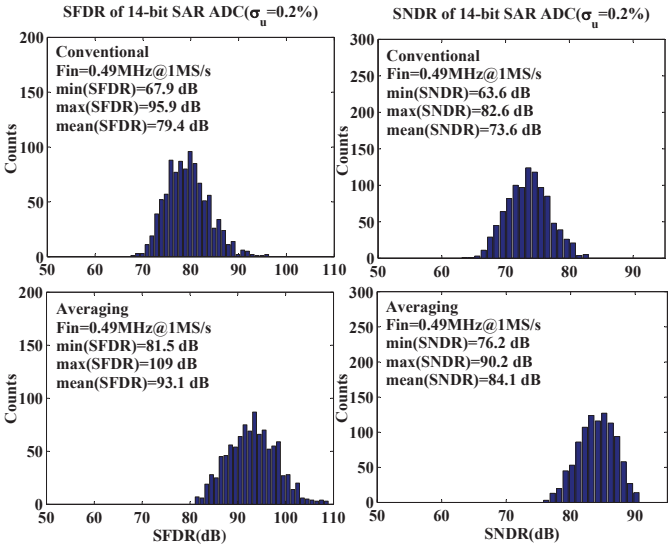

Fig. 4. 500 Monte Carlo SFDR/SNDR simulation results for 14-bit combined RC SAR ADC with respectively Conventional and Averaging technique(σ_u=0.2%) [7].

conventional and the proposed capacitive array optimization technique. The conclusions are finally drawn in section V.

II. PREVIOUS WORK RELATED TO PERFORMANCE ENHANCEMENT METHODS

Averaging technique improves the linearity [7] by performing multiple conversion of the same input sample. The method proposed in [7] makes 4 successive conversions of the input and estimates the average of the four results. Fig. 3 shows the 14-bit SAR schematic used in [7]. It is a capacitor-resistor architecture with a 6-bit capacitive DAC and an 8-bit sub-resistive DAC [7]. Although averaging can ameliorate SFDR that goes up to an average value of 93.1 dB from 79.4 dB, and SNDR is 10 dB better (Fig. 4), the number of clock periods for the conversion increases from N to 4×N; Another capacitor re-configuring technique was proposed in [8], extra 64 capacitors were added to the capacitive array in Fig. 3, then sort and re-combine these capacitors by "one head and one tail", the mismatch can be counteracted to a large extent, although sampling rate remains the same as that of the conventional SAR ADC, extra 64 capacitors lead to inevitable extra chip area consumption.

III. OPTIMIZATION TECHNIQUE OF CAPACITIVE ARRAY

The proposed capacitive array optimization technique is described using the main capacitive DAC of capacitor-resistor combined SAR ADC in Fig. 3 as test vehicle. Fig. 5 illustrates the method. The 6-bit capacitive DAC made by 64 unit capacitors in Fig. 5(a) is expanded into a unary architecture, as shown in Fig. 5(b), then sort the 64 unit capacitors (Fig. 5(c)), and the array is re-organized with the following optimized sequence: C_1, C_{64}, C_3, C_{62}, C_5, C_{60}, C_7, C_{58}, C_9, C_{56}, C_{11}, C_{54}, C_{13}, C_{52}, C_{15}, C_{50}, C_{17}, C_{48}, C_{19}, C_{46}, C_{21}, C_{44}, C_{23}, C_{42}, C_{25}, C_{40}, C_{27}, C_{38}, C_{29}, C_{36}, C_{31}, C_{34}, C_{32}, C_{33}, C_{30}, C_{35}, C_{28}, C_{37}, C_{26}, C_{39}, C_{24}, C_{41}, C_{22}, C_{43}, C_{20}, C_{45}, C_{18}, C_{47}, C_{16}, C_{49}, C_{14}, C_{51}, C_{12}, C_{53}, C_{10}, C_{55}, C_8, C_{57}, C_6, C_{59}, C_4, C_{61}, C_2, C_{63}, finally the optimized capacitors are divided into 4 groups, as shown in Fig. 5(d).

The method exploits the order statistic principles [9], [10], where the ordered sequence of elements is such that the value increases moving form the first to the last one, i.e. $C_i > C_j$, if $i > j$, the order statistic principle states that a capacitor value closer to the middle has smaller standard deviation,

and a capacitor which is far from center has larger standard deviation, therefore, the pairs C_1 and C_{64}, C_2 and C_{63} which have the largest standard deviation are at the extreme, while the pair C_{32} and C_{33} which has the smallest standard deviation is in the center, the standard deviation will change along the sequence with the minimum in the middle. Therefore, when using the array, small input signal around the middle (zero) will use the best capacitors.

In addition to the static optimal selection, the method alternates the 4 groups of capacitors in sequence, as shown in Fig. 6. The alternation of the 4 groups obtains a dynamic matching, further improving the performance of the capacitive DAC.

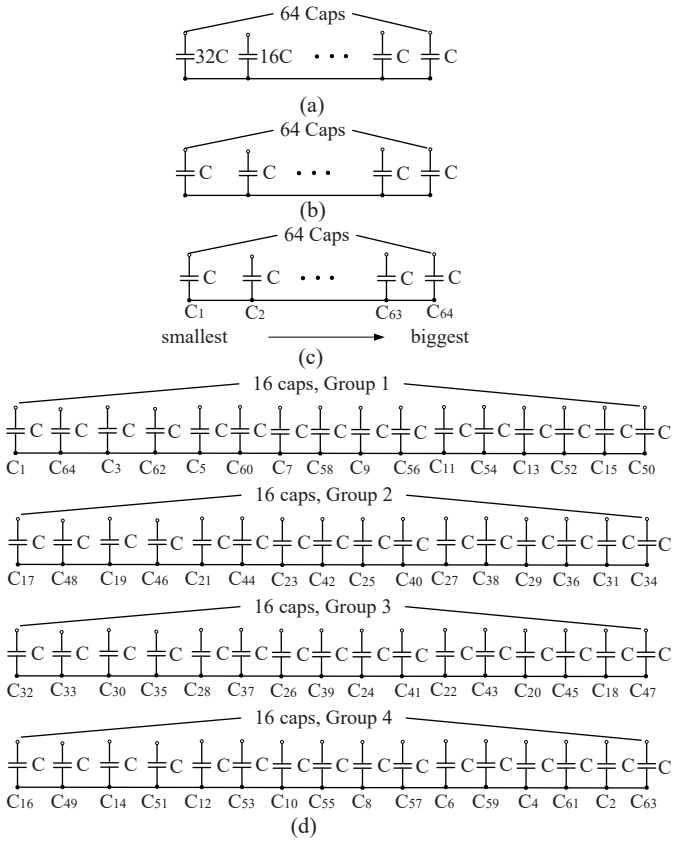

Fig. 5. Capacitor Optimization with 64 unit capacitors: (a) Conventional binary capacitive array in Fig. 3; (b) Split binary capacitive array into unary architecture; (c) Sort the 64 unit capacitors; (d) Divide the 64 unit capacitors into 4 groups.

IV. Simulation Results

Fig. 7 and Fig. 8 show the SFDR and SNDR results based on conventional, capacitor re-configuring proposed in [8] and capacitive array optimization technique proposed in this work for 500 Monte Carlo runs. After using the capacitive array optimization technique, the averaged SFDR is improved from 79.4 dB to 96.6 dB with $\sigma_u = 0.2\%$, 17.2 dB improvement of SFDR is achieved. Although capacitor re-configuring proposed in [8] can also improve SFDR by the same extent, extra 64

	32C	16C	8C 4C 2C C C
Vin(i)	Group1 & Group2	Group3	Group4
Vin(i+1)	Group4 & Group1	Group2	Group3
Vin(i+2)	Group3 & Group4	Group1	Group2
Vin(i+3)	Group2 & Group3	Group4	Group1
Vin(i+4)	Group3 & Group4	Group1	Group2
Vin(i+5)	Group4 & Group1	Group2	Group3
Vin(i+6)	Group1 & Group2	Group3	Group4
⋮	⋮	⋮	⋮

Fig. 6. Alternate 4 groups of capacitors in sequence.

capacitors were added to the capacitive array, and the difference between maximum value and minimum value of SFDR in the set of values obtained by the Monte Carlo simulation reaches 26.6 dB, also, the difference between maximum value and minimum value of SFDR in [7] reaches 27.5 dB(left of Fig. 4), the capacitive array optimization technique proposed can make the SFDR more concentrated in the center, the difference between maximum value and minimum value of SFDR from a Monte Carlo simulation with the same number of runs is only 6 dB, which means more stable performance enhancement. It is worth to mention that the concentration becomes more obvious for the SNDR and SNR results. In a word, the capacitive array optimization technique proposed in this work can achieve excellent performance enhancement without extra capacitors and without sacrificing the sampling rate of conventional SAR ADC.

Table II concludes 500 Monte Carlo SFDR, SNDR and SNR simulation results, improvement of SFDR is about 18 dB when σ_u varies from 0.1% to 0.4%, and for SNDR and SNR, better performance improvement can be achieved with worse σ_u, while the calibration technique proposed in [7] sacrifices the sampling rate a lot by converting the same input voltage four times, although capacitor re-configuring technique proposed in [8] does not alter the sampling rate of conventional SAR ADC, extra 64 unit capacitors were added to the capacitive array, leads to extra chip area and power consumption.

V. Conclusion

Optimization for capacitive array was proposed. Monte Carlo simulation results show that the differences between maximum value and minimum value of SFDR, SNDR and SNR are much smaller than the conventional calibration techniques, which means more stable performance enhancement can be achieved compared with the previous related works.

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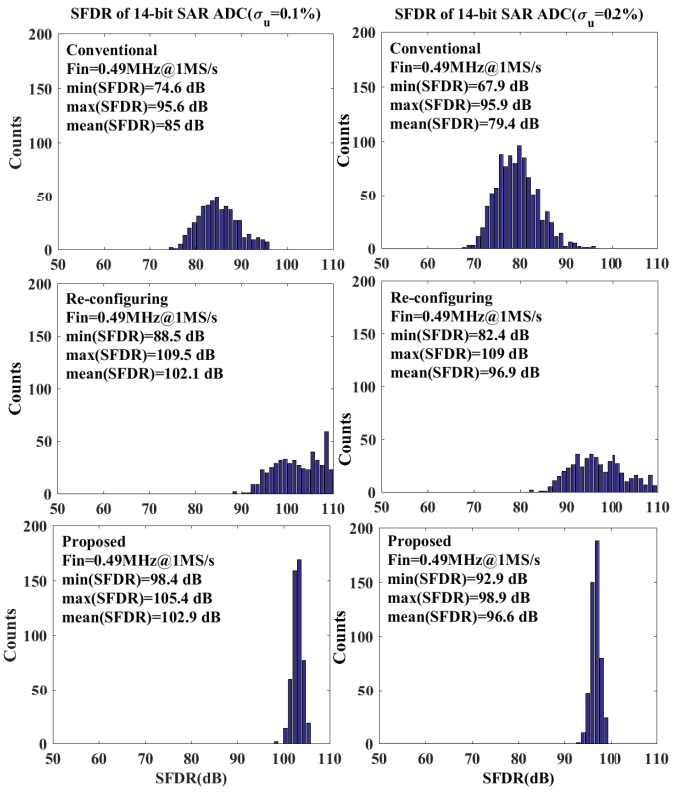

Fig. 7. 500 Monte Carlo SFDR simulation results for 14-bit SAR ADC with respectively Conventional, capacitor re-configuring and proposed with σ_u=0.1% (left) and σ_u=0.2% (right)

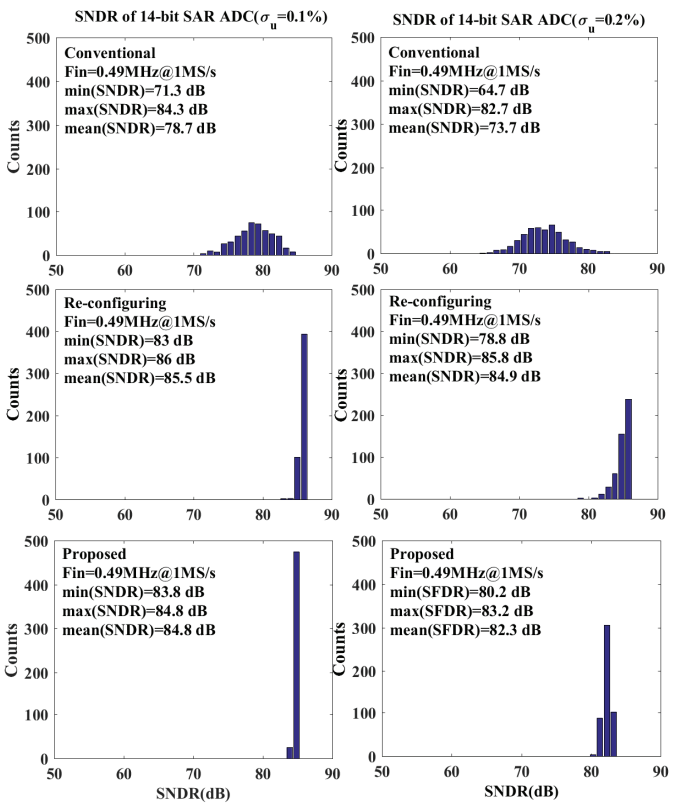

Fig. 8. 500 Monte Carlo SNDR simulation results for 14-bit SAR ADC with respectively Conventional, capacitor re-configuring and proposed with σ_u=0.1% (left) and σ_u=0.2% (right)

TABLE II
500 MONTE CARLO SFDR, SNDR AND SNR SIMULATION SUMMARY

	Conventional (dB)	Proposed (dB)	Improvement (dB)
mean(SFDR)(σ_u=0.1%)	85	102.9	17.9
mean(SFDR)(σ_u=0.2%)	79.4	96.6	17.2
mean(SFDR)(σ_u=0.3%)	75.4	93.5	18.1
mean(SFDR)(σ_u=0.4%)	72.9	91.1	18.2
mean(SNDR)(σ_u=0.1%)	78.7	84.8	6.1
mean(SNDR)(σ_u=0.2%)	73.7	82.3	8.6
mean(SNDR)(σ_u=0.3%)	70.2	80.1	9.9
mean(SNDR)(σ_u=0.4%)	67.7	78.1	10.4
mean(SNR)(σ_u=0.1%)	83.2	85.2	2
mean(SNR)(σ_u=0.2%)	79.5	82.9	3.4
mean(SNR)(σ_u=0.3%)	76.7	80.8	4.1
mean(SNR)(σ_u=0.4%)	74.6	78.9	4.3

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