A low-cost CMOS Neurological Sensor Array

P.Newman[1], P.Lisner[1], Y.Yeow[2], P.Choy[3], N.A Lavidis[3]

[1] School of Microelectronic Engineering, Griffith University, Nathan, QLD, Australia.
[2] School of Information Technology, University of Queensland, St Lucia QLD, Australia.
[3] School of Biomedical Science, University of Queensland, St. Lucia, QLD, Australia.

ABSTRACT

Current methods used to study neural communication have not been able to achieve both good spatial and temporal resolution of recordings. There are two ways to record synaptic potentials from nerve endings: recordings using single or dual intracellular or extra cellular metal electrodes give good temporal resolution but poor spatial resolution, and recording activity with fluorescent dyes gives good spatial resolution but poor temporal resolution. Such medical research activity in the area of neurological signal detection has thus identified a requirement for the design of a CMOS circuit that contains an array of independent sensors. As both spatial and temporal distribution of acquired data is required in this application, the circuit must be capable of continuous measurement of synaptic potentials from an array of points on a tissue sample, with a 10 μm separation between sensor points.

The major requirement for the circuit is that it is capable of sensing synaptic potentials of the order of several mV, with a resolution of 0.05 mV. For data recording purposes, the circuit must amplify these synaptic potentials and digitise them together with their locations in the sensor array. Finally, the circuit must be biologically inert, to avoid specimen deterioration.

This paper presents the design of a prototype single-chip circuit, which provides a 6 x 3 array of independent synaptic potential sensors. The signal from each of the sensors is amplified and time-multiplexed into an on-chip A/D converter. The circuit provides an 8-bit synaptic potential value, together with an 8-bit field containing array location and trigger signals suitable for external data acquisition instrumentation.

Our test circuit is implemented in a low-cost 0.5 um, 5 V CMOS process. The fabricated die is mounted in a standard 40 pin DIP ceramic package, with no lid to allow direct contact of the die surface with the tissue sample. The only post-processing step required for these packages is to encapsulate the exposed bond wires to ensure that the device is biologically inert. No further processing of the silicon die is required. Both the circuit design and the chip performance will be presented in the seminar.

Keywords: Neurological Sensor, Real-Time, Synaptic Potential

1. INTRODUCTION

RECENT research in the medical area has been looking into the operation of the nervous system. Specifically synaptic potentials have been an area of interest. This is the measurement of nerve impulses along a nerve. These signals are normally provided from an external stimulation. A short-sharp pulse is normally sufficient to start an action potential. An action potential is a nerve impulse that propagates in time. Figure A indicates the nerve impulse travels down the nerve with respect to time. The sensors in the array will be placed spatially as V1, V2, and V3 sensors in the figure so that a real-time reading can be taken tracking the position and amplitude.

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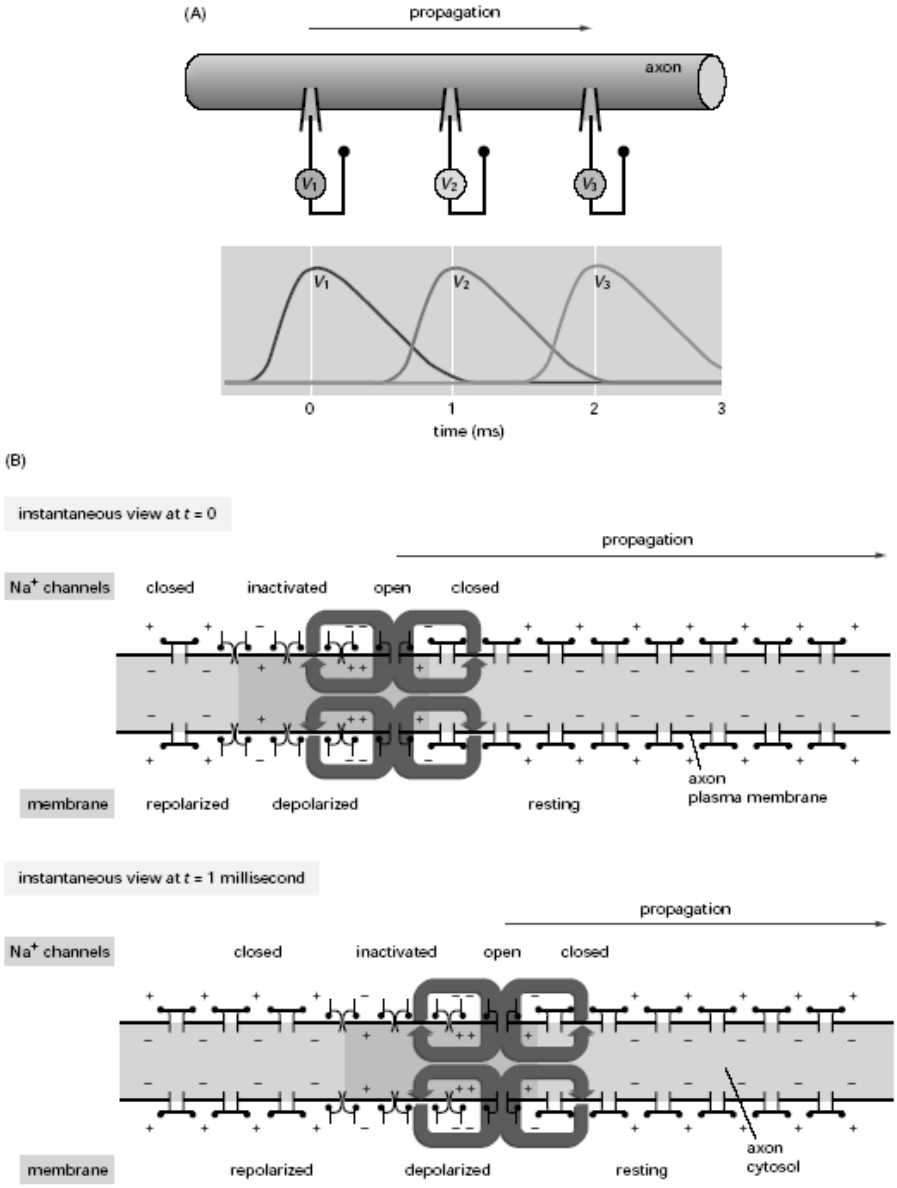

Figure A Action Potential Propagation on a nerve [2]

There are currently two methods for measuring synaptic potentials of nerve endings. The first is the use of fluorescent dyes which provides a spatial representation, but poor temporal resolution. The second method employs 20 μm platinum-saline probes which provide temporal resolution, but their cumbersome size limits spatial resolution.

These limitations have identified the requirement for a neurological sensor array that performs both types of measurement simultaneously. Ideally such an array would consist of sensors that are spaced 10 μm apart, measuring signals at a resolution of 0.05 mV. It would also be desirable to have a sensor-logger system that provides low-noise representation of the synaptic potentials with minimum artifact present. The main artifact of concern is stray noise that can be coupled into interconnecting wires. If we built a system on a monolithic chip then all signals would be processed locally without the need for long interconnecting wires connecting instrumentation needed to measure potentials. Since the output is digitised there is no chance it can get corrupted on external connections. An example waveform is

presented below in figure 1; note the amplitude and the bandwidth required to capture this signal.

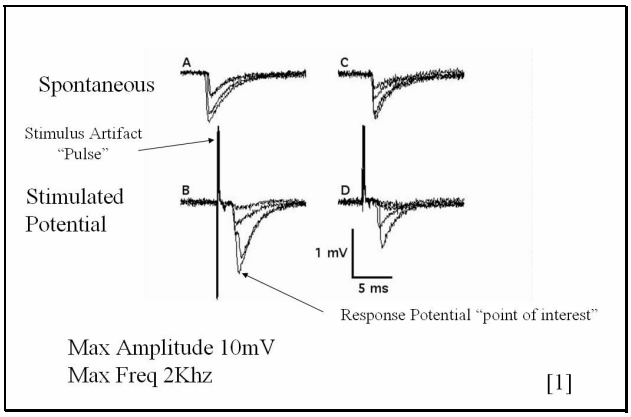

Figure 1 Sample synaptic waveform [1]

A low-cost system has been developed to perform the functions needed to measure synaptic potentials. This consists of a 6x3 sensor array. Each sensor input signal is fed into a differential amplifier, with a voltage gain of 500; so a sensor input signal of 5 mV will result in an amplifier output level of 2.5 V. In order to digitise the measurements all 18 signals are time division multiplexed at a rate controlled by an external clock signal, and input to an 8-bit analog to digital converter. The digital representations of the synaptic potentials measured by the sensors are then provided as system outputs. The system is implemented as a single chip CMOS device that uses a low-cost standard process. The chip has been fabricated through the MOSIS chip fabrication service, using the ami05 process.

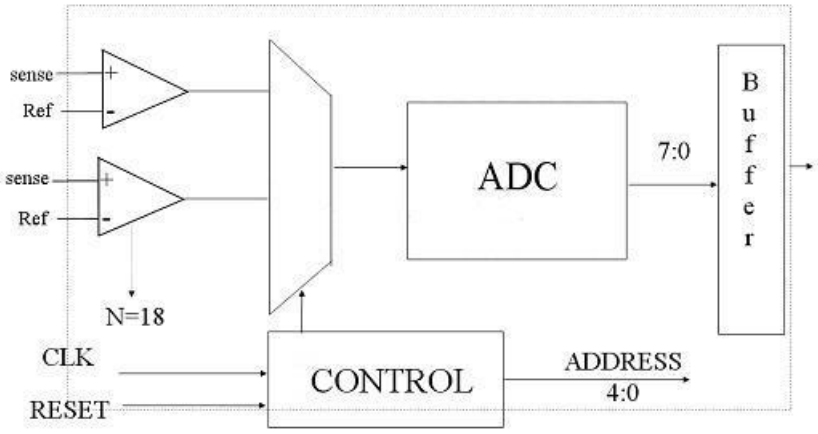

Figure 2 Sensor Array System Overview

Figure 2 provides an overview of the operation of the system.

The control block is a divide by 18 counter that increments with the leading edge of the clock input. The counter output drives the muliplexer select inputs; allowing one of 18 signal amplifier outputs to pass to the ADC block. The same selection signal also provides an index that is output alongside the digitised sensor measurement. This provides sensor position information with the measured synaptic potential at a particular time.

2. SENSOR DESIGN

The most important attribute of the neural sensor in this system is input sensitivity. Since the synaptic potentials are only in the mV range, this is essentially the noise floor for many systems, particularly since the signals only have a maximum bandwidth of 2 kHz.

The basic sensor consists of a CMOS MOSFET, slightly modified so that the gate voltage can be modulated by the potentials appearing at the nerve endings. A MOSFET is essentially a transconductance device in the mode of operation that is used in the sensing of synaptic potentials. E–Field coupling is the primary activation of the MOSFET in this case. For the MOSFET to work in this transconductance mode it must be biased in the active region. Thus the input voltage for the gate must be above the threshold voltage. This is achieved by biasing the tissue at a given DC voltage above the threshold voltage of the transistor. The transconductance of the transistor is linear in this region.

The nerve ending also has an equivalent circuit which represents the junction impedance. It is represented by a resistor in parallel with a capacitor. The resistor value is 6.8 MΩ and the capacitor value is 800 pF. Three different methods were considered to form the interface between the transistor gate and the nerve ending.

2.1. Stacked Via Implementation

The stacked via implementation would be most compatible with the AMI05 process from MOSIS as it only uses standard CMOS layout design rules. The only concern is the capacitance that is present at the nerve to metal 3 interface. This is mainly dependent on the dielectric constant of the overglass layer. A small resistive component is also added in series. The silicon dioxide dielectric constant of 40pF/m^2, with an overglass thickness of 1 μm gives an equivalent capacitance at this junction of 0.0045 fF. The series resistance of the vias used to build from the overglass layer to the polysilicon layer is insignificant compared with the 6.8 MΩ resistance of the nerve interface [1]. This can result in increased signal coupling, but appeared as the most practical way to implement this sensing method. If the final overglass window can be opened directly above the gate, the input capacitance of the nerve to gate interface will be significantly reduced. This overglass layer has been left intact to protect the device aluminum metal layers. As the system will be placed in a saline bath it is important to minimise the risk of corrosion of the metal layers and consequent specimen contamination.

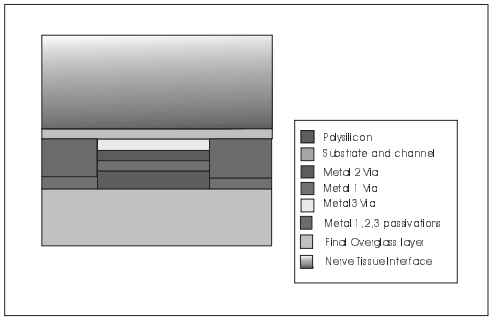

Figure 3 Stacked via Sensor interface

2.2. Passivation removed

In this implementation the overglass and vias were not used to form the junction between the gate and the nerve ending. This implementation moves away from the standard CMOS implementation that was a desirable attribute of this system. One advantage with using this method is the reduction of the input capacitance that was formed by both the stacked vias and the overglass dielectrics. E-field coupling is also improved given the closer proximity of the nerve cell to the polysilicon gate.

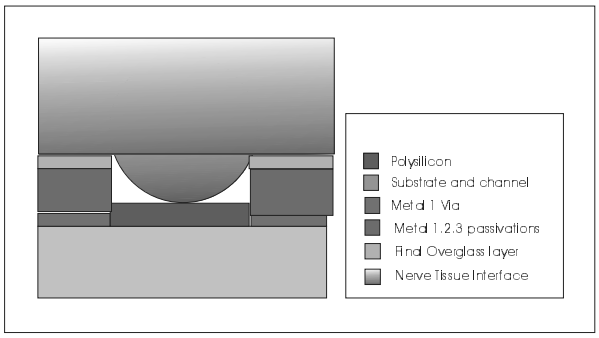

Figure 4 Sensor interface with no overglass and no vias

2.3. Polyless Gate implementation

This implementation is the most specialized implementation proposed to sense synaptic potentials. This design represents the ideal E-field coupled gate bias solution. Manufacturing difficulties of this device in standard CMOS processes exist since the polysilicon has to be removed as well as the overglass and vias. The proximity of the nerve to the substrate will give maximum modulation and sensitivity.

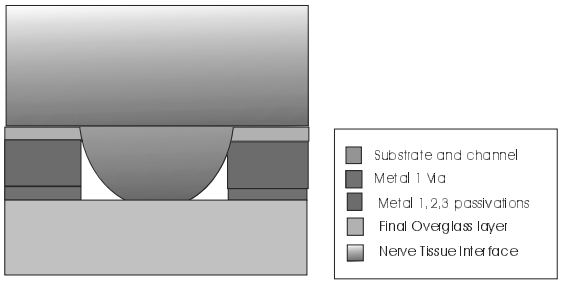

Figure 5 Polyless gate implementation

This implementation also departs from the low-cost design goal since the polysilicon that must be removed provides the self-aligning feature of the standard CMOS process. Also the high aspect ratio sides of the window mean that the window will probably have distorted profile which would decrease the amount of nerve in contact with the substrate.

The stacked via implementation was finally chosen for the prototype design since it is compatible with the standard CMOS process and forms the most protective interface for the electronics embedded in the substrate.

3. AMPLIFIER DESIGN

A differential amplifier design was chosen to reduce the noise level present at the input to the analog to digital converter. The high common-mode rejection of a differential amplifier minimises noise induced from supplies and leads used to power the device.

Since the spacing of the sensor MOSFET s must be less than 20 microns, this limited the channel width of the sensor transistor to a maximum value of 5 µm. The width of the input transistor was set at 2.5µm with a channel length of 0.5 µm. The disadvantage of using small devices is that manufacturing variations result in significant device mismatch, which increase the offset voltage at the output of the amplifier. The differential amplifier stage is not required to have a large gain but must acquire a good quality signal and maintain this signal quality up to the input of the output stage.

The output of this amplifier can be represented by:

$$Vout = Av(Vin - Vref) + Voffset$$

The input Vref is attached to the same bias as the saline bath. Av is a set to be 1. The offset voltage Voffset has been trimmed so the offset voltage of the output is $\frac{1}{2}Vdd$.

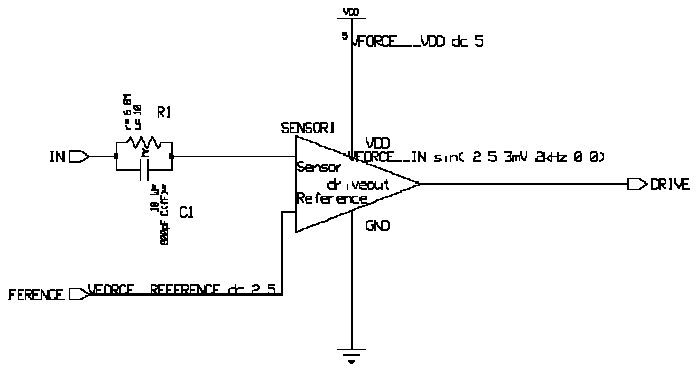

Figure 6 Amplifier Block Diagram Showing Inputs and nerve junction equivalent circuit

The differential stage output is fed into a high gain voltage amplifier optimized to operate around the offset voltage of the differential amplifier. The product of the gain of the differential amplifier and the output stage is around 500.

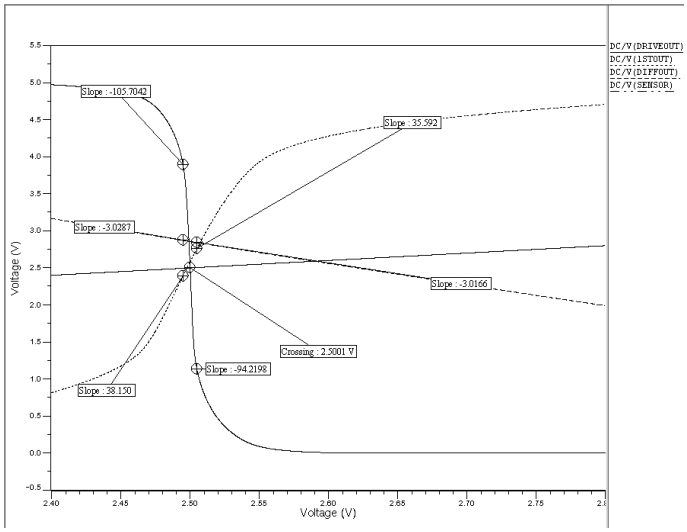

Figure 7 Gain for the differential and output stages of the sensor amplifier

The function of the output stage is to provide a high gain stage that is capable of driving larger loads than that of the input stage. For example a capacitive load of 100 fF is typical. For this output stage it was desirable to maximise the output voltage in order to maximise dynamic range. It is desirable for the amplifier to give maximum gain since the quantisation level size of the analog to digital converter will be the dynamic range divided into 256 levels.

The output stage consists of two inverting amplifier stages which achieve large gain when the input voltage is in the vicinity of ½ Vdd. It can be seen from figure 7 that the output signal of the differential stage contains a small D.C

offset. The operating range of the output stage is optimized to function at the offset voltage of the first stage. The drive strengths of the PMOS and NMOS devices are trimmed to ensure the amplifier will operate at the offset voltage of the first stage.

Specifications for the sensor amplifier:

Common-Mode Input	2.5V
Max small signal input	10mVpp
Supply Voltage	5V/ GND
Slew Rate	6.95 mV/ µsec
Offset Voltage	2.5V
Open Loop Gain	300 Typ 95 Min 350 Max
Operating Temperature	27 °C±2
Rise Time	4 µs (10% - 90%)Vdd

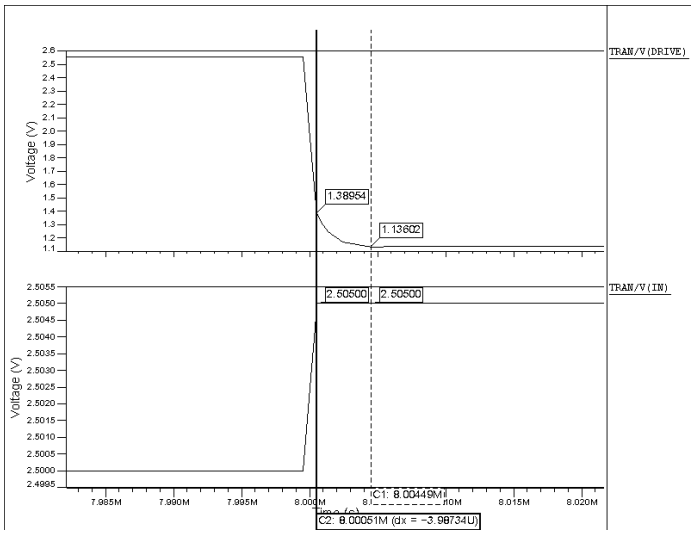

Figure 8 Measurement of the Slew Rate of the amplifier

4. MULTIPLEXER

The multiplexer was used to provide an input signal to the ADC from the array of 17 amplifiers and enable sequential output of signals. The eighteenth amplifier is not included in the ADC input selection as it has a dedicated analog output pin for testing the interface sensing element performance. The Multiplexer in this circuit consists of 17 MOSFET transmission gates. They are controlled by a divide by 17 counter. The clocking for this counter is supplied as a 180KHz input to the chip. The small dimensions of the transmission gates result in a small load on the outputs of the sensor amplifiers.

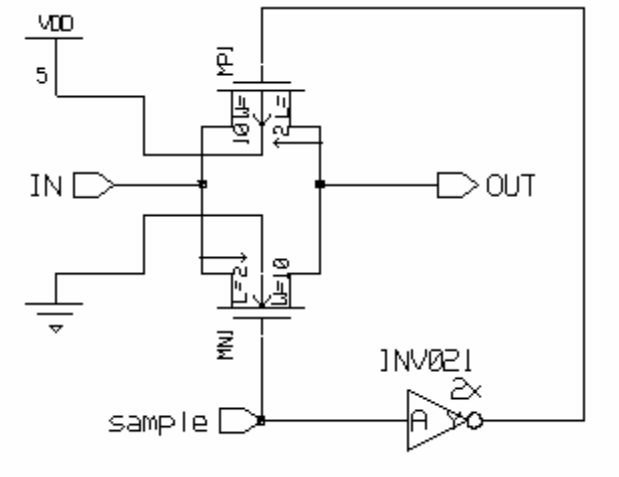

Figure 9 Schematic of the Multiplexer

IN	OUT	Sample
0	0	1
1	1	1
1	Xxx	0
1	Xxx	0

Figure 10 Truth Table for the Multiplexer

5. ANALOG TO DIGITAL CONVERTER

The architecture used in this design is the Flash parallel converter. This converter is 8-bit and has a target input voltage range of 1v to 4volts. This results in a quantisation level of 3v/256 =11.7 mV. For the design of the comparators the maximum error can no more that half of 11.7mV and hysteresis must not exceed 1/4 of the quantisation level. Reference voltages are provided by a high resistance Polysilicon bridge of 258 resistors. The flash converter presents quite a large capacitive load on the sensor amplifiers that must drive them through the Multiplexer. This value must be small enough so the ADC has enough time to acquire the input signal within the required half period of the clock which would be 2.5 µs. An additional significant characteristic of this Converter is the extremely small hysteresis that is present. This is due to the comparators being trimmed to operate at specific voltage ranges.

5.1. Sample and Hold

The sample and hold for ADC consist of a transmission gate. The capacitance that is present from the sampler to comparator network gives sufficient capacitance to capture the input signal for the required time span which is 2.5 µs.

The sampler must also not decay more than 10% of a quantisation level during the time that it is holding so that a good quantisation is completed. Since the quantisation level is 11.7 mV, the decay can not be more than 1.1 mV.

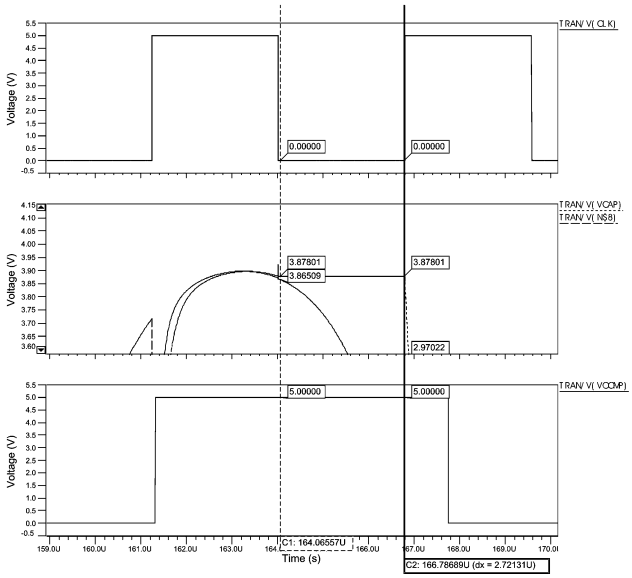

Figure 11 Sample and Hold test waveforms

5.2. Comparators

The comparators used in this design were low hysteresis design to minimise the amount of error in the quantisation of the signal [3]. Simulations showed maximum hysteresis at 500 μV which is 5% of a quantisation level. In a typical operating environment there would be hysteresis due to routing capacitances and transistor sizing mismatch. Hysteresis describes how the trigger point on a comparator changes on whether the input is presented as a positive slope or as a negative slope. The type of optimization would not be as easy to accomplish on a SAC analog to digital converter. The successive approximation ADC uses one comparator over the full range of inputs presented. A SAC converter works by incrementing a counter which is connected to a DAC. The output of this DAC is compared to the analog input of the system, when a match is found the counter is stopped and the binary counter value is returned. The flash converter whilst much larger than the SAC converter can have multiple comparators optimized each to a particular operating range. This will reduce irregularities in trigger points for ADC's.

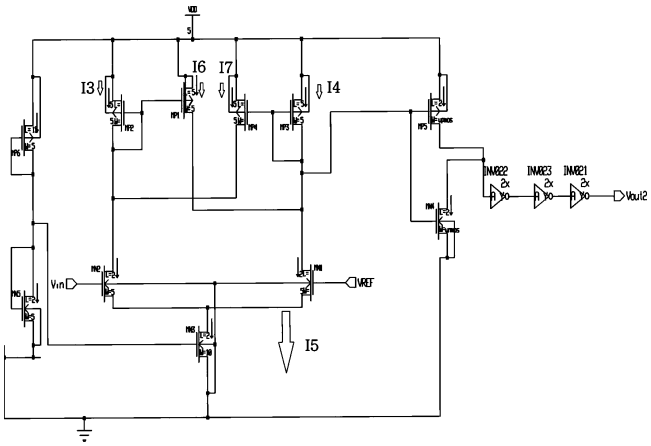

Figure 12 Comparator Schematic

The comparators were simulated in their operating range to give a quantisation level of less than 5 mV.

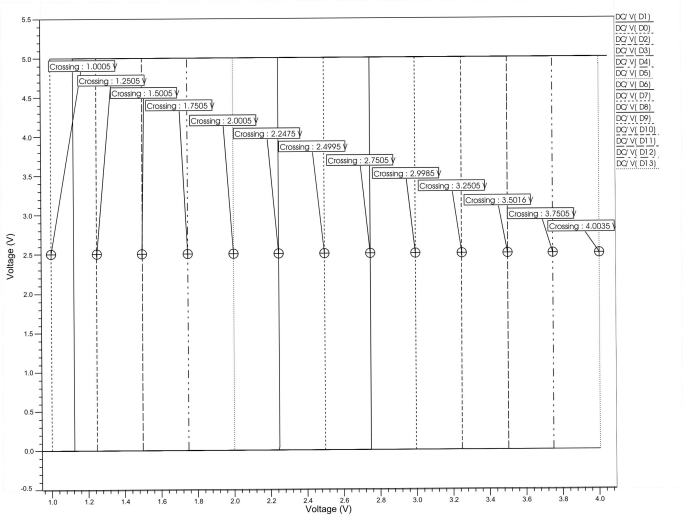

Figure 13 Comparator trigger test points

6. LAYOUT

The sensors were placed in the centre of the die, which allowed placement of the amplifiers around the sensors. Ground shields were used to minimise crosstalk between the sensor elements and the amplifiers was minimised, again to minimise crosstalk, as seen in Figure 14. The sensor to sensor spacing is 7.5 µm which is well under the maximum specified of 20 µm. The sensors have also been placed in an interdigital arrangement that increases the proximity of the sensor to the nerve endings in figure 15.

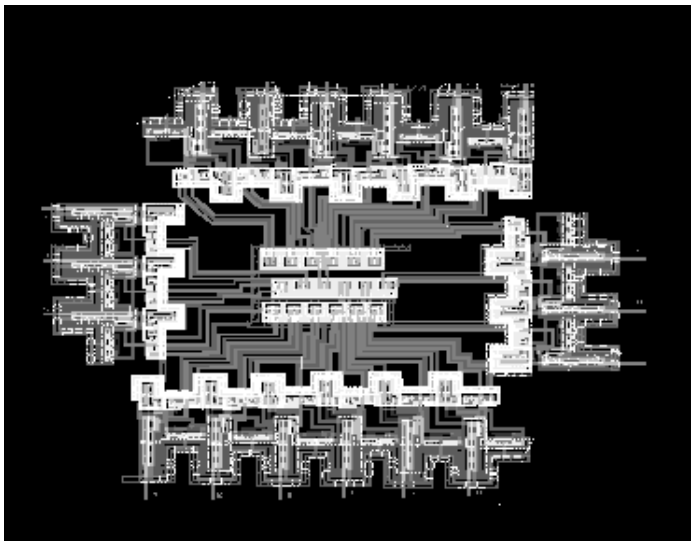

Figure 14 Sensor Array and op amp Layout

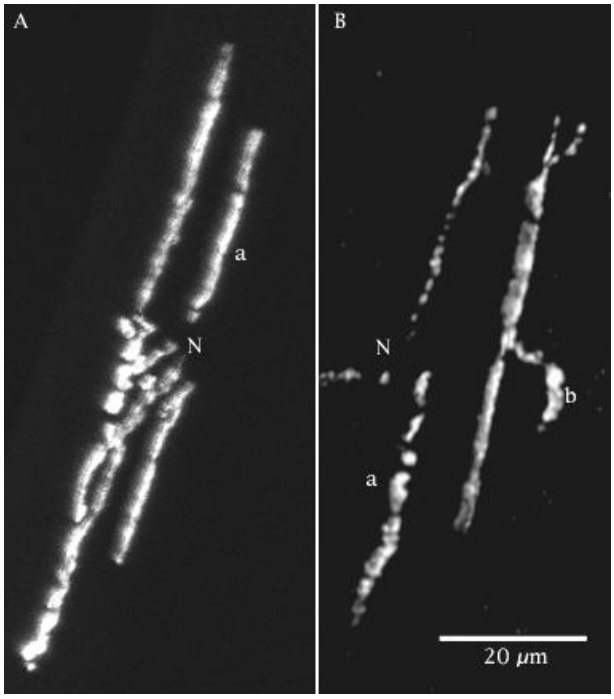

Figure 15 Micrographs of nerve terminal structures used to test the array note the 20 μm scale [4]

7. CONCLUSIONS

An 18 node (6x3) neuron sensor array has been designed and simulated using Mentor Graphics™ with the ami05 process. All sections have simulated and give the following performance parameters.

Amplifier Gain	300
Sampling Frequency	36 kHz
Signal to Noise Ratio	13dB
Number of sensors	18
Analog Amplifier out Ports	1
Max Comparator error	25% of quantisation level
ADC Quantisation Level	11 mV
ADC Resolution	8 –bits
Max ADC Conversion rate	Approx 20 MHz
Sensor Address output	5 bits TTL CMOS compatible
Power Supply	Vdd =5v Vss = GND
Max neuron signal bandwidth	1 kHz

The system is envisaged to be fabricated and tested early in 2005. The extra work involved routing compact low-noise layers of aluminium also took more time than anticipated. Simulations look promising for the first prototype test run.

The system will now be completed in the layout stage and masks will be sent to MOSIS to be manufactured. The die will be mounted in a standard 48-pin DIP package. This will need to be sealed with a silicone compound to seal against the saline bath that will be used in testing. Testing will be performed on a frog nerve placed along the sensor array in direct contact in a saline bath at 27 °C. The chip digital output and clock will be connected to a computer for logging purposes. An action potential will be initiated at one extremity of the nerve and the propagating impulses will be

captured with the array and sent to the computer. The control sensor output will provide an analog output for testing and debugging of the sensor interface.

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