Quantum-error correction on linear-nearest-neighbor qubit arrays

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A quantum circuit implementing 5-qubit quantum-error correction on a linear-nearest-neighbor architecture is described. The canonical decomposition is used to construct fast and simple gates that incorporate the necessary swap operations allowing the circuit to achieve the same depth as the current least depth circuit. Simulations of the circuit's performance when subjected to discrete and continuous errors are presented. The relationship between the error rate of a physical qubit and that of a logical qubit is investigated with emphasis on determining the concatenated error correction threshold.

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The field of quantum computation deals with the manipulation of 2-state quantum systems called qubits. Many different physical systems are being investigated in the race to build a scalable quantum computer [1–6]. Due to the fragility of quantum systems, one property a scalable architecture must possess is the ability to implement quantum-error correction (QEC) [7–9]. The question has been raised as to how well QEC can be implemented on a linear-nearest-neighbor (LNN) quantum computer [10] due to the expectation that numerous swap gates will be required. Working out a way around this is important due to the large number of LNN architectures currently under investigation [11–23]. In this paper a 5-qubit QEC circuit appropriate for a LNN architecture is presented that achieves the same depth as the best known circuit for an architecture able to interact arbitrary pairs of qubits [24]. In this paper, the depth of the circuit is used as a measure of quality of the circuit due to the need to minimize the overall circuit time so that it is short in comparison to the decoherence time of an individual qubit. A QEC circuit will not function unless this condition is met.

The paper is organized as follows. First, the canonical decomposition used to construct efficient 2-qubit gates is discussed in brief. Details of the method used can be found in Ref. [25]. The Kane architecture [1] has been used to construct explicit decompositions, but the methods described apply to any architecture. The 5-qubit QEC scheme is then discussed and the LNN circuit presented. Following this, simulations of quantum data storage with and without QEC are presented. The paper concludes with a summary of all results.

The canonical decomposition enables any 2-qubit operator U_{AB} to be expressed (nonuniquely) in the form $V_A^\dagger \otimes V_B^\dagger U_d U_A \otimes U_B$ where U_A, U_B, V_A, and V_B are single-qubit unitaries and $U_d = \exp[i(\alpha_x X \otimes X + \alpha_y Y \otimes Y + \alpha_z Z \otimes Z)]$ [25]. Moreover, any entangling interaction can be used to create an arbitrary U_d up to single-qubit rotations [26]. These two facts allow the construction of very efficient composite gates on any physical architecture. Figure 1(a) shows the form of such a decomposed controlled-NOT (CNOT) gate on a Kane quantum computer [1,27]. The 2-qubit interaction corresponds to $\alpha_x = \alpha_y = \pi/8$ and $\alpha_z = 0$. Z rotations have been represented by quarter, half, and three-quarter circles corresponding to $R_z(\pi/2)$, $R_z(\pi)$, and $R_z(3\pi/2)$, respectively. Full circles represent Z rotations of angle dependent on the physical construction of the computer. Square gates 1 and 2 correspond to X rotations $R_x(\pi)$ and $R_x(\pi/2)$. Figure 1(b) shows an implementation of the composite gate Hadamard followed by CNOT gate which is followed by swap gate (HCNOTS). Note that the total time of the compound gate is significantly less than the CNOT gate on its own.

The above implies that the swaps inevitably required in a LNN architecture to bring qubits together to be interacted

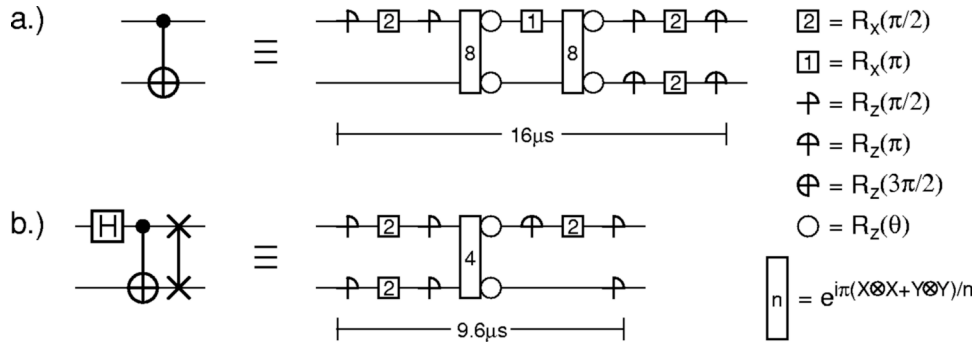

FIG. 1. Decomposition into physical operations of (a) CNOT gate, (b) Hadamard gate, CNOT gate, then swap gate. Note that the Kane architecture has been used for illustrative purposes. In addition to the clear speed advantage when implementing compound gates, the decomposed CNOT gate is faster than its adiabatic equivalent (26 μs) [28].

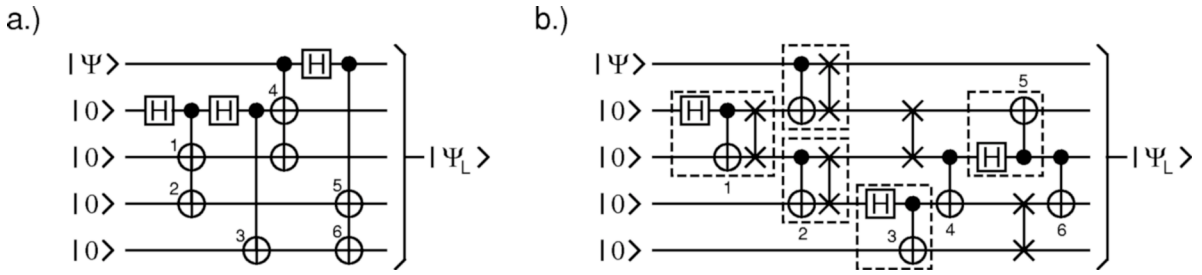

FIG. 2. 5-qubit encoding circuit for general architecture and (b) equivalent circuit for linear-nearest-neighbor architecture with dashed boxes indicating compound gates. CNOT gates that must be performed sequentially are numbered.

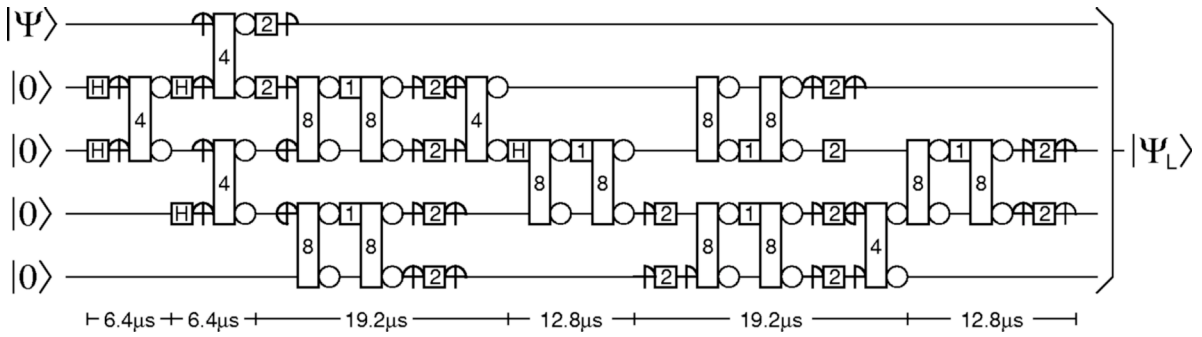

FIG. 3. A sequence of physical gates implementing the circuit of Fig. 2(b). Note the Kane architecture has been used for illustrative purposes.

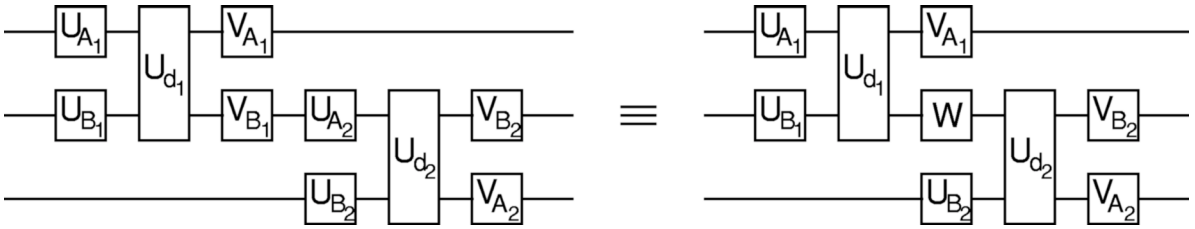

FIG. 4. Circuit equivalence used to reduce the number of physical gates in Fig. 3.

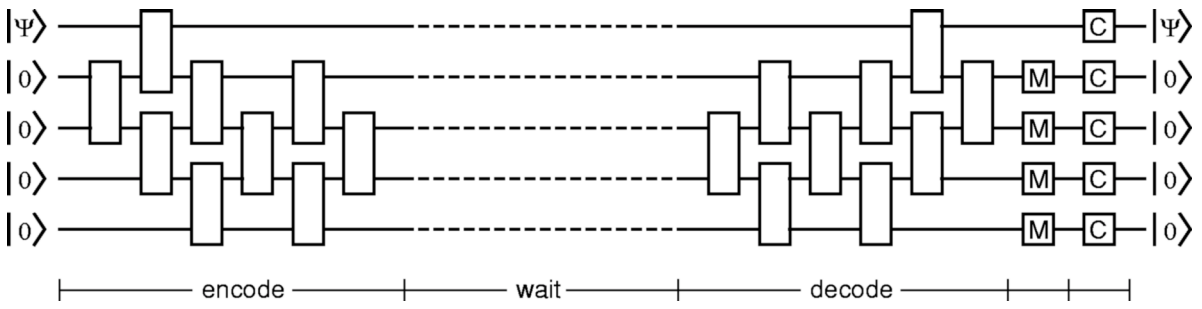

FIG. 5. A complete encode-wait-decode-measure-correct QEC cycle.

TABLE I. Action required to correct the data qubit Ψ' vs measured value of ancilla qubits. Note that the X operations simply reset the ancilla.

Measurement	Action
$\Psi' \otimes 0000$	$I \otimes IIII$
$\Psi' \otimes 0001$	$I \otimes IIIX$
$\Psi' \otimes 0010$	$I \otimes IIXI$
$\Psi' \otimes 0011$	$Z \otimes IIXX$
$\Psi' \otimes 0100$	$I \otimes IXII$
$\Psi' \otimes 0101$	$X \otimes IXIX$
$\Psi' \otimes 0110$	$Z \otimes IXXI$
$\Psi' \otimes 0111$	$X \otimes IXXX$
$\Psi' \otimes 1000$	$Z \otimes XIII$
$\Psi' \otimes 1001$	$I \otimes XIIX$
$\Psi' \otimes 1010$	$X \otimes XIXI$
$\Psi' \otimes 1011$	$X \otimes XIXX$
$\Psi' \otimes 1100$	$Z \otimes XXII$
$\Psi' \otimes 1101$	$Z \otimes XXII$
$\Psi' \otimes 1110$	$XZ \otimes XXXI$
$\Psi' \otimes 1111$	$Z \otimes XXXX$

can be incorporated into other gates without additional cost. Indeed, in certain cases LNN circuits built out of compound gates are actually faster.

5-qubit quantum-error correction schemes are designed to correct a single arbitrary error. No single error correction scheme can use less than 5 qubits [29]. A number of 5-qubit QEC proposals exist [8,9,24,30,31]. Figure 2(b) shows a circuit appropriate for a LNN architecture implementing the encode stage of the QEC scheme proposed in Ref. [24]. For reference, the original circuit is shown in Fig. 2(a). Note that the LNN circuit uses exactly the same number of CNOT gates and achieves minimal depth since the CNOT gates numbered 1–6 in Fig. 2(a) must be performed sequentially on any architecture that can only interact pairs of qubits (not 3 or more at once). The two extra "naked" swap gates in Fig. 2(b) do not significantly add to the total time of the circuit. Figure 3 shows an equivalent circuit broken into physical operations for a Kane quantum computer. Note that this circuit uses the fact that if two 2-qubit gates share a qubit then two single-qubit unitaries can be combined as shown in Fig. 4. The decode circuit is simply the encode circuit run backwards. All 5-qubit QEC schemes are only useful for data storage [9] due to the difficulty of interacting two logical qubits. Figure 5 shows a full encode-wait-decode-measure-correct data storage cycle. Table I shows the range of possible measurements and the action required in each case.

When simulating the QEC cycle, the circuit of Fig. 2(b) was used to keep the analysis architecture independent. Each gate was modeled as taking the same time, allowing the time T to be made an integer such that each gate takes one time step. Gates were furthermore simulated as though perfectly reliable and errors applied to each qubit (including idle qubits) at the end of each time step. The rationale for including idle qubits is that in a LNN architecture physical manipulation of some description is required to decouple neighboring qubits, which inevitably leads to errors.

TABLE II. Probability per time step ϵ_{step} of a discrete error when using 5-qubit QEC vs physical probability p per qubit per time step of a discrete error.

p	T_{opt}	ϵ_{step}	ϵ_{step}/p
10^{-2}	25	1.7×10^{-2}	1.7×10^{0}
1.6×10^{-3}	40	1.6×10^{-3}	1.0×10^{0}
10^{-3}	50	8.4×10^{-4}	8.4×10^{-1}
10^{-4}	150	3.1×10^{-5}	3.1×10^{-1}
10^{-5}	750	1.1×10^{-6}	1.1×10^{-1}
10^{-6}	1500	3.2×10^{-8}	3.2×10^{-2}
10^{-7}	6000	1.1×10^{-9}	1.1×10^{-2}
10^{-8}	10000	2.0×10^{-11}	2.0×10^{-3}

Two error models were used—discrete and continuous. In the discrete model a qubit can suffer either a bit flip (X), phase flip (Z), or both simultaneously (XZ). Each type of error is equally likely with total probability of error p per qubit per time step. The continuous error model involves applying single-qubit unitary operations of the form

$$U_\sigma = \begin{pmatrix} \cos(\theta/2)e^{i(\alpha+\beta)/2} & \sin(\theta/2)e^{i(\alpha-\beta)/2} \\ -\sin(\theta/2)e^{i(-\alpha+\beta)/2} & \cos(\theta/2)e^{i(-\alpha-\beta)/2} \end{pmatrix}, \quad (1)$$

where α, β, and θ are normally distributed about 0 with standard deviation σ.

Both the single-qubit and single-logical qubit (5 qubits) systems were simulated. The initial state

$$|\Psi\rangle = \sin(\pi/8)|0\rangle + \cos(\pi/8)|1\rangle \quad (2)$$

was used in both cases as $|\langle\Psi|X|\Psi\rangle|^2 = 0.5$, $|\langle\Psi|Z|\Psi\rangle|^2 = 0.5$, and $|\langle\Psi|XZ|\Psi\rangle|^2 = 0$ thus allowing each type of error to be detected (but not necessarily distinguished). Simpler states such as $|0\rangle$, $|1\rangle$, $(|0\rangle+|1\rangle)/\sqrt{2}$, and $(|0\rangle-|1\rangle)/\sqrt{2}$ do not have this property. For example, the states $|0\rangle$ and $|1\rangle$ are insensitive to phase errors, whereas the other two states are insensitive to bit flip errors.

Let T_{wait} denote the duration of the wait stage. Note that the total duration of the encode, decode, measure, and correct stages is 14. In the QEC case the total time $T = T_{wait} + 14$ of one QEC cycle was varied to determine the time that minimizes the error per time step

$$\epsilon_{step} = 1 - \sqrt[T]{1 - \epsilon_{final}}, \quad (3)$$

where $\epsilon_{final} = 1 - |\langle\Psi'|\Psi\rangle|^2$ and $|\Psi'\rangle$ is the final logical qubit state. An optimal time T_{opt} exists since the logical qubit is only protected during the wait stage and the correction process can only cope with one error. If the wait time is zero, extra complexity has been added but no corrective ability. Similarly, if the wait time is very large, it is almost certain that more than one error will occur, resulting in the qubit being destroyed during the correction process. Somewhere between these two extremes is a wait time that minimizes ϵ_{step}. Table II shows T_{opt}, ϵ_{step}, and the reduction in error

TABLE III. Probability per time step ϵ_{step} of a discrete error when using 5-qubit QEC vs standard deviation σ of continuous errors.

σ	T_{opt}	p	ϵ_{step}	ϵ_{step}/p
10^{-1}	2.5×10^{1}	5.9×10^{-2}	6.9×10^{-3}	1.2×10^{-1}
10^{-2}	2.5×10^{2}	5.9×10^{-3}	1.4×10^{-5}	2.4×10^{-3}
10^{-3}	2.5×10^{3}	6.0×10^{-4}	1.3×10^{-8}	2.2×10^{-5}
10^{-4}	2.5×10^{4}	6.0×10^{-5}	1.0×10^{-11}	1.7×10^{-7}
10^{-5}	2.5×10^{5}	6.0×10^{-6}	7.2×10^{-15}	1.2×10^{-9}

ϵ_{step}/p versus p for discrete errors. Table III shows the corresponding data for continuous errors. Note that, in the continuous case, the single qubit p has been obtained via 1-qubit simulations and a 1-qubit version of Eq. (3).

The range of threshold error rates p in the literature is enormous, from a very pessimistic $p=10^{-8}$ [32] to a very optimistic $p=2\times10^{-3}$ [33]. The threshold $p=1.6\times10^{-3}$ shown in Table II is comparable to the most optimistic previous estimate which was made using 7-qubit fault tolerant QEC with errors applied only after gate operations and not to idle qubits. This threshold should not, however, be thought of as the allowable operating error rate of a physical quantum computer as precisely no improvement in error rate is achieved when using QEC. If an error rate improvement of a factor of 10 or 100 is desired when using QEC then $p=10^{-5}$ or $p=10^{-7}$ is required, respectively. Further work is required to determine the error rate improvement required to allow robust implementation of large scale quantum algorithms with a reasonable number of error correction qubits.

For continuous errors, there is no true threshold. Even for very large random unitary rotations an improvement is still gained by using the LNN QEC circuit. In this case, provided gates can be implemented such that the angles associated with the continuous error model are of order 10^{-2}, an improvement in error rate of at least a factor of 100 can be achieved.

Further work is required to determine whether the discrete or continuous error model or some other model best describes errors in physical quantum computers.

In conclusion, we have presented a circuit 5-qubit QEC for a LNN architecture, which achieves the same depth as the current least depth circuit [24], and simulated its effectiveness against both discrete and continuous errors. For the discrete error model, if error correction is to provide an error rate reduction of a factor of 10 or 100, the physical error rate p must be 10^{-5} or 10^{-7}, respectively. For the continuous error model, it was acceptable for error angles to have a standard deviation of up to 10^{-2} rad, as using QEC still gives an error rate improvement better than a factor of 100.

Further simulation is required to determine the error thresholds associated with 1- and 2-qubit LNN error-corrected gates.

[1] B. E. Kane, Nature (London) **393**, 133 (1998).
[2] H.-A. Engel *et al.*, Solid State Commun. **119**, 229 (2001).
[3] V. Giovannetti *et al.*, J. Mod. Opt. **47**, 2187 (2000).
[4] E. Hinds, Phys. World July, 39 (2001).
[5] D. F. V. James, Fortschr. Phys. **48**, 823 (2000).
[6] J. E. Mooij, Microelectron. Eng. **47**, 3 (1999).
[7] P. W. Shor, Phys. Rev. A **52**, R2493 (1995).
[8] R. Laflamme *et al.*, Phys. Rev. Lett. **77**, 198 (1996).
[9] J. Niwa *et al.*, e-print quant-ph/0211071.
[10] D. Gottesman, J. Mod. Opt. **47**, 333 (2000).
[11] R. Vrijen *et al.*, Phys. Rev. A **62**, 012306 (2000).
[12] B. Golding and M. I. Dykman, e-print cond-mat/0309147.
[13] L. C. L. Hollenberg *et al.*, e-print cond-mat/0306235.
[14] L. Tian and P. Zoller, Phys. Rev. A **68**, 042321 (2003).
[15] M. Feng *et al.*, e-print quant-ph/0304169 (2003).
[16] J. K. Pachos and P. L. Knight, Phys. Rev. Lett. **91**, 107902 (2003).
[17] L. M. K. Vandersypen *et al.*, e-print quant-ph/0207059.
[18] P. Solinas *et al.*, Phys. Rev. B **67**, 121307 (2003).
[19] J. H. Jefferson *et al.*, Phys. Rev. A **66**, 042328 (2002).
[20] D. Petrosyan and G. Kurizki, Phys. Rev. Lett. **89**, 207902 (2002).
[21] T. D. Ladd *et al.*, Phys. Rev. Lett. **89**, 017901 (2002).
[22] V. V'yurkov and L. Y. Gorelik, e-print quant-ph/0009099.
[23] E. O. Kamenetskii and O. Voskoboynikov, e-print cond-mat/0310558.
[24] S. L. Braunstein and J. A. Smolin, Phys. Rev. A **55**, 945 (1997).
[25] B. Kraus and J. I. Cirac, Phys. Rev. A **63**, 062309 (2001).
[26] M. J. Bremner *et al.*, Phys. Rev. Lett. **89**, 247902 (2002).
[27] C. D. Hill and H.-S. Goan, Phys. Rev. A **68**, 012321 (2003).
[28] A. G. Fowler *et al.*, Phys. Rev. A **67**, 012301 (2003).
[29] M. A. Nielson and I. L. Chuang, *Quantum Computation and Quantum Information* (Cambridge University Press, Cambridge, 2000)
[30] E. Knill *et al.*, Phys. Rev. Lett. **86**, 5811 (2001).
[31] C. H. Bennett *et al.*, Phys. Rev. A **54**, 3824 (1996).
[32] E. Knill *et al.*, e-print quant-ph/9610011.
[33] C. Zalka, e-print quant-ph/9612028.