Accurate Modeling of the Effects of Fringing Area Interface Traps on Scanning Capacitance Microscopy Measurement

Yang David Hong, Yew Tong Yeow, *Senior Member, IEEE*, Wai Kin Chim, *Senior Member, IEEE*, Jian Yan, and Kin Mun Wong

***Abstract*—Scanning capacitance microscopy (SCM) is a dopant profile extraction tool with nanometer spatial resolution. While it is based on the high-frequency MOS capacitor theory, there are crucial second-order effects which make the extraction of dopant profile from SCM data a challenging task. Due to the small size of the SCM probe, the trapped charges in the interface traps at the oxide–silicon dioxide interface surrounding the probe significantly affect the measured SCM data through the fringing electric field created by the trapped charges. In this paper, we present numerical simulation results to investigate the nature of SCM dC/dV data in the presence of interface traps. The simulation takes into consideration the traps' response to the ac signal used to measure dC/dV as well as the fringing field of the trapped charge surrounding the probe tip. In this paper, we present an error estimation of experimental SCM dopant concentration extraction when the interface traps and fringing field are ignored. The trap distribution in a typical SCM sample is also investigated.**

***Index Terms*—Dopant profile extraction, interface traps, scanning capacitance microscopy (SCM), semiconductor device modeling, simulation.**

I. Introduction

With THE rapid shrinkage of integrated circuit (IC) dimensions, new dopant profiling techniques are required to meet the spatial resolution for future generation of semiconductor devices [1]. Scanning capacitance microscopy (SCM) has been reviewed as a dopant profile extraction tool with great potential [2], [3]. It is based on the high-frequency (typically 915 MHz) MOS physics [4] between the SCM probe and the underlying semiconductor substrate [5]–[8].

Despite the similarities between SCM instrumentation and a MOS capacitor, there are crucial differences which make the extraction of dopant profile from SCM a challenging task. First, the measured quantity in SCM instrumentation is not the absolute MOS capacitance between the SCM probe and the semiconductor substrate. This is because this capacitance is small compared to the constant stray capacitances due to the small size of the SCM probe tip. To overcome this, SCM instrumentation measures the change in MOS capacitance (more correctly a signal proportional to this) in response to a small change in the dc bias [9], [10], this is referred to as the dC/dV signal. For the purpose of signal detection, the small change in dc bias is achieved by a small ac signal $V_{\rm ac}$ of the order of tens to hundreds of millivolts at 10 to 100 kHz [9]. Second, the SCM setup is not exactly the same as a one-dimensional MOS capacitor. In comparison, the probe used in SCM measurement has the shape of a small cone or pyramid, whereas in a MOS capacitor the conductor is in the form of large metal disk. The influence of trapped charge in the surrounding of the SCM probe, which is negligible in a MOS capacitor, on SCM measurement is yet to be thoroughly studied. Thus due to the limited understanding of the associated physical effects caused by these differences, to date it has not been possible to use SCM to extract quantitative dopant profile for an arbitrary specimen.

In a previous publication, we have proposed the use of the measured accumulation-to-depletion peak dC/dV at every spatial point for dopant profile extraction [11]. This quantity is a direct function of the underlying semiconductor dopant concentration according to MOS physics. Moreover it is easily determined experimentally. However due to the small-size of the SCM probe, the magnitude of the measured peak dC/dV is affected by the contributions from the semiconductor fringing the probe. This second-order effect is a function of the trapped charge in the oxide in the fringing region. In this paper, we present a numerical simulation study of how the presence of interface traps could affect the magnitude of the SCM peak dC/dV. We start with the physics associated with carriers' response in the presence of interface traps, from which we derive a technique to correctly simulate dC/dV to account for the fact that the interface traps respond to the dc bias but not the small $V_{\rm ac}$ signal used in SCM to stimulate the small change in dc bias needed. We also analyze how interface traps would affect the dC/dV of SCM in a way different from a conventional large area MOS capacitor. Then a quantitative evaluation of the SCM peak dC/dV as a function of interface trap energy levels, densities and dopant concentrations is presented. The type of interface traps and their density distribution are often unknown for SCM specimens. From the simulated peak dC/dV data, it is possible to estimate the accuracy of experimentally extracted dopant profile when the effect of interface traps is not accounted for. Finally

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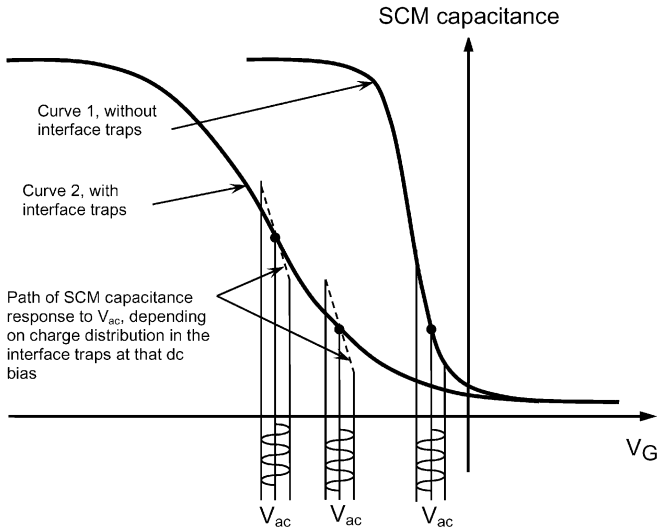

Fig. 1. Theoretical *C–V* curves of samples with uniformly doped p-type substrate. Curve 1 is trap-free and Curve 2 is with interface traps.

based on the findings of our simulation results, the interface trap distribution in a typical SCM sample is justified.

II. A Method to Simulate Interface Trap Response on SCM dC/dV Measurement

To arrive at the method to simulate interface trap response in SCM measurement, we first consider a sufficiently large area SCM probe so that the fringing area can be ignored, i.e., treating it as a large area MOS capacitor. Curve 1 and Curve 2 in Fig. 1 depict the per unit area high-frequency *C–V* curves of p-type MOS capacitors without and with interface traps respectively. The interface traps are assumed to be energy-wise distributed across the bandgap and uniform spatially. As expected, Curve 2 is "stretched" along the bias voltage axis due to the charging of the interface traps. In SCM dC/dV measurement when there are no interface traps, the change in capacitance, ΔC, in response to the change in voltage, ΔV, is simply the slope of the corresponding Curve 1 (with the assumption that the $V_{\rm ac}$ used to sense dC/dV is sufficiently small). When interface traps are present, because interface traps do not respond to the $V_{\rm ac}$, ΔC is the same as that of the sample if it is trap-free and held at the same surface potential [11] and not related to the slope of Curve 2. Theoretically the peak dC/dV, although occurring at different dc bias, would have the same magnitude regardless of the presence of interface traps.

To study the effect of interface trap charge at any dc bias for a nanometer size SCM probe, we propose the following technique to correctly simulate the dC/dV when interface traps do not respond to $V_{\rm ac}$. The spatial charge density distribution in the interface trap changes with dc bias and with distance from the SCM probe. At a given dc bias $V_{\rm dc}$, we first compute the high-frequency capacitance *C* between the probe and the substrate with the interface traps in their equilibrium state at the bias. We also extract this equilibrium spatial charge density distribution present in the interface traps at this dc bias. This extracted charge density distribution remains unchanged when $V_{\rm ac}$ is applied because the traps do not respond to this ac signal. This charge density distribution is then treated as a fixed oxide charge and replacing the interface traps to compute the capacitance $C+\Delta C$ at dc bias $V_{\rm dc}+\Delta V$, where ΔV is the effective change of dc bias introduced by $V_{\rm ac}$ (typically 10 mV). From the ΔC and ΔV, we determine the dC/dV for this $V_{\rm dc}$ from the ΔC and ΔV calculated. This is repeated for whole range of dc bias of interest to arrive at dC/dV as a function of dc bias for a given assumed interface trap energy and density profile. The results also yield the peak dC/dV, a quantity we have proposed for dopant profile extraction. In this way, we have accounted for the spatial variation of interface trap charge density as well as the change with dc bias. Of course for the trap-free case, this technique is literally the same as the numerical differentiation of *C–V* curves.

Silvaco's ATLAS 2-D device simulator was used to carry out the above simulation. The SCM probe tip was modeled as a truncated blade with half angle $=17^\circ$ with probe tip radius (half width of the tip) $=10$ nm. SCM oxide thickness is 8 nm. Most of this study is centred on a uniformly doped p-type silicon substrate with $N_A=1\times10^{17}$ cm^{-3}. Interface trap density and energy distribution in real SCM specimens are unknown; for our work we assumed two discrete energy levels: a donor trap 0.26 eV above E_V and an acceptor trap 0.31 eV below E_C [13]. They are taken to have the same density ranging from 1×10^{10} to 1×10^{12} cm^{-2}.

Fig. 2(a) is the comparison of the SCM *C–V* plots of a trap-free sample (full line) and a sample with trap density $=5\times10^{11}$ cm^{-2} (open circles). The flatband voltage of the sample with interface traps is shifted to a more negative bias due to partial ionization of the donor traps at this condition. By tracking the change in bias voltage needed to change surface band bending under the probe centre for the Fermi level to sweep from the energy position of the donor interface traps (at 0.26 eV above E_V) to that of the acceptor traps (at 0.31 eV below E_C) in the samples, we could see the stretching effect of the interface traps. These are marked as ΔV_A and ΔV_B in Fig. 2(a) for sample with and without interface traps, respectively. As $\Delta V_A > \Delta V_B$, it is clear that stretching does occur.

Fig. 2(b) is dC/dV versus dc bias for the two samples in Fig. 2(a) extracted in the manner described above. With interface traps, the peak dC/dV is significantly higher than the trap-free sample. This differs from the assumption that peak dC/dV should be identical regardless of the presence of interface traps [11]. It is also noted that while stretching of dC/dV versus V curve contributed by the two discrete interface traps is observed, our simulation actually shows a reduction of the full-width at half-maximum (FWHM) of the peak dC/dV-V plot instead of an increase [11]. We attribute these to the lateral electric field from the charge of the interface traps surrounding the SCM probe creating nonuniform 2-D depletion region surrounding the probe leading to contributions to dC/dV that are very different from the trap-free sample. For example, due to the small size of the probe, the potential profile in the direction perpendicular to the oxide-silicon interface under the probe is affected by the lateral electric field of interface trapped charge surrounding the probe. This results in different *C–V* and also dC/dV-V characteristics to those of a large area MOS capacitor. These deviations will affect the accuracy of the dopant profile

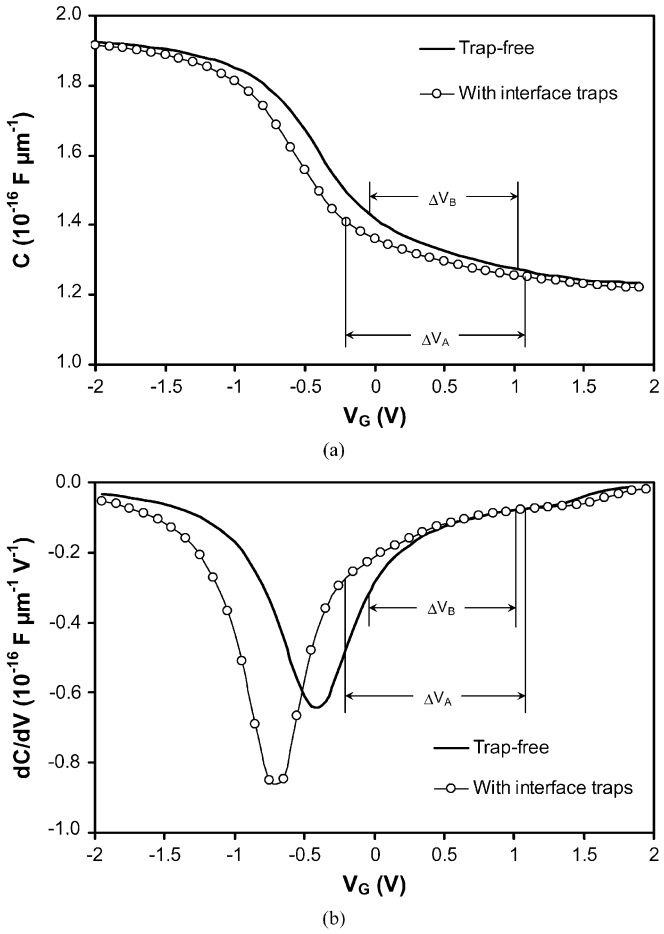

Fig. 2. (a) Simulated *C–V* curves of SCM samples uniformly doped with $N_A = 1 \times 10^{17}$ cm^{-3} to compare the effects of interface traps. (b) Simulated dC/dV-V curves of SCM samples used in Fig. 2(a).

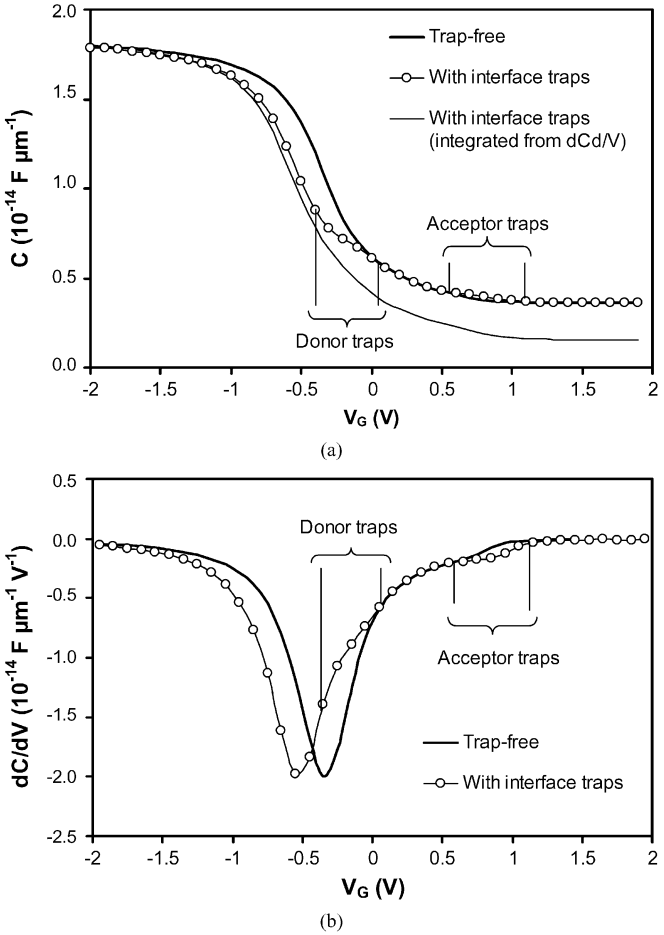

Fig. 3. (a) Simulated *C–V* curves of SCM samples uniformly doped with $N_A = 1 \times 10^{17}$ cm^{-3} using very large probe radius (2 μm). (b) Simulated dC/dV-V curves of SCM samples used in Fig. 3(a).

extraction. We will investigate this aspect of SCM dopant profile extraction subsequently.

To verify our explanation, we repeated the simulation with a larger tip radius of 2 μm so that the fringing field become negligible. All simulation parameters except the probe tip radius are the same as those used in Fig. 2. The simulation results are shown in Fig. 3(a) and (b). The *C–V* curve with interface traps clearly shows stretching due to donor traps and acceptor traps. The larger SCM probe produces a *C–V* plot approaching that of a standard MOS capacitor. Fig. 3(b) shows that the peak dC/dV's are identical regardless of the absence or presence of interface traps in contrast to Fig. 2(b) which shows a significantly higher peak dC/dV in the presence of interface traps when the SCM probe is small. A broader FWHM of the dC/dV-V plot as expected from stretching of the *C–V* curve in the presence of interface traps is also observed in Fig. 3(b). This simulation indicates that use of large size (radius of the order of micrometers) SCM probe has the effect of removing the influence of interface traps. This of course comes with the sacrifice of the nanometer spatial resolution that is the inherent of SCM measurement.

SCM measurement yields only dC/dV-V data not the *C–V* data. Simulation such as Fig. 3 (and also Fig. 2) allows us to explore the relationship between experimental dC/dV-V and the expected *C–V*. In the absence of interface traps, integration of dC/dV-V plot leads to the expected *C–V* curve. In the presence of interface traps which do not respond to the small signal $V_{\rm ac}$ used in dC/dV measurement, it is difficult to interpret the integrated plot. To demonstrate this, we integrate the dC/dV-V for the sample with interface traps in Fig. 3(b). This is shown as the thin line in Fig. 3(a) with an integration constant that matches the accumulation capacitance at -2 V with the computed *C–V* plot. This integration shows deep-depletion-like characteristics for experimental data as reported in [12] despite of the fact that the *C–V* simulation assumes dc equilibrium. If the same integration process is applied to Fig. 2, we will see even deeper depletion capacitance due to the larger peak dC/dV.

III. Effects of Surrounding Interface Trapped Charge on SCM Measurement

From Fig. 2 and Fig. 3 we have seen that peak dC/dV in the presence of interface traps is significantly different from that for a trap-free specimen and we attributed this to the lateral electric field due to the charge in the interface traps surrounding the SCM probe. We now investigate this effect via simulation. Consider a p-type substrate with the SCM probe biased such that the surface of the substrate at the middle of the probe is at flatband, where the peak dC/dV would normally occur without interface

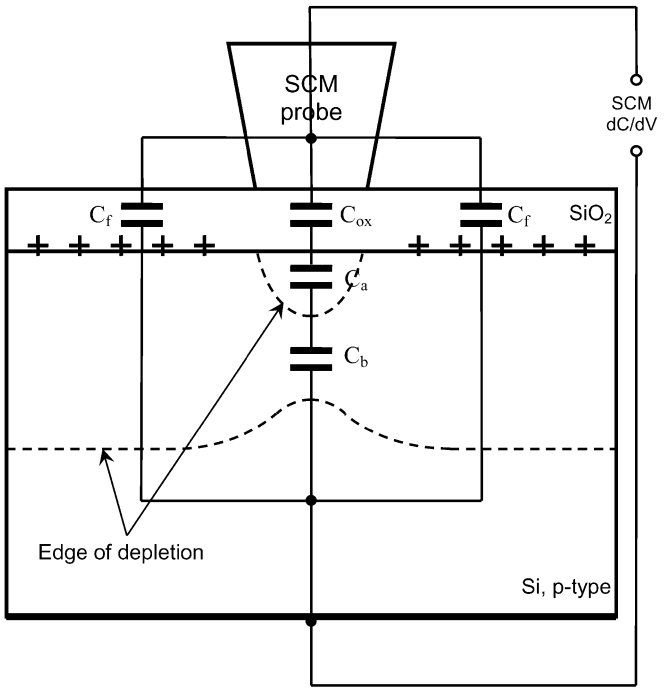

Fig. 4. Positive trapped charge surrounding the probe creates a layer of depletion laterally into the region underneath the SCM probe. Under this condition, the SCM capacitance consists of $C_{\rm ox}, C_a, C_b$, and C_f.

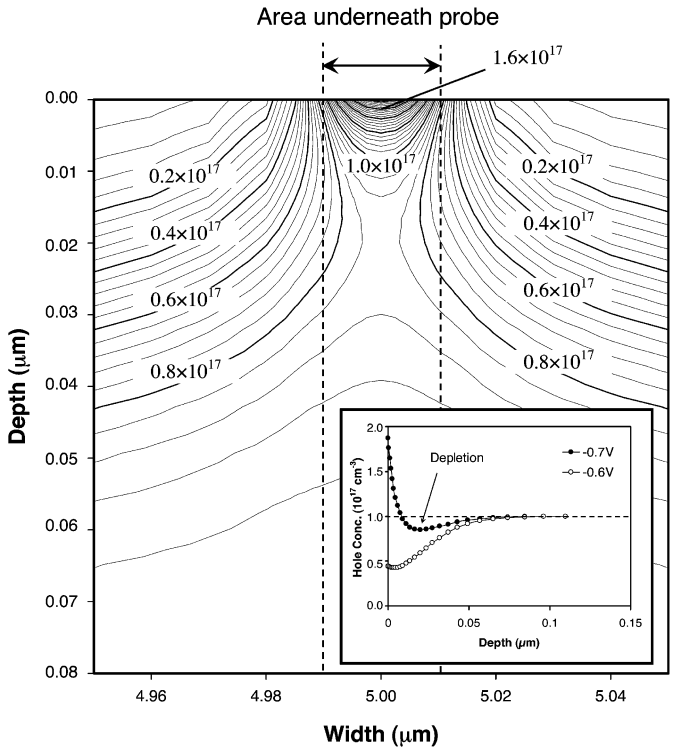

Fig. 5. Contour plot of majority carrier concentration with surface pinned at close to flatband for a p-type substrate uniformly doped with $N_A = 1 \times 10^{17}$ cm^{-3}. Semiconductor surface is at depth$= 0\ \mu$m. Probe tip is centred at width$= 5.00\ \mu$m.

traps. In the presence of interface traps (assuming the two discrete levels used in our earlier simulation), a positive trapped charge (arising from the ionised donor traps) is present in the substrate surface surrounding the probe due to the charge balance between the substrate and the interface traps [14]. This leads to a depletion of majority carriers perpendicular to the semiconductor surface as well as laterally into the substrate underneath the probe. The capacitance contributions from the substrate under the probe can be considered as three capacitances in series: $C_{\rm ox}, C_a$, and C_b, where $C_{\rm ox}$ is the oxide capacitance (fixed, does not contribute to dC/dV), C_a is the contribution of the thin layer of material at or near flatband at the surface and C_b is the contribution from the underlying layer depleted of majority carriers. This is shown in Fig. 4. The degree of depletion is a function of the trapped charge and the substrate dopant concentration. Negative change in dc bias on the probe will accumulate the surface and also reduces the degree of depletion of this underlying region, leading to increase in both C_a and C_b. Conversely, positive change in dc bias depletes the surface and stronger depletion in underlying region giving rise to lower capacitance seen by the probe. The change of the underlying depletion is very sensitive to the change in the probe dc bias around flatband, and thus gives rise to higher peak dC/dV. The fringing regions also contribute to the measured capacitance shown as C_f in Fig. 4. Indeed this fringe capacitance can be a significant fraction of the measured probe capacitance. However due to the weak electric field, substrate surface potential of these regions do not change in response to the probe dc bias (or the small-signal $V_{\rm ac}$), irrespective of the presence or absence of interface traps, there is therefore only a very small contribution to the dC/dV measured.

This majority carrier depletion effect is illustrated by the majority carrier contour plot shown in Fig. 5 which is the structure with interface traps in Fig. 2 biased at $V_{\rm G} = -0.7$ V. The Si-SiO_2 interface is at $\rm depth = 0\ \mu m$ and the SCM probe is centred at $\rm width = 5.00\ \mu m$. The majority carrier profiles at $V_{\rm G} = -0.7$ and -0.6 V as a function of depth are shown in the inset. The difference in majority carrier concentration is related to the measured dC/dV.

The influence of the depletion induced underneath the probe by the surrounding interface trapped charge is significant only when depth of the depleted region (and hence also the lateral extension beneath the probe) is comparable to or larger than the probe tip radius. In Fig. 6, we plot the depletion depth due to the interface trapped charge for an interface trap density of 5×10^{11} cm^{-2} for the discrete interface traps used in Fig. 2. The depletion depth is arbitrarily defined as the distance from the surface at which hole concentration$= 0.8N_{A,}$ where N_A is the dopant concentration. The magnitude of this depletion depth for N_A below 1×10^{17} cm^{-3} is significantly larger than a typical SCM probe tip radius ($\sim$10 nm), which indicates that for this interface trap density, peak dC/dV can be expected to be different from the ideal trap-free case. In the next section, we estimate the deviation of the peak dC/dV as a function of dopant concentration and various interface trap parameters. It is of interest to note that while the trapped charge density for the same trap density actually increases with increasing $N_{\rm A}$, as shown in Fig. 6, the effect of the trapped charge to deplete the substrate reduces as N_A increases as expected from device physics.

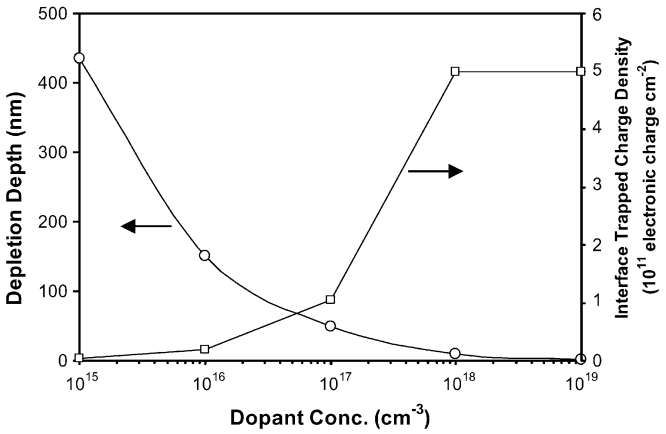

Fig. 6. Depletion depth caused by interface trapped charge and trapped charge density versus dopant concentration.

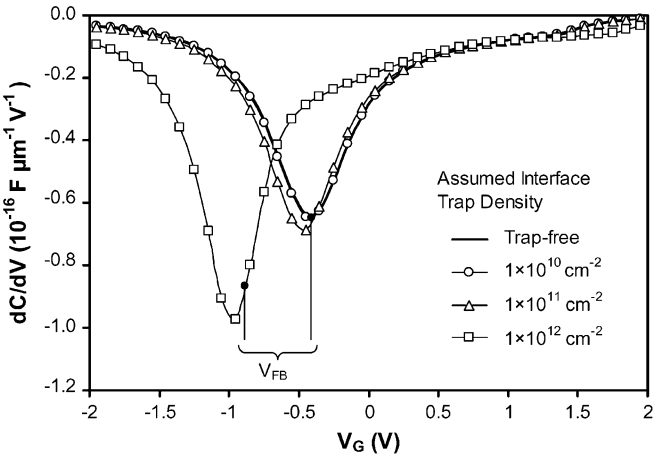

Fig. 7. Comparison of simulated dC/dV of different interface trap densities for a p-type substrate uniformly doped with $N_A = 1 \times 10^{17}$ cm^{-3}.

IV. Dependence of SCM Peak dC/dV on Substrate Dopant Concentrations, Interface Trap Densities and Energy Levels

The interface traps are always present in specimens prepared for SCM measurement. However trap density and energy distribution are unknown quantities. In order to understand the accuracy of extracted dopant profile from SCM measurement, we need to have a quantitative understanding of the effects of interface trap density, trap energy on the peak dC/dV. Each parameter is studied separately with the other parameter held constant. As their effects are also dependent on the actual dopant concentration, we have carried out simulation for p-type substrate with dopant concentration ranging from 1×10^{15} to 1×10^{19} cm^{-3}. The effects on n-type substrates can be deduced from the results for the p-type substrates bearing in mind that positive and negative interface trapped charge have just the opposite effects on p- and n-type substrates and energy position effects are also opposite for the two substrate types.

For trap density study, one discrete donor trap at 0.26 eV above E_V and one discrete acceptor trap at 0.31 eV below E_C with equal density are used. The dC/dV versus V plots are shown in Fig. 7 for three interface trap densities of $1 \times 10^{10}, 1 \times 10^{11}$ and 1×10^{12} cm^{-2} and a substrate concentration of 1×10^{17} cm^{-3}. It is clear that trap density at 1×10^{10} cm^{-2} does not show any significant deviation from the interface trap-free case on the dC/dV data. But with increasing interface trap density, deviation from the trap-free case increases. For the trap density at 1×10^{12} cm^{-2} in particular, the peak dC/dV has increased by 40% and its position along the bias voltage axis has shifted -0.6V. The location of the peak has also shifted slightly (~ -0.1V) from the flatband condition. It is obvious that increasing trap density leads to higher trapped charge at the fringing area and hence greater effect on the SCM capacitance and dC/dV. For a given interface trap density, the effect of trapped charge increases with decreasing dopant concentration. We will be tracking peak dC/dV with dopant concentration in a subsequent plot.

For the study of the trap energy level, we have kept the trap density fixed at 5×10^{11} cm^{-2} and used three donor trap energy: 0.13, 0.26, and 0.39 eV above E_V, while the acceptor

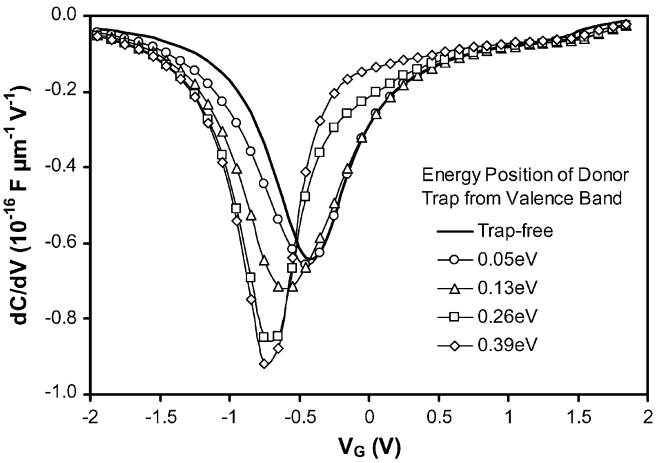

Fig. 8. Comparison of simulated dC/dV of different interface trap energy levels for a p-type substrate uniformly doped with $N_A = 1 \times 10^{17}$ cm^{-3}.

trap remains constant at 0.31 eV below E_C for the p-type substrate. For p-type substrate, acceptor level above mid-gap typically does not have much effect on the SCM data around the dC/dV peak position as they are empty and electrically neutral at this bias condition. Fig. 8 is the dC/dV-V plot for the $N_A = 1 \times 10^{17}$ cm^{-3} substrate. It is seen that traps close to E_V has smaller effect. This is due to the fact that traps close to E_V have higher occupancy probability at any given gate bias and, being donor traps, are electrically neutral and hence exert no effect on the field distribution. A similar deduction can be made regarding acceptor traps on the top half of the band gap. Consequently it can be concluded that when the traps are near the band edges, the peak dC/dV is not affected much even if the trap densities are high. Under this condition, the peak dC/dV can be used for dopant concentration extraction with reasonable accuracy provided that the trap density is low in the mid-gap region.

We present an estimation of the level of interface trap density that can be tolerated for accurate extraction for dopant concentration from SCM peak dC/dV measurement. For a conservative estimation, again the two discrete trap model from [13] (the donor trap is 0.26 eV above E_V and the acceptor trap is 0.31 eV below E_C) is assumed. This will represent a worse scenario

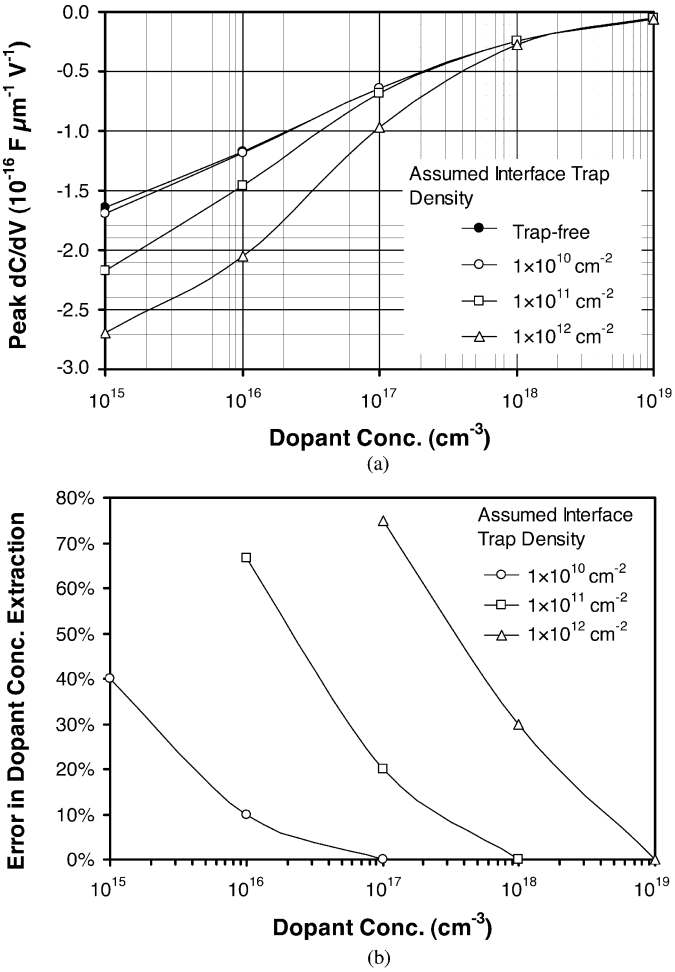

Fig. 9. (a) Simulated peak dC/dV versus dopant concentrations for different interface trap densities. (b) Percentage error in peak dC/dV versus dopant concentration for different interface trap densities.

compared to when the traps are located near the band edges as it results in greater change in the peak dC/dV. Fig. 9(a) is the plot of simulated peak dC/dV versus dopant concentration for three interface trap densities. The graph indicates that as interface trap densities increase, the peak dC/dV exhibits increasing deviation from the trap-free case. This deviation also increases with decreasing dopant concentration. For consistency of measurement, it is obvious that the interface trap density has to be kept to a minimum ($<1 \times 10^{10}$ cm^{-2} of the discrete donor and acceptor traps or $\sim 2 \times 10^{10}$ eV^{-1} cm^{-2} distributed traps across the bandgap) particularly for lightly doped specimens. Unfortunately the surface quality of the SCM specimens and the nature of low temperature oxide used in SCM measurement are not likely to produce oxide–silicon interface with such low interface trap density.

Typically, SCM dopant profile extraction uses some form of calibration chart technique to convert the measured SCM data to dopant concentration [15]. In our earlier proposal of using peak dC/dV as the extraction data, this would be the trap-free peak dC/dV versus dopant concentration plot in Fig. 9(a). Applying such a trap-free calibration plot to extract dopant profile from data measured on specimens with interface traps will lead to

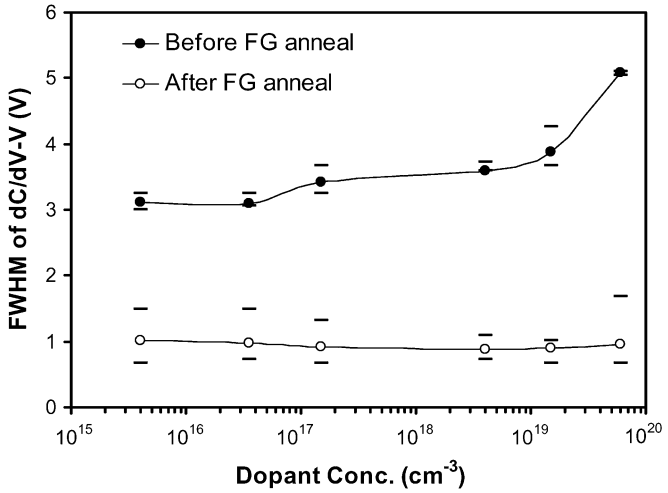

Fig. 10. Experimental FWHM of dC/dV-V curves versus dopant concentration.

error in the extracted dopant concentration. Fig. 9(b) is an estimation of the percentage error in extracted dopant concentration based on the computed peak dC/dV quantity in Fig. 9(a). It can be seen that only if the trap density is below 1×10^{10} cm^{-2} can we be assured that the extracted dopant concentration is meaningful for dopant concentration down to 1×10^{16} cm^{-3}.

V. Experimental Investigation of Interface Trap Effects

It is well known that the interface trap density can be reduced by annealing in hydrogen gas. In this section, experimental data before and after anneal are compared to investigate the effect of interface traps. The measurement was performed with a Digital Instruments Dimension 3000 SCM. The dC/dV data were obtained using 0.2 V ac signal at 90 kHz for dc bias between -6 V and 6 V. The sample was a p-type silicon substrate doped with multiple concentrations between 1×10^{15} and 1×10^{20} cm^{-3}.[1] A 3-nm-thick oxide was grown by wet oxidation at 600°C for 2 h. To reduce the interface trap density, forming gas (FG) consisting of 90% N_2 and 10% H_2, anneal was applied at 450°C for 35 minutes. SCM measurement was carried out before and after the FG annealing. Ten measurements were taken at each dopant concentration to obtain an averaged value of peak dC/dV and FWHM.

The FWHM of the dC/dV-V curves is plotted in Fig. 10. The narrower FWHM of the dC/dV-V after hydrogen anneal, corresponding to the removal of *C–V* curve stretching, indicates that the interface trap density has been reduced. Fig. 11 compares the experimental peak dC/dV before and after hydrogen anneal. The peak dC/dV in the two sets of data show no significant difference across the entire dopant concentration range.

The observation from Fig. 10 and Fig. 11 resembles the simulation result of the donor trap energy level positioned low in the bandgap in Fig. 8. In this scenario, the donor trap is primarily electrically neutral and does not create depletion in the fringing area. Consequently, the peak dC/dV is not affected. However, it will still broaden the FWHM of dC/dV-V in the accumulation

[1]The multiple dopant step wafer piece was purchased from IMEC.

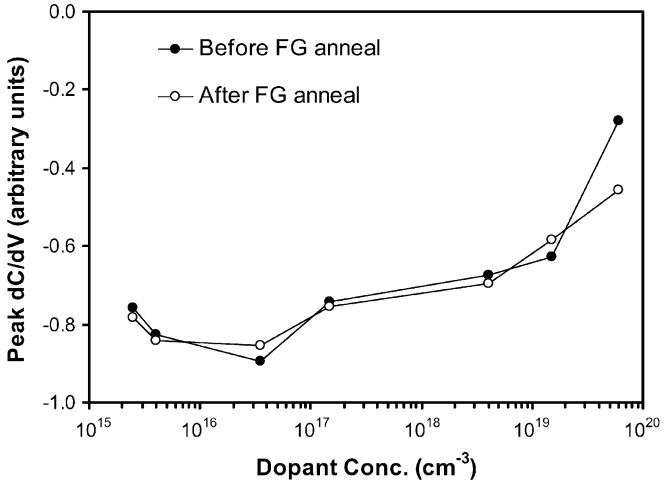

Fig. 11. Experimental peak dC/dV (in arbitrary units of SCM instrumentation) versus dopant concentration.

region by bending the energy bands such that E_F is close to the donor trap. Thus it is believed that this experiment supports the commonly held opinion that the trap density has a U-shape energy distribution - high densities at the band edges and relatively low near the midgap [16]. These experimental results also support the deduction from our simulation that peak dC/dV for dopant extraction can be used for dopant concentration extraction if the interface trap density is low in the mid-gap region.

VI. Conclusion

In this paper, we have described a new technique to simulate SCM measurement in the presence of interface traps to estimate the influence of these traps on the accuracy of dopant concentration extraction from peak SCM dC/dV data. It takes into account the physics of the interface traps' response to the ac signal used in SCM to measure dC/dV. Due to the small dimension of the SCM probe, interface trap charge fringing the probe creates a depletion region under the probe. This effect is more pronounced in low substrate dopant concentrations, and also depends on the interface trap density and energy distribution. From our simulation results, we have estimated the error in dopant concentration extraction if interface traps are not taken into account in treating experimental SCM data. To avoid such discrepancy in the dopant profile extraction it is necessary to keep the interface trap density low during SCM specimen preparation. The error can also be reduced by using a larger SCM probe. However, this will compromise the high spatial resolution provided by scanning probe microscopy.

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