Dopant Profile Extraction by Inverse Modeling of Scanning Capacitance Microscopy Using Peak dC/dV

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Abstract

Scanning capacitance microscopy (SCM) has proven to be successful for junction delineation. However quantitative dopant profile extraction by SCM still remains a difficult challenge, due to limited understanding of relevant physics especially at p-n junction, as well as difficulties to accurately quantify all parameters in modeling.
In this paper we present a new procedure, the use of peak dC/dV at every spatial point, for dopant profile extraction. The advantage of such a technique is twofold. First it eliminates problems encountered using a fixed dc bias such as contrast reversal. Second, it also excludes the need to model interface traps. This is because the peak dC/dV value is independent of the presence of interface traps, as demonstrated in our experimental results.
Furthermore, based on our understanding of the influence of mobility degradation at p-n junction, we propose that low surface mobility model should be used in simulation so that only the accumulation-to-depletion dC/dV is extracted.

1. Introduction

Scanning capacitance microscopy (SCM) is regarded as a 2-D dopant concentration profiling technique with great potential [1, 2] It utilizes the excellent spatial resolution of scanning probe microscopy [2, 3], and is essentially based on the MOS characteristics between the scanning probe and the underlying substrate.
Although SCM has been able to produce contrast images for p-n junction delineation, dopant profile extraction across a p-n junction from SCM data is still a very challenging task [4, 5, 6, 7]. Due to the fact that many physical effects influencing the experimental SCM data are not well understood and hence not accounted for in the associated forward modeling, the use of the inverse modeling technique based on MOS capacitor physics to extract the dopant profile [8, 9] has not been successful to date.

In this paper, we first review the current practice of dopant profile extraction by SCM, which is done at a fixed dc bias, and analyze the associated problems such as contrast reversal. We then compare experimental SCM data to highlight the effect of interface traps. The results of our investigation are used to justify a new approach to dopant profile extraction from SCM measurement: the use of the interface trap-independent peak dC/dV at accumulation-to-depletion transition for each spatial point.

2. Review of current dopant profile extraction method by SCM

The operation of SCM is based on the MOS capacitor theory. A dc bias, V_G, is applied between the probe tip and substrate to sweep the semiconductor surface from accumulation to inversion. An ac signal, V_{ac}, is also applied to cause variations in the capacitance between the probe tip and the sample. These variations are measured by the capacitance sensor and are directly related to the dopant concentration.
Currently the most common technique to convert SCM signal to dopant concentration is the calibration curve method [10, 11]. A database of C-V curves are calculated from simulation for a range of modeling parameters such as oxide thickness, probe tip size and dopant concentrations etc. To extract dopant profile, the experimental SCM signal is compared to a series of simulated C-V curves determined by the same modeling parameters as the actual SCM setup. To account for the different units used in measurement and simulation, the simulated dC/dV is normalized against the SCM signal obtained from a region of the sample where the dopant concentration is known.
Most SCM images are obtained at a single dc bias for convenience. While the SCM has proven to be able to produce contrast images of different dopant concentration and types (for instance, the drain and source regions of a MOSFET), the contrast of the images and the region definitions are highly dependent on the dc bias chosen. It has also been found that at a fixed dc bias,

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the SCM output is not always a monotonically increasing signal with decreasing dopant concentration [12]. With current SCM practice of measuring dC/dV at a fixed dc bias for dopant concentration extraction, the actual surface potential, and hence also the measured dC/dV, is dependent on the interface trap density and distribution as well as the semiconductor work-function difference. This leads to what is referred to as contrast reversal in SCM measurement [12, 13].

We illustrate this by comparing the two sets of experimental dC/dV data in Figure 1. They were measured from different regions of the same n-type sample under the same conditions. It can be deduced that the open circle curve represents higher dopent concentration compared to the filled circle curve as the magnitude of its peak dC/dV is smaller. However if the SCM fixed dc bias is chosen at -2 V, the relative magnitude of the two measured dC/dV at this bias would indicate that the open circle sample has a lower dopant concentration compared to the filled circle sample (which is incorrect), whereas if the dc bias is chosen at 0 V, the dC/dV data would lead to a conclusion that is the exact opposite. At 2 V, it is even difficult to differentiate the two dopant concentrations due to the similarity in their dC/dV magnitude. Use of peak dC/dV, which is unique for each dopant concentration, will eliminate this problem. The two curves in Figure 1 have different peak dC/dV and hence their dopant concentration can be determined accordingly. In the next section we will also show that the peak dC/dV also is independent of the presence of interface traps.

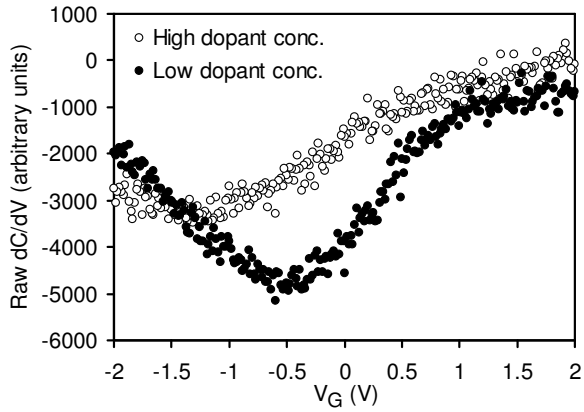

Figure 1. Comparison of dC/dV of two dopent concentraions

3. Effects of interface traps on SCM measurement

In SCM measurement, dC/dV, or more precisely $\Delta C/V_{ac}$, is measured by detecting the change in the capacitance ΔC, in response to V_{ac} (~10 to 100 mV, 10 kHz), superimposed on the dc bias. We believe that the interface traps do not respond to the ac signal at this frequency. The consequence is that the measured dC/dV would be the same for a trap-free sample biased at the same surface potential.

In Figure 2 (a) we elaborate on this point. Consider the theoretical high frequency C-V curves for two p-substrate SCM samples with the same substrate dopant and oxide thickness. Curve 1 is for an interface trap-free sample and Curve 2 is for a sample with interface traps. Curve 2 is stretched along the dc bias axis due to the change in charge trapped in interface traps as the dc bias is varied. From high frequency C-V theory, Point A on Curve 1 and Point B on Curve 2 which have the same MOS capacitance correspond to the same surface potential, despite the difference in dc bias. When the SCM 10 kHz dC/dV sensing signal, V_{ac}, is applied to the two samples at Point A and B respectively, the interface traps in Curve 2 also do not respond to this signal. Consequently the signal induces the same change in surface potential in the sample with interface traps and hence the same change in capacitance, ΔC_A, as the trap-free sample by following the dotted line passing through Point B and parallel to Curve 1 (instead of following Curve 2 which leads to ΔC_B). The detected dC/dV is therefore $\Delta C_A/V_{ac}$ for both samples at their respective dc bias points. In other words, the values of dC/dV detected in SCM measurement at a given surface potential are the same for the two samples and equal to that of a trap-free case. Hence it is not necessary to account for the interface traps in the simulation for the purpose of comparing the magnitude of dC/dV between experimental and simulation data at any specific surface potential.

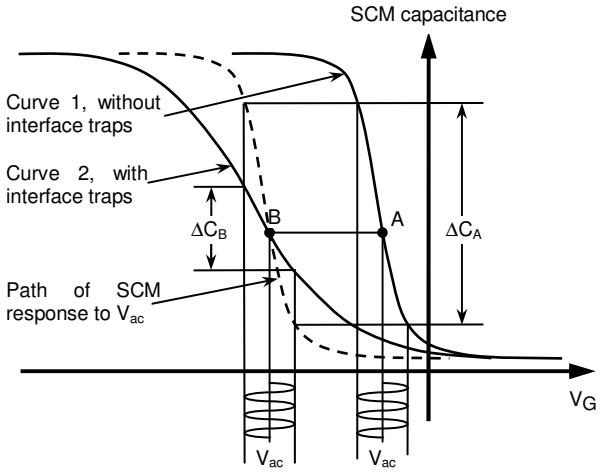

Figure 2 (a). Effects of interface traps on the plots of SCM C-V a p-substrate sample: Curve 1 with no interface traps and Curve 2 with interface traps.

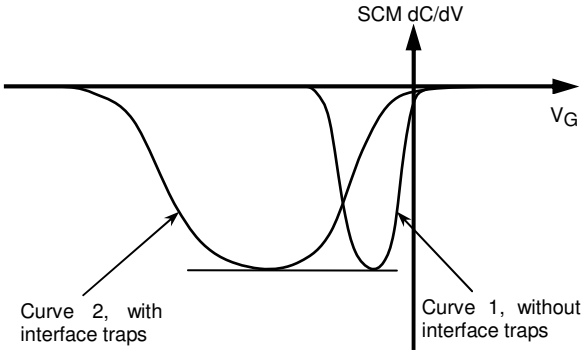

Figure 2 (b). Expected SCM dC/dV versus dc bias plots for Curve 1 and 2 in Figure 2 (a) when interface traps are not responding to the SCM V_{ac} signal

In Figure 2 (b) we depict the dC/dV versus dc bias of the two C-V curves from Figure 2 (a) by a applying the above consideration to other points. It can be seen that although the two curves show identical peak dC/dV values, interface traps will stretch the SCM dC/dV versus dc bias plot for the sample with interface traps.

To verify the effect of interface traps, an SCM measurement has been carried out on two wafers for comparison. Both samples have polished surface of IC-grade and are uniformly doped with $N_A = 2\times10^{15}$ cm^{-3}. One sample has production-grade MOSFET nitrided gate oxide known to be effectively interface trap free; the other has a typical SCM thermal oxide which has high interface traps density. The two samples also have very similar oxide thickness: 3.012 nm for the nitrided oxide, and 3.22 nm for the SCM thermal oxide.

The raw dC/dV versus dc bias plots for these samples are plotted in Figure 3: filled circles represents sample with industrial-grade nitrided gate oxide, and open circles represents sample with SCM thermal oxide. The larger width of the SCM thermal oxide curve compared to the industrial-grade nitrided gate oxide curve indicates the presence of interface traps in the SCM thermal oxide as explained before.

From analysis on theoretical C-V curves of uniformly doped substrate, there is a peak dC/dV (maximum slope of C-V curve) at accumulation-to-depletion transition, i.e. flatband or zero surface potential. This peak value is also different and unique for each dopant concentration. In Figure 3 it shows that the two samples with the same dopant concentration have almost identical peak dC/dV, which verifies our earlier statement that in SCM measurement dC/dV at a given surface potential is not affected by the presence of interface traps. We can therefore use the measured SCM peak dC/dV as a unique parameter for SCM dopant concentration extraction. The use of this parameter for dopant concentration extraction is investigated in the next section.

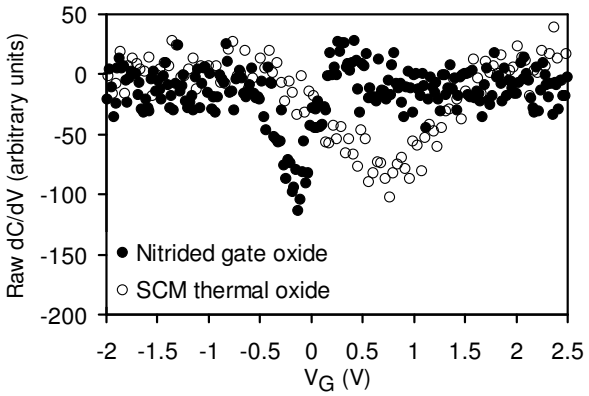

Figure 3. Experimental dC/dV versus dc bias plots of SCM samples on uniformly doped p-type silicon with IC grade polished surface: open circles – sample with SCM thermal oxide; filled circles – sample with industrial-grade nitrided gate oxide

4. Proposal for junction dopant profile extraction

Based on our finding that the peak dC/dV is not affected by the presence of interface traps, and the dc dependence of SCM signal, we believe that the peak dC/dV is a better reference when comparing simulation and experimental results for inverse modeling. Together with our previous analysis that at the p-n junction the inversion capacitance is not seen due to surface mobility degradation [14], we now propose the use of the accumulation-to-depletion peak dC/dV at every spatial point, for dopant profile extraction. In simulation low surface mobility should be used so that only the accumulation-to-depletion dC/dV is extracted [14].

To demonstrate the use of peak dC/dV, we performed SCM measurement on a semiconductor sample with p^+-n junction. The measurement was done with a DI 3000 Nanoscope operating in SCM bias ramping mode to capture dC/dV as a function of dc bias at spatial intervals of approximately 0.1 μm across a 1-D silicon p^+-n junction formed by boron implantation into a n-type substrate uniformly doped at 3×10^{17}cm^{-3}. The SCM oxide is 8 nm thick obtained by low temperature oxidation in ozone. The dc bias is scanned to sweep the surface from accumulation to inversion.

Following our proposal, in Figure 4 we plotted the positive and negative peak dC/dV as a function of spatial position, x. The dC/dV has been normalized against the peak dC/dV at the n-type substrate. In the n and p^+ regions, dC/dV shows positive and negative peaks respectively at the accumulation-to-depletion transition of the surface as expected from MOS C-V theory. Within the space charge region (approximately 1.8 μm < x < 2.2 μm), dC/dV shows both negative and positive peaks

similar to what is observed in a low-frequency MOS C-V curve but measured at 915 MHz, indicating both are accumulation-to-depletion transitions. This arises from the fact that holes and electrons are supplied as majority carriers from the p-side at negative dc bias and from the n-side at a positive dc bias respectively.

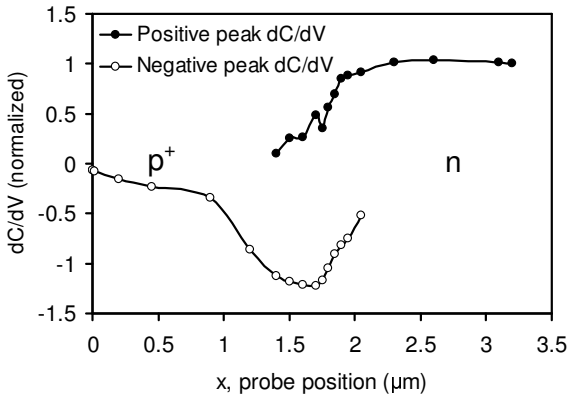

Figure 4. Normalized peak dC/dV across p-n junction

In Figure 5 we also plotted the graph of dC/dV versus spatial position measured at various dc biases for the same p^+-n sample. It is clear that the SCM signal is strongly dependent on the dc bias chosen. Factors such as work function differences, fixed oxide change and interface states would also contribute to the shift of C-V curves along voltage axis, making the comparison between experimental results and simulated theoretical C-V curves using a single dc bias extremely difficult. The use of peak dC/dV can minimize those influences and this method is currently being investigated.

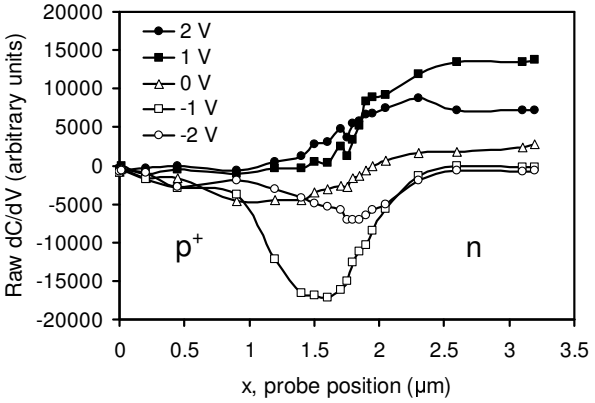

Figure 5. dC/dV data at various dc biases

5. Conclusion

We reviewed the current practice of dopant profile extraction method using SCM and analyzed the problems. We also presented a comparison of experimental SCM measurement to study the effects of oxide-silicon interface traps. Based on theoretical consideration and experiment we have shown that the presence of interface traps does not affect the peak value of the measured dC/dV data at the accumulation-to-depletion transition of the semiconductor surface. We propose that at each spatial position, a single experimental data corresponding to the accumulation-to-depletion transition peak dC/dV be used as the target parameter to be matched by simulation. This avoids the data ambiguity caused by using a fixed dc bias, and also minimizes the effect of interface traps.

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