Modeling the Effects of Interface Traps on Scanning Capacitance Microscopy dC/dV Measurement

Y. D. Hong* and Y. T. Yeow
School of Information Technology and Electrical Engineering
The University of Queensland, Brisbane, QLD, Australia
*Email: hong@itee.uq.edu.au

***Abstract*—Scanning capacitance microscopy (SCM) measurement is a proposed tool for dopant profile extraction for semiconductor material. The influence of interface traps on SCM dC/dV data is still unclear. In this paper we report on the simulation work used to study the nature of SCM dC/dV data in the presence of interface traps. A technique to correctly simulate dC/dV of SCM measurement is then presented based on our justification. We also analyze how charge of interface traps surrounding SCM probe would affect SCM dC/dV due the small SCM probe dimension.**

Keywords-component; SCM; scanning capacitance microscpy; interface traps; modeling

I. INTRODUCTION

Scanning capacitance microscopy (SCM) measurement is a proposed tool for dopant profile extraction for semiconductor material to capitalise on the excellent spatial resolution of the scanning probe microscopy [1-3]. It is based on the high-frequency (typically 915 MHz) MOS physics [4] between the SCM probe and the underlying semiconductor substrate which shows that the capacitance measured is a function of the substrate dopant concentration [5-8]. However due to the small size of the SCM probe tip, the MOS capacitance is small compared to the constant stray capacitances. To overcome this point, in SCM instrumentation the quantity being measured is the change in MOS capacitance in response to a small change in the dc bias [9, 10], this is referred to as the dC/dV signal. For the purpose of signal detection, the small change in dc bias is achieved by a small ac signal V_{ac} of the order of tens' of millivolts at 10 to 100 kHz [9].

For a perfect MOS surface where there are no interface traps, the understanding and analysis of SCM measurement follows directly the theory and simulation of high-frequency MOS structure formed by the SCM probe and substrate, the SCM dC/dV signal will simply be the slope of the high-frequency C-V curve. However in the presence of interface traps which do not respond to the V_{ac} signal [10, 11], it is necessary to understand this effect on the SCM dC/dV signal. Also the effect of interface traps on the SCM measurement will not necessarily be the same as on a MOS capacitor, as the SCM probe has extremely small dimension and the charge from interface traps surrounding the probe is likely to have significant impact on SCM capacitance.

In this paper we report on the simulation work used to study the nature of SCM dC/dV data in the presence of interface traps. In the first part we describe a technique to correctly simulate dC/dV in the case of interface traps not responding to V_{ac}. In the second part we analyse how interface traps would affect the dC/dV of SCM differently due to the small dimension of SCM probe compared to a conventional MOS capacitor. This understanding is relevant to the interpretation of experimental dC/dV data for dopant profile extraction.

II. EFFECTS OF INTERFACE TRAPS ON SCM dC/dV AND PROPOSED SIMULATION TECHNIQUE

In this section we first describe the physics of interface traps and how it would influence SCM dC/dV. Based on our justifications we then propose a technique to correctly simulate this.

It is known that interface traps stretch the C-V curve of a MOS capacitor. To illustrate this, in Fig. 1 we plotted two theoretical C-V curves (capacitance vs. dc bias, V_G) of MOS capacitor: Curve 1 and Curve 2 are with and without interface traps respectively for a p-type uniformly doped substrate and interface traps (acceptor traps above E_i and donor traps below E_i) are assumed to be energy-wise distributed across the bandgap and uniform spatially. As is well known we see the "stretching" of Curve 2.

The physics is more complex when dC/dV, which is the quantity measured in SCM instead of absolute capacitance, is involved. Without interface traps, the change in capacitance ΔC when V_{ac} is applied will just follow the Curve 1. Typically V_{ac} is sufficiently small (of the order of 10 of millivolts), and the ΔC versus dc bias plot is just the slope of the C-V curve at each dc bias point. However when interface traps are present, ΔC follows a different path which is not the slope of Curve 2. It is determined by the band bending at the dc bias and the charge in the interface trap distribution at that band bending. The consequence is that the measured dC/dV will depend on the interface trap distribution as well as the substrate dopant concentration.

Following the justification above, here we describe a technique to correctly simulate the dC/dV in the case of interface traps not responding to V_{ac}. At a given dc bias, we first simulate the capacitance C in the presence of the assumed interface traps. We also extract the spatial charge density distribution present in these interface traps at this dc bias. Thus this charge density distribution will vary with dc bias as the dc

bias determines the occupancy of the interface traps. This extracted charge density distribution remains unchanged when V_{ac} is applied because the traps do not respond to this ac signal. This charge density distribution is then treated as a fixed oxide charge and input to the simulation program and the capacitance (i.e. a capacitance calculation with fixed oxide charge rather than interface traps) is simulated at the original dc bias plus a dV i.e. V + dV to obtain the new capacitance (= C + dC). From the results we can get dC/dV and this is repeated for all dc bias. This technique will be used in the subsequent simulation for SCM dC/dV in the presence of interface traps.

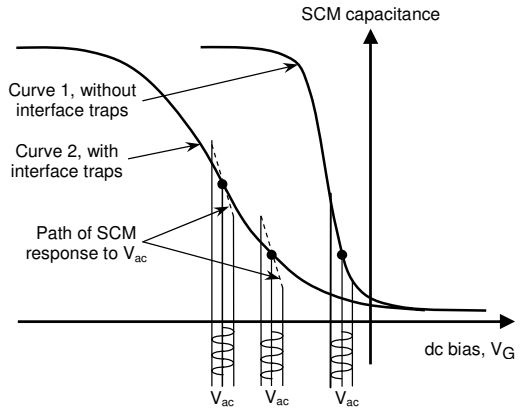

Figure 1. Theoretical C-V curves of MOS capacitors with uniformly doped p-type substrate.

III. Effects of Fringe Interface Trap Charge on SCM Measurement

We also investigate how interface traps would affect capacitance measurement differently in SCM due to the extremely small probe dimension compared to the conductive sheet of conventional MOS capacitor. In the interface trap-free case, the C-V characteristic of a SCM will be very similar to a MOS capacitor. However, with the presence of interface traps, the charge of interface traps surrounding the SCM probe could have significant influence on the carrier distribution directly below the SCM probe, hence alters SCM capacitance. This effect is similar to the short channel effect seen in MOSFET.

We explain this using Fig. 2 which depicts an SCM probe sitting on a p-type semiconductor test sample with two discrete interface trap levels: one donor trap below E_i and one acceptor trap above E_i.

First consider the spatial locations far away from the SCM probe (unshaded area) where the electric field from the SCM probe has minimal influence, the existence of interface traps alters the surface potential spontaneously until a state of equilibrium is reached by balancing out positive charge of donor traps and negative charge of ionized. The net result is that a layer of depletion region will form near the semiconductor surface. The width of this depletion region is dependant on the dopant concentration, the position of the Fermi-level, and the interface trap energy levels. As the electric field from the SCM probe is too small to have any significant impact on these regions, the interface trap charge remains constant regardless of the dc bias applied.

Now in the region directly under the probe (shaded area), there may or may not be any interface trap charge, depending on the dc bias applied between the SCM probe and substrate and band bending at the surface. However at the edge of the region below the SCM probe (Region 1), the lateral electric field lines of the interface trap charge from adjacent region will create a depletion region physically under the SCM probe. The extent of this depletion region is a function of dopant concentration, interface trap charge densities and energy levels. Under the probe but further away from the edge (Region 2), the influence of the lateral electric field of interface traps is smaller and is not depleted as much. The carrier distribution under the SCM probe is thus non-uniform, and this could affect the C-V characteristic of SCM measurement which is a strong function of carrier concentration, leading to a different behaviour from a MOS capacitor. In fact as the SCM probe is so small, it is likely that the entire region under the SCM probe (shaded area) is affected by the electric field from the charge of fringe interface traps. A good analogy to this effect is the short channel effect of MOSET's as mentioned before: the approximation of uniform electric field under gate is invalid when the gate length is small. Of course when the probe tip size is sufficiently large, it can be treated roughly as uniform and the C-V characteristic of such a case should be similar to MOS capacitor.

In the next section we present simulation results to investigate how this influence varies with dopant concentration, interface trap energy distributions and trap densities.

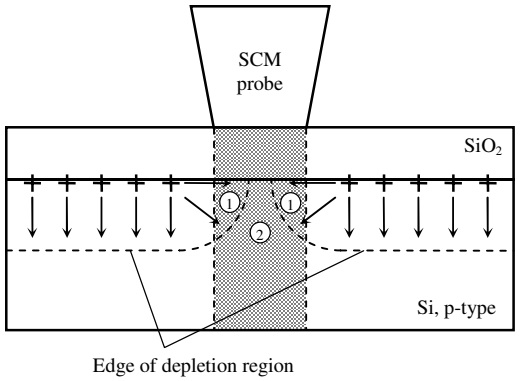

Figure 2. SCM probe sitting on a p-type semiconductor test sample.

IV. Simulation

The measurement is simulated using the small-signal ac analyser in Silvaco's Atlas 2-D device simulator to compute the small-signal gate/probe-to-substrate capacitance as a function of dc bias. The SCM probe tip was modelled with half angle = 17°, probe radius = 10 nm and the SCM oxide thickness = 8 nm. The substrate is uniformly doped with $N_A = 1 \times 10^{15}$ cm^{-3}. Three cases are simulated as summarized in Table 1. Sample A is trap-free. Sample B and C contain two

discrete trap energy levels (one donor trap and one acceptor trap) but different densities.

V. RESULTS

Here we demonstrate that in the case of interface traps not responding to V_{ac}, the dC/dV is not the same as the derivative, or slope, of C-V curve. Fig. 3 (a) compares the simulated C-V curve of Sample A (trap-free) and Sample B (with interface traps). These two samples have identical dopant concentrations. The C-V curve of Sample B is stretched-out compared to Sample A. This is as expected from the standard MOS capacitor theory.

Fig. 3 (b) shows the plots of dC/dV-V of the same samples. For Sample A it is obtained by differentiating the C-V curve, and for Sample B the technique described in the previous section is used. The dC/dV-V of Sample B has a broader full-width-at-half-maximum (FWHM) as its C-V curve is stretched in the presence of interface traps. We would like to point out the dC/dV-V of Sample B has a larger peak dC/dV value compared to Sample A. This contradicts the general notion that a stretched C-V would have a smaller peak dC/dV. The reason behind this is due to the charge of the fringe interface traps near the SCM probe and will be discussed in detail later.

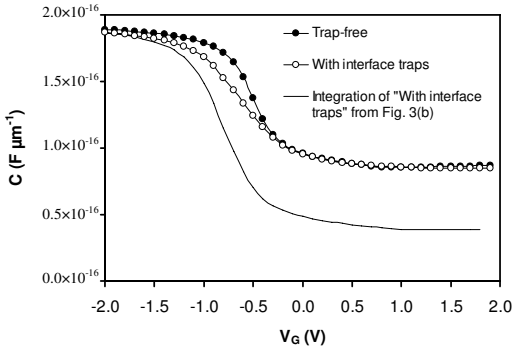

Figure 3 (a). Simulated C-V curves of SCM samples with uniformly doped p-type substrate

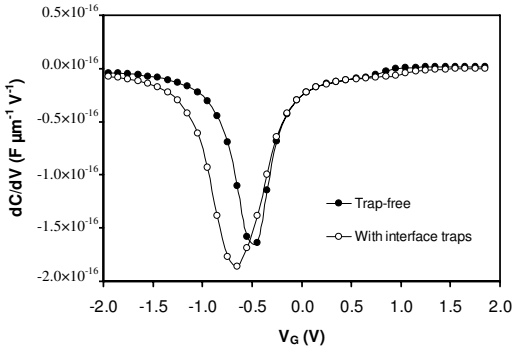

Figure 3 (b). Simulated dC/dV-V curves of SCM samples with uniformly doped p-type substrate

Next we explored the inverse process of integrating dC/dV plots to get back the C-V curves, as could be done with experimental dC/dV versus bias plots. As expected, in the absence of interface traps, integrating the dC/dV-V of Sample A in Fig. 3 (b) will yield the original C-V curve of Sample A in Fig. 3 (a). However when we integrate the dC/dV-V of Sample B in Fig. 3 (b), we get the deep-depletion like C-V curve (thin solid line) as shown in Fig. 3 (a), which is different from the C-V curve of Sample B. This is because the dC/dV-V of Sample B (and the same, we argue, applies to experimental dC/dV curves) does not represent differentiation of the C-V curve when interface traps are present due to the fact that the interface traps do not respond to the V_{ac} signal used to obtain dC/dV-V in the first place.

VI. DISCUSSION

From MOS capacitor theory, we expect to see identical peak dC/dV regardless of the presence of interface traps [11] if using the simulation technique described above. The fact that in Fig. 3 (b) the two set of simulation data have different peak dC/dV contradicts our belief and promotes us to investigate the causes of such discrepancy.

Close inspection reveals that for a p-type substrate, the positive charge of the fringe interface traps surrounding the SCM probe creates a depletion layer near the semiconductor surface, and even alters the carrier distribution directly underneath the SCM probe as explained before. Thus in the region under the SCM probe, the carrier distribution is affected by both the probe-to-substrate voltage, as well as the lateral electric field of the interface traps from adjacent regions. We analyse this by considering the charge and carrier distribution depicted in Fig. 4 (a). While a dc bias is applied to cause accumulation at the surface under the SCM probe, the positive charge of fringe donor traps depletes the holes below the surface. We also plot in Fig. 4 (b) the hole concentration vs. the distance from the semiconductor surface directly under the SCM probe (as indicated by the cross-section line in Fig. 4 (a)) from our simulation, with the SCM probe biased to hold the surface hole concentration at approximately the same level (slightly accumulated) as the bulk, 1×10^{-15} cm^{-3}. It is clear that a depletion region exists between the surface and the bulk. This non-monotonic distribution of carrier concentration is not seen in a MOS capacitor, resulting in smaller capacitance than that of a trap-free sample at the same surface potential. As we sweep the dc bias to accumulate the surface, the increasing electric field from the SCM probe to attract holes will eventually dominate over the repelling electric field from the fringe interface trap charge. The disappearance of the depletion region under the SCM probe allows the capacitance to increase rapidly, hence the peak dC/dV. Consequently the peak dC/dV in the presence of interface traps no longer occurs near flatband condition; instead it occurs when the semiconductor surface is accumulated. Thus for SCM measurement in the presence of interface traps, the capacitance, and hence peak dC/dV, is no longer governed by the dc bias only, but also by the charge of fringe interface traps near the SCM probe.

The depletion region caused by the fringe interface trap charge, and hence its influence on SCM data, is dependent on the substrate dopant doping, and the density and energy distribution of the interface traps. The impact of the fringe interface trap charge will be more pronounced when: (1) the

dopant concentration is low, which will increase the extent of the depletion region, (2) the interface trap density is high, which allows more charge in the interface traps, and (3) donor trap energy level is high (further away from E_V), which reduces its occupancy hence leading to more charge in the interface traps.

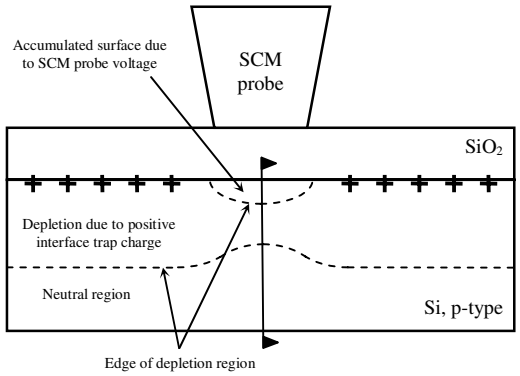

Figure 4 (a). Depletion due to interface trap charge

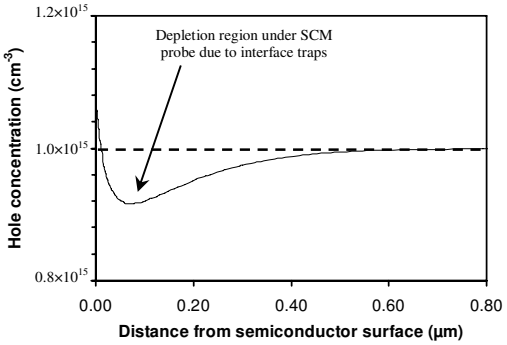

Figure 4 (b). Hole concentration vs. distance from semiconductor surface below SCM probe

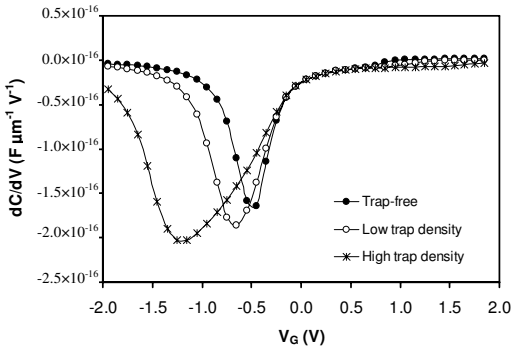

Figure 5. Comparison of simulated dC/dV of trap-free, low trap density and high trap density

In Fig. 5 we plot the simulated dC/dV-V of Sample C together with the two curves from Fig. 3 (b). Sample C has the same dopant concentration and interface trap energy levels as Sample B, but higher interface trap density. This curve has broader FWHM than the other two, and most importantly, an even larger peak dC/dV than the curve of smaller interface trap density, indicating that the higher charge of fringe interface traps alters the SCM data even more. To confirm this point we also performed simulation of the same interface trap energy level and density on a MOS capacitor, ie. no electric field from the fringe interface trap charge. The result (not shown here) is a dC/dV-V curve with broader FWHM than a trap-free case but identical peak dC/dV.

VII. Conclusion

In this paper we have described a new technique for simulating the dC/dV in SCM measurement. We have also investigated the effects of interface traps on SCM data, and analysed the associated physics involved. The interface trap charge creates a depletion region physically under the SCM probe due to its small dimension, similar to the short channel effect of MSOFET's. This causes the C-V characteristic of SCM to behave differently to a MOS capacitor. To avoid such discrepancy in the dopant profile extraction method using peak dC/dV as we proposed in [11], it is necessary to keep the interface trap densities minimum in the sample preparation processes.

References

[1] P. De Wolf, R. Stephenson, T. Trenkler, T. Clarysse, and T. Hantschel, "Status and review of two-dimensional carrier and dopant profiling using scanning probe microscopy," J. Vac. Sci. Technol. B 18, pp. 361-368, 2000.

[2] A.C. Diebold, M.R. Kump, J.J. Kopanski and D.G. Seiler, "Characterization of two-dimensional dopant profiles: status and review," J. Vac. Sci. Technol. B 14, pp.196-201, 1996.

[3] C. C. Williams, "Two-dimensional dopant profiling by scanning capacitance microscopy", Annu. Rev. Mater. Sci. pp. 471-504, 1999

[4] E.H. Nicollian an J. R. Brews, MOS Physics and Technology, Wiley, New York, 1982

[5] Y. Huang, C. C. Williams, "Capacitance-voltage measurement and modelling on a nanometer scale by scanning C-V microscopy", J. Vac. Sci. Technol. B 12, pp. 369-372, 1994

[6] Y. Huang and C.C. Williams, "quantitative two-dimensional dopant profile measurement and inverse modelling by scanning capacitance microscopy", Appl. Phys. Lett. 66, pp 344-346, 1995

[7] J.J. Kopanski, J.F.Marchiando and B.G. Rennex, "Carrier concentration dependence of the scanning capacitance microscopy signal in the vicinity of p-n junctions", J. Vac. Sci. Technol. B 18(1), pp. 409-413, 2000

[8] V.V. Zavyalov, J.S. McMurray, S.D. Stirling and C.C. Williams, "Two dimensional dopant and carrier profiles obtained by scanning capacitance microscopy on an actively biased cross-sectioned metal-oxide-semiconductor field-effect transistor", J. Vac. Sci. Technol. B18(1), pp. 549-554, 2000

[9] J. J. Kopanski, "Scanning Capacitance Microscopy", The Encyclopaedia of Imaging science and Technology, John Wiley & Sons, New York, 2001

[10] A.G. Grove, E. H. Snow, B. E. Deal and C. T. Sah, "Simple physical model for the space-charge capacitance of metal-oxide-semiconductor structures", J. Appl. Phys. vol 35, pp. 2458-2460, 1964

[11] Y. D. Hong, Y. T. Yeow, W. K. Chim, K. M. Wong and J. J. Kopanski, "Influence of Interface Traps and Surface Mobility Degradation on Scanning Capacitance Microscopy Measurement", IEEE Transactions On Electron Devices, Vol. 51. No. 9, pp. 1496-1503, 2004