Modeling mobility degradation in scanning capacitance microscopy for semiconductor dopant profile measurement

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ABSTRACT

This paper addresses the influence of mobility degradation on the SCM measurement via modeling and comparison with experimental SCM data. The rational for looking into mobility effect is that SCM capacitance measurement is carried out at 915 MHz. At this frequency, resistance of semiconductor surface can be comparable to the reactance of the SCM capacitance. In our simulation carrier mobilities at the semiconductor surface are set low compared to their bulk values to reflect surface mobility degradation. Our results show that the simulated SCM dC/dV is significantly reduced in the vicinity of p-n junction reflecting what is observed in experiment. We attribute this to the fact that the capacitance between the inverted surface and the SCM probe is not detected due to the high resistance (compared to the reactance of the SCM capacitance) of the inversion layer below the semiconductor and oxide interface. Only the capacitance on the accumulation side is extracted thus leading to the lowering of the detected SCM capacitance and dC/dV. The major conclusion is that the effect of high resistance due to mobility degradation has to be treated carefully for accurate extraction of dopant profile from experimental SCM data.

Keywords: Scanning capacitance microscope, dopant profile, mobility

1. INTRODUCTION

Scanning capacitance microscopy (SCM) has been reviewed as one of the most promising two-dimensional (2D) dopant profile extraction techniques [1, 2] to satisfy the spatial resolution and accuracy required for future generations of the semiconductor devices as identified by the International Technology Roadmap for Semiconductors [3]. A scanning capacitance microscope (SCM) consists of a capacitance sensor and an atomic force microscope (AFM). The AFM is used to control the position and contact force of the scanning probe tip, while the capacitance sensor measures the capacitance between the probe tip and the underlying semiconductor sample. Only minimal preparation is required for sample to be used in this technique. A thin layer of insulating oxide separates the doped semiconductor sample and the conductive probe tip, forming a structure very similar to metal-oxide-semiconductor (MOS) capacitor. The operation of SCM is based on the MOS capacitor theory. A dc bias is applied between the probe tip and substrate to sweep the semiconductor surface from accumulation to inversion. An ac signal is also applied to cause variations in the capacitance between the probe tip and the sample. These variations are measured by the capacitance sensor and are directly related to the dopant concentration.

To date the SCM has been commonly used for qualitative junction delineation. Typical SCM images display good contrast indicating the locations of p-type region, n-type region and space charge region. However quantitative dopant profile extraction by SCM is still facing difficulties: The selection of appropriate dc bias to acquire SCM image has been an interest to researchers [4]; wear in probe tip causes signals to distort and the influence of probe tip geometry has also been studied [5]. While the calibration curve method [6, 7], in which theoretical C-V curves are calculated and normalized based on the known substrate dopant concentration, has been proven successful for dopant profile extraction of uniformly doped substrates or modest dopant gradient, dopant profile extraction across a p-n junction still remains a challenging task [8, 9, 10, 11]. This is due to the fact that the influence of built-in field of a p-n junction induced space charge region and lateral supply of carriers are not considered when using the calibration curve method, and a better

understanding of the interaction between p-n junction and SCM probe is needed to correctly interpret SCM data. The degradation of carrier mobility on SCM measurement can also have an impact on SCM measurement. It is known that the surface carrier mobility of semiconductor can be significantly degraded from the bulk mobility, or even from that seen in structures with MOSFET-gate quality oxide. The effects of mobility degradation on SCM measurement have to be better understood and handled in order to enhance the accuracy of SCM as a quantitative tool for junction dopant profile extraction.

In this paper, we demonstrate the influence of mobility degradation on SCM by comparing the measured and simulated data. The difference observed in simulations with different mobility models is highlighted. We attribute this to the fact that SCM measurement is carried out at 915 MHz, which makes some of the reactance of the tip-substrate capacitance small compared to substrate resistance, and consequently some of the capacitance is not detected. The SCM data near p-n junction is particularly sensitive to this effect, and careful attention is required when interpreting the SCM data for dopant profile extraction.

2. METHODOLOGY

To investigate the influence of mobility degradation on SCM, we first obtained typical SCM $^{dC}/_{dV}$ experimental data from a semiconductor specimen with a p-n junction included. We then simulated the same setup for an assumed dopant profile with different mobility models. The instrumentation setup, sample preparation procedures and simulation modeling parameters are described below.

2.1 Experiment setup
The SCM measured data was collected using a DI 3000 Nanoscope operating in SCM bias ramping mode to capture $^{dC}/_{dV}$ as a function of dc bias. The sample with a 1-D silicon p^+-n junction was formed by boron implantation into an n-type substrate uniformly doped at 3×10^{17}cm^{-3}. The sample oxide is an 8 nm thick low temperature ozone grown oxide. Measurements of $^{dC}/_{dV}$ were taken at spatial intervals of approximately 0.1 micron across the p-n junction. For comparison, calibration between experimental measurement and simulation is done by using the data from the known substrate as the reference. The SCM measurement setup is illustrated in Fig. 1.

2.2 Simulation
The same SCM setup is also simulated to investigate the effect of surface mobility degradation. The small-signal ac analyzer in SILVACO's ATLAS 2-D device simulator [12] was used to compute the small-signal probe-to-substrate capacitance, C (shunted by small-signal substrate conductance), as a function of dc bias, similar to the detection process in actual SCM measurement. This modeling accounts for the effects of finite resistance of the silicon surface. The computed high frequency C is different from the quasi-static capacitance. It takes account of the fact that under the extremely high frequency 915 MHz probing signal the minority carriers are unable to respond, and the carriers are supplied from bulk instead of being generated locally in a p-n junction induced space charge region. From the computed C-V data, $^{dC}/_{dV}$ is then calculated by numerical differentiation. Short carrier lifetimes ($=10^{-7}$ s) and high signal frequency ($=915$ MHz) are chosen to produce high-frequency C-V response in the bulk regions. The probe tip was modeled with half angle $= 17°$, probe radius $= 10$ nm and the oxide thickness is taken as 8 nm, these parameters being the best description of the actual SCM setup. To demonstrate the effect of mobility degradation on SCM data, two mobility models are investigated. In the first model, constant hole and electron mobilities of 500 cm^2 V^{-1} s^{-1} and 1000 cm^2 V^{-1} s^{-1} respectively are defined throughout the sample. In the second model, both hole and electron mobilities are degraded to 1 cm^2 V^{-1} s^{-1} over 0.1 micron of the semiconductor near the surface but otherwise constant as in the first model.

3. EXPERIMENTAL AND SIMULATION DATA
3.1 Experimental data
The measured SCM data is shown in Fig. 2. $^{dC}/_{dV}$ is plotted as a function of dc bias, and position, x, with x = 0 set at the edge of the sample on the p^+ side. The peak $^{dC}/_{dV}$ of the known n-type substrate is used as the reference to normalize the raw $^{dC}/_{dV}$ data obtained from the instrumentation. The p-n junction is estimated to be at x = 1.9 µm according to Kopanski et al. [13]. The plot displays the results as we expect from standard theory, positive and negative peaks of

$^{dC}/_{dV}$ are observed in the n and p$^+$ regions, respectively. In the space charge region, both negative and positive peaks of $^{dC}/_{dV}$ are shown, similar to low frequency C-V curve. This is because majority carriers of both types are available for accumulation from either side of the space charge region [14].

3.2 Data of simulation with constant mobility

The simulated result for constant mobility for a p$^+$-n junction is shown in Fig. 3, with the assumed dopant profile shown in Fig. 4. It can be seen that in general the $^{dC}/_{dV}$ behaves in the same way as the experimental curve in Fig. 2, however there are several differences. In the space charge region, the $^{dC}/_{dV}$ contour lines exhibit high positive and negative peak $^{dC}/_{dV}$ in the form of sharp "tails" extending to positive and negative dc bias respectively, which are also seen in the simulations by Kleiman et al [9], instead of the rounded and smooth contours lines and low positive and negative peak $^{dC}/_{dV}$ of Fig. 2. The sharp tails correspond to high $^{dC}/_{dV}$ in depletion-to-inversion transition, similar to U-shaped low frequency C-V curves in conventional measurement. However the inversion carriers in this case are not generated in the space charge region, instead they are supplied from across the junction. The same effect has been observed in simulations of a range of assumed dopant profiles. It is relevant to add here that we also observed similar high positive and negative peak $^{dC}/_{dV}$ tails in 3-D simulation of a conical probe over the p-n junction. Hence we believe these tails are not artifacts of the 2-D simulation. We attribute the absence of high inversion $^{dC}/_{dV}$ peaks in measurement to the inversion capacitance is not detected in the actual device. We would like to emphasize that the absence of these tails in experimental data are one of the major problems encountered for dopant profile extraction using the calibration curve method. Within the vicinity of the p-n junction, where these high peak $^{dC}/_{dV}$ are present in simulation but absent in experimental data, the extracted dopant profile from the calibration curve method always results in unrealistic high dopant concentration, as low peak $^{dC}/_{dV}$ corresponds to high dopant concentration in this method. Another difference between experimental and simulation results is the effect of interface traps present in the experimental sample. The peak $^{dC}/_{dV}$ values are independent of the interface traps; however the C-V curve is stretched [15, 16, 17]. This is because most of the interface traps are not able to respond to the high frequency 915 MHz used in SCM measurement. We have rescaled the dc bias of Fig. 2 to an effective dc bias when there is no interface traps using the method described in [17]. This allows us to directly compare the result with simulation where interface traps are not included. The rescaled applied voltage is shown as the second x-axis in Fig. 2.

3.3 Data of simulation with mobility degradation

Research has shown that carrier mobility near the semiconductor surface is lower than the bulk value [18, 19]; this is particularly so for the SCM oxide-silicon interface which can be expected to be high in various forms of crystal defects and interface trap density. This is especially important for inversion layer carrier transport which is parallel to the surface, which we believe to be the main cause of the difference observed between Fig. 2 and Fig. 3. Hence we repeated the simulation of Fig. 3 with the degraded mobility model to investigate the effect of mobility degradation on SCM measurement.

The simulation result of the second mobility model corresponding to mobility degradation effect is shown in Fig. 5. The main difference between this figure and Fig. 3 is the absence of the long tails of high $^{dC}/_{dV}$ in the space charge region, corresponding to $^{dC}/_{dV}$ peaks at depletion-to-inversion transition. While the assumed dopant profile is not meant to be representing the actual profile of the experimental sample of Fig. 2, the better qualitative agreement between Fig. 2 and Fig. 5 indicates that mobility degradation has to be taken into consideration when interpreting data from SCM measurement.

4. DISCUSSION

To analyze the effect of mobility degradation on the SCM data, we examine the p-n junction and non-junction regions separately.

4.1 Effect of mobility degradation in non-junction region

The mobility degradation effect on the SCM data for a non-junction test structure is shown in Fig. 6, which is a series of simulation results of a p-type substrate uniformly doped at 1×10^{16}cm^{-3} with different carrier mobility parameter. It shows that the capacitance decreases as the carrier mobilities decrease. This effect is especially prominent on the accumulation side of the C-V curve. The physics to account for the reduction in capacitance due to mobility degradation

can be explained as follows. In the SCM, the total capacitance measured is the serial combination of the oxide capacitance and the depletion capacitance. So the SCM can be modeled by a capacitance C_s, representing the total capacitance, and a resistance R_s, representing the semiconductor substrate resistance, in series as shown in Fig. 7 (a). However in the SCM simulation and the actual measurement, the capacitance and the resistance are extracted by measuring the imaginary and the real components of the current between the probe tip and the back contact respectively, hence the total impedance through which the electric current flow can be represented by a resistance R_p and a capacitance C_p in parallel, as shown in Fig. 7 (b). The conversion between the series RC and parallel RC can be mathematically derived from the fact that the total impedance Z_{total} is the same in both cases. In the series RC model,

$$Z_{total} = \frac{1}{j\omega C_s} + R_s \quad (1)$$

and in the parallel RC model,

$$Z_{total} = \frac{1}{\dfrac{1}{R_p} + j\omega C_p} \quad (2)$$

By equating the real component and the imaginary component of the total impedance from both models, an expression of the extracted capacitance C_p as a function of the semiconductor resistance R_s can be obtained,

$$C_p = \frac{C_s}{1 + (\omega C_s R_s)^2} \quad (3)$$

From this expression, it can be seen that the extracted capacitance C_p is smaller than the actual capacitance C_s if the semiconductor resistance is large, which could be caused by the degradation of carrier mobilities. The difference between C_p and C_s becomes very significant when the series resistance R_s is greater than the reactance of the series capacitance $1/j\omega C_s$. It is also observed that the decrease of capacitance due to the degradation of mobility is more prominent for semiconductor with low dopant concentration. This is due to the fact that the substrate resistance is larger in this case.

4.2 Effect of mobility degradation at p-n junction

In the vicinity of the p-n junction, the effect of mobility degradation is much more significant and can be explained using Fig. 8. In this figure a SCM probe is positioned at the junction, with a positive dc bias with respect to the substrate such that it induces inversion in the p-side and accumulation in the n-side. A lumped small-signal equivalent circuit of the structure is superimposed on the structure. The total capacitance between the probe tip and the semiconductor consists of three components: C_1, the oxide capacitance between the probe tip and the substrate immediate below the probe; C_2, the fringing capacitance between the side of the probe and the accumulated layer on the n-side and C_3, the fringing capacitance between the side of the probe and the inverted layer on the p-side. As the probe tip diameter is small, it can be expected that C_1 is small and hence C_2 and C_3 become a significant fraction of the total capacitance. C_1, C_2 and C_3 are coupled through resistance R_a, R_b and R_c to the substrate respectively. R_a is the resistance of the n-type substrate, R_b is the resistance of the accumulated n-type surface and R_c is the resistance of the n-type inverted surface over the p-type region. R_a and R_b are typically small, whereas R_c could be high when the surface mobility is low. At the frequency 915 MHz used in SCM measurement, R_c could be large compared to $1/j\omega C_3$, and consequently the inversion capacitance C_3 cannot be detected, leading to the absence of $^{dC}3/_{dV}$ in the SCM data. The result is that the positive $^{dC}/_{dV}$ peak contributed from the inversion capacitance C_3 is not seen in the measured SCM data, while C_1 and C_2 are coupled through small resistances R_a and R_b and there is no problem for them being detected. To verify this, we repeated the simulation with degraded mobility but with the RF signal frequency reduced to 1 MHz. The SCM $^{dC}/_{dV}$ contour plot (not shown here) obtained is similar to that of Fig. 3 where uniform high mobility is used.

The present work does not conclusively prove a cause and effect relationship between mobility degradation and shape of experimental SCM $^{dC}/_{dV}$ contour. However, there is sufficient known evidence of surface mobility degradation that is

applicable to the silicon surface of SCM specimens and our simulation verifies that such degradation has very significant influence on the SCM $^{dC}/_{dV}$ contours. In fact, to date all simulations have never been able to resemble the absence of high peak $^{dC}/_{dV}$ near the p-n junction seen in the experimental data. By including mobility degradation in our simulation, we have produced the first simulated result with similar $^{dC}/_{dV}$ contours near the p-n junction, making mobility degradation the only known physics to account for this phenomenon. Thus for dopant profile extraction with SCM, we believe that mobility degradation has to be considered for accurate SCM data interpretation. Further investigation is required to determine how carrier mobilities can be appropriately adjusted as a parameter in SCM simulation in order to produce more realistic results to match experimental data.

5. CONCLUSIONS

In this paper we have demonstrated the mobility degradation effect on SCM data by comparing the experimental and simulated results. We investigated and explained the effect in both non-junction region and space charge region. In the non-junction region, the extracted capacitance is lower than the actual capacitance when the carrier mobility is low due the increase in the semiconductor substrate resistance. The reduction of the extracted capacitance due to mobility degradation is more prominent in the lightly doped region than in the heavily doped region. In the space charge region, the difference in capacitance due to mobility degradation could be very significant. The inversion-depletion capacitance is not detected due to the relatively high resistance though which the capacitance is coupled to the substrate. By accounting for the mobility degradation, we obtained better agreement between the simulated and measured SCM data. The high peak $^{dC}/_{dV}$ near the p-n junction seen in previous simulations but absent in experimental data is significantly reduced when surface mobility degradation is included the simulation. Therefore we conclude that the mobility is an important factor to be considered for accurate SCM data interpretation and should be carefully treated.

ACKNOWLEDGEMENTS

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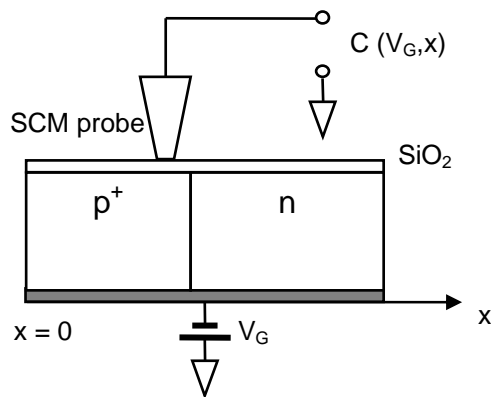
Fig. 1: SCM setup. A DI 3000 Nanoscope operating in SCM bias ramping mode was used to capture $^{dC}/_{dV}$ as a function of dc bias at spatial intervals of approximately 0.1 micron across a 1-D silicon p^+-n junction formed by boron implantation into a n-type substrate uniformly doped at 3×10^{17}cm^{-3}.
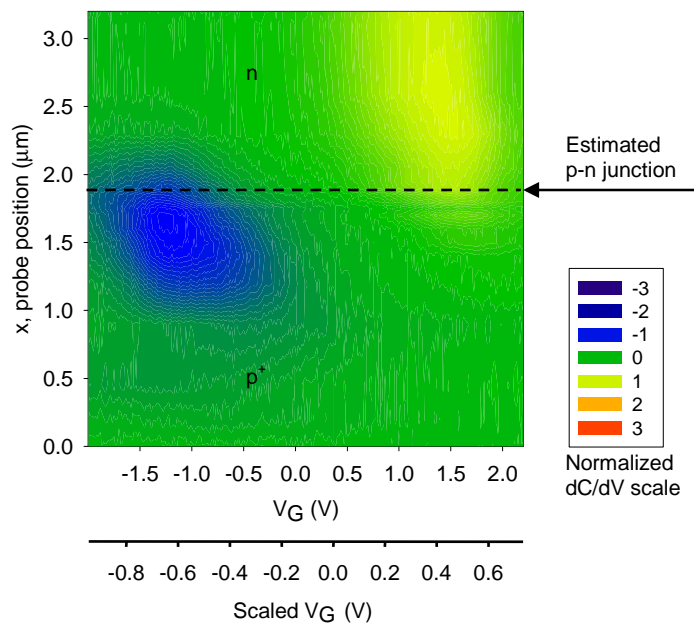

Fig. 2: Contour plot of experimental $^{dC}/_{dV}$ as a function of dc bias, V_G, and position, x for a p^+-n junction, with x = 0 set at the p^+ edge. The second x-axis is the rescaled dc bias based on comparison with simulated $^{dC}/_{dV}$ data to account for the presence of interface traps.
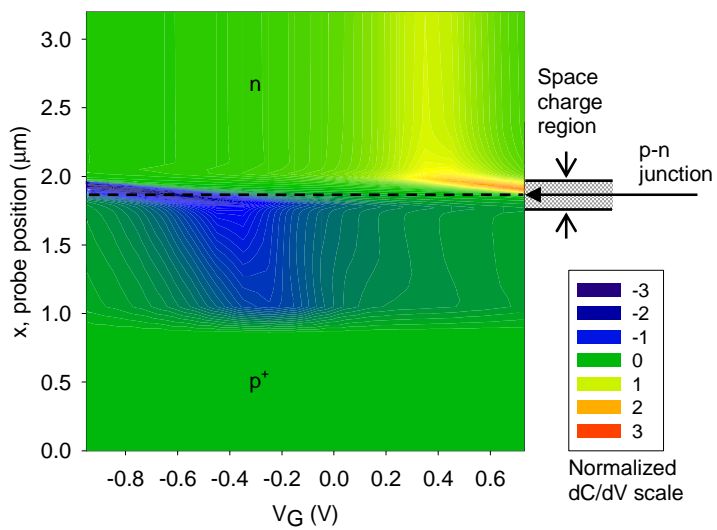
Fig. 3: Contour plot of simulated $^{dC}/_{dV}$ as a function of dc bias, V_G, and position for a p^+-n junction based on constant mobility.
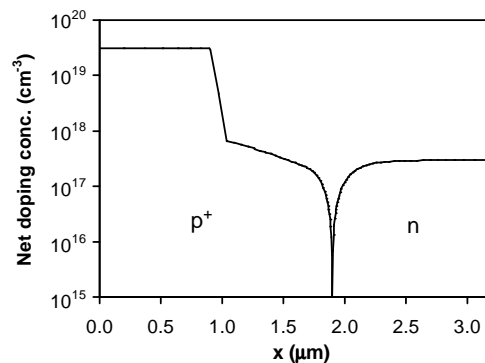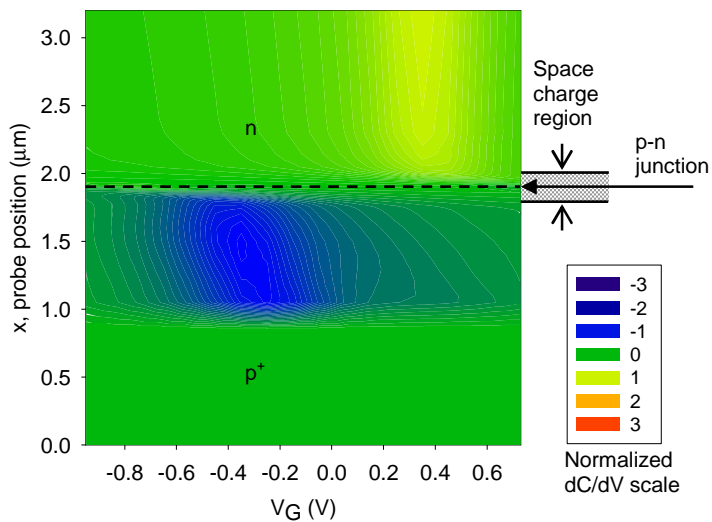

Fig. 4: Assumed dopant profile for simulation.

Fig. 5: Contour plot of simulated $^{dC}/_{dV}$ as a function of dc bias, V_G, and position for a p^+-n junction based on a degraded surface mobility model (see text for mobility model).
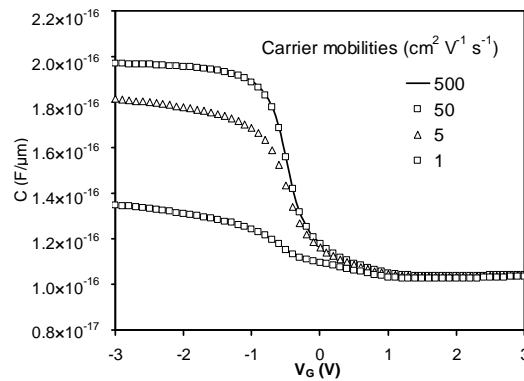

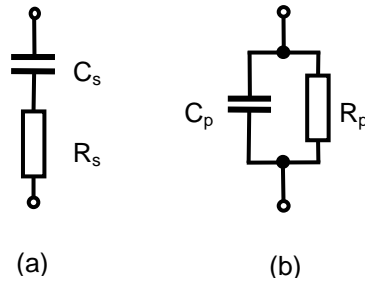Fig. 6: Simulated C-V for a p-type substrate uniformly doped at $1 \times 10^{16} cm^{-3}$.

Fig. 7 (a): Series RC model. C_s, represents the total capacitance, consisting of oxide capacitance and depletion capacitance in series, and, R_s represents the semiconductor substrate resistance.

Fig. 7 (b): Parallel RC model. C_p and R_p represent the imaginary and real components of the impedance respectively, through which electric current flow when extracting capacitance in SCM measurement.
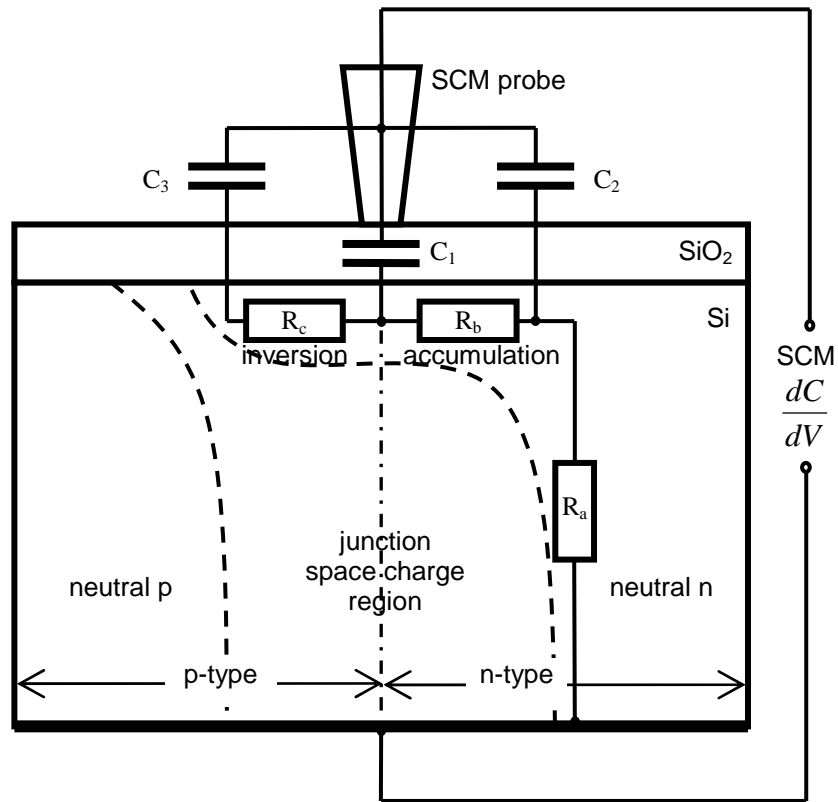

Fig. 8: Lumped-element circuit model of SCM measurement with probe tip located at the junction and dc bias inducing accumulation on the n-side and inversion on the p-side. C_1 is the oxide capacitance between the probe tip and the substrate immediate below the probe. C_2 is the fringing capacitance between the side of the probe and the accumulated n-side. C_3 is the fringing capacitance between the side of the probe and the inverted layer on the p-side. Ra, R_b and R_c are the resistance through which C_1, C_2 and C_3 are coupled to the substrate respectively.