Monitoring Oxide Quality Using the Spread of the dC/dV Peak in Scanning Capacitance Microscopy Measurements

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Abstract—**This article proposes a method for evaluating the quality of the overlying oxide on samples used in scanning capacitance microscopy (SCM) dopant profile extraction. The method can also be used generally as a convenient in-process method for monitoring oxide quality directly after the oxidation process without prior metallization of the oxide-semiconductor sample. The spread of the differential capacitance characteristic (dC/dV versus V plot), characterized using its full width at half maximum (FWHM), was found to be strongly dependent on the interface trap density as a consequence of the stretch-out effect of interface traps on the capacitance–voltage (*C–V*) curve. Results show that the FWHM of the dC/dV characteristic is a sensitive monitor of oxide quality (in terms of interface trap density) as it is not complicated by localized oxide charging effects as in the case of the SCM probe tip voltage corresponding to maximum dC/dV. The magnitude of the dC/dV peak, at any given surface potential, was also found to be independent of the interface traps and only dependent on the substrate dopant concentration, which makes SCM dopant profile extraction possible.**

Index Terms—**Interface trap, oxide quality, scanning capacitance microscopy (SCM), semiconductor dopant extraction.**

I. Introduction

SPATIAL resolution of less than 10 nm has been identified as a requirement for accurate quantitative two-dimensional (2-D) dopant profiling by the International Technology Roadmap for Semiconductors (ITRS) [1]. Since scanning capacitance microscopy (SCM) [2]–[4] can potentially meet this goal, SCM is developing into an important technique for dopant profiling of submicrometer semiconductor structures. Other techniques [5]–[9] have also been investigated as potential candidates for high-resolution 2-D dopant profiling. The SCM technique is based on the high frequency response of the metal–oxide–semiconductor (MOS) structure, formed between the SCM probe, sample oxide and semiconductor. The semiconductor dopant concentration under the probe is

characterized by the change in capacitance, dC, induced by a bias voltage change, dV, applied between the probe and sample. The qualitative aspects of SCM imaging and the bias-dependent contrast formation have been studied and are relatively well understood [10]–[12]. In an earlier work, we proposed a more accurate ratio calibration approach [13], as compared to the calibration curve method [14], [15], to SCM dopant concentration extraction. The approach makes use of combined inverse modeling and forward simulation, based on a 2-D numerical device simulator MEDICI [16], of SCM measurement data. However, the success of the ratio calibration method is highly dependent on *a priori* estimates of the interface trap (D_{it}) and oxide fixed charge (N_f) densities in the inverse modeling. Goghero *et al.* [17] have suggested using the hysteresis of forward and reverse sweep SCM differential capacitance (dC/dV) characteristics, while Bowallius and Anand [18] have proposed using the spread of the dC/dV peak for evaluating oxide quality. However, there has been no detailed work that explicitly attempts to correlate the spread and location of the dC/dV peak with the measured interface trap density. This will be addressed in this work, where we will show that the interface trap density does sensitively affect the shape of the dC/dV characteristic plot.

II. Experimental Details

The differential capacitance was measured as a function of the tip-sample dc bias, as this was swept from -12 to 12 V, using a Digital Instruments Dimension 3000 SCM [19]. In the SCM measurement setup, bias was applied to the sample and the cobalt-coated silicon probe tip was grounded. To enable comparison with *C–V* measurements, which are typically expressed in terms of the gate electrode voltage, the SCM dC/dV results shown henceforth are presented in the form of dc bias applied to the probe tip, V_{tip}, with respect to the sample. The dC/dV sweep measurement was performed at an ac frequency of 90 kHz and ac bias of 100 to 300 mV on several (about 15 to 20) locations across the entire oxide covered silicon sample. Our dc bias sweep rate of 0.1 Hz between -12 to $+12$ V is much higher than the typical 10 mV/s required for equilibrium to be established between the applied dc bias and the occupancy (charging) of the interface traps. Generally we do observe hysteresis between the forward and reverse dC/dV sweeps, especially for large sweep ranges. The oxide quality (i.e., N_f and D_{it}) was characterized using MOS capacitor test dots (area $= 2.54 \times 10^{-4}\,\text{cm}^{-2}$). N_f was extracted by comparing the experimental two-frequency

TABLE I
DESCRIPTION OF SAMPLES (SILICON (Si) SUBSTRATE WITH A THERMALLY GROWN OXIDE) AND SUMMARY OF C–V AND SCM MEASUREMENTS. ALL SAMPLES (BOTH p AND n TYPE SILICON) HAVE ROUGHLY THE SAME SUBSTRATE DOPING CONCENTRATION ($N_{\mathrm{sub}} \sim 2 \times 10^{15}$ cm^{-3}). THE ELECTRICAL OXIDE THICKNESS (t_{ox}) AND FLAT-BAND VOLTAGE (V_{fb}) WERE EXTRACTED FROM HIGH-FREQUENCY C–V MEASUREMENTS USING A TWO-FREQUENCY ($f = 100$ kHz AND 200 kHz) CORRECTED TECHNIQUE ON THE CAPACITOR DOTS. V_{fb} HAS BEEN CORRECTED TO THAT OF A COBALT GATE ELECTRODE/PROBE TIP WHICH IS USED IN THE SCM MEASUREMENTS, BASED ON THE WORK FUNCTION DIFFERENCE (0.9 eV) BETWEEN COBALT AND ALUMINUM, TO FACILITATE COMPARISON WITH V_{tip} CORRESPONDING TO MAXIMUM dC/dV. THE TABLE ALSO SHOWS THE AVERAGE AND STANDARD DEVIATION OF THE PROBE TIP VOLTAGE (V_{tip}) CORRESPONDING TO THE PEAK OF THE dC/dV PLOT OBTAINED FROM SCM MEASUREMENTS ON 15 TO 20 DIFFERENT LOCATIONS ON EACH SAMPLE. THE AVERAGE SPREAD OF THE dC/dV CHARACTERISTIC (dC/dV VERSUS V PLOT), CHARACTERIZED USING THE FWHM, AND THE STANDARD DEVIATION OF THE SPREAD AT 15 TO 20 DIFFERENT LOCATIONS ON EACH SAMPLE ARE ALSO SHOWN

Sample	Oxide/ Substrate Type	t_{ox} (nm)	V_{fb} (V) (cobalt gate/probe tip)	V_{tip} (V) at maximum dC/dV (Mean ± Std. dev.)	FWHM (V) of dC/dV versus V (Mean ± Std. dev.)
C3p1	Nitrided Oxide/ p-type Si	3.1	-0.24	0.096 ± 0.214	0.273 ± 0.115
C3p2	Nitrided Oxide/ p-type Si	3.2	-0.27	0.159 ± 0.428	0.254 ± 0.080
M3n1	Non-nitrided Oxide/ n-type Si	3.7	0.06	-7.270 ± 0.416	1.315 ± 0.285
M3n2	Non-nitrided Oxide/ n-type Si	3.7	0.10	-7.427 ± 0.941	3.195 ± 0.551
M4p1	Non-nitrided Oxide/ p-type Si	4.4	-0.25	-0.803 ± 0.364	0.936 ± 0.312
M4p2	Non-nitrided Oxide/ p-type Si	4.9	-0.38	2.867 ± 0.424	1.024 ± 0.195
M6p1	Non-nitrided Oxide/ p-type Si	6.6	-0.4	1.047 ± 0.487	0.936 ± 0.212
M6p2	Non-nitrided Oxide/ p-type Si	6.3	-0.49	-1.404 ± 0.261	0.810 ± 0.236

($f = 100$ kHz and 200 kHz) corrected C–V curve [20] to an ideal (zero N_f) calculated C–V curve and noting the shift in the flatband voltage V_{fb}. The interface trap density D_{it} was obtained from conductance measurements, at varying gate bias and frequency [21]. Details of the various samples used are shown in Table I together with results of C–V and SCM measurements performed. The industrial-grade nitrided oxides and in-house fabricated nonnitrided oxides were grown by rapid thermal oxidation at 900 to 1000 °C. All samples have about the same substrate doping concentration ($N_{\mathrm{sub}} \sim 2 \times 10^{15}$ cm^{-3}) but varying targeted oxide thickness (t_{ox}) from about 3 to 7 nm. The range of t_{ox} (see Table I for measured values) investigated in this study is comparable to the thickness of the low-temperature ($<400°$C) oxide typically used for SCM dopant extraction [22]. Samples C3p2, M3n2, M4p2, and M6p2 are identical to the respective samples C3p1, M3n1, M4p1, and M6p1, except that they have not been subjected to a final anneal step at a temperature of 400 °C in an ambient of 10% H_2 and 90% N_2 (forming gas) for 3 min.

III. RESULTS AND DISCUSSION

Fig. 1(a) and (b) show typical plots of dC/dV versus V_{tip} for the nitrided (C3p1 and C3p2) and nonnitrided (M4p1 and M4p2) oxide samples, respectively. Except for C3p1 and C3p2, V_{fb} does not fall within the range of V_{tip} corresponding to maximum dC/dV, as seen from Table I. This is because during the dC/dV measurement, charge trapping in the oxide could occur

at the probe tip location (unless the oxide quality is very good or the oxide is very thin as in the case of C3p1 and C3p2) and this will affect the value of V_{tip} corresponding to maximum dC/dV. Calculations of the dC/dV signal versus tip voltage were also performed by solving the Poisson equation assuming a one-dimensional MOS structure [23]. The opposite polarity of V_{tip} corresponding to the dC/dV peak for M4p2 in Fig. 1(b), as compared to the calculated results in Fig. 1(d), is suspected to be due to oxide charge trapping during the dC/dV sweep [24], since the oxide quality of M4p2 is relatively poor. In addition, the large tip voltage at which the experimental dC/dV peak occurs in M3n1 and M3n2 (see Table I) is explained similarly. Our calculations have shown that an oxide trapped charge density of 5×10^{13} cm^{-2} at the oxide-silicon interface can cause the V_{tip} corresponding to maximum dC/dV to shift to about -7.5 V, as observed in the dC/dV measurements for M3n1 and M3n2. This poorer oxide quality is not a result of the different doping type of the substrate for M3n1 and M3n2.

Fig. 2 shows the magnitude of the average of probe tip voltages ($|V_{\mathrm{tip(average)}}|$) corresponding to maximum dC/dV plotted against the mid-gap interface trap density ($D_{it(mg)}$) and N_f. It is seen that there is a strong dependence of $|V_{\mathrm{tip(average)}}|$ on $D_{it(mg)}$ for $D_{it(mg)} > 2 \times 10^{11}$ cm^{-2} eV^{-1}. However, $|V_{\mathrm{tip(average)}}|$ varies widely over a small range of N_f, and this was suspected to be due either to the almost constant N_f for all samples or an artifact of the localized oxide charging during the dC/dV sweep. Although the SCM probe tip voltage magnitude corresponding to maximum dC/dV correlates well with the interface trap density in Fig. 2, the sign of this peak location could be complicated by localized oxide charging effects, as can occur during the dC/dV sweep. For example, in Fig. 1(b), the voltage location of the dC/dV peak has different signs for M4p1 and M4p2. A similar observation is seen for M6p1 and M6p2 (see Table I) even though these samples have almost identical interface trap densities.

Fig. 3 shows the calculated full width at half maximum (FWHM) of the dC/dV characteristic for oxide thickness ranging from 3 to 7 nm and measured FWHM for the various samples. It is seen that there is greater dependence of the FWHM on oxide thickness variation when the interface trap density is high. While not implying that the oxide thickness variation of the various locations tested is as drastic as that used in the calculation of the FWHM, the local variation in oxide quality and thickness (either due to processing variations or the presence of a nonuniform contaminant film on the bare oxide) among the different measured locations are possible reasons for the larger variation in the measured FWHM, especially for samples with high D_{it} (e.g., M3n1 and M3n2). Fig. 3 also shows that a large $D_{it(mg)}$ will result in a large FWHM, which is a consequence of the stretch-out effect of interface traps on the C–V curve. Therefore, the FWHM of the dC/dV peak is very sensitive to the interface trap density and can be used as a monitor of the latter in SCM measurements. It seems that the interface trap concentration does not affect greatly the magnitude of the dC/dV peak as seen by comparing Fig. 1(a) (a low interface trap density sample) with Fig. 1(b) (a high interface trap density sample). The insensitivity of the magnitude of the dC/dV peak to the interface trap concentration could possibly
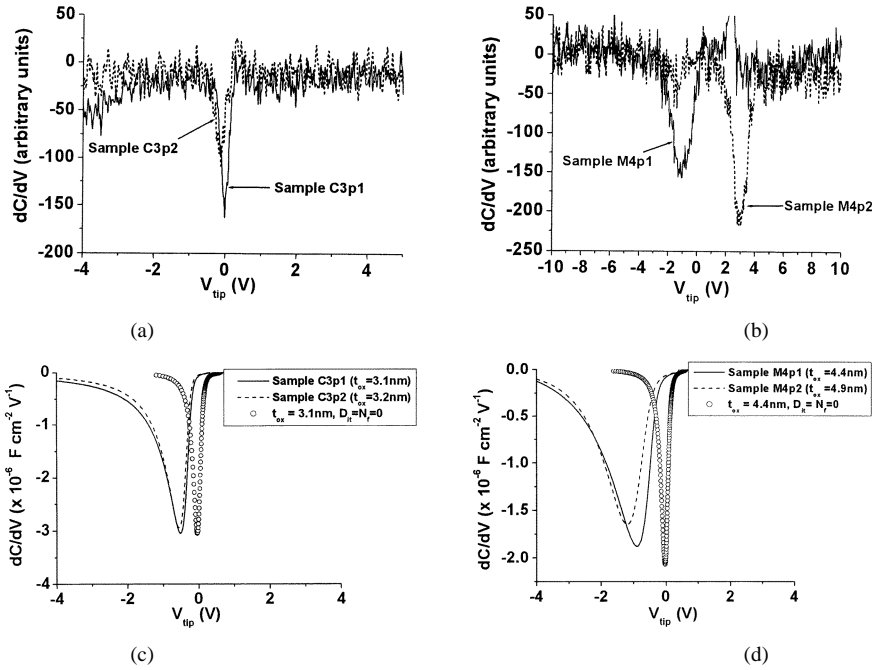
(a)

(b)

(c)

(d)

Fig. 1. Typical plots of dC/dV versus probe tip voltage (V_{tip}) for samples (a) C3p1 and C3p2, and (b) M4p1 and M4p2. The phase of the SCM lock-in detection circuit has been set to result in dC/dV signals of similar polarity for p-type and n-type samples. Calculated dC/dV (for a substrate doping of 2×10^{15} cm^{-3}) versus cobalt probe ($\mathrm{work\ function} = 5.0$ eV) tip voltage (V_{tip}) for samples (c) C3p1 and C3p2, and (d) M4p1 and M4p2. Electron acceptor and donor interface traps (energy distribution extracted from conductance measurements) were assumed to be located in the upper and lower half of the bandgap, respectively, in the calculations. The calculated dC/dV plot for a control sample ($D_{it} = N_f = 0$) is also shown (open circle symbol).
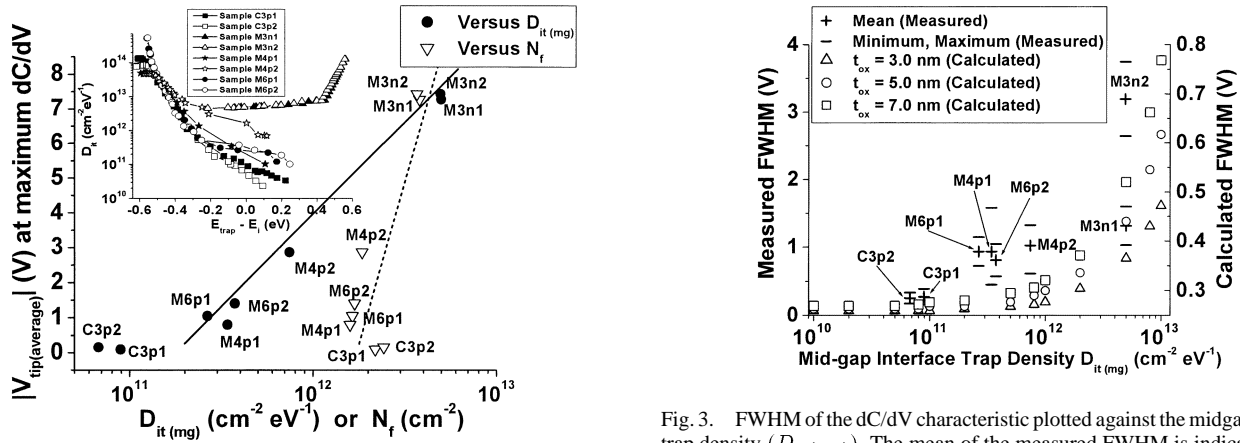

Fig. 2. Magnitude of the average of probe tip voltages ($|V_{\text{tip(average)}}|$) corresponding to maximum dC/dV plotted against the mid-gap interface trap density ($D_{it(mg)}$) and oxide fixed charge density (N_f). The solid and dash lines are merely visual aids to show the general trend of the results. The inset shows the energy distribution of the interface trap density (D_{it}) that was obtained from conductance measurements for each sample. The horizontal axis of the inset shows the trap energy (E_{trap}) measured from the intrinsic Fermi level (E_i). $D_{it(mg)}$ is the value of D_{it} when $E_{\text{trap}} = E_i$.

be explained by the fact that the interface traps are not able to respond to the extremely high frequency of 915 MHz of the SCM resonant detector circuit, from which the dC/dV signal was obtained, except for the faster interface traps (with small time constants) located close to the band edges. As for the 90 kHz ac signal, while this does effectively switch the effective dc bias, most interface traps likewise would not respond to this high frequency signal, so that the change in capacitance detected is close to the slope (equivalent to the magnitude of the dC/dV peak) of an ideal interface trap-free high-frequency C–V

Fig. 3. FWHM of the dC/dV characteristic plotted against the midgap interface trap density ($D_{it(mg)}$). The mean of the measured FWHM is indicated by the cross symbol while the minimum and maximum values of the measured FWHM are indicated by the horizontal bars. The difference between maximum and minimum values is equivalent to two standard deviations of the data obtained from 15 to 20 different locations on each sample. The calculated FWHM for various oxide thickness t_{ox} of 3, 5, and 7 nm are indicated by the triangle, circle, and rectangle symbols.

curve. This results in the magnitude of the dC/dV peak, at any given surface potential, to be independent of interface traps, and to be dependent only on the substrate dopant concentration.

IV. CONCLUSION

In summary, we have shown that the spread of the dC/dV characteristic is a sensitive monitor of the interface trap density. The study was based on samples with measured oxide thickness of 3.1 to 6.6 nm with relatively large values of oxide fixed charge. The extension of the SCM technique to high-quality, sub-2.0-nm-thick gate oxides is potentially

possible provided tunneling current effects can be minimized. For such high-quality thin oxides, the dC/dV peak is typically located at a probe tip-sample bias near to zero volts; hence, tunneling current effects are expected to be small with low applied biases during the dC/dV sweep.

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