Charge-based silicon quantum computer architectures using controlled single-ion implantation

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We report a nanofabrication, control and measurement scheme for *charge*-based silicon quantum computing which utilises a new technique of *controlled* single ion implantation. Each qubit consists of two phosphorus dopant atoms ∼50 nm apart, one of which is singly ionized. The lowest two energy states of the remaining electron form the logical states. Surface electrodes control the qubit using voltage pulses and dual single electron transistors operating near the quantum limit provide fast readout with spurious signal rejection. A low energy (keV) ion beam is used to implant the phosphorus atoms in high-purity Si. Single atom control during the implantation is achieved by monitoring on-chip detector electrodes, integrated within the device structure, while positional accuracy is provided by a nanomachined resist mask. We describe a construction process for implanted single atom and atom cluster devices with all components registered to better than 20 nm, together with electrical characterisation of the readout circuitry. We also discuss universal one- and two-qubit gate operations for this architecture, providing a possible path towards quantum computing in silicon.

I. INTRODUCTION

It is widely believed that solid-state systems have much to offer in the search for a scalable quantum computer (QC) technology. One of the most advanced proposals is based on superconducting qubits [1], where coherent control [2, 3, 4, 5, 6] and two-qubit coupling [7] have been demonstrated. Semiconductor schemes also show promise, in particular those based on silicon metal-oxide-semiconductor (Si MOS) technology, due to their compatibility with existing manufacturing. In Kane's scheme [8] (Fig. 1(a)) the qubits are defined by long-lived nuclear spin states of buried phosphorus dopants in a Si host crystal, and manipulated by external surface gates and radio-frequency (RF) magnetic fields. An alternative Si:P architecture has also been proposed using electron spin states as qubits [9]. While measurement of single nuclear and electron spins in the solid-state has very recently been reported for diamond [10], an electronic method of single spin readout in silicon remains a significant challenge.

Although detection of single spins in silicon has not been achieved, fast single *charge* detection is already in place due to recent developments in RF single-electron transistor (SET) technology [11, 12]. We have therefore proposed a Si:P charge qubit architecture [13] which is complementary to the Kane scheme, but experimentally accessible now. Charge based qubits in large lithographically-defined quantum dots have been proposed previously [14, 15]. In our system the quantum logic states correspond to the lowest two states of the single valence electron localised in the double well formed by two donor phosphorus atoms (see Fig. 1(b)).
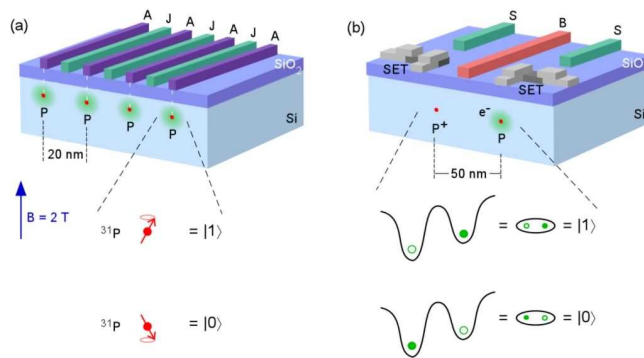

FIG. 1: Quantum computer architectures based on buried dopants in silicon. (a) Kane scheme [8], where a qubit is defined by the spin of a single ^{31}P nucleus. (b) Charge-based scheme [13], discussed here, where the position of a single electron within a double-well potential created by *two* P dopants defines logical states $|0\rangle$ and $|1\rangle$. Dual single electron transistors (SETs) on the surface enable qubit readout.

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Gates above the buried $P - P^+$ system allow for external control over the barrier height (B-gate) and potential symmetry (S-gates) for manipulation of localised qubit states, $|0\rangle = |L\rangle$ and $|1\rangle = |R\rangle$, while twin RF SETs facilitate qubit initialization and readout. A thin barrier layer such as SiO_2 is used to isolate the gates from the donors below. The charge qubit will decohere faster than its spin-based counterpart due to stronger environmental coupling, however, calculated [13] gate operation times of order 50 ps are commensurately faster than the μs operation times [16] for spin qubits. Although not spin-dependent, the electron transfer process in the $P - P^+$ qubit is similar to that in the $P - P$ system used for spin readout in the Kane scheme [8] and as such provides a test bed for the future development of spin-based qubits.

Operational issues aside, the spin- and charge-based Si:P schemes shown in Fig. 1 face an identical challenge – placement of individual phosphorus donors within a low-disorder intrinsic-silicon (i-Si) substrate at precise array sites, accurately positioned with respect to the surface control gates and SETs. Two contrasting approaches are being developed to attain this goal. In the first, scanned-probe lithography of a hydrogenated silicon surface together with epitaxial Si overgrowth may be used to construct a buried P array using a bottom-up atomic assembly approach [17, 18]. While potentially capable of atomic precision, a number of steps remain in the full demonstration of this technology.

Here we describe a second construction approach for which charge qubit test devices have been fabricated. Array sites are defined by top-down lithographic patterning of a resist mask and the donors are implanted through this using a keV phosphorus ion beam, with on-chip single ion detection. We have introduced the concept of single ion implantation in previous work on alternate device structures [19] and here show the first experimental demonstration of the technique for 14 keV phosphorus ions, as required for Si:P qubit construction.

The article is organised as follows. We first describe the process by which the implantation of P donors is controlled with single ion accuracy, allowing devices to be configured atom-by-atom. Ion-impact detectors, integrated into the devices, are monitored electrically during implantation. When a single ion enters the i-Si substrate it produces electron-hole pairs that drift in an applied electric field, creating a detectable current pulse for each ion strike. Although discussed here for construction of QC devices, this technology is applicable to any semiconductor device where accurate control of dopant number in the substrate is important. We then detail a complete fabrication process for the construction of test devices with donors implanted with precision beneath control gates and SETs and describe the use of cross-correlated RF twin-SET measurements which will be necessary for qubit readout. Finally, we outline a scheme for the operation of one- and two-qubit devices accessible using this technology.

II. CONTROLLED SINGLE-ION IMPLANTATION

Fig. 1(a) depicts the technique developed to localize individual phosphorus atoms at the desired qubit array sites. A nano-patterned ion-stopping resist such as polymethyl-methacrylate (PMMA) defines the array sites and a low-energy keV $^{31}P^+$ ion beam is used to implant the P dopants through the thin SiO_2 barrier layer to a mean depth of 20 nm into the substrate.
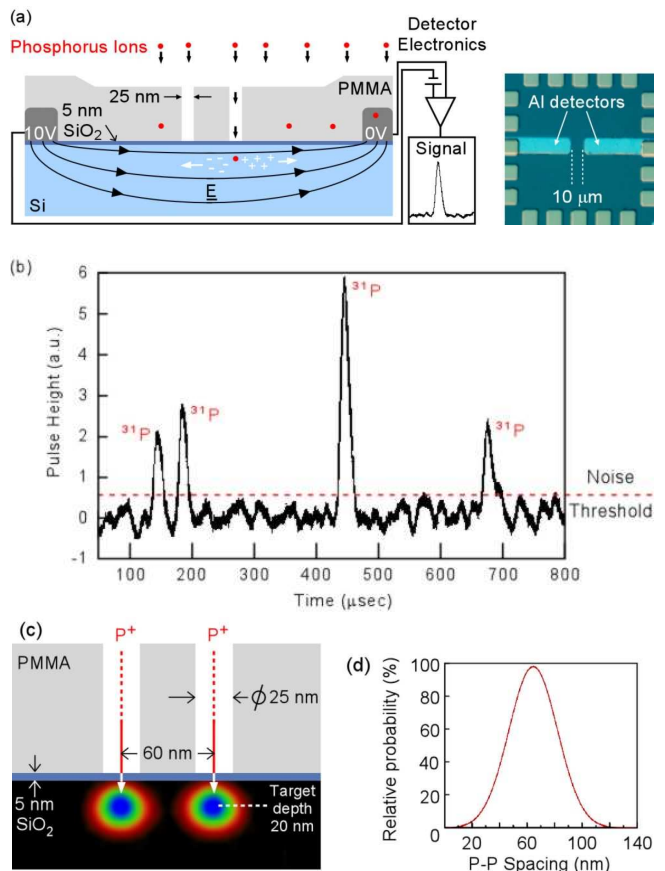

FIG. 2: (a) Schematic (not to scale) showing phosphorus implantation through a resist mask. Each ion strike creates an electron-hole plasma, producing a current pulse monitored by on-chip electrodes (shown in optical micrograph at right). (b) Experimental demonstration of single ion strikes in an i-Si substrate bombarded with a 14 keV phosphorus ion beam. (c) Calculated 14 keV P^+ implant position probability for two 25 nm apertures separated by 60 nm. (d) Resulting histogram of spacings between pairs of P^+ implants through the apertures.

Single ion impacts are detected by two surface aluminium detector electrodes, biased at up to 10 V, which form MOS tunnel junctions and act as back-to-back diodes, restricting the dark current (no $^{31}P^+$ beam) to below 100 pA. Each ion entering the substrate creates $\sim$500 e^-/h^+ pairs which drift in the internal electric field produced by the electrode bias. The e^-/h^+ pair gener-

ation and separation mechanism has been modelled [20] using the semiconductor modeling packages SRIM [21] and TCAD [22] and is found to create a current transient in 40 ps. The current is integrated in an external, high efficiency cooled preamplifier circuit to produce a single pulse for each ion strike. The substrate is also cooled to 115 K to reduce detector noise. Since the collection time is much less than the recombination time, close to 100% charge collection is possible. To measure the efficiency of the detectors, we have rastered a focused MeV ion beam across various electrode geometries and monitored the charge collection efficiency at each point [23], finding charge collection efficiencies of ∼99% at distances up to 10 μm from the electrodes. We have therefore been able to fabricate detector electrodes set back many microns from the central nanostructured region where the qubits and control gates are located (see image in Fig. 2(a)).

Data for an incident 14 keV ^{31}P$^+$ ion beam is shown in Fig. 2(b) for an interdigitated electrode array with lateral dimension ∼100 μm. Pulses above the noise threshold occur at a frequency consistent with the areal ion dose of ∼5 ions/ms across the active device area and can therefore be identified as single ion strikes, as confirmed by analysis of the pulse height distribution, discussed below. The temporal broadening of the peaks in Fig. 2(b) results from the time constant of the detection circuit.

While semiconductor detectors are well-established [24], to our knowledge this is the first use of a detector integrated into a device to control its doping level. Furthermore, the 14 keV data of Fig. 2(b) represents the first detection of implanted keV ^{31}P$^+$ ions, although light ions such as ^{1}H$^+$ and ^{4}He$^+$ have been previously measured in the range 15-30 keV using silicon detectors [25]. The low noise and high energy resolution of our detectors results from their low leakage current together with the very thin SiO$_2$ dead-layer, confirmed to be less than 7 nm from measurements using MeV ions [23].

Because of their mass, ^{31}P$^+$ ions with incident energy 14 keV lose ∼85% of their initial energy to nuclear stopping events in the substrate. The energy available for the creation of e$^-$/h$^+$ pairs is therefore ∼2 keV. Due to variations in ion trajectories the exact number of e$^-$/h$^+$ pairs and the resulting pulse height will vary between events, as observed experimentally in Fig. 2(b). Analysis of a large number of pulses shows a gaussian distribution of peak heights with a mean value consistent with the expected electronic energy loss, confirming each peak as a single ion impact event. To ensure that no ions enter the substrate without detection the noise level must be kept significantly below the mean pulse height. We have been able to reduce the effective noise level to an energy equivalent of ∼1 keV and expect that below 0.2 keV should be attainable, providing greater than 99% confidence that all implanted ions have been detected.

At present we are applying a uniform areal ion dose to our masked substrates, so that ion placement is random between the apertures. For the P − P$^+$ charge qubit device of Fig. 1(b) this leads to 50% probability of correctly configuring a device with one P atom at each site. Such a yield is sufficient for proof-of-principle experiments on one-qubit devices, however, for large-scale qubit arrays it will be necessary to direct each ion to its appropriate array site using a focused ion beam (FIB). We are currently developing this technology using a dual beam FIB/SEM with a 20 nm focus.

Because the path taken through the substrate by each implanted ion is different, there will be variation in the spatial configuration of each P − P$^+$ pair, which must be corrected for by appropriate calibration of the B- and S-gate voltages (defined above) for all qubits in the device. Since the qubit gate operation times are dependent on both the P − P donor spacing and the barrier gate voltage [13], the B-gate can be used to tune individual qubits over a wide range of spacings.

To estimate the spacings in our test devices we have used an implant modeling package [21] to calculate the expected ion straggle. For 14 keV ^{31}P$^+$ ions incident on a silicon substrate with a 5 nm SiO$_2$ gate oxide we find that the ions come to rest 20 nm below the free surface, with a standard deviation of 10 nm in the beam direction and 7 nm in the lateral direction. We have also modeled a typical implant profile for a device with two circular resist apertures of diameter 25 nm and a centre-to-centre spacing of 60 nm. Fig. 2(c) shows the calculated position probability contours, while Fig. 2(d) is the resulting relative probability of P − P donor spacings. Our calculations indicate that the magnitude of the detection pulse is related to the donor depth, meaning that devices with two similar pulses would be closer to optimum configuration and could then be selected for measurement.

At the mean distance of 60 nm we calculate [13] qubit rotation times of ∼200 ps using accessible B-gate voltages, becoming faster for smaller spacings. As seen in Fig. 2(d), for initial two-donor devices ∼40% of P − P pairs will be separated by less than 60 nm, giving functional qubits. We have fabricated resist apertures as small as 15 nm and expect that centre-to-centre spacings of 30 nm can be achieved. In such structures all pair spacings would be below 70 nm, providing a high yield of operational qubits for large scale systems.

III. FABRICATION OF TEST DEVICES

To evaluate the potential of charge qubits constructed via ion implantation we have fabricated test devices in which the two donors in Fig. 1(b) are replaced by implanted *clusters* of phosphorus donors, effectively creating two buried metallic islands. Fig. 3 shows devices incorporating two such clusters buried 20 nm below the surface, accurately aligned to control gates and dual readout SETs. We calculate that approximately 600 donors are required in each cluster to create a metallic density of states separated by a barrier, enabling periodic sequential tunneling *between* clusters upon application of a differential bias between the surface control gates. The
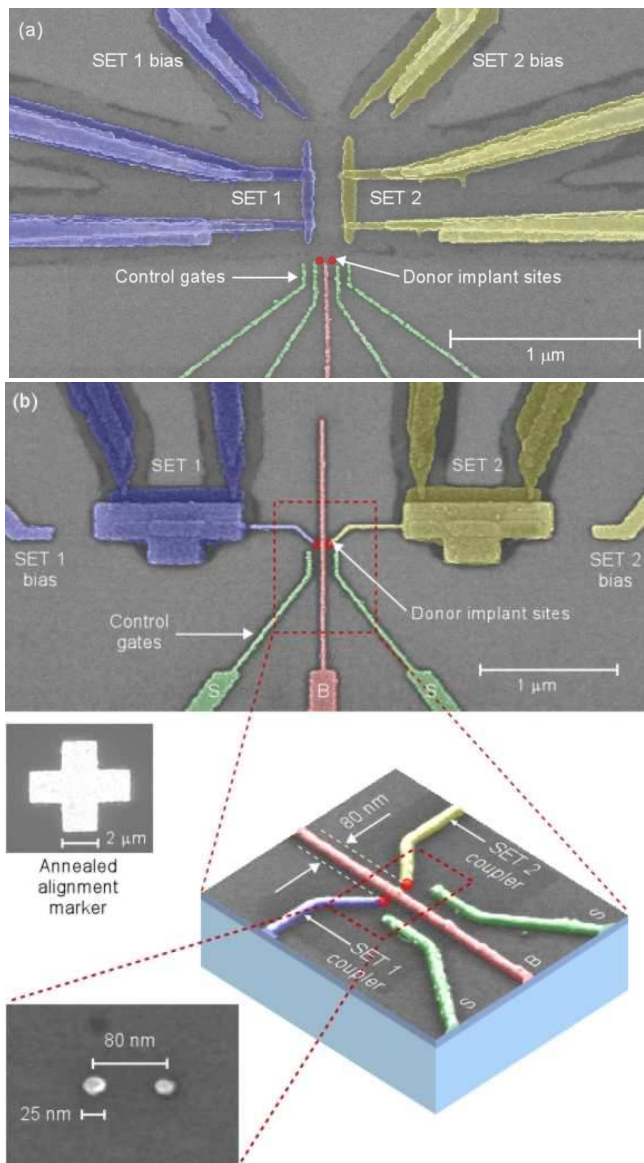
FIG. 3: SEM images of test devices incorporating buried phosphorus ion implants, shown *schematically* here by red markers. (a) Device with five control gates (bottom of image) to control electron motion between donors, together with two closely-spaced SETs to detect electron transfer. (b) Modified device, where each SET island has a coupling electrode to capacitively couple it to a phosphorus donor site. A long central barrier (B) gate may be used to control tunneling between donors. *Bottom left:* Demonstration, via metal lift-off, of 25 nm PMMA implantation apertures.

two read-out SETs may then be used to detect this periodic charge motion. The presence of a *periodic* output signal in test devices would provide an unequivocal demonstration of controlled electron transfer, while the large number of implanted donors minimises the detrimental effects of any traps in the i-Si substrate or at the Si/SiO$_2$ interface.

Fabrication of the devices in Fig. 3 involves a number of high-resolution electron beam lithography (EBL) steps, each of which must be aligned to the others with an accuracy of 20 nm or better, to ensure reliable gate control and sufficient capacitive coupling between the donors and read-out SETs. The process flow proceeds as follows. Firstly, a barrier between the control gates and donors is provided by a 5nm SiO$_2$ layer, thermally grown on a near-intrinsic silicon wafer with a background n-doping level of 10^{12}cm^{-3}.

If single ion implant control is required, micron-scale aluminium detector electrodes are then deposited on the substrate using UV lithography. The electrodes are separated from each other by 10 μm (see Fig. 2(a)), sufficiently close to ensure high-efficiency charge collection, but far enough apart to allow all nanocircuitry to be constructed between them. We note that for the fabrication of test devices with large numbers of P atoms, single ion counting was not required as the cluster size could be determined sufficiently accurately from the incident ion flux and resist-aperture diameter.

To provide sub-20 nm registration between all features on the device, EBL is then used to pattern a number of Ti/Pt alignment markers on the chip. In a second EBL step, two sub-30 nm apertures are opened in an ion-stopping PMMA resist, as depicted schematically in Fig. 2(a). Metallisation and lift-off results shown in the inset to Fig. 3(b) confirm the dimensions of these apertures.

Donor implantation proceeds next using a 14 keV P$^+$ ion beam. Modeling [21] indicates that these ions come to rest in the PMMA at a mean depth of 38 nm, with standard deviation 10 nm, so a layer thickness above 100 nm is sufficient to block phosphorus ions and avoid forward recoils of atoms constituting the resist. Phosphorus ions which pass through the apertures and enter the substrate come to rest at a mean depth of 20 nm below the free surface, as stated above.

Damage to the substrate caused by the implant process must next be removed via a thermal treatment. We employ a 950°C rapid thermal anneal (RTA) for 5 seconds, sufficient to activate the phosphorus donors [26] but limiting their diffusion to $\sim$1 nm based on standard bulk rates [27]. Pulsed laser annealing on ms timescales could also be used to further limit phosphorus diffusion and to localise the region of heating.

Following ion implantation and activation, the remaining nanocircuitry on the surface of the chip is completed using two further EBL steps. Firstly, Ti/Au control gates are deposited following EBL patterning of a single PMMA layer. We routinely fabricate gate widths of 20-30 nm using this process [28] and have also demonstrated continuous gates as narrow as 12 nm. Finally, the two Al/Al$_2$O$_3$ SETs are fabricated using a double-angle metallisation process and a bilayer resist [29]. As seen in Fig. 3(a), the overall alignment between all levels of this process is better than the width of a control gate ($\sim$20 nm).

IV. TWIN-SET READOUT AND ELECTRICAL CHARACTERISATION

The proposed charge qubit device of Fig. 1(b) employs *two* symmetric SETs to read out electron position within a single $P - P^+$ qubit. Whilst in principle a single SET would suffice, by cross-correlating the output from two SETs it is possible to reject spurious events resulting from random charge motion within the Si substrate, the SiO_2 barrier layer, or associated with the SETs themselves. Such *charge noise* rejection has been demonstrated [30] using an all-aluminium twin-SET architecture in which the phosphorus donors are simulated by two aluminium islands separated by a tunnel junction. In the device of Fig. 3(a) each SET is designed to capacitively couple most strongly to its nearest donor cluster. Preliminary measurements, however, indicated significant cross-coupling between SETs, making signal discrimination difficult, and it was necessary to reconfigure the device with the two SETs separated from each other by around 1 μm (Fig. 3(b)). Additional antenna electrodes are then used to couple each SET to its target donor or donor cluster, while a long central barrier (B) gate increases screening between SETs. In the following we focus on characterisation of the control and readout circuitry of this modified device with no implanted donors.

To read out the state of a charge qubit it will be necessary to perform a projective measurement with the two SETs on a timescale shorter than the qubit mixing time [12] t_{mix}, which we expect to be of order microseconds based on spontaneous emission results obtained for superconducting circuits [31]. Using radio-frequency (RF) SET technology [11, 12] we have developed a twin RF-SET measurement system [32] and used it to demonstrate cross-correlated single-shot measurements of controlled charge motion within all-aluminium devices on sub-microsecond timescales [33]. The time τ_{meas} required to perform single-shot measurements of electron position on buried donor devices will depend on the capacitive coupling between the donor electrons and SETs [30, 33]. Estimates of this coupling [34] indicate that $\tau_{meas} \sim 1$ μs can be achieved, making qubit readout possible.

When applied to the device of Fig. 3(b) this RF measurement system enables independent operation of the two SETs on microsecond timescales. Fig. 4(a) shows typical Coulomb blockade oscillations in the d.c. source-drain conductance of SET 1 on a control device with no implants as a function of S-gate bias, while Fig. 4(b) shows the reflected RF power as a function of frequency under two different bias conditions. The red trace corresponds to the situation when *both* SETs are biased to a conductance peak, while the black trace corresponds to both SETs at conductance minima. SET 1 is impedance-matched to a 50 Ω transmission line at 322 MHz while SET 2 is matched at 357 MHz. By supplying and monitoring two independent RF carrier signals we then use wavelength division multiplexing [32] to independently monitor each SET, providing nanosecond time resolution
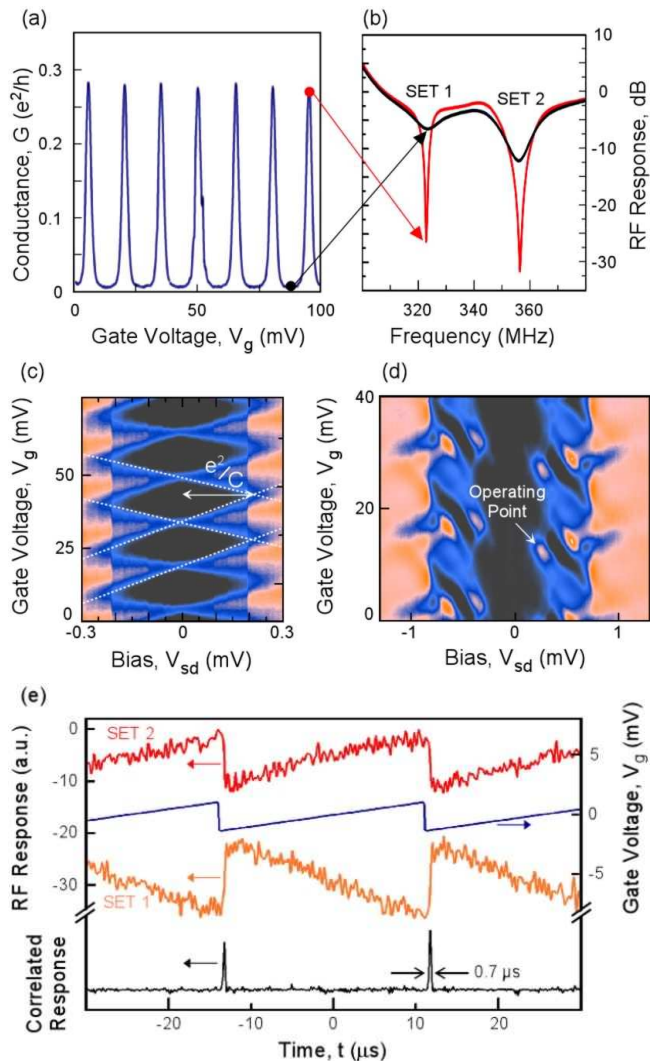

FIG. 4: (a) Coulomb blockade oscillations in SET conductance on a control device as in Fig. 3(b), but with no phosphorus implants. (b) Reflected RF power as a function of frequency on a similar device when the two SETs are biased at conductance maxima (red) and minima (black). (c, d) RF bias spectroscopy of SET 2 on a control device in the normal state (c), and the superconducting state (d), measured using a carrier frequency of 357 MHz. Each plot contains 250,000 data points, accumulated at a rate of 0.3 ms per datum. (e) Reflected RF power for two SETs on a device with a modified gate arrangement, together with their cross-correlated output (black), showing sub-μs response to a sawtooth potential (blue) applied to a control gate to simulate charge transfer.

for fast read-out.

The devices are further characterised using bias spectroscopy measurements in which a d.c. source-drain voltage V_{sd} is applied to an SET and its response monitored. Fig. 4 shows bias spectroscopy for a control device SET, operated at radio frequencies in the normal ($B = 2$T) and superconducting ($B = 0$) states, respectively. In the normal state (Fig. 4(c)) we see a characteristic "Coulomb diamond" spectrum, from which a charging energy of e^2/C

= 0.2 meV may be obtained. In the superconducting state (Fig. 4(d)) the data is more complex and exhibits features due to resonant Josephson effects [35].

From measurements on all-aluminium devices [32] we find that optimal sensitivity to charge motion is obtained by operating the two SETs in the superconducting state and biasing each to a Josephson quasiparticle peak, as shown in Fig. 4(d). In this way we have attained sensitivities with twin SETs of 4.4 $\mu e/\sqrt{Hz}$ and 7.5 $\mu e/\sqrt{Hz}$ respectively [32], close to the quantum limited sensitivity [36]. Fig. 4(e) shows RF data obtained on an all-aluminium device when a control gate is ramped with a sawtooth potential to *simulate* periodic charge transfer. The gate voltage amplitude corresponds to an induced charge of $\sim 0.1e$ on each SET island. In addition to the *single-shot* (non-averaged) RF output from each SET, Fig. 4(e) shows the cross-correlated signal obtained by simply multiplying the time derivatives of the two outputs. Much of the noise detected by the individual SETs is rejected by the correlation and the combined system shows a response time below 1 μs, as required for charge qubit readout.

V. CHARGE QUBIT OPERATION AND COUPLING

We now discuss possible one- and two-qubit operations which will be accessible using the devices shown in Fig. 3(b) when configured with just two activated phosphorus donors. There exist two choices for the basis of logical qubit states corresponding to the lowest two states being localised or de-localised. Since SET readout is most easily carried out for localised states, we focus here on the configuration with non-zero S-gate biases ($V_S \neq 0$ in Fig. 5(a)), which serves to localize the electron into the qubit states $|0\rangle = |L\rangle$ and $|1\rangle = |R\rangle$. Calculations [13] show that for equal and opposite applied voltages on the S-gates of order 0.1 V the fidelity of qubit definition is optimal, with mixing of higher states less than 10^{-4}. We discuss later the alternative delocalised basis choice $|0\rangle = (|L\rangle + |R\rangle)/\sqrt{2}$ and $|1\rangle = (|L\rangle - |R\rangle)/\sqrt{2}$ in the context of reducing the effects of decoherence.

To perform a single qubit $\pi/2$ rotation in the localized basis the S-gate biases are adjusted to zero, to symmetrize the potential, and the B-gate bias made negative to raise the barrier and slow the coherent oscillations ($V_S = 0$ in Fig. 5(a)). Typically, such operations will require gate bias precision down to the mV level. The time for a $\pi/2$ rotation will depend primarily on the donor spacing and chosen B-gate bias. For a typical bias $V_B \sim 0.5$ V we calculate [13] rotation times longer than 50 ps, which are accessible using fast pulse generation technology.

Before the qubit is operational it must be pre-initialised after fabrication to remove one of the electrons from the P − P system. The pre-initialisation process is carried out using the S and B gates: the electron in the right-hand donor well is ionized to the continuum by a
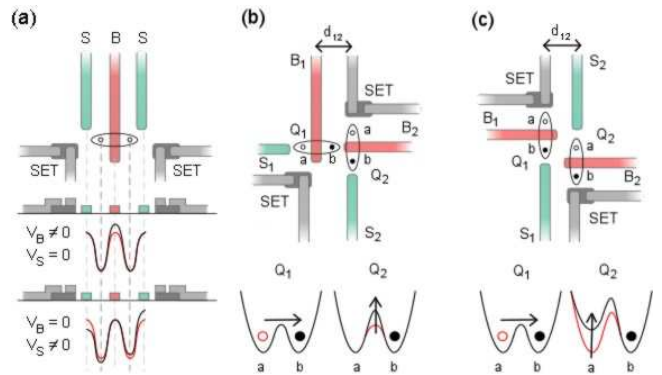

FIG. 5: (a) Operation of a single charge-qubit showing barrier (B-gate) and symmetry (S-gates) control, with twin-SET for correlated charge-position readout. (b, c) Qubit coupling schemes based on the Coulomb interaction. (b) "CNOT" configuration, where the control qubit Q_1 alters the effective barrier height as seen by the target qubit Q_2. (c) "CPHASE" configuration, where the control qubit Q_1 alters the potential symmetry at the target qubit Q_2.

negative bias $\sim$-0.4V on the right-hand S-gate [13], while the electron in the left donor well is partially screened by grounding the B-gate and left-hand S-gate. Once the qubit has been pre-initialised, the two SET outputs can be calibrated for the $|L\rangle$ and $|R\rangle$ states. Thereafter, initialisation of the charge qubit into the ground state $|0\rangle = |L\rangle$ is effected by simply biasing the S-gates and observing the SET outputs.

In the SET readout process we wish to make a projective measurement of a general state $|\Psi\rangle = c_0|0\rangle + c_1|1\rangle$, resulting from a sequence of gate operations with the SETs blockaded so that no current flows [35, 36]. As a result of measurement we obtain $|0\rangle$ or $|1\rangle$ with probabilities $|c_0|^2$ and $|c_1|^2$ respectively. When voltages are applied to the SET bias gates (see Fig. 3(b)) tuning each SET to a conductance peak, the current flow through the device decoheres the charge qubit strongly, causing a rapid transition to a statistical mixture of the localised eigenstates. The SETs will then give distinguishable output signals, determined during calibration, corresponding to the system having collapsed into the left or right state.

Two possible qubit coupling schemes are shown in Figs. 5(b) and 5(c), leading to different coupling dynamics. For simplicity we have included only one SET readout device per qubit in the schematics. In the first "CNOT" arrangement, the horizontal qubit Q_1 acts on the effective barrier height of the vertical qubit Q_2, and the coupling is primarily $\Gamma_{zx}\sigma_z^{(1)}\sigma_x^{(2)}$. In the second "CPHASE" arrangement the effective coupling is $\Gamma_{zz}\sigma_z^{(1)}\sigma_z^{(2)}$. Precise determination of the coupled qubit dynamics in the presence of the full gate structure is beyond the scope of this paper, however, we have performed a semi-classical calculation to obtain an order of magnitude estimate. We calculate the effect on Q_2 of moving a charge of 1.0 e between the a and b positions of Q_1 (see Fig. 5(b)) with

a and b chosen to be 60 nm and 30 nm respectively from Q_2, and obtain $\Gamma \approx 10^{-4} - 10^{-5}$ meV corresponding to coupled qubit operation times of 0.1 - 1 ns.

VI. DISCUSSION

Given a capability to implant controlled numbers of donors into silicon devices with nanoscale gates there do not appear to be any fundamental limits posed by fabrication technologies for scale-up of this architecture to many qubits. For example, long linear arrays of charge qubits can be envisaged [13] with "CPHASE" coupling as in Fig. 5(c). Such devices would require a focused phosphorus ion beam combined with an EBL-defined resist aperture mask to position each dopant at the appropriate array site in a step-and-repeat process.

Some device-related issues still require further experimental work before Si:P qubit operation can be demonstrated. For example, it will be necessary to minimise defects at the Si/SiO_2 interface which could trap the sole electron in the qubit. Interface trap densities below $10^9 cm^{-2}$ have been reported [37] that correspond to trap spacings in excess of 300 nm, sufficient for qubit operation, however, such interfaces require high levels of purity during oxide growth. Also, to ensure that only the intended phosphorus ions enter the device during implantation, the detector dark currents must be further reduced. We are currently incorporating p- and n-doped wells below the detector electrodes to create a p-i-n structure for this purpose.

The key factor determining the limit to scale-up will be decoherence of the qubits due to environmental coupling. Successful operation of quantum devices is contingent on coherence times remaining longer than the time required for arbitrary rotations. The primary sources of decoherence for the charge qubit are expected to include phonons, Johnson noise from the gates and charge noise from the material environment. A recent calculation of LA phonon induced decoherence on the $P - P^+$ system [38] concluded that for donor separations of 25 nm and greater, τ_{phonon} is of order μs, well above the gate operation times. Similarly, Johnson noise due to fluctuations on the S and B gates is also calculated [13, 39] to give decoherence on timescales ~ 1 μs.

The $1/f$ noise resulting from charge fluctuations in the surrounding environment is believed to be the limiting factor for all charge-based qubits [40]. In particular, individual charge traps can produce sudden and large changes in the noise signal at random times (random telegraph signals). Ensemble coherence times of $\tau_2^* \sim 1$ ns have been observed in GaAs quantum dots [41] suggesting a lower bound for the single particle coherence time of $\tau_2 > 1$ ns. In comparison with the buried Si:P charge qubit, these lithographically-defined GaAs devices were quite large - approximately 0.02 μm^2 in area with around 25 electrons per dot. We therefore expect the quantum coherence time for the Si:P charge qubit to be long enough to allow coherent control of devices such as in Fig. 3.

The use of high quality materials with low trap densities should also extend the coherence time, while refocusing pulse techniques can minimise the effects of decoherence [42]. Furthermore, τ_2 may be increased by defining the logical states in terms of de-localised symmetric and anti-symmetric wavefunctions. Since the delocalised states have a very similar charge distribution they will be less vulnerable to environmental charge fluctuations [5], although charge readout will be more difficult in this case.

Prior to coherent gate operations two key experiments will be undertaken. Controlled tunneling between clusters of phosphorus donors must first be demonstrated with SET readout to ascertain the signal level corresponding to single electron transfer. Microwave spectroscopy [31] on a $P - P^+$ device may then be used to map out the qubit energy levels and determine τ_1 and τ_2^* for the system.

In summary, a top-down process for constructing small-scale Si:P quantum computer devices has been developed that is capable of accurately locating single phosphorus atoms in an i-Si substrate below custom-configured control gates and SET readout devices. Ion detection electrodes, integrated into the device structure, make this single atom doping possible and open the way for a new class of implanted devices at the single donor level. We have outlined a scheme for operation of these Si:P devices as charge qubits, including coupling architectures suitable for scalable computing, and have discussed in detail the operation of twin RF SETs for state readout with charge noise rejection. With these fabrication and measurement technologies in place, a path is open for the realisation of quantum gate operations in silicon.

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