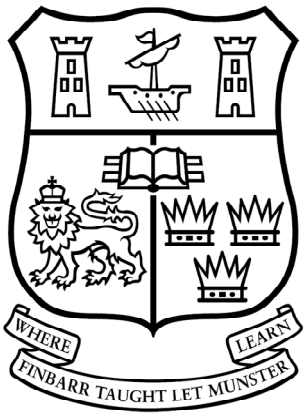

Modelling and Digital Control of Two-Phase Interleaved Coupled-Inductor Non-Isolated DC-DC Converters

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A thesis presented to the National University of Ireland for the degree of Doctor of Philosophy

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DECLARATION

I hereby declare that I am the sole author of this thesis and all of the work undertaken in this thesis is original in content and was carried out by the author. Work carried out by others has been duly acknowledged in this thesis.

This is a true copy of the thesis, including any required final revisions, as accepted by my examiners. The work presented has not been accepted in any other previous application for a degree.

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ABSTRACT

This thesis focuses on the complete mathematical modelling and digital closed-loop control of two-phase interleaved coupled-inductor non-isolated dc-dc converters. Coupled-inductors have been shown to reduce the cost, size, and weight of high-power magnetic components while increasing efficiency.

The complete large-signal model of the coupled-inductor boost converter is presented and compared to the traditional single-phase and two-phase discrete inductor dc-dc converters. The CCM-DCM mode maps are presented and discussed for the coupled-inductor boost converter. Sample analyses of several different CCM and DCM modes of operation are also presented. The different CCM and DCM waveforms are experimentally produced by a 1 kW laboratory prototype.

Following on from the large-signal model, the complete small-signal model of the coupled-inductor boost converter is presented. The method of solving for the small-signal models is discussed, and sample analyses of several different CCM and DCM modes of operation are presented. Calculated and experimental frequency sweeps for several of the CCM and DCM modes of operation are produced and compared to verify the accuracy of the small-signal models.

Controllers for the 1 kW prototype are designed from the transfer functions derived from the small-signal models. The control strategy of average-current-mode control is digitally implemented, which uses an outer voltage loop and an inner current loop to eliminate any error between the output and the desired output. The FPGA used in testing is the Altera Cyclone III FPGA. Initially, PI controllers are developed and compared to simulated results.

In order to improve the closed-loop performance of the converter, the inner current loop PI controllers are replaced with Type II compensators. Several compensators are designed as examples for a number of CCM and DCM modes of operation. Finally, to increase the stability of the converter, bumpless PI control and forced-output control utilizing the Type II compensators are introduced and implemented.

Additional analyses and results are presented in the appendix.

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LIST OF PUBLICATIONS

Journal Papers

1. B. C. Barry, J. G. Hayes, and M. S. Ryłko, "CCM and DCM operation of the interleaved two-phase boost converter with discrete and coupled-inductors," *IEEE Transactions on Power Electronics*, vol. 30, no. 12, pp. 6551-6567, December 2014.
2. K. J. Hartnett, J. G. Hayes, M. S. Ryłko, B. C. Barry, and Jerzy W. Masłoń, "Comparison of 8 kW CCTT IM and discrete inductor interleaved boost converter for renewable energy applications," *IEEE Transactions on Industry Applications*, vol. 51, no. 3, pp. 2455-2469, December 2014.

Conference Papers

1. B. C. Barry, J. G. Hayes, M. G. Egan, M. S. Ryłko, Jerzy W. Masłoń, and K. J. Hartnett "CCM and DCM operation of the integrated-magnetic interleaved two-phase boost converter," *29th Annual IEEE Applied Power electronics Conference and Exposition*, Fort Worth, Texas, March 2014.
2. B. C. Barry, J. G. Hayes, M. S. Ryłko, Jerzy W. Masłoń, and K. J. Hartnett, "Two-phase interleaved boost converters for distributed generation," *IEEE 5th International Symposium on Power Electronics for Distributed Generation*, Galway, Ireland, June 2014.
3. B. C. Barry, J. G. Hayes, M. S. Ryłko, and Jerzy W. Masłoń, "Discontinuous conduction mode operation of the two-phase integrated-magnetic boost converter," *IEEE Energy Conversion Congress and Exposition, Pittsburgh, Pennsylvania*, September 2014.
4. B. C. Barry, J. G. Hayes, M. S. Ryłko, R. Stala, A. Penczek, A. Mondzik, and R. T. Ryan, "Small-signal model and control of the interleaved two-phase coupled-inductor boost converter," *IEEE Energy Conversion Congress and Exposition*, Milwaukee, Wisconsin, September 2016.

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NOMENCLATURE

dc	direct current
ac	alternating current
CCM	Continuous conduction mode
DCM	Discontinuous conduction mode
BCM	Boundary conduction mode
1L	Single-phase converter
2L	Two-phase converter
CL	Coupled-inductor converter
RMS	Root-mean-square
PV	Photovoltaic
EV	Electric vehicle
HEV	Hybrid electric vehicle
FCEV	Fuel-cell electric vehicle
SiC	Silicon Carbide
GaN	Gallium Nitride
PFC	Power factor correction
THD	Total harmonic distortion
MPPT	Maximum-power-point tracking
PCU	Power control unit
SWIM	Split winding integrated magnetic
FPGA	Field-programmable gate array
OC	Open-circuit
RB IGBT	Reverse blocking IGBT
PWM	Pulse-width modulation
ACMC	Average-current-mode control
PCMC	Peak-current-mode control
VMC	Voltage-mode control
ADC	Analogue-to-digital converter
PID	Proportional-integral-derivative
ZVS	Zero-voltage switching

RHP Zero ..... Right half plane zero

ESR ..... Equivalent series resistance

G_m ..... Gain margin

P_m ..... Phase margin

PLC ..... Phase lead/lag compensator

FOC ..... Forced-output control

NEDC ..... New European driving cycle

EMI ..... Electromagnetic interference

CM ..... Common mode

V_{in} ..... Input voltage

V_{out} ..... Output voltage

$V_{Llkx.y}$ ..... Leakage inductance voltage drop over cycle time x in phase y

$V_{Tx.y}$ ..... Magnetizing inductance voltage drop over cycle time x in phase y

$I_{in(DC)}$ ..... dc input current

I_{Lx} ..... Inductor current of phase x

$I_{L(DC)}$ ..... dc inductor current

$I_{L(RMS)}$ ..... Inductor RMS current

I_o ..... dc output current

I_{S1} ..... dc switch current

I_{D1} ..... dc diode current

I_{oB} ..... Output current when converter is in BCM

$I_{oB,max}$ ..... Maximum output current when converter is in BCM

$\Delta I_{L(p-p)}$ ..... Peak-to-peak inductor current

$\Delta I_{m(p-p)}$ ..... Peak-to-peak magnetizing current

$\Delta I_{in(p-p)}$ ..... Peak-to-peak input current

I_{LxB} ..... Phase current of phase x when converter is in BCM

T_s ..... PWM switching cycle time

f_s ..... PWM switching frequency

L ..... Phase inductance

L_x ..... Phase inductance of phase x

L_{Lk} ..... Leakage inductance

L_m ..... Magnetizing inductance

R_{out} ..... Output resistance

C_{out} ..... Output capacitance

C_{in} ..... Input capacitance

P_{in} ..... Input power

P_{out} ..... Output power

η ..... Efficiency

D ..... Duty cycle

D_{off} ..... Diode conduction time

D_x ..... Cycle time x

Q_x ..... Semiconductor switch in phase x

V_{Qx} ..... Pole voltage across the semiconductor switch of phase x

V_{LV} ..... Low-side voltage

V_{HV} ..... High-side voltage

C_{LV} ..... Low-side capacitance

C_{HV} ..... High-side capacitance

$G_{vv}(s)$ ..... Input voltage-to-output voltage transfer function

$G_{vd}(s)$ ..... Duty cycle-to-output voltage transfer function

$G_{vi}(s)$ ..... Inductor current-to-output voltage transfer function

$G_{di}(s)$ ..... Duty cycle-to-output voltage transfer function

$G(s)$ ..... Plant transfer function

$C(s)$ ..... Controller transfer function

$H(s)$ ..... Sensor transfer function

f_c ..... crossover frequency

φ_m ..... Phase margin

φ_{boost} ..... Desired phase injection

N ..... Ratio of leakage inductance to magnetizing inductance

K_p ..... Proportional gain

K_i ..... Integral gain

K_d ..... Derivative gain

K_c ..... Type-II compensator gain

ω_p ..... Frequency of pole

ω_z ..... Frequency of zero

T_{Ds} ..... Discrete sampling time

1 INTRODUCTION

This chapter presents an overview of the research topics discussed in this thesis. The body of work presented is focused on the implementation, mathematical modelling and control of non-isolated multi-phase dc-dc converters utilizing coupled inductors. The applications of dc-dc converters range from the high-power, high-current automotive and renewable sectors, to the low-power, low-current consumer electronics sector, such as laptop and mobile phone chargers. This chapter presents the current technology used in such applications, as well as the motivation for the development and implementation of high-efficiency, low-box-volume magnetic components.

1.1 Overview

The year 2015 is on record for being, on average, the warmest year since official records began in 1880 [1.1]. Figure 1.1 presents the average global temperature difference per year for over the last 100 years [1.2].

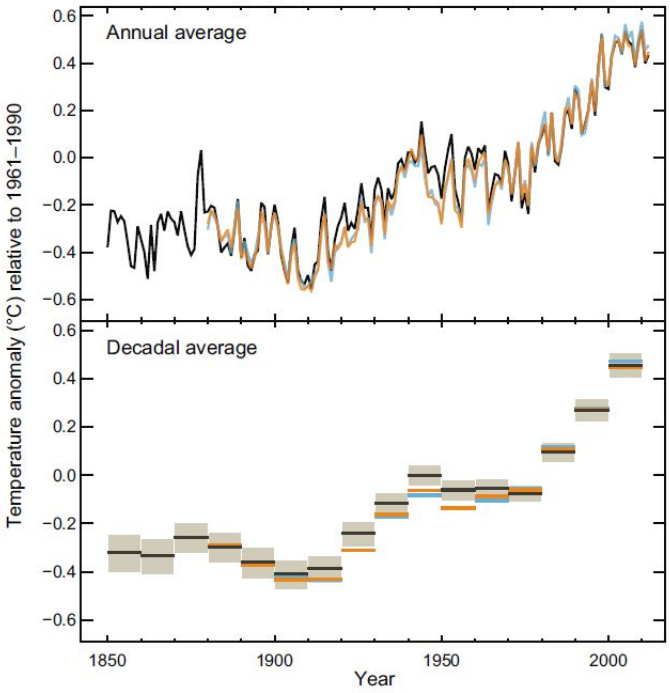


Figure 1.1. Observed globally averaged combined land and ocean surface temperature anomaly 1850-2012 [1.2].

As can be seen from Figure 1.1, the global temperature has risen by approximately 1°C in the last 100 years. A growing worry among the scientific community is that this temperature rise may be man-made, due to the high levels of greenhouse gases such as carbon dioxide being produced every day. Another worrying trend in today's economy is the volatility of oil prices, as well as the threat of oil and gas shortages. The current estimation of oil reserves left globally is approximated at 1,500 billion barrels, much of which are located in countries with volatile political and social environments [1.3].

Hence, in recent years there has been a growing push into the area of clean and renewable energy. In 2014, it was estimated that 19% of the world's energy consumption was supplied via renewable energy sources, 9% of which is coming from traditional biomass, while the remaining 10% coming from modern renewable energy sources such as wind turbines, hydroelectric dams, and photovoltaic (PV) cells [1.4]. Global leaders such as the United States and China are beginning to invest heavily in the renewable energy sector while in Europe, Germany is spearheading a PV initiative in an attempt to completely phase out nuclear power from the country. Smaller countries are also beginning to take part in this energy revolution. For example, in 2015,

24% of both the Republic of Ireland's and Northern Ireland's energy demands were met with wind power, supplied by a total of 235 wind farms on the island [1.5].

Another global initiative which is gaining traction in recent years is the introduction of environmentally-friendly vehicles. A large portion of the greenhouse gases produced globally comes from the transportation sector, with an estimated 26% of emissions coming from transportation in 2014 [1.6]. In an effort to cut down on these emissions, Electric Vehicles (EV), Hybrid Electric Vehicles (HEV), and Fuel-Cell Electric Vehicles (FCEV) are quickly becoming more favourable than internal combustion engine vehicles. Companies such as Tesla, Nissan, GM, and Ford have realised the market potential for such technology, and are spearheading this transportation revolution.

A key part of HEVs and FCEVs is the power converter. Various types of power converter topologies are found in many areas of this industry. For example, a high-power boost converter is essential in a fuel-cell vehicle to buffer the poorly-regulated output voltage of the PEM fuel-cell, and efficiently distribute this voltage to the traction-motor inverters [1.7]-[1.10]. Similarly, the THS II HEV power-train, developed by the Toyota Motor Company, features a high-power single-phase dc-dc converter to interface the battery pack to the high-voltage dc link [1.11]-[1.12]. In regards to renewable energies, dc-dc converters are essential in PV systems for stabilization of the dc-link voltage as well as for Maximum-Power-Point Tracking (MPPT) [1.13]-[1.16]. Power converters are also critical components of ac and dc microgrids [1.17]. The utilization of power converters in microgrids can contribute to grid stability, as well as improved efficiency when importing from the national grid to on-site microgrids.

For renewable and automotive applications, the single-phase buck or boost converter is the most commonly used converter. With the ever growing demand for higher power, designers are now looking at multi-phase converters, so as to reduce size, cost, and power losses. The downside to this approach is the addition of more magnetic components into the system; more specifically inductors. In addition, the recent advancements in wide-band-gap materials such as the Silicon-Carbide (SiC) and Gallium-Nitride (GaN) greatly reduce switching losses in semiconductor devices. This allows power converters to operate at a much higher frequency and power-density [1.18].

For these reasons, developers are now looking into decreasing the size and weight of the magnetic components, while increasing the power density. A common solution to this is the use of coupled-inductors and integrated-magnetics. In interleaving

applications, coupled-inductors have been shown to reduce the size and weight of the magnetic components when compared to their discrete inductor counterparts, without forfeiting efficiency [1.19].

The objective of this chapter is to give a brief introduction to the layout, motivation and current technology used in today's power converters. Section 1.1 gives a brief overview of the motivation for this body of work, while Section 1.2 presents the objectives of the thesis. Section 1.3 gives a brief summary of each chapter, while Section 1.4 discusses the applications and current technology of power converters. Finally, Section 1.5 gives a brief overview of the dc-dc converters analysed in this thesis, as well as the coupled-inductor used in experimental testing.

1.2 Thesis Objectives

The objective of this thesis is the complete mathematical modelling and digital control of the two-phase interleaved coupled-inductor dc-dc converter.

The first objective is to derive the large-signal characteristics of the converter. Due to the nature of a coupled-inductor converter, many of the current waveforms in both Continuous-Conduction Mode (CCM) and Discontinuous-Conduction Mode (DCM) are vastly different to a discrete-inductor converter. This, in turn, causes the converter characteristics to differ greatly, especially in DCM. These characteristics are fully derived for all CCM and DCM modes of the coupled-inductor boost and buck converters.

The second objective is to derive the small-signal model of each CCM and DCM mode of operation. In dc-dc converters, controllers, either analogue or digital, decide the duty cycle so as to ensure that the output voltage on the dc link is at a suitable level. One of the most efficient ways to design such controllers is to first find the transfer functions of the system, and to begin controller design at this starting point. As with the large-signal model, the small-signal models of the coupled-inductor converter differ greatly from the discrete-inductor converter. These models are fully derived for the coupled-inductor boost and buck converters.

The final objective is the complete closed-loop control of the coupled-inductor boost converter. There are several methods of control in power converters. Many ac-dc and dc-dc converters implement voltage-mode control, average-current-mode control, peak-current-mode control and hysteretic control. Due to the number of modes available in a coupled-inductor converter, a control method is implemented for each mode, with the ability to determine which mode the converter is operating in, and determining which controller to use.

Experimental results of each of these objectives are provided.

1.3 Thesis Structure

This thesis is split into five chapters. Chapter 1 gives a brief overview of the motivation and objectives of the research undertaken. The various areas in which power converters are used are discussed. The current technology utilized in today's power electronics industry is investigated, as well as the components.

Chapter 2 presents an investigation of the various continuous-current (CCM) and discontinuous-current (DCM) modes of operation of the coupled-inductor interleaved two-phase boost converter. The various CCM and DCM modes of the converter are identified together with their sub-modes of operation. The standard discrete-inductor interleaved two-phase boost can be seen as a subset of the coupled-inductor converter family with zero mutual coupling between the phases. The steady-state operating characteristics, equations and waveforms for the many CCM and DCM modes will be presented for the converter family. Mode maps will be developed to map the converter operation across the modes over the operating range. Experimental validation is presented from a 1 kW laboratory prototype. Design considerations and experimental results are presented for a 72 kW prototype.

Chapter 3 presents the small-signal analysis of a coupled-inductor boost converter operating in both CCM and DCM. Due to the complexity of operation of a coupled-inductor boost converter operating in DCM, several small-signal models must be derived. Experimental validation of the small-signal models are presented from the 1 kW coupled-inductor boost converter laboratory prototype.

Chapter 4 presents the development of PI controllers used in an Average-Current Mode control scheme, to stabilise the output voltage of the coupled-inductor boost converter. For highest efficiency and disturbance rejection, fast acting closed-loop control is necessary. Simulations are used to identify the best type of controller, which is then developed and implemented into the 1 kW prototype converter via FPGA. Experimental validation of these controllers is then presented.

Chapter 5 presents the design and implementation of Type II compensators, which replace the inner current loop PI controllers. The advantages and disadvantages of Type II compensators are discussed. Finally, the concept of bumpless control with PI controllers and Forced-Output control for Type II compensators are introduced, so as to improve the performance of the converter.

Chapter 6 presents the conclusions of the research and details possible future work in this area of research.

1.4 Power converters: A General Background

Dc-dc converters are used in a wide range of applications, including gate drivers, consumer electronics, energy storage, and renewable energy and automotive systems. This section will discuss related applications.

1.4.1 Semiconductor Gate Drivers

Low power dc-dc converters are often needed to step up the supply rail of semiconductor gate drivers to reach a voltage which will effectively switch on the semiconductor, as shown in Figure 1.2. These converters are often open-loop controlled, and so need a regulated supply to ensure the correct output is given.

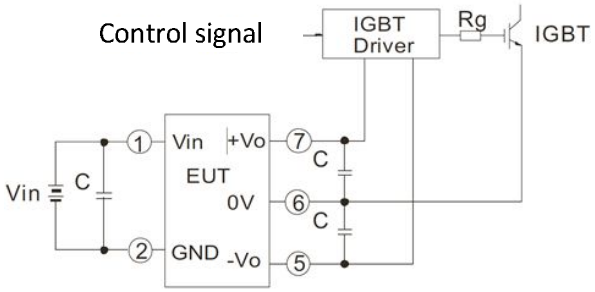


Figure 1.2. IGBT gate driver circuit featuring a dc-dc converter [1.20].

1.4.2 Consumer Electronics

Some higher power examples are laptop battery-charger power supplies, which use an ac-dc converter to rectify the ac input and provide a regulated dc output, usually at 12V-15V. Likewise, boost converters are often used in Power-Factor Correction (PFC) to reduce the Total Harmonic Distortion (THD) that is inherent to systems which utilize rectifiers. A PFC boost rectifier, presented in Figure 1.3, changes the duty cycle in such a way that it forces the input current to be in phase with the input voltage, while still giving a regulated dc output. Such PFC circuits are essential in ac-dc systems where the quality of the supply must be maintained.

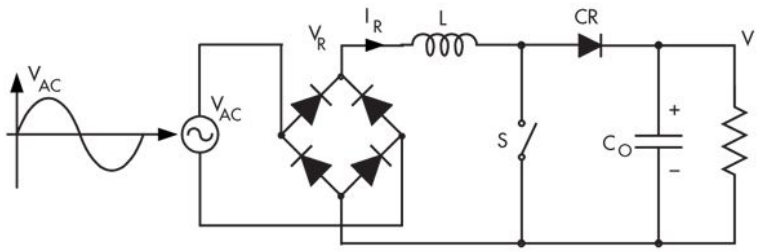


Figure 1.3. Power-factor correction boost converter [1.54].

1.4.3 AC Source Renewable Energy Systems

The most common renewable energy sources are wind, solar, hydroelectricity, and geothermal. Hydroelectricity alone is estimated to provide nearly 4% of the world's

electrical energy consumption [1.4], while sources like wind, solar, and geothermal power add a further 1.4%.

Wind and hydroelectric turbines extract the kinetic energy from their respective media for transformation into electrical energy via rotational generators. Geothermal sources extract heat from the earth's core, which is used to create high-pressure steam to turn a steam generator. Due to the nature of these systems, i.e. differing wind speeds, the output power of the generator is often unusable if extracted directly. Hence, power converters are utilized to manipulate the output power into a more practical form. A review of power electronics in renewable energy systems is discussed in detail in [1.21]-[1.27].

When exporting power to the grid, wind and hydroelectric turbines must ensure that the quality of the exported power meets grid standards. For example, the Danish national grid authority ELTRA provides specifications on voltage, frequency and reactive power that grid-connected wind turbines must meet [1.28]. One method of ensuring good quality power is the use of a variable-speed wind energy supply system, presented in Figure 1.4. In a variable-speed system, the output of the wind turbine is rectified into dc, and a dc-dc converter is used to regulate the dc-link voltage. At this point, the power may be supplied to an energy-storage system, or inverted into either single-phase or three-phase ac, to power a three-phase load or to be exported to the grid. The method presented in Figure 1.4 is most often used at low power. At higher power, the components of the rectifier, converter and inverter become increasingly expensive, and the system becomes uneconomical. One solution to this is the use of Doubly-Fed-Induction-Generators (DFIG), presented in Figure 1.5.

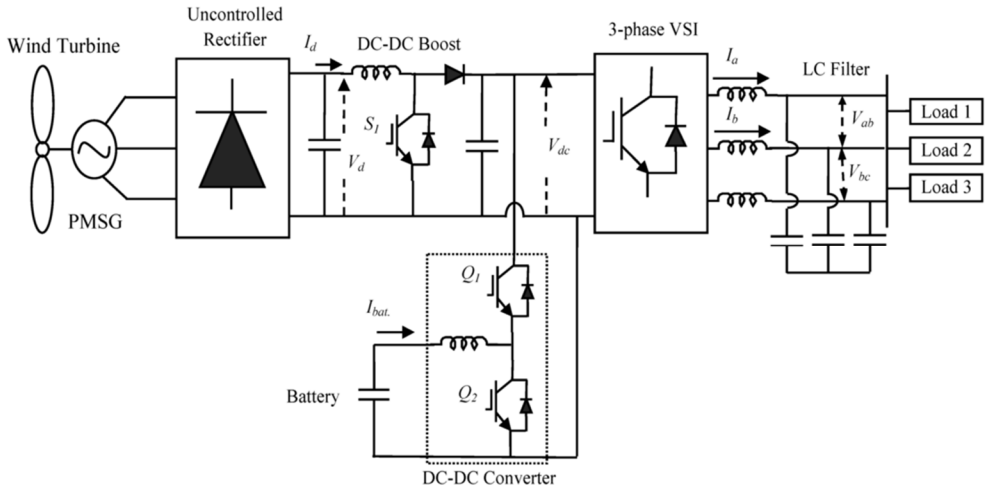


Figure 1.4. Variable speed wind energy supply system [1.51].

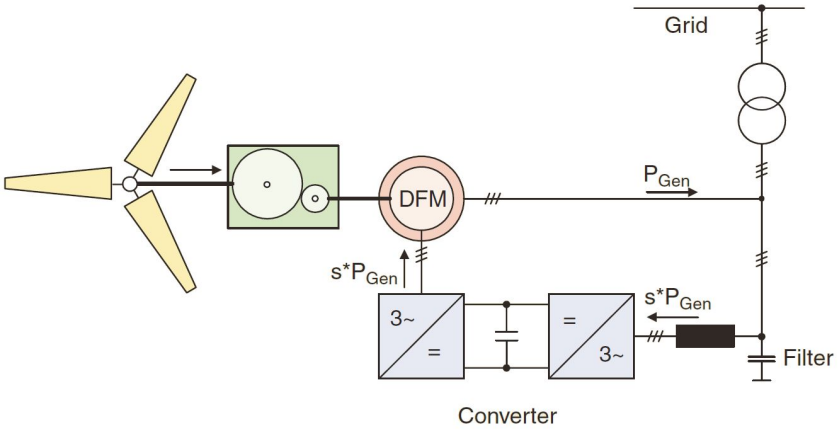


Figure 1.5. Wind turbine generator utilizing a DFIG setup [1.29].

In a DFIG configuration, the stator current of the generator is fed directly to the grid at the desired frequency. The rotor current is connected to a back-to-back converter via a low-pass filter. The frequency of the output of the inverter is variable, and compensates for any change in frequency in the generator due to changes in wind speed.

1.4.4 DC Source Renewable Systems

While sources such as wind are dependent on the kinetic energy of the source, solar power relies on the photoelectric effect, which is the ability of matter to emit electrons when hit with light. Photovoltaic (PV) cells take advantage of this property in semiconductor materials such as silicon to produce a dc current from light sources. A typical PV cell Current-Voltage (I-V) characteristic curve is presented in Figure 1.6. The level of current produced in solar cells is proportional to the amount of light that falls on the PV cell surface. Figure 1.6 shows that as the current decreases, the voltage across the PV cells will increase in a non-linear relationship. Along with this, the characteristics will vary depending on environmental factors such as temperature, irradiation and cleanliness of the panel [1.30]-[1.31].

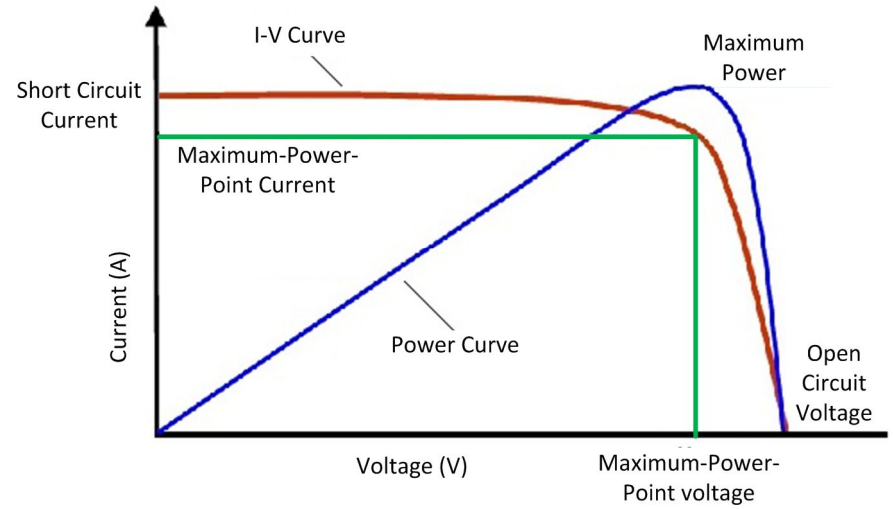


Figure 1.6. The I-V characteristics of a PV cell [1.52].

To remedy this, dc-dc converters are utilised to regulate the output to the dc-link for the ac-dc inverter. Dc-dc converters are also used as pre-regulators for Maximum-Power-Point Tracking (MPPT). Similar to the layout of a battery system, PV cells can either be connected in series to increase voltage capabilities, or in parallel to increase current capabilities. There are four main types of PV installation systems, each of which can either export to the grid, a load or an energy storage unit, presented in Figure 1.7.

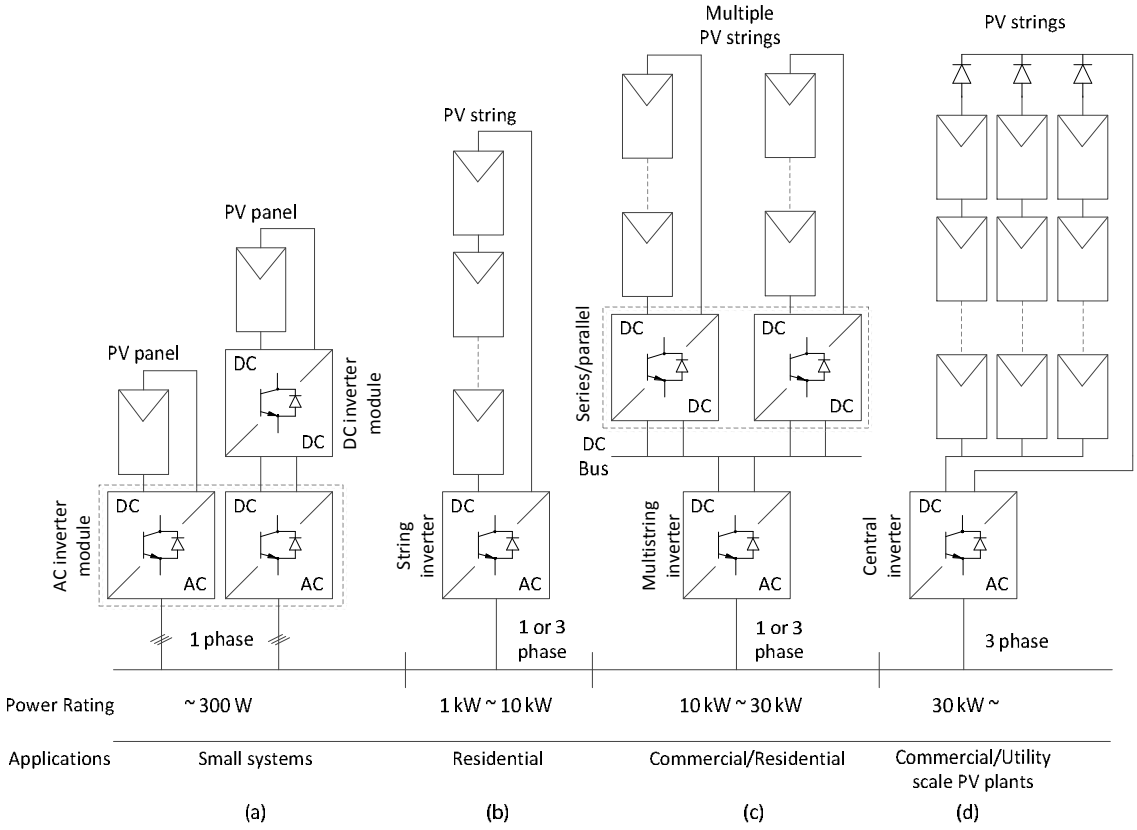


Figure 1.7. The four main types of PV installations [1.32].

1.4.4.1 Micro-Inverter Systems

For loads up to 500 W, PV cells often utilise a micro-inverter system which is presented in Figure 1.7 (a). Micro-inverter systems allow for more flexibility in terms of MPPT tracking and monitoring by allocating a dedicated dc-ac inverter for one to two solar panels. This also increases the redundancy of the system.

1.4.4.2 String Systems

For higher power, up to 10 kW, the micro-inverter system becomes too expensive to become economical. Hence, string systems are more desirable at these power ratings. String systems, presented in Figure 1.7 (b), use a single inverter for a string of solar panels, hence the name. Due to the reduced number of components, the cost of the system decreases. This comes at the cost of decreased flexibility. Another disadvantage

is the reduction in redundancy. If a single solar panel or an inverter switches offline, the entire string becomes inactive.

1.4.4.3 String Systems using Power Optimizers

To increase flexibility and MPPT tracking in string systems, each string may be fitted with a dc-dc pre-regulator, known as a power optimizer. This allows for optimum control of each panel, while still feeding into a centralised dc-ac inverter. A string system with power optimizers is presented in Figure 1.7 (c).

1.4.4.4 Central systems

For applications greater than 30 kW, central systems are often the preferred choice. In a central system, a single ac-dc inverter is used for all PV cells in the system. While this cuts cost, it also drastically reduces flexibility. A central system is presented in Figure 1.7 (d).

1.4.5 Automotive Applications

The electric automotive sector can be broadly split into three categories. These are electric vehicles, hybrid electric vehicles and fuel-cell electric vehicles [1.33]-[1.34].

1.4.5.1 Electric Vehicles

Electric Vehicles (EV) are vehicles which rely completely on power supplied from an on-board battery. A typical battery state of charge curve for several battery types is presented in Figure 1.8. Lithium-ion batteries, such as $LiNiMnCoO_2$ and $LiMn_2O_4$, are the most common choice for electric vehicle batteries due to their light weight and relatively high energy density. A major disadvantage to Li-ion batteries is the volatility of Lithium. Hence, a protective housing is often needed to ensure the safety of the vehicle and the operator in the event of an accident.

It is evident from the curves in Figure 1.8 that as the charge in the battery changes, the cell voltage can vary substantially, especially in Li-ion batteries. Therefore, a boost converter is often essential to increase the poorly regulated voltage and distribute it to the traction motor inverters. Figure 1.9 presents standard layout of an EV drive train, such as the Nissan Leaf [1.36]-[1.37].

In a typical EV drive train, an ac-dc rectifier is used to charge the battery from the main supply. A dc-ac inverter is then utilized to power a three-phase ac motor, which in turn powers the drive axle. It should be noted that, as more and more electric cars are employed, the effect of THD from the charger on the grid is significant. Hence, PFC converters are often employed as one stage of the ac-dc charger.

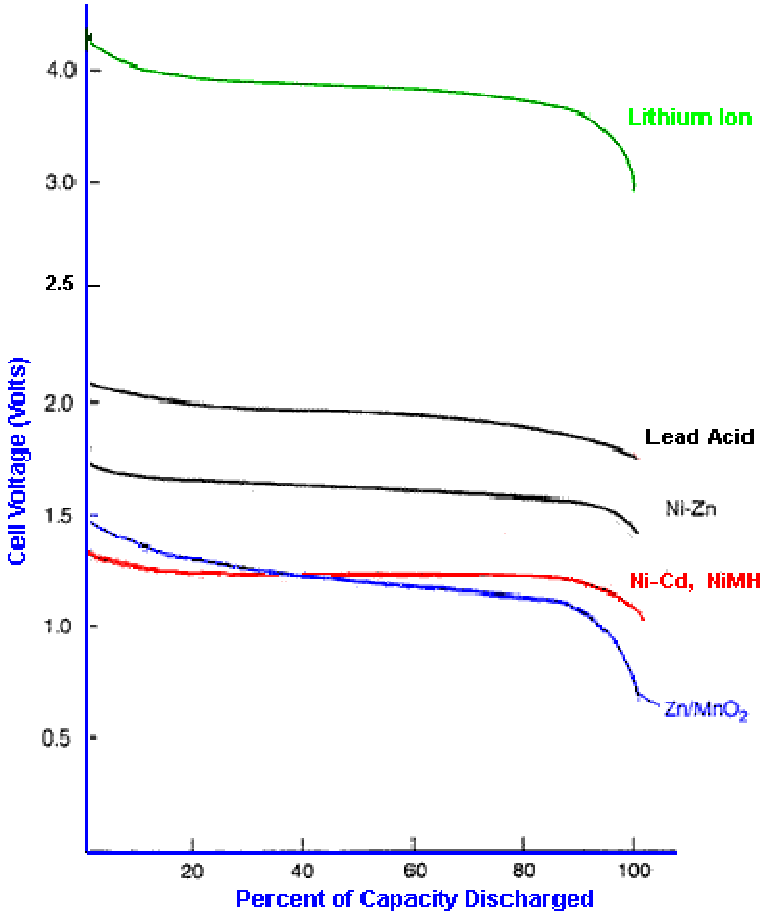


Figure 1.8. Cell voltage vs. state of charge of typical batteries [1.35].

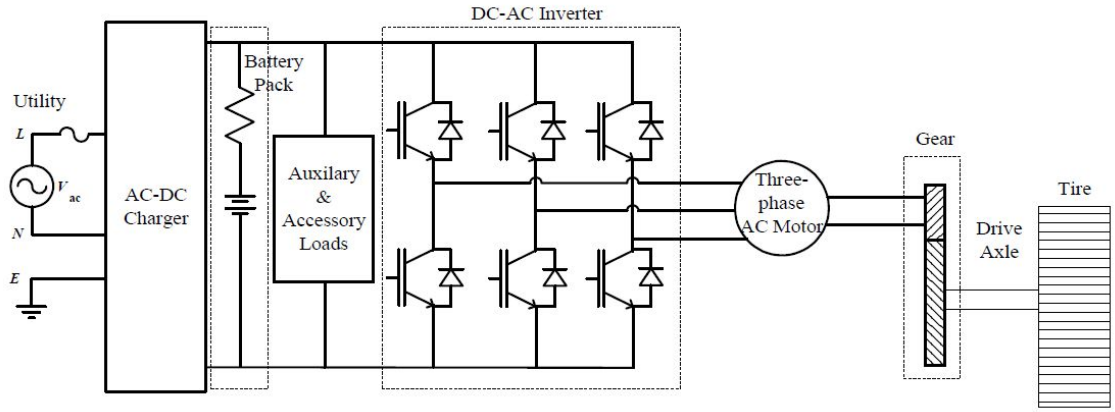


Figure 1.9. Block diagram of electric vehicles drive train [1.36].

One of the major drawbacks of a pure EV is the charge time of the battery and range. The Renault Zoe typically takes six to nine hours for a full battery charge on a 230 V supply [1.38]. The Nissan Leaf takes up to eight hours for a full charge off a 220/240 V supply, which more than doubles for a 110/120 V supply [1.39]. On full charge and under ideal conditions, the estimated range of the Leaf is 199 km, while the Zoe makes it further with 201 km [1.53]. These numbers do not factor in road conditions, traffic and air conditioning, and are tested under the New European Driving cycle (NEDC) [1.55].

1.4.5.2 Hybrid Electric Vehicles

Hybrid Electric Vehicles (HEVs) are fast becoming the first choice in greener transport. By combining the battery storage system of an electric vehicle with a typical combustion engine, fuel costs and greenhouse gas emissions drop without a sacrifice in range. The best-selling HEV, the Toyota Prius, uses a Series-Parallel power train to supply power to the wheels, or charge the battery [1.56].

The early generations of the Toyota Prius, such as the THS I and II were solely powered by gasoline. Power was supplied by the internal combustion engine and used to power the vehicle. To save on fuel, regenerative braking was introduced. The energy recouped from the braking was turned into electrical power by an on-board generator which charged the battery. The main difference between the THS I and THS II was the introduction of a dc-dc converter in the drive train between the battery and the dc-ac inverter. This allowed the THS II to increase part-load efficiency [1.40].

More recent generations, such as the Prius Plug-in Hybrid Electric Vehicle (PHEV), the Chevy Volt, [1.57], and the Mitsubishi Outlander, [1.58], uses a plug-in battery charger to initially charge the battery. The vehicle is then run off the battery until empty, at which point the gas tank takes over as the source of fuel. A typical HEV power train is presented in Figure 1.10.

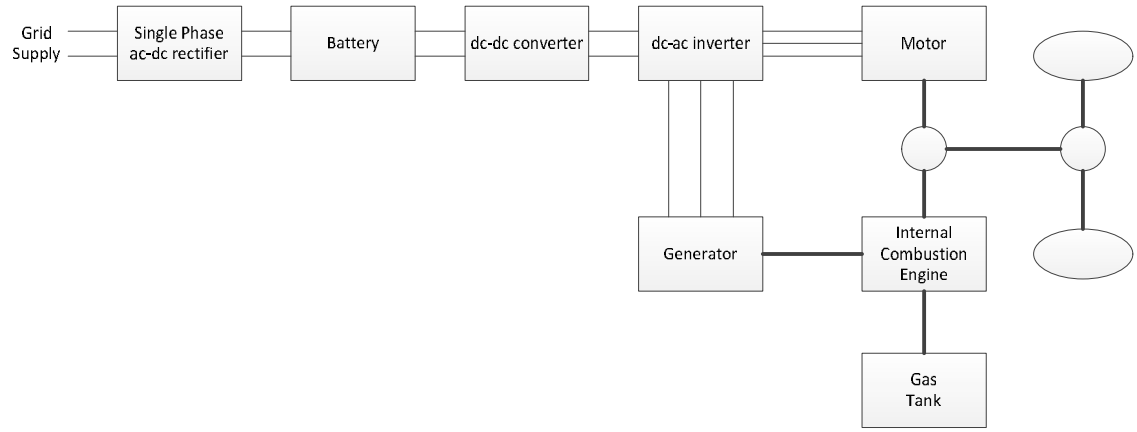


Figure 1.10. Series/parallel plug-in HEV drive train.

In a PHEV drive train, the battery is initially charged through an ac-dc inverter, similar to an EV. The energy in the battery is fed through a Power Control Unit (PCU), which consists of a dc-dc converter to regulate the output at partial loads, and a dc-ac inverter. The output of the inverter is a three-phase ac supply, which powers the motor, which in turn powers the drive train.

For regenerative braking, the torque supplied from the axle causes the motor to turn into a generator, and supply the Power Control Unit (PCU) with current, which in turn, recharges the battery. Finally, as the charge in the battery runs out, the internal

combustion engine takes over. This simultaneously charges the battery, while supplying power to the vehicle.

1.4.5.3 Fuel-Cell Electric Vehicles

Fuel-Cell Electric Vehicles (FCEV) are similar to HEVs in that instead of an internal combustion engine, a fuel-cell is used in conjunction with the on-board battery. In a typical FCEV system, hydrogen and oxygen react to produce electricity, with the only emissions being heat and water. Any pollutants that can be connected to an FCEV system are produced during hydrogen production. A fuel-cell polarization curve is presented in Figure 1.11.

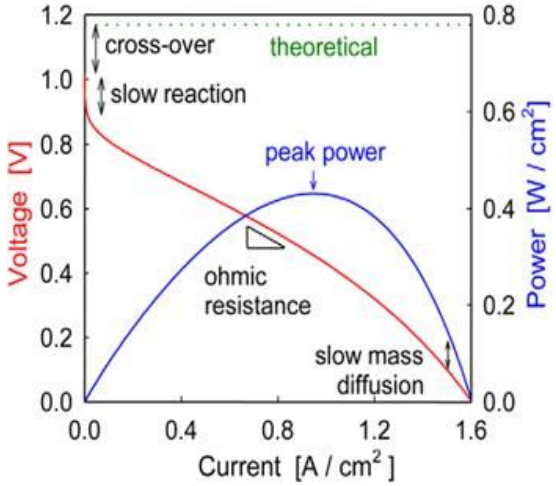


Figure 1.11. A typical fuel-cell polarization curve [1.41].

It is evident from the polarization curve that as the current draw from the fuel-cell increases, the available voltage decreases. Hence, dc-dc converters are critical components in a FCEV system to regulate the output of the fuel-cell.

As with a HEV system, the power produced by the fuel-cell can either be used to charge the on-board battery or super capacitors, or run the motor to drive the vehicle. The drive train of an FCEV system is presented in Figure 1.12. In an FCEV drive train, the fuel-cell typically supplies power for constant load portions, such as cruising, while the on-board storage is employed during transient phases, such as take-off.

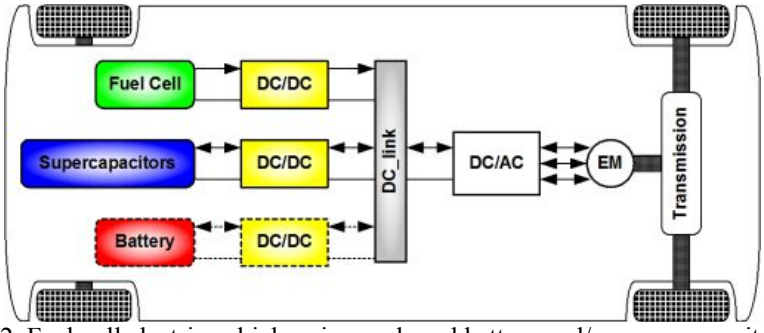


Figure 1.12. Fuel-cell electric vehicle using on-board battery and/or super capacitors [1.42].

1.5 DC-DC Converter Topologies

The area of dc-dc converters can be divided into two categories: isolated and non-isolated. Both of these categories can also be divided into step-up converters, more commonly known as boost converters, and step-down converters, commonly known as buck converters. This thesis focuses on the implementation of coupled-inductors in two-phase non-isolated dc-dc converters.

1.5.1 Boost Converter

The three different boost converter topologies discussed in this thesis are presented in Figure 1.13. These are the (a) single-phase (1L), (b), two-phase (2L), and (c) the two-phase coupled-inductor (XL or CL).

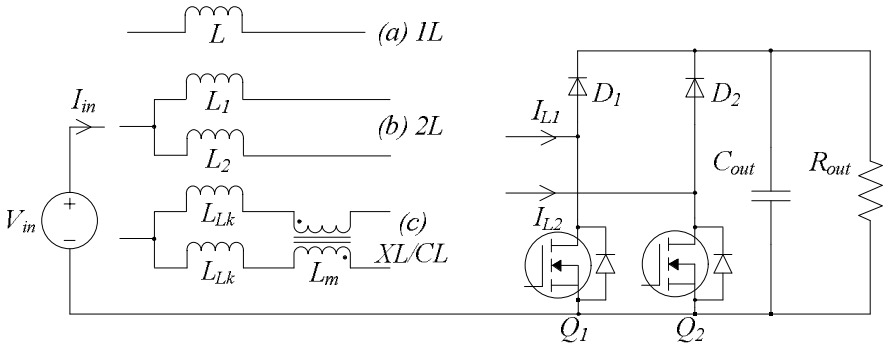


Figure 1.13. The (a) 1L, (b) 2L and (c) CL boost converter topologies.

In a single-phase boost converter, the switch Q_2 and diode D_2 in Figure 1.13 do not exist. The remaining switch Q_1 and diode D_1 are used in conjunction with an inductor to increase the dc voltage from one level to another. When the switch closes, the total input voltage is dropped across the inductor, which causes an energy build-up in the inductor. Once the switch opens, the inductor is then connected through the diode to the output, and the energy is released. The output capacitor of the converter gives a path to ground for the ac ripple current, while the dc current flows into the load. The value of the output voltage is dependent on how long the switch is closed during one full switching cycle.

In a two-phase boost converter, the current which flows through the converter is split in two, effectively halving the current in each phase. One of the major benefits of interleaving is the ability to decrease the input current ripple, allowing for smaller input capacitors, especially at duty cycles around 0.5. Interleaving also leads to a more complicated control structure, as current balancing in both phases must be ensured.

1.5.2 Buck converter

As with the boost converter, the three different buck converter topologies discussed in this thesis are presented in Figure 1.14. These are the (a) single-phase (1L), (b), two-phase (2L), and (c) the two-phase coupled-inductor (XL or CL).

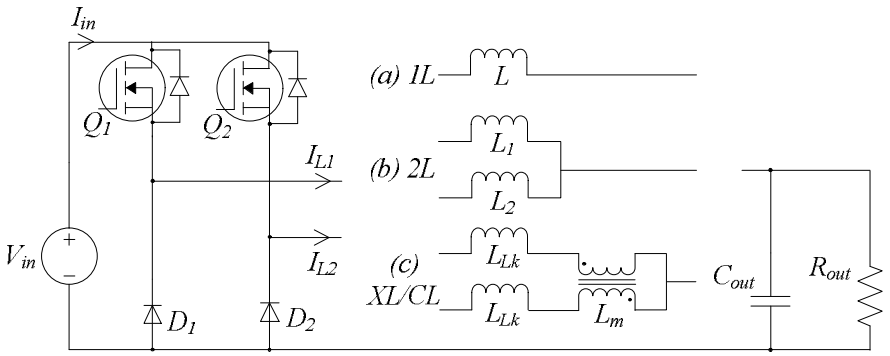


Figure 1.14. The (a) 1L, (b) 2L and (c) CL boost converter topologies.

In a single-phase buck converter, when the switch closes, the input voltage is connected to the inductor and output load, causing a build-up of energy in the inductor. Once the switch opens, the energy in the inductor is released into the load. As with the boost converter, the output capacitor of the buck converter gives the ac current a path to ground, while the dc current flows into the load.

1.5.3 Coupled-Inductor DC-DC Converters

Inductor size, cost, efficiency, and manufacturability studies are an active area of research [1.43]-[1.45]. One solution to this problem is the utilization of coupled-inductors. Coupled-inductors are inductors in which more than one phase winding is wrapped around a single core. A comparison of coupled inductors over traditional discrete inductors has shown significant reduction in the size of the magnetic components [1.46], [1.48]. This is of significant benefit in applications where the size and weight of the converter components are critical, such as EVs and HEVs [1.62]. On the other hand, increased power density in magnetic components comes at the cost of increased thermal density. Hence, if the losses in a coupled-inductor are high, a more efficient cooling system may be required.

While the maximum allowable power loss and temperature rise in inductors are considered in the design phase, these calculations are often approximations. Hence, an inductor may go through several stages of design in order to get the smallest volume possible while keeping core and winding losses to a minimum. The complexity of design only increases when trying to implement coupled-inductors.

Utilising coupled-inductors in dc-dc converters has also been shown to perform faster under load transient conditions when compared to their discrete inductor

counterpart [1.60]. However, if a coupled-inductor converter is designed to have a comparable peak-to-peak phase current ripple, and then the peak-to-peak input current ripple will be larger, leading to bigger filter capacitors. This can be justified by the fact that capacitors are cheaper to manufacture and implement. This larger amount of capacitance, especially the output capacitance, also increases the resonance of the converter, which somewhat limits the control design, since the controller must be designed to lie between the resonance of the converter and the switching frequency.

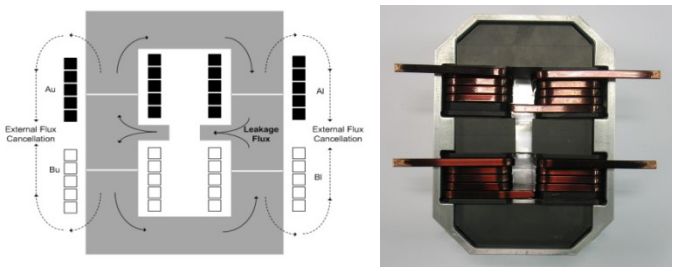
Coupled-inductor converters have also been shown to reduce Common Mode (CM) noise when compared to their discrete inductor counterparts, with the amount of noise attenuation directly linked to the number of phases in the converter [1.61].

Coupled-inductors can be broadly separated into two categories; loosely-coupled, and close-coupled. Loosely-coupled inductors are where the coupling between the phases is relatively small, and the ratio of leakage inductance to magnetizing inductance is large enough that the leakage inductance has a sizeable effect on the circuit. This allows for only one magnetic component in the converter. Close-coupled inductors are where the coupling between the phases is relatively high, and the leakage inductance is small enough that it can be disregarded. Of course, since it is the leakage inductance that is the main contributor to the operation of a boost converter, an auxiliary inductance will have to be added to the phases in order for the converter to suitably operate. While this leads to an increase in the number of magnetic components, the main advantage to this is the fact that both magnetic components can be made from different materials, which is impossible in loosely-coupled inductors, as all inductance are on the one core [1.63].

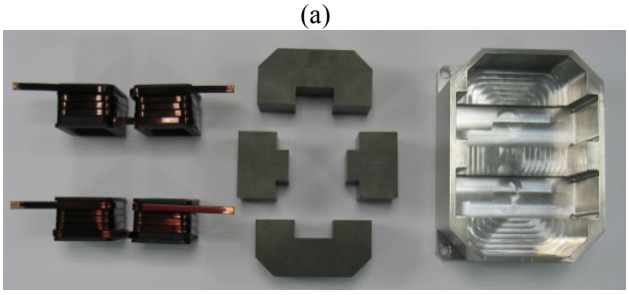
The integrated-magnetics concept discussed in this paper has been demonstrated at 8 kW for distributed generation in [1.49] and at 72 kW for fuel-cell applications in [1.50]. The coupled inductor used in the experimental testing of this thesis is the CCTT-shaped split-winding integrated magnetic (SWIM), as shown in Figure 1.15 [1.47]. This section presents a design example of a 72 kW CCTT IM, which is considered a loosely-coupled inductor.

1.5.3.1 CCTT Coupled-Inductor Design Example

Similar design issues must be considered when designing 2L or CL converters. Depending on the frequency of operation, the semiconductors available, the size of the converter, and other specifications, a major design consideration may be whether to operate in CCM or Boundary Conduction Mode (BCM).



(a)



(b)

Figure 1.15. CCTT SWIM 72 kW prototype (a) assembled and (b) disassembled.

For both the 2L and the CL converters, BCM mode and the various DCM modes have the advantage of a zero-current turn-off of the power diode and a zero-current turn-on of the power switch. This soft-switched operation is often used in order to reduce switching losses in the semiconductor components. Of course, many boost converters are designed to operate in CCM mode with SiC or fast-recovery Si diodes, but BCM enables the use of lower-cost Si diodes. BCM converters often operate in a variable-frequency mode in order to ensure soft switching over the load range. DCM operation is typically entered at part load for CCM and BCM converters, and the 2L and CL converters will maintain the zero-current turn-off of the diode, resulting in efficient operation. The first prototype in this body of work by the authors featured a 72 kW design for an automotive fuel-cell application [1.50] operating in both CCM and DCM.

The 72 kW converter switches at 25 kHz and operates with an input voltage range from 155 V at full load to 260 V at no-load for a 420 V output. Figure 1.16 and Figure 1.17 show the per-phase peak, RMS and peak-to-peak current for the 2L and CL converters, respectively, over the fuel-cell power range. The advantage of the CCTT CL compared to the 2L can be seen more clearly in Figure 1.16 and Figure 1.17. There is little difference between the maximum peak, RMS and peak-to-peak per-phase currents at full power despite the fact that the coupled-inductor is designed for three times less per-phase inductance than the 2L for this particular design.

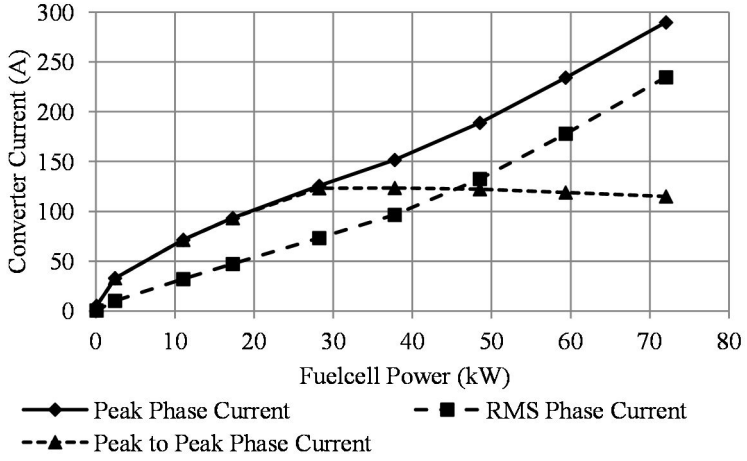


Figure 1.16. Peak, RMS and peak-peak per-phase currents for 2L converters.

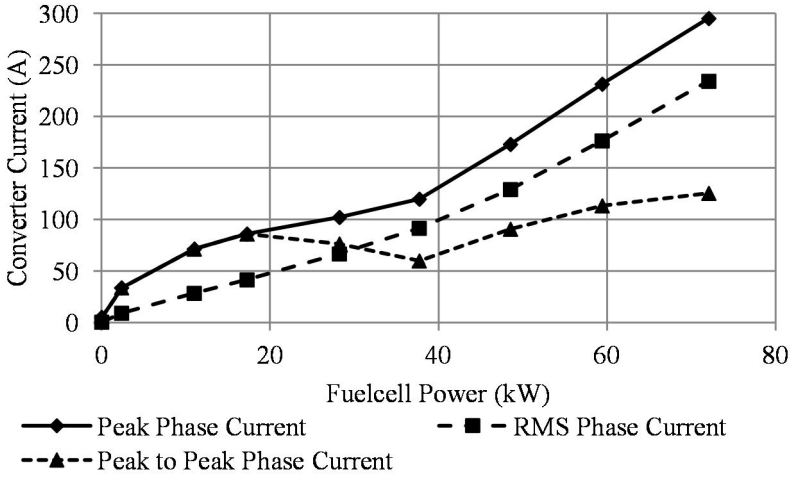


Figure 1.17. Peak, RMS and peak-peak per-phase currents for CCTT CL converters.

The reduction in per-phase inductance is enabled by the mutual coupling. This reduction in required per-phase leakage inductance leads to a significant reduction in the size and weight of the magnetic component and facilitates the use of low-flux ferrite rather than high-flux materials. Additionally, it can be seen that the per-phase peak-to-peak currents drop significantly for the low-to-medium power levels resulting in significantly reduced core and copper losses for the CCTT CL versus the 2L discrete, and improved part-load efficiency.

Two Semikron SEMiX603GB066HDs IGBT modules, [1.59], are used for the power switches. As documented in [1.48], the power loss of both the 2L and CL topologies is very similar. Although the CCTT CL benefits from reduced phase-current ripple, especially at medium load, any reduction in turn-off current (for the IGBT) is offset by an increased turn-on current. Figure 1.18 presents the total predicted 2L and CCTT CL converter efficiencies. The CCTT CL converter efficiency is greater than that of the 2L over the entire load range and it is significantly greater at part-load conditions. The reduced 2L efficiency at part-load is explained by its greater phase-current ripple which

contributes to increased ac winding and core loss. At part load, the 2L converter experiences maximum per-phase currents, as the duty cycle is close to 0.5, resulting in high peak-to-peak currents with resulting copper and core losses, as can be seen in Figure 1.16. The CCTT CL converter has minimum peak-to-peak currents for duty cycles close to 0.5, as can be seen in Figure 1.17, resulting in low phase currents and related copper and core losses.

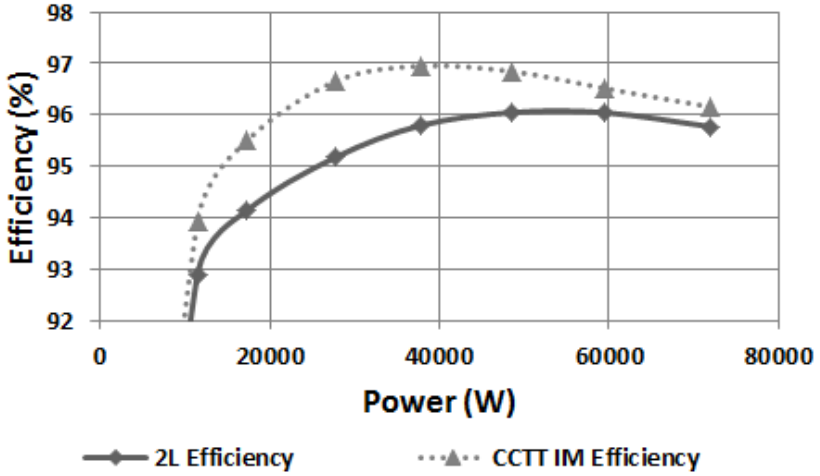


Figure 1.18. Predicted CCTT CL and 2L converter efficiency as fuel-cell power varies.

A 72 kW converter was built and tested to validate the CCTT CL by the authors [1.50]. The total measured converter efficiency versus output power is shown in Figure 1.19 for various boost conditions corresponding to V_{in} = 155 V and V_{out} = 310 V, 360 V and 420 V. The converter power loss is largely due to the semiconductors. The experimental full-load efficiency is 95.5 % at V_{out} = 420 V and P_{in} = 72 kW, and 96.7 % at 310 V, 72 kW.

This thesis is the next stage in the CCTT development and follows on from the work of the 72 kW converter, which largely focused on magnetics.

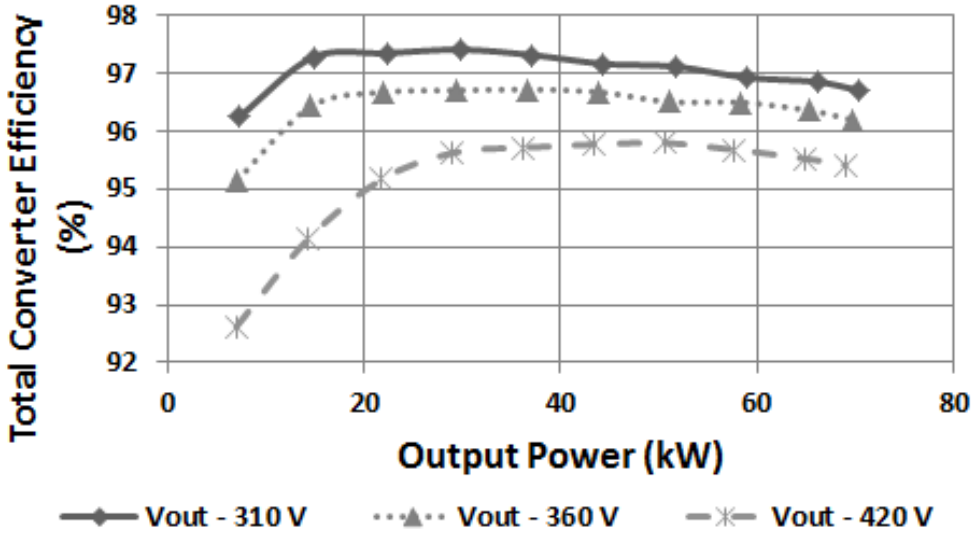


Figure 1.19. CCTT CL converter experimental efficiencies at V_{in} = 155 V.

1.6 References

[1.1] http://www.noaa.gov/climate (Accessed on 25/11/2016).

[1.2] https://www2.ucar.edu/climate/faq/how-much-has-global-temperature-risen-last-100-years (Accessed on 25/11/2016).

[1.3] http://www.opec.org/opec_web/en/data_graphs/330.htm (Accessed on 25/11/2016).

[1.4] "Renewables Global Status Report 2016," Renewable Energy Policy Network for the 21st Century, France.

[1.5] http://www.iwea.com/windstatistics (Accessed on 25/11/2016).

[1.6] https://www3.epa.gov/climatechange/ghgemissions/sources.html (Accessed on 25/11/2016).

[1.7] L. Palma and P.N. Enjeti, "Modular fuel cell, modular DC–DC converter concept for high performance and enhanced reliability," *IEEE Transactions on Power Electronics*, vol. 24, no. 6, pp. 1437-1443, June 2009.

[1.8] K. Jin, X. Ruan, M. Yang, and M. Xu, "A hybrid fuel cell power system," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 4, pp. 1212-1222, April 2009.

[1.9] S. Chandrasekaran and L. U. Gokdere, "Integrated magnetics for interleaved dc-dc boost converter for fuel cell powered vehicles," *IEEE Power Electronics Specialists Conference,* vol. 1, pp. 356-361, June 2004.

[1.10] A. Kirubakaran, S. Jain, and R. K. Nema. "A review on fuel cell technologies and power electronic interface," *Renewable Sustainable Energy Review*, pp. 1-6, 2009.

[1.11] N. Nozawa, T. Maekawa, S. Nozawa, and K. Asakura, "Development of power control unit for compact-class vehicle," *SAE International Journal of Passenger Cars-Electronic and Electrical Systems*, pp.376-382, October 2009.

[1.12] Staff ORNL, Evaluation of the 2010 Toyota Prius Hybrid Electric Drive System, *Oak Ridge National Lab report*, March 2011.

[1.13] C. Ngai-Man Ho, H. Breuniger, S. Pettersson, G. Escobar, L. Serpa, and A. Coccia, "Practical design and implementation procedure of an interleaved boost converter using SiC diodes for PV applications," *IEEE Transactions on Power Electronics*, vol. 27, no. 6, pp. 2835-2845, June 2012.

[1.14] Q. Li and P. Wolfs, "A review of the single phase photovoltaic module integrated converter topologies with three different DC link configurations," *IEEE Transactions on Power Electronics*, vol. 23, no. 3, pp. 1320-1333, May 2008.

[1.15] Y. Fang and X. Ma, "A novel PV micro-inverter with coupled inductors and double-boost topology," *IEEE Transactions on Power Electronics*, vol. 25, no. 12, pp. 3139-3147, Dec. 2010.

[1.16] D. Y. Jung, Y. H. Ji, S. H. Park, Y. C. Jung, and C. Y. Won, "Interleaved soft-switching boost converter for photovoltaic power-generation system," *IEEE Transactions on Power Electronics*, vol. 26, no. 4, pp. 1137-1145, Apr. 2011.

[1.17] S. M. Sharkh, M. A. Abu-Sara, G. I. Orfanoudakis, and B. Hussain (2013), *Power Electronic Converters for Microgrids*: Wiley

[1.18] A.K. Panda, R.K. Parida, N.C. Agrawala, and G.N. Dash, "Comparative study on the high-band gap material (GaN and SiC)-based impact avalanche transit time device" *IET Microwaves, Antennas and Propagation*, vol. 2, no. 8, pp. 789-793, December 2007.

[1.19] K.J. Hartnett, B.J. Lyons, J.G. Hayes, M.G. Egan, M. Ryłko, and J.W. Masłoń, "Comparison of CCTT-core split-winding integrated magnetic and discrete inductors for high-power dc-dc converters," *IEEE Applied Power Electronics Conference*, pp. 1675-1682, March 2013.

[1.20] http://www.digikey.com/en/product-highlight/c/cui/igbt-gate-driver-dc-dc-converters (Accessed on 25/11/2016).

[1.21] J. M. Carrasco, L. G. Franquelo, J. T. Bialasiewicz, E. Galvin, R. C. Portillo-Guisado, M. A. M. Prats, J. I. Leon and N. Moreno-Alfonso, "Power electronics systems for the grid integration of renewable energy sources" *IEEE Transactions on Industrial Electronics*, vol. 53, no. 4, pp. 1002-1016, June 2006.

[1.22] B. Kroposki, C. Pink, R. DeBlasio, H. Thomas, M. Simeos, and P. K. Sen, "Benefits of power electronic interfaces for distributed energy systems," *IEEE Power Engineering Society General Meeting*, pp. 901-908, Montreal, 2006.

[1.23] F. Blaabjerg, Z. Chen, and S. B. Kjaet, "Power Electronics as efficient interface in dispersed power generation systems," *IEEE Transactions on Power Electronics*, vol. 19, no. 5, pp. 1184-1194, September 2004.

[1.24] H. Abu-Rub, M. Malinowski, and K. Al-Haddad (2014), *Power Electronics for Renewable Energy Systems, Transportation and Industrial Application*, Wiley.

[1.25] M. Liserre, T. Sauter, and J. Y. Hung, "Future energy systems: Integrating renewable energy sources into the smart power grid through industrial electronics," *IEEE Industrial Electronics Magazine*, vol. 4, no. 1, pp. 18-37, March 2010.

[1.26] M. Elbuluk, and N. R. N. Idris, "The role of power electronics in future energy systems and green industrialization," *IEEE Power and Energy Conference*, pp. 1-6, December 2008.

[1.27] F. Blaabjerg, F. Iov, R. Teodorescu, and Z. Chen, "Power Electronics in renewable energy systems," *EPE Power Electronics and Motion Control Conference*, pp. 1-17, August 2006.

[1.28] ELTRA. (2000) Specifications for connecting wind farms to the transmission network. (www.offshorecenter.dk/log/bibliotek/Specifications-Eltra.pdf, accessed on 25/11/2016).

[1.29] S. Muller, M. Diecke, and R. W. De Donker, "Double fed induction generator systems for wind turbines," *IEEE Industry Applications Magazine*, vol. 8, no. 3, pp. 26-33, June 2002.

[1.30] SMA Solar Technology AG, "Inverter and PV system technology industry guide 2012," Renewables Insight – Energy Industry Guides, 2012.

[1.31] Solmetric, "A guide to interpreting I-V Curve Measurements of PV Arrays," *Application Note PVA-600-1*, 2011.

[1.32] Y. Yang, and F. Blaabjerg, "Overview of single-phase grid-connected photovoltaic systems", *Electric Power Components and Systems*, vol. 43, no. 12, pp. 1352-1363, July 2015.

[1.33] C. C. Chan and Y. S. Wong, "Electric Vehicles Charge Forward," *IEEE Power and Energy Magazine*, vol. 2, no. 6, pp. 24-33, November 2004

[1.34] C. C. Chan, "The state of the art electric, hybrid and fuel-cell vehicles," *Proceedings of the IEEE*, vol. 95, no. 4, pp 704-718, April 2004

[1.35] http://www.mpoweruk.com/images/discharge-chemistry.gif (Accessed on 25/11/2016).

[1.36] J. G. Hayes, K. Davis, "Simplified electric vehicle power train model for range and energy consumption based on EPA coast-down parameters and test validation by Argonne National Lab data on the Nissan Leaf," *2014 IEEE Transportation Electrification Conference and Exposition*, pp. 1-6, June 2014.

[1.37] J. G. Hayes, "Simplified electric vehicle models for use in undergraduate teaching and research," *IEEE Energy Conversion Congress and Exposition,* pp. 1271-1277, September 2014.

[1.38] http://myrenaultzoe.com/index.php/zoe-description/charging/ (Accessed on 25/11/2016).

[1.39] S. O'Reilly, "Nissan Leaf Frequently-Asked-Questions" *Nissan Ireland Zero Emission Report*, 2015.

[1.40] S. Nozawa, T. Maekawa, E. Yagi, Y. Terao and H. Kohno, "Development of new power control unit for compact-class vehicle" *Symposium on Power Semiconductor Devices and IC's*, pp. 43-45, June 2010.

[1.41] http://nptel.ac.in/courses/103102015/introduction%20and%20overview%20of%20fuel%20cell/images/fig24.1.JPG (Accessed on 25/11/2016).

[1.42] https://daryanenergyblog.wordpress.com/peak-oil-primer/part-4_energy_efficiency/4-2-1-powertrain-options/ (Accessed on 25/11/2016).

[1.43] M. S. Ryłko, B. J. Lyons, J. G. Hayes, and M. G. Egan, "Revised magnetics performance factors and experimental comparison of high-flux materials for high-current dc-dc inductors," *IEEE Transactions on Power Electronics*, vol. 26, no. 8, pp. 2112-2126, August 2011.

[1.44] B. G. You, J. S. Kim, G. K. Lee, G. B. Choi, D. W. Yoo, "Experimental comparison of Mega Flux and JNEX inductors in high power dc-dc converter of hybrid electric vehicles," *IEEE Vehicle Power and Propulsion Conference*, pp. 1-7, September 2011.

[1.45] M. Gerber, J.A. Ferreira, "A high-density heat-sink-mounted inductor for automotive applications," *IEEE Transactions on Industrial Electronics*, vol. 40, no. 4, pp. 1031-1038, July/August 2004.

[1.46] K. J. Hartnett, M. S. Ryłko, J. G. Hayes, and M. G. Egan, "A comparison of classical two phase (2L) and transformer – coupled (XL) interleaved boost converters for fuel cell applications," *IEEE Applied Power Electronics Conference*, pp. 787-793, February 2010.

[1.47] EP (11179872.4) and US (13/602,727) patent application.

[1.48] K. J. Hartnett, B. J. Lyons, J. G. Hayes, M. G. Egan, M. S. Ryłko, and J. W. Masłoń, "Comparison of CCTT-core split-winding integrated magnetic and discrete inductors for high-power dc-dc converters," *IEEE Applied Power Electronics Conference*, pp. 1675-1682, March 2013.

[1.49] K. J. Hartnett, B. J. Lyons, J. G. Hayes, M. G. Egan, M. S. Ryłko, and J.W. Masłoń, "CCTT-core split-winding integrated magnetic interleaved boost converter for high-current renewable energy applications," *IEEE Energy Conversion Conference and Exhibition,* pp. 635-642, September 2013.

[1.50] K. J. Hartnett, J. G. Hayes, M. G. Egan, and M. S. Ryłko, "CCTT-core split-winding integrated magnetic for high-power DC-DC converters," *IEEE Transactions on Power Electronics*, vol. 28, no. 11, pp. 4970-4974, November 2013.

[1.51] M. M. Hussein, T. Senjyu, M. Orabi, M. A. A. Wahab, and M. M. Hamada, "Control of a stand-alone variable speed wind energy supply system," *Applied Sciences*, vol. 4, no. 2, pp. 437-456, 2013.

[1.52] http://myelectrical.com/notes/entryid/225/photovoltaic-pv-electrical-calculations (Accessed on 25/11/2016).

[1.53] http://www.greencarcongress.com/2012/03/zoe-20120309.html (Accessed on 25/11/2016).

[1.54] http://electronicdesign.com/power/factor-pfc-your-power-supply-design (Accessed on 26/11/2016).

[1.55] http://www.unep.org/transport/gfei/autotool/approaches/information/test_cycles.asp (Accessed on 27/11/2016).

[1.56] https://www.toyota.ie/models/prius/index.json?gclid=Cj0KEQiAperBBRDfuMf72sr56fIBEiQAPFXszYcZKB_hI17iFOo19eLLSuxF35aoykQZQb7wGNxIfXAaAirL8P8HAQ (Accessed on 27/11/2016).

[1.57] http://www.chevrolet.com/volt-electric-car.html (Accessed on 27/11/2016).

[1.58] http://mitsubishi-motors.ie/car/outlander/ (Accessed on 27/11/2016).

[1.59] https://www.semikron.com/dl/service-support/downloads/download/semikron-datasheet-semix603gb066hds-27891132 (Accessed on 27/11/2016).

[1.60] G. Zhu, B. A. McDonald, and K. Wang, "Modeling and Analysis of Coupled Inductors in Power Converters," *IEEE Transactions on Power Electronics*, vol. 26, no. 5, pp. 1355-1363, May 2011.

[1.61] S. Lu, M. Mu, Y. Jiao, F. C. Lee, and Z. Zhao, "Coupled Inductors in Interleaved Multiphase Three-Level DC–DC Converter for High-Power Applications," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 120-134, Jan. 2016.

[1.62] Y. Itoh, S. Kimura, J. Imaoka and M. Yamamoto, "Inductor loss calculation of coupled inductors for high power density boost converter," *2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA)*, pp. 2497-2502, May 2014.

[1.63] S. Kimura, Y. Itoh, W. Martinez, M. Yamamoto and J. Imaoka, "Downsizing Effects of Integrated Magnetic Components in High Power Density DC–DC Converters for EV and HEV Applications," *IEEE Transactions on Industry Applications*, vol. 52, no. 4, pp. 3294-3305, July-Aug. 2016.

2 COUPLED-INDUCTOR INTERLEAVED CONVERTER LARGE SIGNAL MODEL

The objective of this thesis is the complete mathematical modelling and control of two-phase interleaved dc-dc converters utilizing coupled-inductors. As such, the first step in this process is to find the large-signal model of the converter. This chapter focuses on the characterization of the continuous-conduction and discontinuous-conduction modes of operation of a two-phase coupled-inductor interleaved boost converter.

2.1 Introduction

The operation of conventional single-phase and two-phase dc-dc converters are well documented [2.1]-[2.2], [2.29]. With applications ranging from power-factor correction, presented in [2.3]-[2.5], to microgrid control, presented in [2.6], a full understanding of all possible modes of operation in dc-dc converters is critical. For example, the author of [2.2] presents solutions for the inductor current waveforms for the three most common types of dc-dc converter; the buck, boost, and buck-boost.

There is a wide body of literature on the subjects of interleaving and coupled inductors. However, very little has been published on the dc-dc converter topology presented in this thesis. Several papers have documented the use of CL converters, such as the buck-boost [2.7], the bridgeless PFC boost [2.8], a PV module converter [2.9], a single-switch high-step-up boost [2.10], and basic interleaving of two-phase boost converters utilizing a CL [2.11]-[2.12]. The use of a single discrete inductor with inter-phase transformer has been documented in [2.13]-[2.15]. A coupled-inductor boost is investigated in [2.16] where the winding arrangement of the terminals of the coupled inductor is direct, rather than the inverse connection implemented in this study. The inverse and direct connections are discussed in [2.17]-[2.18] where it is noted that the inverse coupling has advantages of reduced ripple and wider CCM operation. A coupled-inductor dc-dc buck converter is operated in DCM for efficient low-load operation in [2.19], highlighting the need to document and understand the various modes of operation.

In [2.20] the XL converter is designed to operate in boundary-conduction mode (BCM) with zero-voltage-switching (ZVS). The use of a coupled inductor in a push-pull boost converter is presented in [2.21], and offers lower input ripple into the system. The author of [2.22] presents a process-flow diagram for the use of a CL in a boost converter, but only includes CCM operation. While [2.23] utilizes a coupled inductor in a buck-boost system, DCM operation is chosen to be eliminated due to its over-boost effect and instability. In [2.24] the use of coupled inductors for a fuel-cell has been analysed in CCM and DCM, but the study was only concerned with ensuring the input current operates in CCM, even if each phase current is operating in DCM.

Operation in CCM is similar for the 2L and CL boost converters. However, the discontinuous-conduction modes (DCM) differ greatly due to the mutual coupling within the coupled inductor, resulting in numerous conduction modes and output voltage characteristics.

In order to fully understand the operation of a coupled-inductor two-phase boost converter, it is critical to fully understand the circuit operation of a single-phase boost (1L) and discrete-inductor two-phase boost (2L) converter. Section 2.2 presents the analysis of a single-phase boost converter, while Section 2.3 presents the analysis of a two-phase discrete-inductor boost converter. Section 2.4 presents the analysis of a two-phase coupled-inductor (CL) boost converter which includes the two CCM modes and the ten different DCM modes that can occur together with their respective circuit sub-modes. Section 2.5 presents a detailed analyses of the CL converter operating in CCM mode and the resulting boundary conditions. Section 2.6 presents an analysis of two different DCM modes of operation, which can be extended to find the characteristics of the various other modes. Section 2.7 presents what are called the CCM-DCM mode maps of the CL boost converter. In order to test the theories presented in this thesis, a 1 kW CL boost converter prototype, the design of which is presented in Section 2.8. Section 2.9 presents the experimental results from the 1 kW prototype. Appendix A contains a similar analysis of a CL buck converter, while Appendix B contains the simultaneous equations required to solve the various modes of the CL boost converter, as well as the equations for the duty cycle D, and the off-time, D_{off}. This chapter is based on, and expands on, the work presented in [2.32].

2.2 Single-Phase Boost Converter (1L) Modes of Operation

A 1L boost converter, presented in Figure 2.1, is one of the most common dc-dc converters used in industry due to the relative simplicity of operation.

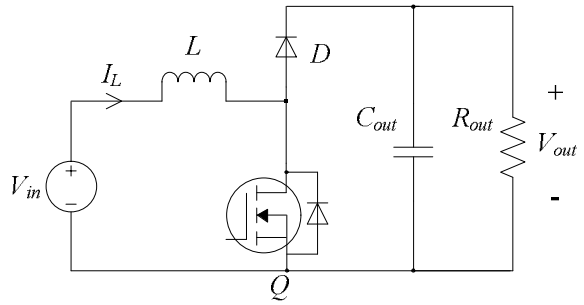


Figure 2.1. The single-phase boost converter.

There are four different modes of operation when utilising a single-phase boost converter; two for continuous-conduction mode (CCM) and two for discontinuous-conduction mode (DCM). The current waveforms of each mode are presented in Figure 2.2.

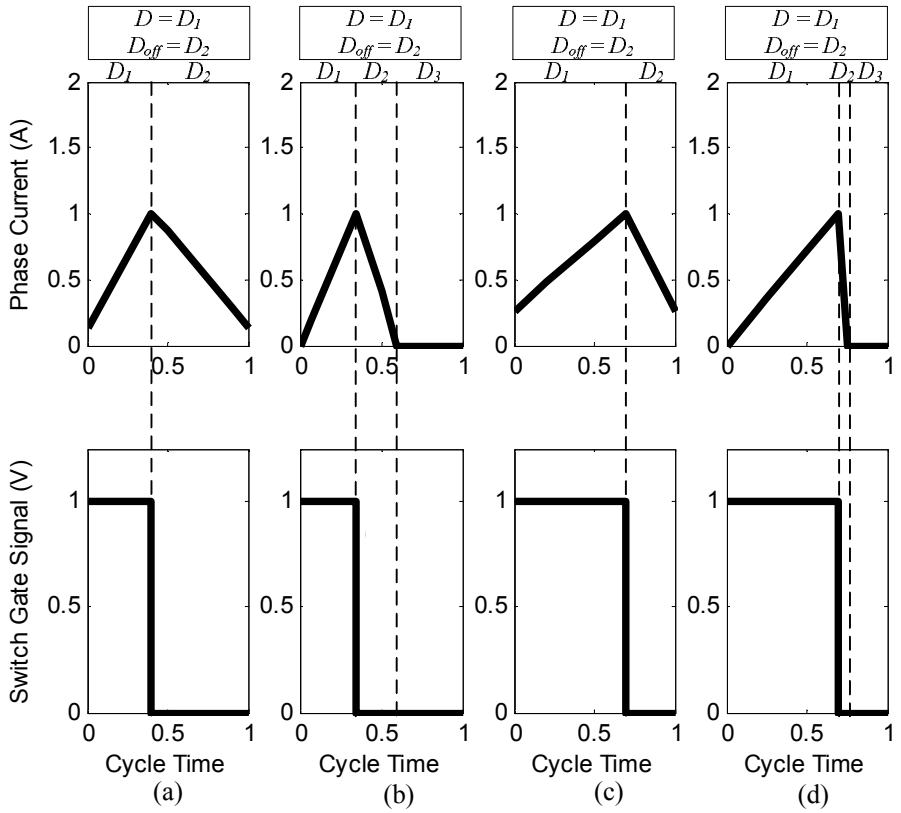


Figure 2.2. Current and gate-drive waveforms of (a) 1L CCM 1, (b) 1L DCM 1, (c) 1L CCM 2 and (d) 1L DCM 2.

In Figure 2.2, D_{off} is the part of the cycle where the diode conducts. The two CCM modes, 1L CCM 1 and 1L CCM 2 occur when the converter is in CCM and the duty cycle is less than, and greater than 0.5 respectively. The gain of the converter when operating in both these modes is

$$\frac{V_{out}}{V_{in}} = \frac{1}{1-D} \tag{2.1}$$

As can be seen from equation (2.1), the load current does not affect the gain of the system when operating in CCM. As the load current begins to drop, the inductor current will begin to reach zero at every cycle. This region of operation is termed Boundary Conduction Mode (BCM). The two remaining modes are when the converter is operating in DCM, and are named 1L DCM 1, where the converter has a duty cycle of less than 0.5, and 1L DCM 2, where the converter has a duty cycle greater than 0.5. This occurs when the current does not flow through the inductor for a finite length of time. The gain of the converter when operating in both these modes is

$$\frac{V_{out}}{V_{in}} = \frac{2}{1+\sqrt{\frac{8L}{R_{out}T_sD^2}}} \tag{2.2}$$

where R_{out} is the output load resistance of the converter. Since the gain of the converter now relies on the output resistance, it is said to be load dependent.

The characteristics of the 1L boost converter are plotted in Figure 2.3 to Figure 2.5 in what are termed the CCM-DCM mode maps by the author. These mode maps are based on the diagrams given in [2.26], and provide a more comprehensive overview of the different modes of operation in a dc-dc converter.

The mode maps plot the duty cycle of the converter D, against the dc output current of the converter I_o in Figure 2.3, the RMS phase current $I_{L(RMS)}$ in Figure 2.4, and the input dc current $I_{in(DC)}$ in Figure 2.5 for three different voltage gain ratios. The x-axis, which represents the various currents, is normalised to the maximum output boundary current $I_{oB,max}$, which occurs at a duty cycle of $0.3\dot{3}$. The maximum output boundary current, derived in [2.26], is found to be

$$I_{oB,Max} = D(1-D)^2\frac{V_{out}T_s}{2L} = 0.074\frac{V_{out}T_s}{L} \text{ for } D = 0.33 \tag{2.3}$$

where V_{out} is the converter output voltage, T_s is the switching cycle time, and L is the phase inductance. In all of the CCM-DCM mode maps presented, the solid lines represent the characteristic curves of the converter, i.e. a plot of the duty cycle at the specified current for a given voltage gain, while the dashed lines represent the boundaries between the various CCM and DCM modes of operation. This analysis has also been carried out using K factors [2.27], which are preferred by some authors to graphically represent the boundary between CCM and DCM, and are discussed in [2.27].

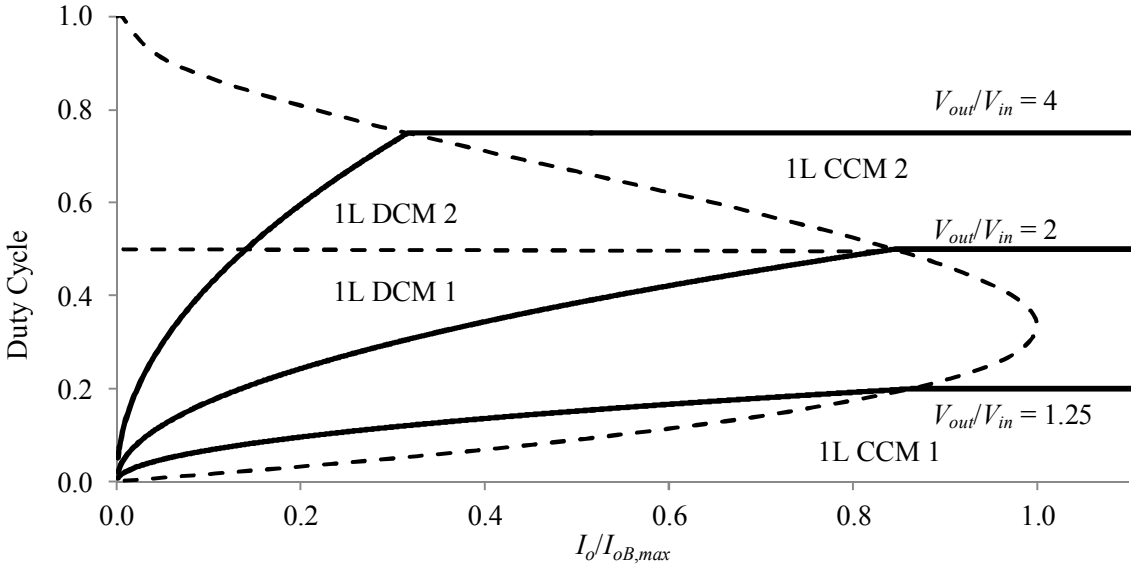


Figure 2.3. Output current CCM-DCM mode map for the 1L boost converter.

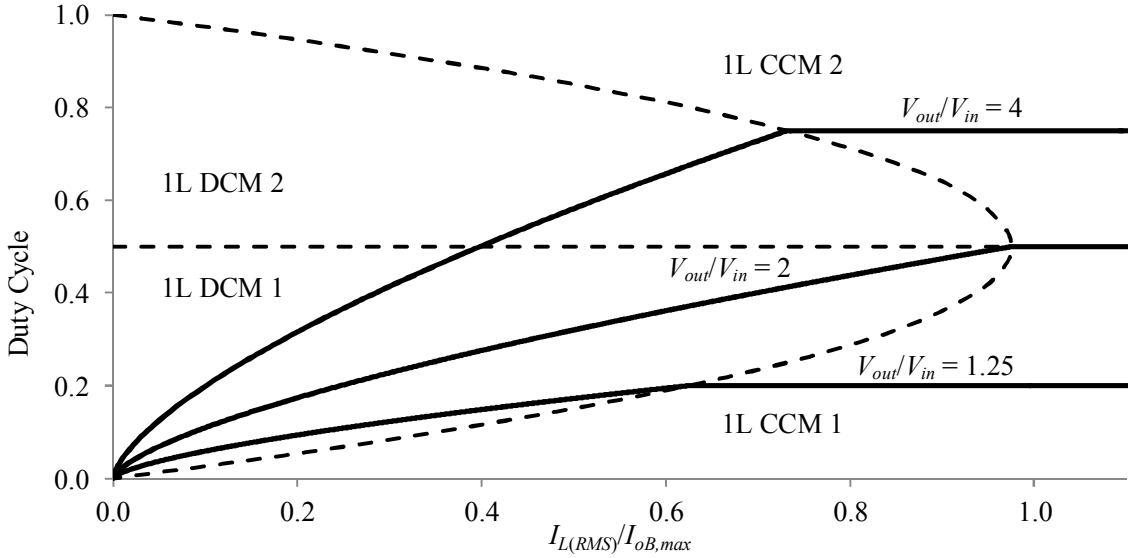


Figure 2.4. RMS phase current CCM-DCM mode map for the 1L boost converter.

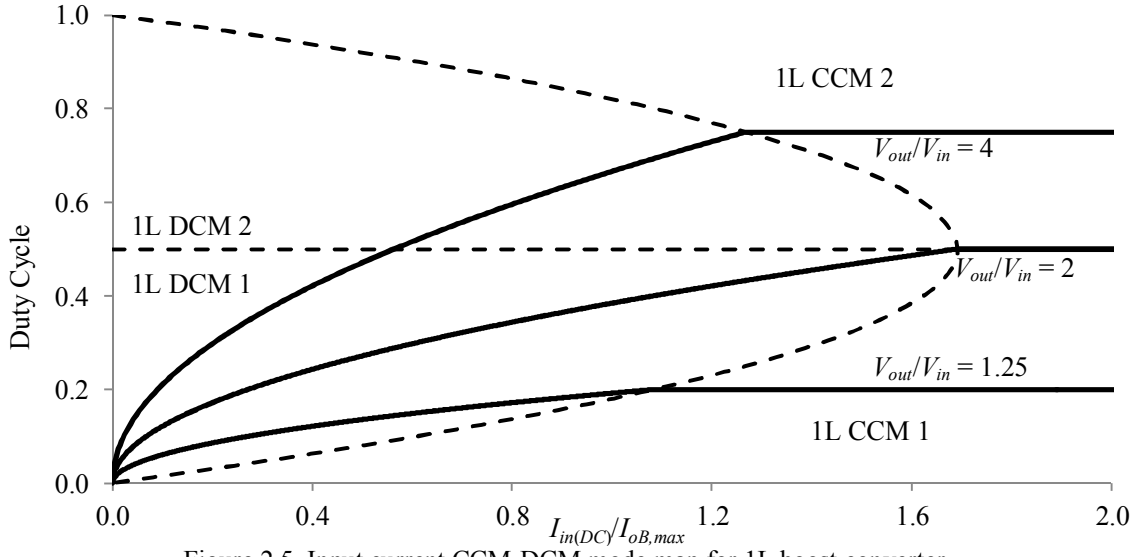


Figure 2.5. Input current CCM-DCM mode map for 1L boost converter.

2.3 Discrete-Inductor Two-Phase Boost Converter (2L) Modes of Operation

The discrete-inductor two-phase boost converter (2L) is presented in Figure 2.6, and differs from the 1L boost converter in that there are two paths for the current to flow. A properly designed 2L boost converter should ensure that both phases carry an equal amount of current. This allows for the inductors and semiconductor switches to be de-rated to half the current compared to the 1L converter.

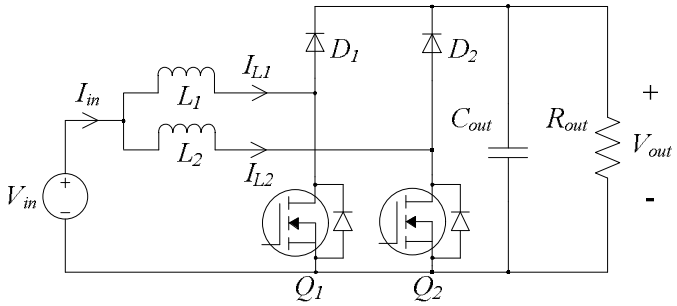


Figure 2.6. Two-phase discrete-inductor boost converter.

The implementation of a second phase into a boost converter increases the number of operation modes from four to five; two of which are in CCM operation, and the remaining three during DCM operation. The current waveforms of each mode of the 2L boost converter are presented in Figure 2.7. As with the single-phase converter, D_{off} represents the time in the cycle where the diode is conducting, while both D and D_{off} are with respect to phase 1 of the converter. The current waveforms presented in Figure 2.7 (a) and (b) occur when the converter is operating in CCM and are labelled 2L CCM 1 and 2L CCM 2. These occur when the duty cycle is less than and greater than 0.5 respectively. Like the 1L converter, the gain of the 2L converter in these modes is

$$\frac{V_{out}}{V_{in}} = \frac{1}{1-D} \tag{2.4}$$

Once again, it is evident that the gain of the system does not depend on the current flowing through the system. As current begins to drop, the instantaneous inductor current will eventually reach zero, and enter DCM. The remaining three modes occur when the converter is operating in DCM and are labelled 2L DCM 1, 2L DCM 2 and 2L DCM 3. 2L DCM 3 occurs when the converter is operating at a duty cycle greater than 0.5, while 2L DCM 1 and 2L DCM 2 occurs when the converter is operating at a duty cycle of less than 0.5. The difference between 2L DCM 1 and 2L DCM 2 depends on whether the input current is still operating continuously or discontinuously. When the converter is operating in 2L DCM 1, the input current, which is the sum of the two phase currents, do not reach zero.

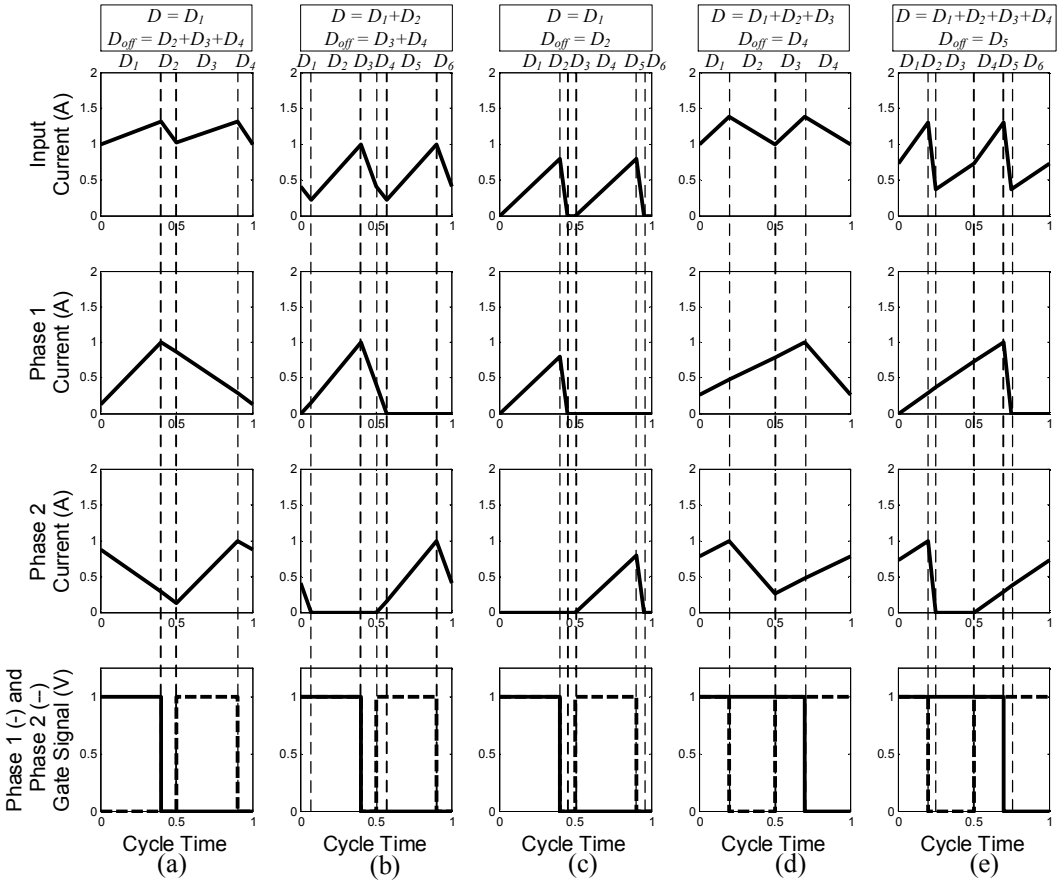


Figure 2.7. Current and gate-drive waveforms of (a) 2L CCM 1, (b) 2L DCM 1, (c) 2L DCM 2, (d) 2L CCM 2 and (e) 2L DCM 3.

Conversely, the input current does reach zero in 2L DCM 2. If the duty cycle is greater than 0.5, the input current of the converter does not go to zero. This is due to the fact that for duty cycles greater than 0.5, at least one switch will always be closed, leading to current rising in the inductor. The gain of the converter when operating in any of the three DCM modes is identical, and is given by

$$\frac{V_{out}}{V_{in}} = \frac{2}{1+\sqrt{\frac{4L}{R_{out}T_s D^2}}} \tag{2.5}$$

As can be seen from equation (2.5), the converter is now load-dependent when in DCM. The equation for the gain of the 2L converter when operating in DCM is very similar to that of a 1L operating in DCM. The difference is a factor of two which appears inside the square root. This is due to the fact that in a 2L converter, each phase of the converter only sees half the load current. Like the 1L converter, the CCM-DCM mode maps of the 2L boost converter are presented in Figure 2.8, Figure 2.9 and Figure 2.10 for the converter output current, RMS phase current and input current, respectively.

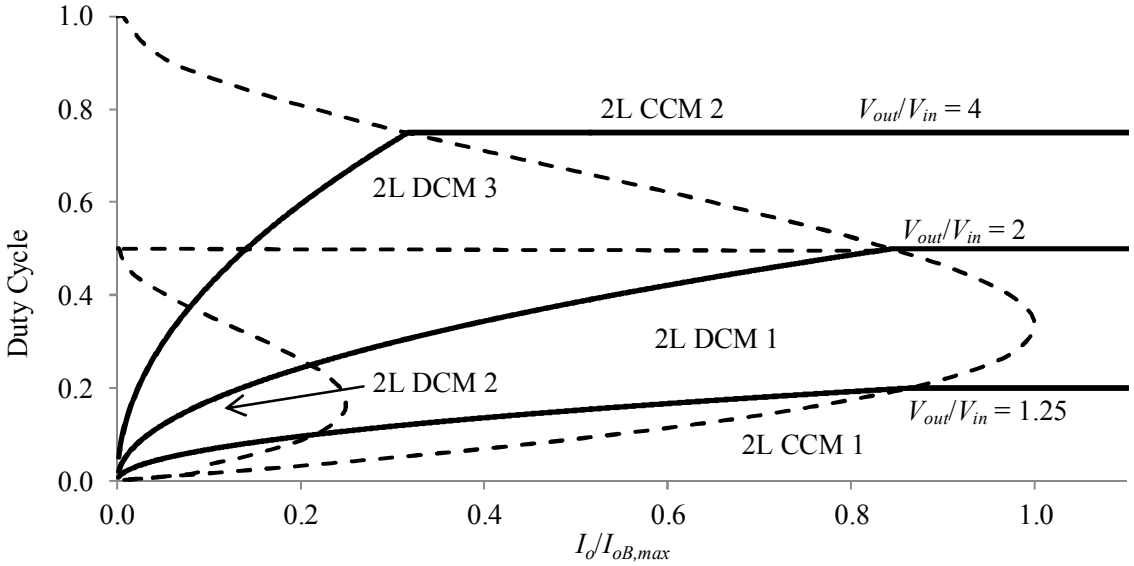


Figure 2.8. Output current CCM-DCM mode map for 2L boost converter.

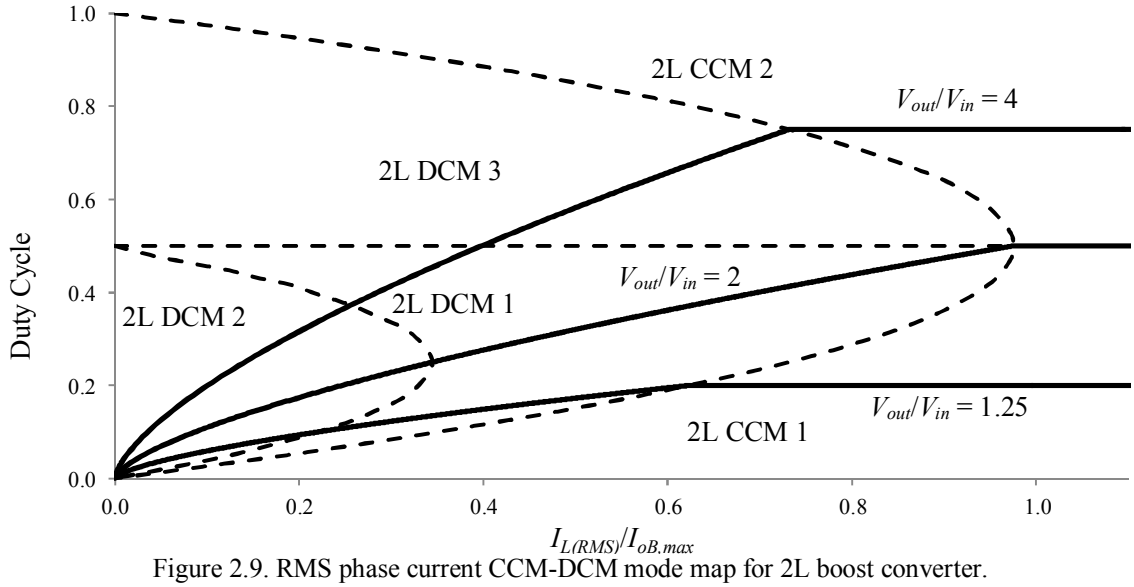


Figure 2.9. RMS phase current CCM-DCM mode map for 2L boost converter.

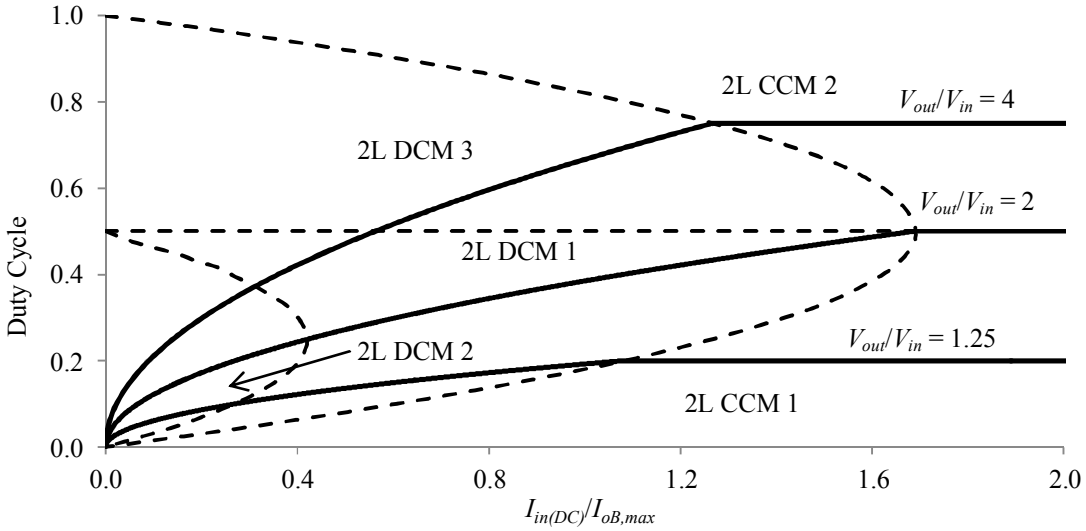


Figure 2.10. Input current CCM-DCM mode map for 2L boost converter.

The maximum output boundary current of the 2L, which occurs at a duty cycle of 0.33, is half the value it would be if operating as a 1L converter, i.e.

$$I_{oB,Max} = D(1-D)^2 \frac{V_{out}T_s}{2L} = 0.074\frac{V_{out}T_s}{2L} \text{ for } D = 0.3\dot{3} \tag{2.6}$$

2.4 Coupled-Inductor Two-Phase Boost Converter (CL) Modes of Operation

The operation of multi-phase coupled-inductor dc-dc converters is more complex than their traditional discrete-inductor counter-parts, especially when operating in discontinuous-conduction mode. In a coupled-inductor converter, both the leakage inductance L_{Lk} and the magnetising inductance L_m must be taken into account. The coupled-inductor two-phase boost converter (CL) is presented in Figure 2.11, which shows the leakage and magnetising inductances.

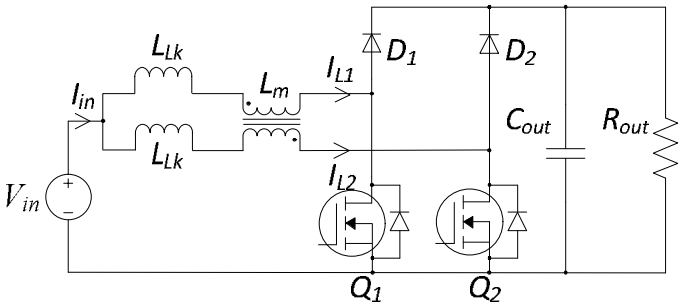


Figure 2.11. The two-phase coupled-inductor boost converter with MOSFETs.

As with the single-phase and two-phase converters, there are two CCM modes of operation; CCM 1, and CCM 2. However, while the single-phase and two-phase boost converters had two and three DCM modes respectively, the CL boost converter contains ten DCM modes of operation. The current waveforms for each mode of operation of the CL boost converter are presented in Figure 2.12 to Figure 2.14.

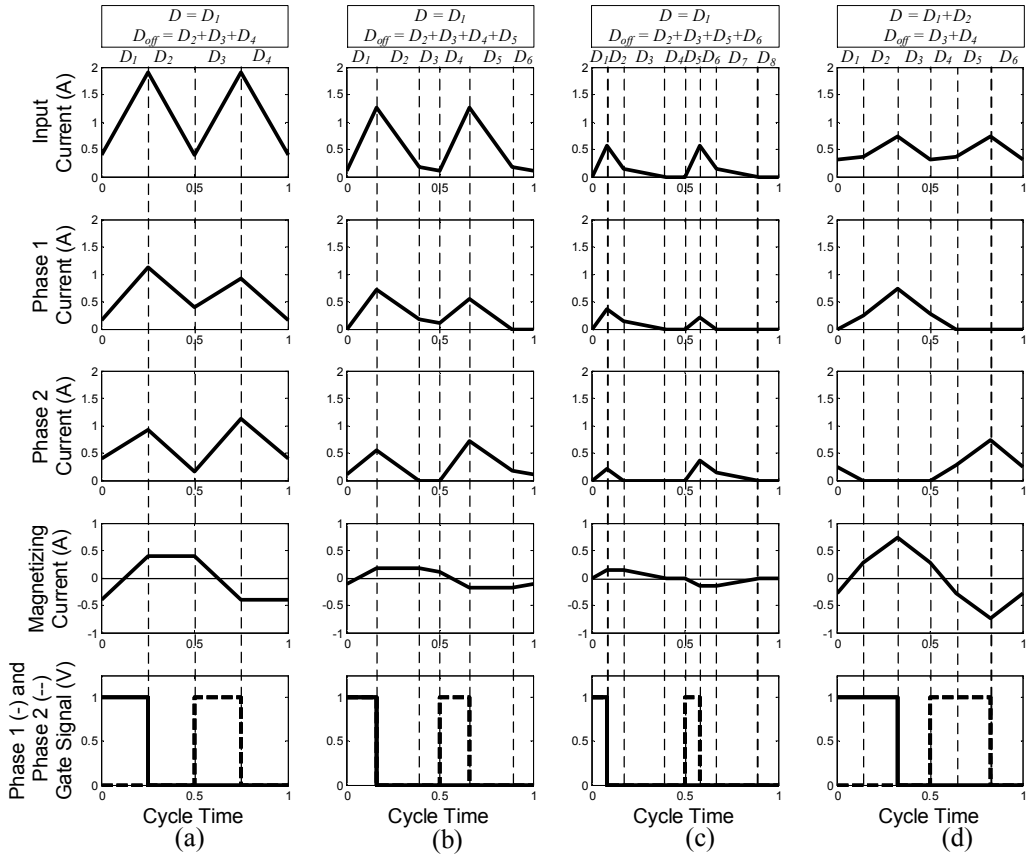


Figure 2.12. Current and gate-drive waveforms of (a) CCM 1, (b) DCM 1, (c) DCM 2 and (d) DCM 3 of a CL boost converter.

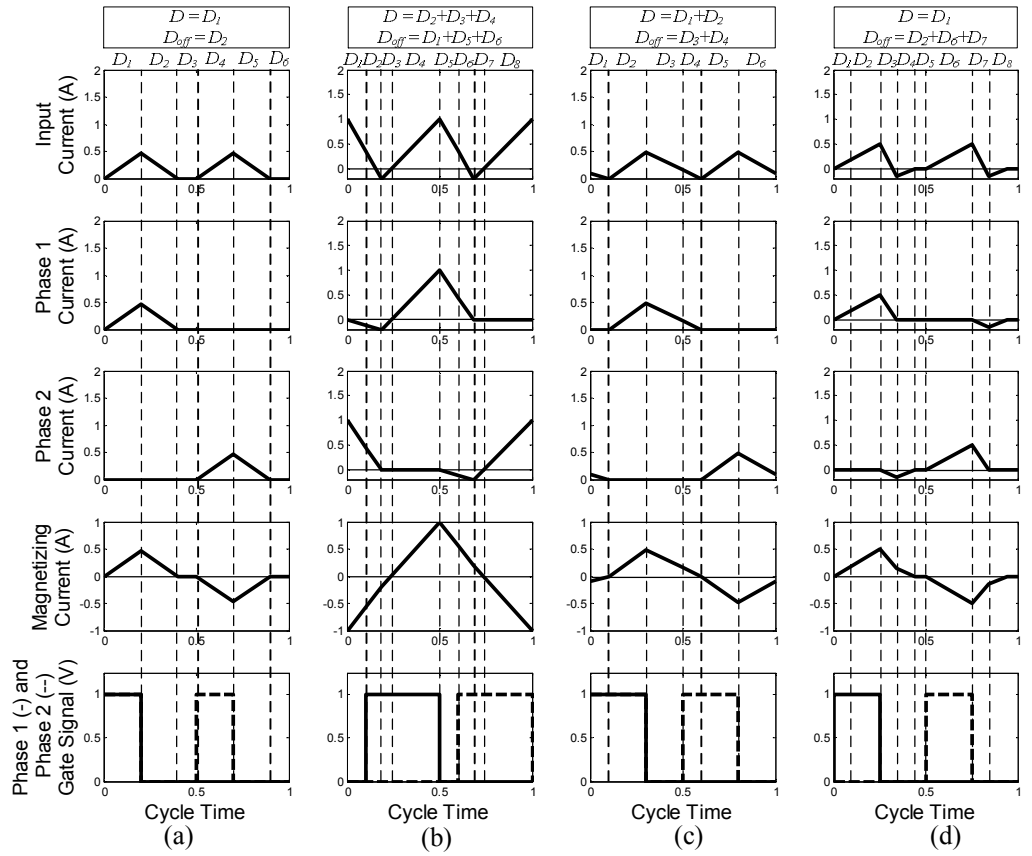


Figure 2.13. Current and gate-drive waveforms of (a) DCM 4, (b) DCM 5, (c) DCM 6 and (d) DCM 7 of a CL boost converter.

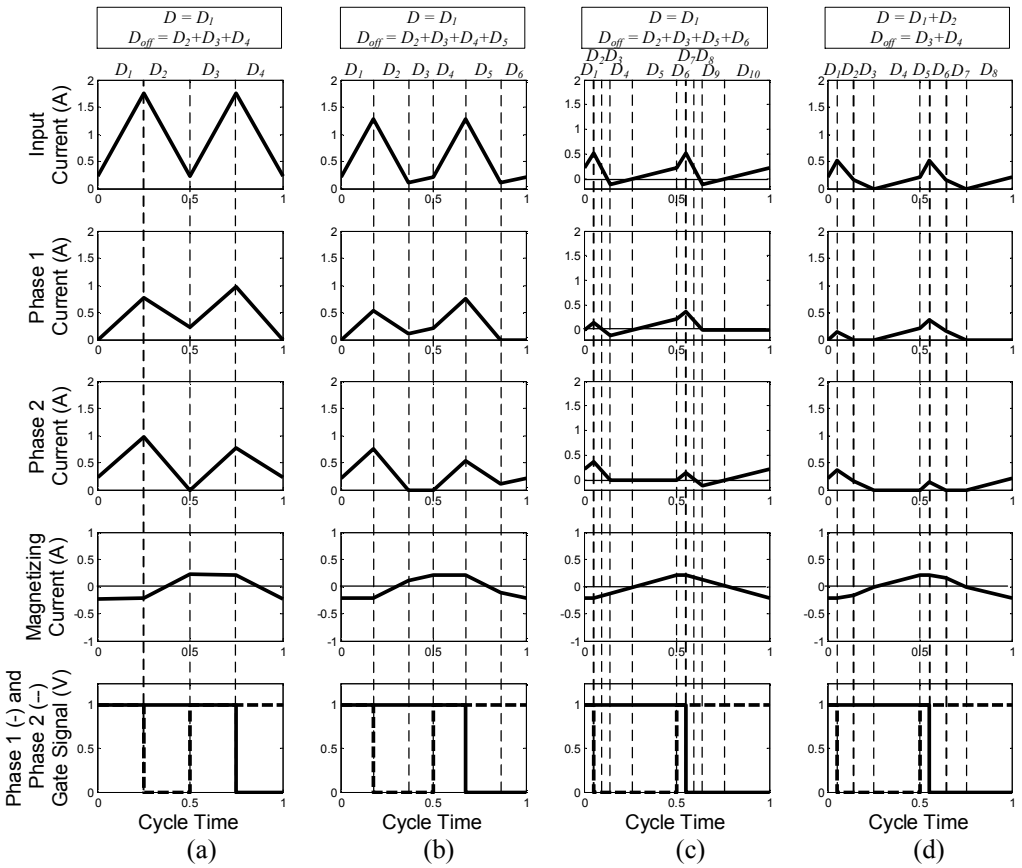


Figure 2.14. Current and gate-drive waveforms of (a) CCM 2, (b) DCM 8, (c) DCM 9 and (d) DCM 10 of a CL boost converter.

A brief explanation of each mode is as follows

CCM 1: Figure 2.12 (a) shows the current waveforms for CCM 1. In this mode of operation, the peak of the phase 1 inductor current occurs in the first half of the cycle time. The voltage gain for this mode is the same as for a single-phase and two-phase boost converter.

DCM 1: Figure 2.12 (b) shows the current waveforms for DCM 1. In this mode, only one phase will cease to conduct at any one time. The input current will continue to operate in CCM. The voltage gain of the converter is now load-dependent.

DCM 2: Figure 2.12 (c) shows the current waveforms for DCM 2. In this mode, both phases will cease to conduct during the same cycle time. This causes the input current to also enter DCM.

DCM 3: Figure 2.12 (d) shows the current waveforms of DCM 3. In this mode, de-coupling action begins to take effect i.e. a rise in current in one phase does not give a rise in current in the other, and a piece-wise-linear rise in current can be seen.

DCM 4: Figure 2.13 (a) shows the current waveforms of DCM 4. In this mode, complete de-coupling of the phases can be seen, with the characteristics similar to that of a single-phase and two-phase boost converter. In this mode, the input current

operates in DCM. The size of the region of DCM 4 is also dependent on the type of switch used in the converter. When using a unidirectional switch, the region of DCM 4 is much larger when compared to using a bidirectional switch. Section IV uses the solution of DCM 4 as an example of characterizing DCM modes of operation.

DCM 5: Figure 2.13 (b) shows the current waveforms of DCM 5. Mode DCM 5 is unusual in that, in this mode, a change in duty cycle will not result in a change in current. This mode occurs when operating with a freewheeling diode. Due to the coupling of the phases, the current path created by the free-wheeling diode allows the reverse flow of current in one phase as soon as the opposite phase opens its switch. The input current will also begin to flow in the negative direction for a short period of time.

DCM 6: Figure 2.13 (c) shows the current waveforms of DCM 6. This mode replaces DCM 5 when an inverse diode is not present. In this mode, the duty cycle is not dependent on the converter current.

DCM 7: Figure 2.13 (d) shows the current waveforms of DCM 7. Again, this mode occurs when operating with an inverse diode. Due to the coupling of the phases, the current path created by the free-wheeling diode allows the reverse flow of current in one phase as soon as the opposite phase opens its switch. The input current will also flow in the negative direction for a short period of time, similar to DCM 5. When the converter is in this mode, the duty cycle is once again dependent on the converter current.

CCM 2: Figure 2.14 (a) shows the current waveforms for CCM 2. In this mode of operation, the peak of the phase 1 inductor current occurs in the second half of the cycle time. The voltage gain for this mode is the same as for a single- and two-phase boost converter.

DCM 8: Figure 2.14 (b) shows the current waveforms of DCM 8. In this mode, only one phase will cease to conduct at any one time. The input current will operate in CCM. The converter duty cycle is once again load-dependent.

DCM 9: Figure 2.14 (c) shows the current waveforms of DCM 9. Again, coupling action forces a negative flow of current through the switch at some point during the cycle time. The input current will also flow in the negative direction for a short period of time, similar to DCM 5 and DCM 7.

DCM 10: Figure 2.14 (d) shows the current waveforms of DCM 10. This mode replaces DCM 7 when the reverse flow of current is blocked in the switch.

2.4.1 Modal Analysis

The determination of the operating modes for a single-phase and two-phase boost converter has been documented in [2.26], but limited research had been done for a CL boost. The 2L and CL circuits of Figure 2.6 and Figure 2.11 can be redrawn as shown in Figure 2.15, where v_{in} is the input voltage, i_{in} is the input current, i_{L1} and i_{L2} are the currents of phase 1 and phase 2, respectively, L_{Lk} and L_m are the leakage and magnetizing inductances, respectively, and Y_1 and Y_2 are the quad-state output variables. For the 2L circuit, the value of the magnetizing inductance is zero.

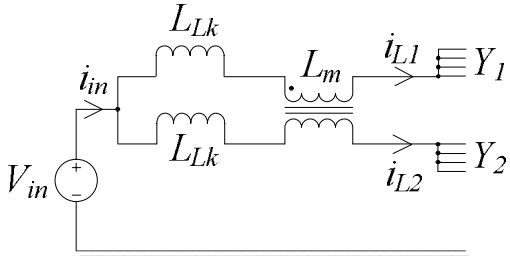


Figure 2.15. Simplified coupled-inductor boost converter with quad-state outputs.

The solutions to the quad-state variables in Figure 2.15 are shown in equation (2.7), where V_{out} represents the state when the diode is conducting, open circuit, (OC), represents the state when the phase current is zero, 0 represents the state when the switch switch Q is conducting, and D_L represents the state when the freewheeling diode of the switch is conducting.

$$Y_1, Y_2 = \begin{cases} V_{out} \\ OC \\ 0 \\ D_L \end{cases} \tag{2.7}$$

There are a resulting thirteen sub-modes of operation as shown in Figure 2.16. The modes of operation for the 2L and CL are presented in Table 2.1 and Table 2.2, along with their sub-modes (SM) and the Y_1 and Y_2 quad-state output variables. Each cycle can have several different sub-modes.

As an example, mode 2L CCM 1 is the 2L continuous-conduction mode for $D < 0.5$ and this has four sub-modes, shown in Table 2.1 as D_1-D_4. The current waveforms and gate voltages are shown in Figure 2.7 (a) for 2L CCM 1. As can be seen this mode has four sub-modes which are shown in Table 2.1 and Figure 2.7 (a) as D_1-D_4. Table 2.1 shows the quad-state outputs for the various sub-modes. Table 2.1 and Table 2.2 contain all the information on the time intervals and sub-modes for all 4 CCM modes and 13 DCM modes in this boost converter family.

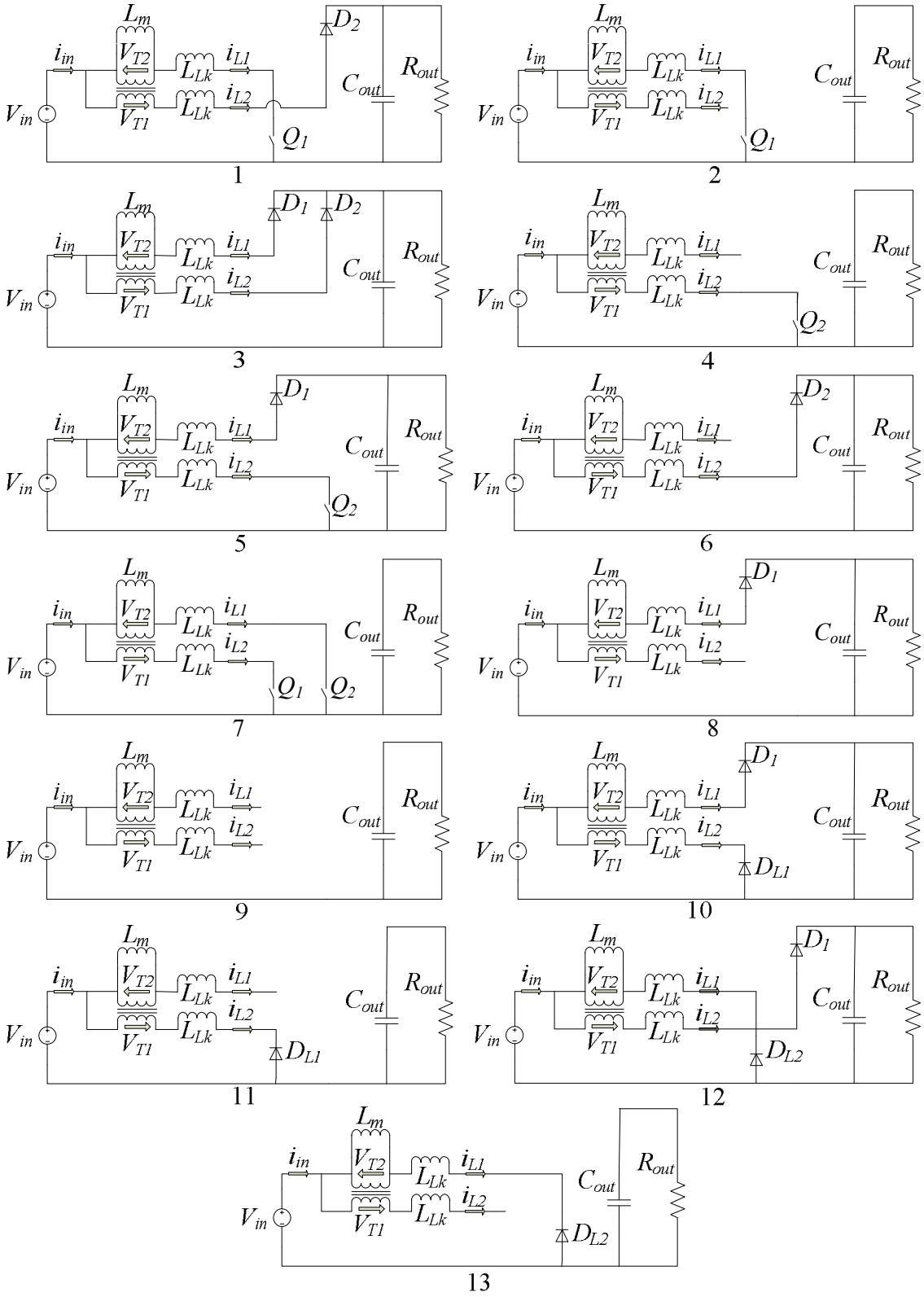


Figure 2.16. Sub-modes of operation for the 2L and CL boost converters.

Table 2.1. Sub-modes of operation and quad-state Y solutions for a two-phase (2L) interleaved boost converter.

SM, Y1, Y2		D1	D2	D3	D4	D5	D6
2L CCM 1	D < 0.5	1, 0, V_{out}	3, V_{out}, V_{out}	5, V_{out}, 0	3, V_{out}, V_{out}		
2L DCM 1	D < 0.5	1, 0, V_{out}	2, 0, OC	8, V_{out}, OC	5, V_{out}, 0	4, OC, 0	6, OC, V_{out}
2L DCM 2	D < 0.5	2, 0, OC	8, V_{out}, OC	9, OC, OC	4, OC, 0	6, OC, V_{out}	9, OC, OC
2L CCM 2	D > 0.5	7, 0, 0	1, 0, V_{out}	7, 0, 0	5, V_{out}, 0		
2L DCM 3	D > 0.5	7, 0, 0	1, 0, V_{out}	2, 0, OC	7, 0, 0	5, V_{out}, 0	4, OC, 0

Table 2.2. Sub-modes of operation and quad-state Y solutions for a CL interleaved boost converter.

SM, Y1, Y2		D1	D2	D3	D4	D5	D6	D7	D8	D9	D10
CCM 1	D < 0.5	1, 0, V_{out}	3, V_{out}, V_{out}	5, V_{out}, 0	3, V_{out}, V_{out}						
DCM 1	D < 0.5	1, 0, V_{out}	3, V_{out}, V_{out}	8, V_{out}, OC	5, V_{out}, 0	3, V_{out}, V_{out}	6, OC, V_{out}				
DCM 2	D < 0.5	1,0, V_{out}	3, V_{out}, V_{out}	8, V_{out}, OC	9, OC, OC	5, V_{out}, 0	3, V_{out}, V_{out}	6, OC, V_{out}	9, OC, OC		
DCM 3	D < 0.5	1, 0, V_{out}	2, 0, OC	8, V_{out}, OC	5, V_{out}, 0	4, OC, 0	6, OC, V_{out}				
DCM 4	D < 0.5	2, 0, OC	8, V_{out}, OC	9, OC, OC	4, OC, 0	6, OC, V_{out}	9, OC, OC				
DCM 5	D < 0.5	12, D_L, V_{out}	12, D_L, V_{out}	13, D_L, OC	2, 0, OC	10, V_{out}, D_L	10, V_{out}, D_L	11, OC, D_L	4, OC, 0		
DCM 6	D < 0.5	6, OC, V_{out}	2, 0, OC	8, V_{out}, OC	8, V_{out}, OC	4, OC, 0	6, OC, V_{out}				
DCM 7	D < 0.5	2, 0, OC	10, V_{out}, D_L	11, OC, D_L	9, OC, OC	4, OC, 0	12, D_L, V_{out}	13, D_L, OC	9, OC, OC		
CCM 2	D > 0.5	7, 0, 0	1, 0, V_{out}	7, 0, 0	5, V_{out}, 0						
DCM 8	D > 0.5	7, 0, 0	1, 0, V_{out}	2, 0, OC	7, 0, 0	5, V_{out}, 0	4, OC, 0				
DCM 9	D > 0.5	7, 0, 0	1, 0, V_{out}	12, D_L, V_{out}	13, D_L, OC	5, 0, OC	7, 0, 0	5, V_{out}, 0	10, V_{out}, D_L	11, OC, D_L	4, OC, 0
DCM 10	D > 0.5	7, 0, 0	1, 0, V_{out}	6, OC, V_{out}	2, 0, OC	7, 0, 0	5, V_{out}, 0	8, V_{out}, OC	4, OC, 0		

2.5 CCM Operation & CCM-DCM Boundary Conditions

As shown in Figure 2.12 to Figure 2.14, there are a total of twelve modes of operation; two in CCM and ten in DCM. The two CCM modes, CCM 1 and CCM 2, occur when the duty cycle is less than and greater than 0.5, respectively. The gain of the converter when operating in CCM is given by

$$\frac{V_{out}}{V_{in}} = \frac{1}{1-D} \tag{2.8}$$

Once again, as with the 1L and 2L converters, the gain of system does not depend on the current flowing through the converter. One of the major differences between a 2L converter and a CL converter is the shape of the boundary between CCM and DCM. As the currents in the converter phases drops, the inductor current will eventually reach zero and enter BCM. The boost converter is said to be operating in CCM when the phase current is, at all times, greater than zero, i.e.

$$i_{L1}(t) \text{ and } i_{L2}(t) > 0 \tag{2.9}$$

To ensure this condition, the converter must be designed so that the dc phase current, $I_{L(DC)}$, is always greater than half the value of the peak-to-peak phase ripple $\Delta I_{L(p\text{-}p)}$:

$$I_{L(DC)} > \frac{\Delta I_{L(p-p)}}{2} \tag{2.10}$$

The converter is said to be operating in DCM when the conditions of (2.9) and (2.10) are not met. In a coupled-inductor boost converter, the ripple currents in each phase are a combination of the input ripple current, which depends solely on the leakage inductance, and the magnetizing ripple-current component. To fully realize each phase current, the input and magnetizing ripple currents, as shown in Figure 2.7 (a) and Figure 2.13 (a) must first be analysed for CCM 1 and CCM 2, respectively. To quantify each ripple current, the voltage drop over the leakage inductance is found for both phases over the period D_1, where D_1 is the on-time of the switch, as done as follows for CCM 1:

$$V_{in} - V_{Llk1.1} - V_{T1.1} = 0 \tag{2.11}$$

$$V_{in} - V_{Llk2.1} - V_{T2.1} - V_{out} = 0 \tag{2.12}$$

where $V_{Llkx.y}$ equates to the voltage across the leakage inductance in phase x during the cycle time D_y, and $V_{Tx.y}$ equates to the voltage drop across the magnetizing inductance in phase x during the cycle time D_y. It is assumed that the current in phase 1 is the sum of the current in phase 2 and the magnetizing current, i_m. Hence, to find the magnetizing

ripple, (2.11) and (2.12) are subtracted from each other, and the following assumptions are applied:

$$\begin{gathered} D_1 = D_3 \\ D_2 = D_4 \\ V_{T1.1} = V_{T1.3} = -V_{T2.1} = -V_{T2.3} = L_m \frac{di_m}{dt} \\ V_{T1.2} = V_{T1.4} = V_{T2.2} = V_{T2.4} = 0 \end{gathered} \tag{2.13}$$

Thus,

$$L_{Lk} \frac{di_{L1}}{dt} + L_m \frac{di_m}{dt} - V_{out} + L_m \frac{di_m}{dt} - L_{Lk} \frac{di_{L2}}{dt} = 0 \tag{2.14}$$

Since it is assumed that

$$i_{L1} - i_{L2} = i_m \tag{2.15}$$

Then, simplifying (2.14) yields the peak-to-peak magnetizing current ripple $\Delta I_{m(p\text{-}p)}$:

$$\Delta I_{m(p-p)} = \frac{V_{out} D_1 T_s}{L_{Lk} + 2L_m} \tag{2.16}$$

In multiphase boost converters, the input current is the sum of the phase currents. Hence, to find the input current ripple, (2.11) and (2.12) are added together, and again (2.13) is applied yielding

$$V_{in} - V_{Llk1.1} - V_{T1.1} + V_{in} - V_{Llk2.1} + V_{T2.1} - V_{out} = 0 \tag{2.17}$$

Thus,

$$2V_{in} - V_{out} = L_{Lk} \frac{di_{L1}}{dt} + L_{lk} \frac{di_{L2}}{dt} \tag{2.18}$$

The input current is the sum of the two phase-currents

$$i_{L1} + i_{L2} = i_{in} \tag{2.19}$$

Hence, the peak-to-peak input ripple current $\Delta I_{in(p\text{-}p)}$ is

$$\Delta I_{in(p-p)} = \frac{V_{out}\left(1-2D_1\right)D_1}{L_{Lk}\left(1-D_1\right)} T_s \tag{2.20}$$

The phase current ripple is then found as

$$\Delta I_{L(p-p)} = \left| \frac{\Delta I_{in(p-p)}}{2} \right| + \left| \frac{\Delta I_{m(p-p)}}{2} \right| \tag{2.21}$$

As can be seen for CCM 1, the input current ripple is dependent only on the leakage inductance, and increasing the leakage inductance will decrease the input-current ripple. The phase-current ripple and magnetizing-current ripple are dependent on the leakage and magnetizing inductances. By following the same method for a duty cycle greater

than 0.5, the ripple currents for $D > 0.5$ can be found. To find the boundary between CCM and DCM, half the peak-to-peak phase current ripple is equated to the dc phase current, i.e.

$$\frac{\Delta I_{L(p-p)}}{2} = I_{L(DC)} \tag{2.22}$$

Hence, the following boundary conditions are obtained.

$$\begin{aligned} \frac{\Delta I_{L(p-p)}}{2} < I_{L(DC)} &\rightarrow \text{CCM} \\ \frac{\Delta I_{L(p-p)}}{2} > I_{L(DC)} &\rightarrow \text{DCM} \end{aligned} \tag{2.23}$$

Table 2.3 provides the solutions to the peak-to-peak input current ripple, magnetizing current ripple and phase current ripple for the CL boost converter operating in CCM.

Table 2.3. Peak-to-peak ripple currents for the input, magnetizing and phase currents of a CL boost converter when operating in CCM.

CCM Mode	$\Delta I_{in(p\text{-}p)}$	$\Delta I_{m(p\text{-}p)}$	$\Delta I_{L(p\text{-}p)}$
CCM 1 (D < 0.5)	$\frac{V_{out}D(1-2D)T_s}{L_{lk}}$	$\frac{V_{out}DT_s}{L_{Lk}+2L_m}$	$\frac{\Delta I_{in(p-p)}}{2}+\frac{\Delta I_{\mathrm{m}(p-p)}}{2}$
CCM 2 (D > 0.5)	$\frac{V_{in}(2D-1)T_s}{L_{Lk}}$	$\frac{V_{in}T_s}{L_{Lk}+2L_m}$	$\frac{\Delta I_{in(p-p)}}{2}+\frac{\Delta I_{\mathrm{m}(p-p)}}{2}$

2.6 DCM Characteristics

The following section provides a sample analysis of two CL boost converter DCM modes; DCM 4 and DCM 9. The characteristics of both modes are developed, as well as boundary conditions between the modes and another mode of operation.

2.6.1 DCM 4

Due to its simplicity and its similarities to a two-phase boost converter, DCM 4 will be analysed first.

2.6.1.1 DCM 4 Characteristics

To find the duty cycle of the converter in DCM 4, the voltage drop across the leakage inductance of one phase is taken over the whole cycle period.

$$V_{Llk1.1} = V_{in} - V_{T1.1} \tag{2.24}$$

$$V_{Llk1.2} = V_{in} - V_{T1.2} - V_{out} \tag{2.25}$$

$$V_{Llk1.3} = 0 \tag{2.26}$$

$$V_{Llk1.4} = 0 \tag{2.27}$$

By applying the volt-second balance to the leakage inductance, the following equation is found

$$D_1 V_{in} + D_{off} V_{in} - D_{off} V_{out} = 0 \tag{2.28}$$

Next, the peak of the phase current is found as

$$\Delta I_{L(p-p)} = \frac{V_{in} D_{off} T_s}{L_{Lk} + L_m} \tag{2.29}$$

By averaging the peak over the full cycle time, the dc phase current is found, i.e.

$$I_{L1} = \frac{\Delta I_{L(p-p)} (D + D_{off})}{2} \tag{2.30}$$

Finding Equation (2.30) in terms of D_{off} gives

$$D_{off} = \frac{2 I_{L1} (L_{Lk} + L_m) - V_{in} D^2 T_s}{V_{in} D T_s} \tag{2.31}$$

Inserting equation (2.31) into (2.28) and isolating for D gives

$$D_1 = \sqrt{\frac{2 I_{L1} (V_{out} - V_{in})(L_{Lk} + L_m)}{V_{out} V_{in} T_s}} \tag{2.32}$$

Knowing D_1, the other circuit parameters can be determined. This allows for the complete characterisation of DCM 4.

2.6.1.2 DCM 3/DCM 4 Boundary

One of the modes that DCM 4 shares a boundary with is DCM 3. In order to find the boundary conditions of these modes, the inductor current waveforms of both modes must be compared. These waveforms are presented in Figure 2.17.

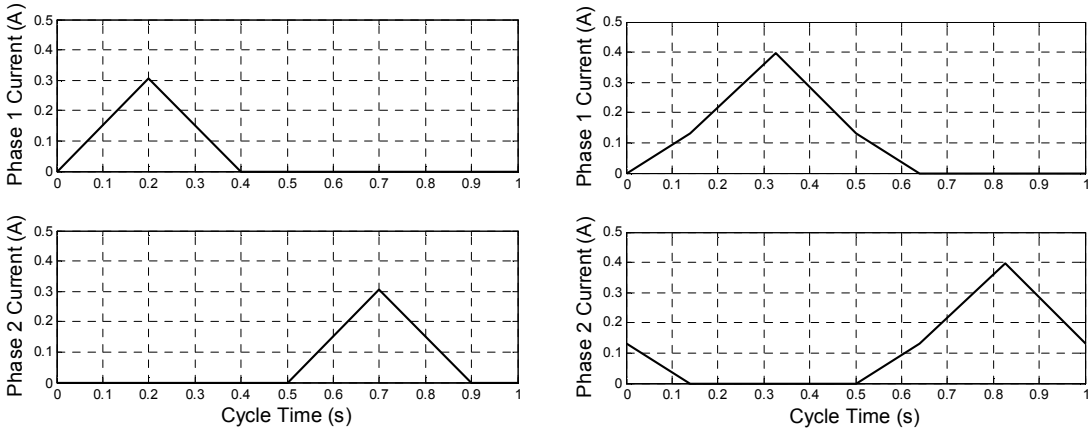


Figure 2.17. Phase current waveforms of (a) DCM 4 and (b) DCM 3.

As can be seen from the DCM 4 waveforms in Figure 2.17 (a), the current in phase 1 stops flowing before the current in phase 2 begins. However, as the duty cycle increases, so does the amount of time that current flows in phase 1. At a certain point, the current in phase 2 will begin to rise before the current in phase 1 ceases to flow. It is at this point that the converter enters DCM 3, as shown in Figure 2.17 (b). Hence, the boundary between DCM 3 and DCM 4 depends on the values of D and D_{off} of DCM 4 i.e.

$$\begin{aligned} D_{(DCM\,4)} + D_{off\,(DCM\,4)} &< 0.5 \rightarrow \text{DCM 4} \\ D_{(DCM\,4)} + D_{off\,(DCM\,4)} &> 0.5 \rightarrow \text{DCM 3} \end{aligned} \tag{2.33}$$

2.6.2 DCM 9

Due to its complicated phase current waveform, DCM 9, shown in Figure 2.18, is one the more difficult modes of operation to characterise. Hence, by covering this mode of operation along with the earlier analysis of DCM 4, the all analytical tools needed to solve DCM operation are presented and can easily be applied to all other modes of operation.

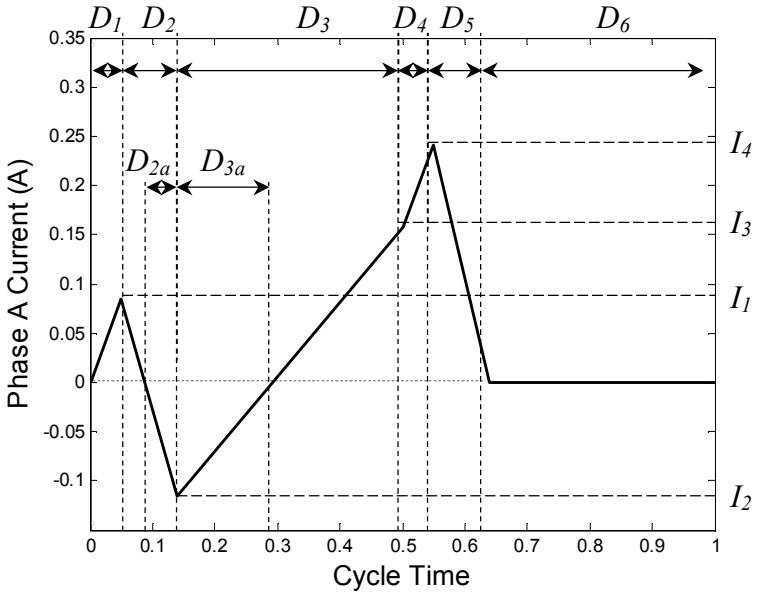


Figure 2.18. Phase current of DCM 9.

2.6.2.1 DCM 9 Characteristics

To correctly analyse DCM 9, the negative portion of the phase current must be taken into consideration. Hence, the cycle times D_2 and D_3 must be dismantled into parts. The values of I_1, I_2, I_3 and I_4 in Figure 2.18 must also be found. By analysing the phase, input and magnetising currents using the method presented in Section 2.2, it is found that

$$I_1 = \frac{2V_{in}(D-0.5)T_s}{L_{Lk}} \tag{2.34}$$

$$I_2 = I_1 - \frac{(V_{out}-2V_{in})D_{off}T_s}{2L_{Lk}} - \frac{V_{out}D_{off}T}{2(L_{Lk}+2L_m)} \tag{2.35}$$

$$I_3 = I_2 + \frac{V_{in}(1-D-D_{off})T_s}{(L_{Lk}+L_m)} \tag{2.36}$$

$$I_4 = I_1 + I_3 \tag{2.37}$$

and using basic trigonometry, D_2 and D_3 are dismantled into D_{2a} and D_{3a} as shown in Figure 2.18 and found to be

$$D_{2a} = D_{off}\left(1 - \frac{I_1}{I_1 - I_2}\right) \tag{2.38}$$

$$D_{3a} = \frac{(1-D-D_{off})I_2}{I_2 - I_3} \tag{2.39}$$

By using Equations (2.34) to (2.39), the dc phase current of DCM 9 is found to be

$$I_{L1} = \begin{bmatrix} V_{in}(D^2 L_T{}^2 - DL_m L_T) + D_{off}{}^2 L_T(L_{Lk}(V_{out}-V_{in}) + \\ L_m(V_{out}-2V_{in})) + D_{off}L_m(V_{in}L_T - V_{out}L_S) \end{bmatrix} \frac{T_s}{2L_{Lk}L_S L_T} \tag{2.40}$$

where

$$L_T = L_{Lk} + 2L_m \tag{2.41}$$

and

$$L_S = L_{Lk} + L_m \tag{2.42}$$

The voltage drop across the leakage inductance during DCM 9 is

$$V_{Llk} = V_{in}(D + D_{off}) - V_{out}D_{off} - V_{T1} = 0 \tag{2.43}$$

By analysing the magnetizing current of DCM 9 in Figure 2.18, V_{T1} is found as

$$V_{T1} = \frac{L_m V_{in}(1 - D - D_{off})}{L_S} \tag{2.44}$$

Hence

$$V_{in}(D + D_{off}) - V_{out}D_{off} - \frac{L_m V_{in}(1 - D - D_{off})}{L_S} = 0 \tag{2.45}$$

Equations (2.40) and (2.45) are considered to be a set of simultaneous equations used to find the two unknowns D and D_{off}. This concludes the large-signal modeling of DCM 9. The simultaneous equations for each DCM mode of operation are presented in the appendix, as well as the solutions to D and D_{off}.

2.6.2.2 DCM8/DCM9 Boundary

As with the boundary between DCM 3 and DCM 4, the phase currents of DCM 8 and DCM 9 need to be analysed in order to find the boundary between the two. The waveforms of these modes are presented in Figure 2.19.

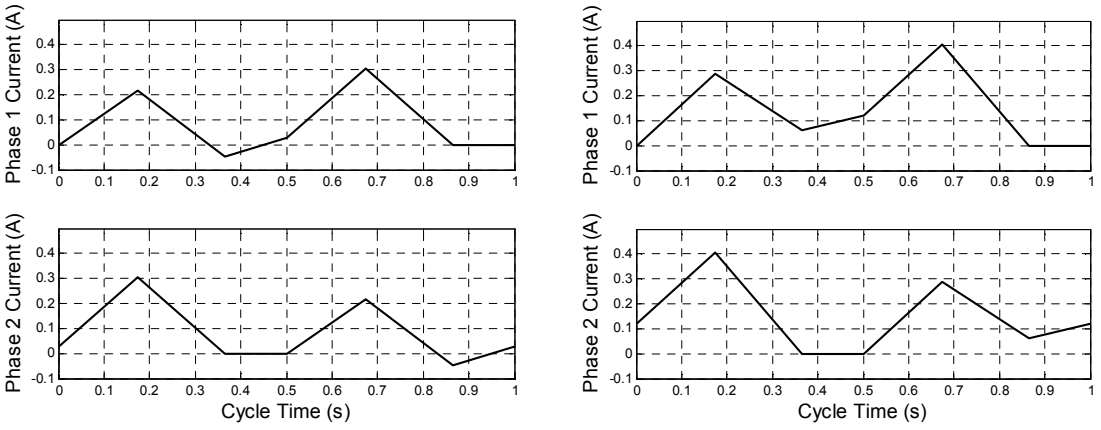


Figure 2.19. Phase current waveforms of (a) DCM 9 and (b) DCM 8.

One of the main differences between DCM 8 and DCM 9 is the fact that, for a small portion of the cycle time, the current begins to flow negatively in DCM 9. This is due to the fact that the fall in current during the cycle time D_2 of DCM 9 is greater than the rise in current during the cycle time D_1 of DCM 9, as seen in Figure 2.19 (a). When

operating in DCM 8, the opposite is true, as shown in Figure 2.19 (b). Hence, the boundary between DCM 8 and DCM 9 is decided via the following condition.

$$\begin{aligned} \Delta I_{L(D2)DCM8} < \Delta I_{L(D1)DCM8} &\rightarrow \text{DCM 8} \\ \Delta I_{L(D2)DCM8} > \Delta I_{L(D1)DCM8} &\rightarrow \text{DCM 9} \end{aligned} \tag{2.46}$$

2.6.3 Modal Boundary Flowchart

Due to the many modes of operation in DCM, a boundary condition for each border must be developed. The flow chart presented in Figure 2.20 has been developed to document each of these boundary conditions. When applying the flow chart, the direction of the arrow indicates the inequality symbol of the boundary condition to be used. An explanation for each condition is also presented. To find the boundary between DCM 2 and DCM 4, the waveform of DCM 2 must be analysed. The key difference between both waveforms is the presence of the coupling of the waveforms in DCM 2 compared to the lack of coupling in DCM 4. This coupling causes a rise in current during the cycle time D_5 which is not observed in DCM 4. Hence, by letting the formula for this rise in current equate to zero and simplifying, the boundary between both modes is found. Applying this method also yields the boundary between DCM 3 and DCM 5/6. In DCM 3, the initial change in current is to flow in the positive direction, whereas in DCM 5, it flows in the negative direction. In the case of DCM 6, it does not flow at all. Hence, by letting the formula for this initial rise in current in DCM 3 equate to zero and simplifying, the boundary between these two regions is obtained.

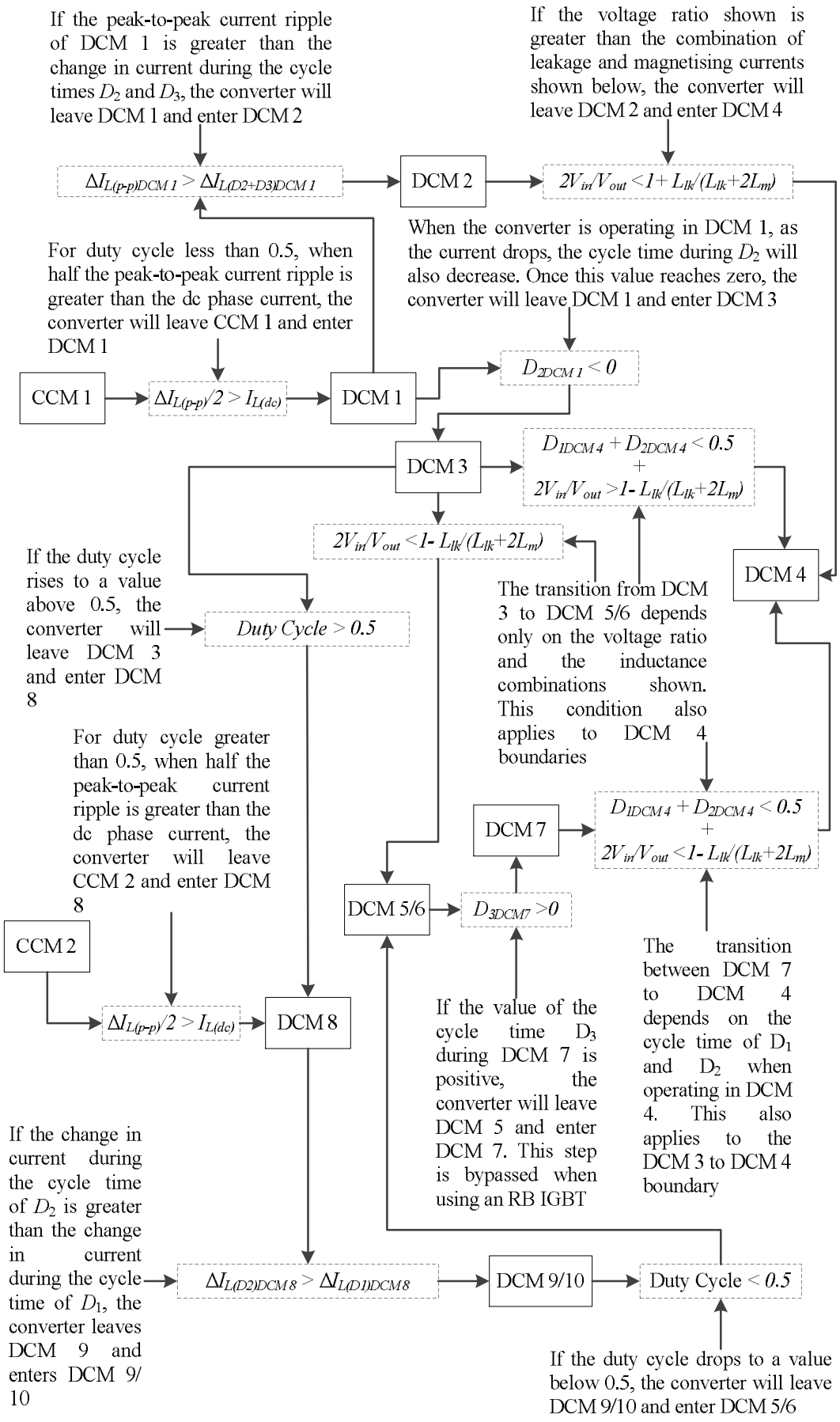


Figure 2.20. CCM-DCM mode map boundary conditions for the CL boost converter.

2.7 CL Boost Converter CCM-DCM Mode Maps

With the solution of the characteristics and boundaries of each mode of operation of the CL converter, the CCM-DCM mode maps can now be developed. The mode maps of the CL converter with are plotted in Figure 2.21, Figure 2.22 and Figure 2.23 for the output current, RMS phase current and input dc current, respectively. As with the 1L and 2L, the currents on the *x*-axis are normalised to the maximum output boundary current, which is derived as follows.

The boundary between CCM and DCM occurs when the peak-to-peak ripple of the phase current reaches zero for an instant. At this point, the dc phase current is equal to half the peak-to-peak phase ripple i.e.

$$I_{L1B} = \frac{\Delta I_{L(p-p)}}{2} \tag{2.47}$$

where I_{L1B} is the phase current when the converter is in BCM. The dc phase current is related to the dc output current by the relationship

$$I_{L1B} = \frac{I_{oB}}{2(1-D)} \tag{2.48}$$

where I_{oB} is the output current when the converter is in BCM. Hence, by inserting equation (2.47) into (2.48), it is found that

$$I_{oB} = \Delta I_{L(p-p)}(1-D) \tag{2.49}$$

The expression for the peak-to-peak phase current ripple in a CL boost converter, which is derived in Section 2.5, is dependent on whether the duty cycle is less than or greater than 0.5. From Figure 2.21, it is evident that the maximum output boundary current occurs at a duty cycle of $0.2\dot{3}$, which is less than 0.5. Section 2.5 derives the expression for the peak-to-peak phase current ripple, which is found as

$$\Delta I_{L(p-p)} = \frac{V_{out}\left(1-2D_1\right)D_1T_s}{2L_{Lk}\left(1-D_1\right)} + \frac{V_{out}D_1T_s}{2(L_{Lk}+2L_m)} \tag{2.50}$$

By inserting 0.23 in for the duty cycle and simplifying, the maximum output boundary current is found as

$$I_{oB,Max} = 0.115V_{out}T_s\left(\frac{0.696}{2L_{Lk}} + \frac{1}{2(L_{Lk}+2L_m)}\right) \text{ for } D = 0.2\dot{3} \tag{2.51}$$

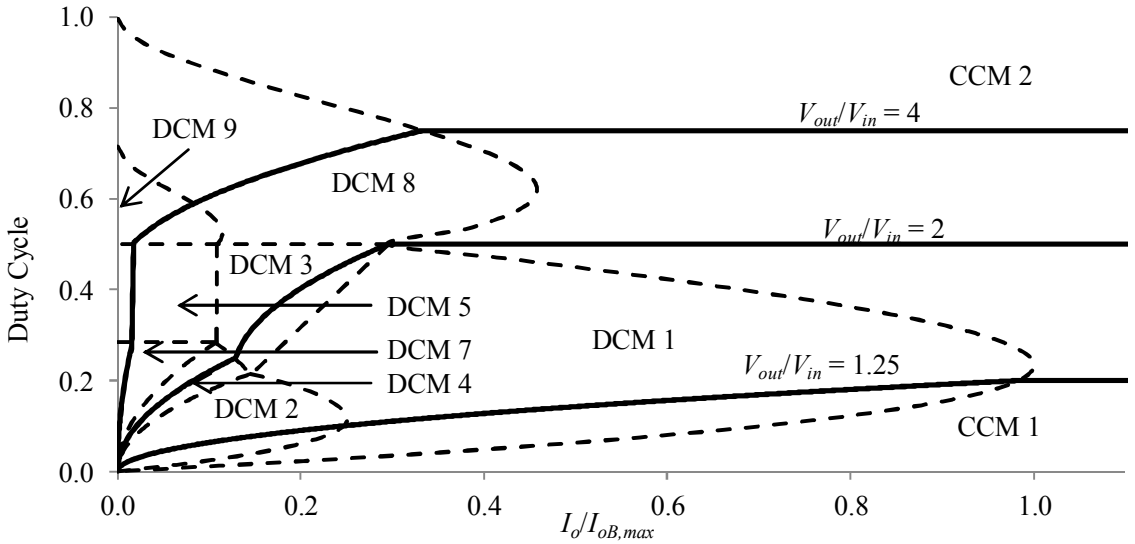


Figure 2.21. Output current CCM-DCM mode map for CL boost converter.

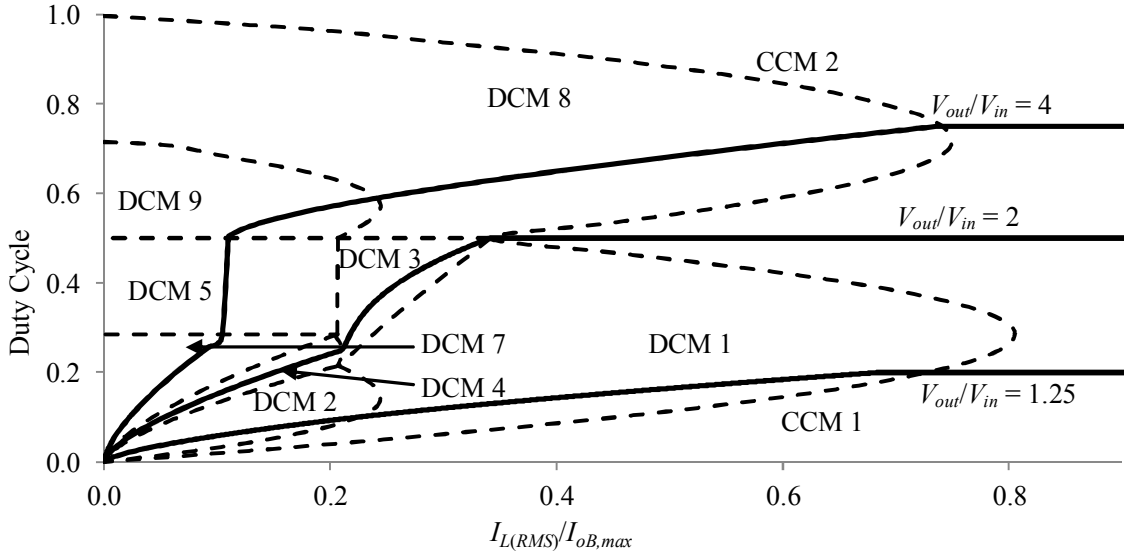


Figure 2.22. RMS phase current CCM-DCM mode map for CL boost converter.

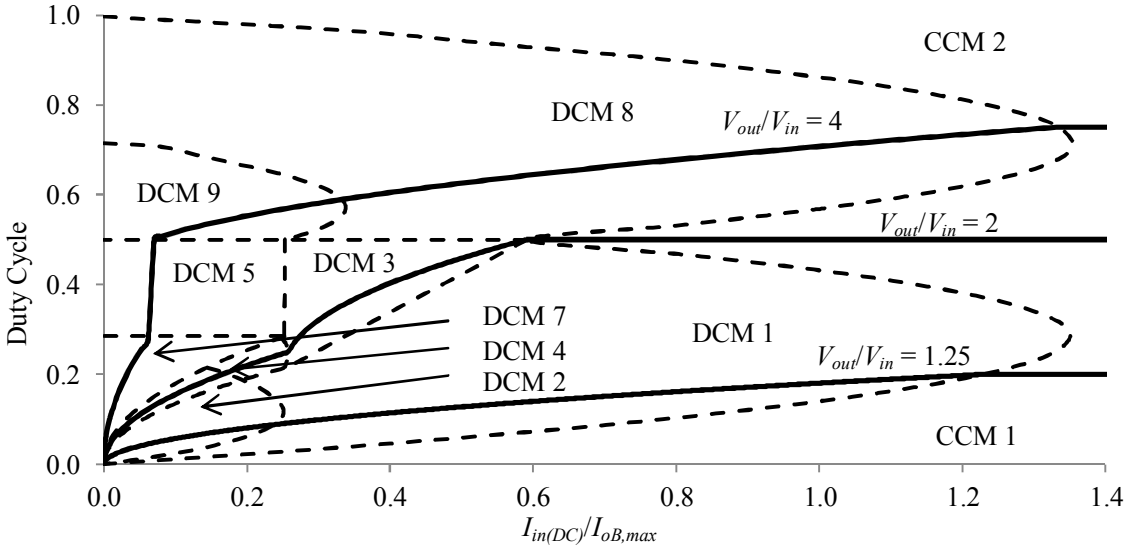


Figure 2.23. Input current CCM-DCM mode maps for CL boost converter.

There are a number of key points to note on these figures. Firstly, the circuit stresses are highest for the 2L at a duty cycle of 0.5, for example, switch turn-off and diode turn-on occur at the highest possible currents. On the other hand, this 0.5 duty cycle is very low stress for the CL boost, while the CL boost can have relatively high phase currents at lower and higher duty cycles. Another key point is that, while the three DCM modes in the 2L converter all have the same gain, the same cannot be said for the CL converter. A converter gain for each DCM mode must be derived. Hence, the gain of one DCM mode will not give the correct value when used in another DCM mode.

As can be seen from Figure 2.13 and Figure 2.14, current briefly flows in the negative direction in three of the DCM modes, DCM 5, DCM 7, and DCM 9. This is achieved by the current flowing backwards through the switch via the freewheeling diode. If the reverse flow of current in the lower switch is blocked, e.g. by a series-blocking diode or the use of a unidirectional switch as shown in Figure 2.24, two new modes, DCM 6 and DCM 10, replace DCM 5 and DCM 7. Therefore, a new mode map with new boundaries must be developed. This mode map is presented in Figure 2.25.

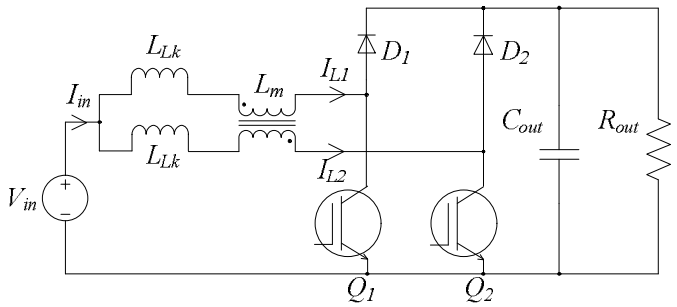


Figure 2.24. The two-phase coupled-inductor boost converter with unidirectional switch.

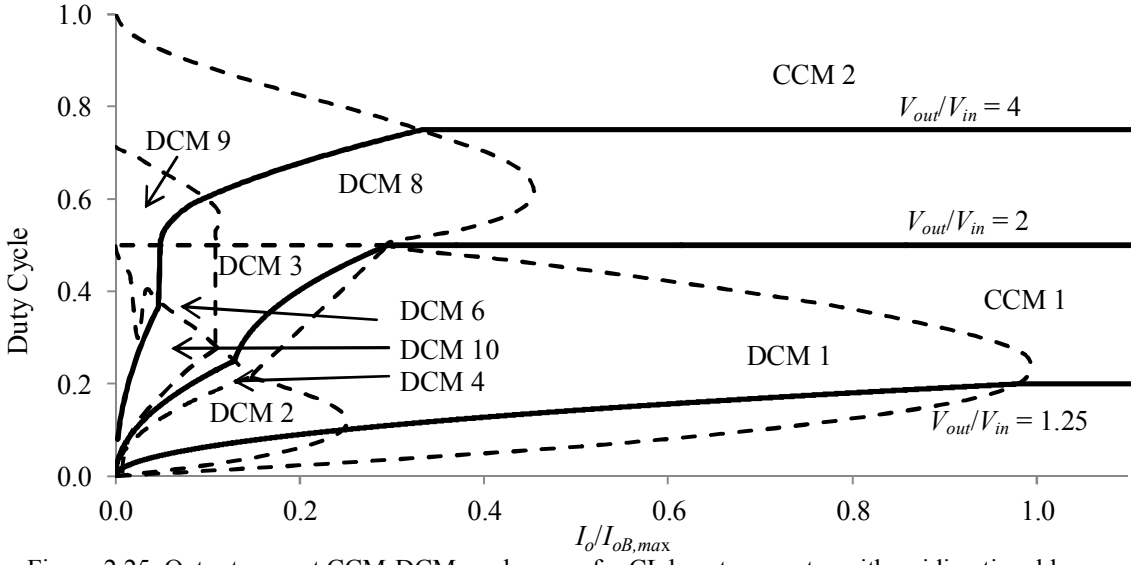


Figure 2.25. Output current CCM-DCM mode maps for CL boost converter with unidirectional lower switch e.g. IGBT.

2.7.1 Effect of Inductance Coupling Factor

When designing a coupled-inductor for a dc-dc converter, one of the major considerations is the coupling factor between the leakage and magnetising inductance. To demonstrate the effect of the coupling factor, the output current mode map of a CL boost converter for different coupling factors are presented in Figure 2.26. It should be noted that the mode maps presented in Figure 2.26 are normalised to the same maximum output boundary current. This is to allow a like-for-like comparison.

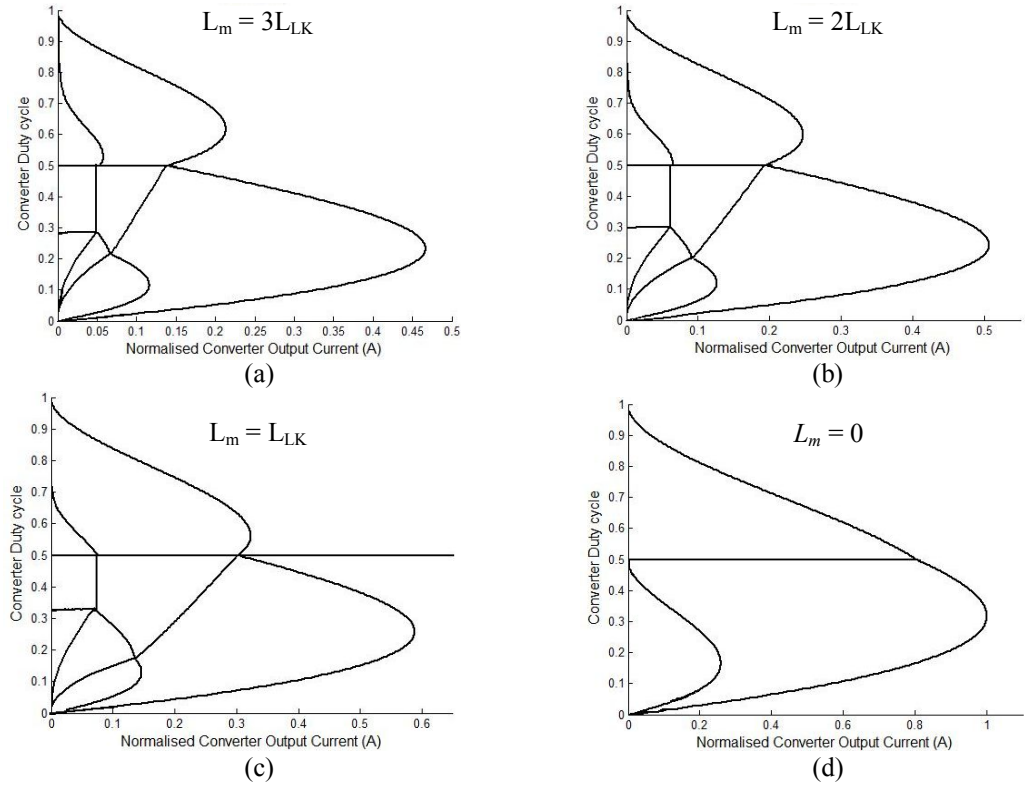


Figure 2.26. CCM-DCM mode maps of a CL boost converter where (a) $L_{Lk} = 3L_m$, (b), $L_m = 2\ L_{Lk}$, (c) $L_m = L_{Lk}$ and (d), $L_m = 0$.

As can be seen from Figure 2.26, as the magnetising inductance of the converter decreases, the mode map transforms more and more into the mode map of a 2L converter. However, the boundary currents between CCM and DCM, and between each DCM mode increase dramatically.

2.7.2 72 kW Design Example

In chapter 1, a design example of a 72 kW coupled-inductor for use in a boost converter was presented. By creating a CCM-DCM mode map for the 72 kW converter, designers can now easily anticipate the modes of operation the converter will enter over the full load range. As can be seen from the converters mode map, presented in Figure 2.27, the converter operates in CCM 2 up to approximately 30 kW. At this point, the converter enters CCM 1. As power continues to drop to approximately 25 kW, the

converter enters DCM 1, the first DCM mode to be encountered. Finally, at 10 kW and below, the converter enters DCM 2.

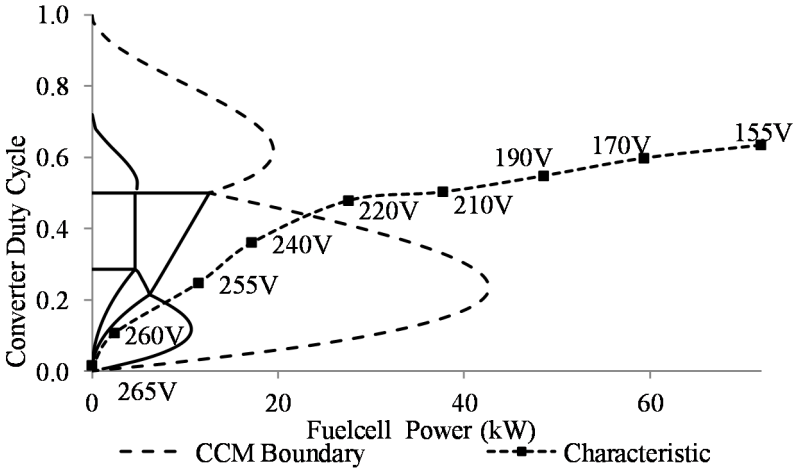


Figure 2.27. CCM-DCM operating mode map for 72 kW CL boost converter.

2.8 Design of 1 kW Two-Phase Interleaved Coupled-Inductor Boost Converter

In order to test the validity of the large signal model, a 1 kW CL boost converter prototype was developed. Due to laboratory constraints, the maximum power available for testing is 1.2 kW. The maximum voltage and current ratings available are 500 V and 25 A respectively. Hence, the rated voltage of the converter was designed to be 450 V, with a full-load current of 2.5 A.

Several assumptions were made during the design of the converter. The first assumption is that the converter will operate at a fixed PWM switching frequency throughout all testing. The advantages of fixed-frequency include a simpler controller design and implementation. When operating in DCM, a converter often utilises variable-frequency control, in order to increase the on time of the switch, and in turn, reduce harmonics. Due to the fact that the purpose of the 1 kW prototype is to investigate the large-signal and small-signal model of each CCM and DCM mode, the implementation of variable-frequency control is not considered.

The next assumption is that the converter be able to operate bi-directionally i.e. step-up the voltage in one direction, and step-down the voltage in the opposite direction. Hence, all components are rated at 500 V minimum. This is to ensure that, whether the converter is in buck mode or boost mode, failure in any one component would not cause damage to others. However, the buck function was not utilised. Hence, only two MOSFETs and two diodes were implemented.

The final assumption made during the design of the converter was the different input voltage levels. Three different input voltage values were chosen in order to ensure that all DCM modes were encountered with as little variation as possible. Hence, the three different input voltage levels were set as 150 V, 225 V, and 300 V.

In order to fully test all modes of operation of a CL boost converter, the area of each mode was maximised by selecting appropriate values of leakage inductance, magnetising inductance, and switching frequency. For example, if the switching frequency and inductances of the system were too low, the peak-to-peak inductor current ripple would be too high for the converter to operate in CCM at a power below the rated power level. However, if the values of frequency and inductances were too high, then there would be very little room to operate in many of the DCM modes, especially the modes that occur at low power. Hence, a leakage inductance of 335 μH, a magnetising inductance of 1 mH, and a switching frequency of 16 kHz were chosen.

The mode map of the 1 kW prototype CL boost converter is presented in Figure 2.28. As can be seen from the mode map, the area of each CCM and DCM mode is now large enough to accommodate experimental testing using a large range of parameters.

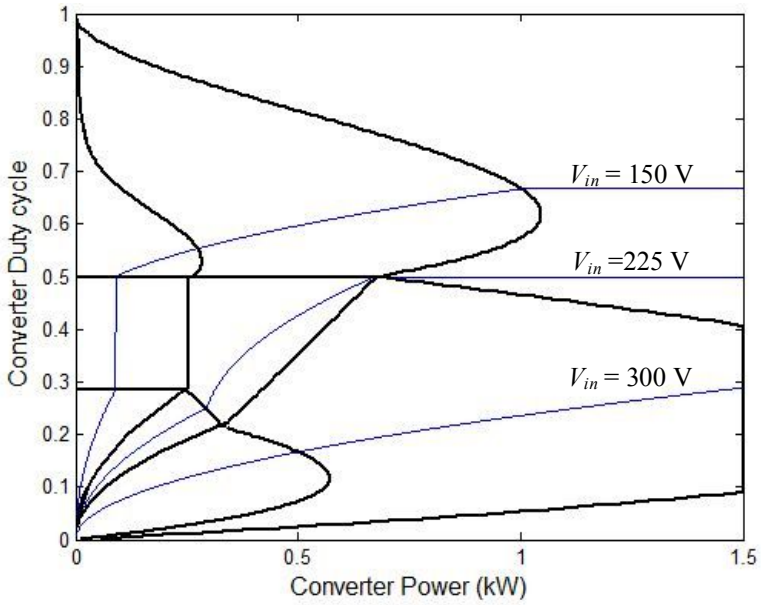


Figure 2.28. 1 kW CL boost converter CCM-DCM mode map.

The semiconductors chosen for the prototype are the Infineon CoolMOS MOSFET (IPW60R075CPA [2.33]) and the Cree Silicon Carbide (Sic) Schottky diode (CVFD20065A [2.34]). The high current ratings of both components are desired due to the fact that this prototype is for testing circuit operation theories, and as such, must be capable of handling high current levels, should anything unexpected occur. With the components designed, the 1 kW converter was developed, and is presented in Figure 2.29. The coupled-inductor utilised in this design is the CCTT integrated magnetic, presented in Figure 2.30. A set of eight 440 µF electrolytic capacitor are connected in series and parallel to give approximately 900 µF of capacitance for the output filter, presented in Figure 2.31. This is to ensure that the output power of the converter is clean, and does not damage the dc electronic load.

The phase currents of the converter are measured by the ABB EL 25 P Hall Effect sensor [2.35], while the input and output voltages are measured by the LEM LV25-p [2.36]. Both are presented in Figure 2.32. Finally, the converter is controlled by the Altera Cyclone III FPGA [2.37], presented in Figure 2.33. The small sampling time of the FPGA allows controllers to be designed in the analogue domain, and accurately emulated into the digital domain for digital implementation. Once developed, the converter efficiency was tested at an input voltage of 150 V at full load, and found to be 97.5%.

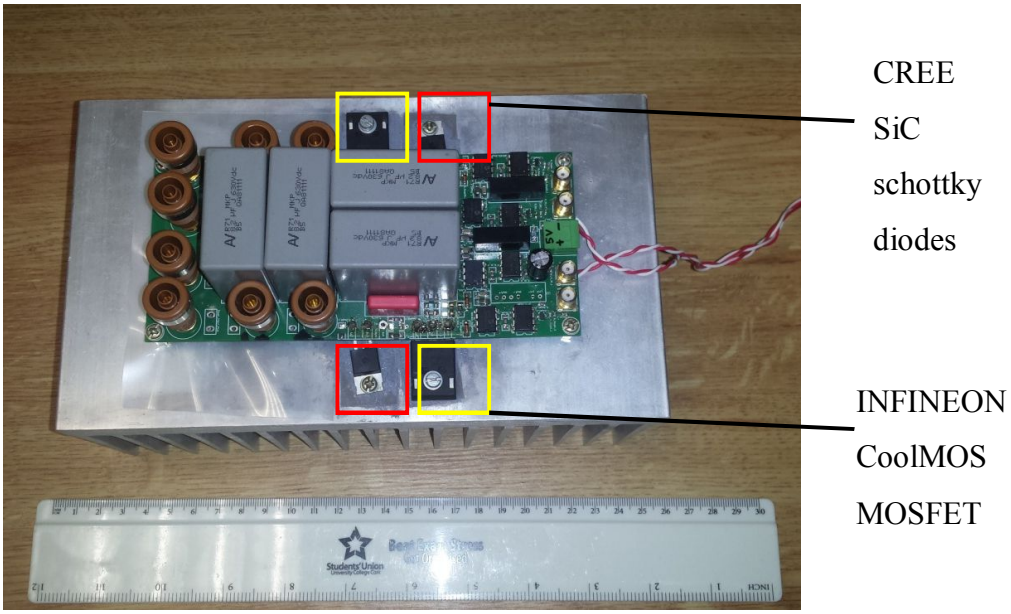


Figure 2.29. The two-phase interleaved coupled-inductor boost converter.

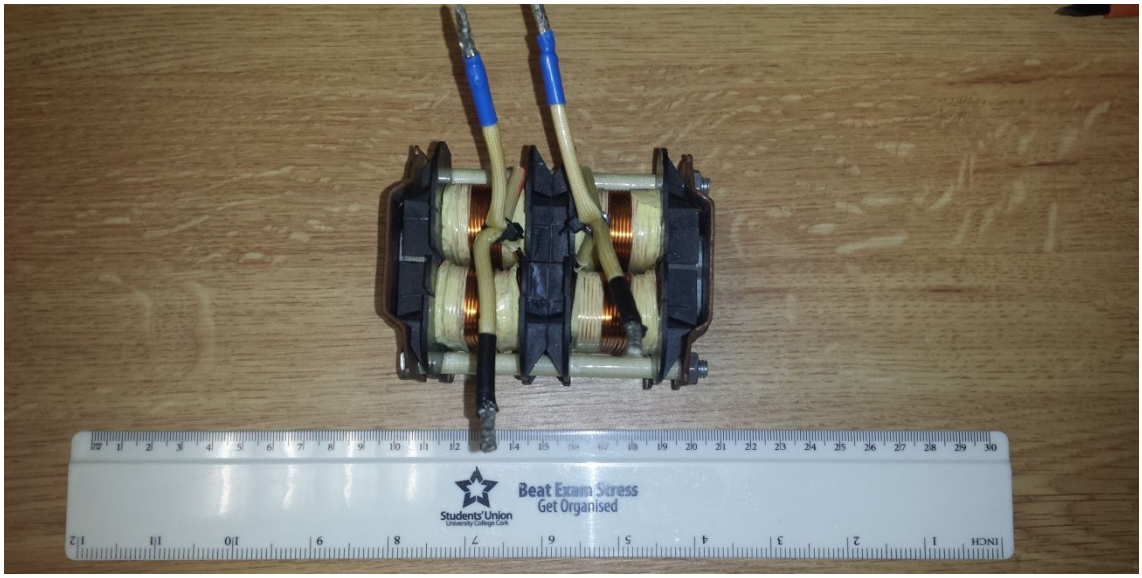


Figure 2.30. The CCTT integrated magnetic.

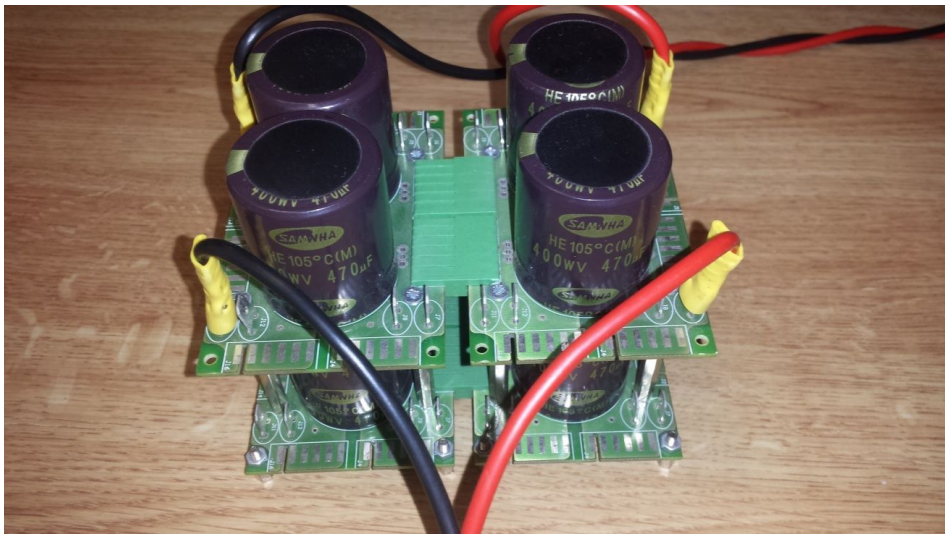


Figure 2.31. The converter output capacitor

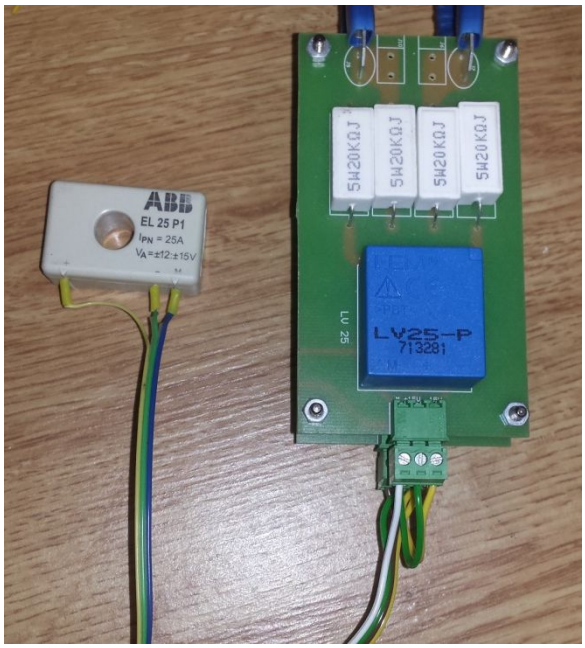


Figure 2.32. The current and voltage sensors utilised in the 1 kW prototype.

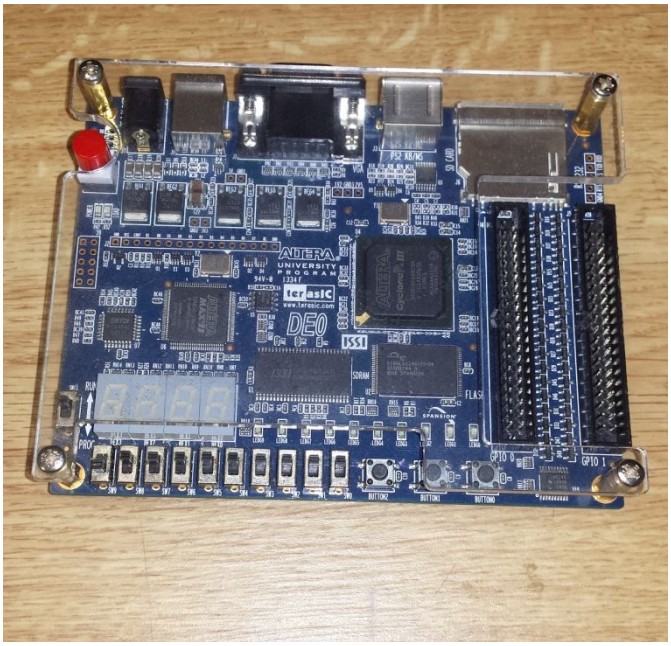


Figure 2.33. The Altera cyclone III FPGA.

2.9 Experimental Results

Initial experimental results from the 1 kW CL boost converter prototype are presented below. The following parameters are used to test the different modes of the circuit: V_{in} = 50-275 V, V_{out} = 300 V, P_{out} = 40 W – 750 W, L_{Lk} = 335 µH, L_m = 1 mH, T_s = 62.5 µs. Figure 2.34 to Figure 2.45 show the experimental waveforms obtained during testing. The green waveform is the pole output voltage of phase 1, i.e. the voltage across the switch Q_1, V_{Q1}, and the blue and purple waveforms are the current waveforms of phase 1 and phase 2, respectively. Realization of unidirectional DCM 6 and DCM 10 was initially attempted with an IGBT with no inverse diode. However, per the device specification (IRG4PC40K) [2.28], the IGBT experienced reverse breakdown as shown in Figure 2.46 and Figure 2.47. A series-blocking diode was subsequently required to realize DCM 6 and DCM 10. This issue can be more cleanly resolved by using the reverse-biased IGBT technology used in matrix converters from suppliers such as Fuji or IXYS. As can be seen from Figure 2.34 to Figure 2.45, all CCM and DCM modes of the CL converter are verified to exist.

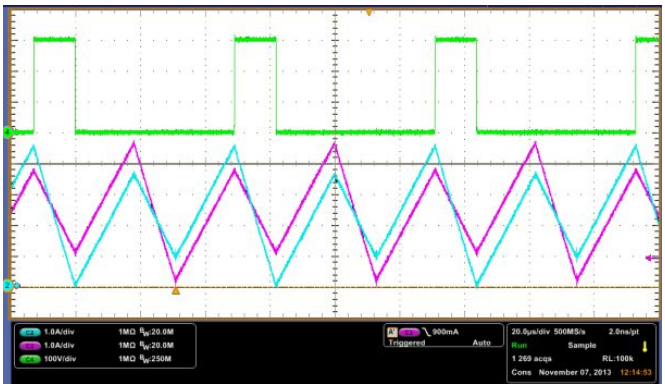


Figure 2.34. Experimental waveforms of CCM 2. The Q1 voltage (green) is 100V/div, while the phase 1 current (blue) and phase 2 current (purple) are 1A/div each.

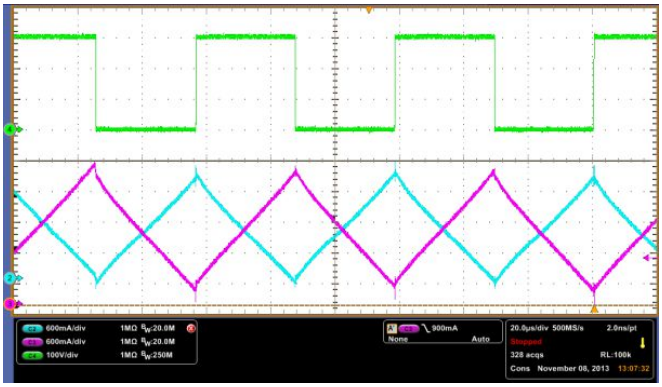


Figure 2.35. Experimental waveforms of D = 0.5 in CCM. The Q1 voltage (green) is 100 V/div, while the phase 1 current (blue) and phase 2 current (purple) are 600 mA/div each.

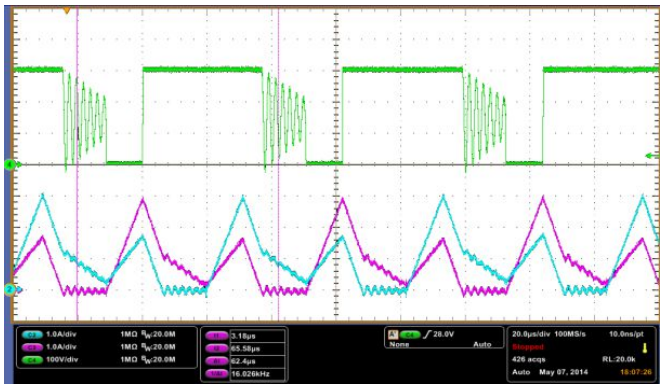


Figure 2.36. Experimental waveforms of DCM 1. The Q1 voltage (green) is 100 V/div, while the phase 1 current (blue) and phase 2 current (purple) are 1 A/div each.

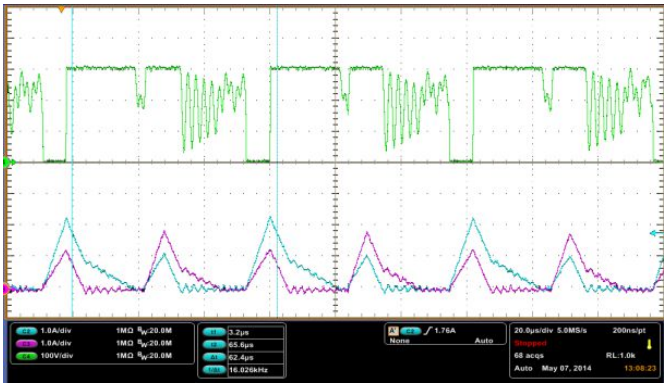


Figure 2.37. Experimental waveforms of DCM 2. The Q1 voltage (green) is 100 V/div, while the phase 1 current (blue) and phase 2 current (purple) are 1 A/div each.

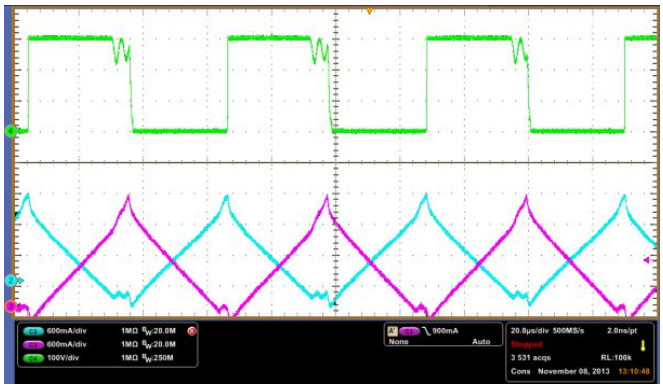


Figure 2.38. Experimental waveforms of DCM 3. The Q1 voltage (green) is 100 V/div, while the phase 1 current (blue) and phase 2 current (purple) are 600 mA/div each.

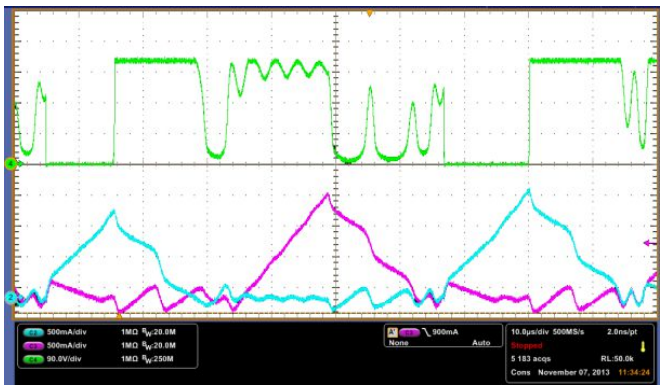


Figure 2.39. Experimental waveforms of DCM 4. Q1 voltage (green) is 100V/div, while the phase 1 current (blue) and phase 2 current (purple) are 500 mA/div each.

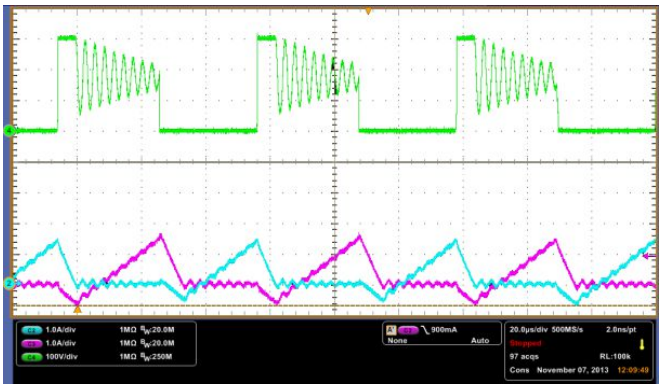


Figure 2.40. Experimental waveforms of DCM 5. The Q1 voltage (green) is 100 V/div, while the phase 1 current (blue) and phase 2 current (purple) are 1 A/div each.

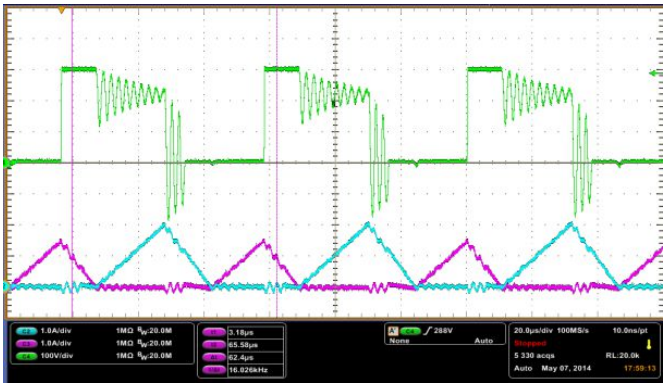


Figure 2.41. Experimental waveforms of DCM 6. The Q1 voltage (green) is 100 V/div, while the phase 1 current (blue) and phase 2 current (purple) are 1 A/div each.

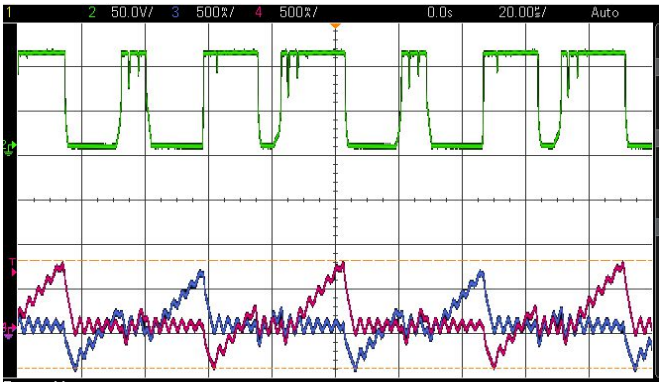


Figure 2.42. Experimental waveforms of DCM 7. The Q1 voltage (green) is 50 V/div, while the phase 1 current (blue) and phase 2 current (purple) are 500 mA/div each.

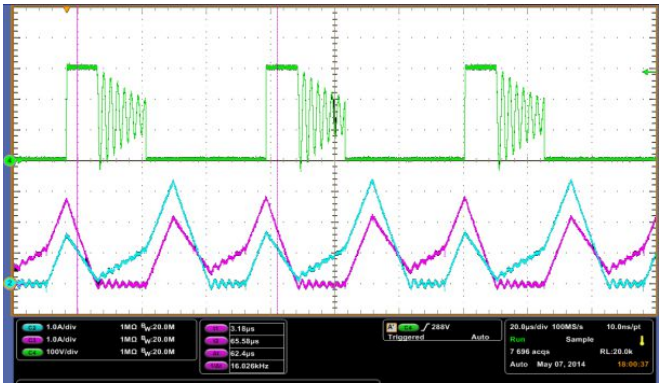


Figure 2.43. Experimental waveforms of DCM 8. The Q1 voltage (green) is 100 V/div, while the phase 1 current (purple) and phase 2 current (blue) are 1 A/div each.

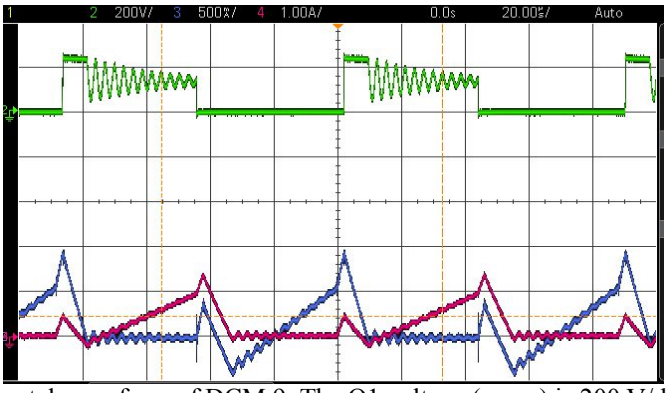


Figure 2.44. Experimental waveform of DCM 9. The Q1 voltage (green) is 200 V/div, while the phase 1 current (blue) and phase 2 current (purple) are 500 mA/div and 1 A/div respectively.

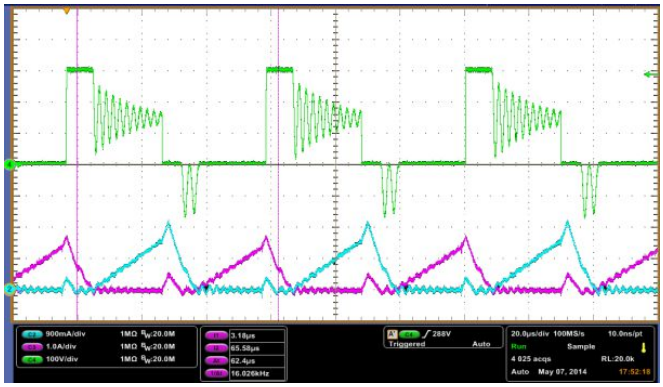


Figure 2.45. Experimental waveform of DCM 10. The Q1 voltage (green) is 100 V/div, while the phase 1 current (purple) and phase 2 current (blue) are 1 A/div and 900 mA/div respectively.

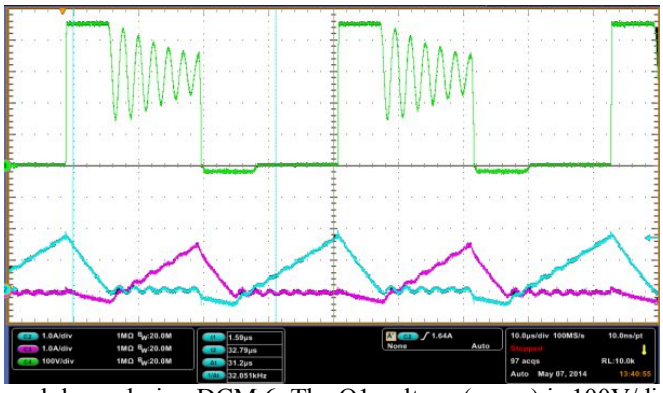


Figure 2.46. IGBT breakdown during DCM 6. The Q1 voltage (green) is 100V/div, while the phase 1 current (purple) and phase 2 current (blue) are 1A/div each.

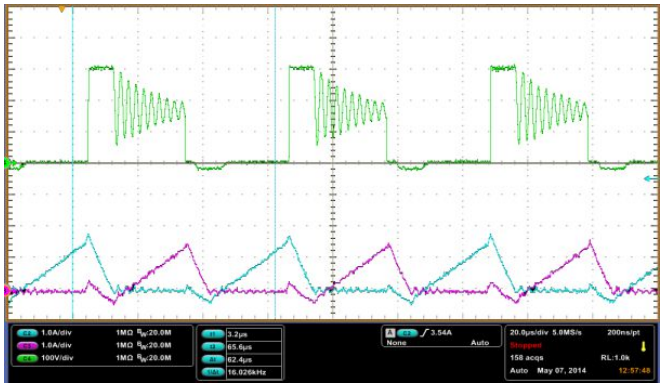


Figure 2.47. IGBT breakdown during DCM 10. The Q1 voltage (green) is 100V/div, while the phase 1 current (blue) and phase 2 current (purple) are 1A/div each.

The ringing which is evident in the pole voltage occurs in all dc-dc converters when operating in DCM, be it a discrete-inductor, or coupled-inductor converter. This ringing is due to the parasitic capacitances and inductances which are inherent in semiconductor switches such as MOSFETs [2.38]. In industrial applications, this ringing may be undesirable, and steps may have to be taken to reduce the effects of this ringing, such as accidental turn-on of the switch. Also evident in a number of the waveforms is an imbalance of current. This is mainly due to the fact that the tests were run in open loop, and while theoretically, the converter is completely symmetrical i.e. both phases are identical, in reality, slight differences in phase inductances and semiconductor characteristics will contribute to imbalances in the phases. Hence, while both phases are given identical duty cycles, differences in the current waveforms are expected.

During testing, the converter input voltage is set to a constant value ranging from 50 V to 275 V, and the load current is varied for that constant voltage. The closed-loop controller then settles on the duty cycle value needed to keep the output at 300V. The duty cycle and dc output current are then recorded. A plot of duty cycle versus dc output current for various voltage gains is shown in Figure 2.48. An excellent correlation is demonstrated between the analytical and experimental results.

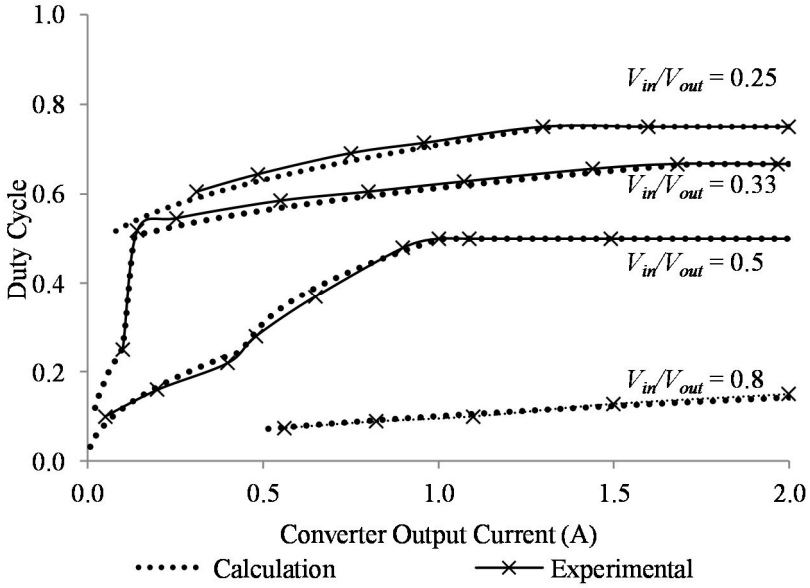


Figure 2.48. Experimental and calculated values of converter characteristics.

As can be seen from Figure 2.48 it is now possible to predict the large signal behaviour of the CL boost converter. Though slight differences can be seen between the predicted and measured values, these can be explained via circuit parasitic, such as the inductor and capacitor ESRs, semiconductor losses, and core losses in the inductor.

2.10 Conclusions

This chapter has presented an investigation of the various continuous-current (CCM) and discontinuous-current (DCM) modes of operation of the coupled-inductor interleaved two-phase boost converter. A comprehensive investigation of the DCM modes is required in order to optimize the converter for full-load and part-load operation, especially when considering such factors as control, efficiency, Electromagnetic Interference (EMI), and failure modes. The various CCM and DCM modes of the converter were identified together with their sub-modes of operation. The steady-state operating characteristics, equations and waveforms for the many CCM and DCM modes were presented for the converter family. Brief solutions were presented for the CCM modes and two of the DCM modes. A set of simultaneous equations was presented for full set of DCM modes. Mode maps were developed to characterize the converter operation across the various modes over the operating range. An excellent correlation was demonstrated between the analytical predictions and the experimental results from a 1 kW boost laboratory prototype. A similar analysis of a CL buck converter is presented in Appendix A.

2.11 References

[2.1] G. W. Wester, and R. D. Middlebrook, "Low-frequency characterization of switched dc-dc converters," *IEEE Transactions on Aerospace and Electronic Systems*, vol. 9, no. 3, pp. 376-385, May 1973.

[2.2] S. Cuk, "Discontinuous inductor current in the optimum topology switching converter," *IEEE Power Electronics Specialists Conference*, pp. 105-123, June 1978.

[2.3] J. P. M. Figueiredo, F. L. Tofoli, and B. L. A. Silva, "A review of single-phase PFC topologies based on the boost converter," *9th IEEE/IAS International Conference on Industry Applications*, pp. 1-6, November 2010.

[2.4] H. Wei, and I. Batarseh, "Comparison of basic converter topologies for power-factor correction," *Proceedings on the IEEE Southeastcon*, pp. 348-358, April 1998.

[2.5] T. Oba, H. Murabayashi, S. Murasige, and I. Takahashi, "Single-switch buck-boost type dither PFC converter using centre-tapped transformer," *29th Annual IEEE Power Electronics Specialists Conference*, pp. 1822-1827, May 1998.

[2.6] P. Biczel, "Power Electronic Converters in DC microgrid," *2007 Compatibility in Power Electronics*, pp. 1-6, May 2007.

[2.7] J. Zakis, D. Vinnikov and L. Bisenieks, "Some design considerations for coupled inductors for integrated buck-boost converters," *IEEE International Conference on Power Engineering, Energy and Electrical Drives*, pp. 1-6, May 2011.

[2.8] Y. Jang and M. M. Jovanovic, "A bridgeless PFC boost rectifier with optimised magnetic utilisation," *IEEE Transactions on Power Electronics*, vol. 24, no. 1, pp. 85-93, January 2009.

[2.9] Q. Li and P. Wolfs, "A current fed two-inductor boost converter with an integrated magnetic structure and passive lossless snubbers for photovoltaic module integrated converter applications," *IEEE Transactions on Power Electronics*, vol. 22, no. 1, pp. 309-321, January 2007.

[2.10] S. Dwari and L. Parsa, "An efficient high-step-up interleaved DC–DC converter with a common active clamp," *IEEE Transactions on Power Electronics*, vol. 26, no. 1, pp. 66-78, January 2011.

[2.11] J. W. Kolar, G. R. Kamath, N. Mohan and F. C. Zach, "Self-adjusting input current ripple cancellation of coupled parallel connected hysteresis-controlled boost power-factor correctors," *IEEE Power Electronics Specialists Conference*, vol. 1, no. 1, pp. 164-173, June 1995.

[2.12] P. L. Wong and F. C. Lee, "Interleaving to reduce reverse recovery loss in power-factor correction circuits," *IEEE Industry Applications Conference*, vol. 4, no. 1, pp. 2311-2618, October 2000.

[2.13] A. J. Forsyth and F. J. Bryan, "A power dense DC-DC converter for a small electric vehicle," *6th IET International Conference Power Electronics, Machines and Drives*, pp. 1-6, March 2012.

[2.14] G. Calderon-Lopez and A. J. Forsyth, "Sampled-data analysis of the dual-interleaved boost converter with interphase transformer," *IEEE Transactions on Power Electronics*, Vol. 27, No. 3, pp. 1338-1346, August 2011.

[2.15] G. Calderon-Lopez and A. J. Forsyth, "High power density DC-DC converter with SiC MOSFETs for electric vehicle," *7th IET International Conference on Power Electronics, Machines and Drives*, pp. 1-6, April 2014.

[2.16] P. W. Lee, Y. S. Lee, D. K. W. Cheng, and X. C. Liu, "Steady state analysis of an interleaved boost converter with coupled inductors," *IEEE Transactions on Industrial Electronics*, vol. 26, no. 1, pp. 66-78, August 2000.

[2.17] H. Kosai, S. McNeal, B. Jordan, J. Scofield, B. Ray, and Z. Turgut, "Coupled inductor characterization for a high performance interleaved boost converter," *IEEE Transactions on Magnetics*, vol. 45, no. 10, pp. 4812 – 4815, October 2009.

[2.18] J. Scofield, S. McNeal, B. Jordan, H. Kosai, and B. Ray, "Studies of interleaved DC-DC boost converters with coupled inductors," *Air Force Research Laboratory Wright-Patterson AFB OH Propulsion Directorate*, April 2011.

[2.19] A. Stratakos, J. Li, B. Beronja, D. Lidsky, M. McJimsey, A. Schultz, C. R. Sullivan, and C. Nickel, "Method and apparatus for multi-phase dc-dc converters using coupled inductors in discontinuous conduction mode," U.S. Patent 7 548 046 B1, June 16, 2009.

[2.20] G. Calderon-Lopez and A. J. Forsyth, "High-power dual-interleaved ZVS boost converter with interphase transformer for electric vehicles," *24th Annual Applied Power Electronics Conference and Exposition*, pp. 1078-1083, February 2009.

[2.21] R. T. Chen and Y. Y. Chen, "Single-stage push-pull boost converter with integrated magnetics and input current shaping technique," *IEEE Transactions on Power Electronics*, vol. 21, no. 5, pp. 1193-1203, September 2006.

[2.22] M. Veerachary, "Analysis of interleaved dual boost converter with integrated magnetics: signal flow graph approach," *IEEE Proceedings in Electric Power Applications*, vol. 150, no. 4, pp. 407-416, July 2003.

[2.23] J. Zakis, D. Vinnikov and L. Bisenieks, "Some design considerations for coupled inductors for integrated buck-boost converters," *IEEE International Conference on Power Engineering, Energy and Electrical Drives*, pp. 1-6, May 2011.

[2.24] M. Phattanasak, W. Kaewmanee, R. Gavagsav-Ghoachai, J. P. Martin, S. Pierfederici, and B. Davat, "Study of two-phase interleaved boost converter using coupled inductors for a fuel cell," *Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology*, pp. 1-6, May 2013.

[2.25] B.C. Barry, J.G. Hayes, M.S. Ryłko, J.W. Masłoń, K.J. Hartnett "Two-phase interleaved boost converters for distributed generation," *IEEE Power Electronics for Distributed Generation Conference*, pp. 1-8, June 2014.

[2.26] N. Mohan, T. M. Undeland and W. P. Robbins (2003). *Power Electronics; Converters, Applications and Design, 3rd Edition*, John Wiley & Sons, Inc.

[2.27] Erickson, R. W. (1997). *Fundamentals of Power Electronics*, Kluwer Academic Publishers.

[2.28] http://www.irf.com/product-info/datasheets/data/irg4pc40k.pdf (IRG4PC40K, accessed on 25/11/2016).

[2.29] S. Dwari and L. Parsa, "An efficient high-step-up interleaved DC–DC converter with a common active clamp," *IEEE Transactions on Power Electronics*, vol. 26, no. 1, pp. 66-78, January 2011.

[2.30] M. K. Yoong, Y. H. Gan, G. D. Gan, C. K. Leong, Z. Y. Phuan, B. K. Cheah, K. W. Chew, "Studies of regenerative breaking in electric vehicles," *IEEE Conference on Sustainable Utilization in Engineering and Technology*, pp. 40-45, November 2010.

[2.31] P. Pany, R. K. Singh, R. K. Tripathi, "Bidirectional dc-dc converter fed drive for electric vehicle system," *International Journal of Engineering, Science and Technology*, vol. 3, no. 3, pp. 101-110, 2011.

[2.32] B. C. Barry, J. G. Hayes, and M. S. Ryłko, "CCM and DCM operation of the interleaved two-phase boost converter with discrete and coupled inductors," *IEEE Transactions on Power Electronics*, vol. 30, no. 12, pp. 6551-6567, December 2014.

[2.33] http://www.infineon.com/cms/en/product/power/power-mosfet/20v-650v-automotive-mosfet/600v-and-650v-n-channel-automotive-mosfet/IPW60R075CPA/productType.html?productType=db3a3044288793430128ed806f2c585d (IPW60R075CPA, accessed on 25/11/2016).

[2.34] http://www.digikey.com/product-detail/en/cree-inc/CVFD20065A/CVFD20065A-ND/4849863 (CVFD20065A, accessed on 25/11/2016).

[2.35] https://library.e.abb.com/public/5136590a04ba0934c1256e920028dc42/1SBC140142C0201.pdf (Accessed on 27/11/2016).

[2.36] http://www.lem.com/docs/products/lv_25-p.pdf (Accessed on 27/11/2016).

[2.37] https://www.altera.com/products/fpga/cyclone-series/cyclone-iii/overview.html (Accessed on 27/11/2016).

[2.38] J. Falin, "Minimizing ringing at the switch node of a boost converter", *Texas Instruments Application Note*, September 2006, (www.ti.com/lit/an/slva255/slva255.pdf, accessed on 02/12/2016).

3 COUPLED-INDUCTOR INTERLEAVED CONVERTER SMALL-SIGNAL AND TRANSFER FUNCTION MODELS

Small-signal models of dc-dc converters are essential in designing suitable controllers to ensure a regulated and stable output. Hence, this chapter focuses on the small-signal models and transfer functions of the continuous-conduction and discontinuous-conduction modes of operation of the two-phase CL interleaved converter.

3.1 Introduction

Small-signal models are frequency-dependent mathematical models which characterise the non-linear dynamics of a system as a set of linear equations. These models can be utilised to characterise all levels of a multi-level system. For example, switch-mode power supplies have their own dynamics, and hence, have their own small-signal models [3.1]-[3.3]. Along with this, device components in these switch-mode power supplies, such as diodes and semiconductor switches, will themselves have their own dynamics, which are independent of the converter. Hence, these devices will also have their own small-signal models [3.4]-[3.5].

A wide body of literature is available on the methods of derivation of small-signal models for switch-mode power supplies. A comparison of the different methods of obtaining small-signal models of converters is presented in [3.7], which compares an experimental frequency sweep of a bidirectional dc-dc converter to the derivation of a small-signal equivalent circuit model. It is found that, while running an experimental frequency sweep yields more accurate results, it is harder to determine the factors that affect the small-signal models of converters, without running a multitude of sweeps and changing a single circuit parameter in each sweep. The authors of [3.1] apply a state-space approach to a buck and boost converter, which can then be extended to other converter topologies. A similar approach is taken in [3.6], where a state-space model of a generic converter is first derived, and discretized to give an accurate state-space model in the discrete domain.

Along with the different methods, each switch-mode power supply topology also has a unique small-signal model. For example, while both are considered a second-order system, the small-signal models of a buck converter and a boost converter differ due to the different gains, as well as the fact that a boost converter operating in CCM contains a right-half plane zero in its transfer function. This right-half plane zero is due to the fact that, in order to increase the output voltage in a boost converter, the output must be disconnected from the input for a longer period of time. Initially, as this happens, the output capacitor does not have sufficient charge to supply the output. This causes the output of the system to drop before it rises, which is represented by the right-half plane zero [3.16].

There are various examples of small-signal modelling of different converters available. For example, the authors of [3.8]-[3.9] provide the derivation of the small-signal model of a zero-voltage-switching phase-shifted PWM full-bridge power

converter, while the small-signal model for the quadratic buck converter is presented in [3.10].

In the area of coupled-inductors, a zero-voltage switched Single-Ended Primary Inductor Converter (SEPIC) dual converter utilising coupled-inductors is analysed via the small-signal equivalent circuit model in [3.11], while in [3.12] the small-signal model of a two-phase buck converter utilising centre-tapped coupled-inductors is discussed. Once again, the method of deriving the small-signal model in [3.12] involves replacing the circuit elements with their small-signal equivalent components. However, the converter is always assumed to be operating in CCM, and is not analysed for DCM operation. In [3.14] the authors present a generalised small-signal model derivation for several high-gain dc-dc converters utilizing coupled-inductors. As before, the initial step is to convert the system into its state-space model, and also replace the circuit components with their small-signal equivalent components. However, once again, each converter is assumed to be operating in CCM, and DCM operation is not included.

As can be seen, very little research has been done on the area of dc-dc coupled-inductor converters operating in DCM. The objective of this chapter is to give an extensive overview of the small-signal modelling and transfer function derivation of the single-phase (1L), two-phase (2L), and two-phase coupled-inductor (CL) dc-dc converters operating in both CCM and DCM.

Section 3.2 presents the method of linearisation used in this thesis, as well as the derivation of the transfer functions of the dc-dc converter family from the small-signal models. Section 3.3 focuses on the small-signal model of the 1L boost converter operating in both continuous-conduction mode and discontinuous-conduction mode. Section 3.4 extends this analysis into a 2L boost converter. Section 3.5 focuses on the small-signal model of a CL boost converter. Section 3.6 verifies the small-signal model of the CL converter with Matlab®/Simulink simulations and experimental frequency sweeps from the 1 kW laboratory prototype. Section 3.7 compares the small-signal models of the 2L and CL converters operating in CCM, while Section 3.8 compares the frequency responses of all CL converter DCM modes to their 2L counterparts.

3.2 Linearisation and Transfer Function Models of the DC-DC Converter Family

For each mode of operation in either the buck or boost converter, there are four transfer function models of interest; $G_{vv}(s)$, the input voltage-to-output voltage model, $G_{vd}(s)$, the duty cycle-to-output-voltage model, $G_{id}(s)$, the duty cycle-to-inductor-current model and G_{vi}(s), the inductor current-to-output voltage model [3.13]. Hence, there are four states of interest when analysing the converter; the input voltage V_{in}, the output voltage V_{out}, the inductor currents I_{L1} and I_{L2}, and the duty cycle D.

3.2.1 Converter Linearisation

One of the major difficulties in deriving the small-signal models of power converters is the inherent non-linearity present in the converter large-signal models. Since small-signal models are only accurate for linear models, the states of the converter are typically linearised around its operating points [3.15]. In order to linearise the states of the converter, the following linearisation method is applied.

If

$$\frac{dX}{dt} = f(X,Y)$$

then

$$\frac{d\tilde{x}}{dt} = \frac{\delta f(X,Y)}{\delta X}\tilde{x} + \frac{\delta f(X,Y)}{\delta Y}\tilde{y}$$

where $\tilde{x}$ is the small perturbation of X and $\tilde{y}$ is the small perturbation of Y. The operating points are defined as $\bar{X}$ and $\bar{Y}$. Hence, the states of the converter, once linearised, transform into

$$\begin{aligned} V_{in} &= \overline{V}_{in} + \tilde{v}_{in} \\ V_{out} &= \overline{V}_{out} + \tilde{v}_{out} \\ I_{L1} &= \overline{I}_{L1} + \tilde{i}_{L1} \\ D &= \overline{D} + \tilde{d} \end{aligned} \tag{3.1}$$

where $\overline{V}_{in}$ is the input voltage at the operating point, and $\tilde{v}_{in}$ is its perturbation, $\overline{V}_{out}$ is the output voltage at the operating point, and $\tilde{v}_{out}$ is its perturbation, $\overline{I}_{L1}$ is the phase 1 inductor current at the operating point, and $\tilde{i}_{L1}$ is its perturbation, $\overline{D}$ is the duty cycle at the operating point, and $\tilde{d}$ is its perturbation. This method of linearisation is easily implemented in software such as Matlab®, and as such is the method of choice. Throughout this chapter, the derivation of the small-signal models of the dc-dc

converter will be presented. For each converter, the resulting dynamic models will take the form of

$$L\frac{d\tilde{i}_{L1}(t)}{dt} = \alpha_1\tilde{v}_{in}(t) + \beta_1\tilde{v}_{out}(t) + \gamma_1\tilde{d}(t) + \delta_1\tilde{i}_{L1}(t) \tag{3.2}$$

$$C_{out}\frac{d\tilde{v}_{out}(t)}{dt} = \alpha_2\tilde{v}_{in}(t) + \beta_2\tilde{v}_{out}(t) + \gamma_2\tilde{d}(t) + \delta_2\tilde{i}_{L1}(t) \tag{3.3}$$

3.2.2 Converter Transfer Function Models

The two most common forms of representing small-signal models for control design are state-space models [3.16] and transfer functions. This section focuses on the derivation of the transfer function models from the small-signal models presented in equations (3.2) and (3.3). Transfer functions are representations of the gain and phase of the linearised system in the frequency domain. Hence, equations (3.2) and (3.3) must be converted into the frequency domain using the Laplace transform, which results in

$$sL\tilde{i}_{L1}(s) = \alpha_1\tilde{v}_{in}(s) + \beta_1\tilde{v}_{out}(s) + \gamma_1\tilde{d}(s) + \delta_1\tilde{i}_{L1}(s) \tag{3.4}$$

$$sC_{out}\tilde{v}_{out}(s) = \alpha_2\tilde{v}_{in}(s) + \beta_2\tilde{v}_{out}(s) + \gamma_2\tilde{d}(s) + \delta_2\tilde{i}_{L1}(s) \tag{3.5}$$

3.2.2.1 Input Voltage-to-Output Voltage Small-Signal Model

In order to find the input voltage-to-output voltage transfer function $G_{vv}(s)$, the inductor current in equation (3.4) is isolated.

$$\tilde{i}_{L1}(s) = \frac{\alpha_1\tilde{v}_{in}(s) + \beta_1\tilde{v}_{out}(s) + \gamma_1\tilde{d}(s)}{(sL - \delta_1)} \tag{3.6}$$

This expression is then substituted into equation (3.5).

$$sC_{out}\tilde{v}_{out}(s) = \alpha_2\tilde{v}_{in}(s) + \beta_2\tilde{v}_{out}(s) + \gamma_2\tilde{d}(s) + \delta_2\frac{\alpha_1\tilde{v}_{in}(s) + \beta_1\tilde{v}_{out}(s) + \gamma_1\tilde{d}(s)}{(sL - \delta_1)} \tag{3.7}$$

By gathering all the terms of the dynamic coefficients together, it is found that

$$\tilde{v}_{out}(s) = \frac{(sL\alpha_2 - \delta_1\alpha_2 + \delta_2\alpha_1)\tilde{v}_{in}(s) + (sL\gamma_2 - \delta_1\gamma_2 + \delta_2\gamma_1)\tilde{d}(s)}{(s^2LC_{out} - s(L\beta_2 + C_{out}\delta_1) + (\delta_1\beta_2 - \delta_2\beta_1))} \tag{3.8}$$

By letting $\tilde{d}(s) = 0$, the input voltage-to-output voltage transfer function is found as

$$G_{vv}(s) = \frac{\tilde{v}_{out}(s)}{\tilde{v}_{in}(s)} = \frac{(sL\alpha_2 - \delta_1\alpha_2 + \delta_2\alpha_1)}{(s^2LC_{out} - s(L\beta_2 + C_{out}\delta_1) + (\delta_1\beta_2 - \delta_2\beta_1))} \tag{3.9}$$

3.2.2.2 Duty Cycle-to-Output Voltage Small-Signal Model

In order to find the duty cycle-to-output voltage transfer function $G_{vd}(s)$, $\tilde{v}_{in}(s)$ is set to zero in equation (3.8). Hence

$$G_{vd}(s)=\frac{\tilde{v}_{out}(s)}{\tilde{d}(s)}=\frac{(sL\gamma_2-\delta_1\gamma_2+\delta_2\gamma_1)}{(s^2LC_{out}-s(L\beta_2+C_{out}\delta_1)+(\delta_1\beta_2-\delta_2\beta_1))} \tag{3.10}$$

3.2.2.3 Duty Cycle-to-Inductor Current Small-Signal Model

In order to find the duty cycle-to-inductor current transfer function $G_{id}(s)$, the output voltage in equation (3.5) is isolated.

$$\tilde{v}_{out}(s)=\frac{\alpha_2\tilde{v}_{in}(s)+\gamma_2\tilde{d}(s)+\delta_2\tilde{i}_{L1}(s)}{(sC_{out}-\beta_2)} \tag{3.11}$$

This expression for the output voltage is then inserted into equation (3.4).

$$sL\tilde{i}_{L1}(s)=\alpha_1\tilde{v}_{in}(s)+\gamma_1\tilde{d}(s)+\delta_1\tilde{i}_{L1}(s)+\beta_1\frac{\alpha_2\tilde{v}_{in}(s)+\gamma_2\tilde{d}(s)+\delta_2\tilde{i}_{L1}(s)}{(sC_{out}-\beta_2)} \tag{3.12}$$

By gathering all the terms of the dynamic coefficients together, it is found that

$$\tilde{i}_{L1}(s)=\frac{(sC_{out}\alpha_1-\beta_2\alpha_1+\beta_1\alpha_2)\tilde{v}_{in}(s)+(sC_{out}\gamma_1-\beta_2\gamma_1+\beta_1\gamma_2)\tilde{d}(s)}{(s^2LC_{out}-s(L\beta_2+C_{out}\delta_1)+(\delta_1\beta_2-\delta_2\beta_1))} \tag{3.13}$$

In order to find the duty cycle-to-inductor current transfer function $G_{id}(s)$, $\tilde{v}_{in}(s)$ is set to zero in equation (3.13). Hence

$$G_{id}(s)=\frac{\tilde{i}_{L1}(s)}{\tilde{d}(s)}=\frac{(sC_{out}\gamma_1-\beta_2\gamma_1+\beta_1\gamma_2)}{(s^2LC_{out}-s(L\beta_2+C_{out}\delta_1)+(\delta_1\beta_2-\delta_2\beta_1))} \tag{3.14}$$

3.2.2.4 Inductor Current-to-Output Voltage Small-Signal Model

In order to find the inductor current-to-output voltage transfer function $G_{vi}(s)$, the duty cycle in equation (3.5) is isolated.

$$\tilde{d}(s)=\frac{sC_{out}\tilde{v}_{out}(s)-\alpha_2\tilde{v}_{in}(s)-\beta_2\tilde{v}_{out}(s)-\delta_2\tilde{i}_{L1}(s)}{\gamma_2} \tag{3.15}$$

This expression for the duty cycle is then inserted into equation (3.4) and the dynamic coefficients gathered.

$$\tilde{v}_{out}(s)=\frac{(s\gamma_2L+\delta_2\gamma_1-\delta_1\gamma_2)\tilde{i}_{L1}(s)+(\alpha_2\gamma_1-\alpha_1\gamma_2)\tilde{v}_{in}(s)}{(s\gamma_1C_{out}+\beta_1\gamma_2-\beta_2\gamma_1)} \tag{3.16}$$

In order to find the inductor current-to-output voltage transfer function $G_{vi}(s)$, $\tilde{v}_{in}(s)$ is set to zero in equation (3.16). Hence

$$G_{vi}(s)=\frac{\tilde{v}_{out}(s)}{\tilde{i}_{L1}(s)}=\frac{(s\gamma_2L+\delta_2\gamma_1-\delta_1\gamma_2)}{(s\gamma_1C_{out}+\beta_1\gamma_2-\beta_2\gamma_1)} \tag{3.17}$$

The transfer functions represented in equations (3.9), (3.10), (3.14), and (3.17) can be applied to the 1L, 2L or CL boost converter. The remainder of the chapter will focus on the derivation of the small-signal models of equations (3.2) and (3.3) for each converter.

3.3 Single-Phase Boost Converter (1L) Small-Signal Model

The following section presents the derivation of each CCM and DCM dynamic model for the 1L boost converter.

3.3.1 Small-Signal Models of 1L Boost Converter in CCM

In order to derive the small-signal model of a 1L boost converter, expressions for the inductor voltage and output capacitor current must first be developed over one full switching cycle. When operating in CCM, there are two distinct sub-modes of operation: (i) when the switch in closed during cycle time DT_s and current builds in the inductor, and (ii) when the switch is open during cycle time $(1\text{-}D)T_s$ and current drops in the inductor, as shown in Figure 3.1.

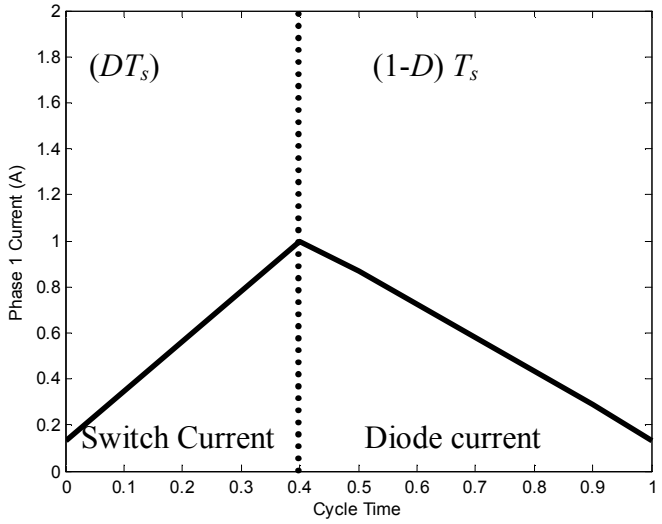


Figure 3.1. Inductor current waveform of a 1L boost converter operating in CCM.

In order to analyse the converter over one full cycle, the converter average model will be found [3.16].

When the switch is closed, the input and output of the converter are isolated, as shown in Figure 3.2.

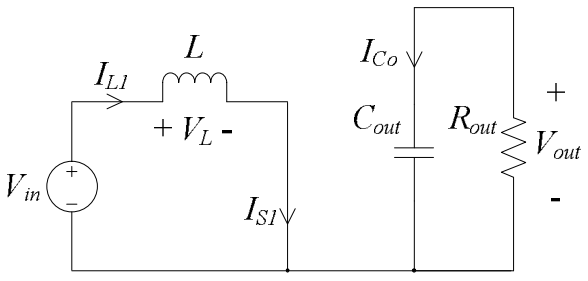


Figure 3.2. 1L boost converter during cycle time DT_s.

The inductor voltage $V_{L(D)}$ and output capacitor current $I_{Co(D)}$ in this state are expressed as

$$V_{L(D)} = L\frac{dI_{L1(D)}}{dt} = V_{in(D)} \tag{3.18}$$

$$I_{Co(D)} = C_{out}\frac{dV_{out(D)}}{dt} = -\frac{V_{out(D)}}{R_{out}} \tag{3.19}$$

where $I_{L1(D)}$ is the dc inductor current during switch on-time, $V_{in(D)}$ is the converter input voltage during switch on-time, V_{out} is the converter output voltage during switch on time, R_{out} is the converter load resistance, L is the value of inductance and C_{out} is the output capacitance. When the switch is open, the input and output are directly connected to each other, as shown in Figure 3.3.

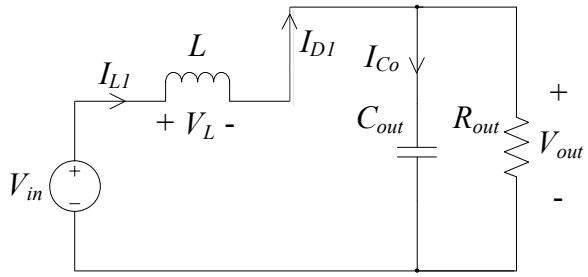


Figure 3.3. 1L boost converter during cycle time (1-D)T_s.

The inductor voltage $V_{L(1-D)}$ and output capacitor current $I_{Co(1-D)}$ in this state are expressed as

$$V_{L(1-D)} = L\frac{dI_{L1(1-D)}}{dt} = V_{in(1-D)} - V_{out(1-D)} \tag{3.20}$$

$$I_{Co(1-D)} = C_{out}\frac{dV_{out(1-D)}}{dt} = I_{L1(1-D)} - \frac{V_{out(1-D)}}{R_{out}} \tag{3.21}$$

By averaging equations (3.18) with (3.20) and (3.19) with (3.21), equations (3.22) and (3.23), the weighted average dynamic equations of the 1L boost converter are derived.

$$V_{L(D)} + V_{L(1-D)} = L\frac{dI_{L1}}{dt} = V_{in} - (1-D)V_{out} \tag{3.22}$$

$$I_{Co(D)} + I_{Co(1-D)} = C_{out}\frac{dV_{out}}{dt} = (1-D)I_{L1} - \frac{V_{out}}{R_{out}} \tag{3.23}$$

As stated in Section 3.2.1, equations (3.22) and (3.23) are non-linear, and must be linearised around the operating points of the inductor current, input voltage, output voltage and duty cycle. In order to simplify the linearisation process, equation (3.22) is first expanded, removing the brackets i.e.

$$L\frac{dI_{L1}}{dt} = V_{in} - V_{out} + DV_{out} = f_1(V_{in}, V_{out}, D) \tag{3.24}$$

Each state equation will be linearised independently, and added, to find the full small-signal model of equation (3.24).

$$\frac{\delta f_1}{\delta V_{in}} = 1 \tag{3.25}$$

$$\frac{\delta f_1}{\delta V_{out}} = -(1-\overline{D}) \tag{3.26}$$

$$\frac{\delta f_1}{\delta D} = \overline{V}_{out} \tag{3.27}$$

$$\frac{\delta f_1}{\delta I_{L1}} = 0 \tag{3.28}$$

Hence, the small-signal model of the inductor voltage is found to be

$$L\frac{d\tilde{i}_{L1}(t)}{dt} = \tilde{v}_{in}(t) - (1-\overline{D})\tilde{v}_{out}(t) + \overline{V}_{out}\tilde{d}(t) \tag{3.29}$$

Linearising equation (3.23) in precisely the same manner, the small-signal model of the output capacitor current is found.

$$C_{out}\frac{d\tilde{v}_{out}(t)}{dt} = (1-\overline{D})\tilde{i}_{L1}(t) - \overline{I}_{L1}\tilde{d}(t) - \frac{\tilde{v}_{out}(t)}{R_{out}} \tag{3.30}$$

In order to simplify the small-signal models, the following substitutions are made for the coefficients of the perturbations.

$$\begin{aligned} \alpha_1 &= 1 \\ \beta_1 &= -(1-\overline{D}) \\ \gamma_1 &= \overline{V}_{out} \\ \delta_1 &= 0 \end{aligned} \tag{3.31}$$

and

$$\begin{aligned} \alpha_2 &= 0 \\ \beta_2 &= -\frac{1}{R_{out}} \\ \gamma_2 &= -\overline{I}_{L1} \\ \delta_2 &= (1-\overline{D}) \end{aligned} \tag{3.32}$$

Hence, the dynamic equations (3.29) and (3.30) become

$$L\frac{d\tilde{i}_{L1}(t)}{dt} = \alpha_1\tilde{v}_{in}(t) + \beta_1\tilde{v}_{out}(t) + \gamma_1\tilde{d}(t) + \delta_1\tilde{i}_{L1}(t) \tag{3.33}$$

$$C_{out}\frac{d\tilde{v}_{out}(t)}{dt} = \alpha_2\tilde{v}_{in}(t) + \beta_2\tilde{v}_{out}(t) + \gamma_2\tilde{d}(t) + \delta_2\tilde{i}_{L1}(t) \tag{3.34}$$

which are identical to equations (3.2) and (3.3). By substituting (3.31) and (3.32) into the transfer functions presented in equations (3.9), (3.10), (3.14), and (3.17), $G_{vv}(s)$, $G_{vd}(s)$, $G_{id}(s)$, and $G_{vi}(s)$ are found for the 1L boost converter as

$$G_{vv}(s)=\frac{\tilde{v}_{out}(s)}{\tilde{v}_{in}(s)}=\frac{1-\overline{D}}{C_{out}Ls^2+\frac{L}{R_{out}}s+(1-\overline{D})^2} \tag{3.35}$$

$$G_{vd}(s)=\frac{\tilde{v}_{out}(s)}{\tilde{d}(s)}=\frac{\overline{V}_{out}(1-\overline{D})-sL\overline{I}_{L1}}{C_{out}Ls^2+\frac{L}{R_{out}}s+(1-\overline{D})^2} \tag{3.36}$$

$$G_{id}(s)=\frac{\tilde{i}_{L1}(s)}{\tilde{d}(s)}=\frac{sC_{out}\overline{V}_{out}+\frac{\overline{V}_{out}}{R_{out}}-\overline{I}_{L1}(1-\overline{D})}{C_{out}Ls^2+\frac{L}{R_{out}}s+(1-\overline{D})^2} \tag{3.37}$$

$$G_{vi}(s)=\frac{\tilde{v}_{out}(s)}{\tilde{i}_{L1}(s)}=\frac{-sL\overline{I}_{L1}+(1-\overline{D})\overline{V}_{out}}{sC_{out}\overline{V}_{out}+\frac{\overline{V}_{out}}{R_{out}}+\overline{I}_{L1}(1-\overline{D})} \tag{3.38}$$

3.3.2 Small-Signal Models of 1L Boost Converter in DCM

The inductor current waveform of a 1L boost converter operating in DCM is presented in Figure 3.4.

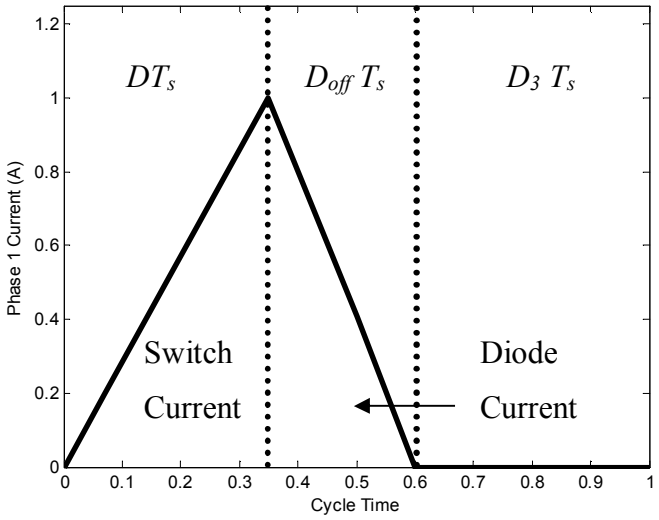


Figure 3.4. Inductor current waveform of a 1L boost operating in DCM.

From Figure 3.4, it can be seen that a third segment now exists in the waveform during the cycle time D_3T_s. This part of the cycle is shown in Figure 3.5.

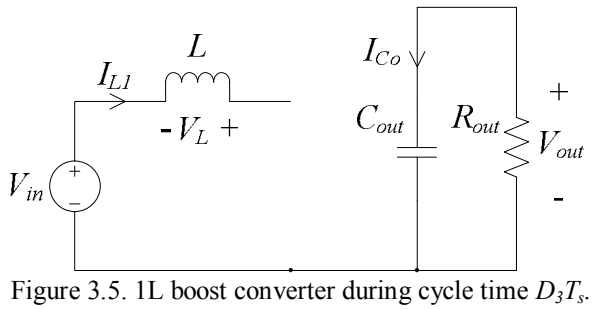


Figure 3.5. 1L boost converter during cycle time D_3T_s.

By applying Figure 3.4 to Figure 3.2, Figure 3.3 and Figure 3.5, the dynamic equations of the 1L boost converter operating in DCM are found.

$$L\frac{dI_{L1}}{dt} = V_{in}(D + D_{off}) - D_{off}V_{out} \tag{3.39}$$

$$C_{out}\frac{dV_{out}}{dt} = I_{L1} - I_{S1} - \frac{V_{out}}{R_{out}} \tag{3.40}$$

where I_{S1} is the dc current flowing through the switch, which, when subtracted from the inductor current, gives the converter diode current. Both the equations above contain unknown variables which must first be solved before linearisation. The peak-to-peak inductor current ripple of the converter is expressed as

$$\Delta I_{L1p-p} = \frac{V_{in}DT_s}{L} \tag{3.41}$$

By using the formula for the area of a triangle, the dc phase current is found as

$$I_{L1} = \frac{\Delta I_{L1p-p}(D + D_{off})}{2} = \frac{V_{in}DT_s}{2L}(D + D_{off}) \tag{3.42}$$

Solving equation (3.42) for D_{off} yields

$$D_{off} = \frac{2I_{L1}L}{V_{in}DT_s} - D \tag{3.43}$$

Similarly, the dc switch current is found to be

$$I_{S1} = \frac{\Delta I_{L1p-p}D}{2} = \frac{V_{in}D^2T_s}{2L} \tag{3.44}$$

Inserting equation (3.43) into equation (3.39), and equation (3.44) into equation (3.40), the full dynamic models of the 1L converter operating in DCM are found.

$$L\frac{dI_{L1}}{dt} = \frac{2I_{L1}L}{DT_s} - \left(\frac{2I_{L1}L}{V_{in}DT_s} - D\right)V_{out} \tag{3.45}$$

$$C_{out}\frac{dV_{out}}{dt} = I_{L1} - \frac{V_{in}D^2T_s}{2L} - \frac{V_{out}}{R_{out}} \tag{3.46}$$

Linearising equations (3.45) and (3.46), the small-signal models of the 1L boost converter operating in DCM are found as

$$L\frac{d\tilde{i}_{L1}(t)}{dt} = \alpha_1\tilde{v}_{in}(t) + \beta_1\tilde{v}_{out}(t) + \gamma_1\tilde{d}(t) + \delta_1\tilde{i}_{L1}(t) \tag{3.47}$$

$$C_{out}\frac{d\tilde{v}_{out}(t)}{dt} = \alpha_2\tilde{v}_{in}(t) + \beta_2\tilde{v}_{out}(t) + \gamma_2\tilde{d}(t) + \delta_2\tilde{i}_{L1}(t) \tag{3.48}$$

where

$$\begin{aligned}
\alpha_1 &= \frac{2\bar{I}_{L1}L\bar{V}_{out}}{\bar{D}T_s\bar{V}_{in}^{\,2}} \\
\beta_1 &= \bar{D} - \frac{2\bar{I}_{L1}L}{\bar{D}T_s\bar{V}_{in}} \\
\gamma_1 &= \bar{V}_{out}\left(\frac{2\bar{I}_{L1}L}{\bar{D}^2T_s\bar{V}_{in}} + 1\right) - \frac{2\bar{I}_{L1}L}{\bar{D}^2T_s} \\
\delta_1 &= -\frac{2L(\bar{V}_{out} - \bar{V}_{in})}{\bar{D}T_s\bar{V}_{in}}
\end{aligned} \tag{3.49}$$

and

$$\begin{aligned}
\alpha_2 &= -\frac{\bar{D}^2T_s}{2L} \\
\beta_2 &= -\frac{1}{R_{out}} \\
\gamma_2 &= -\frac{\bar{D}T_s\bar{V}_{in}}{L} \\
\delta_2 &= 1
\end{aligned} \tag{3.50}$$

The transfer functions of the converter are found by substituting (3.49) and (3.50) into the transfer functions presented in equations (3.9), (3.10), (3.14), and (3.17).

3.4 Two-Phase Boost Converter (2L) Small-Signal Model

The following section presents the derivation of each of the four transfer functions found in a 2L boost converter operating in CCM and DCM. For the analysis, it is assumed that the two phases of the converter are balanced i.e. the phase 1 dc current I_{L1} equals the phase 2 dc current I_{L2}, the phase 1 inductance $L_1 = L$ equals the phase 2 inductance $L_2 = L$, and the phase 1 duty cycle $D_1 = D$ is equal to the phase 2 duty cycle $D_2 = D$.

3.4.1 Small-Signal Models of 2L Boost Converter in CCM

When assuming balanced phases in a multi-phase converter, the solution of one phase can be directly applied to all other phases. Hence, only phase 1 of the 2L converter needs be analysed. In the 2L converter, the current waveform in phase 1 is identical to the waveform from a single phase converter, shown in Figure 3.1. Hence, the inductor voltage dynamic equation is also identical.

$$L\frac{dI_{L1}}{dt} = V_{in} - (1-D)V_{out} \tag{3.51}$$

The output capacitor current can also be derived in a similar manner. In the 1L converter, the output capacitor current was the sum of the diode current and the output load current. In a 2L converter, the current from the second phase must be added. Since $I_{L1} = I_{L2}$, the output capacitor current dynamic equation is derived as

$$C_{out}\frac{dV_{out}}{dt} = 2(1-D)I_{L1} - \frac{V_{out}}{R_{out}} \tag{3.52}$$

Equations (3.51) and (3.52) are linearised, and the small-signal models of the 2L boost converter operating in CCM are found as

$$L\frac{d\tilde{i}_{L1}(t)}{dt} = \alpha_1\tilde{v}_{in}(t) + \beta_1\tilde{v}_{out}(t) + \gamma_1\tilde{d}(t) + \delta_1\tilde{i}_{L1}(t) \tag{3.53}$$

$$C_{out}\frac{d\tilde{v}_{out}(t)}{dt} = \alpha_2\tilde{v}_{in}(t) + \beta_2\tilde{v}_{out}(t) + \gamma_2\tilde{d}(t) + \delta_2\tilde{i}_{L1}(t) \tag{3.54}$$

where

$$\begin{aligned} \alpha_1 &= 1 \\ \beta_1 &= -(1-\overline{D}) \\ \gamma_1 &= \overline{V}_{out} \\ \delta_1 &= 0 \end{aligned} \tag{3.55}$$

and

$$\begin{aligned}\alpha_2 &= 0\\ \beta_2 &= -\frac{1}{R_{out}}\\ \gamma_2 &= -2\overline{I}_{L1}\\ \delta_2 &= 2(1-\overline{D})\end{aligned} \tag{3.56}$$

3.4.2 Small-Signal Models of 2L Boost Converter in DCM

As with CCM operation, DCM operation in a 2L converter is very similar to a 1L converter. The dynamic equation of the inductor voltage is

$$L\frac{dI_{L1}}{dt} = V_{in}(D + D_{off}) - D_{off}V_{out} \tag{3.57}$$

While the equation of the output capacitor current, which must take into account the second phase, is

$$C_{out}\frac{dV_{out}}{dt} = 2I_{L1} - 2I_{S1} - \frac{V_{out}}{R_{out}} \tag{3.58}$$

Equations (3.43) and (3.44) are inserted into the dynamic equations above to yield

$$L\frac{dI_{L1}}{dt} = \frac{2I_{L1}L}{DT_s} - \left(\frac{2I_{L1}L}{V_{in}DT_s} - D\right)V_{out} \tag{3.59}$$

$$C_{out}\frac{dV_{out}}{dt} = 2I_{L1} - \frac{V_{in}D^2T_s}{L} - \frac{V_{out}}{R_{out}} \tag{3.60}$$

Equations (3.59) and (3.60) are linearised, and the small-signal models of the 2L boost converter operating in DCM are found as

$$L\frac{d\tilde{i}_{L1}(t)}{dt} = \alpha_1\tilde{v}_{in}(t) + \beta_1\tilde{v}_{out}(t) + \gamma_1\tilde{d}(t) + \delta_1\tilde{i}_{L1}(t) \tag{3.61}$$

$$C_{out}\frac{d\tilde{v}_{out}(t)}{dt} = \alpha_2\tilde{v}_{in}(t) + \beta_2\tilde{v}_{out}(t) + \gamma_2\tilde{d}(t) + \delta_2\tilde{i}_{L1}(t) \tag{3.62}$$

where

$$\begin{aligned}\alpha_1 &= \frac{2\overline{I}_{L1}L\overline{V}_{out}}{\overline{D}T_s\overline{V}_{in}^{\,2}}\\ \beta_1 &= \overline{D} - \frac{2\overline{I}_{L1}L}{\overline{D}T_s\overline{V}_{in}}\\ \gamma_1 &= \overline{V}_{out}\left(\frac{2\overline{I}_{L1}L}{\overline{D}^2T_s\overline{V}_{in}} + 1\right) - \frac{2\overline{I}_{L1}L}{\overline{D}^2T_s}\\ \delta_1 &= -\frac{2L(\overline{V}_{out} - \overline{V}_{in})}{\overline{D}T_s\overline{V}_{in}}\end{aligned} \tag{3.63}$$

and

$$\begin{aligned} \alpha_2 &= -\frac{\overline{D}^2 T_s}{L} \\ \beta_2 &= -\frac{1}{R_{out}} \\ \gamma_2 &= -\frac{2\overline{D}T_s\overline{V}_{in}}{L} \\ \delta_2 &= 2 \end{aligned} \tag{3.64}$$

3.5 Coupled-Inductor Boost Converter (CL) Small-Signal Model

The following section presents the derivation of each of the four transfer functions found in a CL boost converter operating in CCM and three of the eight modes of DCM; DCM 4, DCM 1 and DCM 8.

For the analysis, it is assumed that the two phases of the converter are balanced i.e. the phase 1 dc current I_{L1} equals the phase 2 dc current I_{L2}, the phase 1 leakage inductance $L_{Lk1} = L_{Lk}$ equals the phase 2 inductance $L_{Lk2} = L_{Lk}$, and the phase 1 duty cycle $D_1 = D$ is equal to the phase 2 duty cycle $D_2 = D$.

3.5.1 Small-Signal Models of the CL Boost Converter in CCM

As with the 1L and 2L converters, to develop the small-signal model of a CL boost converter, expressions for the inductor voltage and output capacitor current must first be developed over one full switching cycle. For this analysis, it is assumed the duty cycle is at a value less than 0.5. The phase 1, phase 2, and magnetising current waveforms of the CL converter operating in CCM for a duty cycle less than 0.5 are presented in Figure 3.6.

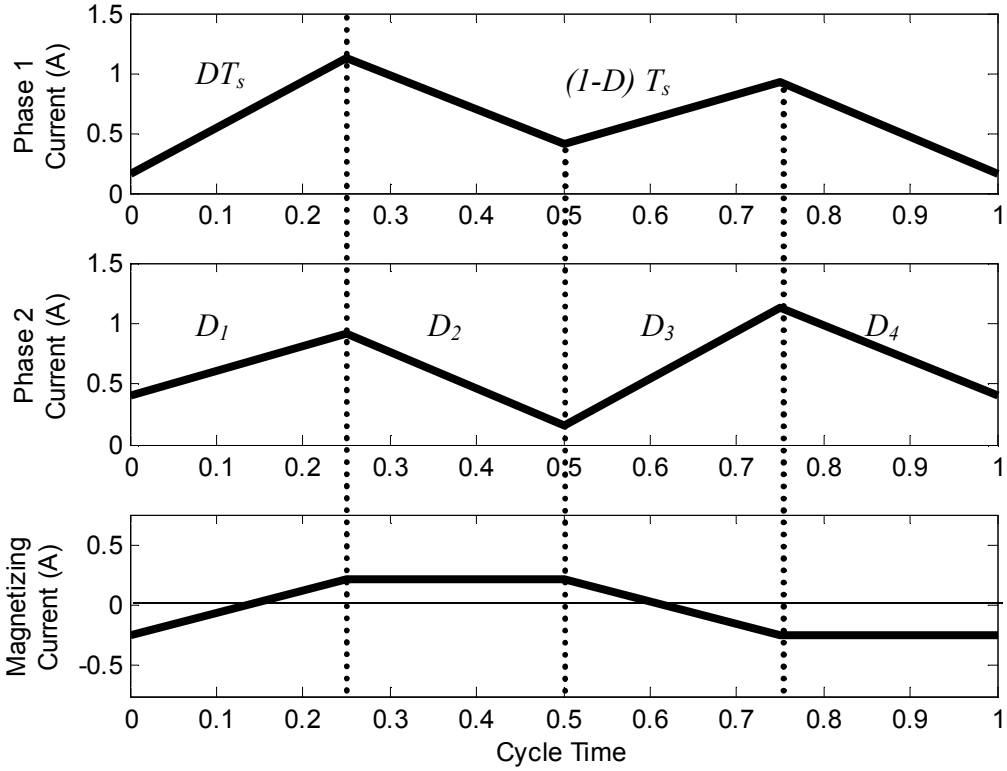


Figure 3.6. Current waveforms of phase 1, phase 2, and magnetising currents.

As stated in chapter 2, in the CL boost converter, there are four sub-modes of operation when the converter is in CCM. These are presented in Figure 3.7 and Figure 3.8, and correspond with the segments D_1, D_2, D_3 and D_4 of Figure 3.6.

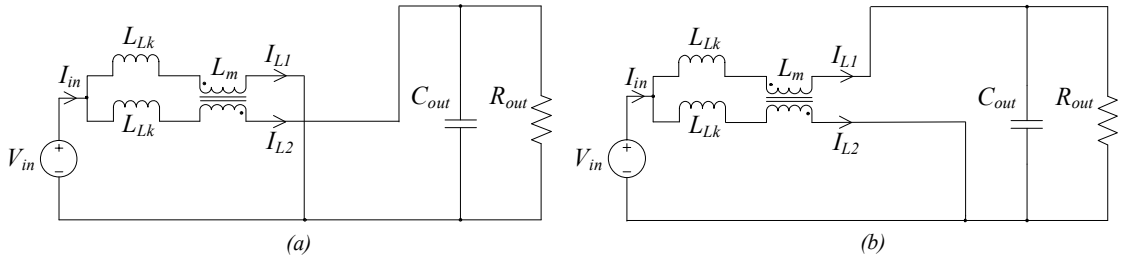


Figure 3.7. CL boost converter operating in region (a) D_1 and (b) D_3.

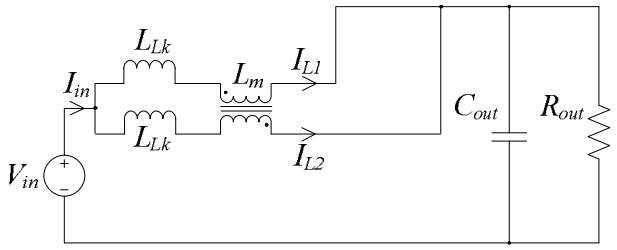


Figure 3.8. CL boost converter operating in regions D_2 and D_4.

As with the 2L converter, since it is assumed that the operation of both phases is balanced; only one phase needs to be solved. The solution of this phase can then be directly applied to the second phase. Hence, using Figure 3.6, Figure 3.7 and Figure 3.8, the CL boost dynamic equations are

$$V_{Lk} = L_{Lk}\frac{d\,\mathrm{I}_{L1}}{dt} = V_{in} - (1-D)V_{out} - V_{T1} \tag{3.65}$$

$$I_{Co} = C_{out}\frac{dV_{out}}{dt} = 2I_{L1}(1-D) - \frac{V_{out}}{R_{out}} \tag{3.66}$$

where

$$V_{M1} = L_m\frac{d\,\mathrm{I}_{\mathrm{m}}}{dt} = L_m\frac{dI_{L1}}{dt} - L_m\frac{dI_{L2}}{dt} \tag{3.67}$$

where I_m is the magnetizing current, which is the difference in current between I_{L1} and I_{L2}, and L_m is the magnetizing inductance. From Figure 3.6, it is evident that the total change in the magnetising current over one full cycle is zero. Hence

$$V_{M1} = 0 \tag{3.68}$$

By applying Equation (3.68) to equation (3.65), the dynamic equation for the inductor voltage simplifies down to that of a 2L converter. Therefore, the solutions of the 2L boost converter given in equations (3.35) to (3.38) also hold true for the CL boost converter if the leakage inductance of the CL converter is equal to the phase inductance of the 2L converter.

3.5.2 Small-Signal Models of the CL Boost Converter in DCM 4

Due to the similarities of DCM 4 with DCM operation in a 2L converter, it will be the first DCM mode to be analysed. The phase current and magnetising current waveforms of DCM 4 are presented in Figure 3.9.

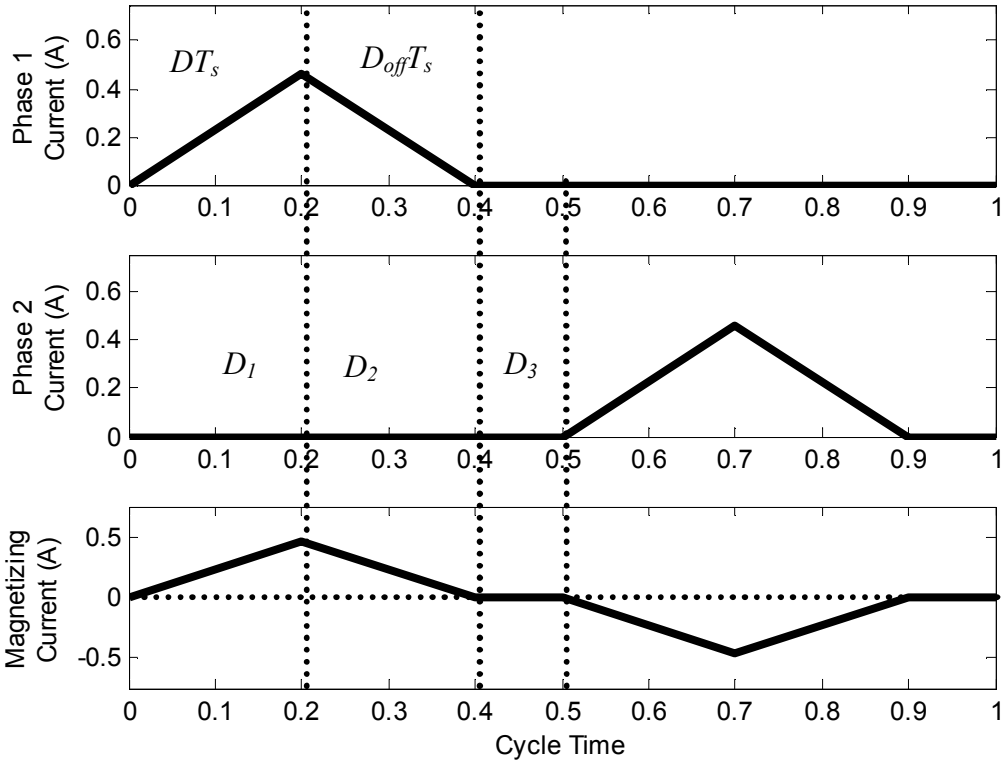


Figure 3.9. Phase and magnetising currents of CL boost converter operating in DCM 4.

As stated in Chapter 2, there are six sub-modes of operation in DCM 4. Since balanced operation is assumed, only one phase of the converter needs to be analysed. This reduces the number of modes to be analysed from six to three, as shown in Figure 3.9. These sub-modes are presented in Figure 3.10 and Figure 3.11.

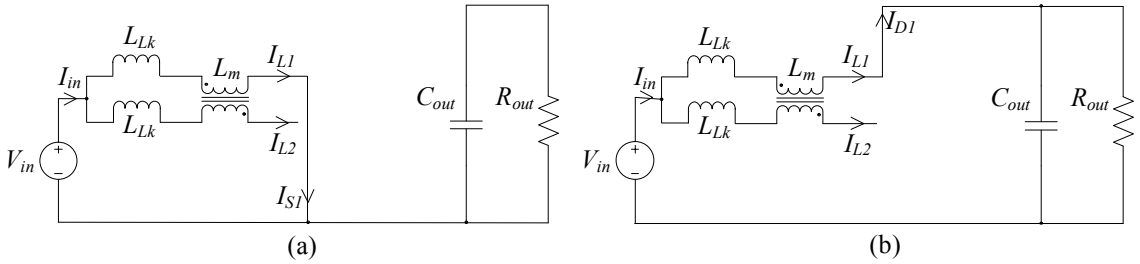


Figure 3.10. The sub-modes of operation (a) D_1 and (b) D_2 of DCM 4.

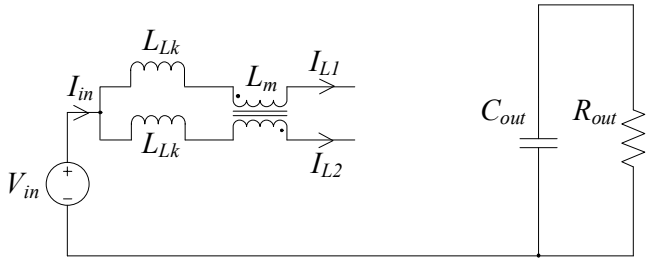


Figure 3.11. The sub-mode of operation D_3 of DCM 4.

Using Figure 3.9, Figure 3.10, and Figure 3.11, the dynamic equations of DCM 4 are found to be

$$L_{Lk}\frac{dI_{L1}}{dt} = V_{in}(D + D_{off}) - D_{off}V_{out} - V_{T1} \tag{3.69}$$

$$C_{out}\frac{dV_{out}}{dt} = 2I_{L1} - 2I_{S1} - \frac{V_{out}}{R_{out}} \tag{3.70}$$

As with CCM operation, the total change in magnetising current in the regions of D_1 and D_3 equals 0, hence

$$V_{T1} = 0 \tag{3.71}$$

Equation (2.31) for D_{off} of DCM 4, which was derived in Chapter 2, is entered into equation (3.83), to complete the inductor voltage equation. In order to find an expression for I_{S1}, the peak-to-peak inductor current ripple is applied as follows

$$I_{S1} = \frac{\Delta I_{L1p-p}D}{2} = \frac{V_{in}D^2T_s}{2(L_{Lk} + L_m)} \tag{3.72}$$

Hence, the full dynamic equations of the DCM 4 CL boost converter are

$$L_{Lk}\frac{dI_{L1}}{dt} = \frac{2I_{L1}(L_{Lk} + L_m)}{DT_s} - \left(\frac{2I_{L1}(L_{Lk} + L_m)}{V_{in}DT_s} - D\right)V_{out} \tag{3.73}$$

$$C_{out}\frac{dV_{out}}{dt} = 2I_{L1} - \frac{V_{in}D^2T_s}{(L_{Lk} + L_m)} - \frac{V_{out}}{R_{out}} \tag{3.74}$$

Equations (3.73) and (3.74) are linearised, and the small-signal models of the CL boost converter operating in DCM 4 are found as

$$L_{Lk}\frac{d\tilde{i}_{L1}(t)}{dt} = \alpha_1\tilde{v}_{in}(t) + \beta_1\tilde{v}_{out}(t) + \gamma_1\tilde{d}(t) + \delta_1\tilde{i}_{L1}(t) \tag{3.75}$$

$$C_{out}\frac{d\tilde{v}_{out}(t)}{dt} = \alpha_2\tilde{v}_{in}(t) + \beta_2\tilde{v}_{out}(t) + \gamma_2\tilde{d}(t) + \delta_2\tilde{i}_{L1}(t) \tag{3.76}$$

where

$$\begin{aligned}
\alpha_1 &= \frac{2\overline{I}_{L1}(L_{Lk} + L_m)\overline{V}_{out}}{\overline{D}T_s\overline{V}_{in}^{\,2}} \\
\beta_1 &= \overline{D} - \frac{2\overline{I}_{L1}(L_{Lk} + L_m)}{\overline{D}T_s\overline{V}_{in}} \\
\gamma_1 &= \overline{V}_{out}\left(\frac{2\overline{I}_{L1}(L_{Lk} + L_m)}{\overline{D}^2T_s\overline{V}_{in}} + 1\right) - \frac{2\overline{I}_{L1}(L_{Lk} + L_m)}{\overline{D}^2T_s} \\
\delta_1 &= -\frac{2(L_{Lk} + L_m)(\overline{V}_{out} - \overline{V}_{in})}{\overline{D}T_s\overline{V}_{in}}
\end{aligned} \tag{3.77}$$

and

$$\alpha_2 = -\frac{\overline{D}^2 T_s}{(L_{Lk} + L_m)}$$
$$\beta_2 = -\frac{1}{R_{out}} \tag{3.78}$$
$$\gamma_2 = -\frac{2\overline{D}T_s\overline{V}_{in}}{(L_{Lk} + L_m)}$$
$$\delta_2 = 2$$

From the coefficients of given in (3.77) and (3.78), the small-signal equations of DCM 4 are nearly identical to those of a 2L boost operating in DCM. The main difference is that the magnetising inductance must now be taken into account.

3.5.3 Small-Signal Models of the CL Boost Converter in DCM 1

When the converter enters DCM with a duty cycle less than 0.5, the first mode it enters is DCM 1, the waveforms of which are shown in Figure 3.12. As previously stated in Chapter 2, there are six sub-modes of operation of the converter when operating in DCM 1. These are labelled D_1 to D_6 in Figure 3.12. Once again, if balanced operation is assumed, only one phase needs to be analysed, and D_6 can be eliminated from the analysis. The remaining sub-modes are presented in Figure 3.13 and Figure 3.14.

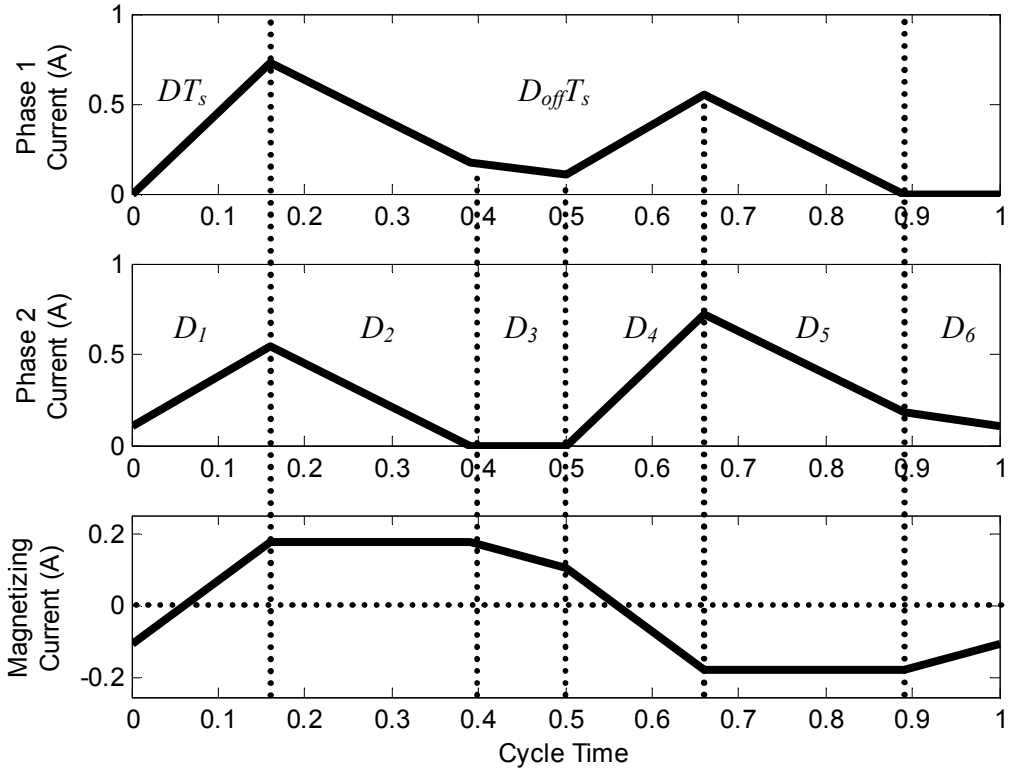


Figure 3.12. Phase and magnetising currents of CL boost converter operating in DCM 1.

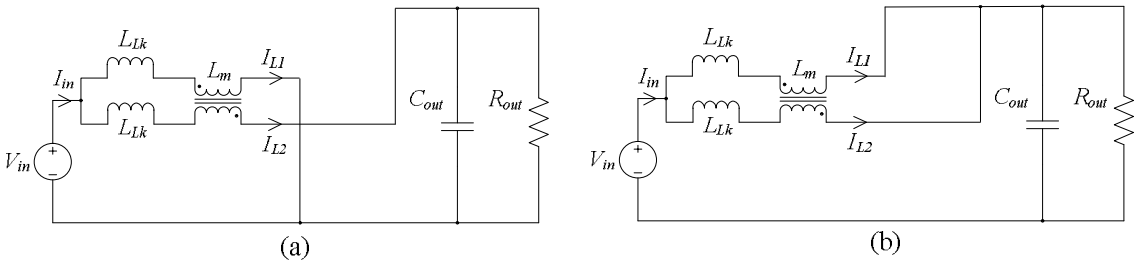


Figure 3.13. The sub-modes of operation (a) D_1 and (b) D_2 and D_5 of DCM 1.

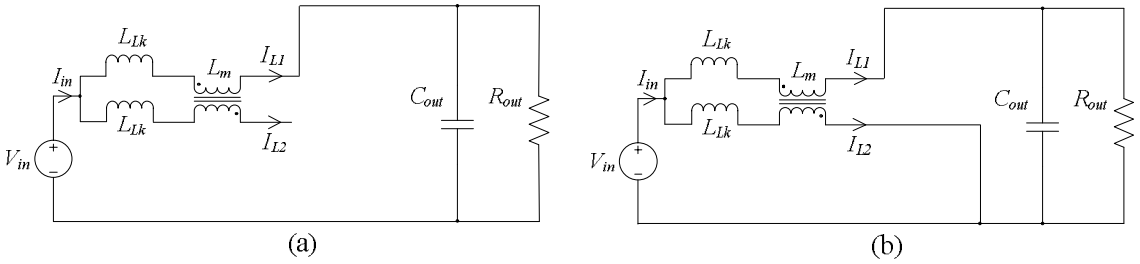


Figure 3.14. The sub-modes of operation (a) D3 and (b) D4 of DCM 1.

Using Figure 3.12, Figure 3.13,and Figure 3.14, the dynamic equations of DCM 1 are found to be

$$L_{Lk}\frac{dI_{L1}}{dt} = V_{in}(D + D_{off}) - D_{off}V_{out} - V_{T1} \tag{3.79}$$

$$C_{out}\frac{dV_{out}}{dt} = 2I_{L1} - 2I_{S1} - \frac{V_{out}}{R_{out}} \tag{3.80}$$

The switch current of DCM 1 occurs during the sub-mode D_1, which is also the cycle time of the peak-to-peak ripple current. Hence

$$I_{S1} = \frac{\Delta I_{Lp-p} D}{2} \tag{3.81}$$

By following the method given in section 2.5, the peak-to-peak inductor current ripple is given by

$$\Delta I_{Lp-p} = \frac{(2V_{in} - V_{out})D_1 T_s}{2L_{Lk}} + \frac{V_{out} D_1 T_s}{2(L_{Lk} + 2L_m)} \tag{3.82}$$

Hence, the switch current of DCM 1 is given by

$$I_{S1} = \left(\frac{(2V_{in} - V_{out})}{L_{Lk}} + \frac{V_{out}}{(L_{Lk} + 2L_m)}\right)\frac{D_1^2 T_s}{2} \tag{3.83}$$

In order to complete the inductor voltage equation, the magnetizing term V_{T1} must be found. V_{T1} is the voltage drop across the magnetizing inductance due to the change in magnetizing current. Hence, to simplify the expression for V_{T1}, it is broken down into its component parts i.e.

$$V_{T1} = \sum_{x=1}^{5} D_x L_m \frac{dI_{mx}}{dt} \tag{3.84}$$

where x denotes the sub-mode of operation. By analysing the magnetizing waveform given in Figure 3.12, it is evident that

$$\begin{aligned} \Delta I_{m1} &= -\Delta I_{m4} \\ \Delta I_{m2} &= \Delta I_{m5} = 0 \end{aligned} \tag{3.85}$$

Hence

$$V_{T1} = L_m \frac{\Delta I_{m3}}{T_s} \tag{3.86}$$

The change in magnetizing current during the cycle time D_3 is given by the expression

$$\Delta I_{m3} = \frac{(V_{in} - V_{out}) D_3 T_s}{L_{Lk} + L_m} \tag{3.87}$$

From Figure 3.12, the cycle time D_3 can be expressed as

$$D_3 = 1 - D - D_{off} \tag{3.88}$$

Therefore, the magnetizing element of the inductor voltage equation is expressed as

$$V_{T1} = L_m \frac{(V_{in} - V_{out})(1 - D - D_{off})}{L_{Lk} + L_m} \tag{3.89}$$

Equations (3.83) and (3.89) are substituted into equations (3.79) and (3.80), respectively, to give

$$L_{Lk} \frac{dI_{L1}}{dt} = V_{in}(D + D_{off}) - D_{off} V_{out} - L_m \frac{(V_{in} - V_{out})(1 - D - D_{off})}{L_{Lk} + L_m} \tag{3.90}$$

$$C_{out} \frac{dV_{out}}{dt} = 2I_{L1} - \left(\frac{(2V_{in} - V_{out})}{L_{Lk}} + \frac{V_{out}}{(L_{Lk} + 2L_m)} \right) D_1^2 T_s - \frac{V_{out}}{R_{out}} \tag{3.91}$$

Finally, the solution for D_{off} during DCM 1, which is given in the appendix, is entered into equation (3.90) and solved. Due to the length of the solution, it is not presented here. Equations (3.90) and (3.91) are linearised, and the small-signal models of the CL boost converter operating in DCM 1 are found as

$$L_{Lk} \frac{d\tilde{i}_{L1}(t)}{dt} = \alpha_1 \tilde{v}_{in}(t) + \beta_1 \tilde{v}_{out}(t) + \gamma_1 \tilde{d}(t) + \delta_1 \tilde{i}_{L1}(t) \tag{3.92}$$

$$C_{out} \frac{d\tilde{v}_{out}(t)}{dt} = \alpha_2 \tilde{v}_{in}(t) + \beta_2 \tilde{v}_{out}(t) + \gamma_2 \tilde{d}(t) + \delta_2 \tilde{i}_{L1}(t) \tag{3.93}$$

As with D_{off}, the expressions for the α, β, γ, and δ coefficients are too large to present here. However, with the expressions for D_{off}, I_{S1}, V_{T1}, and the non-linearised equations (3.90) and (3.91) given in the appendix for all DCM modes, as well as the Matlab® code used to generate the α, β, γ, and δ coefficients, all information needed to solve for the small-signal models is given. From the solutions presented in the appendix, it is

clear to see that the magnetising inductance now plays quite a large role in the small-signal model.

3.5.4 Small-Signal Models of the CL Boost Converter in DCM 8

When the converter enters DCM with a duty cycle greater than 0.5, the first mode it enters is DCM 8, the waveforms of which are shown in Figure 3.15. Similar to DCM 1, there are six sub-modes of operation of the converter when operating in DCM 8. These are labelled D_1 to D_6 in Figure 3.15. Once again, if balanced operation is assumed, only one phase needs to be analysed, and D_6 can be eliminated from the analysis. The remaining sub-modes are presented in Figure 3.16 and Figure 3.17.

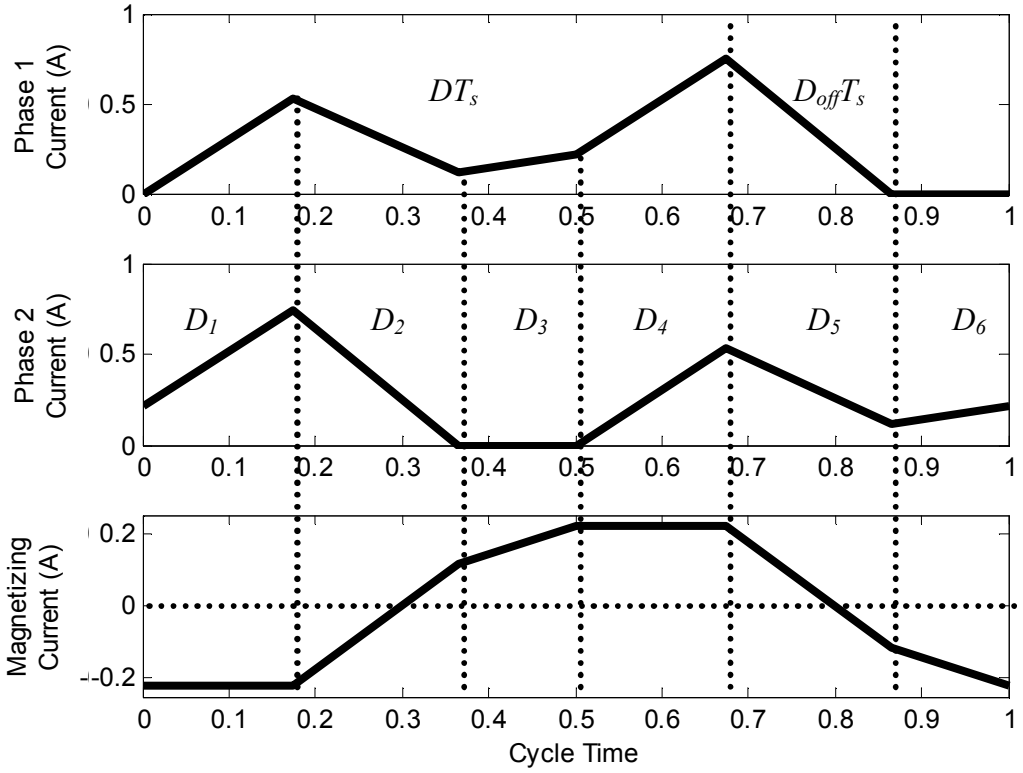


Figure 3.15. Phase and magnetising currents of CL boost converter operating in DCM 8.

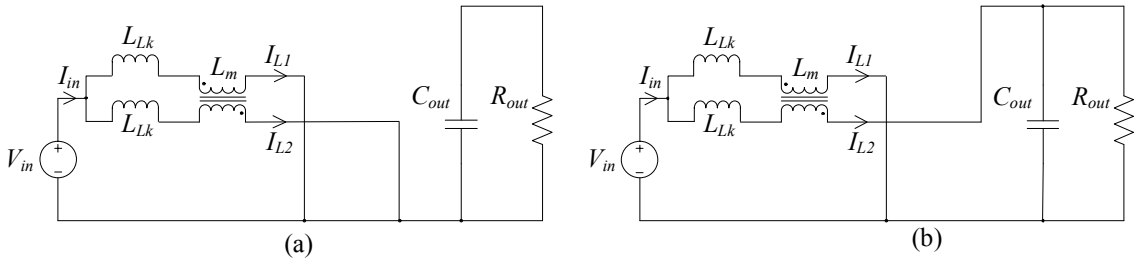


Figure 3.16. The sub-modes of operation of (a) D_1 and D_4 and (b) D_2 of DCM 1.

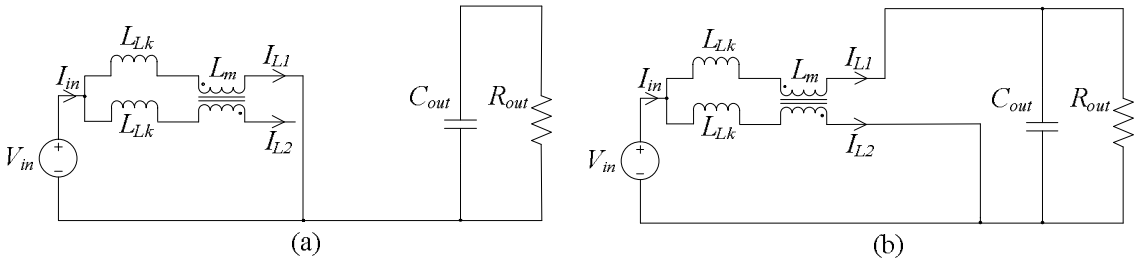


Figure 3.17. The sub-modes of operation of (a) D_3 and (b) D_5 of DCM 1.

Using Figure 3.15, Figure 3.16 and Figure 3.17, the dynamic equations of DCM 8 are found to be

$$L_{Lk}\frac{dI_{L1}}{dt} = V_{in}(D + D_{off}) - D_{off}V_{out} - V_{T1} \tag{3.94}$$

$$C_{out}\frac{dV_{out}}{dt} = 2I_{L1} - 2I_{S1} - \frac{V_{out}}{R_{out}} \tag{3.95}$$

The switch current of DCM 8 occurs during the sub-modes D_1 to D_4, as shown in Figure 3.18.

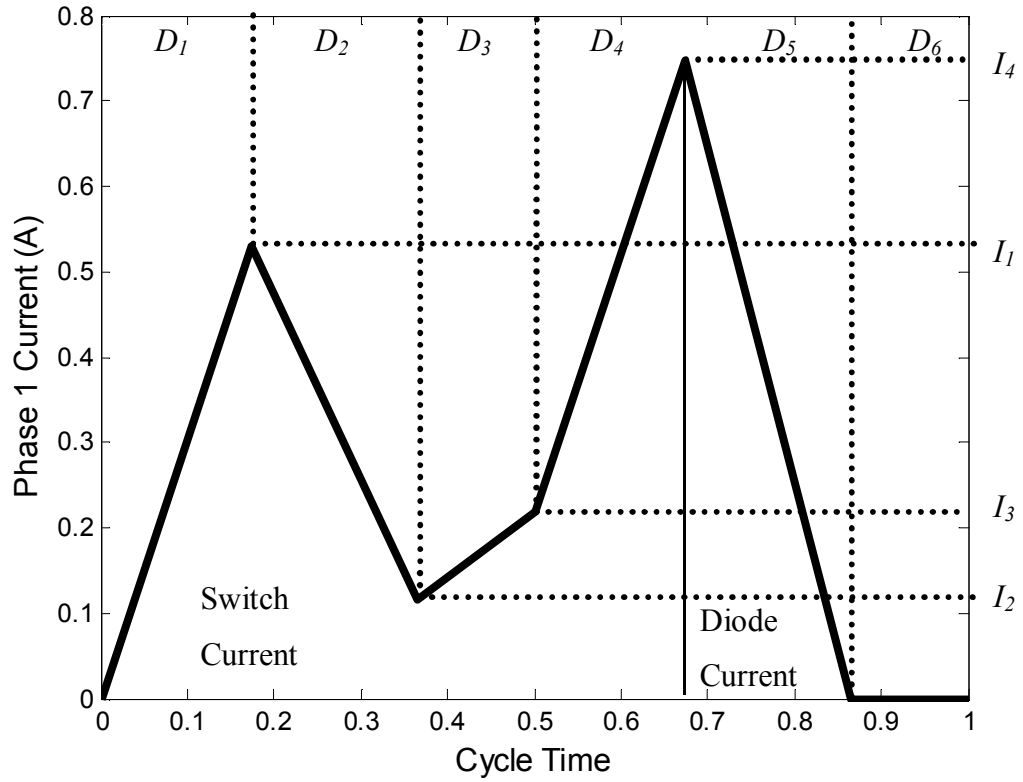


Figure 3.18. Phase 1 inductor current waveform of DCM 8.

By analysing the values of I_1, to I_4 of Figure 3.18 in a similar manner to Section 2.6.2, the switch current of DCM 8 is found to be

$$I_{S1} = \begin{bmatrix} \dfrac{V_{in}T_s(D_1 - D_1^{\,2} + D_{off}^{\,2} - D_{off})}{2(L_{Lk} + L_m)} + \ldots \\ \dfrac{T_s V_{in}(4D_1^{\,2} - 2D_1)}{4L_{Lk}} + \ldots \\ \dfrac{T_s(2V_{in} - V_{out})\left(D_{off} - D_{off}^{\,2}\right)}{4L_{Lk}} + \ldots \\ \dfrac{V_{out}D_{off}T_s(1 - D_{off})}{4(L_{Lk} + 2L_m)} \end{bmatrix} \tag{3.96}$$

Once again, to complete the inductor voltage equation, the magnetizing term V_{T1} must be found where

$$V_{T1} = \sum_{x=1}^{5} D_x L_m \frac{dI_{mx}}{dt} \tag{3.97}$$

where x denotes the sub-mode of operation. By analysing the magnetizing waveform given in Figure 3.18, it is evident that

$$\begin{aligned} \Delta I_{m1} &= \Delta I_{m4} = 0 \\ \Delta I_{m2} &= -\Delta I_{m5} \end{aligned} \tag{3.98}$$

Hence

$$V_{T1} = L_m \frac{\Delta I_{m3}}{T_s} \tag{3.99}$$

The change in magnetizing current during the cycle time D_3 is given by the expression

$$\Delta I_{m3} = \frac{V_{in}D_3T_s}{L_{Lk} + L_m} \tag{3.100}$$

From Figure 3.18, the cycle time D_3 can be expressed as

$$D_3 = 1 - D - D_{off} \tag{3.101}$$

Therefore, the magnetizing element of the inductor voltage equation is expressed as

$$V_{T1} = L_m \frac{V_{in}(1 - D - D_{off})}{L_{Lk} + L_m} \tag{3.102}$$

Finally, the equation for D_{off} for DCM 8, given in the appendix, is entered into equation (3.94) and (3.100), and solved. Due to the length of the solution, it will not be presented here. The expressions for V_{T1}, D_{off} and I_{S1} are inserted into equations (3.94) and (3.95), and are linearised to find the small-signal models of the CL boost converter operating in DCM 8.

$$L\frac{d\tilde{i}_{L1}(t)}{dt} = \alpha_1\tilde{v}_{in}(t) + \beta_1\tilde{v}_{out}(t) + \gamma_1\tilde{d}(t) + \delta_1\tilde{i}_{L1}(t) \tag{3.103}$$

$$C_{out}\frac{d\tilde{v}_{out}(t)}{dt}=\alpha_2\tilde{v}_{in}(t)+\beta_2\tilde{v}_{out}(t)+\gamma_2\tilde{d}(t)+\delta_2\tilde{i}_{L1}(t) \tag{3.104}$$

As with DCM 1, the expressions for the α, β, γ, and δ coefficients are too large to present here. However, as discussed in Section 3.5.3, with the expressions for D_{off}, I_{S1}, V_{T1}, and the non-linearised expressions given in the appendix for all DCM modes, as well as the Matlab® code used to generate the α, β, γ, and δ coefficients, all information needed to solve for the small-signal models is given. Once again, it is evident that the magnetising inductance plays a large role in the small-signal models.

3.6 Verification of Small-Signal Models

The power electronics package SimPowerSystems in Matlab®/Simulink [3.17] was used to build and simulate an accurate circuit model of 1 kW CL boost converter prototype, presented in Figure 3.19.

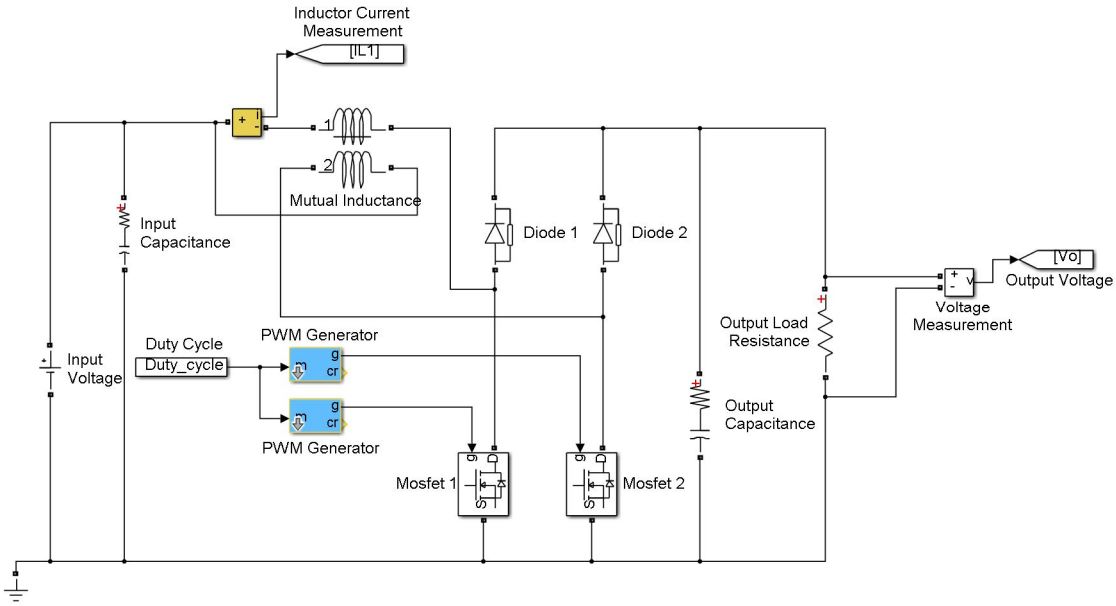


Figure 3.19. Matlab®/Simulink block Diagram of the 1 kW CL boost converter prototype.

An algorithm was developed to generate a sine wave duty cycle with a dc bias and sweeping frequency. For example, when the converter is operating in CCM 1, the operating point of the duty cycle is given as 0.5, with a perturbation of ±0.03, with the frequency sweep beginning at 10 Hz, and ending at 10 kHz. The output voltage is then measured, and its amplitude and phase compared to the amplitude and phase of the input duty cycle. The magnitude and phase difference is then calculated from these measurements, and a transfer function and Bode plot are estimated from the results.

3.6.1 Coupled-Inductor CCM Small-Signal Model Verification

The input voltage, output voltage, duty cycle and phase current are set to ensure the converter operates in CCM. The open-loop duty cycle-to-output voltage transfer function is then estimated, and compared with the duty cycle-to-output voltage transfer function obtained in Section 3.4.1. The results are resented in Figure 3.20.

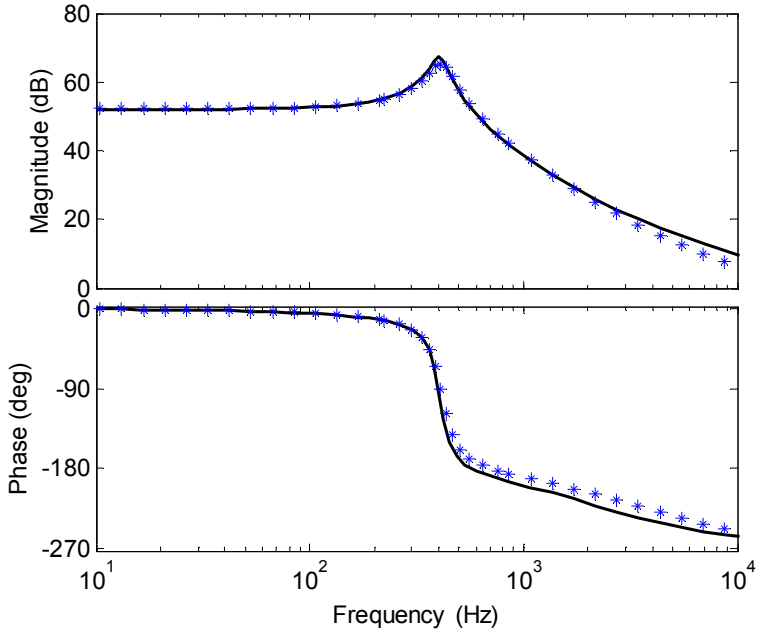


Figure 3.20. Frequency response of simulated (*) and calculated (-) $G_{vd}(s)$, the duty cycle –to-output voltage transfer function of the coupled-inductor boost converter operating in CCM.

As can be seen in Figure 3.20, there is an excellent match between the estimated and calculated transfer functions for the CL converter operating in CCM.

An experimental frequency sweep was performed on the 1 kW laboratory prototype and compared to a calculated frequency response. The results are presented in Figure 3.21. It should be noted that, due to resolution issues, and the large attenuation at higher frequencies, only results up to 1 kHz are considered accurate.

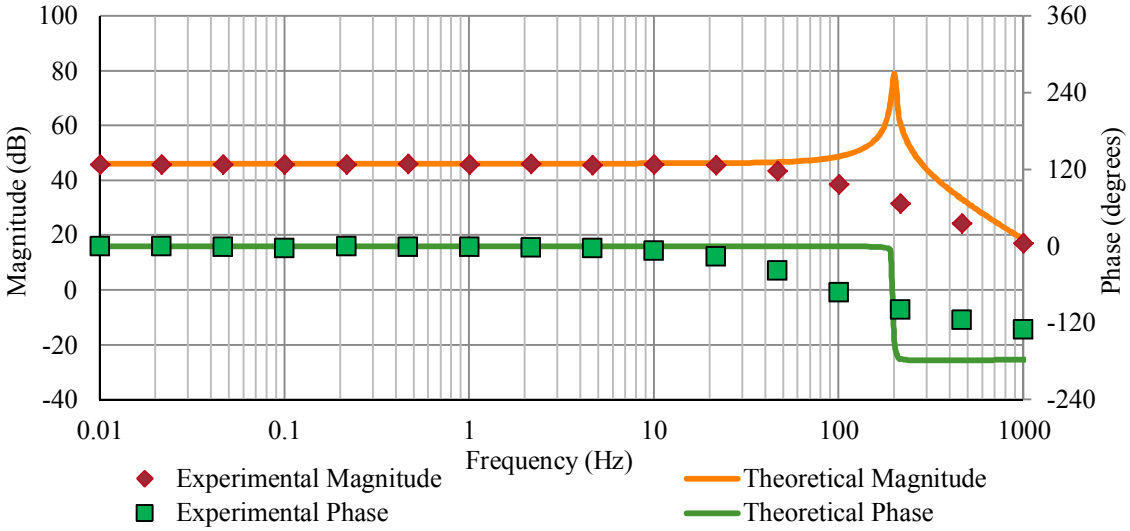


Figure 3.21. Experimental Frequency sweep vs. theoretical frequency sweep of the CL boost converter operating in CCM for $G_{vd}(s)$, the duty cycle-to-output voltage transfer function.

As can be seen from Figure 3.20, the dc gain and gain at high frequencies are similar. A major difference is seen between 100 Hz and 1 kHz. This is due to the fact that the equivalent series resistance (ESR) of the output capacitor is not taken into account in the derived transfer functions. In real converters, this capacitor ESR dampens the

resonance of the converter, making the magnitude and phase change much more gradual than what is calculated. This is verified by inserting the capacitance ESR into the Simulink simulation and repeating the frequency sweep, the results of which are presented in Figure 3.22. As can be seen, the resonance has now completely disappeared.

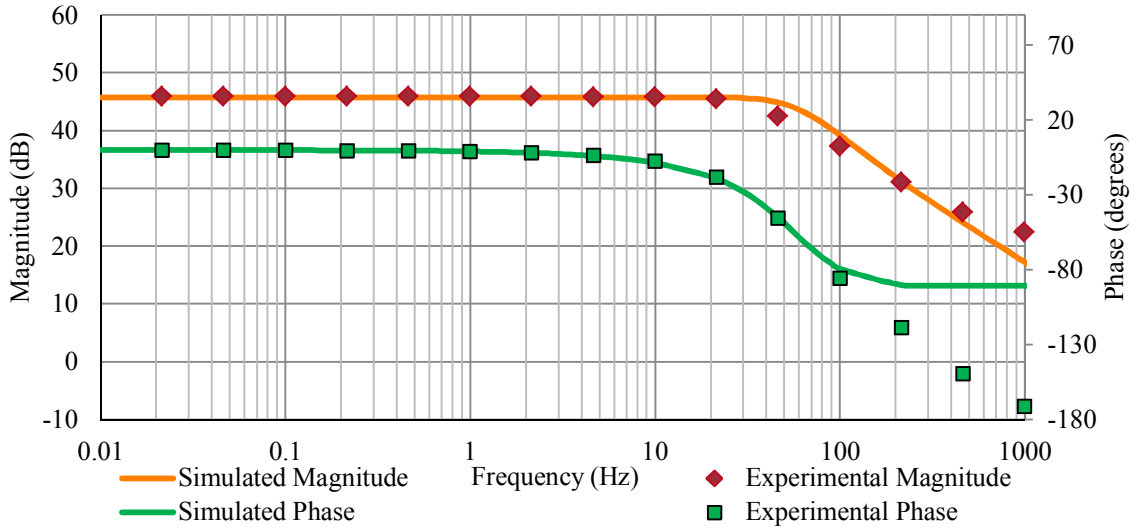


Figure 3.22. Experimental Frequency sweep vs. simulated frequency sweep of the CL boost converter operating in CCM for $G_{vd}(s)$, the duty cycle-to-output voltage transfer function.

3.6.2 Coupled-Inductor DCM 4 Small-Signal Model Verification

The input voltage, output voltage, duty cycle and phase current are set to ensure the converter operates in DCM 4. The open loop duty cycle-to-output voltage transfer function is then estimated, and compared with the duty cycle-to-output voltage transfer function obtained in Section 3.4.2. The results are presented in Figure 3.23.

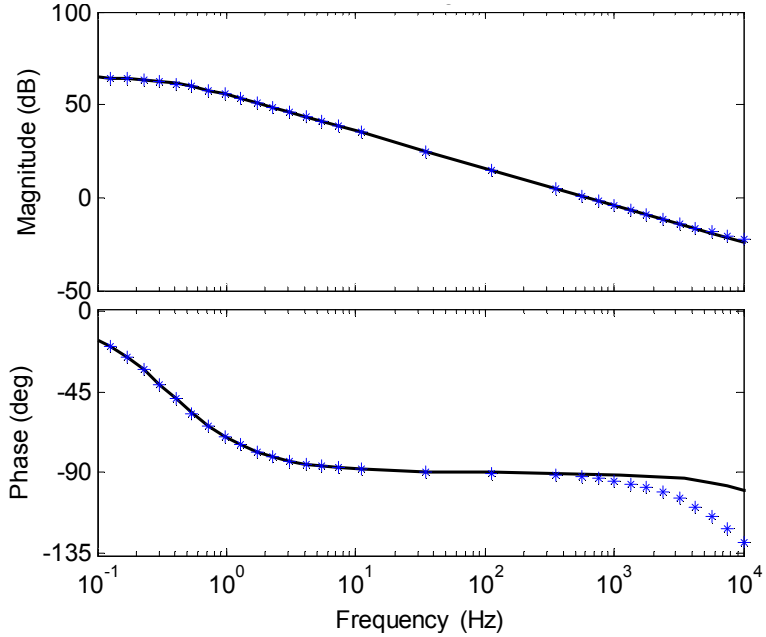


Figure 3.23. Frequency Response of simulated (*) and calculated (-) $G_{vd}(s)$, the duty cycle –to-output voltage transfer function of the coupled-inductor boost converter operating in DCM 4.

As can be seen from Figure 3.23, the estimated frequency response of DCM 4 follows the frequency response of the calculated transfer function closely. The results begin to diverge at 10 kHz.

3.6.3 Coupled-Inductor DCM 8 Small-Signal Model Verification

The input voltage, output voltage, duty cycle and phase current are set to ensure the converter operates in DCM 8. The open loop duty cycle-to-output voltage transfer function is then estimated, and compared with the duty cycle-to-output voltage transfer function obtained in Section 3.4.4. The results are resented in Figure 3.24.

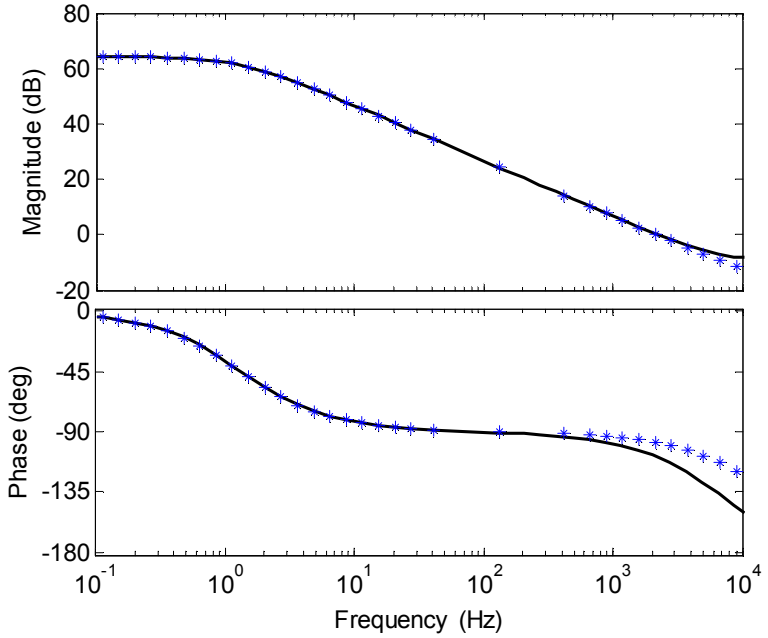


Figure 3.24. Frequency Response of simulated (*) and calculated (-) $G_{vd}(s)$, the duty cycle –to-output voltage transfer function of the coupled-inductor boost converter operating in DCM 8.

Once again, the estimated frequency response of DCM 8 follows the frequency response of the calculated transfer function closely. The results do begin to diverge at 10 kHz.

3.6.4 Coupled-Inductor DCM 2 Small-Signal Model Verification

An experimental frequency sweep was performed on the 1 kW laboratory prototype and compared to a calculated frequency response for verification of DCM 2. The results are presented in Figure 3.25.

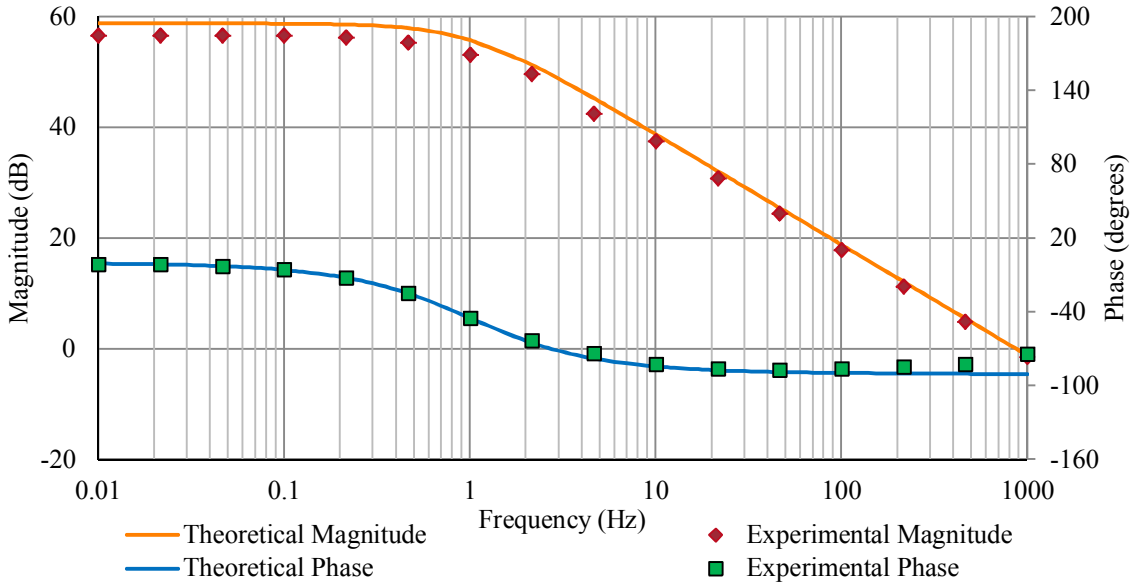


Figure 3.25. Experimental Frequency sweep vs. theoretical frequency sweep of the CL boost converter operating in DCM 2 for $G_{vd}(s)$, the duty cycle-to-output voltage transfer function.

3.6.5 Coupled-Inductor DCM 9 Small-Signal Model Verification

As with DCM 2, an experimental frequency sweep was performed on the 1 kW laboratory prototype and compared to a calculated frequency response for verification of DCM 9. The results are presented in Figure 3.26.

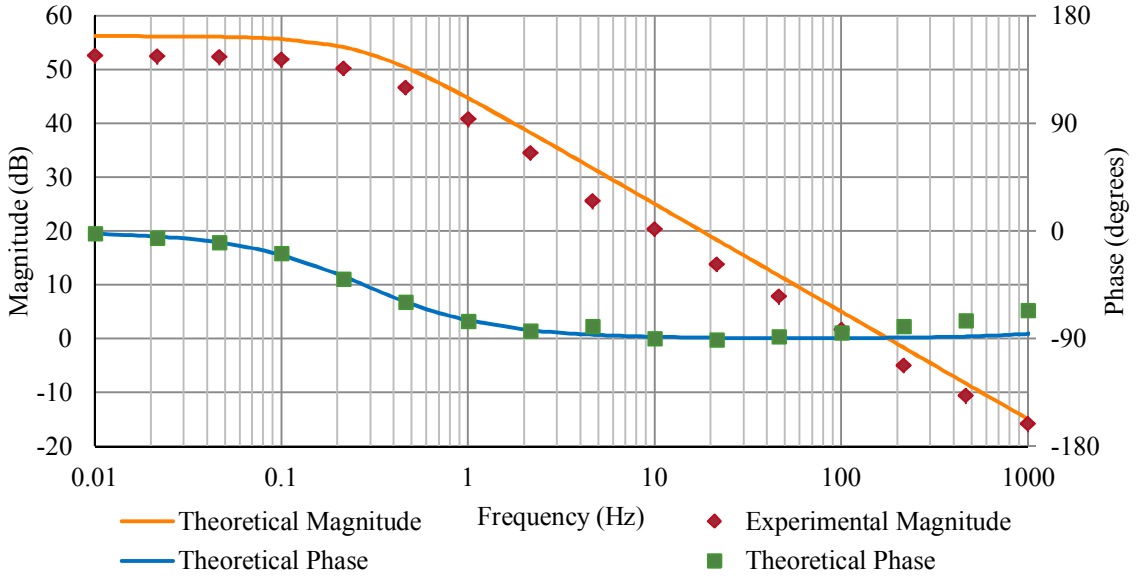


Figure 3.26. Experimental Frequency sweep vs. theoretical frequency sweep of the CL boost converter operating in DCM 9 for $G_{vd}(s)$, the duty cycle-to-output voltage transfer function.

As can be seen from Figure 3.25 and Figure 3.26, a slight offset in the magnitude is evident. This is due to the fact that the MOSFETs in the laboratory prototype contains an equivalent output capacitance of about 1.5 nF. This capacitance causes resonance to occur when the current drops to zero when operating in DCM, as shown in Figure 3.26.

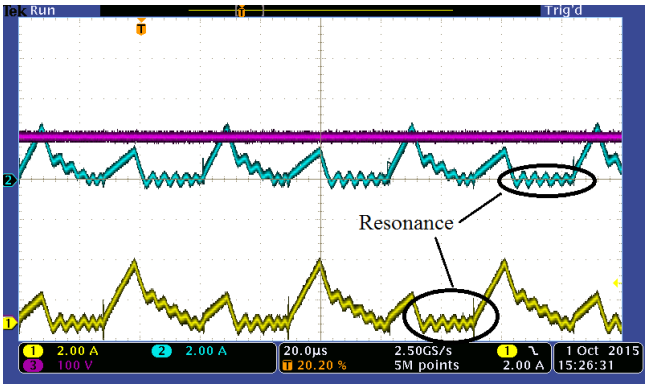


Figure 3.27. Current Waveforms of DCM with showing resonance due to the equivalent output capacitance of MOSFETs.

However, this capacitance is not included in the derivation of the small-signal model, hence giving rise to the difference in the gain. What is also evident at higher frequencies is the effect of the output capacitor equivalent series resistance (ESR), which causes the slight increase in phase of the experimental results. Again, this ESR is not included in the derivation.

3.7 Comparison of 2L and CL CCM Small-Signal Models

For appropriate comparison between CCM operation of the 2L and CL converters, suitable phase, leakage and magnetizing inductances must be chosen. When designing a dc-dc converter, one of the chief design considerations is the maximum allowed peak-to-peak phase current, which can dictate the maximum rating of the semi-conductor devices. Hence, to compare the 2L converter to a CL converter, both converter designs assume identical phase current ripples at a given CCM operating point. For the purpose of this analysis, the magnetizing inductance of the CL boost converter is set to be N times the leakage inductance, where N is the ratio of magnetizing inductance to Leakage inductance i.e.

$$L_m = L_{Lk} N \tag{3.105}$$

Table 3.1 provides the calculations for the leakage inductance of a CL boost converter operating with the same CCM worst-case peak-to-peak phase current ripple as an equivalent 2L converter.

Table 3.1. Leakage inductance values of the boost CL converters for the same peak-to-peak conditions as a 2L converter.

	$D < 0.5$	$D > 0.5$
L_{Lk}	$\frac{1}{2} L_1 \left(\frac{1-2D}{1-D} + \frac{1}{(2N+1)(1-D)} \right)$	$L_1 \left(1 - \frac{N}{D(2N+1)} \right)$

From Table 3.1, it is evident that when N is greater than zero, the leakage inductance will always be less than the phase inductance. In order to see the effect this has on the system dynamics, the Bode plots of the 2L and CL boost converter transfer functions are compared in Figure 3.28 to Figure 3.30.

3.7.1 Duty Cycle-to-Output voltage Frequency Response

Figure 3.28 compares the duty cycle-to-output voltage frequency responses of the 2L and CL converters operating in CCM. As can be seen, the lower value of leakage inductance in the CL converters causes resonance to occur at a slightly higher frequency. It also causes the phase shift from 0^o to -180^o to occur at a higher frequency.

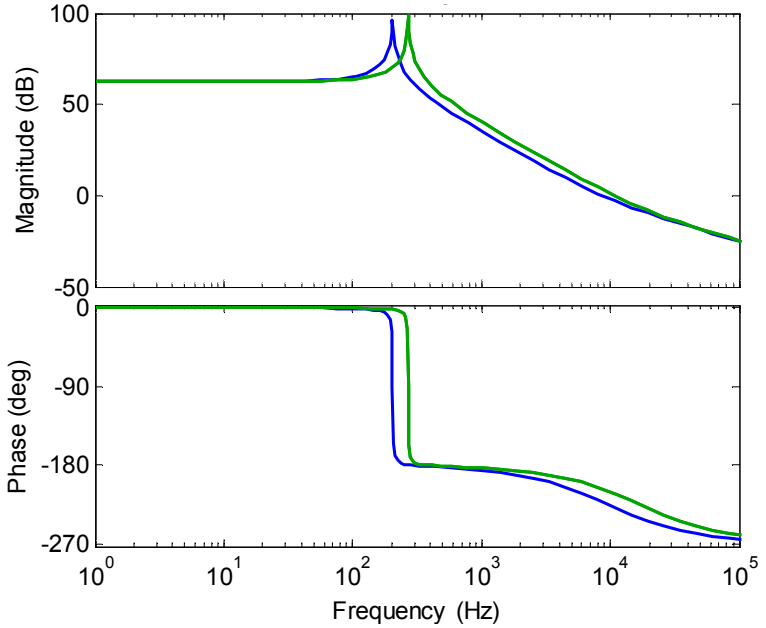


Figure 3.28. Bode plots of the transfer function G_{vd}(s) for the 2L (blue) and CL (green) boost converters.

3.7.2 Duty Cycle-to-Inductor Current Frequency Response

Figure 3.29 compares the duty cycle-to-inductor current frequency responses of the 2L and CL converter operating in CCM. Once again, resonance occurs at a slightly higher frequency in the CL converter than in the 2L converter, as does the phase shift. The gain of the CL converter is also higher at higher frequencies.

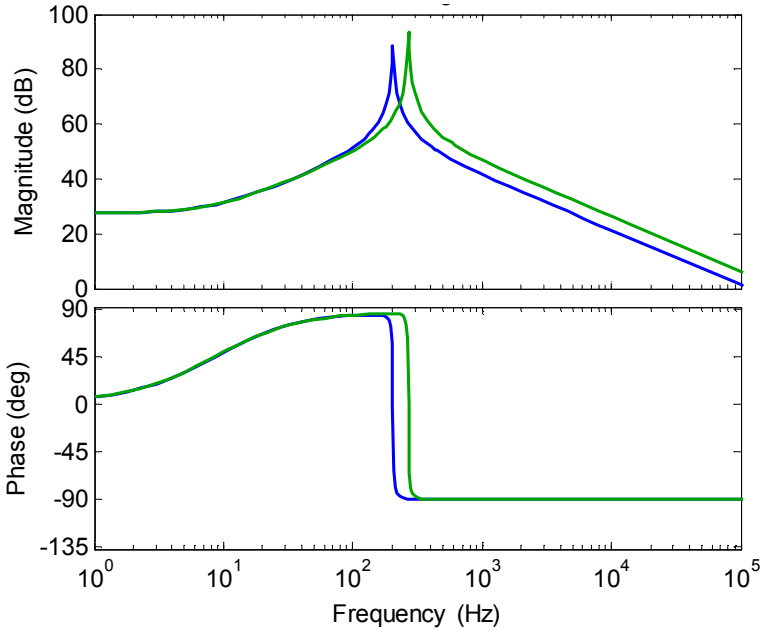


Figure 3.29. Bode plots of the transfer function G_{id}(s) for the 2L (green) and CL (blue) boost converters.

3.7.3 Inductor Current-to-Output Voltage Frequency Response

Figure 3.30 compares the inductor current-to-output voltage frequency responses of the 2L and CL converter operating in CCM. As can be seen, the responses are identical up to 1 kHz. This is to be expected due to the fact that the relationship between the dc

phase current and the output voltage is a simple RC network, in which the phase inductance does not play a part.

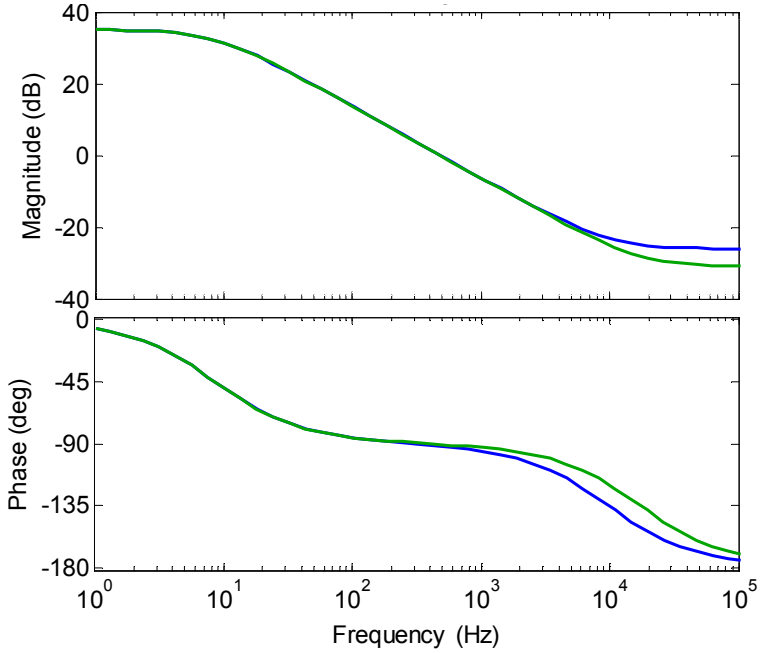


Figure 3.30. Bode plots of the transfer function G_{id}(s) for the 2L (green) and CL (blue) boost converters.

3.8 Comparison of 2L and CL DCM Small-Signal Models

In order to continue a like-for-like comparison of the 2L and CL converters, the same leakage and phase inductance inductances used in the previous section for CCM will be used in this section for DCM. Due to the fact that the gain of a 2L DCM converter is different to that of a CL DCM converter, it should be noted that, as well as different inductance values, the duty cycle will also be different.

3.8.1 Duty Cycle-to-Output Voltage Frequency Response of DCM 1

Figure 3.31 compares the duty cycle-to-output voltage frequency responses of the 2L converter operating in DCM and the CL converter operating in DCM 1.

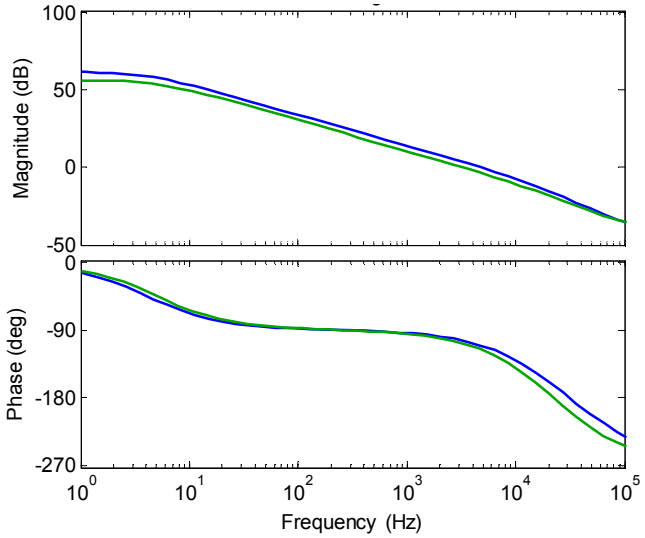


Figure 3.31. Bode plots of the transfer function $G_{vd}(s)$ for the 2L (blue) and CL (green) boost converters in DCM and DCM 1.

3.8.2 Duty Cycle-to-Output Voltage Frequency Response of DCM 2

Figure 3.32 compares the duty cycle-to-output voltage frequency responses of the 2L converter operating in DCM and the CL converter operating in DCM 2.

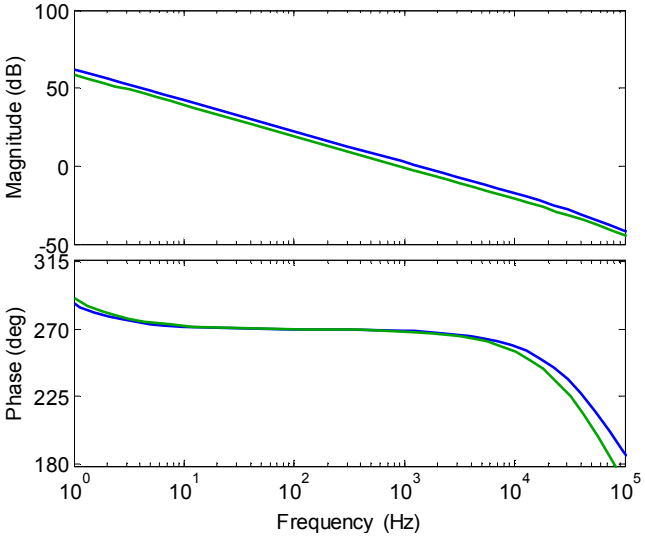


Figure 3.32. Bode plots of the transfer function $G_{vd}(s)$ for the 2L (blue) and CL (green) boost converters in DCM and DCM 2.

3.8.3 Duty Cycle-to-Output Voltage Frequency Response of DCM 3

Figure 3.33 compares the duty cycle-to-output voltage frequency responses of the 2L converter operating in DCM and the CL converter operating in DCM 3.

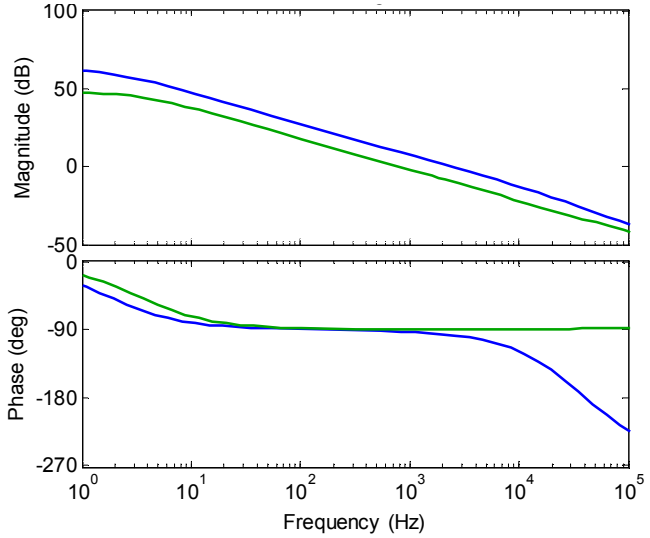


Figure 3.33. Bode plots of the transfer function $G_{vd}(s)$ for the 2L (blue) and CL (green) boost converters in DCM and DCM 3.

3.8.4 Duty Cycle-to-Output Voltage Frequency Response of DCM 4

Figure 3.34 compares the duty cycle-to-output voltage frequency responses of the 2L converter operating in DCM and the CL converter operating in DCM 4.

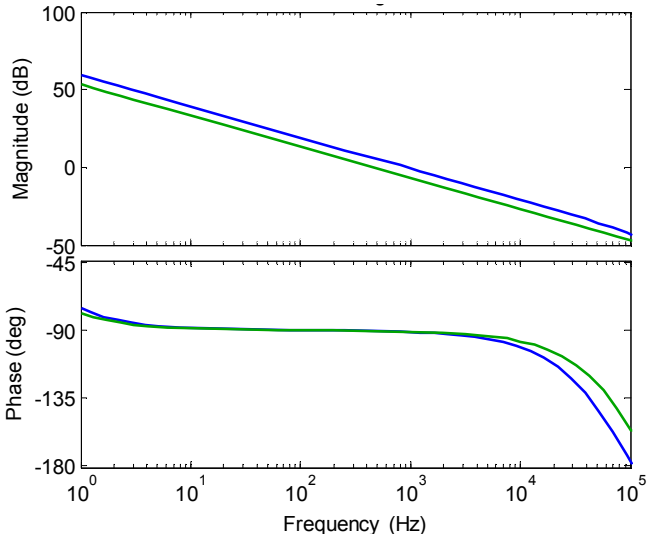


Figure 3.34. Bode plots of the transfer function $G_{vd}(s)$ for the 2L (blue) and CL (green) boost converters in DCM and DCM 4.

3.8.5 Duty Cycle-to-Output Voltage Frequency Response of DCM 7

Figure 3.35 compares the duty cycle-to-output voltage frequency responses of the 2L converter operating in DCM and the CL converter operating in DCM 7.

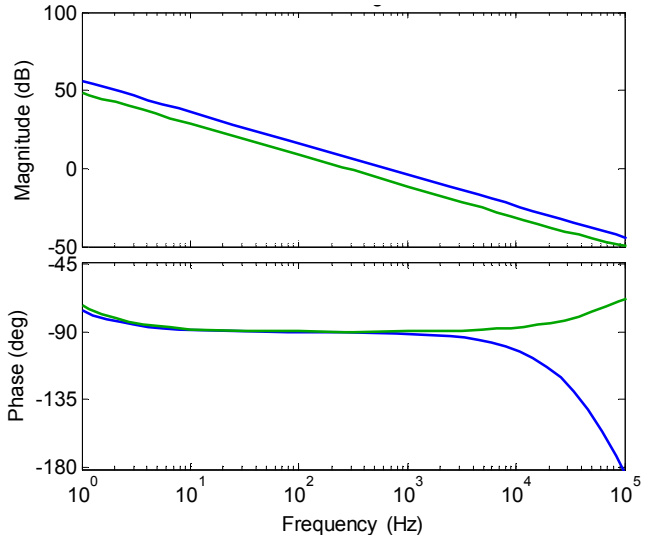


Figure 3.35. Bode plots of the transfer function $G_{vd}(s)$ for the 2L (blue) and CL (green) boost converters in DCM and DCM 7.

3.8.6 Duty Cycle-to-Output Voltage Frequency Response of DCM 8

Figure 3.36 compares the duty cycle-to-output voltage frequency responses of the 2L converter operating in DCM and the CL converter operating in DCM 8.

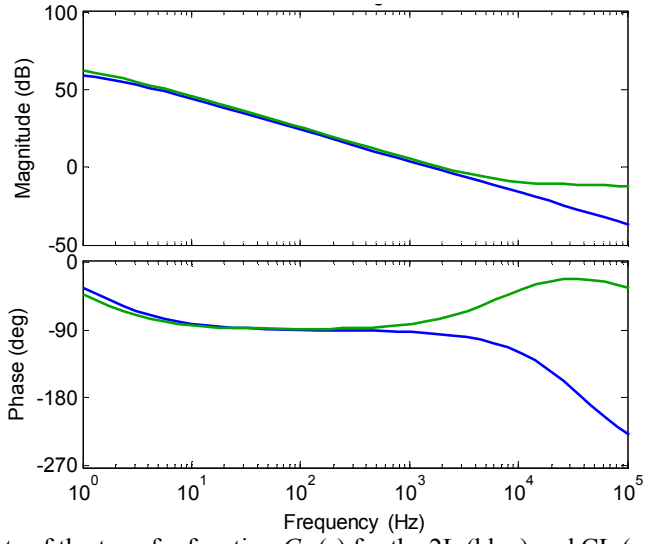


Figure 3.36. Bode plots of the transfer function $G_{vd}(s)$ for the 2L (blue) and CL (green) boost converters in DCM and DCM 8.

3.8.7 Duty Cycle-to-Output Voltage Frequency Response of DCM 9

Figure 3.37 compares the duty cycle-to-output voltage frequency responses of the 2L converter operating in DCM and the CL converter operating in DCM 9.

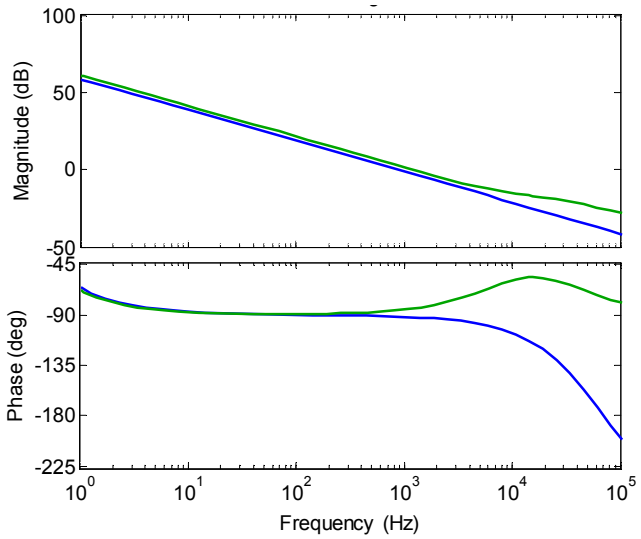


Figure 3.37. Bode plots of the transfer function G_{vd}(s) for the 2L (blue) and CL (green) boost converters in DCM and DCM 9.

As can be seen from the comparisons, at lower frequencies, the frequency responses of both the 2L and CL converters are quite similar, except for a slight difference in the magnitudes. However, large deviations in the phase responses are evident at higher frequencies.

3.8.8 Discussion on Comparisons

As can be seen from Figure 3.28 to Figure 3.37, there is often very little difference between the frequency response s of the 2L and CL converters. Most differences are the slightly different gain, such as in Figure 3.33, Figure 3.34, and Figure 3.35. Other differences are the converters poles and zeros occurring at slightly higher frequencies, such as in Figure 3.34. However, the Bode plots of DCM 7, DCM 8, and DCM 9, differ quite a bit from their discrete inductor counterparts at higher frequencies. However, these high frequencies are often disregarded due to the fact that the control loops will rarely, if ever, operate at such frequencies.

An argument can be made as to whether it is better to use the relatively complex coupled-inductor small-signal models, or the simpler 2L models. It should be noted though, that these comparisons are for converters with similar operating characteristics i.e. the inductance values of the 2L and CL converter were designed to give the same worst-case peak-to-peak current ripple. If the design criteria is different, such as comparable boxed-volume, or cost of manufacture, it may not be viable to use the 2L models, as the equivalent inductance values may not suitably represent the CL converter.

Another advantage of using the models from the CL converter over the 2L converter is the coupling factor. Since coupled-inductor can have varying levels of magnetic

coupling, it would be impossible to see the effect of differing the coupling factor when utilising the “l small-signal models. However, since the models of the CL converter take into account both the leakage and magnetising inductances, either one can be varied, and the effects on the frequency responses easily found.

3.9 Conclusions

This chapter focused on the small-signal models of the 1L, 2L and CL converters. The duty cycle-to-output voltage, duty cycle-to-inductor current and inductor current-to-output voltage transfer functions were derived for all three converters, both in CCM and DCM. The small-signal models of the CL boost converter were verified via simulation using Matlab®/Simulink, and experimentally using the 1 kW laboratory prototype. The experimental results also present the effect of the MOSFET output capacitance as well as the ESR of the output capacitor. Finally, all CCM and DCM small-signal models of the CL converter were compared against their 2L counterparts.

3.10 References

[3.1] M. Grotzbach, and R. Von Lutz, "Unified modelling of rectifier-controlled dc-power supplies," *IEEE Power Electronics Specialists conference*, pp. 304-315, June 1984.

[3.2] F. Guinjoan, A. Poveda, L. Martinez, L. G. Vicuna, and J. Majo, "An accurate small-signal modelling approach for switching dc-dc converters," *IEEE International Symposium on Circuits and Systems*, pp. 2351-2354, May 1993.

[3.3] J. M. F. D. Costa, and M. M. Silva, "Small-signal models of quasi-resonant converters," *IEEE International Symposium on Industrial Electronics*, pp. 258-262, July 1997.

[3.4] S. Liu, and L. W. Nagel, "Small-signal MOSFET models for analog circuit design," *IEEE Journal of Solid-State circuits*, vol. 17, no. 6, pp. 983-998, December 1992.

[3.5] J. S. Linder, "Small-signal model of the parallel-plane vacuum diode," *Electronic Letters*, vol. 1, no. 5, pp. 141-142, July 1965.

[3.6] H. R. Visser, and P. P. J. van den Bosch, "Dynamic modelling of switching systems," *Fifth European conference on Power Electronics and Applications*, pp. 342-346, September 1993.

[3.7] E. Ugur, and B. Vural, "Comparison of different small-signal modelling methods for bidirectional dc-dc converters," *International Conference on Renewable Energy Research and Applications*, pp. 913-915, October 2014.

[3.8] M. J. Schutten, and D. A. Torrey, "Improved small-signal analysis for the phase-shifted PWM power converter," *IEEE Transactions on Power Electronics*, vol. 18, no. 2, pp. 659-669, March 2003.

[3.9] X. Xiaofeng, "Small-signal model for current mode control full-bridge phase shifted ZVS converter," *International Power Electronics and Motion Control Conference*, pp. 514-518, August 2000.

[3.10] A. Ayachit, and M. K. Kazimierczuk, "Open-loop small-signal transfer functions of the quadratic buck PWM dc-dc converter in CCM," *Annual Conference of the IEEE Industrial Electronics Society*, pp. 1643-1649, October 2014.

[3.11] L. Hsiu, W. Kerwin, and A. F. Witulski, "Small-signal models of a zero-voltage-switched SEPIC dual converter with a coupled-inductor," *Annual IEEE Power Electronics Specialists Conference*, pp. 814-820, June 1994.

[3.12] M. Xu, J. Zhou, K. Yao, and F. C. Lee, "Small-signal modelling of a high bandwidth voltage regulator using coupled inductors," *IEEE Transactions on Power Electronics*, vol. 22, no. 2, pp. 399-406, March 2007.

[3.13] B. Bryant, and M. K. Kazimierczuk, "Open-loop power-stage stage transfer functions relevant to current-mode control of boost PWM converter operating in

CCM," *IEEE Transactions on Circuits and Systems I*, vol. 52, no. 10, pp. 2158-2164, October 2005.

[3.14] R. D. Middlebrook, "Modelling current-programmed buck and boost regulators," *IEEE Transactions on Power Electronics*, vol. 4, no. 1, pp. 36-52, January 1989.

[3.15] S. Tang, K. Goto, Y. Imamura and M. Shoyama, "Dynamic characteristics model of bi-directional dc-dc converter using state-space averaging method," *Intelec 2012*, pp. 1-5, September 2012.

[3.16] R. W. Erickson (1997), *Fundamentals of Power Electronics*, Kluwer Academic Publishers.

[3.17] https://uk.mathworks.com/products/simulink/?requestedDomain=www.mathworks.com (Accessed on 29/11/2016).

4 COUPLED-INDUCTOR INTERLEAVED CONVERTER CLOSED-LOOP PI DIGITAL CONTROL

One of the most common applications of power converters is voltage regulation. It is critical for a dc-dc converter, whether it functions as a step-up or step-down converter, to produce a well-regulated and stable output voltage and current. As discussed in Chapter 1, the load profile of a typical Lithium-ion battery, as well as the current-voltage curve of PV cells signify that power converters must be able to give a regulated and stable output voltage at a varying load. The power converter is expected to operate at the highest efficiency, while still being able to quickly and effectively reject any disturbances in the system. This chapter focuses on the implementation of a closed-loop digital PI controller for a coupled-inductor dc-dc converter.

4.1 Introduction

The control of dc-dc converters is a well-established area of research in the power electronics community with many power electronics books dedicating entire chapters to controller design and implementation [4.1]-[4.3]. A traditional controller scheme is presented in Figure 4.1. The controller compares the output of a system, $G(s)$, to a desired output, X^*. The error from this comparison is then manipulated internally by the controller, $C(s)$, to give an input into the system which corrects the output X. This output is measured by the sensor, $H(s)$, and once again compared to the set-point.

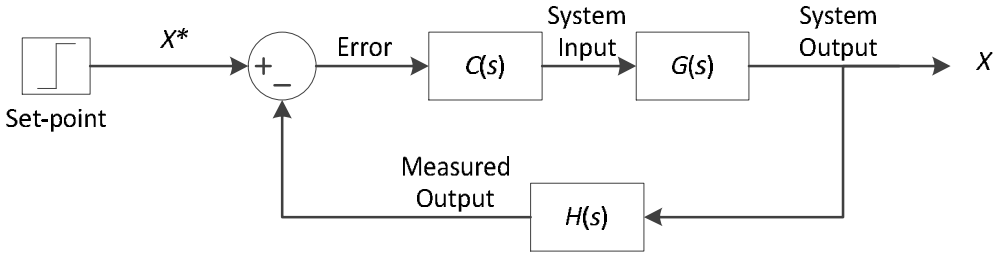


Figure 4.1. Typical closed-loop control block diagram.

By analysing the block diagram, the closed-loop system gain is derived as

$$B(s) = \frac{C(s)G(s)}{1 + C(s)G(s)H(s)} \tag{4.1}$$

It should be noted, however, that the set-point must take into account the gain of the sensor $H(s)$. In most closed-loop systems, the steady-state gain of the system is designed to ensure that the output equals the input i.e.

$$B(s) = 1 \tag{4.2}$$

Since the $G(s)$ and $H(s)$ are fixed, the controller gain $C(s)$ is selected to ensure equation (4.2) is met.

The objective of this chapter is to design the controller for the coupled-inductor two-phase interleaved (CL) dc-dc converter using the small-signal models derived in Chapter 3. Section 4.2 discusses and compares the various types of control utilised in dc-dc converters. Section 4.3 presents the design of a controller for a single-phase (1L) and discrete-inductor two-phase (2L) boost converter, while Section 4.4 presents the design of a controller for a CL dc-dc converter operating in CCM and DCM 4. Section 4.5 improves on the design of the CL converter controllers and implements the new controllers in CCM, DCM 1 and DCM 8. Section 4.6 implements “Anti-Bump” control for the CL converter in CCM and DCM 8.

4.2 DC-DC Converter Control

In the area of dc-dc converters, there are four main types of control schemes that are most often implemented in industry. These are voltage-mode control, hysteretic control, peak-current-mode control, and average-current-mode control.

4.2.1 Voltage Mode Control

Voltage-Mode Control (VMC) of a dc-dc converter utilises a single control loop to force the output voltage of the converter to follow a set-point specified by the user. The control scheme of VMC, presented in Figure 4.2, measures the output voltage and compares this value to the desired output voltage. A single controller then takes the error from this comparison and calculates the duty cycle needed to eliminate the error.

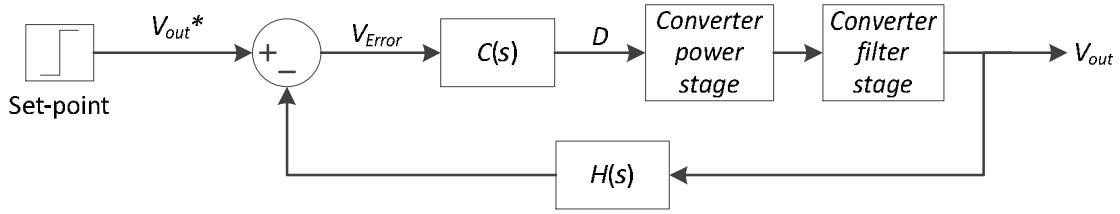


Figure 4.2. Voltage-mode control scheme for a dc-dc converter.

Much research has been done on the utilisation of VMC due to its relatively simple implementation and low cost [4.4]-[4.7]. Not only does VMC show good noise immunity, since the only measured state is the output voltage, current sensors are unnecessary, which reduces system cost. The need to design only one controller also reduces the complexity of the system. However, there are disadvantages to using VMC. For one, it is much harder to balance current in multi-phase systems without an additional control scheme. Another drawback is the relative difficulty in designing the controller itself for certain converter topologies. For example, while the design of VMC for a buck converter is straightforward, the right-half-plane (RHP) zero that appears in a boost converter complicates the design.

This RHP zero occurs due to the fact that, during the on-time of the switch, the load is disconnected from the input, and supplied by the capacitor. To increase the output voltage in a boost converter, the duty cycle increases, and the load is disconnected from the source for a longer period of time, meaning the capacitor must supply more charge than it had previously stored. The controller must be designed in such a way that the open-loop crossover frequency is high enough to reject any disturbances and track the set-point quickly, but at a low enough frequency so as to not be affected by the RHP zero. The transfer functions derived in Chapter 3 show that the RHP zero of the 2L boost converter occurs at the frequency

$$f = \frac{2R_{out}(1-D)^2}{2\pi L} \tag{4.3}$$

where R_{out} is the output load of the converter, D is the duty cycle, and L is the phase inductance.

4.2.2 Hysteretic Control

Hysteretic control, as presented in Figure 4.3, is one of the simplest control methods for dc-dc converters. Hysteretic control allows stable closed-loop operation of a dc-dc converter with only a single comparator with a small amount of hysteresis, and hence, does not need the additional cost of operational amplifiers or microcontrollers. It is also one of the fastest topologies, as the reaction time of the loop is determined only by the propagation delay of the comparator and the gate driver.

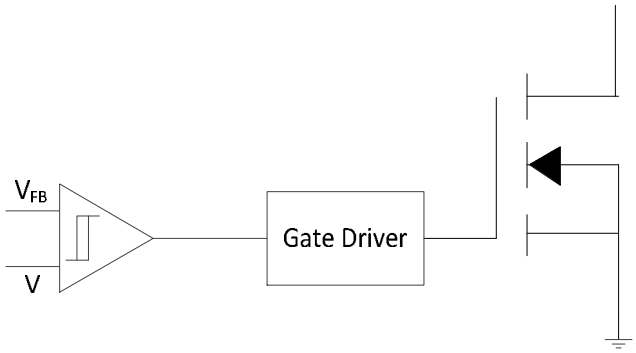


Figure 4.3. Block diagram of hysteretic control.

The major disadvantage of hysteretic control is the inherent switching frequency variation. Since there is no clock signal in the control scheme, the frequency is dependent on the size of the hysteresis. This is unsuitable for multi-phase dc-dc converters where synchronization of the phases is essential. Other disadvantages include steady-state error in high gain converters, as well as the requirement for a high output capacitor equivalent series resistance (ESR) [4.18]. Hence, hysteretic control is usually only considered for low-power, low cost applications, such as children's toys or other small battery-operated goods. Several papers look to improve hysteretic control by introducing an additional current loop, as well as fixed-frequency applications [4.8]-[4.10].

4.2.3 Peak-Current Mode Control

Peak-Current-Mode Control (PCMC), presented in Figure 4.4, is one of the most popular control structures for dc-dc converters. Some of the advantages of PCMC include good stability and performance characteristics, the option to implement current balancing techniques in multi-phase converters and inherent short circuit protection. It

is also easier to implement in the analogue domain. The major advantage of using PCMC, especially for boost converters, is the ability to have a fast inner loop, which helps with rejecting disturbances quickly. Since the RHP zero of a boost converter appears in the filter stage of the converter, it can be ignored when designing the inner control loop. Due to the fact that the crossover frequency of the outer loop is often designed to be an order of magnitude less than the inner loop, the RHP zero should also not affect the design of the outer loop controller.

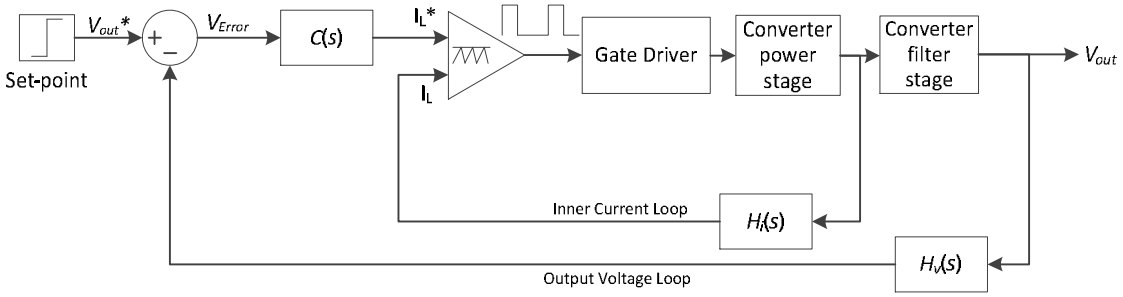


Figure 4.4. Block diagram of peak-current-mode control.

Two control loops are utilised in PCMC. The outer loop is typically called the voltage loop. This loop measures the output voltage and compares it to a reference voltage set by the user. The error from this comparison is entered into the designed controller, which outputs a reference peak value of phase current. This reference value is then compared to the measured inductor current, as shown in Figure 4.5. If the inductor current is less than the reference value, the output of the comparator is high, and the switch is closed, allowing current to build in the inductor. One the inductor current reaches the reference current, the output of the comparator switches to low, and the switch opens. An internal clock and flip-flop are used to ensure the switch does not turn on again until the beginning of the next cycle, as shown in Figure 4.6.

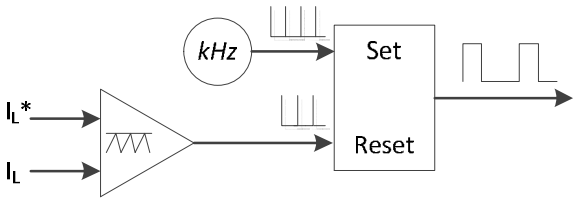


Figure 4.5. Comparator diagram of peak-current mode control

One of the main disadvantages to PCMC is the need for slope compensation when operating at duty cycles greater than 0.5 [4.11], [4.12]. Other disadvantages include low noise immunity, and the difficult of digital implementation due to the need for an external comparator. Finally, an outer control loop needs to be designed in order to calculate the reference current level, which is an approximation of the peak inductor current. [4.13].

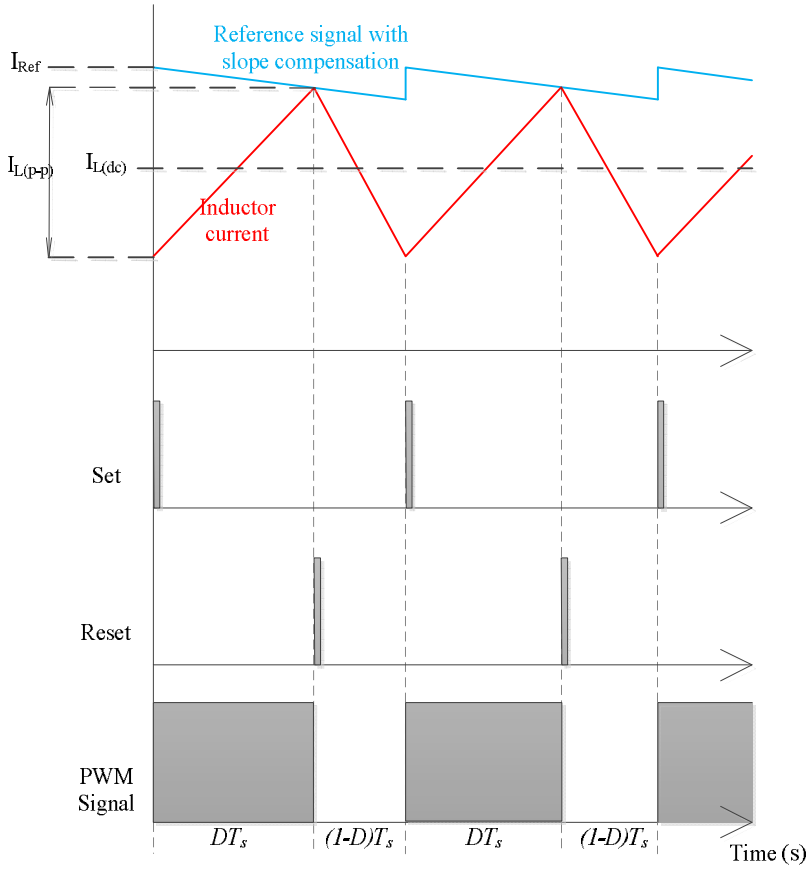


Figure 4.6. PWM signal generator for peak-current mode control.

4.2.4 Average-Current Mode Control

Average-Current-Mode Control (ACMC) is similar to PCMC in that it utilises a cascade control structure i.e. an inner current loop and an outer voltage loop. As with PCMC, the output voltage is measured and compared to a user-defined voltage reference. The error from this comparison is entered into the controller which outputs a reference value for the dc inductor current instead of a reference peak value. This dc current is then compared to the actual dc inductor current, with the error entered into a second controller. The output of this controller is the duty cycle of the converter, which drives a PWM generator [4.13]. The block diagram of ACMC is presented in Figure 4.7.

ACMC combines the advantages of VMC, which include good noise immunity and efficiency, with the advantages of PCMC, which are good stability and performance characteristics [4.14]. It is also much easier to implement digitally than PCMC, and the frequency of the system can be varied more easily. As with PCMC, the RHP zero of the boost converter can be usually be disregarded. The disadvantages of ACMC include a more complex inner loop design, and no inherent short-circuit protection.

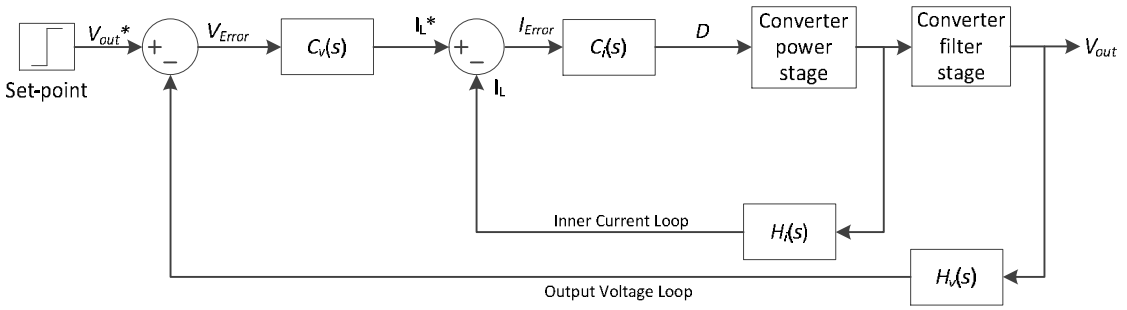


Figure 4.7. Block diagram of average-current mode control.

For converters with high ripple currents, it may also be necessary to filter the measured inductor current.

4.2.5 Coupled-Inductor Converter Controller

The objective of this chapter is to develop a digital-control structure for the CL dc-dc converter which keeps a stable and regulated output voltage over a wide load range. To ensure that current is balanced evenly in both phases of the converter, VMC and hysteretic control are disregarded as choices for possible control structures. This leaves PCMC and ACMC.

One of the key differences between a typical 1L and 2L converter, and a CL converter is operation in the discontinuous-conduction mode (DCM). Not only are the characteristics different, but when in DCM, the average inductor current is no longer half the peak-to-peak current. Another issue when operating in DCM is the inherent resonance due to the effective output capacitance of the MOSFET, which will be coupled between both phases along with the phase current. Since PCMC relies on an accurate estimation of the peak inductor current, and ACMC has better noise immunity when compared to PCMC [4.22], ACMC is the preferred control structure for the converter, and will be the main focus for the rest of the thesis.

Finally, the FPGA used in this body of work is the Altera Cyclone III development kit [4.19]. The FPGA has a 50 MHz clock signal during calculations, while the ADCs used in the system sample at a frequency of 1 MHz. Hence, the controller is designed in the continuous-time domain, and transformed into the digital domain for implementation.

4.3 Digital Controller Design Parameters

The main benefit of using digital control is the ability to quickly change loop parameters in code, without the need of physically changing any hardware in the system. This section will introduce several parameters that need to be considered when designing and implementing a digital controller for a switch-mode power supply.

4.3.1 Design Parameters

While it is the eventual closed-loop characteristics that will determine the response of the system, these characteristics can be predicted by the open-loop system. The most important characteristics are the crossover frequency, the phase margin and the gain margin.

- Crossover Frequency

The crossover frequency is defined as the frequency of the system when the magnitude crosses the 0 dB axis. Hence, the gain of the controller and plant must equal 1 at the crossover frequency, i.e.

$$C(s)G(s)H(s)\big|_{f=f_c} = 1 \tag{4.4}$$

where $C(s)$ is the controller, $G(s)$ is the plant, and f_c is the crossover frequency of the open-loop system. In switch-mode power supplies, the crossover frequency of the open-loop system should be five to ten times lower than the switching frequency [4.16]. In a cascade controller, such as the one implemented here, there are two crossover frequencies to be determined; the inner current loop and outer voltage loop. The crossover frequency of the inner loop must be high enough so that the outer loop is not affected by it. Hence, the following rule of thumb is critical to designing average-current-mode control for dc-dc converters

$$f_v << f_i << f_s \tag{4.5}$$

where f_s is the switching frequency, f_i is the crossover frequency of the inner current loop, and f_v is the crossover frequency of the outer voltage loop.

- Phase Margin

The phase margin, φ_m, of the system is defined as the difference between the phase of the response and -180^o when the gain of the system is one i.e. at the crossover frequency.

$$\varphi_m = \left[\varphi + 180\right]_{f=f_c} \tag{4.6}$$

where φ_i is the phase of the open-loop system. To ensure sufficient conditions of relative stability [4.17], the phase margin of the open-loop system is often chosen to be 60^o, but cannot be any lower than 45^o.

- Gain Margin

The gain margin of the system is the difference between the gain of the system and the 0 dB axis when the phase of the system crosses the -180^o value. A general rule of thumb when designing closed-loop systems for power converters is to ensure that the gain margin of the open-loop system is chosen to be at least -10 to -20 dB [4.17].

4.3.2 Implementation Parameters

- Analogue-to-Digital Converter, Current and Voltage Sensors

The analogue-to-digital converters used are 12-bit ADCs with a sampling rate of 1 µs. There are four ADCs implemented, which are used in measuring the input and output voltages, as well as the two phase currents. The current sensors used are the EL25 P1 from ABB [4.20] while the voltage sensor used is the LV25-P voltage transducer from LEM [4.21]. Coupled with the ADC, the gain of the current sense system as seen by the FPGA is calculated at H_c = 161, while the gain of the voltage sensor is H_v = 7.

- PWM Generator

The PWM generator used is a falling-edge triangular carrier wave. This wave is compared to the output of the inner current-loop controller, i.e. the duty cycle, as shown in Figure 4.8. When the carrier wave is less than the duty cycle, the PWM generator outputs a high value. When the carrier wave is greater than the duty cycle, the PWM output is low. The peak of the carrier wave and the duty cycle must be scaled by a factor of 2^n-1 to allow it to be implemented digitally. The PWM generator for this body of work is capable of 11-bit operation, allowing for 11-bit accuracy. Hence, the carrier wave and duty cycle will be scaled by 2^{11}-1.

- Soft Start

A common problem in dc-dc converters, especially boost converters, is the sudden in rush of current when the converter is switched on. This is due to the output capacitor quickly drawing current from the source, so as to charge enough to supply the load. To circumvent the inrush current, the initial output voltage set-point is set to the value of the input voltage, and increased to the desired output voltage value using the function

$$V_{out}* = V_{in} + (V_{out} - V_{in})(1 - e^{-10t}) \tag{4.7}$$

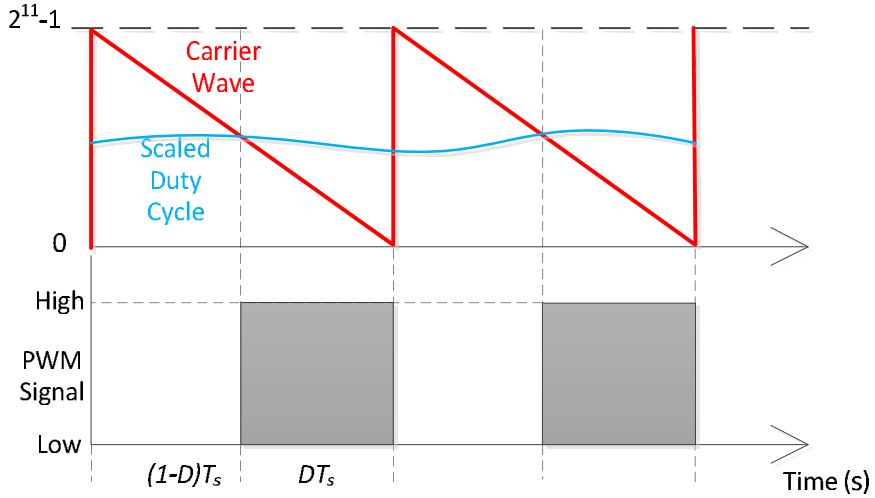


Figure 4.8. Falling edge PWM wave generator.

4.4 CL Converter PI Controller Design and Implementation

Proportional-Integral-Derivative, or PID, controllers are one of the most common controller forms. A PID controller typically takes the form of

$$C(s) = \frac{C_o(s)}{S_{Error}(s)} = K_p + \frac{K_i}{s} + K_d s \tag{4.8}$$

This is presented in block diagram form in Figure 4.9.

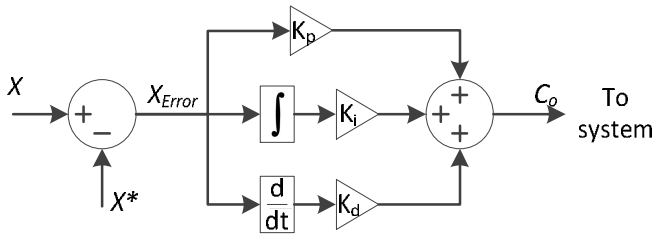


Figure 4.9. Block diagram of PID controller.

In many real-world applications, the derivative action of a PID controller is not included due to the fact that it is difficult to design with, and may even lead to system instability [4.15]. Hence, for the design of the CL converter controllers, the derivative term will be omitted, and the controller will become PI controllers. To control the inner current loop, the PI controller will take the form

$$C_i(s) = \frac{\tilde{I}_{Error}(s)}{\tilde{d}(s)} = K_{pi} + \frac{K_{ii}}{s} = \frac{sK_{pi} + K_{ii}}{s} \tag{4.9}$$

where $C_i(s)$ is the current controller, $I_{Error}(s)$ is the error from the comparator comparing the inductor current to the reference inductor current, $d(s)$ is the duty cycle of the converter, K_{pi} is the proportional gain and K_{ii} is the integral gain. With the desired phase margin and crossover frequency determined, the conditions for designing the PI controller are

$$\left| \frac{sK_{pi} + K_{ii}}{s} \frac{(sC_{out}\gamma_1 - \beta_2\gamma_1 + \beta_1\gamma_2)}{(s^2 LC_{out} - s(L\beta_2 + C_{out}\delta_1) + (\delta_1\beta_2 - \delta_2\beta_1))} \right|_{s=2\pi f_i} = 1 \tag{4.10}$$

and

$$\angle \left[\frac{sK_{pi} + K_{ii}}{s} \frac{(sC_{out}\gamma_1 - \beta_2\gamma_1 + \beta_1\gamma_2)}{(s^2 LC_{out} - s(L\beta_2 + C_{out}\delta_1) + (\delta_1\beta_2 - \delta_2\beta_1))} \right]_{s=2\pi f_i} + 180^o = \varphi_m \tag{4.11}$$

To control the outer voltage loop, the PI controller will take the form

$$C_v(s) = \frac{\tilde{V}_{Error}(s)}{\tilde{I}_{Ref}(s)} = K_{pv} + \frac{K_{iv}}{s} = \frac{sK_{pv} + K_{iv}}{s} \tag{4.12}$$

where $C_v(s)$ is the voltage controller, $V_{Error}(s)$ is the error from the comparator comparing the output voltage to the reference output voltage, $I_{Ref}(s)$ is the reference

inductor current, K_{pv} is the proportional gain and K_{iv} is the integral gain. With the desired phase margin and crossover frequency determined, the conditions for designing the PI controller are

$$\left| \frac{sK_{pv} + K_{iv}}{s} \frac{(s\gamma_2 L_{Lk} + \delta_2\gamma_1 - \delta_1\gamma_2)}{(s\gamma_1 C_{out} + \beta_1\gamma_2 - \beta_2\gamma_1)} \right|_{s=2\pi f_v} = 1 \tag{4.13}$$

and

$$\angle \left[\frac{sK_{pv} + K_{iv}}{s} \frac{(s\gamma_2 L_{Lk} + \delta_2\gamma_1 - \delta_1\gamma_2)}{(s\gamma_1 C_{out} + \beta_1\gamma_2 - \beta_2\gamma_1)} \right]_{s=2\pi f_v} + 180^{\circ} = \varphi_m \tag{4.14}$$

4.4.1 Design of Inner Current Loop PI Controller for CCM Operation

The controllers designed in the following section are to digitally control the 1 kW CL boost converter prototype introduced in Chapter 1. The converter parameters are as follows for CCM operation: input voltage V_{in} = 225 V, output voltage V_{out} = 450 V, converter power P_{out} = 1.35 kW, output current I_{out} = 3 A, output load resistance R_{out} = 150 Ω, leakage inductance L_{Lk} = 350 μH, magnetising inductance L_m = 1050 μH, output capacitance C_{out} = 900 μF, and duty cycle D = 0.5. The switching frequency f_s of the converter is 16 kHz.

The Bode plot of the duty cycle-to-inductor current transfer function $G_{id}(s)$ of the CL boost converter operating in CCM is presented in Figure 4.10.

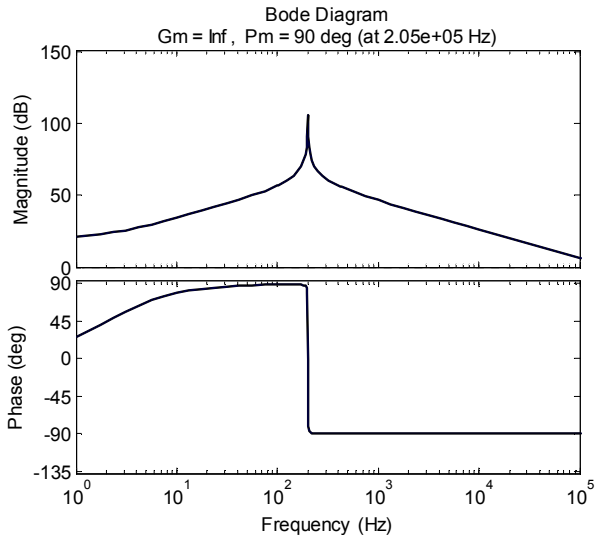


Figure 4.10. Theoretical Bode plot of $G_{id}(s)$, the duty cycle-to-inductor current transfer function.

The crossover frequency of the open-loop current loop is designed to be twenty times less than the switching frequency of the converter in order to attenuate the inductor current ripple as much as possible. Hence

$$f_i = \frac{f_s}{20} = 800 \text{ Hz} \tag{4.15}$$

The desired phase margin of the system at this frequency is designed to be 60°. The current phase at this frequency is 90°. Hence, a phase lag of 30° needs to be introduced by the PI controller. Since the phase of the system will never reach the -180° axis, the gain margin will be infinite, and so does not need to be considered. By inputting the desired crossover frequency and phase margin into equations (4.10) and (4.11), the two equations are solved simultaneously to find that

$$K_{pi} = 0.0032 \tag{4.16}$$

and

$$K_{ii} = 9.18 \tag{4.17}$$

With the current controller designed, the frequency response of the open-loop system is presented in Figure 4.11.

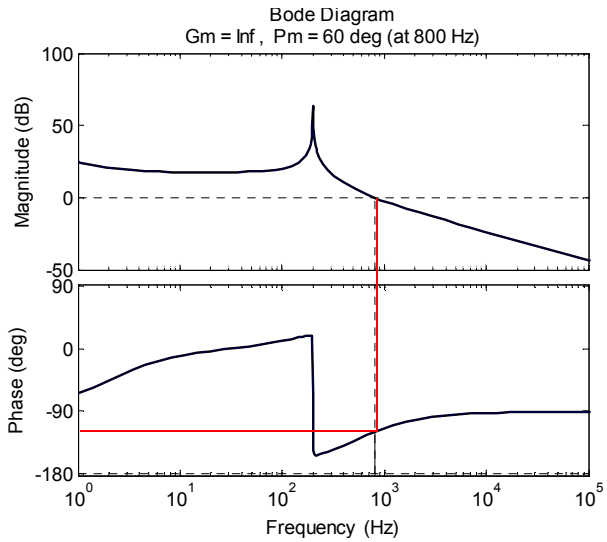


Figure 4.11. Theoretical Bode plot of the open-loop current loop of the CL boost converter in CCM.

As can be seen from the frequency response, the open-loop phase margin is now 60°, at a crossover frequency of 800 Hz, and an infinite gain margin. This satisfies the criteria for the current controller. The closed-loop frequency response of the inner loop is presented in Figure 4.12.

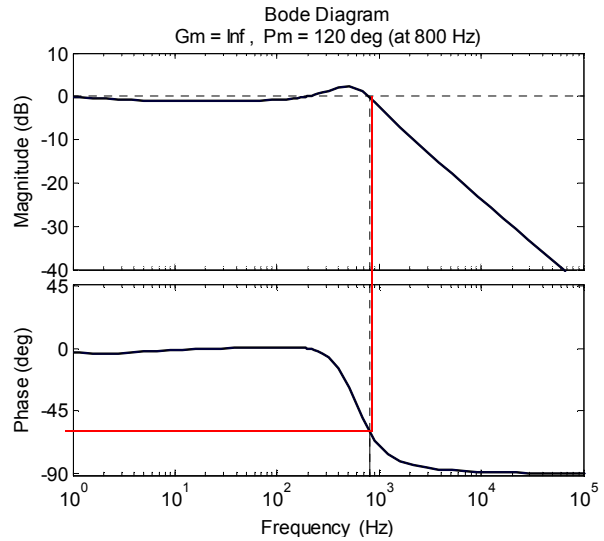


Figure 4.12. Theoretical Bode plot of the closed-loop current loop of the CL boost converter in CCM.

4.4.2 Design of Outer Voltage Loop PI Controller for CCM Operation

The Bode plot of the inductor current-to-output voltage transfer function $G_{vi}(s)$ of the CL boost converter operating in CCM is presented in Figure 4.13.

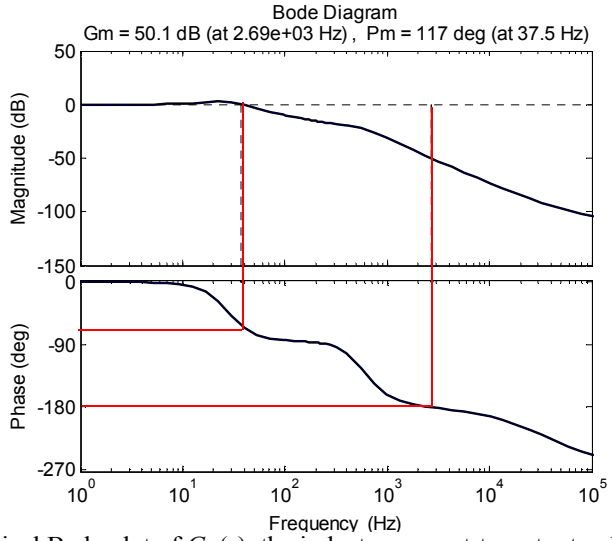


Figure 4.13. Theoretical Bode plot of $G_{vi}(s)$, the inductor current-to-output voltage transfer function.

The crossover frequency of the open-loop voltage loop is often designed to be ten to twenty times less than the crossover frequency of the open-loop current loop converter. Due to the soft start the controller implements, the outer voltage loop needs to be slow enough so as to take into account the soft start action. Hence the open-loop crossover frequency is designed to be twenty times less than the crossover frequency of the current loop in order to ensure the inner loop is fast enough to leave the outer loop unaffected. Therefore

$$f_v = \frac{f_i}{20} = 40 \text{ Hz} \tag{4.18}$$

The desired phase margin of the system at this frequency is also be designed to be 60^o. The current phase at this frequency is -80^o. Hence, a phase lag of 40^o needs to be introduced by the PI controller. By inputting the desired crossover frequency and phase margin into equations (4.13) and (4.14), the two equations are solved simultaneously to find that

$$K_{pv} = 0.1894 \tag{4.19}$$

and

$$K_{iv} = 31.27 \tag{4.20}$$

The frequency response of the open-loop system is presented in Figure 4.14. As can be seen from the frequency response, the open-loop phase margin is now 60^o, at a crossover frequency of 40 Hz, and a gain margin of 61.2 dB. This satisfies the criteria for the voltage controller. The closed-loop frequency response of the outer loop is presented in Figure 4.15.

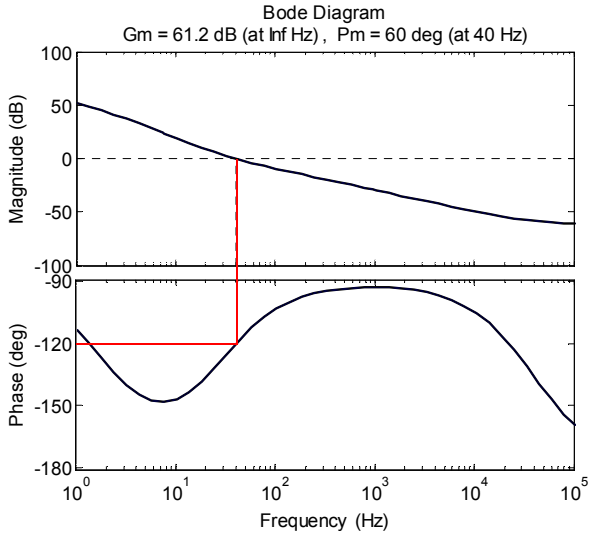


Figure 4.14. Theoretical Bode plot of the open-loop current loop of the CL boost converter in CCM.

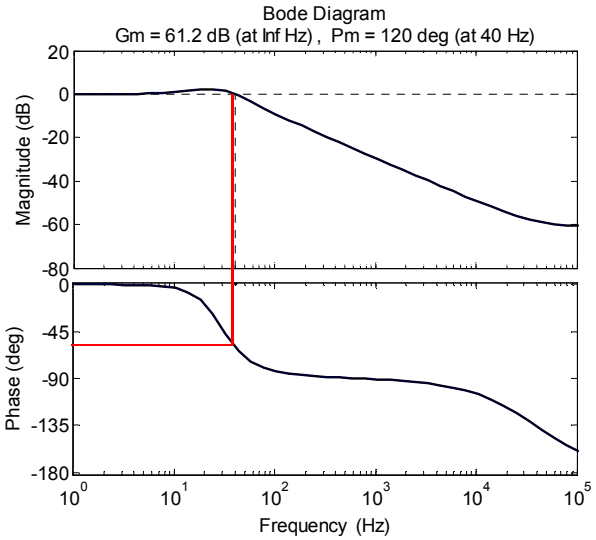


Figure 4.15. Theoretical Bode plot of the closed-loop current loop of the CL boost converter in CCM.

4.4.3 Simulation and Experimental Results of PI Controllers in ACMC of the CL Boost Converter operating in CCM

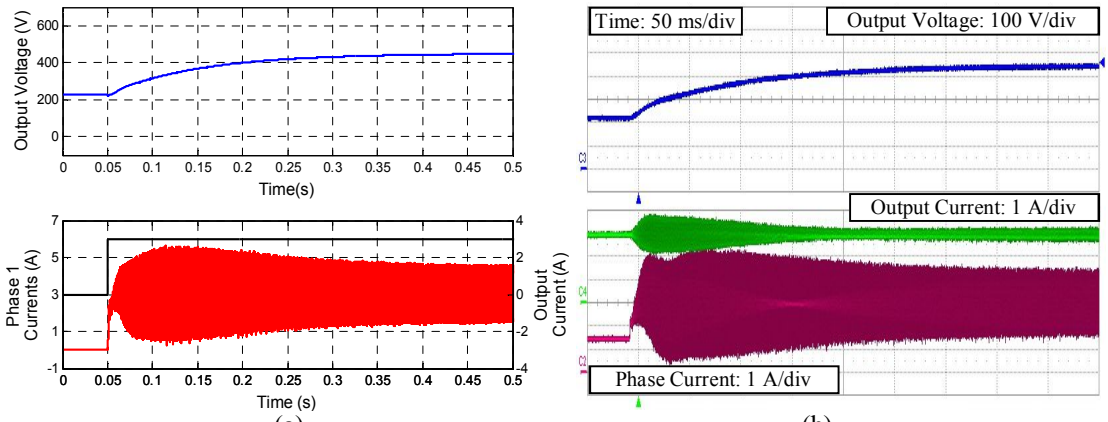
The SimPowerSystems package in the Matlab®/Simulink software is utilized to first test the designed controllers before implementation. A two-phase interleaved coupled-inductor boost converter is developed in Simulink, and controlled via ACMC utilising PI controllers developed in Section 4.4.2. The circuit elements are presumed ideal, as are the semiconductor switch and diode.

For the practical experiments, the control scheme designed is digitised using the bilinear transform, and implemented into the 1 kW prototype converter. To compare to the results, three tests of the converter are performed; start-up, steady-state and load step response. Differing values of load-drops are utilised in each load step response, and depend on the mode of operation. This is to ensure the converter sees a large enough disturbance, while staying in the desired mode.

In order to do the comparison, the *x*-axis and *y*-axis scaling of the experimental results are identical to those of the simulated results. For all experimental results presented in this chapter, the scaling of the oscilloscope for all experimental waveforms are specified with the results.

4.4.3.1 Converter Start-Up in CCM Utilising PI Controllers

Before the converter begins switching, the output is directly connected to the input, and the output capacitor voltage equals the input voltage. The converter is then switched on, and the output voltage and one phase current are recorded. Figure 4.16 presents the output voltage and the phase 1 inductor current responses over the full start-up time of the converter.

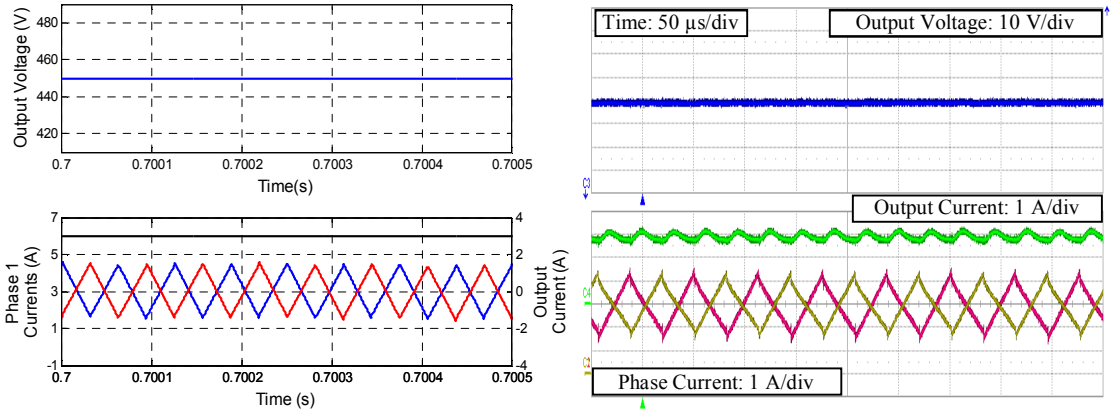


(a) (b)

Figure 4.16. Simulated (a) and experimental (b) response of the closed-loop CL boost converter operating in CCM during start-up.

4.4.3.2 Steady-State in CCM Utilising PI Controllers

Once start-up is complete, the converter is allowed to run for approximately 5 minutes to ensure stable operation. Figure 4.17 presents the output voltage and both inductor current responses over the 500 µs.

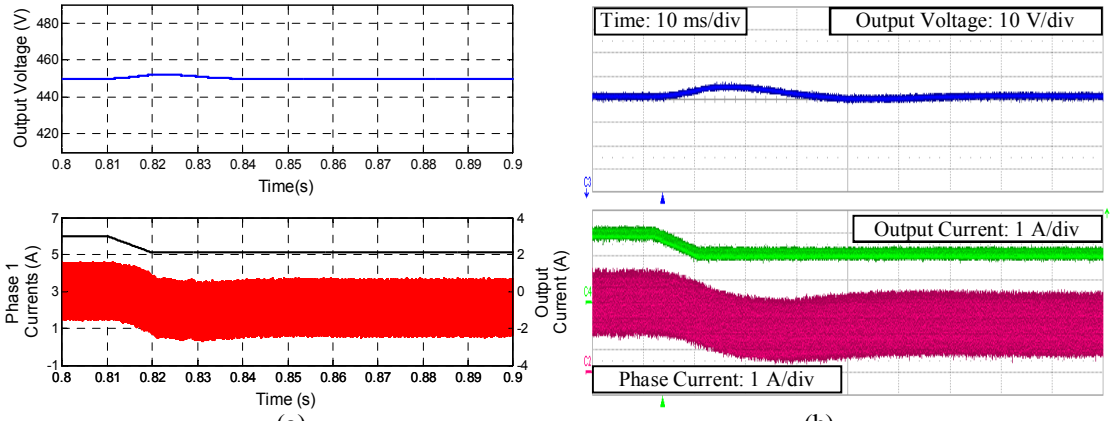


(a) (b)

Figure 4.17. Simulated (a) and experimental (b) response of the closed-loop CL boost converter operating in CCM during steady-state operation.

4.4.3.3 Load Step Test in CCM Utilising PI Controllers

During operation, the value of the output current of the converter is determined by a dc electronic load. During the load-step test, a command is sent to the load to drop the value of current to 70 % of its initial current value at a rate of 90 A/s. The transients of the output voltage and one of the phase currents are recorded, and presented in Figure 4.18.

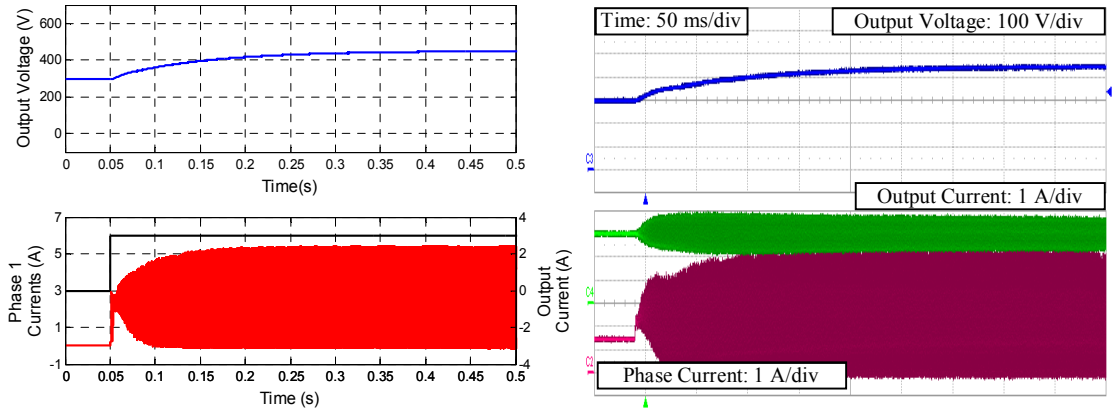


(a) (b)

Figure 4.18. Simulated (a) and experimental (b) response of the closed-loop CL boost converter operating in CCM during load step test.

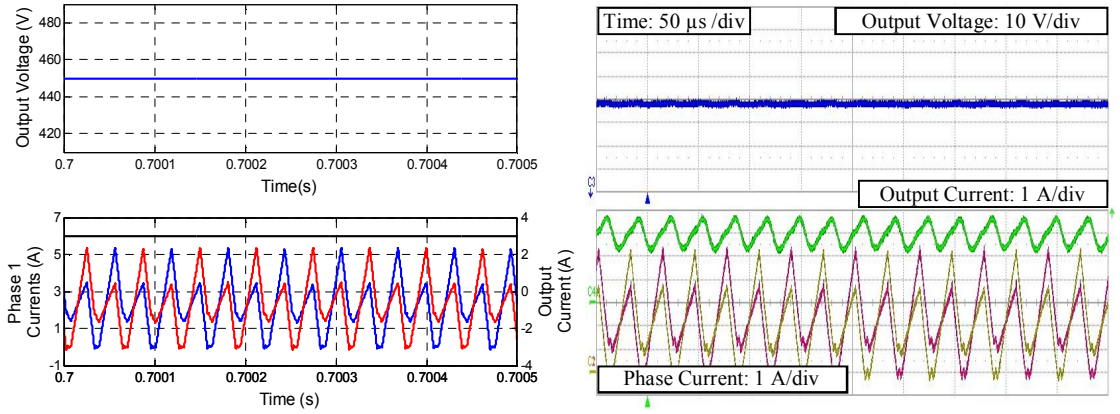
4.4.4 CCM Designed PI Controllers for DCM 1 Operation

To test the stability of the controllers when operating in DCM, the input voltage is increased to 300 V, while the output current remains at 3 A, causing the converter to enter DCM 1. Once again, the three tests of start-up (Figure 4.19), steady-state (Figure 4.20), and load step response (Figure 4.21) are undertaken.



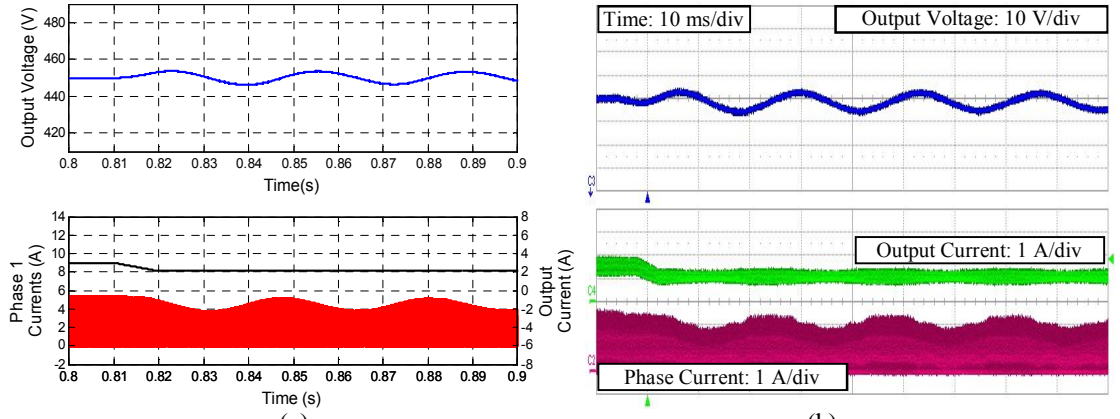
(a) (b)

Figure 4.19. Simulated (a) and experimental (b) response of the closed-loop CL boost converter utilizing CCM controllers operating in DCM 1 during start-up.



(a) (b)

Figure 4.20. Simulated (a) and experimental (b) response of the closed-loop CL boost converter utilizing CCM controllers operating in DCM 1 during steady-state.



(a) (b)

Figure 4.21. Simulated (a) and experimental (b) response of the closed-loop CL boost converter utilizing CCM controllers operating in DCM 1 during a load step response.

4.4.5 Design of Inner Current Loop PI Controller for DCM 1/DCM 9 Operation

Two DCM modes are chosen to test the DCM controllers on the CL boost converter, DCM 1 and DCM 9. The converter parameters are as follows: output voltage is V_{out} = 450 V, leakage inductance is L_{Lk} = 350 µH, magnetising inductance is L_m = 1000 µH, output capacitance is C_{out} = 900 µF, duty cycle is D = 0.5, and frequency is f_s = 16 kHz.

For testing of the controllers designed for DCM 1, the input voltage is Vin = 300 V, the converter power is Pout = 1.35 kW, the output current is Iout = 3 A and the output load resistance is Rout = 150 Ω, while for the DCM 9 controllers, the input voltage is Vin = 150 V, the output current is Iout = 0.5 A, the converter power is Pout = 225 W, and the output load resistance is Rout = 900 Ω. Initially, a test was performed to examine the effects of using the designed CCM controller on DCM 1. Both the simulated and experimental tests were performed. The Bode plots of the duty cycle-to-inductor current transfer function $G_{id}(s)$ of the CL boost converter operating in DCM 1 and DCM 9 are presented in Figure 4.22.

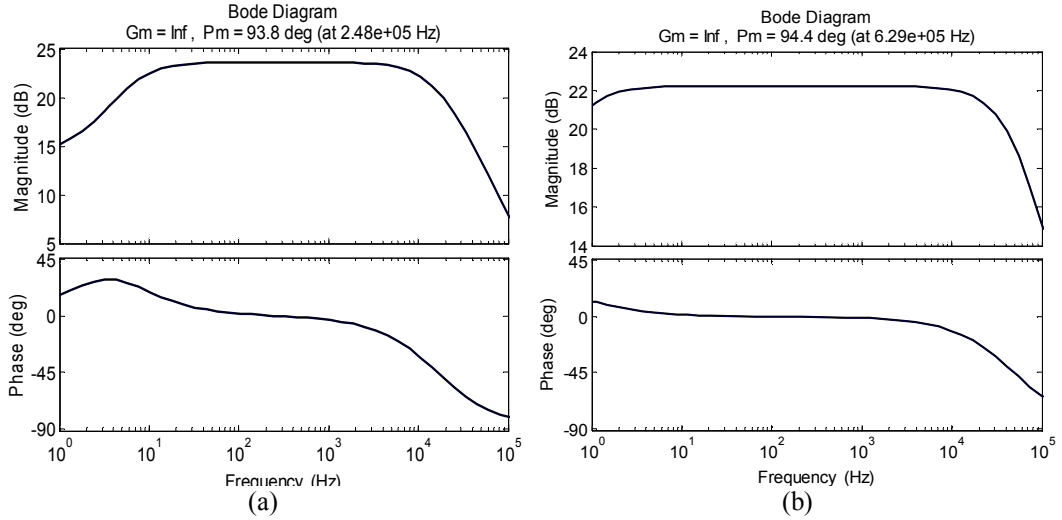


Figure 4.22. Bode plot of $G_{id}(s)$, the duty cycle-to-inductor current transfer function of (a) DCM 1 and (b) DCM 9.

The crossover frequency of the open-loop current loop is once again designed to be twenty times less than the switching frequency of the converter i.e.

$$f_i = \frac{f_s}{20} = 800 \text{ Hz} \tag{4.21}$$

As with CCM operation, the phase margin is typically designed to be 60^o. By analysing both Bode plots it is evident that this objective is not possible due to the fact that a PI controller can only introduce a maximum phase of 90^o. Since both Bode plots show the phase of the system at approximately -2^o to -5^o, it is impossible to attain -120^o phase. Hence, the phase margin of both systems is chosen to be 100^o. By inputting the desired crossover frequency and phase margin into equations (4.10) and (4.11), the two equations are solved simultaneously to find that, for DCM 1

$$K_{pi} = 0.0142 \tag{4.22}$$

and

$$K_{ii} = 323 \tag{4.23}$$

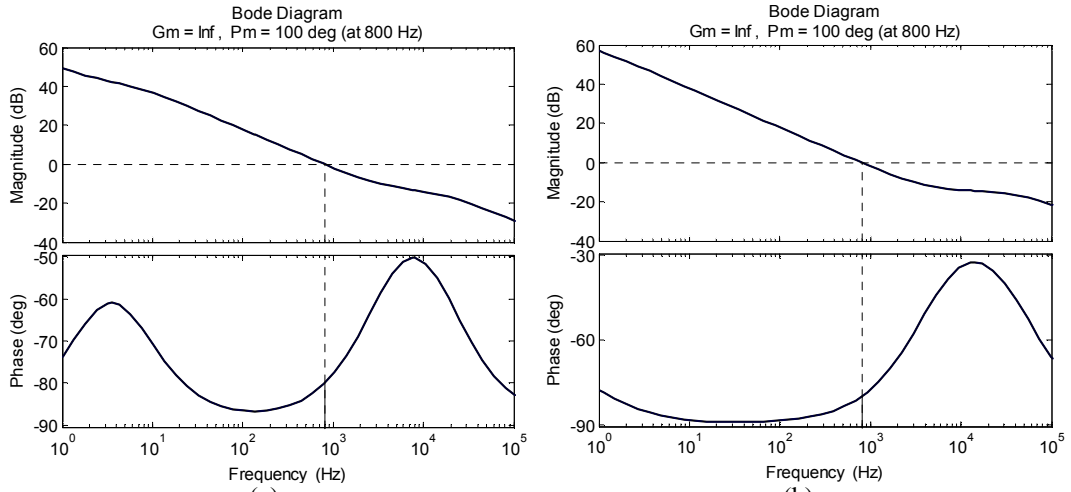
while for DCM 9

$$K_{pi} = 0.0147 \tag{4.24}$$

and

$$K_{ii} = 384 \tag{4.25}$$

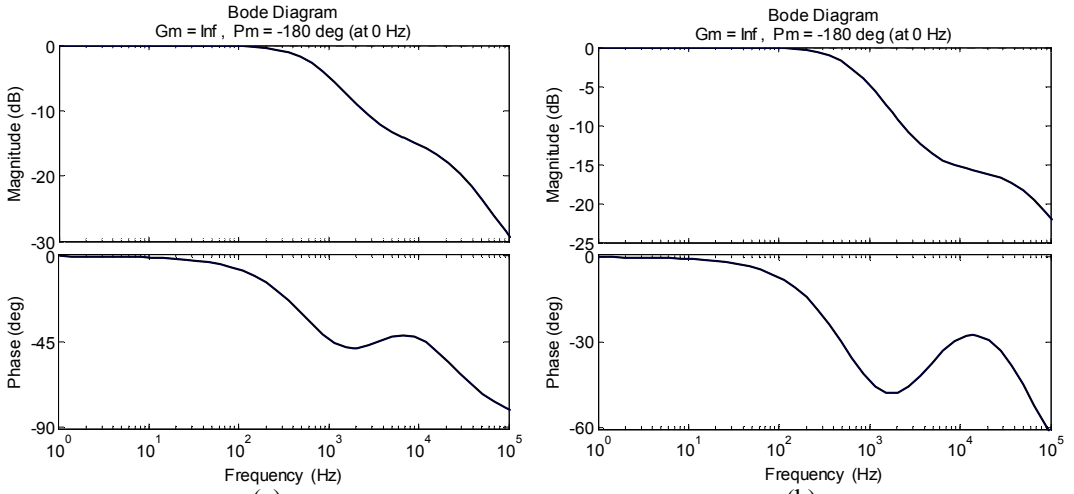
With the current controllers designed, the frequency responses of the open-loop systems are presented in Figure 4.



(a) (b)

Figure 4.23. Bode plot of the open-loop current loop of the CL boost converter in (a) DCM1 and (b) DCM 9.

As can be seen from the frequency responses, the open-loop phase margins are now 100^{o}, at a crossover frequency of 800 Hz, and there is an infinite gain margin. This satisfies the criteria for the current controller. The closed-loop frequency responses of the inner loops are presented in Figure 4.24.



(a) (b)

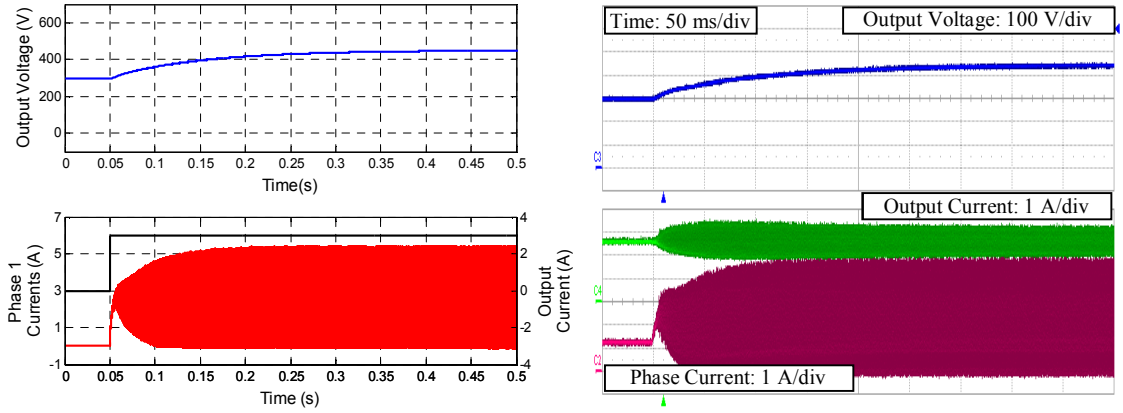
Figure 4.24. Bode plot of the closed-loop current loop of the CL boost converter in (a) DCM 1 and (b) DCM 9.

4.4.6 Simulation and Experimental Results of PI Controllers in ACMC of the CL Boost Converter operating in DCM 1/DCM 9

As with the CCM tests, a Simulink model of the closed-loop CL converter operating in DCM 1 and DCM 9 is compared to experimental tests run on the 1 kW prototype during start-up, steady-state and load step response. Once again, the scaling of the experimental results is identical to the simulated results. Results from all other DCM modes of operation are presented in the appendix.

4.4.6.1 Converter Start-Up in DCM 1 Utilising PI Controllers

As with earlier tests, the output capacitor is initially charged to the value of the input voltage. The converter is then switched on, and the output voltage and phase currents are recorded. Figure 4.25 presents the output voltage and one of the inductor current responses over the full start-up time of the converter.

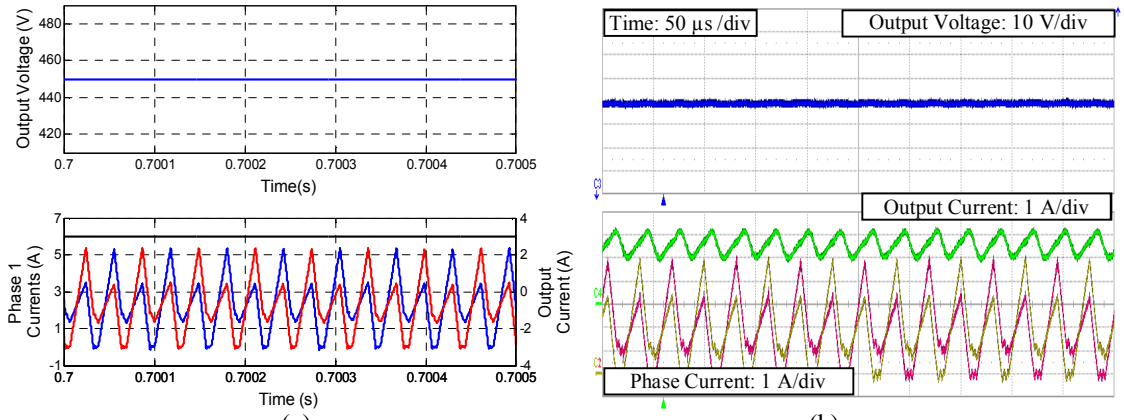


(a) (b)

Figure 4.25. Simulated (a) and experimental (b) response of the closed-loop CL boost converter operating in DCM 1 during start-up.

4.4.6.2 Steady-State in DCM 1 Utilising PI Controllers

Once start-up is complete, the converter is again allowed to run for approximately 5 minutes to ensure stable operation. Figure 4.26 presents the output voltage and inductor current responses over the 500 µs.

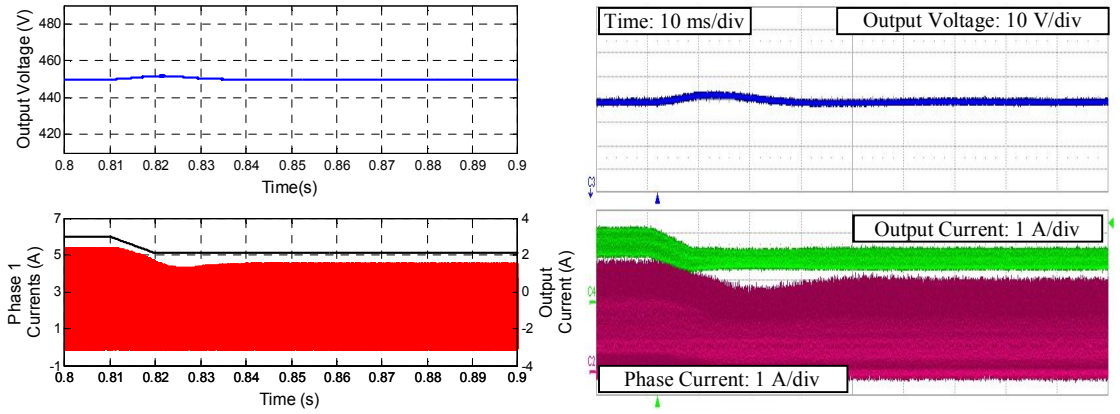


(a) (b)

Figure 4.26. Simulated (a) and experimental (b) response of the closed-loop CL boost converter operating in DCM 1 during steady-state operation.

4.4.6.3 Load Step Test in DCM 1 Utilising PI Controllers

During the load-step test, a command is sent to the load to drop the value of current to 60 % of its initial current value at a rate of 78 A/s. The transients of the output voltage and one of the phase currents are recorded, and presented in Figure 4.27 below.

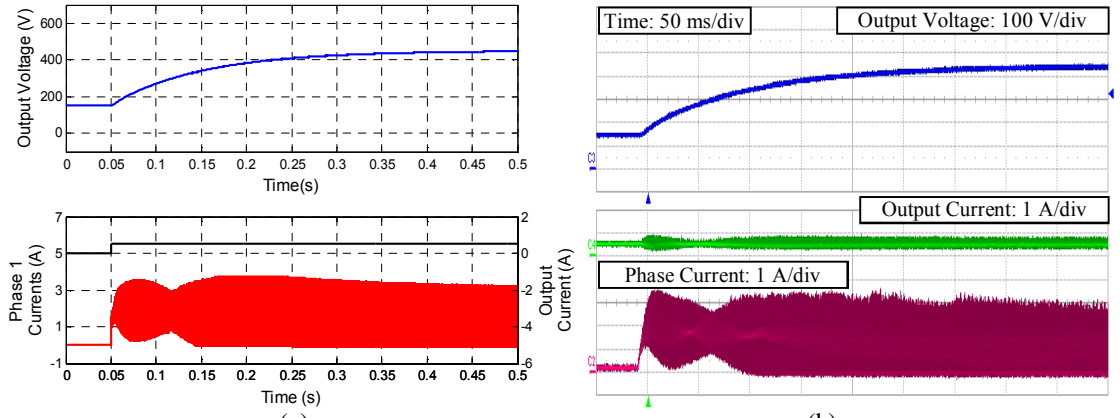


(a) (b)

Figure 4.27. Simulated (a) and experimental (b) response of the closed-loop CL boost converter operating in DCM 1 during load step test.

4.4.6.4 Converter Start-Up in DCM 9 Utilising PI Controllers

Figure 4.28 presents the output voltage and inductor current responses over the full start-up time of the converter.

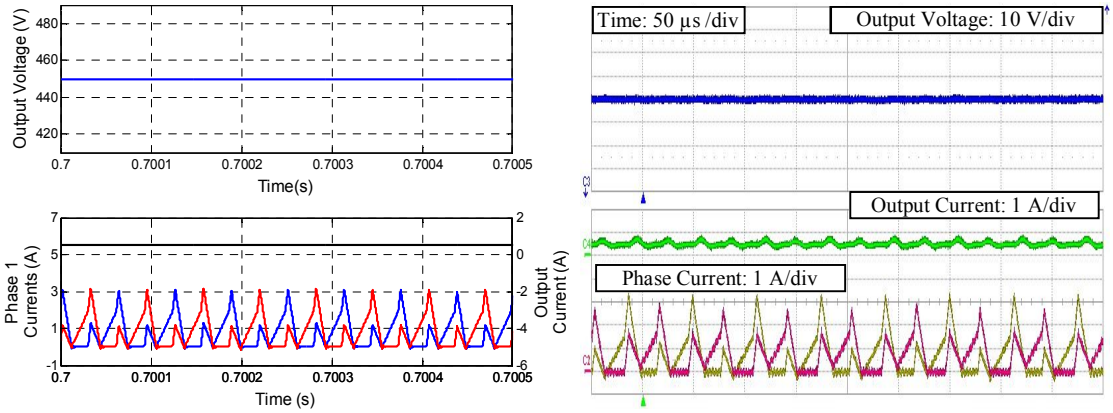


(a) (b)

Figure 4.28. Simulated (a) and experimental (b) response of the closed-loop CL boost converter operating in DCM 9 during start-up.

4.4.6.5 Steady-State in DCM 9 Utilising PI Controllers

Figure 4.29 presents the output voltage and inductor current responses over the 500 µs.

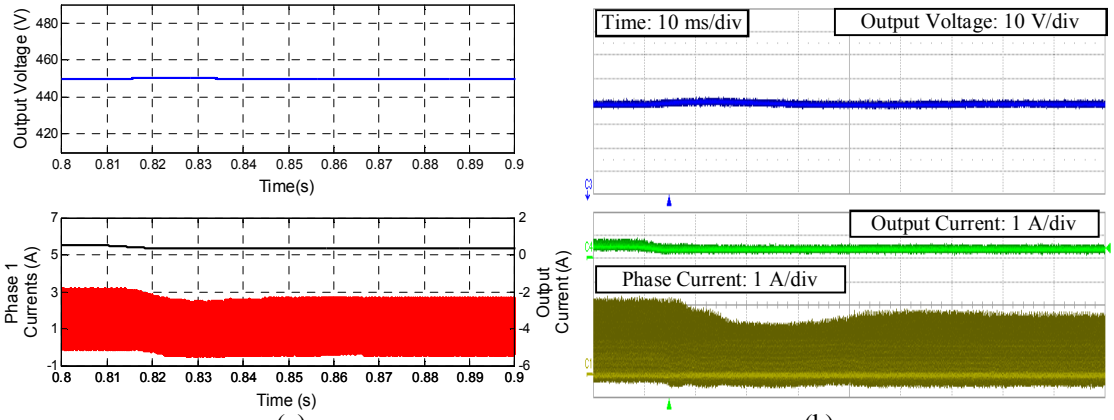


(a) (b)

Figure 4.29. Simulated (a) and experimental (b) response of the closed-loop CL boost converter operating in DCM 9 during steady-state operation.

4.4.6.6 Load Step Test in DCM 9 Utilising PI Controllers

During the load-step test, a command is sent to the load to drop the value of current to 70 % of its current value at a rate of 15 A/s. The transients of the output voltage and one of the phase currents are recorded, and presented in Figure 4.30 below.



(a) (b)

Figure 4.30. Simulated (a) and experimental (b) response of the closed-loop CL boost converter operating in DCM 9 during load step test.

When comparing the simulated and experimental responses of all tests presented, an excellent correlation exists between the two. This further proves, not only the validity of the small-signal models of the CL boost converter, but also the chosen control scheme of ACMC, and the actual controller design. It should be noted that no tuning of the control parameters was done before implementation i.e. the controller parameters implemented into the FPGA are identical to those calculated. This is an important point to make, as often enough, controllers designed from calculated transfer functions often need retuning due to the inaccuracies of the models available.

As can be seen from some steady-state waveforms, a slight imbalance in the system is present between the phases when operating in DCM. This imbalance was also seen in the open loop tests of Chapter 2. However, due to the fact that the results shown in Chapter 3 are closed-loop results, it should be noted that the duty cycles between the

phases are no longer identical. To circumvent any imbalances in the system, a current-balancing scheme may be introduced.

4.5 Conclusions

This chapter presented the design and implementation of digital average-current-mode control utilizing PI controllers. The various control structures most often used in dc-dc converters were briefly discussed and compared. The design parameters of the CL boost converter were developed, and a brief discussion on PI controllers was presented. With the circuit and design parameters, suitable PI controllers for the inner current loop and outer voltage loop were designed. These controllers were first implemented into Matlab®/Simulink to simulate the responses. These responses were compared to actual experimental results taken from the closed-loop control of the 1 kW prototype CL converter for CCM, DCM 1 and DCM 9 operation. An excellent correlation is found to exist between the simulated results and the experimental results. Finally, the closed-loop responses of the three converter tests; start-up, steady-state and load step response show excellent stability, transient response and load-disturbance rejection. Results from all other DCM modes of operation are presented in the appendix.

4.6 References

[4.1] N. Mohan, T. M. Undeland and W. P. Robbins (2003). *Power Electronics; Converters, Applications and Design, 2nd Edition*, John Wiley & Sons, Inc., pp 161-199.

[4.2] R. W. Erickson (1997), *Fundamentals of Power Electronics*, Kluwer Academic Publishers, pp. 323-368.

[4.3] N. Mohan (2003), *First Course on Power Electronics and Drives*, MNPERE, pp. 4.1-4.21, 6.1-6.11..

[4.4] G. Garcera, J. M. Benavent, M. Pascual and J. A. Martinez, "Adaptive two-loop voltage mode control of dc-dc switching converters," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 1, pp. 239-253, February 2006.

[4.5] M. Veerachery, "Two-loop voltage-mode control of coupled-inductor step-down buck converter," *IEEE Proceedings – Electrical Power Applications*, vol. 152, no. 6, pp. 1516-1524, November 2005.

[4.6] A. R. Olivia, S. S. Ang and G. E. Bortolotto, "Digital control of a voltage-mode synchronous buck converter," *IEEE Transactions on Power Electronics*, vol. 21, no. 1, pp. 157-163, January 2006.

[4.7] F. Xia, R. Yang and B. Zhang, "Bifurcation and border collision analysis of voltage-mode controlled flyback converter based on total ampere-turns," *IEEE Transactions on Circuits and Systems I*, vol. 58, no. 9, pp. 2269-2280, March 2011.

[4.8] S. Marques, C. Cruz, F. Antunes and J. Farias, "Step-down converter with hysteretic current control for welding applications" *International Conference on Industrial Electronics, Control and Instrumentation*, pp. 676-681, November 1997.

[4.9] K. Y. Hu, S. M. Lin and C. H. Tsai, "A fixed-frequency quasi-V2 hysteretic buck converter with PLL-based two-stage adaptive window control," *IEEE Transactions on Circuits and systems I*, vol. 62, no. 10, pp. 2565-2573, October 2015.

[4.10] F. Su, W. H. Ki and C. Y. Tsui, "Ultra-fast fixed-frequency hysteretic buck converter with maximum charging current control and adaptive delay compensation for DVS applications," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 4, pp. 815-822, April 2008.

[4.11] T. Suntio, M. Rahkala, I. Gadoura and K. Zenger, "Dynamic effects of inductor current ripple in peak-current and average-current current mode control," *IEEE Conference of the Industrial Electronics Society*, vol. 2, pp. 1072-1077, November 2001.

[4.12] R. B. Radley, "A new, continuous-time model for current-mode control," *IEEE Transactions on Power Electronics*, vol. 6, no. 2, pp. 271-280, August 2002.

[4.13] B. G. Cho, H. S. Bae and J. H. Lee, "Review of current mode control schemes and introduction of a new digital current mode control method for the parallel module dc-dc converters," *IEEE International Power Electronics and Motion control Conference*, pp. 202-210, May 2009.

[4.14] "DC-DC Controllers Use Average-Current Mode Control for Infotainment Applications," *Maxim Integrated Application Note*, https://www.maximintegrated.com/en/app-notes/index.mvp/id/3939 (Accessed on 30/11/2016).

[4.15] K. H. Ang, G. Chong and Y. Li, "PID control system analysis, design and technology," *IEEE Transactions on Control Systems and Technology*, vol. 13, no. 4, pp. 559-576, July 2005.

[4.16] G. Gercera, E. Figueres and A. Mocholi, "Novel three-controller average current mode control of dc-dc PWM converters with improved robustness and dynamic response," IEEE *Transactions on Power Electronics*, vol. 15, no. 3, pp. 516-528, August 2002.

[4.17] M. K. Kazimierczuk, R. S. Geise, A Reatti, "Small-signal analysis of a PWM boost dc-dc converter with a non-symmetric phase integral-lead controller," *International Telecommunications Energy Conference*, pp 608-615, October 1995.

[4.18] LM3475 Hysteretic PFET Buck Controller datasheet, http://www.ti.com/lit/ds/symlink/lm3475.pdf (Accessed on 30/11/2016).

[4.19] https://www.altera.com/products/fpga/cyclone-series/cyclone-iii/overview.html (Accessed on 25/11/2016).

[4.20] www.datasheet-pdf.com/PDF/EL50P1-Datasheet-ABB-805347 (Accessed on 25/11/2016).

[4.21] http://www.alldatasheet.com/datasheet-pdf/pdf/87952/LEM/LV25-P.html (Accessed on 25/11/2016).

[4.22] V. R. Chandranadhan, and G. Renjini, "Comparison between peak and average current mode control of improved bridgeless flyback rectifier with bidirectional switch," *2015 International Conference on Technological Advancements in Power and Energy*, pp. 254-259, June 2015.

5 COUPLED-INDUCTOR INTERLEAVED CONVERTER CLOSED-LOOP TYPE II DIGITAL CONTROL

Phase Lead/Lag Compensators give control designers much more freedom when implementing closed-loop control. Along with this, the addition of a pole at 0 Hz of the controller allows for the elimination of steady-state error. As such, phase compensators with a pole at the origin, also known as Type II compensators, are often the controller of choice when closing the loop of a dc-dc converter. This chapter presents the design and implementation of such controllers for the continuous-conduction, and discontinuous-conduction modes of the two-phase interleaved coupled-inductor boost converter.

5.1 Introduction

The maximum amount of phase which can be injected into a system by a Proportional-Integral (PI) controller is 90^o. As seen in Chapter 4, most DCM modes of operation have a low phase at the desired crossover frequencies, making it difficult to design for an open-loop phase margin of anything under 100^o. By implementing a Phase Lead/Lag Compensator (PLC) with a pole at 0 Hz, often termed in power electronics as a Type II controller [5.1], a phase margin of 60^o is much more easily attained.

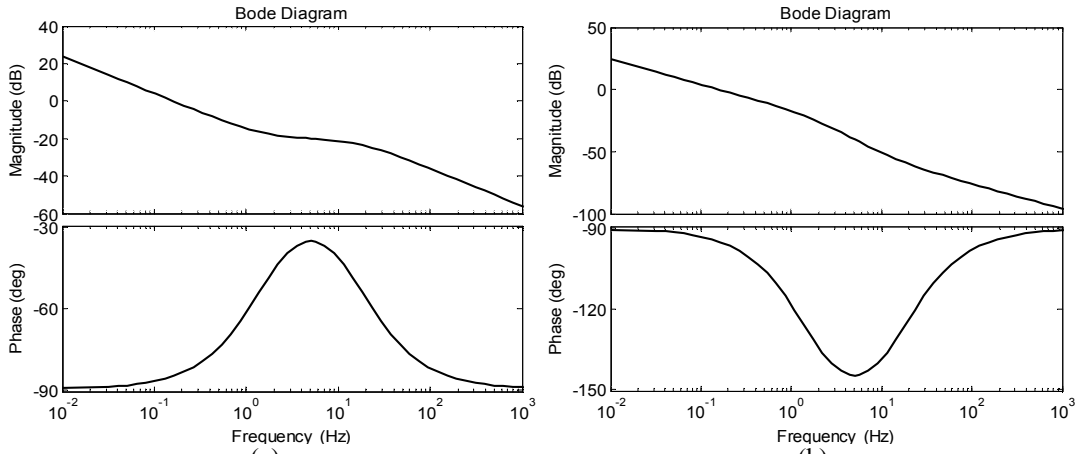
The objective of this chapter is to replace the PI controllers designed for the inner current loop in Chapter 4 with Type II controllers. Section 5.2 discusses the structure of a Type II compensator, and its digital implementation. Section 5.3 presents the design and implementation of Type II compensators for CCM operation in the CL boost converter. Section 5.4 presents the design of the Type II controllers for DCM operation, and the problems encountered during implementation. Finally, Section 5.5 introduces the idea of bumpless control, the ability to seamlessly transition from one controller to another, allowing for the implementation of the DCM designed Type II compensator.

5.2 Type II Compensator Structure and Implementation

The structure of a Type II compensator is presented in equation (5.1).

$$C(s) = \frac{K_c}{s} \frac{1 + s/\omega_z}{1 + s/\omega_p} \tag{5.1}$$

where $C(s)$ is the controller, K_c is the gain of the controller, ω_z is the frequency of the controller zero, and ω_p is the frequency of the second controller pole, the first being at 0 Hz. By choosing the frequencies of the pole and the zero, the controller either adds, or subtracts the amount of phase needed to attain the desired phase margin. The gain is calculated to give the desired crossover frequency. The Bode plots of a typical Type II compensator are presented in Figure 5.1 (a), for when $\omega_z < \omega_p$, and (b) for when $\omega_z > \omega_p$.



(a) (b)

Figure 5.1. Bode plots of Type II compensator when (a) $\omega_z < \omega_p$, and (b) $\omega_z > \omega_p$.

A Type II compensator is often designed in the continuous domain, and can then be implemented in an analogue controller by utilising operational-amplifiers (op-amps), or digitally with the use of microcontrollers or FPGAs.

5.2.1 Analogue Implementation of the Type II Compensator

The schematic of a Type II op-amp compensator [5.2], [5.3] is presented in Figure 5.2.

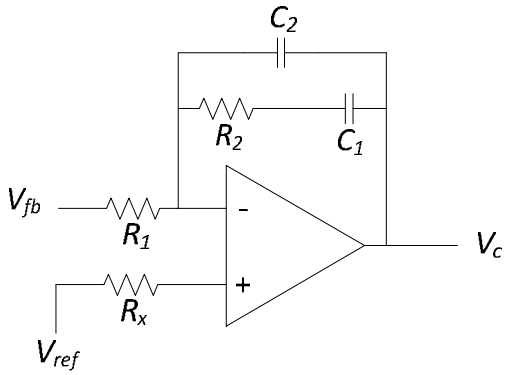


Figure 5.2. Op-amp design of Type II compensator.

In the circuit diagram given in Figure 5.2, V_{fb} is the measured output of the system being controlled, which is compared to V_{ref}, the desired set point. The resistors R_1 and R_2, and capacitors C_1 and C_2 are calculated to give the desired Type II response. The output of the op-amp, V_c, is the controlled input into the system. The resistor R_1 is typically chosen to limit the current of the circuit, while the following equations determine the values of the capacitors and the remaining resistor.

$$C_2 = \frac{\omega_z}{\omega_p R_1 K_c}$$
$$C_1 = C_2\left(\frac{\omega_p}{\omega_z} - 1\right) \tag{5.2}$$
$$R_2 = \frac{1}{\omega_z C_1}$$

The resistor R_x is chosen to ensure common-mode balance so that any voltage drop across R_1 due to current leakage is offset by dropping a similar voltage across R_x.

5.2.2 Digital Implementation of the Type II Compensator

To implement the Type II compensator digitally, the Backwards Rectangular transform [5.6] is used to convert equation 5.1 into the digital domain i.e.

$$\frac{1}{s} = \frac{z}{z-1}T_{Ds} \tag{5.3}$$

where T_{Ds} is the discrete sampling time of the system. Hence, the difference equation form of a Type II compensator is

$$out(n) = G_2 in(n) - G_4 in(n-1) + G_1 out(n-1) - G_3 out(n-2) \tag{5.4}$$

where *out* is the output of the controller, *in* is the input of the controller, n is the n^{th} sample, and the gains G_1, G_2, G_3, and G_4 are given by

$$G_1 = \frac{2 + \omega_p T_{Ds}}{1 + \omega_p T_{Ds}} \tag{5.5}$$

$$G_2 = \frac{K_c \omega_p T_{Ds} \left(1 + \omega_z T_{Ds}\right)}{\omega_z \left(1 + \omega_p T_{Ds}\right)} \tag{5.6}$$

$$G_3 = \frac{1}{1 + \omega_p T_{Ds}} \tag{5.7}$$

$$G_4 = \frac{K_c \omega_p T_{Ds}}{1 + \omega_p T_{Ds}} \tag{5.8}$$

The block diagram of the difference equation represented in equation (5.4) is presented in Figure 5.3.

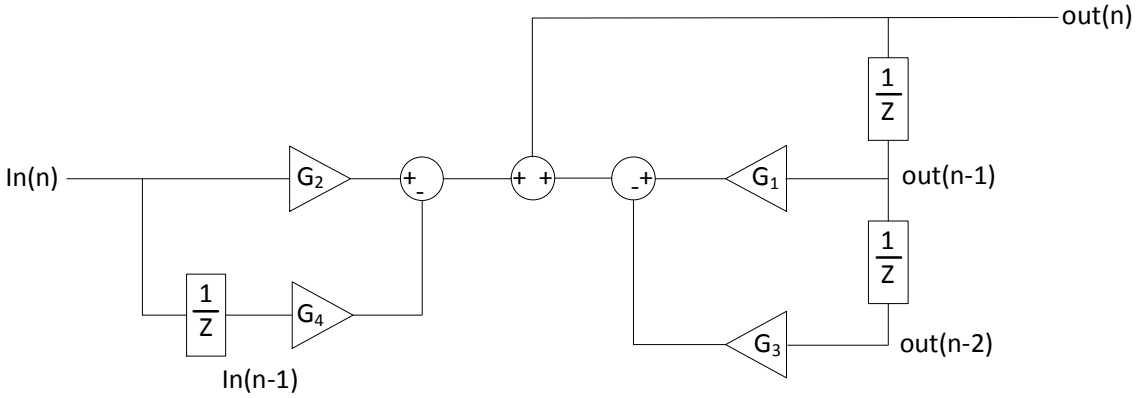


Figure 5.3. Block diagram of the difference equation for a Type II compensator.

5.3 CL Converter Type II Compensator Design and Implementation for CCM Operation

This section presents the design and implementation of a Type II compensator for the inner current loop of the CL boost converter operating in CCM. Due to the fact that the outer-voltage loop PI controller can easily obtain the desired phase margin and crossover, a Type II compensator for the outer loop is unnecessary. The circuit parameters used for the design of the controller are identical to those presented in Section 4.4.1. However, in order to present operation over the full range of the converter, the input voltage is decreased to 150 V, which causes the converter to operate in CCM 2.

5.3.1 Design of Inner Current Loop Type II Compensator

The Bode plots of the duty cycle-to-inductor current transfer function $G_{id}(s)$ of the CL boost converter operating in CCM is presented in Figure 5.4.

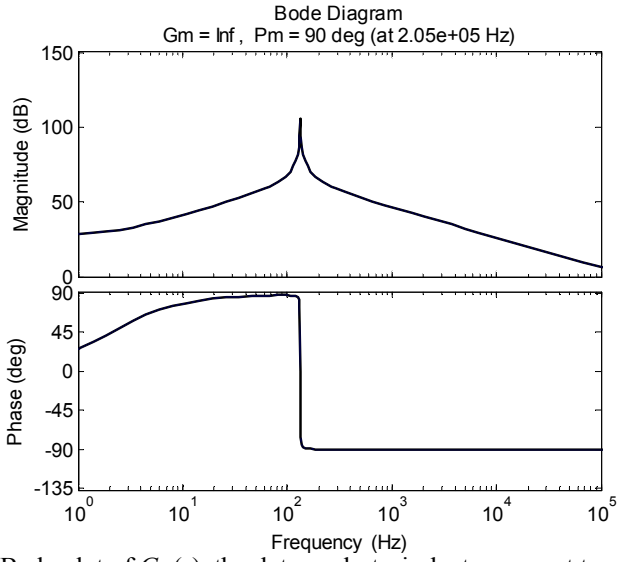


Figure 5.4. Bode plot of $G_{id}(s)$, the duty cycle-to-inductor current transfer function.

Once again, the open-loop phase margin, φ_{pm}, and crossover frequency, f_i, of the system are designed to be 60° and 800 Hz respectively. The current phase at the chosen crossover frequency is -90°. To calculate the position of the pole and zero of the compensator, the phase shift due to the pole at 0 Hz is first added, making the phase at 800 Hz decrease to -180°, as shown in Figure 5.5. Therefore, the current phase margin is 0°.

Since a phase margin of 60° is required, the controller needs to decrease the amount of phase in the system at 1.6 kHz. Hence, the compensator used will be a phase lead

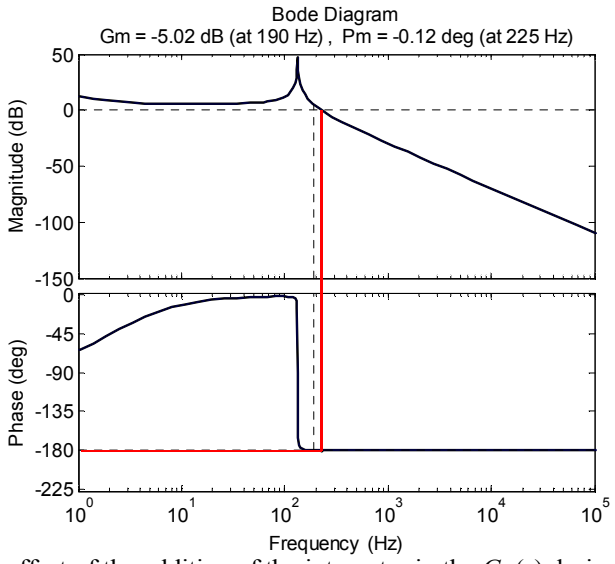


Figure 5.5. The effect of the addition of the integrator in the $G_{id}(s)$ during CCM operation.

compensator, i.e. $\omega_z < \omega_p$. The amount of phase boost needed to be injected, φ_{boost}, is found as

$$\phi_{boost} = \phi_{pm} - \phi_{cpm} \tag{5.9}$$

where φ_{pm} is the desired phase margin, and φ_{cpm} is the current phase margin. From Figure 5.5, it is clearly seen that the current phase margin is 0^o. Hence

$$\phi_{boost} = 60 - 0 = 60 \tag{5.10}$$

With the phase boost and crossover frequency now known, the controller zero is calculated as

$$\omega_z = \frac{2\pi f_i}{\tan\left(45 + \frac{\phi_{boost}}{2}\right)} \tag{5.11}$$

and the controller pole is calculated as

$$\omega_p = 2\pi f_i \tan\left(45 + \frac{\phi_{boost}}{2}\right) \tag{5.12}$$

Hence, the controller pole and zero are at the frequencies

$$\omega_z = 1343 \text{ Hz} \tag{5.13}$$

$$\omega_p = 18811 \text{ Hz} \tag{5.14}$$

To calculate the gain required to bring the crossover frequency to 800 Hz, the pole and zero are inserted into the Type II compensator, the gain, K_c, is set to one, and the open-loop controller and system Bode plot is developed, presented in Figure 5.6.

From Figure 5.6, it is evident that a gain of 14.2 dB is required to increase the magnitude of the open-loop system to 0 dB at 800 Hz. Hence,

$$K_c = 4.92 \tag{5.15}$$

The Type II compensator is now completed, and is in the form

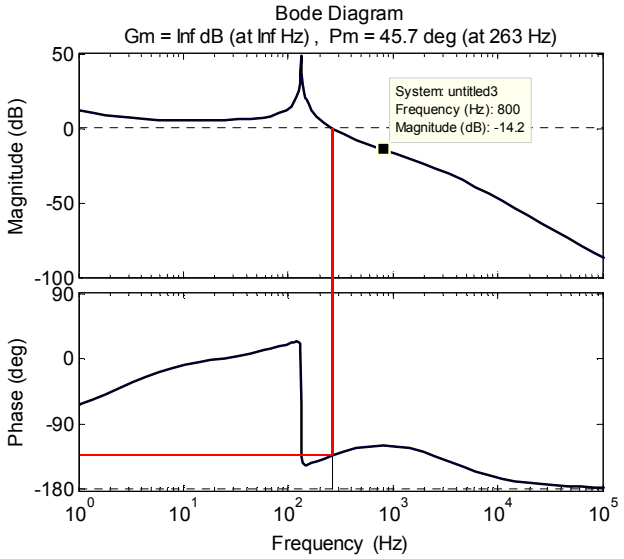


Figure 5.6. Open-loop Bode plot of the Type II compensator and system with controller gain set to 1.

$$C(s) = \frac{4.92}{s}\frac{1+s/1343}{1+s/18811} \tag{5.16}$$

With the compensator designed, the completed open-loop frequency response is presented in Figure 5.7.

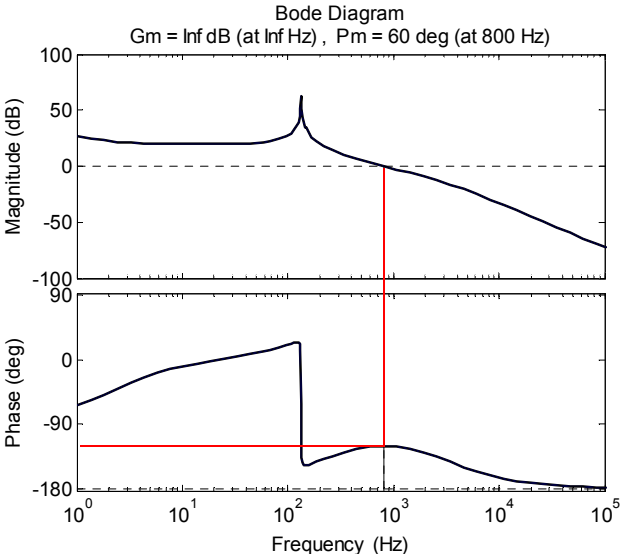


Figure 5.7. Open-loop frequency response of the inner current loop utilising a Type II compensator.

As can be seen from Figure 5.7, the phase margin is now 60° at an open-loop crossover frequency of 800 Hz, and the gain margin is infinite. The closed-loop frequency response is presented in Figure 5.8.

An added benefit of a Type II compensator over the traditional PI controller is the added filtering that comes with the compensator. For example, the Bode plots of the

Type II compensator, and the inner current loop PI controller designed in Section 4.4.1 are presented in Figure 5.9.

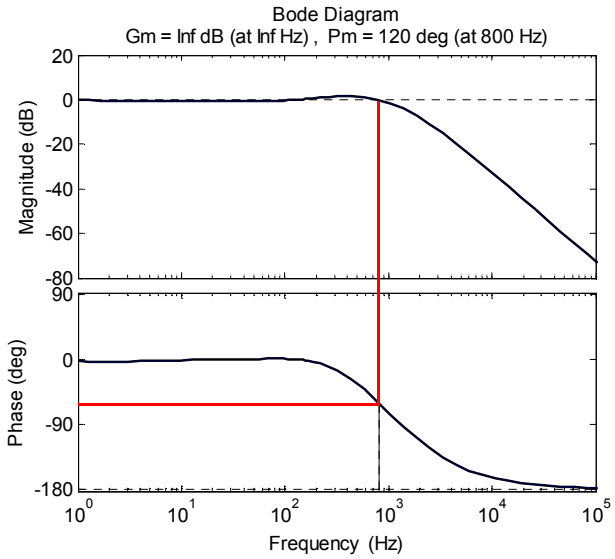


Figure 5.8. Closed-loop frequency response of inner current loop utilising a Type II compensator.

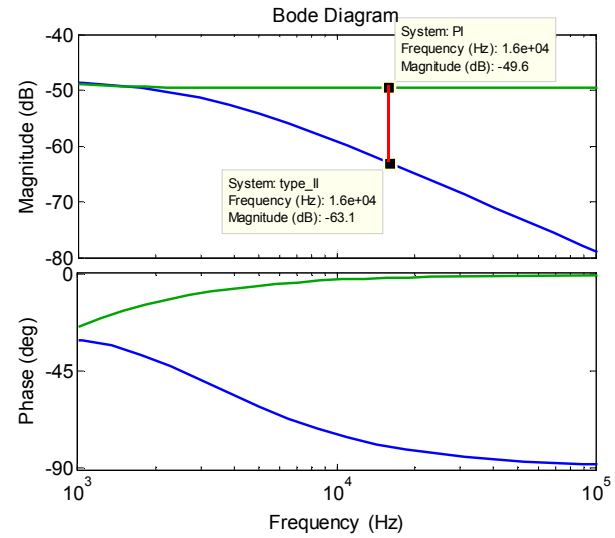


Figure 5.9. Frequency response of C(s) as a PI controller (green) and a Type II compensator (blue).

As can be seen from Figure 5.9, the use of the Type II compensator adds an extra 13.5 dB of attenuation at the switching frequency of the converter. Since the current measurement and feedback into the controller is not filtered, any extra filtering due to the controllers is an added benefit.

With the compensator gain, pole, zero, and a sampling time of 1 µs, the values of G_1, G_2, G_3, and G_4 in the difference equation (5.4) are calculated as

$$G_1 = 1.9815 \tag{5.17}$$

$$G_2 = 8.6116\text{x}10^{-4} \tag{5.18}$$

$$G_3 = 0.9815 \tag{5.19}$$

$$G_4 = 8.6\text{x}10^{-4} \tag{5.20}$$

5.3.2 Simulation and Experimental Results for Type II Compensator

The SimPowerSystems package in the Matlab®/Simulink software is once again utilized to first test the designed controllers before implementation. For the practical experiments, the difference equation is programmed into the FPGA for testing on the 1 kW prototype. To compare to the results, the three tests, start-up, steady-state and load-step response are performed.

5.3.2.1 Converter Start-Up in CCM Utilising Type II Compensators

As with the previous testing, the output capacitor is first allowed to charge to the level of the input voltage. Once the capacitor is fully charged, the converter is switched on, and the output voltage and phase currents are recorded. Figure 5.10 presents the output voltage and inductor current responses over the full start-up time of the converter. For all experimental results presented in this chapter, the scaling of the scope for all experimental waveforms are specified with the results.

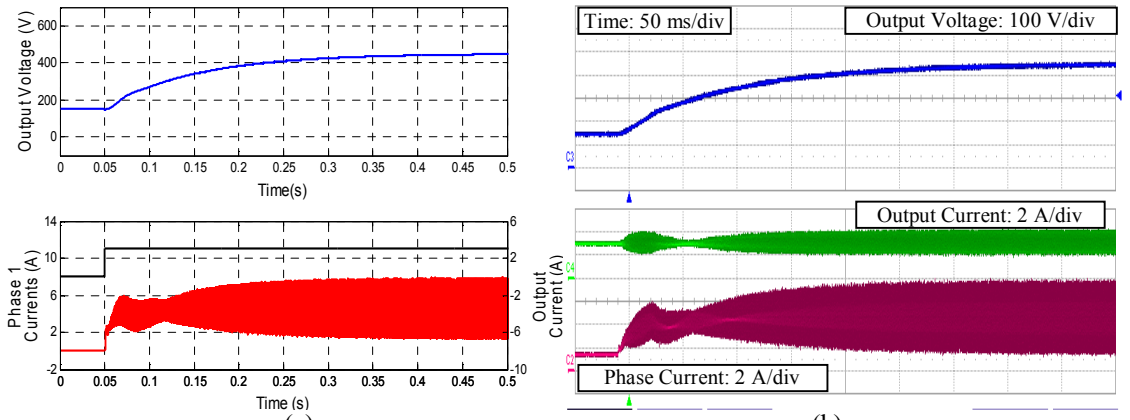
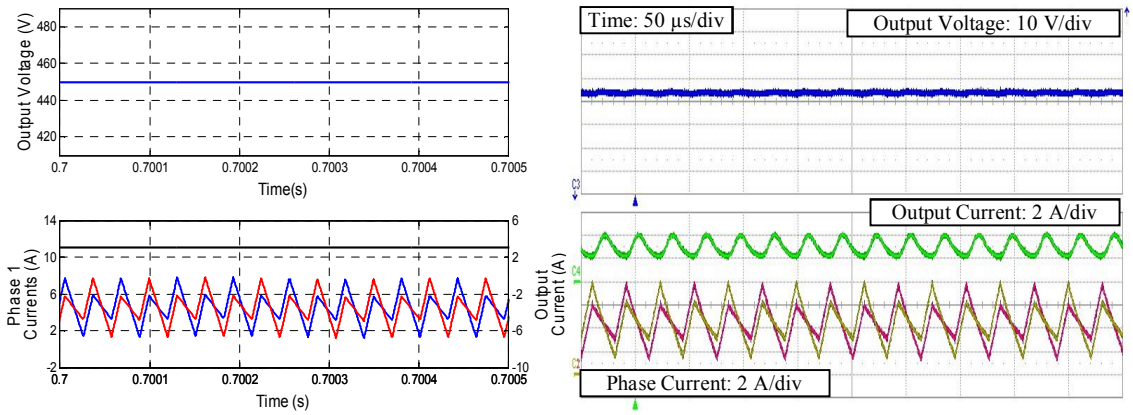


Figure 5.10. Simulated (a) and experimental (b) response of the closed-loop CL boost converter operating in CCM during start-up.

5.3.2.2 Steady-State in CCM Utilising Type II Compensators

As with the PI controller tests, the converter is allowed to run for approximately 5 minutes to ensure stable operation. Figure 5.11 presents the output voltage and inductor current responses over 500 µs.

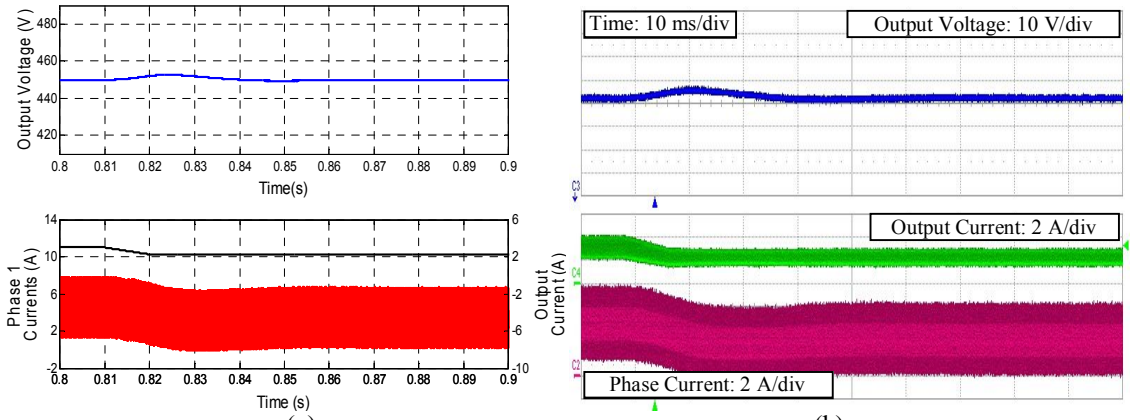


(a) (b)

Figure 5.11. Simulated (a) and experimental (b) response of the closed-loop CL boost converter operating in CCM during steady-state operation.

5.3.2.3 Load-step Test in CCM Utilising Type II Compensators

During the load-step test, a command is sent to the load to drop the value of current to 75 % of its current value at a rate of 66 A/s. The transients of the output voltage and phase currents are recorded, and presented in Figure 5.12 below.

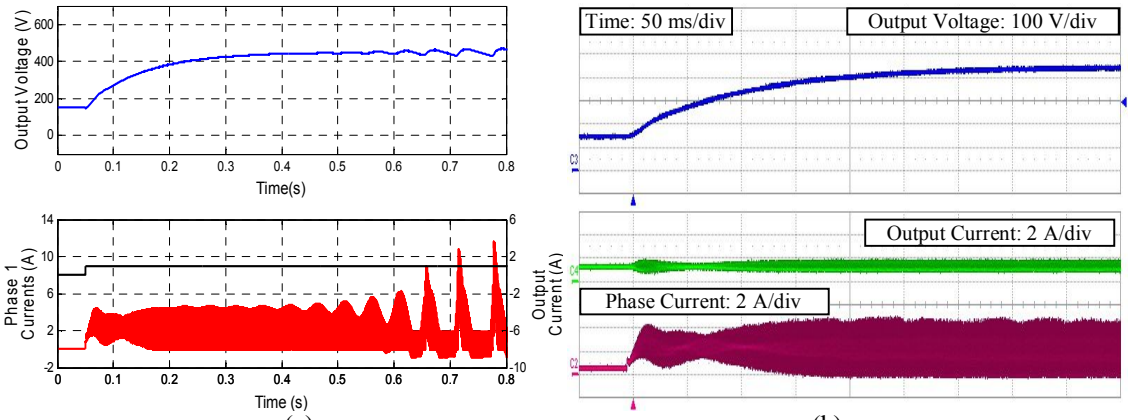


(a) (b)

Figure 5.12. Simulated (a) and experimental (b) response of the closed-loop CL boost converter operating in CCM during load-step test.

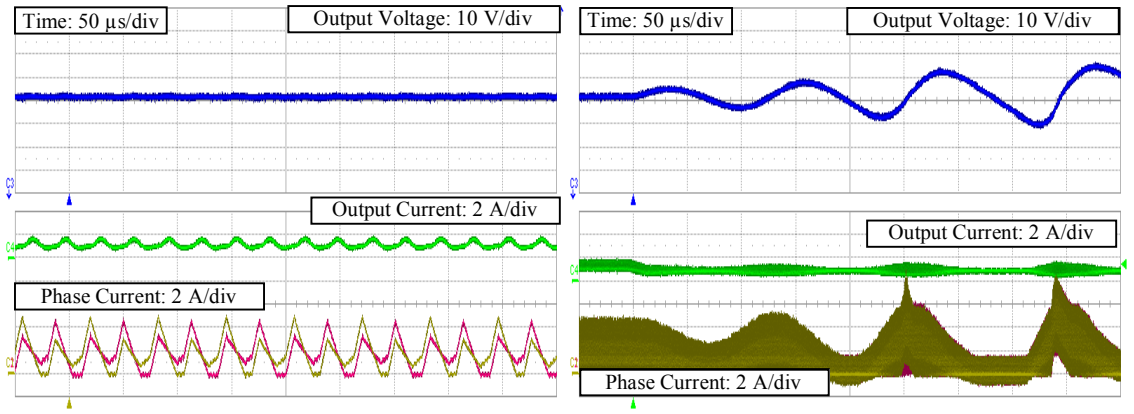
5.3.3 CCM Designed Type II Compensators for DCM 8 Operation

In order to test the stability of the CCM controllers for DCM operation, the output current is dropped to 1.2 A, causing the converter to enter DCM 3. The two tests of start-up (Figure 5.13), and steady-state (Figure 5.14 (a)), are undertaken. As can be seen from the simulated results, the converter begins to oscillate before settling into steady-state. Due to this, a simulated load-step test was not performed. However, during the experimental tests, the converter does settle to a steady-state value, as seen in Figure 5.14. This enabled a load-step to 0.7 A over 10 ms to be introduced into the system, presented in Figure 5.15 (b). As can be seen, the load-step causes the converter to begin oscillating, similar to the oscillations seen in the simulated results.



(a) (b)

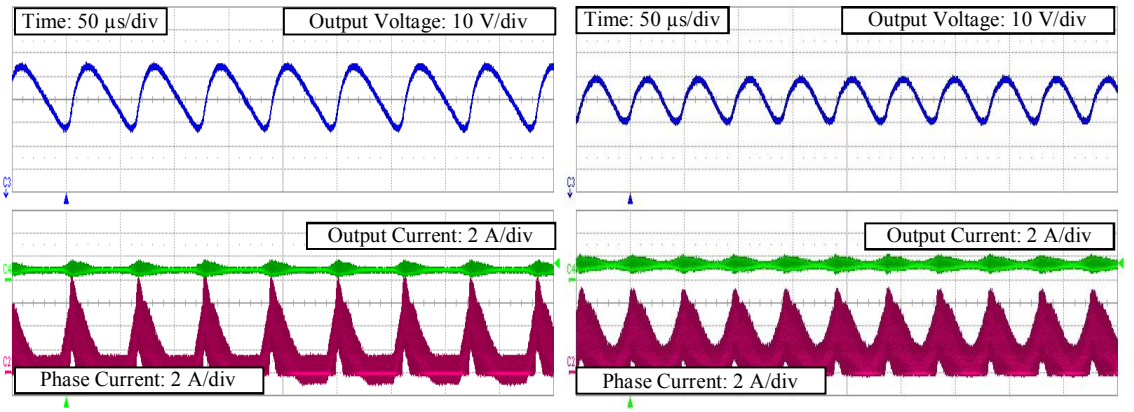
Figure 5.13. Simulated (a) and experimental (b) response of the closed-loop CL boost converter utilizing CCM controllers operating in DCM 3 during start-up.



(a) (b)

Figure 5.14. Experimental response of the closed-loop CL boost converter utilizing CCM controllers operating in DCM 8 during steady-state (a), and load-step test (b).

Figure 5.15 (a) presents the converter in steady-state after the load drops. As can be seen, the converter does not settle after the oscillations begin. Finally, the current was increased to the original value of 1.2 A to check whether the oscillations disappear, as shown in Figure 5.15 (b). As can be seen, the oscillations to not settle, and the converter continues to operate in marginal stability.



(a) (b)

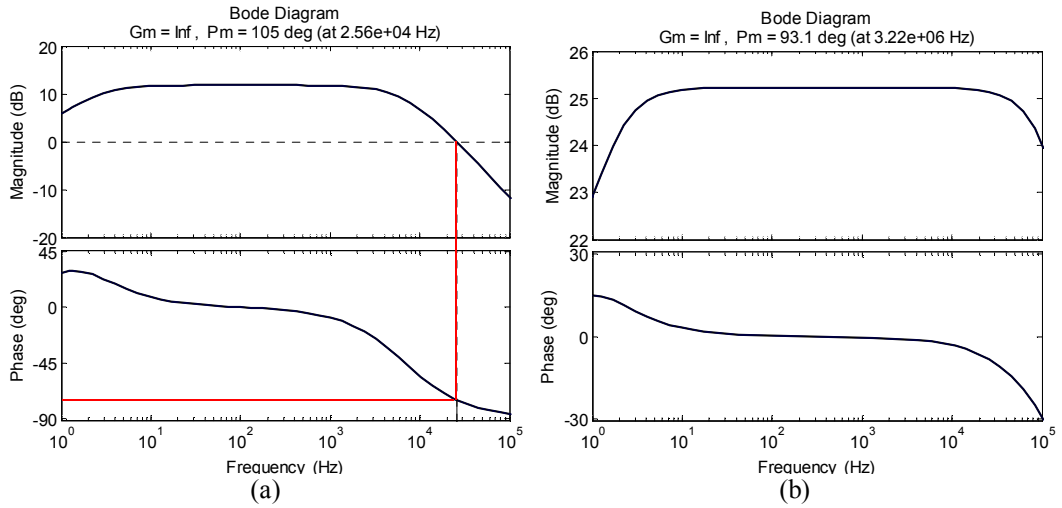
Figure 5.15. Experimental response of the closed-loop CL boost converter operating in CCM during steady-state operation at 0.7 A (a), and 1.2 A (b).

5.3.4 Design of Inner Current Loop Type II Compensators for DCM Operation

Two DCM modes are chosen to test the DCM controllers on the CL boost converter, DCM 3 and DCM 8. Due to the noise that is inherent to operation in DCM 3, it is one of the most difficult modes to control.

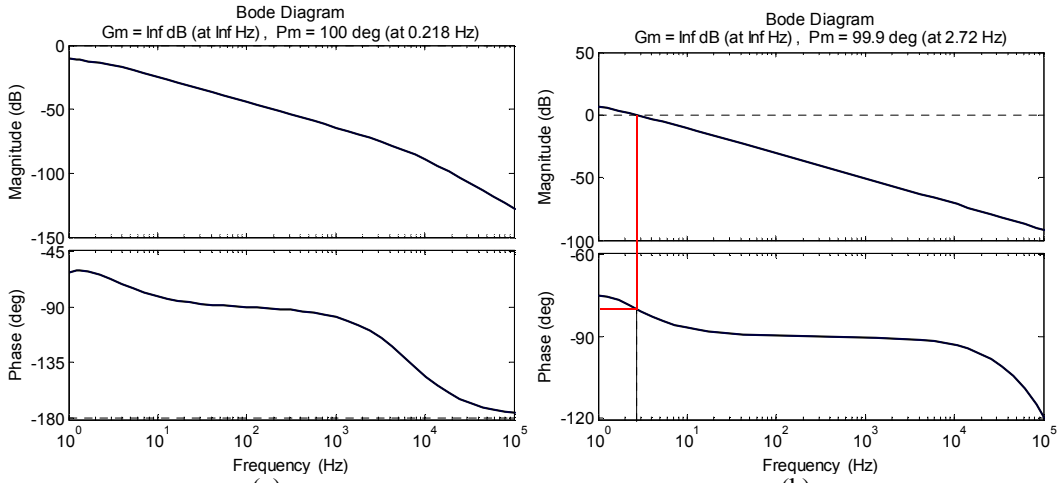
The converter parameters are as follows; output voltage is V_{out} = 450 V, leakage inductance is L_{Lk} = 350 µH, magnetising inductance is L_m = 1000 µH, output capacitance is C_{out} = 900 µF, duty cycle is D = 0.5, frequency is f_s = 16 kHz, output load resistance is R_{out} = 450 Ω, and the converter power is P_{out} = 450 W. In order to test DCM 3 operation, the input voltage is set to V_{in} = 225 V, while for DCM 8, it is set to V_{in} = 150 V.

The Bode plots of the duty cycle-to-inductor current transfer function $G_{id}(s)$ of the CL boost converter operating in DCM 3 and DCM 8 are presented in Figure 5.16. Through experimental testing, it is found that DCM 3 is one of the noisiest DCM modes of operation. Hence, to help with the attenuation of the noise, the crossover frequency of the inner current loop will be set to thirty times less than the switching frequency i.e. for DCM 3, f_i = 530 Hz. For DCM 8, the crossover frequency will remain at 800 Hz. To design such a controller, the Bode plots of $G_{id}(s)$, with the inclusion of the pole at 0 Hz are once again presented in Figure 5.16 and Figure 5.17 respectively.



(a) (b)

Figure 5.16. Bode plot of $G_{id}(s)$, the duty cycle-to-inductor current transfer function of (a) DCM 3 and (b) DCM 8.



(a) (b)

Figure 5.17. The effect of the addition of the integrator in the $G_{id}(s)$ during (a) DCM 3 and (b) DCM 8.

As can be seen from the frequency responses, the phase margin of both systems are above 60° at the desired crossover frequencies. Hence, the compensator used in both systems will be a phase lag compensator i.e. $\omega_z > \omega_p$. The amount of phase boost that needs to be injected, φ_{boost}, is found as

$$\phi_{boost} = -(\phi_{pm} - \phi_{cpm}) \tag{5.21}$$

where φ_{pm} is the desired phase margin, and φ_{cpm} is the current phase margin. From Figure 5.17, it is clearly seen that the current phase margins are 85° for DCM 3 and 90° for DCM 8. Hence

$$\phi_{boost} = -(60 - 85) = 25 \tag{5.22}$$

for DCM 3, and

$$\phi_{boost} = -(60 - 90) = 30 \tag{5.23}$$

for DCM 8. With the phase boost and crossover frequency now known, the controller zero is calculated as

$$\omega_z = 2\pi f_i \tan\left(45 + \frac{\phi_{boost}}{2}\right) \tag{5.24}$$

and the controller pole is calculated as

$$\omega_p = \frac{2\pi f_i}{\tan\left(45 + \frac{\phi_{boost}}{2}\right)} \tag{5.25}$$

Hence, for DCM 3, the controller pole and zero are at the frequencies

$$\omega_z = 5330 \text{ Hz} \tag{5.26}$$

$$\omega_p = 2107 \text{ Hz} \tag{5.27}$$

while for DCM 8,

$$\omega_z = 8668 \text{ Hz} \tag{5.28}$$

$$\omega_p = 2915 \text{ Hz} \tag{5.29}$$

To calculate the gain required to bring the crossover frequency to 530 Hz for DCM 3 and 800 Hz for DCM 8, the pole and zero are inserted into the Type II compensator, the gain, K_c, is set to one, and the open-loop controller and system Bode plot is developed, presented in Figure 5.18.

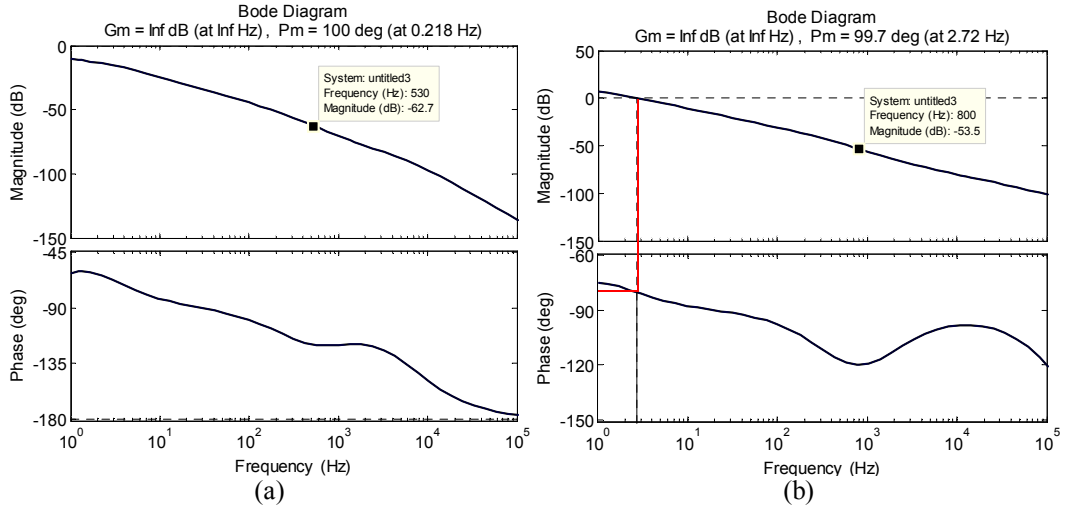


Figure 5.18. Open-loop Bode plot of the Type II compensator and system with controller gain set to 1 during (a) DCM 3, and (b) DCM 8.

From Figure 5.18, it is evident that, for DCM 3 a gain of 62.7 dB is required to increase the magnitude of the open-loop system to 0 dB at 800 Hz, while for DCM 8, 50.8 dB is required. Hence, for DCM 3

$$K_c = 1373 \tag{5.30}$$

and

$$C(s) = \frac{1373}{s} \frac{1 + s/5330}{1 + s/2107} \tag{5.31}$$

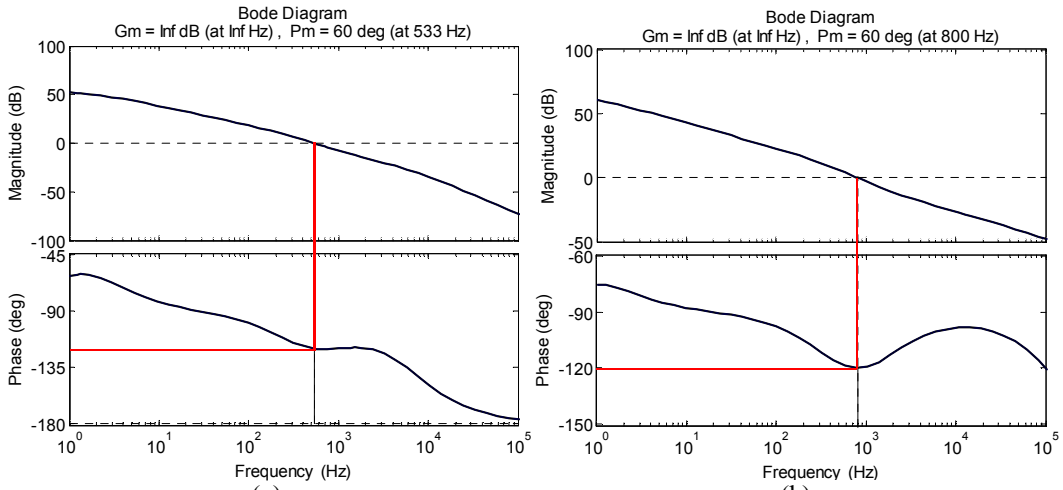
while for DCM 8

$$K_c = 474 \tag{5.32}$$

and

$$C(s) = \frac{474}{s} \frac{1 + s/8668}{1 + s/2915} \tag{5.33}$$

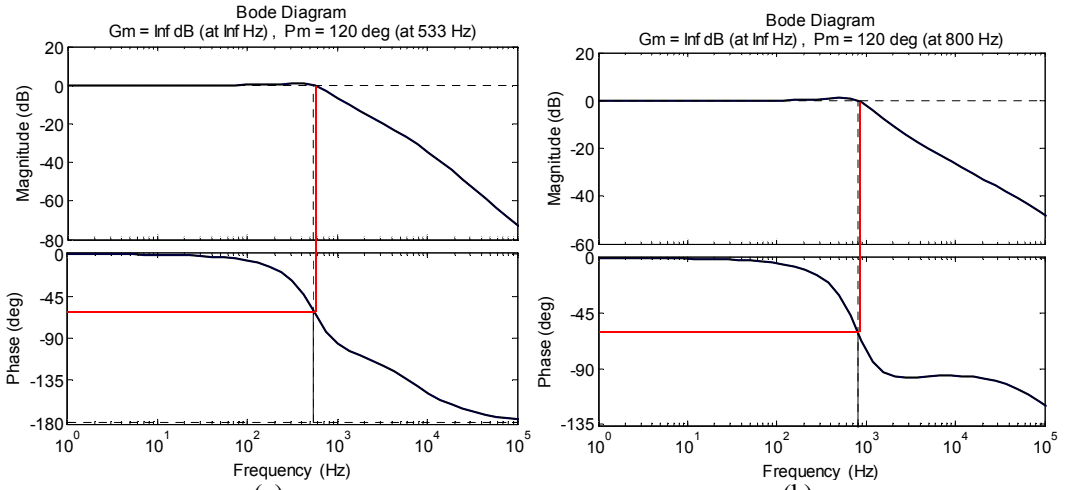
With the compensator designed, the completed open-loop frequency response is presented in Figure 5.19.



(a) (b)

Figure 5.19. Open-loop frequency response of the inner current loop utilising a Type II compensator during (a) DCM 3 and (b) DCM 8.

As can be seen from Figure 5.19, the phase margins are now 60° at an open-loop crossover frequency of 800 Hz for DCM 3 and 1.6 kHz for DCM 8. The gain margin is infinite. The closed-loop frequency responses are presented in Figure 5.20.



(a) (b)

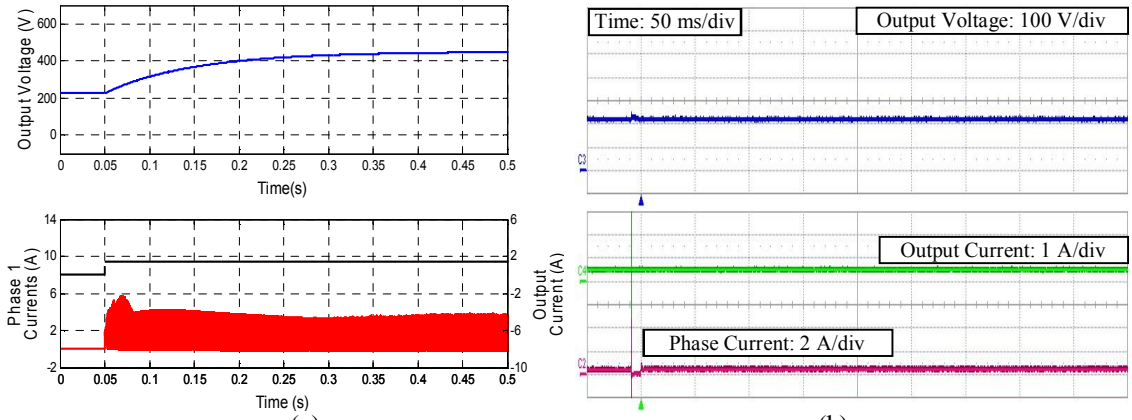
Figure 5.20. Bode plot of the closed-loop current loop of the CL boost converter in (a) DCM 3 and (b) DCM 8 utilizing a Type II compensator.

5.3.5 Simulation and Experimental Results of Type II Controllers in ACMC of the CL Boost Converter operating in DCM

As with the CCM tests, a Simulink model of the closed-loop CL converter operating in DCM 8 and DCM 3 is compared to experimental tests run on the 1 kW prototype during start-up.

5.3.5.1 Converter Start-Up in DCM 3 Utilising Type II Compensators

Figure 5.21 presents the output voltage and inductor current responses over the full start-up time of the converter.



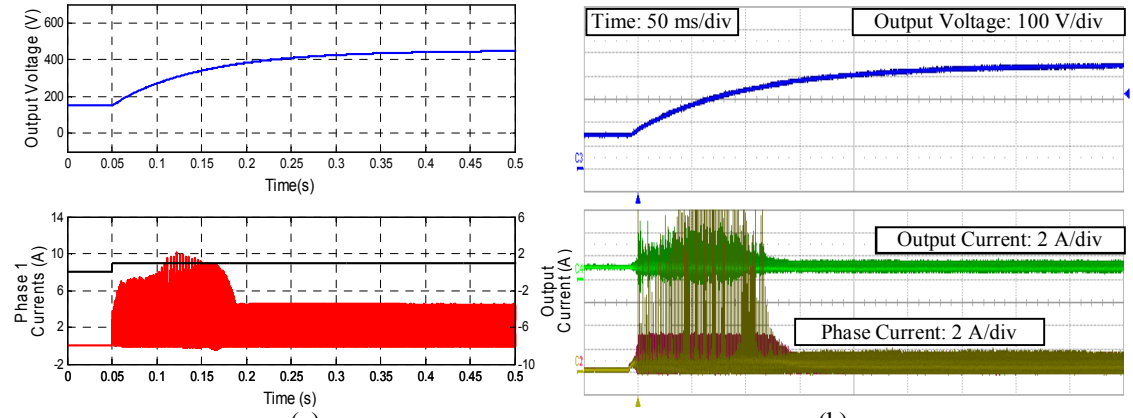
(a) (b)

Figure 5.21. Simulated (a) and experimental (b) response of the closed-loop CL boost converter operating in DCM 3 during start-up.

It is clear from the simulated results that the converter is highly unstable during start-up, but stabilises after 80 ms. However, during experimental testing, the converter appears to enter current limit, and switches off completely.

5.3.5.2 Converter Start-Up in DCM 8 Utilising Type II Compensators

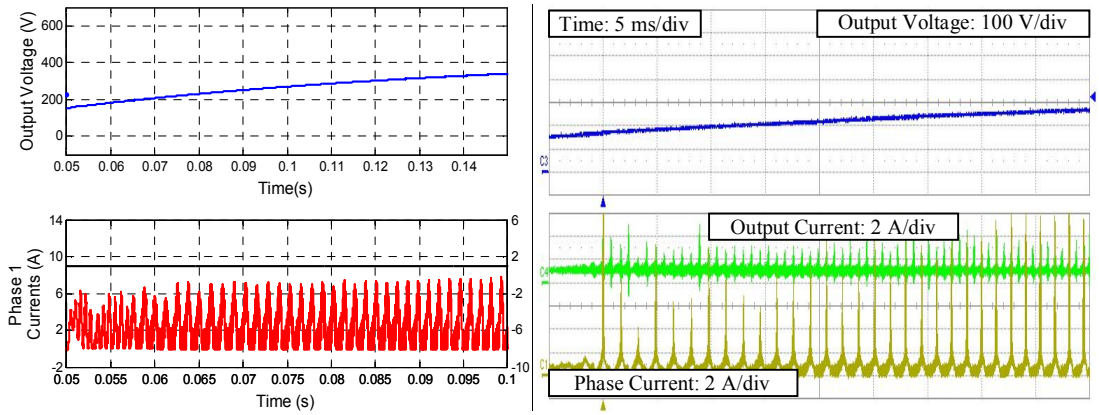
Figure 5.22 presents the output voltage and inductor current responses over the full start-up time of the converter.



(a) (b)

Figure 5.22. Simulated (a) and experimental (b) response of the closed-loop CL boost converter operating in DCM 8 during start-up over 500 ms.

As with DCM 3, the initial start-up of the converter is highly unstable. A closer look is presented in Figure 5.23. Conversely to DCM 3 operation, the converter is able to stabilise before switch off in DCM 8.



(a) (b)

Figure 5.23. Simulated (a) and experimental (b) response of the closed-loop CL boost converter operating in DCM 8 during start-up over 100 ms.

5.4 Forced-Output Control of CL Converter

The Type II compensators developed in Section 5.3 are designed specifically for each CCM and DCM mode of operation. A compensator designed for CCM, while stable, will not be optimal for DCM operation. A more strenuous problem is the fact that a controller designed for DCM operation, will most likely be unstable for CCM operation. This is due to the fact that, to obtain a phase margin of 60^o during DCM operation, the current loop controllers need to inject over 90^o of phase into the system. If this controller is utilised when operating in CCM, the open-loop phase margin will cross the -180^o axis, causing loop instability. This is evident during converter start-up, presented in Figure 5.21 to Figure 5.23. As the converter begins to power up, it initially operates in CCM. As can be seen from the experimental results, the oscillations in the waveforms may cause the converter to go unstable unless it enters DCM quickly. While a solution to this problem is to increase the converter start-up time, ensuring the converter never enters CCM, it is not an ideal solution. Another problem with this is the inability of the converter to operate over the entire range of its load.

One of the major benefits of digital control is the ability to introduce several different controllers, with no added hardware. Hence, in order to control the CL converter over several modes of operation, a Type II compensator for each mode is designed and programmed into the FPGA. During operation, each compensator calculates the required duty cycle needed to decrease the converter output voltage error to zero. However, the output of only one compensator is used at any one time. This is labelled as the active controller. All remaining controllers are labelled as inactive. The active controller is determined by the mode of operation the converter is in.

A disadvantage of using this type of control is the inherent “bump” which will occur when changing controllers. Even though all controllers are Type II compensators, they will be designed with different coefficients. Hence, the output of the inactive controllers will not equal the output of the active controller. When the system determines it must change from the output of the active controller to the output of the inactive controller, the difference in the output between the previously active controller and the now active controller will cause a large transient, which may be sufficient to cause the system to go unstable.

5.4.1 Bumpless Control

In order to counteract this transient, a “bumpless” control strategy, presented in Figure 5.24, is introduced [5.4]. The control strategy presented in [5.4] utilises an

additional controller, $G_{bx}(s)$, to try to force the output of the inactive controller, $C_{i2}(s)$, to equal the output of the active controller, $C_{i1}(s)$. Hence, when a controller changes from the output of the active controller to the inactive controller, there is little to no transient. The output of the now inactive controller, $C_{i1}(s)$, is forced to try to equal the output of the now active controller, $C_{i2}(s)$, which takes full control of the converter.

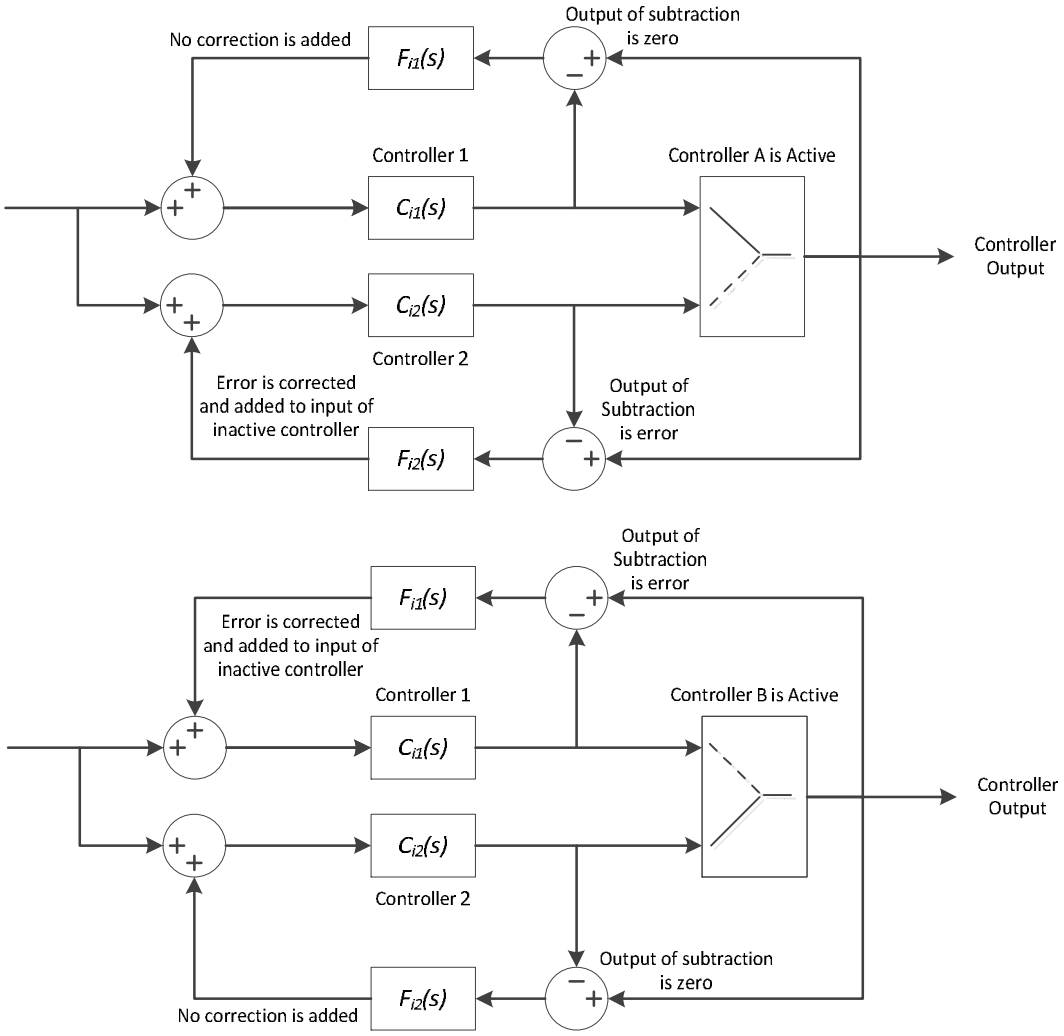


Figure 5.24. Bumpless control strategy.

5.4.2 Mode Determination

In order to determine the mode of operation of the converter, the output of the voltage-loop PI controller, i.e. the reference current, is measured. This measured value is then compared to a given value of dc current, chosen by the operator, called the mode limit. If the reference current is greater than the mode limit, the controller will assume the converter is operating in mode A, and the mode A controller is active. If the reference current is less than the mode limit, the controller for mode B is activated. For example, the CCM-DCM mode map of a CL boost converter is presented in Figure 5.25. For the purpose of this analysis, it is assumed that the voltage gain of the converter

is constant, and set at three. As can be seen, once the dc current in the converter drops to a certain value, the converter will enter DCM. With the mode map, it is easy to calculate the condition. Since it is the reference current that is measured, the mode limit will be determined by the dc phase currents.

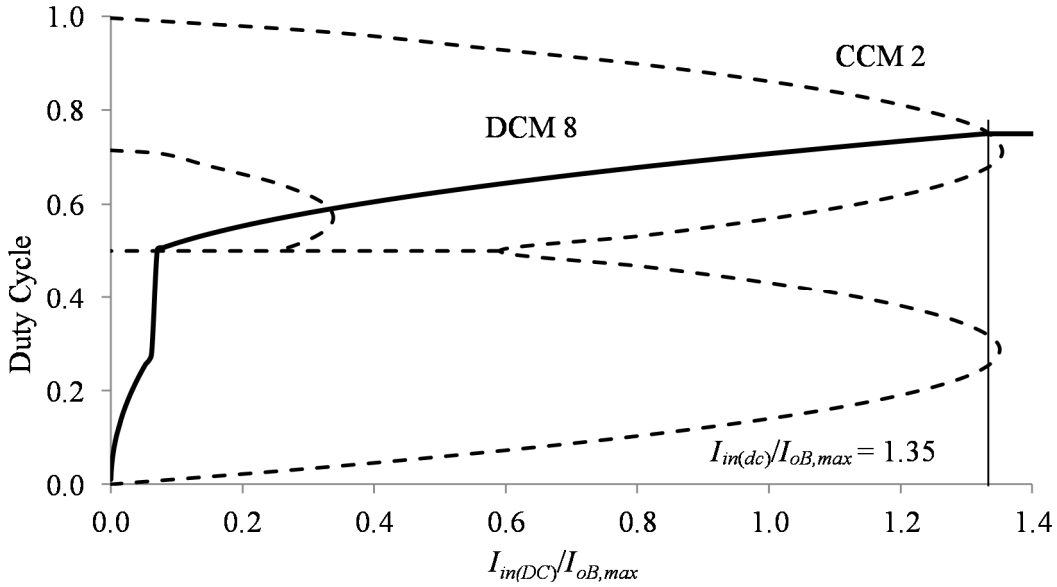


Figure 5.25. CCM-DCM mode map of the CL converter, showing the input current at which the converter leaves CCM 2 and enters DCM 8.

By comparing this phase current with the mode limit, it is easy to ascertain which mode the converter is operating in. This method can also be applied to all other modes of operation, assuming the voltage gain of the converter remains constant.

5.4.3 Bumpless PI Control

This section focuses on implementing bumpless control for the inner current loop when utilising PI controllers. Due to the simplicity of programming PI controllers, these control types will be the first to be implemented with bumpless control. A single PI voltage controller will be implemented, which will produce the reference phase current for all PI current controllers which follow. The converter will operate with an input voltage of 150 V, and an output voltage of 450 V. The initial output current will be set at 400 mA. This will cause the converter to operate in DCM 9. A PI current controller is developed for an open-loop phase margin of 100^{o} and a crossover frequency of 800 Hz. The PI controller gains are

$$\begin{aligned} K_{pi(D9)} &= 0.0169 \\ K_{ii(D9)} &= 400 \end{aligned} \tag{5.34}$$

A load-step drop of 280 mA over 10 ms will then cause the converter to leave DCM 9 and enter DCM 7. Hence, a second PI controller is developed for DCM 7, in which

the open-loop phase margin and crossover over frequency are once again 100° and 800 Hz, respectively. The PI controller gains are

$$K_{pi(D7)} = 0.1$$
$$K_{ii(D7)} = 2941 \tag{5.35}$$

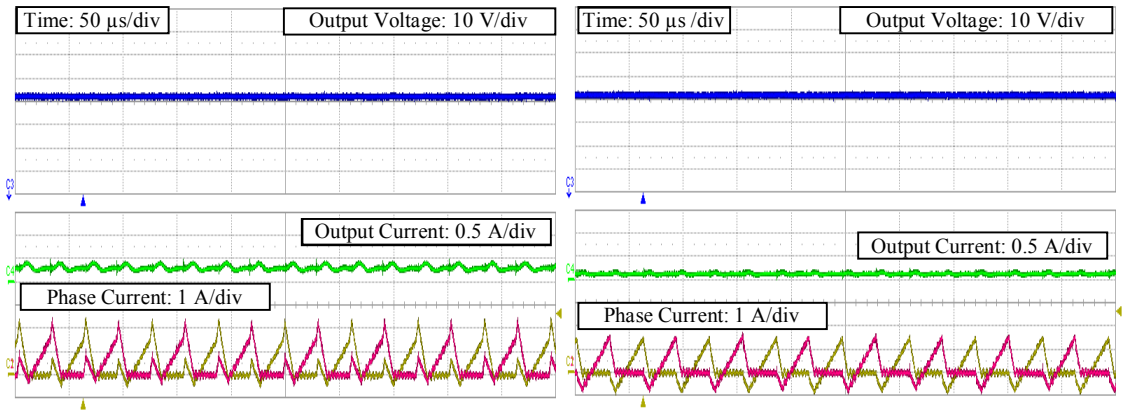
With the PI controllers designed, the bumpless controllers must next be designed. To ensure stability, a proportional controller is implemented. Both open-loop PI controllers are designed for a crossover frequency of 100 Hz. Hence, the gain for the DCM 9 PI controller is

$$K_{BD9} = 1.9 \tag{5.36}$$

While the gain for the DCM7 PI controller is

$$K_{BD7} = 0.39 \tag{5.37}$$

Using the mode map, it is found that the converter will leave DCM 9 and enter DCM 7 at 300 mA dc phase current. Hence, the mode limit is set to 0.5. Figure 5.26 presents the steady-state waveforms of DCM 9 and DCM 7, while Figure 5.27 presents the experimental results of the load-step drop.



(a) (b)

Figure 5.26. Experimental steady-state waveforms of DCM 9 (a) and DCM 7 (b) under PI control.

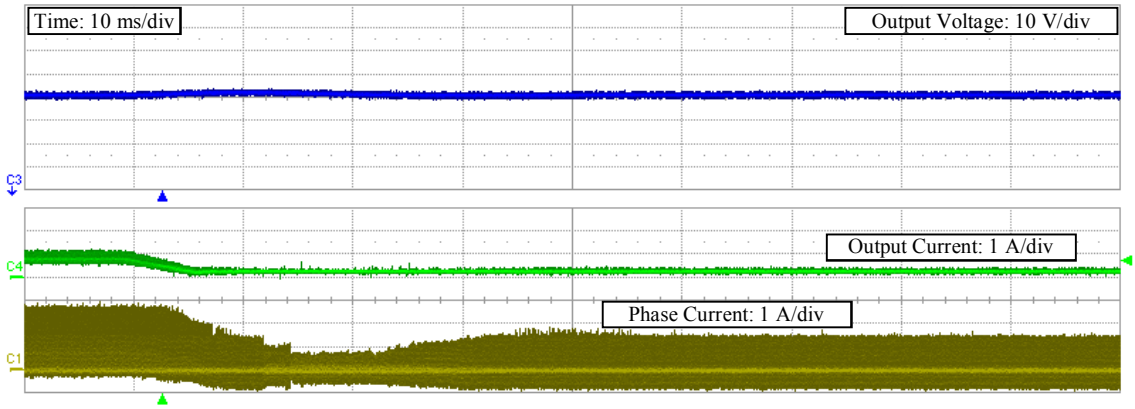


Figure 5.27. Experimental results of the load-step drop, causing the converter to leave DCM 9 and enter DCM 7 utilising PI controllers with bumpless control.

The Quartus FPGA programming software allows the user to view signals which are running in the FPGA via the SignalTap II Logic analyser tool. With this tool, the user is able to view the moment the controllers switch, the output of both controllers, and the final chosen output. These plots are presented in Figure 5.28 to Figure 5.30.

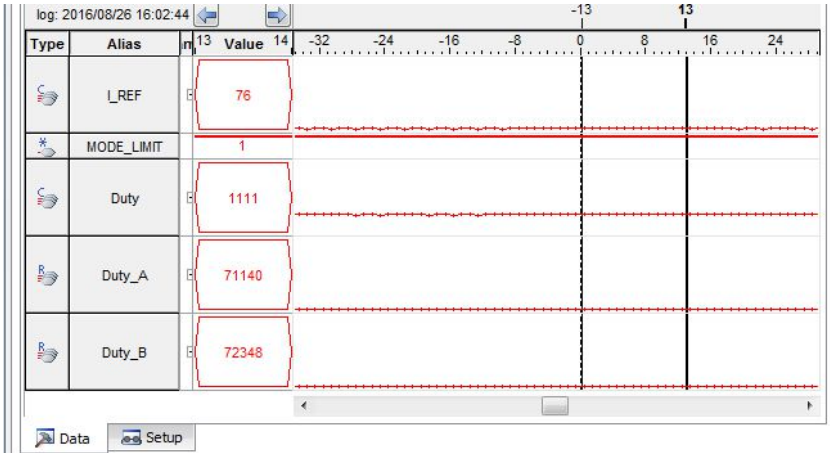


Figure 5.28. SignalTap tool showing operation during DCM 9 utilising PI controller with bumpless control.

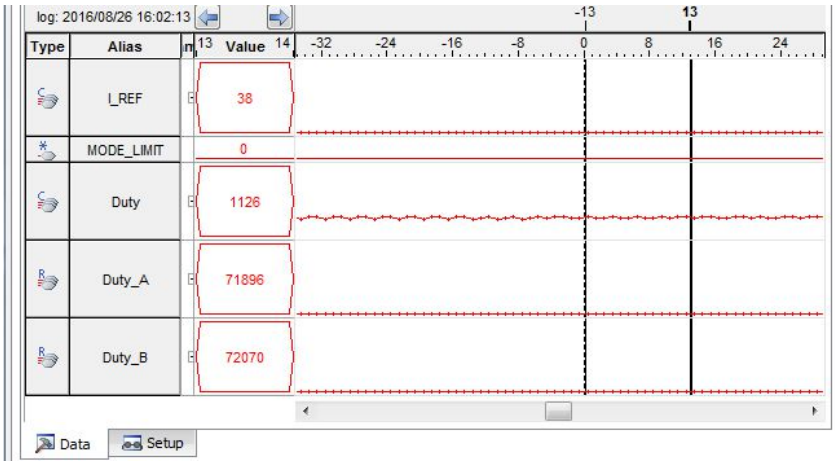


Figure 5.29. SignalTap tool showing operation during DCM 7 utilising PI controller with bumpless control.

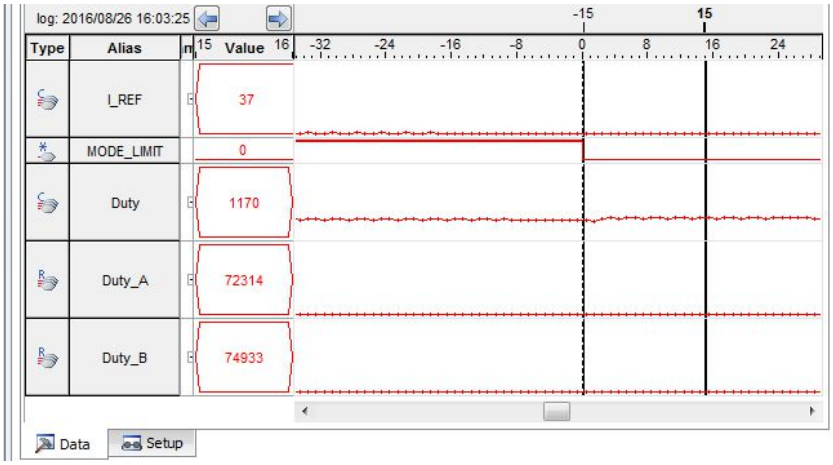


Figure 5.30. SignalTap tool showing the moment of switching between DCM 9 and DCM 7 utilising PI controller with bumpless control.

In Figure 5.28 to Figure 5.30, the reference inductor current, I_REF, the converter duty cycle Duty, and the output of both PI controllers Duty_A and Duty_B are presented in the form of unsigned line charts. Also shown is MODE_LIMIT, which determines which mode the converter is in. When the value of TST is 1, the converter is in DCM 9, and the output of the controller comes from Duty_A. When TST is 0, the converter is in DCM 7, and the output of the controller comes from Duty_B. It should be noted that the duty cycle of the converter, as well as active and inactive PI controllers are in the form of 2^Q notation. The duty cycle is scaled by 2^{11}, while the output of the PI controllers are scaled by 2^{17}. The reference current is scaled by 161.

As can be seen, a slight transient is seen during the load drop. By analysing the SignalTap screenshot, it can be seen that while in DCM 9, the output of the controller is identical to the output of the active PI controller, but not the inactive controller i.e.

$$\frac{1111}{2^{11}} = \frac{71140}{2^{17}} = 0.543 \neq \frac{72348}{2^{17}} = 0.552 \tag{5.38}$$

Since the outputs of the active and inactive controllers are not equal, a small steady-state error is present in the bumpless control scheme.

5.4.4 Forced-Output Control

This section focuses on the implementation of what the author termed Forced-Output Control (FOC). The FOC strategy is similar to the bumpless control strategy in that the objective is to force the output of the inactive controller to equal the output of the active controller up until the mode limit is encountered. The advantages of FOC over bumpless control are the ability to essentially eliminate steady-state errors between both controller outputs, as well as the fact that no feedback control needs to be designed. Another benefit of forced-output control is the relative ease of implementation compared to bumpless control. The main drawback of FOC is the inability to implement it in an analogue controller.

To design an FOC strategy, the difference equation of the Type II compensator presented in (5.4) is given for the active controller

$$out_{ac}(n) = G_{2ac}in_{ac}(n) - G_{4ac}in_{ac}(n-1) + G_{1ac}out_{ac}(n-1) - G_{3ac}out_{ac}(n-2) \tag{5.39}$$

and the inactive controller

$$out_{nc}(n) = G_{2nc}in_{nc}(n) - G_{4nc}in_{nc}(n-1) + G_{1nc}out_{nc}(n-1) - G_{3nc}out_{nc}(n-2) \tag{5.40}$$

The objective of the controller is to ensure the output of the inactive controller equals the output of the active controller i.e.

$$out_{nc}(n) = out_{ac}(n) \tag{5.41}$$

In reality, this is impossible due to the fact that the coefficients of the difference equations are not equal i.e.

$$\begin{aligned} G_{1ac} &\neq G_{1nc} \\ G_{2ac} &\neq G_{2nc} \\ G_{3ac} &\neq G_{3nc} \\ G_{4ac} &\neq G_{4nc} \end{aligned} \tag{5.42}$$

Due to the fact that, in a digital controller, the previous samples of a system are accessible, what is possible is the ability to force the output of the inactive controller to equal the previously sampled output of the active controller i.e.

$$out_{nc}(n) = out_{ac}(n-1) \tag{5.43}$$

To implement equation (5.43), the following assumption is made

$$out_{nc}(n-1) = out_{nc}(n-2) \tag{5.44}$$

Hence

$$out_{nc}(n) = out_{ac}(n-1) = G_{2nc} in_{nc}(n) - G_{4nc} in_{nc}(n-1) + (G_{1nc} - G_{3nc}) out_{nc}(n-1) \tag{5.45}$$

By rearranging equation (5.45), it is found that

$$out_{nc}(n-1) = \frac{out_{ac}(n-1) - G_{2nc} in_{nc}(n) + G_{4nc} in_{nc}(n-1)}{(G_{1nc} - G_{3nc})} \tag{5.46}$$

Since

$$G_1 - G_3 = 1 \tag{5.47}$$

then

$$out_{nc}(n-1) = out_{ac}(n-1) - G_{2nc} in_{nc}(n) + G_{4nc} in_{nc}(n-1) \tag{5.48}$$

Inserting equation (5.48) into the (5.40) and simplifying, it is found that

$$out_{nc}(n) = out_{ac}(n-1) \tag{5.49}$$

By implementing equations (5.44) and (5.48) into the inactive controller, the output of the inactive controller is forced to equal the output of the active controller, delayed by one sample. Hence, the steady-state error between the active controller and the inactive controller is minimized, and, for a fast enough sampling time, can be considered to be zero. Once the inactive controller is activated, and the active controller is deactivated, the now active controller reverts to the difference equation of (5.4), and the now inactive controller reverts into the difference equations of (5.44) and (5.48). A block diagram of the system is presented in Figure 5.31.

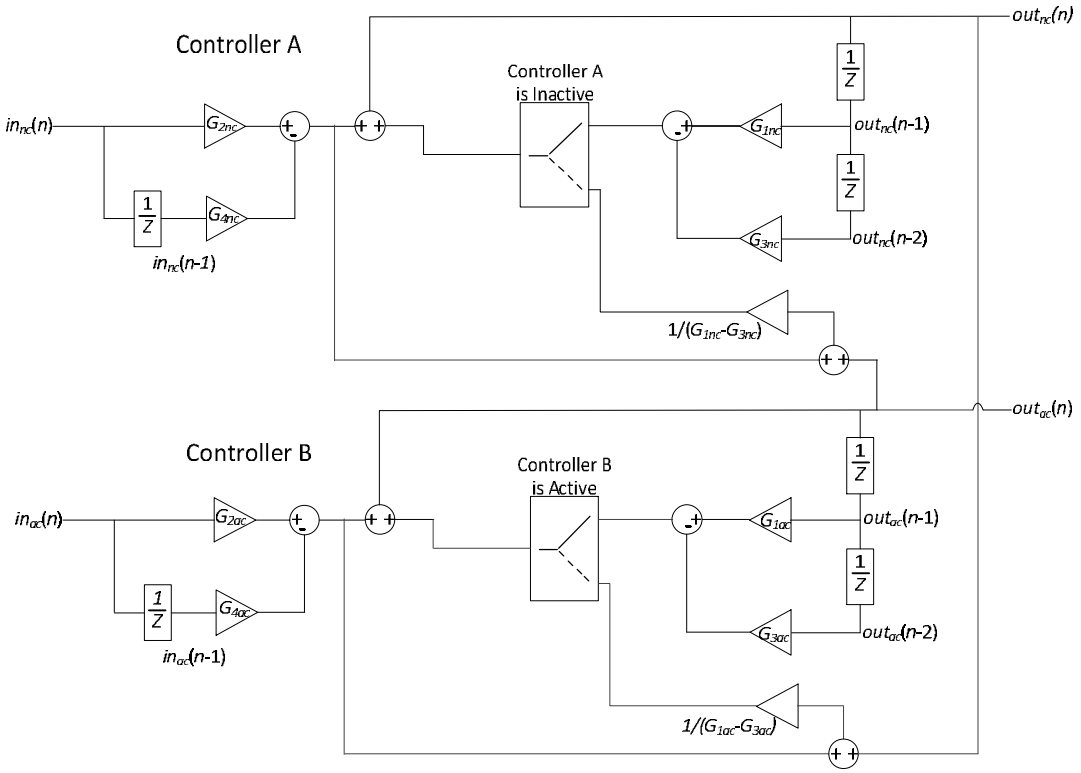


Figure 5.31. Block Diagram of Forced-Output Control for two Type II compensators.

A simplified version of Figure 5.31 is presented in Figure 5.32, in which a FOC control scheme is implemented into Controller A, but not on Controller B, which is set as the active controller. The signal $E(z)$, is the result of the input sample, $in_{nc}(n)$, times $X_1(z)$. This signal is subtracted from the output of the active controller, but delayed by one sample. This "inherent delay" is due to the fact that the program must wait one sample to determine which controller output is active. Finally, the result from the subtraction is added to $E(z)$, which cancels with the negative $E(z)$ i.e.

$$out_{ac}(n-1) - E(z) + E(z) = out_{ac}(n-1) = out_{nc}(n) \tag{5.50}$$

Therefore, the output if the inactive controller is forced to equal the output of the active controller, delayed by one sample.

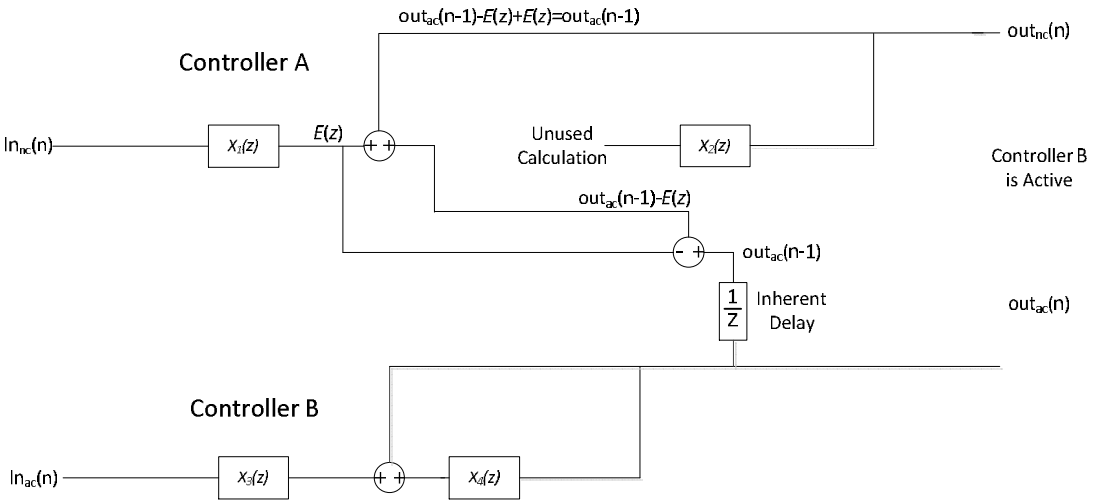


Figure 5.32. Simplified block diagram of FOC.

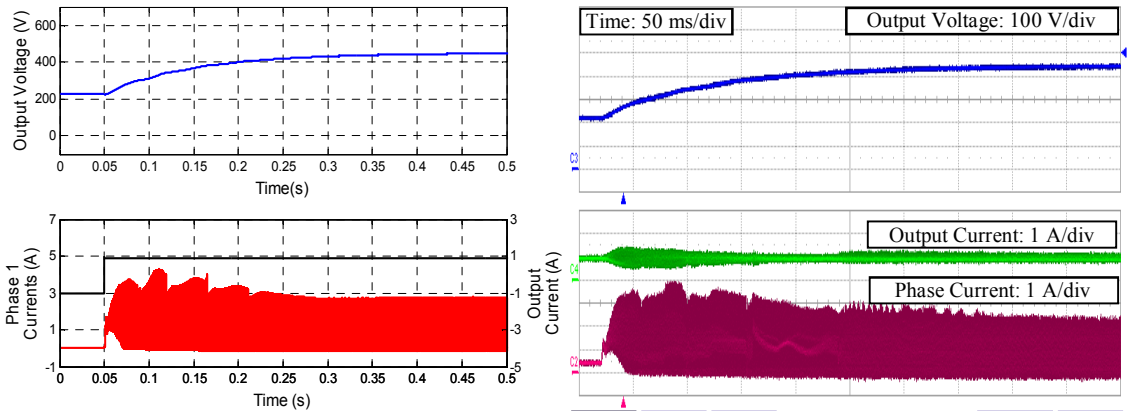
With the ability to seamlessly switch between converter modes of operation, experimental testing of the DCM Type II compensators can now be performed.

5.4.5 Simulation and Experimental Results of Type II Controllers in ACMC of the CL Boost Converter operating in DCM using Forced-Output Control

As shown in Section 5.3.5, it was impossible to fully test the Type II compensators for DCM operation without stability issues due to the converter entering CCM during start up. The use of FOC control solves these issues by ensuring the converter is initially controlled by the CCM Type II compensator. Once the reference current of the controller passes the mode limit, the output of the controller will be switched from the CCM compensator to the DCM compensator. To avoid ringing around the mode limit, a hysteresis band of 10% is applied to the value of the mode limit. In addition, a dead time is introduced into the mode limit to ensure the converter will always use the CCM Type II compensator until a certain output voltage is reached. This is due to the fact that, during the first few milliseconds of start-up, the converter current will be less than the mode limit, even though it is still operating in CCM. Through experimentation, it is found that at approximately 200 V on the output, the converter current will enter DCM 3, while it will enter DCM 8 at approximately 400 V. It is possible to calculate the exact voltage the converter will enter DCM by plotting the inductor current peak-to-peak ripple and the inductor dc current over the range of input voltages, while keeping the output voltage constant. However, experimental results were utilised due to their availability at the time.

5.4.5.1 Converter Start-Up in DCM 3 Utilising Type II Compensators with FOC

Figure 5.33 presents the output voltage and inductor current responses over the full start-up time of the converter. The output current of the converter is set to 0.9 A.



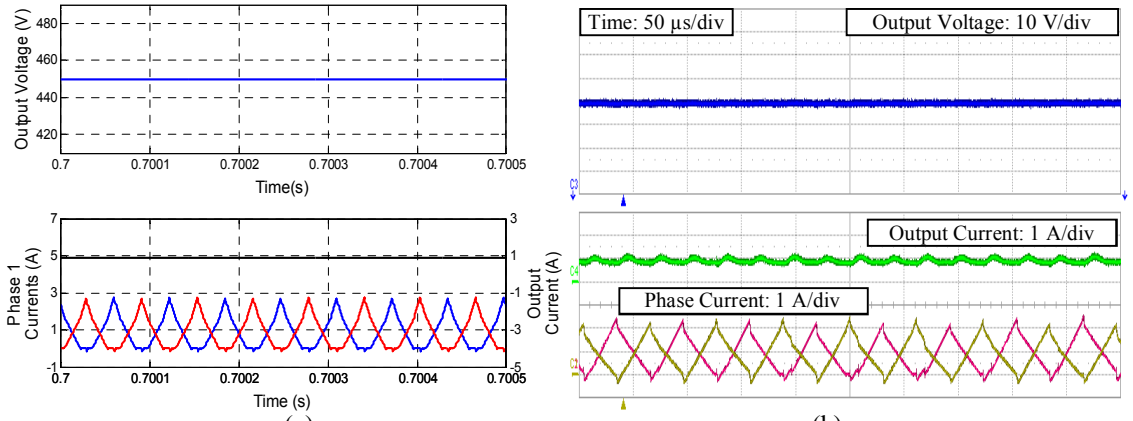
(a) (b)

Figure 5.33. Simulated (a) and experimental (b) response of the closed-loop CL boost converter operating in CCM during start-up.

The notches which are evident from Figure 5.34 are when the controller switches. As can be seen, the FOC scheme switches controllers several times during start-up, which is undesirable. More stringent parameters for when the controller switches may be introduced to reduce this ringing.

5.4.5.2 Steady-State in DCM 3 Utilising Type II Compensators with FOC

Figure 5.34 presents the output voltage and inductor current responses over the following 500 µs.

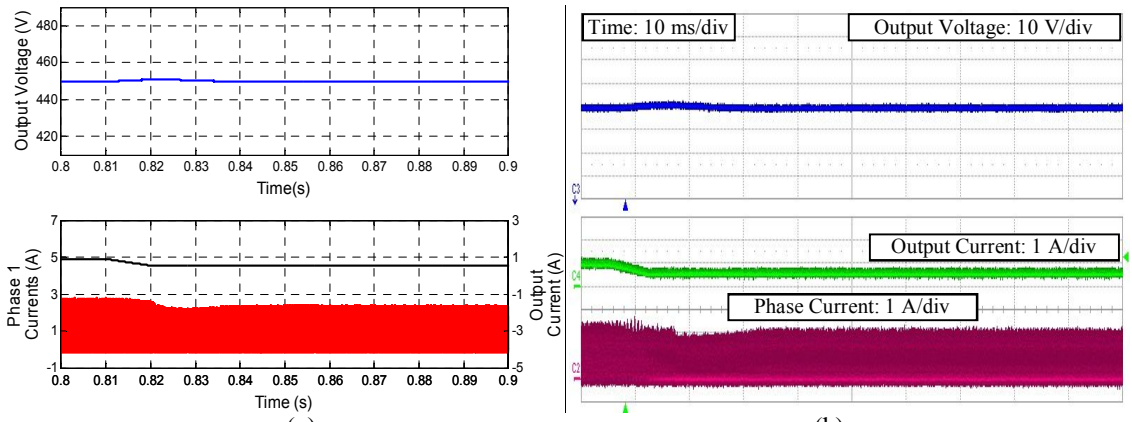


(a) (b)

Figure 5.34. Simulated (a) and experimental (b) response of the closed-loop CL boost converter operating in CCM during steady-state operation.

5.4.5.3 Load- Step Test in DCM 3 Utilising Type II Compensators with FOC

During the load-step test, a command is sent to the load to drop the value of current to 65 % of its current value at a rate of 30 A/s. The transients of the output voltage and phase currents are recorded, and presented in Figure 5.35 below.

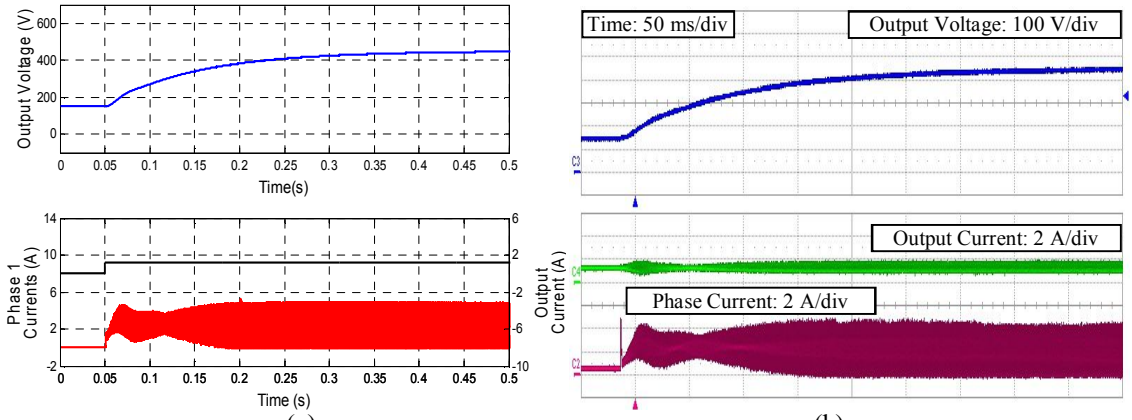


(a) (b)

Figure 5.35. Simulated (a) and experimental (b) response of the closed-loop CL boost converter operating in CCM during load-step test.

5.4.5.4 Converter Start-Up in DCM 8 Utilising Type II Compensators with FOC

Figure 5.36 presents the output voltage and inductor current responses over the full start-up time of the converter.

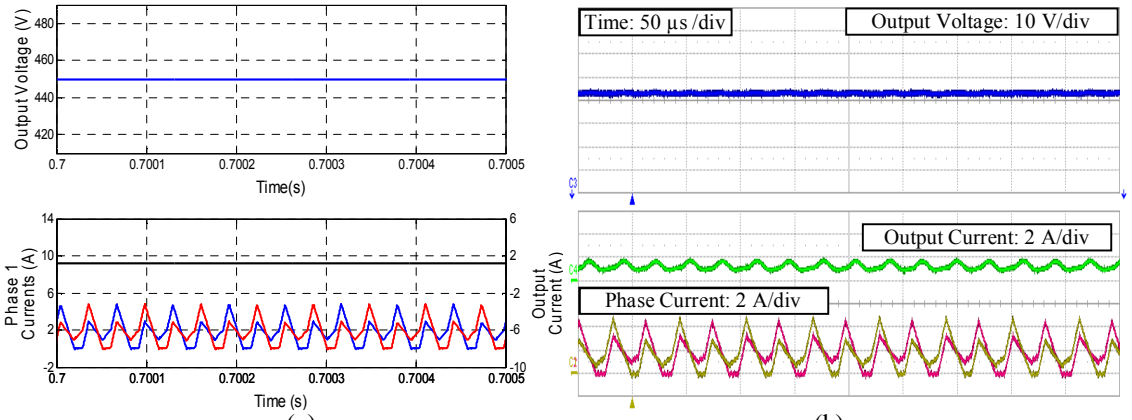


(a) (b)

Figure 5.36. Simulated (a) and experimental (b) response of the closed-loop CL boost converter operating in CCM during start-up.

5.4.5.5 Steady-State in DCM 8 Utilising Type II Compensators with FOC

Figure 5.37 presents the output voltage and inductor current responses over the following 500 µs. The output current is set at 1.5 A.

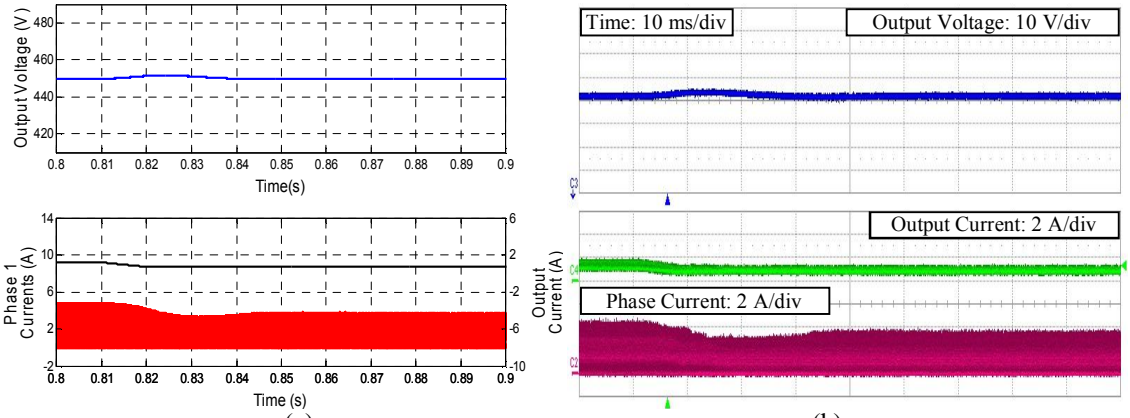


(a) (b)

Figure 5.37. Simulated (a) and experimental (b) response of the closed-loop CL boost converter operating in CCM during steady-state operation.

5.4.5.6 Load-Step Test in DCM 8 Utilising Type II Compensators with FOC

During the load-step test, a command is sent to the load to drop the value of current to 54 % of its current value at a rate of 70 A/s. The transients of the output voltage and phase currents are recorded, and presented in Figure 5.38 below.



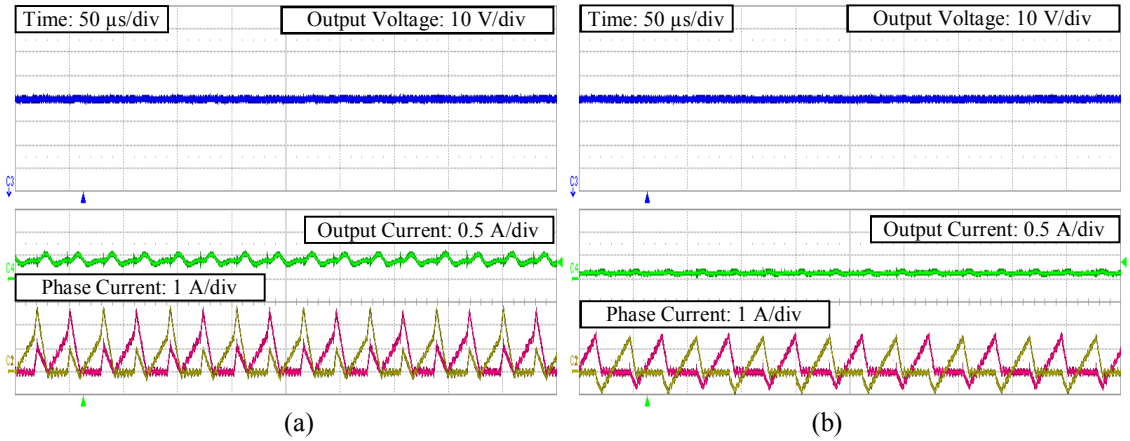
(a) (b)

Figure 5.38. Simulated (a) and experimental (b) response of the closed-loop CL boost converter operating in CCM during load-step test.

One of the more evident benefits of utilising type-II compensators is the apparent balance between the phases when operation in DCM. As can be seen from Figure 5.34 and Figure 5.37, the steady-state waveforms of both phases are nearly identical, indicating both the dc currents and duty cycles of the two phases are similar in value.

5.4.5.7 Load-Step Test from DCM 9 to DCM 7 Utilising Type II Compensators with FOC

To compare the bumpless control strategy with the FOC control strategy, an identical load-step from DCM 9 to DCM 7 was performed. The results are presented in Figure 5.39 and Figure 5.40 and compared to the bumpless controller in Figure 5.41.



(a) (b)

Figure 5.39. Experimental steady-state waveforms of DCM 9 (a) and DCM 7 (b) under Type II compensator control.

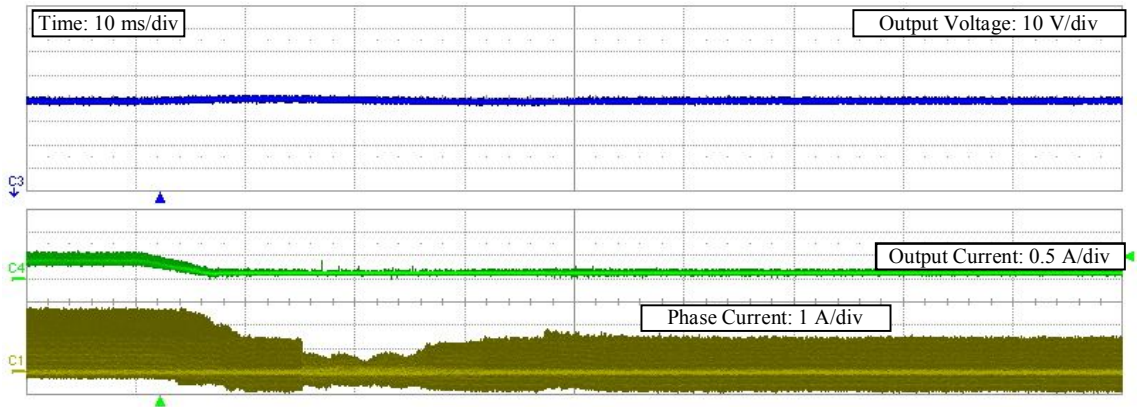
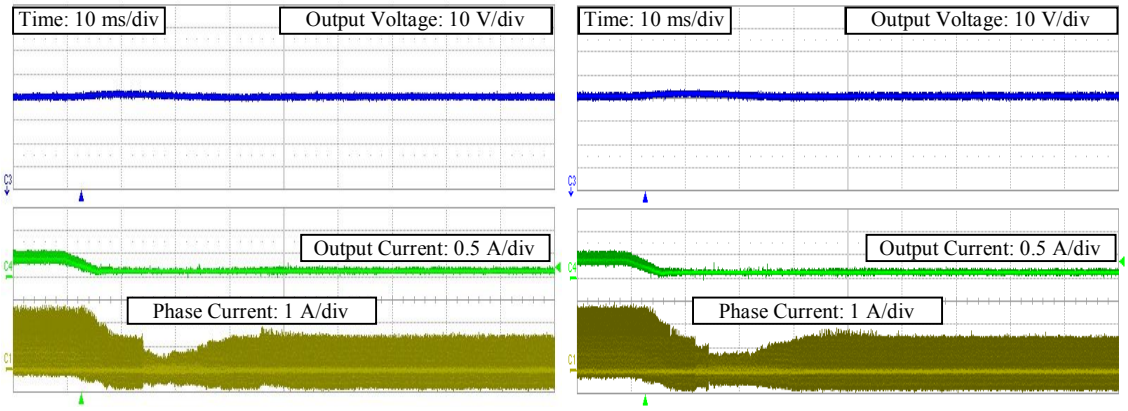


Figure 5.40. Experimental results of the load-step drop, causing the converter to leave DCM 9 and enter DCM 7 utilising Type II compensators with FOC.



(a) (b)

Figure 5.41. A comparison of controller and mode change from DCM 9 to DCM 7 utilising FOC (a) and bumpless control (b).

As can be seen from Figure 5.39 to Figure 5.41, the utilisation of Type II compensators for control yields a much better steady-state operation. Not only is steady-state operation improved, but the implementation of the FOC strategy yields a faster transient response. The diagrams of the SignalTap tool are presented in Figure 5.42 and Figure 5.43.

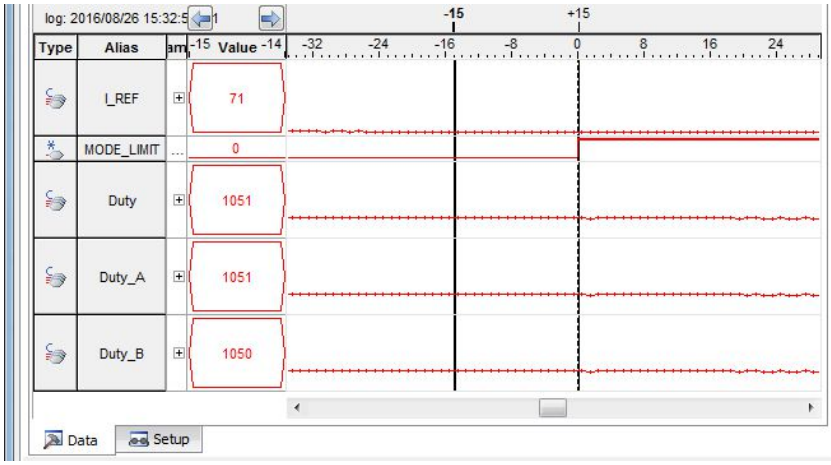


Figure 5.42. SignalTap tool showing the switching between DCM 9 and DCM 7 utilising Forced-Output control controller with bumpless control (Duty cycles before switch).

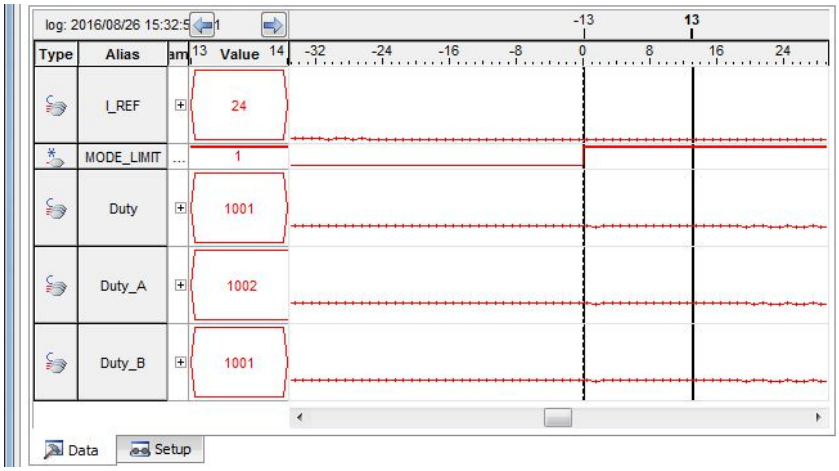


Figure 5.43. SignalTap tool showing the switching between DCM 9 and DCM 7 utilising Forced-Output control controller with bumpless control (Duty cycles after switch).

As with the previous SignalTap diagrams, in Figure 5.42 and Figure 5.43, the reference inductor current, I_REF, the converter duty cycle Duty, and the output of both PI controllers, Duty_A and Duty_B, are presented in the form of unsigned line charts. Also shown is MODE_LIMIT, which determines the converter mode. For this test, when the value of TST is 0, the converter is in DCM 9, and the output of the controller comes from Duty_B. When TST is 1, the converter is in DCM 7, and the output of the controller comes from Duty_A. All controller outputs are scaled by 2^{11}, while the reference inductor current is once again scaled by 161.

As can be seen, a slight transient is seen during the load drop. By analysing the SignalTap screenshot, it can be seen that while in DCM 9, the output of the controller is identical to the both Type II compensator outputs i.e.

$$\frac{1051}{2^{11}} = \frac{1051}{2^{11}} = \frac{1050}{2^{11}} = 0.51 \tag{5.51}$$

Therefore, there is no steady-state error between the outputs of the two Type II compensators, minimising any transient that occurs during the load-step.

5.5 Conclusions

This chapter has presented the design and implementation of digital average-current-mode control utilizing Type II compensators. The Type II compensators are designed for CCM operation, and were tested in both simulation and experimentation. The CCM designed compensator was tested for use with DCM. These results are not optimal due to the oscillations which occur during the load-step test. Hence, additional Type II compensators were designed for several DCM modes. Due to the fact that, during start-up, the converter operates in CCM, these DCM designed controllers may lead to instability during start-up. Hence, bumpless control and Forced-Output control (FOC) were developed. A bumpless control scheme was applied to the PI controllers designed in Chapter 4 for a load-step test between DCM 9 and DCM 7. These results were compared to a FOC strategy designed with Type II compensators. The results show much better operation when utilising Type II compensators with FOC control. With the ability to implement FOC control, the start-up, steady-state and load-step tests of DCM 3 and DCM 8 were performed with Type II compensators.

5.6 References

[5.1] A. Ghosh and S. Banerjee, "Design and implementation of Type II compensator in dc-dc switch-mode step-up power supply," *International Conference on Computer, Communication, Control and Information Technology*, pp. 1-5, February 2015.

[5.2] C. Shetty, "Studying the dynamics of the second-order dc-dc converter with single and multi-loop feedback for the optimum bandwidth," *International Conference on Advances in Computing and Communications*, pp. 352-355, August 2014.

[5.3] N. Mohan (2003), *First Course on Power Electronics and Drives*, MNPERE.

[5.4] J. Steenis, and A. Dumais, "Bumpless control for reduced THD in power-factor correction circuits," *IEEE Applied Power Electronics Conference*, pp. 3219-3223, March 2016.

[5.5] P. Y. Wang, S. Y. Huang, K. Y. Fang, and T. H. Kuo, "An undershoot/overshoot-suppressed current-mode buck converter with voltage-setting control for Type II compensator," *IEEE Asian Solid-State Circuits Conference*, pp. 1-4, November 2015.

[5.6] M. Comanescu, "Influence of the discretization method on the integration accuracy of observers with continuous feedback," *2011 IEEE International Symposium on Industrial Electronics*, pp. 625-630, Gdansk, 2011.

6 CONCLUSIONS

This chapter presents a summary and discussion of the findings presented in this thesis. With the complete mathematical solutions of the large-signal and small-signal models now available, the ability to digitally control a two-phase interleaved coupled-inductor boost converter is made much easier. Along with this, the introduction of bumpless control utilising PI type controllers, and Forced-Output Control utilising Type II compensators, allow for optimal performance of the converter over the full load range of the converter.

6.1 Chapter Summaries

This section briefly summarises the content and results of each chapter of this thesis.

6.1.1 Chapter 1

Chapter 1 presents an introduction, and the motivation for the work presented in this thesis. The objectives and structure of the thesis are presented, as well as a thorough literature review of the current technologies which utilise switch-mode power supplies. Renewable systems utilising dc and ac sources are discussed, as are the applications of dc-dc converters in automotive applications. A discussion of several dc-dc converter topologies is presented, as well as the utilisation of coupled-inductors in multi-phase converters. A design example of a 72 kW CCTT IM is presented. Finally, a 1 kW laboratory prototype two-phase interleaved coupled-inductor boost converter is presented. This is the converter on which all experimental testing in the thesis is performed.

6.1.2 Chapter 2

The complete large-signal model of the CL boost converter is presented in Chapter 2. To fully understand the large-signal model, the solutions to the single-phase and two-phase discrete-inductor boost converters are first presented. The phase current waveforms, CCM-DCM mode maps, and sub-modes of operation of all three types of the converter are presented and compared. Each CCM and DCM mode of operation of the CL boost converter is briefly discussed. The boundary conditions between CCM and DCM of the CL boost converter are presented, and a sample analysis of DCM 4 and DCM 9 are also given. These examples can then be extended to all other DCM modes of operation. The modal boundary flowchart presents a flowchart of each CCM and DCM mode of operation, as well as the boundary conditions between each mode. Results from the 1 kW laboratory prototype are presented. These results show the experimental waveforms of all CCM and DCM modes of operation.

6.1.3 Chapter 3

Chapter 3 presented the complete small-signal model of the CL boost converter operating in all CCM and DCM modes of operation. Initially, the method of linearisation is presented, which is then extended to the solutions presented in Chapter 3. The final solution of the small-signal models of the single-phase, two-phase discrete-inductor, and two-phase coupled-inductor boost converter are presented in a unified form which can be applied to all modes of operation. The unified transfer function

models are then derived from these small-signal models for each of the four desired transfer functions; the input voltage-to-output voltage transfer function, the duty cycle-to-output voltage transfer function, the duty cycle-to-inductor current transfer function, and finally, the inductor current-to-output voltage transfer function. The derivation of the small-signal models of the single-phase and two-phase discrete inductor boost converter are derived for both CCM and DCM operation. The small-signal models of the CL boost converter operating in CCM, DCM 4, DCM 1, and DCM 8 are derived. These derivations can then be extended for all other modes of operation. The verification of these small-signal models are presented by comparing the mathematical models to a frequency sweep of a simulated CL boost converter using Matlab®/Simulink. The small-signal models of the 2L and CL converter are then compared to each other.

6.1.4 Chapter 4

In Chapter 4, the transfer functions derived in Chapter 3 are used to design PI controllers for the CL boost converter. Initially, a comparison of the different switch-mode power supply control schemes, such as voltage-mode control and current-mode control, is presented. Through this comparison, Average-Current-Mode Control is chosen as the control scheme to be implemented. The digital design and implementation parameters are presented. The design of PI type controllers for the outer voltage loop and inner current loop of the CL converter operating in CCM is presented. These PI controllers are then implemented into the Altera cyclone III FPGA for experimental testing. Several tests are performed on the converter, such as start-up, steady-state and a load step change. The CCM designed PI controllers are then utilised for DCM operation, the results of which showing a less than optimal performance. PI controllers are then designed for operation in DCM 1 and DCM 9, and the experimental testing is repeated, with the results showing an improvement over the CCM designed controllers operating in DCM.

6.1.5 Chapter 5

Chapter 5 presents the design of Type II compensators for use in the average-current-mode control scheme, replacing PI controllers in the inner current loop. The analogue and digital implementations of Type II compensators are briefly discussed. The design of the Type II compensator for CCM operation is presented, and the controller verified via simulation and experimentation on the 1 kW prototype. As with the PI controllers, the CCM designed controllers are tested during DCM operation, and show instability in

both simulations and experimental testing. Hence, the design of Type II compensators for DCM 3 and DCM 9 operation are presented. These designs can then be extended for all other modes of operation. In order to ensure stability across the full load range of the converter, as well as optimal performance, bumpless control is introduced in an effort to switch controllers, depending on the mode of operation. The bumpless control scheme is initially designed for the PI controllers designed in Chapter 4. After testing, it is evident that a slight bump between the controllers is evident due to the steady-state error present between both controllers. Hence, the implementation of Forced-Output Control is presented. Forced-Output control is utilised for switching between the outputs of the Type II compensators, allowing a bumpless transition between the two, depending on the current mode of operation. Comparisons between the bumpless control scheme and the forced-output control scheme show a much better transient response for the latter.

6.2 Contributions

This thesis presents the complete mathematical model and digital control of a two-phase interleaved coupled-inductor boost converter. Due to the magnetizing effects of the coupled-inductor, operation of the boost converter can vary greatly from that of a single-phase and two-phase discrete inductor boost converter, especially in during DCM. The relationship between the input voltage and output voltage of a CL converter operating in DCM was previously unknown, and the solution difficult to attain. This may deter developers from implementing coupled-inductors into dc-dc converters. Since the benefits of utilizing coupled-inductors have been well documented, the ability to completely predict the large-signal operation of a CL converter is essential if the use of coupled-inductors is to become viable. Hence, chapter 2 presents the complete large-signal solution to the CL boost converter operating in both CCM and DCM. This allows designers and operators to completely predict the large-signal behaviour of a coupled-inductor boost converter, furthering the area of coupled-magnetics in switch mode power supplies. The accuracy of the large-signal model is verified with experimental results from a 1 kW CL boost converter prototype.

In order to fully capitalize on the benefits of a CL converter, optimal closed-loop control is required to ensure the desired voltages and currents are attained, while rejecting any disturbances. While there are several methods of closing the loop of a power converter, one of the more popular methods is the direct design of controllers from a systems small-signal model. Hence, chapter 3 presents the complete small-signal model of the CL boost converter. These models are verified experimentally via a frequency sweep of the 1 kW CL boost converter prototype. The small-signal models presented in chapter 3 will help developers design suitable controllers for CL converters, for a wide range of applications.

With the large-signal and small-signal models derived, the design of closed-loop controllers in the form of PI controllers and type-II compensators are developed. The controllers are developed for two reasons. The first is further verification of the large- and small-signal models. By developing optimal closed-loop controllers designed solely on the models presented in chapter 2 and chapter 3, designers can be comfortable in knowing that the mathematical models presented are not only accurate, but also beneficial.

Finally, due to the varying dynamics between the different modes of operation of a CL boost converter, especially between CCM and DCM, Forced-Output Control is

developed to allow the converter to switch between controllers mid-operation. This method of control is extremely beneficial, due to the fact that it is now possible to implement optimal control for all operating points of a dc-dc converter, allowing the full-load range of a converter to be utilised to the best of its abilities.

6.3 Future Work

Switch-mode power supplies and more specifically, dc-dc converters are used in a large range of applications. The incorporation of a coupled-inductor into a dc-dc converter has been shown to improve the performance of the converter, in terms of both efficiency and size. The body of work presented in this thesis now gives designers and operators the ability to predict the large-signal, and small-signal characteristics of a CL converter. However, due to the complexity of design and implementation, the technology is still in its infancy in terms of applications in industry, and much more work may need to be done to fully utilise coupled-inductors into power converters. For example, the efficiency of each mode of operation should be calculated and verified with experimental results. A comparison of the efficiencies of each mode should also be undertaken. While the coupled-inductor has been shown to have greater efficiency at lighter loads, it has yet to be determined whether a specific DCM mode operates at consistently higher efficiencies, and if so, what are the more efficient modes.

While the main focus of this thesis was the analysis of a coupled-inductor boost converter, a similar analysis of a CL buck converter is presented in the Appendix. However, there is currently no experimental validation of the theory presented. It is the aim of the author to modify the 1 kW boost converter prototype in order to implement bidirectional operation, in which a CL buck converter is a part of. With this modification, experimental validation of the theory presented for the CL boost converter can be presented.

One of the main shortcomings of this body of work is the fact that the solutions presented only apply to two-phase interleaved converters, when dc-dc converters can have any number of phases. Another restriction to the work presented is the fact that the coupled-inductors are inversely coupled. Possible future work may include general large-signal, and small-signal models which can easily characterise dc-dc converters with any number of phases, and for any winding arrangement.

Finally, with the ability to predict the operation of coupled-inductor boost converters comes the opportunity to implement such a scheme into PFC applications. PFC boost converters are one of the most common converter schemes in the area of power electronics. Implementing a coupled-inductor into a PFC boost can give many possible advantages, such as reduced size and weight of the converter, and reduced THD, due to the added ability of the coupled-inductor to reduce common mode noise. Presented with the mathematical modelling of the CL converter is the introduction of the FOC scheme.

PFC boost converters operating in CCM must inherently enter DCM operation at some point, due to the input current being ac. Most CCM PFC boost converters use a single controller, which is designed for CCM operation. With the ability to quickly and smoothly switch controllers via FOC, a controller for DCM can also be incorporated into the PFC boost converter, giving optimal performance at any point of the input sine wave.

7 APPENDIX

Appendix A presents the large-signal, and small-signal analysis of a two-phase interleaved coupled-inductor buck converter.

Appendix B presents the various expressions needed to solve all CCM and DCM modes of operation of the two-phase interleaved coupled-inductor boost converter. Also presented in Appendix B is the Matlab® code used to solve for the α, β, γ, and δ coefficients of the small-signal models.

Appendix C presents the results of the implementation of the closed-loop PI controller for all CCM and DCM modes of operation.

Appendix A.
Buck Converter Analysis

Boost converters are often implemented into bidirectional converters to step-up the voltage one direction, while a buck converter steps the voltage back down when the flow of power is reversed [2.31]. For example, the regenerative braking system in modern electric and hybrid cars use a bidirectional converter to supply power to the wheels when driving via boosting, and reverse the flow of power back into the battery when braking via bucking [2.30]. This system is presented in Figure 7.1. In Figure 2.40, V_{LV} and C_{LV} are the low voltage side voltage and capacitance, while V_{HV} and C_{HV} are the high voltage side voltage and capacitance. To use a coupled-inductor in a bidirectional converter, the effects of the coupling must also be examined in a buck converter.

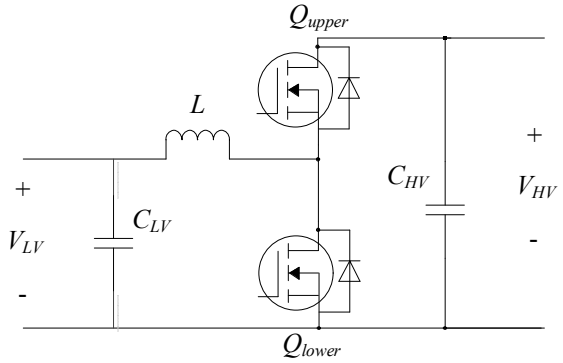


Figure 7.1. Bidirectional dc-dc converter with dc motor and battery.

7.1.1 A.1 1L Buck Converter Large-Signal Model

To properly analyse a CL buck converter, the 1L and 2L buck converters must first be understood. The 1L buck converter CCM-DCM mode map is presented in Figure 7.2. The *x*-axis details the output current of the buck converter, normalised to the maximum output boundary current of the converter. This occurs at a duty cycle of 1, and is found as

$$I_{oB,Max} = \frac{V_{in} T_s}{2L} \tag{7.1}$$

Similar to the 1L boost converter, the 1L buck converter has two CCM modes, 1L CCM 1 and 1L CCM 2. The gain of the converter when operating in these modes is

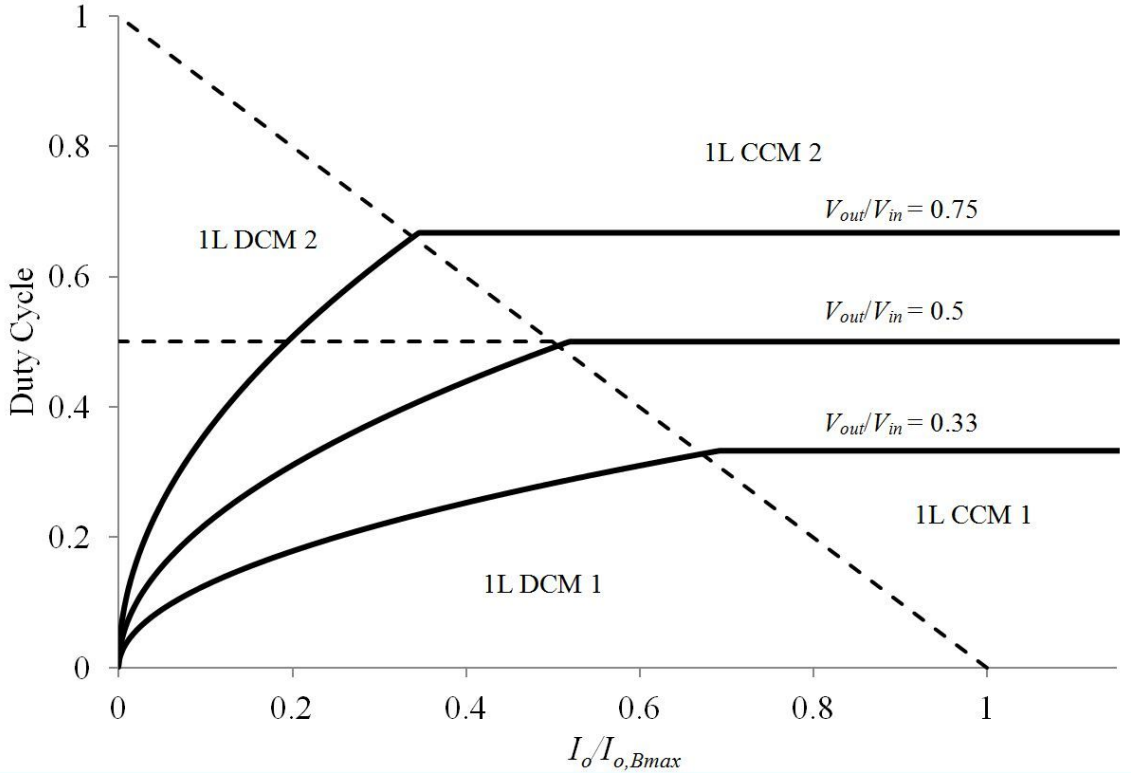


Figure 7.2. Output current CCM-DCM mode map for 1L buck converter.

$$\frac{V_{out}}{V_{in}} = D \tag{7.2}$$

As the current in the converter drops, the system begins to enter one of two DCM modes, 1L DCM 1, which occurs at a duty cycle less than 0.5, and 1L DCM 2, which occurs at a duty cycle greater than 0.5. The gain of the converter when operating in these modes is

$$\frac{V_{out}}{V_{in}} = \frac{D^2}{D^2 + \frac{L}{2R_{out}T_s}} \tag{7.3}$$

7.1.2 A.2 2L Buck Converter Large-Signal Model

The 2L CCM-DCM mode map is presented in Figure 7.3. The *x*-axis represents the converter output current normalised to the maximum output boundary current, which is found as

$$I_{oB,Max} = \frac{V_{in}T_s}{4L} \tag{7.4}$$

Similar to the 2L boost converter, there are two CCM modes of operation, 2L CCM 1, which occurs at a duty cycle less than 0.5, and 2L CCM 2 which occurs at a duty cycle greater than 0.5. The gain of the converter in these modes is

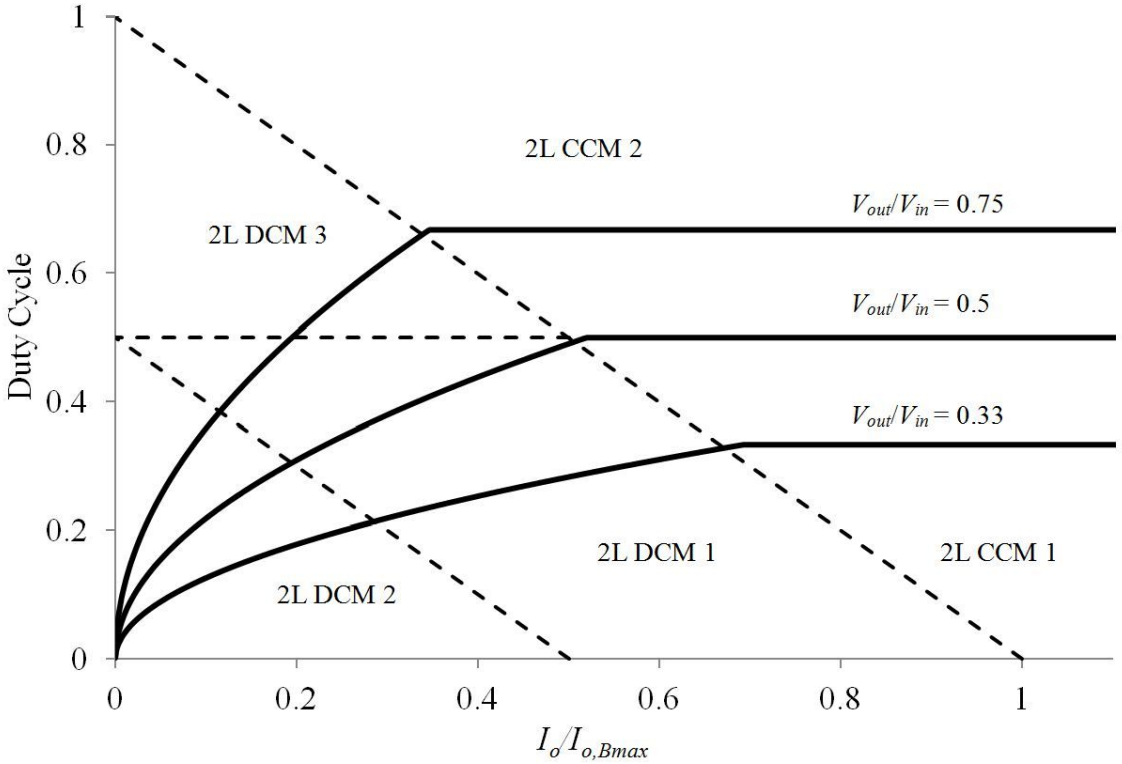


Figure 7.3. Output current CCM-DCM mode map for 2L buck converter.

$$\frac{V_{out}}{V_{in}} = D \tag{7.5}$$

As the current drops, the system will enter DCM. There are three DCM modes present in a 2L buck converter. 2L DCM 1 and 2L DCM 3 occur when the duty cycle is less than and greater than 0.5 respectively. In both these modes, the input current does not reach zero. The final DCM mode, 2L DCM 3 occurs when the input current reaches zero in every cycle. The converter cannot enter 2L DCM 3 if the duty cycle ii 0.5 or greater. The gain of the system when operating in all three DCM modes is

$$\frac{V_{out}}{V_{in}} = \frac{D^2}{D^2 + \frac{L}{4R_{out}T_s}} \tag{7.6}$$

Once again, the difference between the DCM gain of the 1L and 2L buck is a factor of two represented by the fact that the inductor current is now half the value.

7.1.3 A.3 CL Buck Converter Large-Signal Model

The CCM-DCM mode map of the CL buck converter is presented in Figure 7.4. Similar to the CL boost converter, there are a total of ten modes of operation; two in CCM and eight in DCM. The waveforms of each CCM and DCM mode of the CL buck converter are identical to the CL boost converter waveforms presented in Figure 2.12 to Figure 2.14. Hence, for simplicity, each mode has been given the same name as their boost converter counterpart.

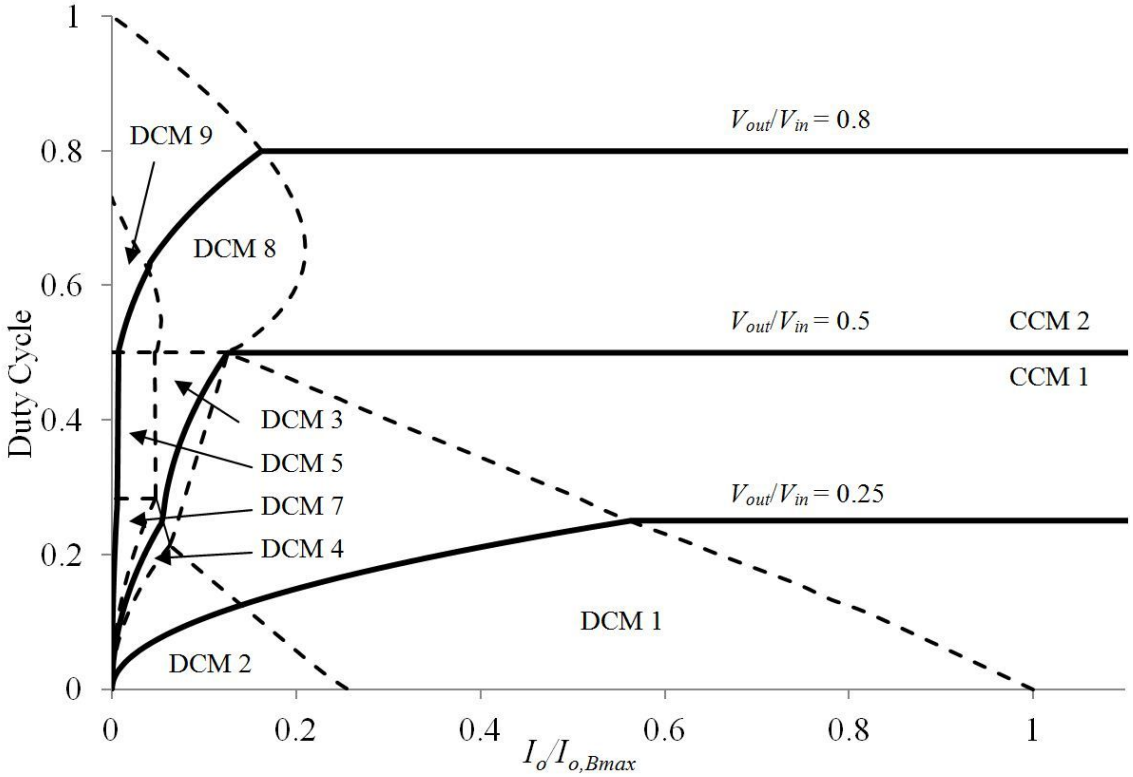


Figure 7.4. Output current CCM-DCM mode map for CL buck converter.

Once again, the *x*-axis represents the converter output current normalised to the maximum output boundary current. The formula for the maximum output boundary current for the CL buck converter is

$$I_{oB,Max} = \frac{V_{out}T_s(L_{Lk}+L_m)}{L_{Lk}(L_{Lk}+2L_m)} \tag{7.7}$$

which occurs at a duty cycle of $D = 0$, as can be seen in Figure 7.4. The gain of the converter when operating in both CCM modes of operation is

$$\frac{V_{out}}{V_{in}} = D \tag{7.8}$$

As with the CL boost converter, the gain of each DCM mode is unique. The ripple currents of the CL buck converter when operating in DCM are given in Table 7.1.

Table 7.1. Peak-to-peak ripple currents for the input, magnetizing and phase currents of a CL buck converter when operating in CCM.

CCM Mode	ΔIout(p-p)	ΔIm(p-p)	ΔIL(p-p)
CCM 1 (D < 0.5)	$\frac{(V_{in}-V_{out})DT_s}{L_{lk}}$	$\frac{V_{in}DT_s}{L_{Lk}+2L_m}$	$\frac{\Delta I_{out(p-p)}}{2}+\frac{\Delta I_{m(p-p)}}{2}$
CCM 2 (D > 0.5)	$\frac{(2V_{out}-V_{in})(1-D)T_s}{L_{Lk}}$	$\frac{V_{in}(1-D)T_s}{L_{Lk}+2L_m}$	$\frac{\Delta I_{out(p-p)}}{2}+\frac{\Delta I_{m(p-p)}}{2}$

7.1.4 A.4 CL Buck Converter Small-Signal Model

The analysis presented in section 3.4 can easily be applied to a CL buck converter to find its small-signal models for all CCM and DCM modes also. The characteristic equations for the CL buck converter operating in CCM are

$$L_{Lk}\frac{dI_{L1}}{dt} = V_{in}D - V_{out} - V_{T1} \tag{7.9}$$

$$C_{out}\frac{dV_{out}}{dt} = I_{L1} - \frac{V_{out}}{R_{out}} \tag{7.10}$$

while the characteristic equations for all DCM modes are

$$L_{Lk}\frac{dI_{L1}}{dt} = V_{in}D - V_{out}(D + D_{off}) - V_{T1} \tag{7.11}$$

$$C_{out}\frac{dV_{out}}{dt} = I_{L1} - \frac{V_{out}}{R_{out}} \tag{7.12}$$

The expressions for V_{T1} for the CL Buck converter in CCM, DCM 1, DCM 4 and DCM 8, respectively, are

$$V_{T1} = 0 \tag{7.13}$$

$$V_{T1} = L_m\frac{V_{out}(1 - D - D_{off})}{L_{Lk} + L_m} \tag{7.14}$$

$$V_{T1} = 0 \tag{7.15}$$

$$V_{T1} = L_m\frac{(V_{in} - V_{out})(1 - D - D_{off})}{L_{Lk} + L_m} \tag{7.16}$$

As with the boost converter, the expression for D_{off} is derived. It is then inserted into the characteristics equation, along with V_{T1}. The results are linearised, and the small-signal models of the CL buck converter are found as

$$L\frac{d\tilde{i}_{L1}(t)}{dt} = \alpha_1\tilde{v}_{in}(t) + \beta_1\tilde{v}_{out}(t) + \gamma_1\tilde{d}(t) + \delta_1\tilde{i}_{L1}(t) \tag{7.17}$$

$$C_{out}\frac{d\tilde{v}_{out}(t)}{dt} = \alpha_2\tilde{v}_{in}(t) + \beta_2\tilde{v}_{out}(t) + \gamma_2\tilde{d}(t) + \delta_2\tilde{i}_{L1}(t) \tag{7.18}$$

As with the CL boost converter, the expressions for the α, β, γ, and δ coefficients are too large to present here. However, the Matlab® code used to solve for the coefficients is supplied in the appendix. Once again, it is evident that the magnetising inductance plays a large role in the small-signal models.

A. 5 CL Buck Converter Small-Signal Model

The analysis presented in Section 3.5 can easily be applied to a CL buck converter to find its small-signal models for all CCM and DCM modes also. The characteristic equations for the CL buck converter operating in CCM are

$$L_{Lk}\frac{dI_{L1}}{dt} = V_{in}D - V_{out} - V_{T1} \tag{7.19}$$

$$C_{out}\frac{dV_{out}}{dt} = I_{L1} - \frac{V_{out}}{R_{out}} \tag{7.20}$$

while the characteristic equations for all DCM modes are

$$L_{Lk}\frac{dI_{L1}}{dt} = V_{in}D - V_{out}(D + D_{off}) - V_{T1} \tag{7.21}$$

$$C_{out}\frac{dV_{out}}{dt} = I_{L1} - \frac{V_{out}}{R_{out}} \tag{7.22}$$

The expressions for V_{T1} for the CL Buck converter in CCM, DCM 1, DCM 4 and DCM 8, respectively, are

$$V_{T1} = 0 \tag{7.23}$$

$$V_{T1} = L_m\frac{V_{out}(1 - D - D_{off})}{L_{Lk} + L_m} \tag{7.24}$$

$$V_{T1} = 0 \tag{7.25}$$

$$V_{T1} = L_m\frac{(V_{in} - V_{out})(1 - D - D_{off})}{L_{Lk} + L_m} \tag{7.26}$$

As with the boost converter, the expression for D_{off} is derived. It is then inserted into the characteristics equation, along with V_{T1}. The results are linearised, and the small-signal models of the CL buck converter are found as

$$L\frac{d\tilde{i}_{L1}(t)}{dt} = \alpha_1\tilde{v}_{in}(t) + \beta_1\tilde{v}_{out}(t) + \gamma_1\tilde{d}(t) + \delta_1\tilde{i}_{L1}(t) \tag{7.27}$$

$$C_{out}\frac{d\tilde{v}_{out}(t)}{dt} = \alpha_2\tilde{v}_{in}(t) + \beta_2\tilde{v}_{out}(t) + \gamma_2\tilde{d}(t) + \delta_2\tilde{i}_{L1}(t) \tag{7.28}$$

As with the CL boost converter, the expressions for the α, β, γ, and δ coefficients are too large to present here. However, the Matlab® code used to solve for the coefficients is supplied in the appendix. Once again, it is evident that the magnetising inductance plays a large role in the small-signal models.

Appendix B

7.1.5 CCM Equations

Simultaneous Equation 1 needed to solve for D and D_{off}

$$V_{in} - (1-D)V_{out} = 0 \tag{A.1}$$

Simultaneous Equation 2 needed to solve for D and D_{off}

N/A

Duty Cycle

$$D = 1 - \frac{V_{in}}{V_{out}} \tag{A.2}$$

Off-Time

$$D_{off} = 1 - D \tag{A.3}$$

Non-linearised Equations

$$L_{Lk}\frac{dI_{L1}}{dt} = V_i(D + D_o) - V_o D_o - V_{T1} \tag{A.4}$$

$$C_o\frac{dV_{out}}{dt} = 2I_{L1} - 2I_{S1} - \frac{V_{out}}{R_{out}} \tag{A.5}$$

Switch current

$$I_{S1} = DI_{L1} \tag{A.6}$$

Voltage drop across the magnetising inductance

$$V_{T1} = 0 \tag{A.7}$$

7.1.6 DCM 1 Equations

Simultaneous Equation 1 needed to solve for D and D_{off}

$$V_{in}(D_1 + D_{off}) - V_{out}D_{off} - \frac{L_m(V_{out} - V_{in})(D1 + D_{off} - 1)}{(L_{Lk} + L_m)} = 0 \tag{A.8}$$

Simultaneous Equation 2 needed to solve for D and D_{off}

$$I_{L1} - \frac{T_s((4V_{in} - 2V_{out})D_1^{\,2} + (4V_{in} - 2V_{out})D_{off}D_1 + (2V_{in} - 2V_{out})D_{off} + V_{out} - V_{in})}{4L_{Lk}} - \ldots$$
$$\ldots \frac{(V_{out}D_1T_s)}{4(L_{Lk} + 2L_m)} - \frac{T_s(2D_1 + 1)(V_{out} - V_{in})(D1 + D_{off} - 1)}{4(L_{Lk} + L_m)} = 0 \tag{A.9}$$

Duty Cycle

$$D = \frac{\sqrt{2L_{Lk}V_oI_{L1}T(L_{Lk} + 2L_m)(V_o - V)(L_{Lk}V - L_mV_o + 2L_mV)}}{V_oT(L_{Lk}V - L_m(V_o - 2V_i))} \tag{A.10}$$

Off-Time

$$D_o = -\frac{L_{Lk}}{2(L_{Lk} + 2L_m)} - \frac{4L_{Lk}I_{L1} - V_oT + V_iT + 2V_oD^2T - 4V_iD^2T}{2T(V_o - V_i + V_oD - 2V_iD)} - \ldots$$
$$\ldots \frac{L_{Lk}(4L_{Lk}I_{L1} - V_oDT)(2D + 1)(V_o - V_i)}{2T(L_{Lk}V_o - L_{Lk}V_i + L_m(2V_o - 2V_i + 2V_oD - 4V_iD) - 2L_{Lk}V_iD)(V_o - V_i + V_oD - 2V_iD)} \tag{A.11}$$

Non-linearised Equations

$$L_{Lk}\frac{dI_{L1}}{dt} = V_i(D + D_o) - V_oD_o - V_{T1} \tag{A.12}$$

$$C_o \frac{dV_{out}}{dt} = 2I_{L1} - 2I_{S1} - \frac{V_{out}}{R_{out}} \tag{A.13}$$

Switch current

$$I_{S1} = \frac{V_o D^2 T}{4(L_{Lk} + 2L_m)} - \frac{D^2 T(V_o - 2V_i)}{4L_{Lk}} \tag{A.14}$$

Voltage drop across the magnetising inductance

$$V_{T1} = \frac{(1 - D - D_o)(V_i - V_o)L_m}{(L_{Lk} + L_m)} \tag{A.15}$$

7.1.7 DCM 2 Equations

Simultaneous Equation 1 needed to solve for D and D_{off}

$$V_i(D+D_o)-V_oD_o-\frac{L_mV_oD(L_{Lk}+L_m)(V_i-V_o)}{(L_{Lk}+2L_m)(V_o-V_i)(L_{Lk}+L_m)}=0 \tag{A.16}$$

Simultaneous Equation 2 needed to solve for D and D_{off}

$$I_{L1}-\frac{2T(V_o-V_i)(D+D_3-D_o)^2-4V_iD^2T+V_oTD(D_3-D_o+3D)}{8L_{Lk}}+\ldots \\ \ldots\frac{V_oTD(D-D_3T-3D_o)}{8(L_{Lk}+2L_m)}=0 \tag{A.17}$$

Duty Cycle

$$D=\sqrt{\frac{L_{Lk}(L_{Lk}+2L_m)(2R_oI_{L1}+V_o)}{R_oT(L_{Lk}V_i-L_mV_o+2L_mV_i)}} \tag{A.18}$$

Off-Time

$$Do=\frac{\sqrt{-\frac{L_{Lk}V_oT(L_{Lk}+2L_m)((9V_o^2-24V_oV_i-2R_oI_{L1}V_o+16V_i^2)L_m^2+\ldots}{\ldots(4L_{Lk}Vo^2-20L_{Lk}VoVi+16L_{Lk}Vi^2)L_m+4L_{Lk}^2V_i^2-4V_oL_{Lk}^2V_i)}{L_{Lk}R_oV_i-L_mR_oV_o+2L_mR_oV_i}}}{T(L_{Lk}+2L_m)(V_o-V_i)}-\ldots \\ \ldots\frac{(L_{Lk}V_i-2L_mV_o+2L_mV_i)\sqrt{\frac{L_{Lk}(L_{Lk}+2L_m)(V_o-2R_oI_{L1})}{R_oT(L_mV_o-V_i(L_{Lk}+2L_m))}}}{(L_{Lk}+2L_m)(V_o-V_i)}; \tag{A.19}$$

$$D_3 = \frac{(V_o D(L_{Lk} + L_m))}{(L_{Lk} + 2L_m)(V_o - V_i)}$$

Non-linearised Equations

$$L_{Lk} \frac{dI_{L1}}{dt} = V_i(D + D_o) - V_o D_o - V_{T1} \tag{A.20}$$

$$C_o \frac{dV_{out}}{dt} = 2I_{L1} - 2I_{S1} - \frac{V_{out}}{R_{out}} \tag{A.21}$$

Switch current

$$I_{S1} = 0.5D\left(\frac{V_o DT}{2(L_{Lk} + 2L_m)} - \frac{(V_o - 2V_i)DT}{2L_{Lk}} \right) \tag{A.22}$$

Voltage drop across the magnetising inductance

$$V_{T1} = \frac{L_m V_o D(L_{Lk} + L_m)(V_i - V_o)}{(L_{Lk} + 2L_m)(V_o - V_i)(L_{Lk} + L_m)} \tag{A.23}$$

7.1.8 DCM 3 Equations

Simultaneous Equation 1 needed to solve for D and D_{off}

$$V_i(D+D_o)-V_oD_o-\frac{L_mV_i(0.5-D_o)+(V_i-V_o)(0.5-D)}{L_{Lk}+L_m}=0 \tag{A.24}$$

Simultaneous Equation 2 needed to solve for D and D_{off}

$$I_{L1}+\frac{(T(V_iD-Vi+V_oD_o+V_iD_o-2V_oDD_o))}{4(L_{Lk}+L_m)}-\ldots$$
$$\ldots\frac{V_oT(2D+2D_o-1)}{8(L_{Lk}+2L_m)}+\frac{T(V_o-2V_i)(2D+2D_o-1)}{8L_{Lk}}=0 \tag{A.25}$$

Duty Cycle

$$D=\frac{L_m}{2(L_{Lk}+2L_m)}+\ldots$$
$$\ldots\frac{\sqrt{V_oT(L_{Lk}+L_m)(L_{Lk}V_i-L_mV_o+2L_mV_i)(8I_{L1}L_{Lk}{}^2+32I_{L1}L_{Lk}L_m+32I_{L1}L_m{}^2-V_oTL_m)(L_{Lk}V_o+L_mV_o-L_{Lk}V_i-2L_mV_i)}}{2V_oT(L_{Lk}+2L_m)(L_{Lk}V_i-L_mV_o+2L_mV_i)} \tag{A.26}$$

Off-Time

$$D_{off}=\frac{L_m}{2(L_{Lk}+2L_m)}+\ldots$$
$$\ldots\frac{\sqrt{V_oT(L_{Lk}+L_m)(L_{Lk}V_i-L_mV_o+2L_mV_i)(8I_{L1}L_{Lk}{}^2+32I_{L1}L_{Lk}L_m+32I_{L1}L_m{}^2-V_oTL_m)(L_{Lk}V_o+L_mV_o-L_{Lk}V_i-2L_mV_i)}}{2V_oT(L_{Lk}+2L_m)((L_{Lk}V_o+L_mV_o-L_{Lk}V_i-2L_mV_i))} \tag{A.27}$$

Non-linearised Equations

$$L_{Lk}\frac{dI_{L1}}{dt} = V_i(D + D_o) - V_o D_o - V_{T1} \tag{A.28}$$

$$C_o\frac{dV_{out}}{dt} = 2I_{L1} - 2I_{S1} - \frac{V_{out}}{R_{out}} \tag{A.29}$$

Switch current

$$I_{S1} = 0.5D\left(\frac{V_o DT}{2(L_{Lk} + 2L_m)} - \frac{(V_o - 2V_i)DT}{2L_{Lk}}\right) \tag{A.30}$$

Voltage drop across the magnetising inductance

$$V_{T1} = \frac{L_m V_i(0.5 - D_o) + (V_i - V_o)(0.5 - D)}{L_{Lk} + L_m} \tag{A.31}$$

7.1.9 DCM 4 Equations

Simultaneous Equation 1 needed to solve for D and D_{off}

$$V_i(D+D_o)-V_oD_o=0 \tag{A.32}$$

Simultaneous Equation 2 needed to solve for D and D_{off}

$$\frac{V_iDT(D+D_o)}{2(L_{Lk}+L_m)}-I_{L1}=0 \tag{A.33}$$

Duty Cycle

$$D=\frac{\sqrt{2V_oV_iI_{L1}T(V_o-V_i)(L_{Lk}+L_m)}}{V_oV_iT} \tag{A.34}$$

Off-Time

$$D_{off}=\frac{2L_{Lk}I_{L1}+2L_mI_{L1}-V_iTD^2}{V_iDT} \tag{A.35}$$

Non-linearised Equations

$$L_{Lk}\frac{dI_{L1}}{dt}=V_i(D+D_o)-V_oD_o-V_{T1} \tag{A.36}$$

$$C_o\frac{dV_{out}}{dt}=2I_{L1}-2I_{S1}-\frac{V_{out}}{R_{out}} \tag{A.37}$$

Switch current

$$I_{S1} = \frac{0.5 V_i D^2 T}{L_{Lk} + L_m} \tag{A.38}$$

Voltage drop across the magnetising inductance

$$V_{T1} = 0 \tag{A.39}$$

7.1.10 DCM 7 Equations

Simultaneous Equation 1 needed to solve for D and D_{off}

$$V_i(D+D_o)-\frac{V_o(D_o-D_3)}{2}-\frac{L_mV_iD}{L_{Lk}+L_m}-\frac{L_mV_iD_3}{L_{Lk}+L_m}=0 \tag{A.40}$$

Simultaneous Equation 2 needed to solve for D and D_{off}

$$I_{L1}+\frac{T(V_o-2V_i)(D_3-D_o)}{2L_{Lk}}-\frac{V_oT(D_3-D_o)}{4(L_{Lk}+2L_m)}-\frac{V_iD_1^2T}{2(L_{Lk}+L_m)}+\frac{V_iD_3^2T}{2(L_{Lk}+L_m)}+\frac{V_iD_1T(D_3-D_o)}{4(L_{Lk}+L_m)}=0 \tag{A.41}$$

Duty Cycle

$$D=\frac{(L_{Lk}+L_m)\sqrt{2L_{Lk}V_oV_iI_{L1}T(L_{Lk}+2L_m)(L_{Lk}V_o+L_mV_o-L_{Lk}V_i-2L_mV_i)}}{L_{Lk}V_oV_iT(L_{Lk}+2L_m)} \tag{A.42}$$

Off-Time

Equation for Doff is too long. Solve Simultaneous Equations above to find Doff.

$$D_3=D_o-\frac{2L_{Lk}V_iD_o(L_{Lk}+2L_m)}{L_m(L_{Lk}V_o+L_{Lk}V_i)+L_{Lk}V_i+L_m(V_o-2V_i)}; \tag{A.43}$$

Non-linearised Equations

$$L_{Lk}\frac{dI_{L1}}{dt}=V_i(D+D_o)-\frac{V_o(D_o-D_3)}{2}-\frac{L_mV_iD}{L_{Lk}+L_m}-\frac{L_mV_iD_3}{L_{Lk}+L_m} \tag{A.44}$$

$$C_o\frac{dV_{out}}{dt}=2I_{L1}-2I_{S1}-\frac{V_{out}}{R_{out}} \tag{A.45}$$

Switch current

$$I_{S1} = \frac{V_i D^2 T}{2(L_{Lk} + L_m)} - (\frac{V_i D_3{}^2 T}{2(L_{Lk} + L_m)}) + \frac{T(D_3 - D_o)^2 (L_{Lk} V_i - L_m V_o + 2L_m V_i)}{8L_{Lk}(L_{Lk} + 2L_m)} \quad \text{(A.46)}$$

Voltage drop across the magnetising inductance

$$V_{T1} = \frac{L_m V_i D}{L_{Lk} + L_m} + \frac{L_m V_i D_3}{L_{Lk} + L_m} \quad \text{(A.47)}$$

7.1.11 DCM 8 Equations

Simultaneous Equation 1 needed to solve for D and D_{off}

$$V_i(D+D_o)-V_oD_o-\frac{L_m(1-D-D_o)V_i}{L_{Lk}+L_m}=0 \tag{A.48}$$

Simultaneous Equation 2 needed to solve for D and D_{off}

$$I_{L1}+\frac{T(2V_iD+V_oD_o-2V_iD_o-4V_iD^2-2V_oD_o{}^2+4V_iD_o{}^2)}{4L_{Lk}}-\frac{V_oD_oT}{4(L_{Lk}+2L_m)}-\frac{V_iT(D-D^2+D_o{}^2-D_o)}{2(L_{Lk}+L_m)}=0 \tag{A.49}$$

Duty Cycle

$$D=\frac{L_m}{L_{Lk}+2L_m}+\frac{\sqrt{2L_{Lk}V_oV_iI_{L1}T(L_{Lk}+2L_m)^3(L_{Lk}V_o+L_mV_o-L_{Lk}V_i-2L_mV_i)}}{V_oV_iT(L_{Lk}+2L_m)^2} \tag{A.50}$$

Off-Time

$$D_{off}=\frac{2D_x+L_m{}^2T(V_o-2V_i)+L_{Lk}L_mT(V_o-V_i)}{2T((L_{Lk}{}^2+3L_{Lk}L_m+2L_m{}^2)V_o-(L_{Lk}{}^2+4L_{Lk}L_m+4L_m{}^2)V_i)} \tag{A.51}$$

$$D_x=\sqrt{\frac{\begin{array}{c}T((L_{Lk}+L_m)V_o-(L_{Lk}+2L_m)V_i)((-4L_{Lk}{}^3-24L_{Lk}{}^2L_m-48L_{Lk}L_m{}^2-32L_m{}^3)V_iD^2+\ldots\\ \ldots(4L_{Lk}{}^2L_m+16L_{Lk}L_m{}^2+16L_m{}^3)V_iD+(L_m{}^3+L_{Lk}L_m{}^2)V_o-2V_iL_m{}^3-L_{Lk}V_iL_m{}^2)T+(8L_{Lk}{}^4+40L_{Lk}{}^3L_m+64L_{Lk}{}^2L_m{}^2+32L_{Lk}L_m{}^3)I_{L1}\end{array}}{4}} \tag{A.52}$$

Non-linearised Equations

$$L_{Lk}\frac{dI_{L1}}{dt}=V_i(D+D_o)-V_oD_o-V_{T1} \tag{A.53}$$

$$C_o \frac{dV_{out}}{dt} = 2I_{L1} - 2I_{S1} - \frac{V_{out}}{R_{out}} \tag{A.54}$$

Switch current

$$I_{S1} = \frac{V_i T(-D^2 + D + D_o{}^2 - D_o)}{2(L_{Lk} + L_m)} - \ldots$$
$$\ldots \frac{T(2V_i D + V_o D_o - 2V_i D_o - 4V_i D^2 - V_o D_o D_o{}^2 + 2V_i D_o{}^2)}{4L_{Lk}} + \frac{V_o D_o T(1 - D_o)}{4(L_{Lk} + 2L_m)} \tag{A.55}$$

Voltage drop across the magnetising inductance

$$V_{T1} = \frac{L_m(1 - D - D_o)V_i}{L_{Lk} + L_m} \tag{A.56}$$

7.1.12 DCM 9 Equations

Simultaneous Equation 1 needed to solve for D and D_{off}

$$V_i(D+D_o)-V_oD_o-\frac{V_iL_m(1-D-D_o)}{L_{Lk}+L_m}=0 \tag{A.57}$$

Simultaneous Equation 2 needed to solve for D and D_{off}

$$I_{L1}+\frac{T(2V_iD+V_oD_o-2V_iD_o-4V_iD^2-2V_oD_o{}^2+4V_iD_o{}^2)}{4L_{Lk}}-\frac{V_oD_oT}{4(L_{Lk}+2L_m)}+\frac{V_iT(D-D_o)(D+D_o-1)}{2(L_{Lk}+L_m)}=0 \tag{A.58}$$

Duty Cycle

$$D=\frac{L_m}{L_{Lk}+2L_m}+\frac{\sqrt{2L_{Lk}V_oV_iI_{L1}T(L_{Lk}+2L_m)^3(L_{Lk}V_o+L_mV_o-L_{Lk}V_i-2L_mV_i)}}{V_oV_iT(L_{Lk}+2L_m)^2} \tag{A.59}$$

Off-Time

$$D_{off}=\frac{\frac{L_{Lk}L_m(V_o-V_i)}{2}+\frac{L_m{}^2V_o}{2}-L_m{}^2V_i}{(L_{Lk}+2L_m)(L_{Lk}V_o+L_mV_o-L_{Lk}V_i-2L_mV_i)}-D_x$$

$$D_x=\frac{\sqrt{T(L_{Lk}V_o+L_mV_o-L_{Lk}V_i-2L_mVi)(\frac{8L_{Lk}{}^4V_iI_{L1}-D_y+64L_{Lk}L_m{}^3V_iI_{L1}+48L_{Lk}{}^3L_mV_iI_{L1}+96L_{Lk}{}^2L_m{}^2V_iI_{L1}}{Vo}+\ldots}}{2T(L_{Lk}+2L_m)(L_{Lk}V_o+L_mV_o-L_{Lk}V_i-2L_mV_i)} \tag{A.60}$$

$$\ldots L_m{}^2T(L_{Lk}V_o+L_mV_o-L_{Lk}V_i-2L_mV_i))$$

$$D_y=4L_m\sqrt{2L_{Lk}V_oV_iI_{L1}T(L_{Lk}+2L_m)^3(L_{Lk}V_o+L_mV_o-L_{Lk}V_i-2L_mV_i)} \tag{A.61}$$

Non-linearised Equations

$$L_{Lk}\frac{dI_{L1}}{dt} = V_i(D + D_o) - V_o D_o - V_{T1} \tag{A.62}$$

$$C_o\frac{dV_{out}}{dt} = 2I_{L1} - 2I_{S1} - \frac{V_{out}}{R_{out}} \tag{A.63}$$

Switch current

$$I_{S1} = \frac{V_i T(D - D^2 + D_o{}^2 - D_o)}{2L_{Lk} + 2L_m} - \ldots$$
$$\ldots\frac{T(2V_m D + V_o D_o - 2V_m D_o - 4V_m D^2 - V_o D_o{}^2 + 2V_m D_o{}^2)}{4L_{Lk}} - \frac{V_o D_o T(D_o - 1)}{4L_{Lk} + 8L_m} \tag{A.64}$$

Voltage drop across the magnetising inductance

$$V_{T1} = \frac{V_i L_m(1 - D - D_o)}{L_{Lk} + L_m} \tag{A.65}$$

7.1.13 Matlab® code for small-signal model coefficients α, β, γ, and δ

The expressions for Doff, IS1 and VT1 are first declared in Matlab®. For example, when solving DCM 1, equations (A.11), (A.14), and (A.15) are expressed as

```
Doff = - LLk/(2*(LLk + 2*Lm)) - ((Vi - Vo + 2*Vo*D^2 - 4*Vi*D^2)*ts +
4*LLk*IL1)/(2*ts*(Vo-... Vi + Vo*D - 2*Vi*D)) - (LLk*(4*LLk*IL1 -
Vo*D*ts)*(2*D + 1)*(Vo - Vi))/(2*ts*(LLk*Vo-… LLk*Vi + Lm*(2*Vo - 2*Vi +
2*Vo*D - 4*Vi*D) - 2*LLk*Vi*D)*(Vo - Vi + Vo*D - 2*Vi*D));
Is1 = (Vo*D^2*ts)/(4*(LLk + 2*Lm)) - (D^2*ts*(Vo - 2*Vi))/(4*LLk);
Dil1 = (Vi*(D+Doff) - Vo*(Doff) - VT1;
```

The Non-linearised equations given in (A.12) and (A.13) are expressed in Matlab® as

```
Dil = (Vi*(D+Doff) - Vo*(Doff) – VT1;

Dvo = 2*IL1 - 2*Is1 - Vo/Ro;
```

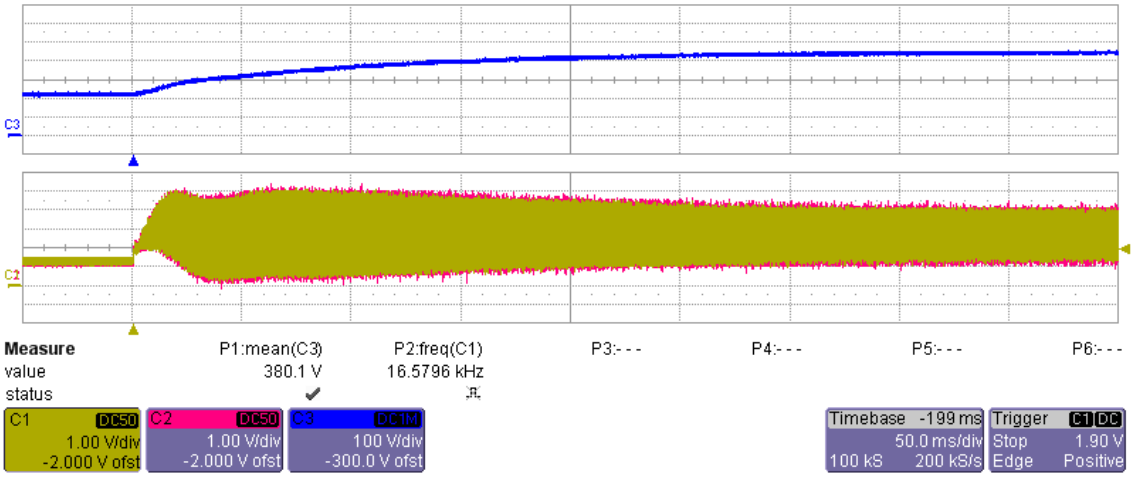
Finally, the α, β, γ, and δ coefficients are solved via the differentiation command, "`diff`", in Matlab®, and simplified using the simplify command, "`simplify`", i.e.

```
al1 = simplify(diff(Dil7,Vi));      = α1
be1 = simplify(diff(Dil7,Vo));      = β1
ga1 = simplify(diff(Dil7,D));       = γ1
de1 = simplify(diff(Dil7,IL1));     = δ1
al2 = simplify(diff(Dvo7,Vi));      = α2
be2 = simplify(diff(Dvo7,Vo));      = β2
ga2 = simplify(diff(Dvo7,D));       = γ2
de2 = simplify(diff(Dvo7,IL1));     = δ2
```

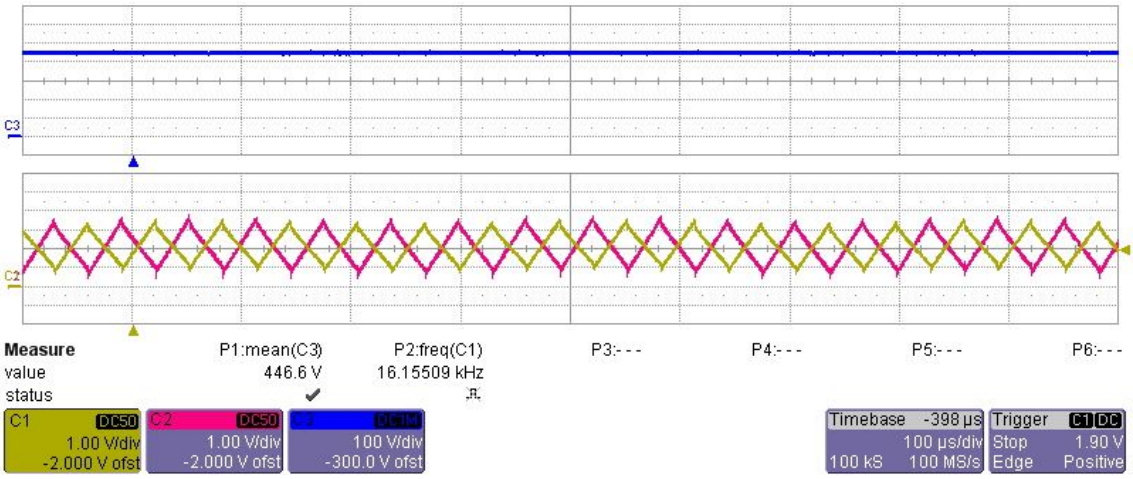
Appendix C

7.1.14 CCM Closed-Loop Responses with PI Controllers at Duty Cycle of 0.5

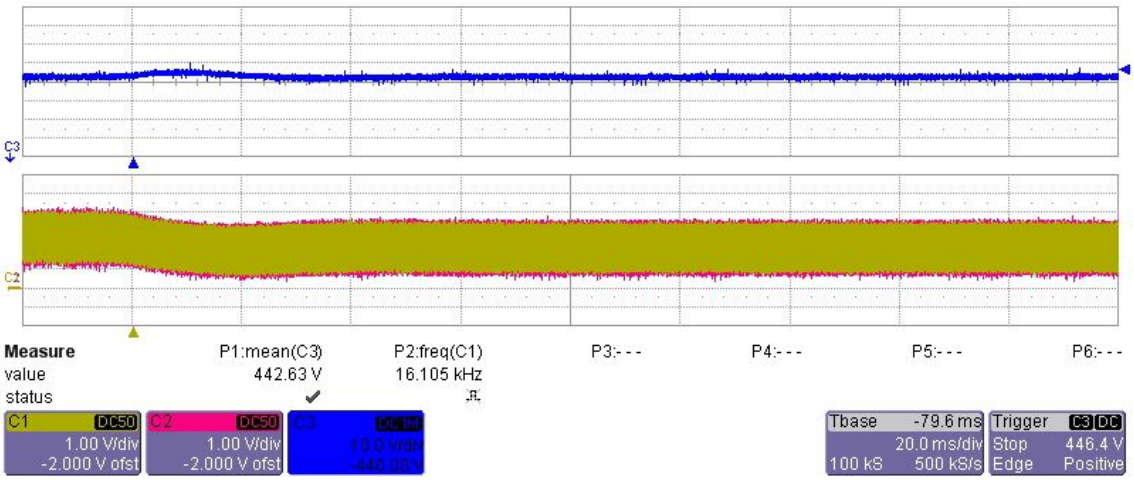
7.1.14.1 Converter Start-Up



7.1.14.2 Converter Steady-State

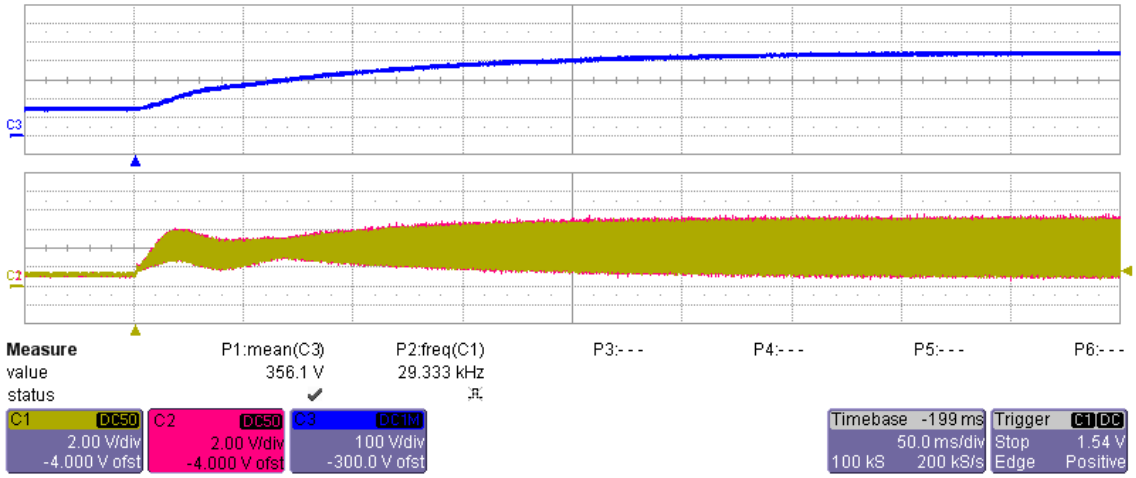


7.1.14.3 Converter Load Drop

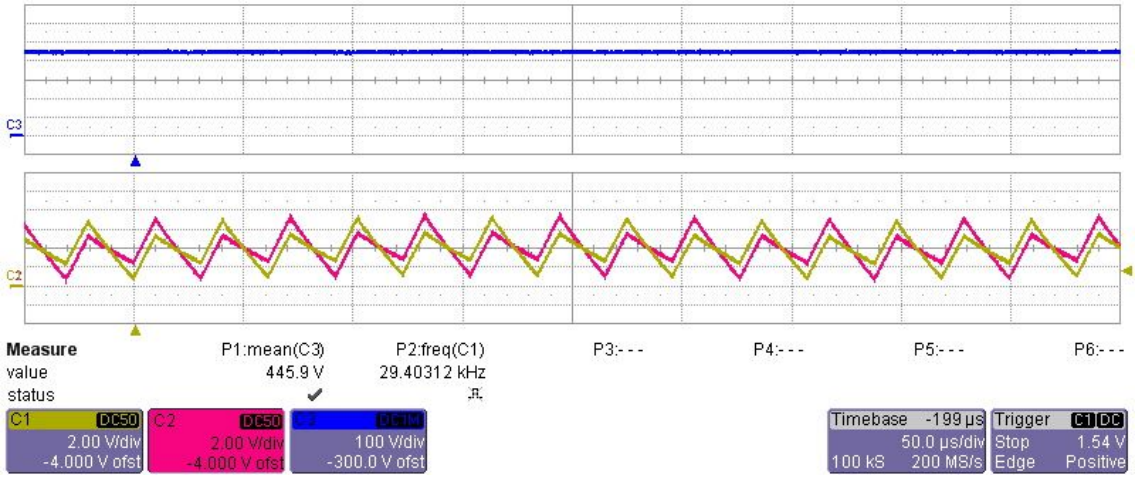


7.1.15 CCM Closed-Loop Responses with PI Controllers at Duty Cycle of 0.67

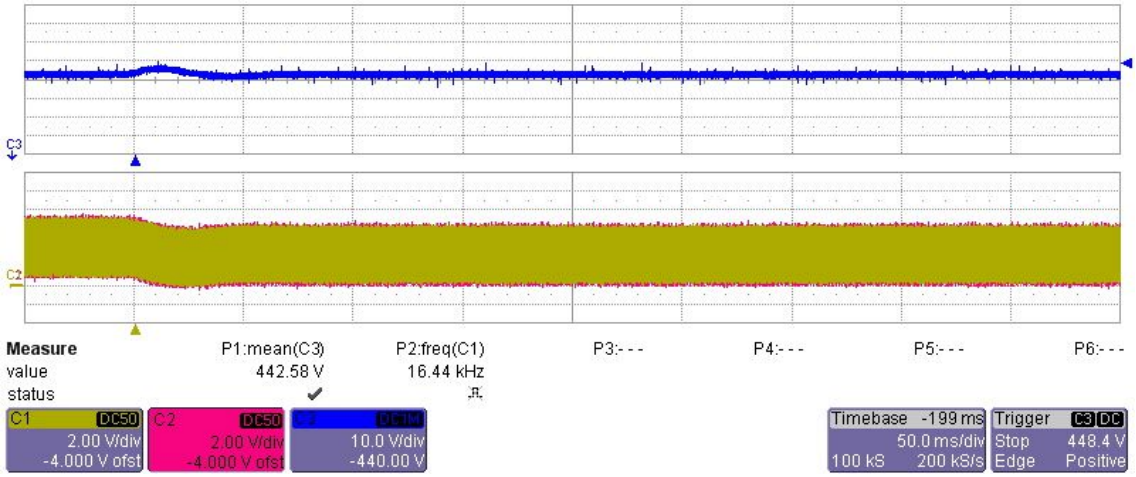
7.1.15.1 Converter Start-Up



7.1.15.2 Converter Steady-State

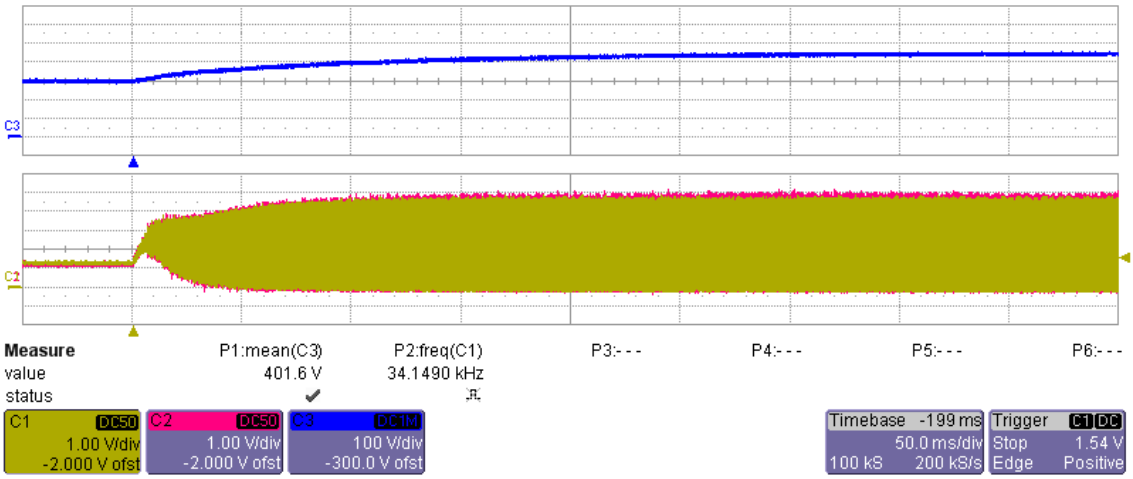


7.1.15.3 Converter Load Drop

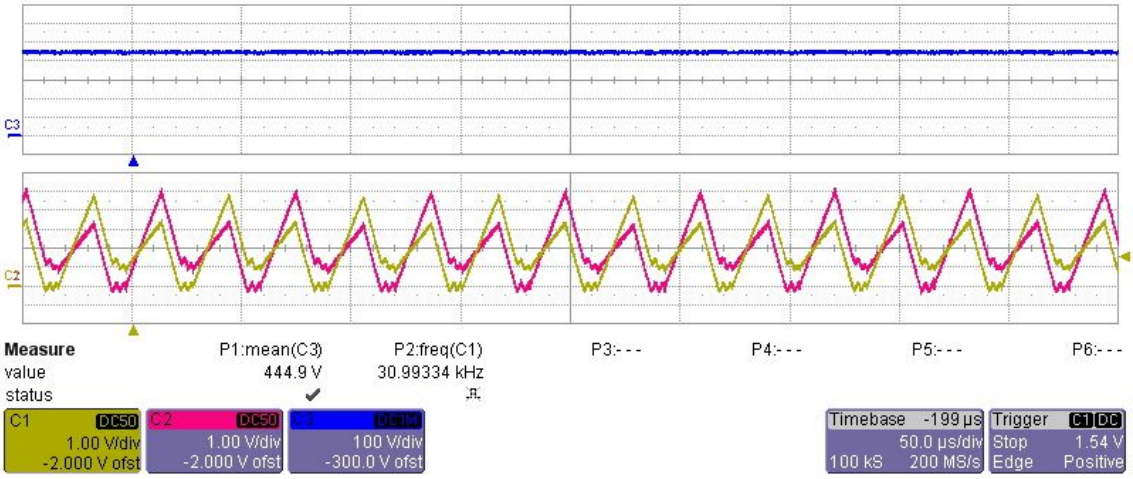


7.1.16 DCM 1 Closed-Loop Responses with PI Controllers

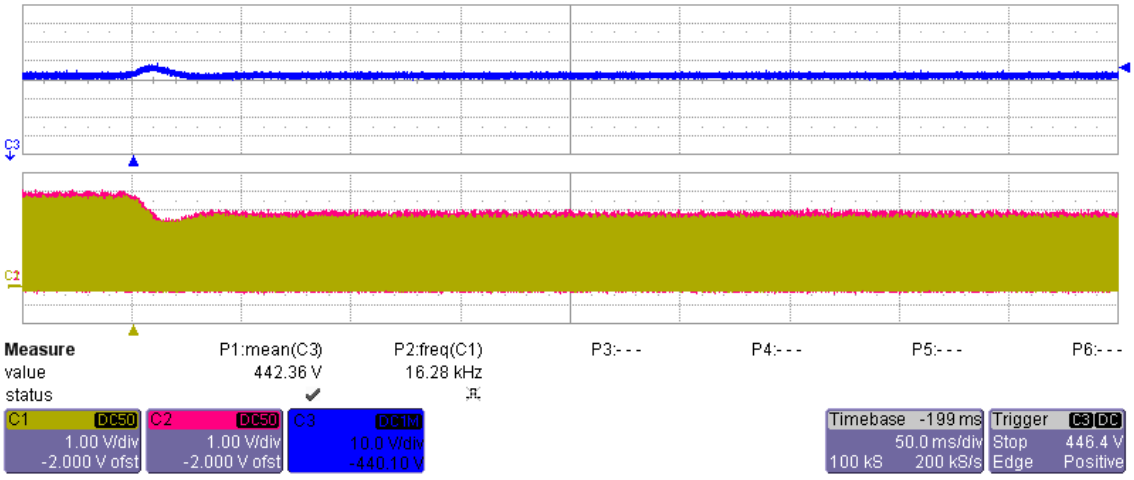
7.1.16.1 Converter Start-Up



7.1.16.2 Converter Steady-State

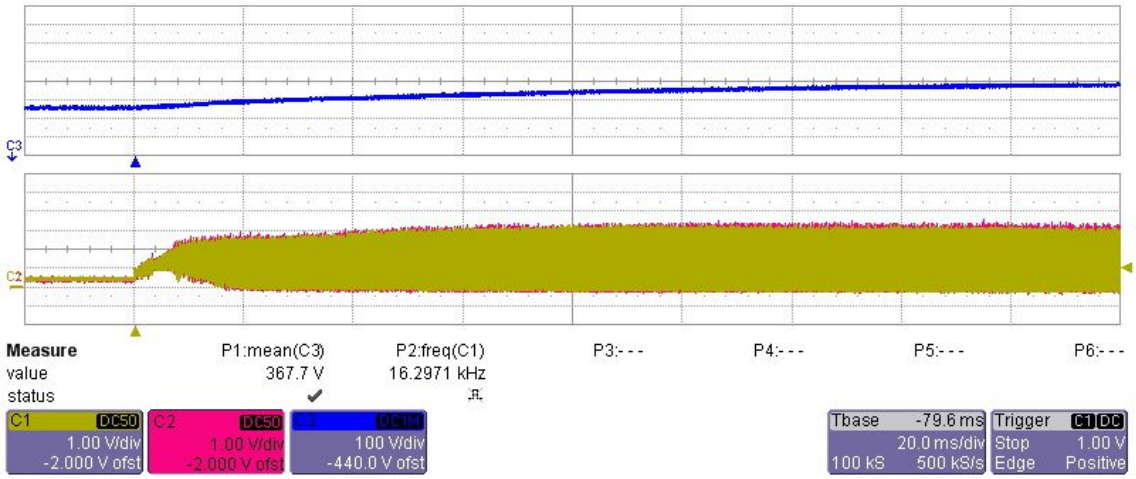


7.1.16.3 Converter Load Drop

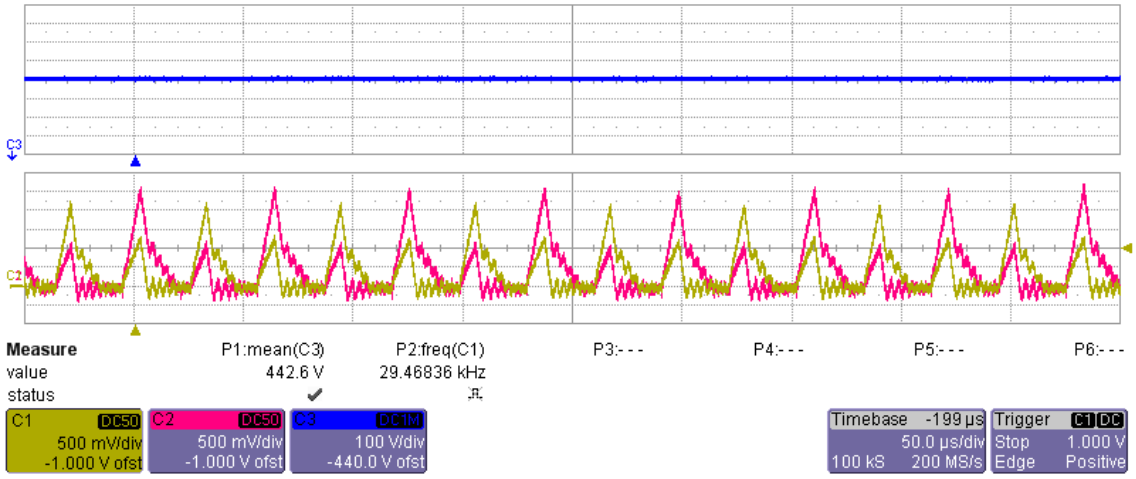


7.1.17 DCM 2 Closed-Loop Responses with PI Controller

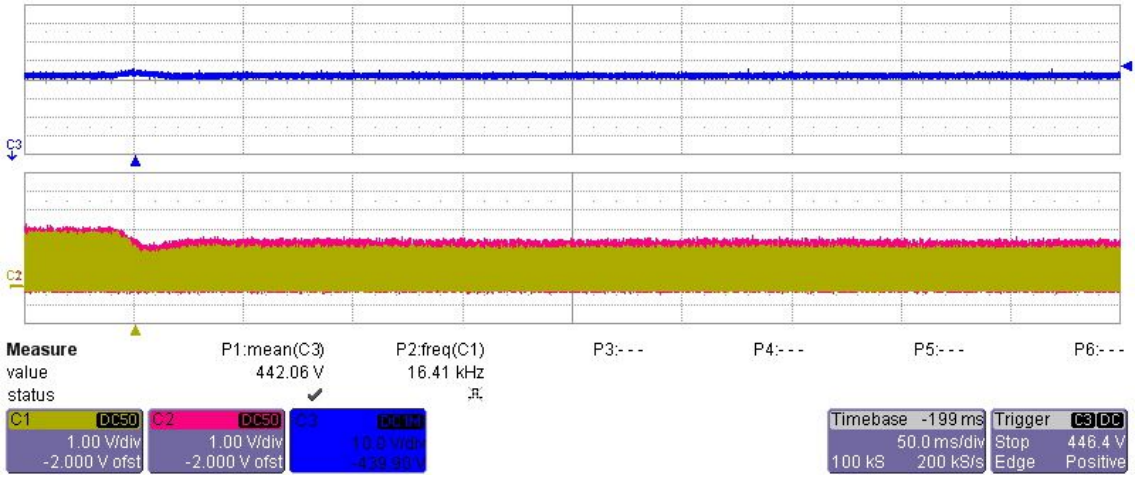
7.1.17.1 Converter Start-Up



7.1.17.2 Converter Steady-State

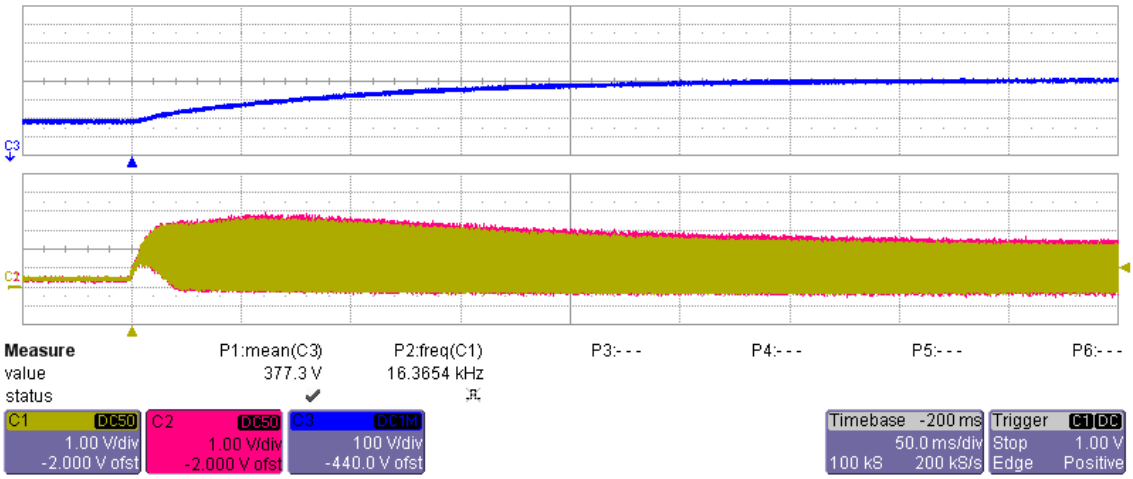


7.1.17.3 Converter Load Drop

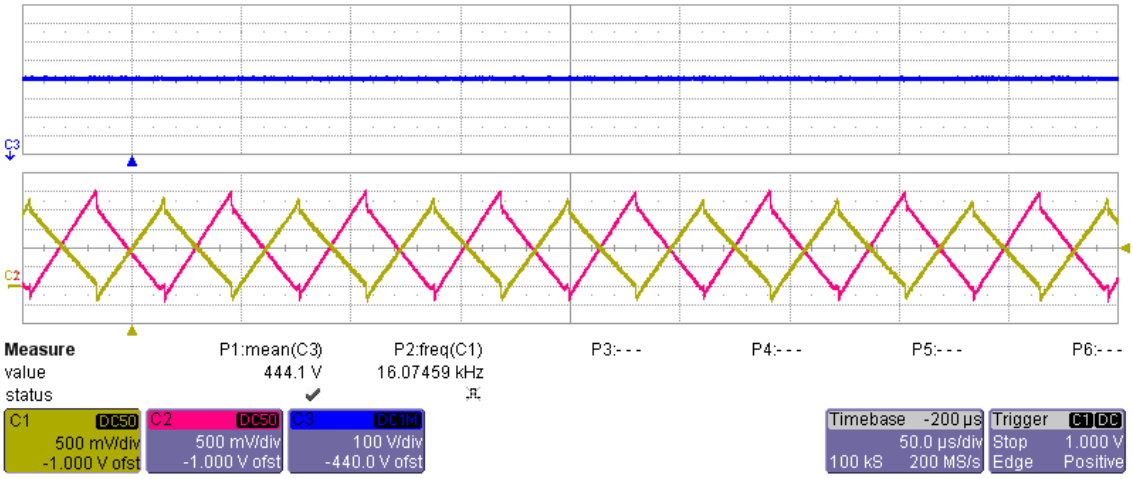


7.1.18 DCM 3 Closed-Loop Responses with PI Controllers

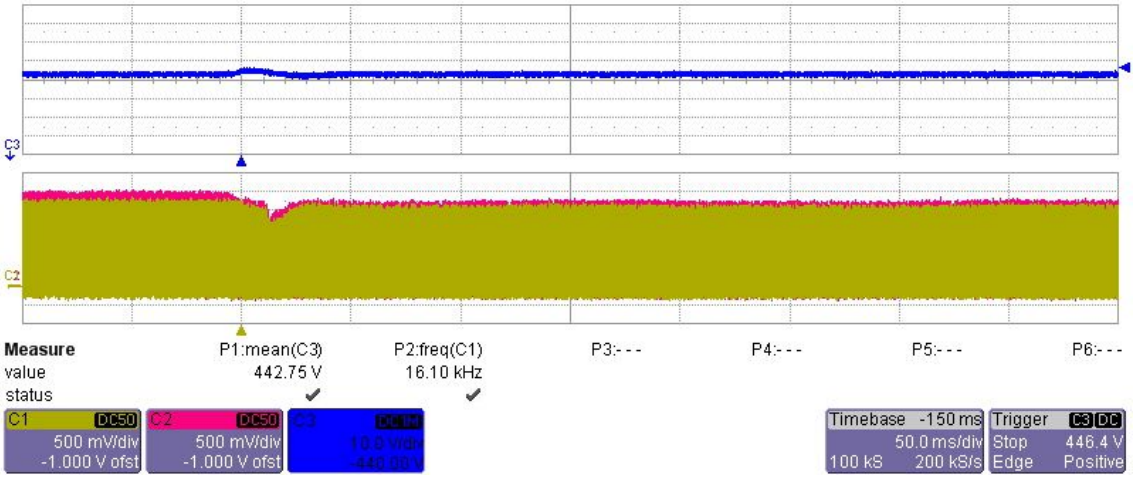
7.1.18.1 Converter Start-Up



7.1.18.2 Converter Steady-State

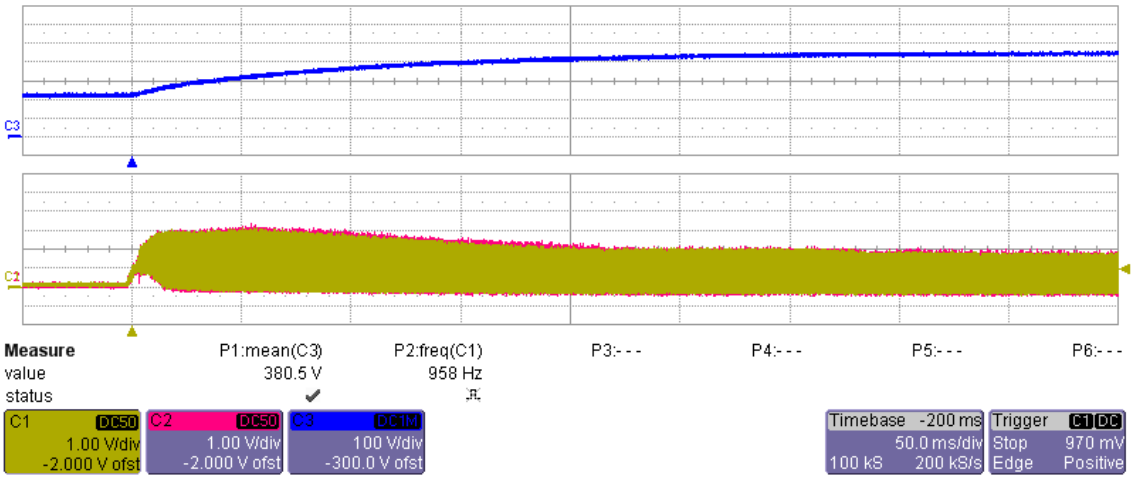


7.1.18.3 Converter Load Drop

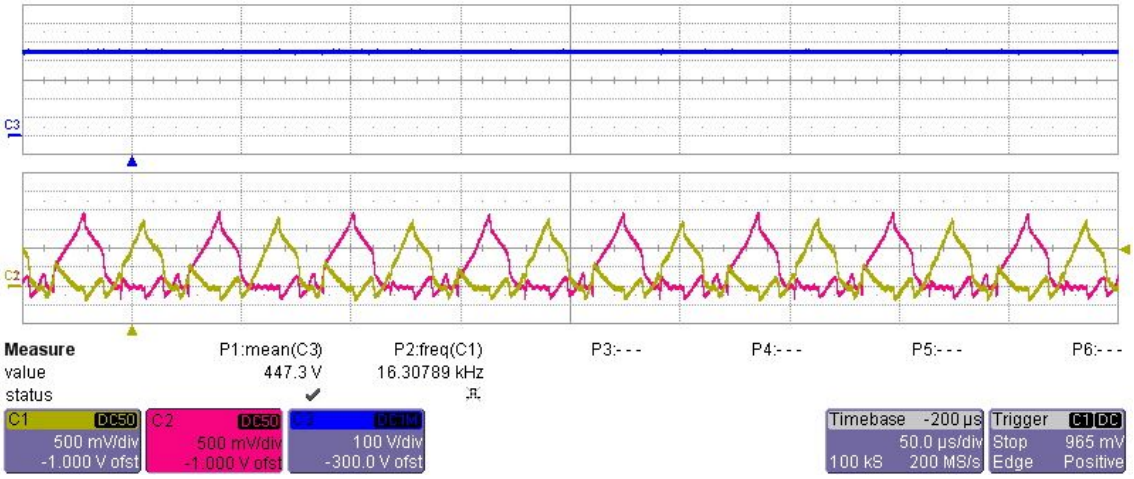


7.1.19 DCM 4 Closed-Loop Responses with PI Controllers

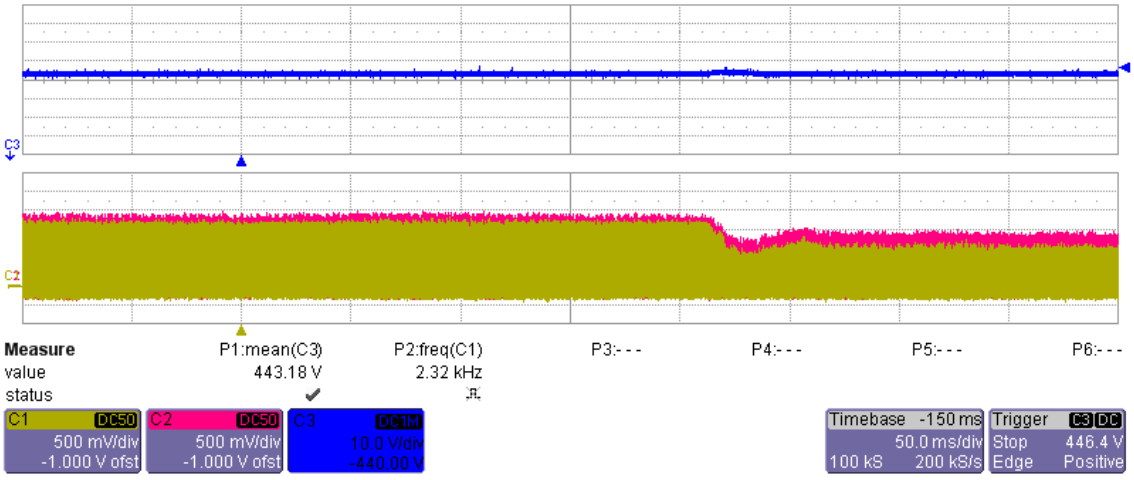
7.1.19.1 Converter Start-Up



7.1.19.2 Converter Steady-State

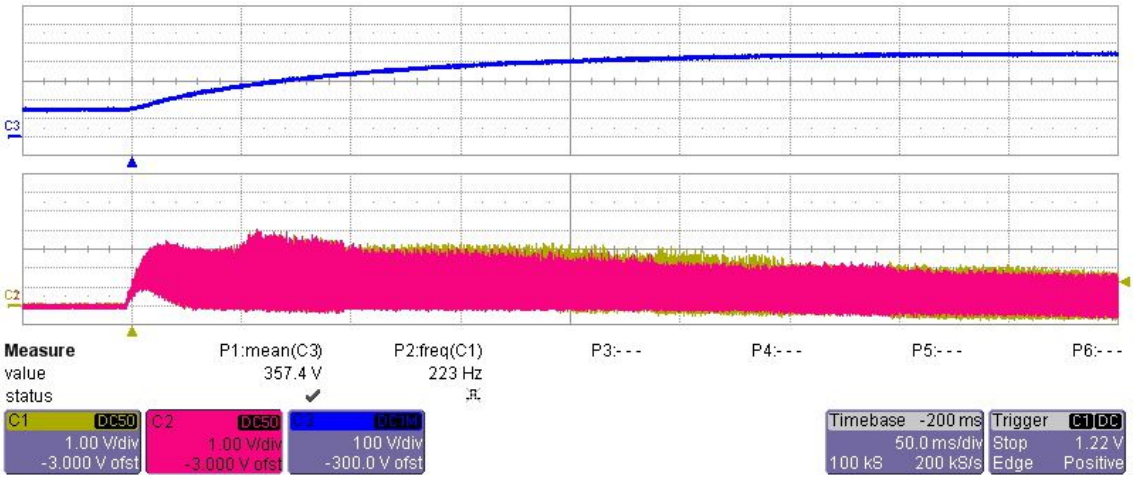


7.1.19.3 Converter Load Drop

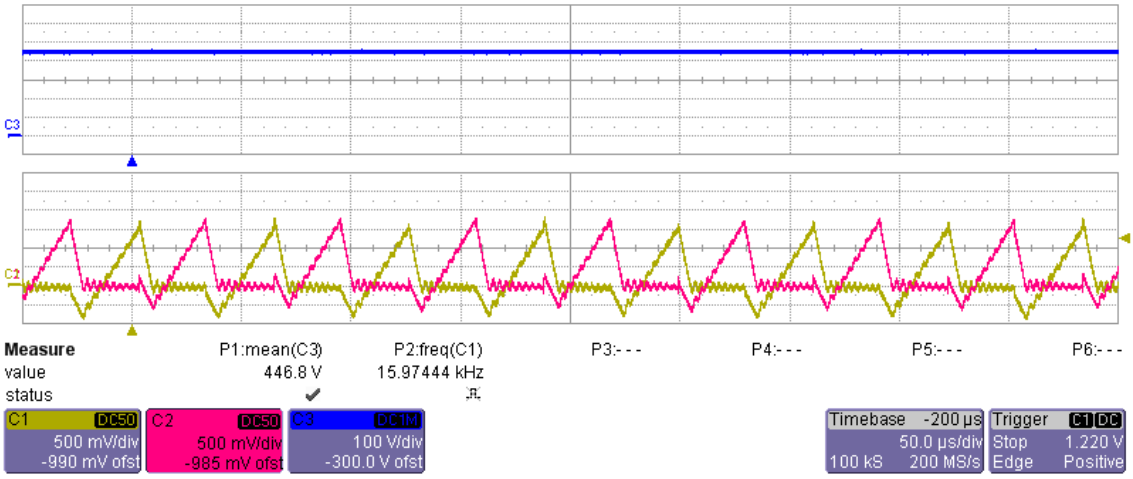


7.1.20 DCM 7 Closed-Loop Responses with PI Controllers

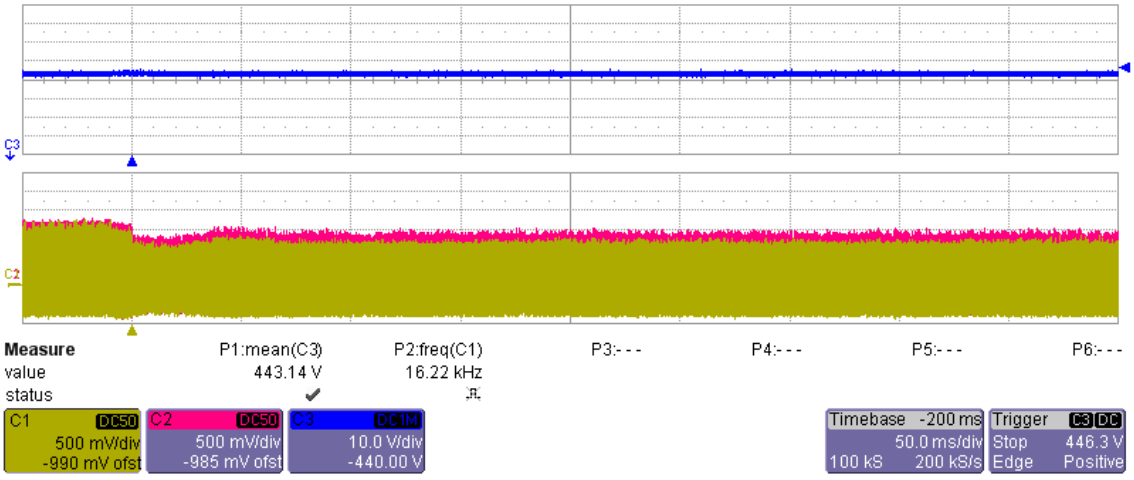
7.1.20.1 Converter Start-Up



7.1.20.2 Converter Steady-State

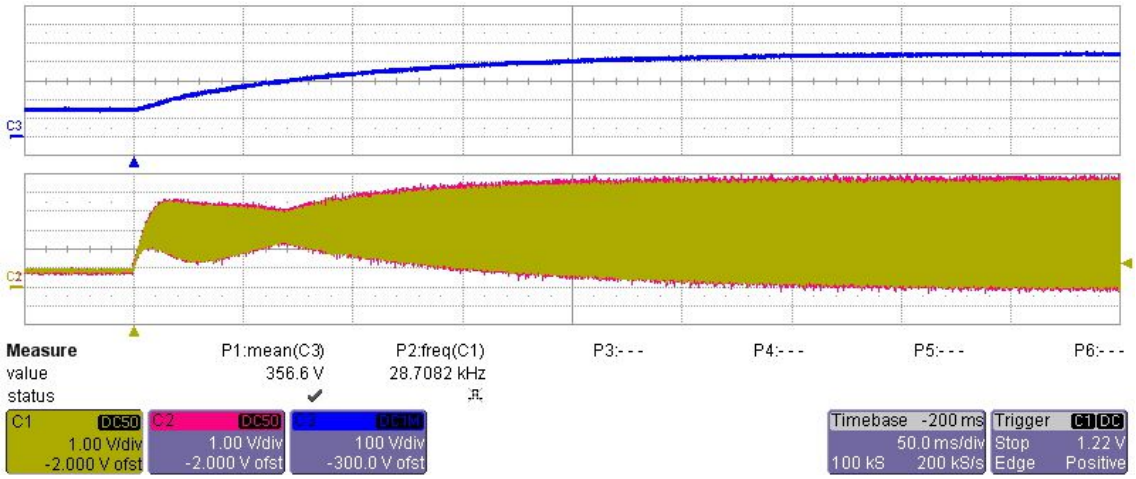


7.1.20.3 Converter Load Drop

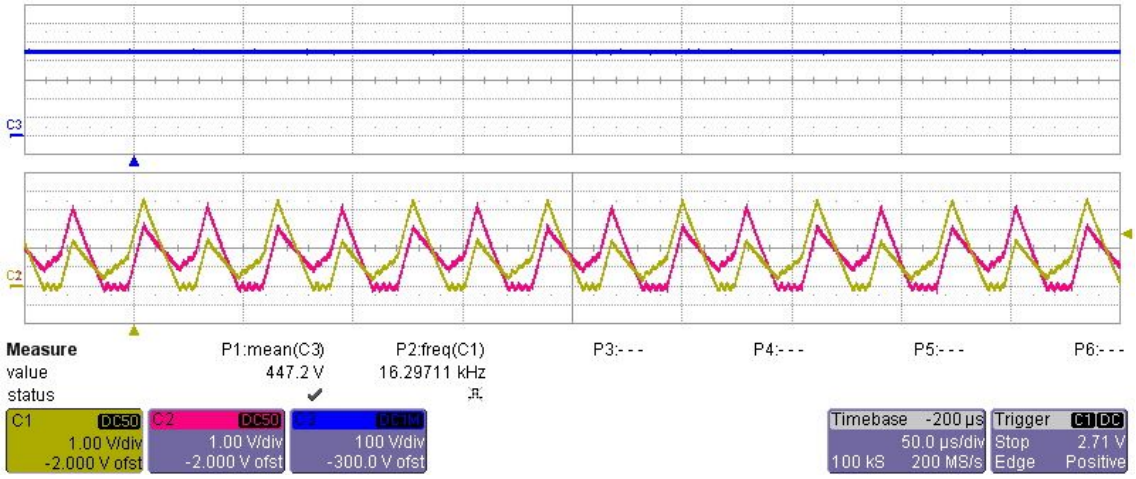


7.1.21 DCM 8 Closed-Loop Responses with PI Controllers

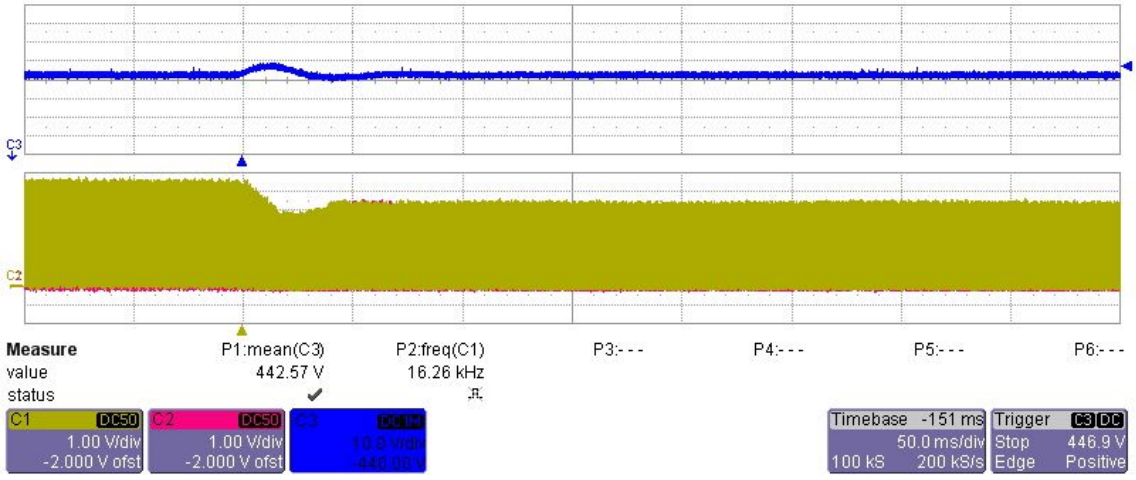
7.1.21.1 Converter Start-Up



7.1.21.2 Converter Steady-State

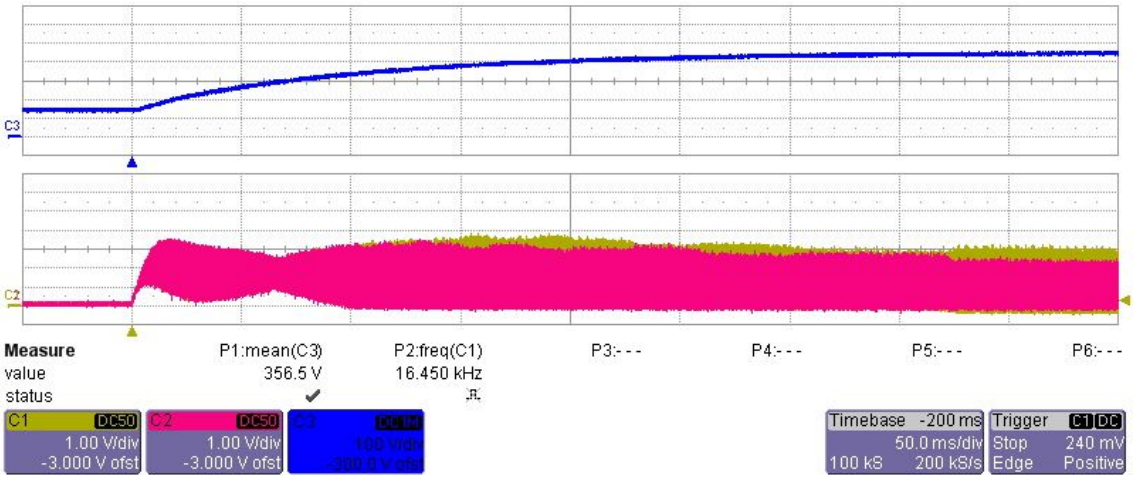


7.1.21.3 Converter Load Drop

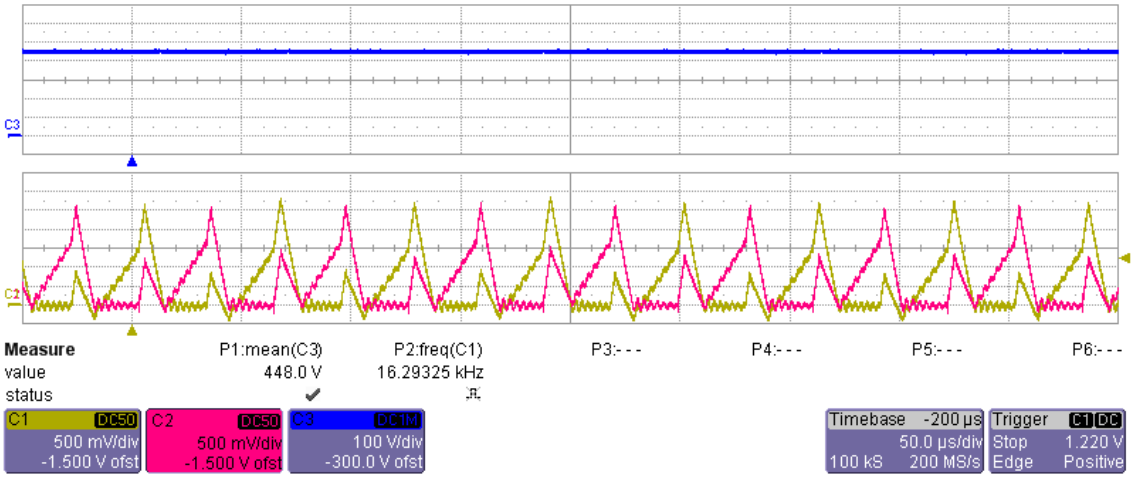


7.1.22 DCM 9 Closed-Loop Responses with PI Controllers

7.1.22.1 Converter Start-Up



7.1.22.2 Converter Steady-State



7.1.22.3 Converter Load Drop