

Copper Diffusion Barrier Deposition on Integrated Circuit Devices by Atomic Layer Deposition Technique

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Academic Dissertation

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ABSTRACT

Transfer from aluminum to copper metallization and decreasing feature size of integrated circuit devices generated a need for new diffusion barrier process. Copper metallization comprised entirely new process flow with new materials such as low-k insulators and etch stoppers, which made the diffusion barrier integration demanding. Atomic Layer Deposition technique was seen as one of the most promising techniques to deposit copper diffusion barrier for future devices.

Atomic Layer Deposition technique was utilized to deposit titanium nitride, tungsten nitride, and tungsten nitride carbide diffusion barriers. Titanium nitride was deposited with a conventional process, and also with new *in situ* reduction process where titanium metal was used as a reducing agent. Tungsten nitride was deposited with a well-known process from tungsten hexafluoride and ammonia, but tungsten nitride carbide as a new material required a new process chemistry. In addition to material properties, the process integration for the copper metallization was studied making compatibility experiments on different surface materials. Based on these studies, titanium nitride and tungsten nitride processes were found to be incompatible with copper metal. However, tungsten nitride carbide film was compatible with copper and exhibited the most promising properties to be integrated for the copper metallization scheme. The process scale-up on 300 mm wafer comprised extensive film uniformity studies, which improved understanding of non-uniformity sources of the ALD growth and the process-specific requirements for the ALD reactor design. Based on these studies, it was discovered that the TiN process from titanium tetrachloride and ammonia required the reactor design of perpendicular flow for successful scale-up.

The copper metallization scheme also includes process steps of the copper oxide reduction prior to the barrier deposition and the copper seed deposition prior to the copper metal deposition. Easy and simple copper oxide reduction process was developed, where the substrate was exposed gaseous reducing agent under vacuum and at elevated temperature. Because the reduction was observed efficient enough to reduce thick copper oxide film, the process was considered also as an alternative method to make the copper seed film via copper oxide reduction.

PREFACE

This work that eventually resulted in my dissertation was started at ASM Microchemistry Oy in year 1999. This work comprised an early phase of copper diffusion barrier studies, and since then a lot of new results have been published by several authors.

I am grateful to my astonishing and unforgettable team in ASM Microchemistry Oy including Sari Kaipio, Ville Saanila, Pekka J. Soininen, Wei-Min Li, and Juhana Kostamo, as well as all other co-authors for their great contribution. From my foreign co-authors I wish to thank particularly Alessandra Satta, Steven Smith, and Wim Besling with whom I worked very closely.

I am very grateful to Prof. Markku Leskelä who has offered me support whenever it was needed. Without his flexibility and patience for my never ending studies, this work would not have taken place. I express my kind gratitude to Prof. Mikko Ritala for introducing me to the wonderful world of ALD.

I am thankful for Pekka Reinikainen who volunteered to read proof of my thesis and made good suggestions.

I am thankful for my loving parents, Marjatta and Nils-Erik who have always given me unquestionable support. Most of all, I am grateful to my wife, Virpi who has been standing close by and been supportive towards my studies.

LIST OF PUBLICATIONS

Thesis is composed of the publications listed below. The publications are listed in chronological order and they are referred in the text with a Roman number.

- I** A.Satta, M. Baklanov, O. Richard, A. Vantomme, H. Bender, T. Conard, K. Maex, W. M. Li, K.-E. Elers, and S. Haukka: Enhancement of ALCVD TiN growth on Si-O-C and α -SiC:H films by O₂-based plasma treatments, *Microelectronic Engineering*, 60 (2002) 59.

- II** K.-E. Elers, V. Saanila, P.J. Soininen, W.-M. Li, J.T. Kostamo, S. Haukka, J. Juhanaja, W.F.A. Besling: The diffusion barrier deposition on copper surface by atomic layer deposition technique, *Chem. Vap. Deposition*, 8 (2002) 149.

- III** S. Smith, W.-M. Li, K.-E. Elers, K. Pfeifer: Physical and electrical characterization of ALCVD TiN and W_{N_x}C_y used as a copper diffusion barrier in dual damascene backend structures (08.2), *Microelectronic Engineering*, 64 (2002) 247.

- IV** K.-E. Elers, V. Saanila, W.-M. Li, P.J. Soininen, J.T. Kostamo, S. Haukka, J. Juhanaja, W.F.A. Besling: Atomic layer deposition of W_xN/TiN and W_{N_x}C_y/TiN nanolaminates, *Thin Solid Films*, 434 (2003) 94.

- V** P.J. Soininen, K.-E. Elers, V. Saanila, S. Kaipio, T. Sajavaara, S. Haukka: Reduction of Copper Oxide Film to Elemental Copper, *Journal of the Electrochemical Society*, 152 (2005) G122.

- VI** K.-E. Elers, J. Winkler, K. Weeks, S. Marcus: TiCl₄ as a Precursor in the TiN Deposition by ALD and PEALD, *Journal of the Electrochemical Society*, 152 (2005) G589.

- VII** K.-E. Elers, T. Blomberg, M. Peussa, B. Aitchison, S. Haukka, S. Marcus: Film Uniformity in Atomic Layer Deposition, *Chem. Vap. Deposition*, 12 (2006) 13.

OTHER PUBLICATIONS BY THE SAME AUTHOR

This work resulted in the following US patents:

- 1) Method for bottomless deposition of barrier layers in integrated circuit metallization schemes.¹
- 2) Production of elemental thin films using a boron-containing reducing agent.²
- 3) Deposition of transition metal carbides.³
- 4) Method of growing electrical conductors by reducing metal oxide film with organic compound containing -OH, -CHO, or -COOH.⁴
- 5) Process for growing metalloid thin films utilizing boron-containing reducing agents.⁵
- 6) Sealing porous structures.⁶
- 7) Method of modifying source chemicals in an ALD process.⁷
- 8) Method of depositing transition metal nitride thin films.⁸
- 9) Method for depositing nanolaminate thin films on sensitive surfaces.⁹
- 10) Metal nitride deposition by ALD with reduction pulse.¹⁰
- 11) Multilayer metallization.¹¹
- 12) Oxygen bridge structures and methods to form oxygen bridge structures.¹²
- 13) Conformal lining layers for damascene metallization.¹³
- 14) Process for producing integrated circuits including reduction using gaseous organic compounds.¹⁴

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LIST OF ABBREVIATIONS AND ACRONYMS

AFM	atomic force microscope
ALD	atomic layer deposition
ALE	atomic layer epitaxy
AR	aspect ratio
ASM	advanced semiconductor materials
ASML	ASM lithography
BTS	bias temperature stress
CMOS	complementary metal-oxide semiconductor
CMP	chemical-mechanical polishing
CV	capacitance voltage
CVD	chemical vapor deposition
ECD	electrochemical deposition
EDS	energy dispersive spectroscopy
EELS	electron energy-loss spectroscopy
FIB-SEM	focused-ion-beam SEM
FSG	fluoro-silicate glass
FTIR	Fourier transform infrared
HRTEM	high resolution TEM
HVM	high volume manufacturing
IC	integrated circuit
IMP	ionized metal plasma
IPVD	ionized PVD
LEIS	low-energy ion scattering
MEMS	microelectromechanical system
MOS	metal-oxide-semiconductor
MPU	microprocessor unit
PEALD	plasma enhanced ALD
PVD	physical vapor deposition
R&D	research and development
RBS	Rutherford backscattering spectroscopy
RC	resistance times capacitance
REALD	radical enhanced ALD
RMS	root mean square
SEM	scanning electron microscope
TDMAT	tetrakis(dimethylamido)titanium
TEB	triethyl boron
TEM	Transmission electron microscopy
TEMAT	tetrakis(ethylmethylamido)titanium

TFEL	thin film electroluminescent
TMA	trimethyl aluminium
TOF-ERDA	time-of-flight elastic recoil detection analysis
VLSI	very large scale of integration
XPS	x-ray photoelectron spectroscopy
XRR	x-ray reflectometer

1. Introduction

In April 1965 Intel's co-founder, Gordon Moore, published a paper in *Electronics* magazine, where he introduced a "legendary" figure that has been referred to as Moore's Law.¹⁵ This figure depicted that the number of transistors in a square inch of silicon doubles every 12 months. Legend it became after the prediction was found correct until nearly these days, although a slight deceleration down to 18 months has occurred. After the first microprocessor that contained about 2,200 transistors, the progress has been tremendous. For example, Intel's 8080 processor in 1974 contained 6,000 transistors, the first Pentium processor in 1993 contained 3,100,000 transistors, and Pentium 4 in 2004 contained already 125,000,000 transistors on the chip when the chip size was only 112 mm², which equals the size of a finger tip. Today, when industry moves towards 45 nm process technology node, CoreTM2 quad-core processor comprises more than 500 million transistors. Such a transistor can be switched on and off approximately 300 billion times a second. Since the magnitude of these numbers is often very difficult to visualize, some simplifications are needed. For example: 1) you could fit more than 2000 transistors (45 nm) across the width of a human hair, 2) 300 billion times a second means that one switch equals the time a beam of light travels a couple of centimeters.

For the further discussion of the development of the integrated circuit (IC) industry later in this thesis, the background of Moore's Law has been explained here. Understanding of the background is important because it helps to understand many decisions made in the IC industry, as well as possible future predictions. Although the performance of processors has improved with increased number of transistors, Moore was primarily interested in shrinking transistor costs instead of improving transistor performance in his paper. Moore's paper also introduced a less known cost/integration curve that depicts how the relative manufacturing cost per component changes as a function of the number of component per integrated circuit. This figure shows that the manufacturing cost decreases rapidly with increased level of integration cutting down packaging cost. This continues until the integration challenges become overwhelming, thus increasing defect yield and manufacturing cost. The lowest point of this curve is a combination of certain major factors such as: 1) the maximum number of transistors, 2) the average number of defect per square inch, 3) the size of wafer, and 4) the costs

associated with producing multiple components like packaging costs. Consequently, the figure referred to as the Moore's Law, shows an important parameter how the cost/integration curve can function. When the feature sizes are shrinking, the cost/integration curve moves downwards. In other words, Moore's law was one of the major factors leading to the reducing of costs in the IC manufacturing. The cost-driven factors are also dominating when new process technologies are chosen for the IC manufacturing.

Moore's Law has led to increasing function density in the chip, defining the number of interconnected devices per chip area. As the minimum feature size of an IC decreases, the active device density increases. The device integration became more demanding because the area occupied by the interconnection lines on the chip surface extended more rapidly than the area needed to accommodate the active devices. Eventually, minimum chip area became interconnect-limited. At this point, continued shrinking of complementary metal-oxide semiconductor (CMOS) transistors produced less circuit-performance benefits. This dilemma was solved by a multilevel-interconnection system in which the area needed by the interconnect lines is shared among two or more levels (Figure 1). In 2010, the functional density of active devices in microprocessor unit (MPU) is so high that the number of metal levels is expected to be 12.¹⁶ Furthermore, because there are more gates, a larger number of connections between gates must be made, and the average length of the interconnection lines will increase. Total length of interconnects in MPU is expected be over 2 km/cm^2 when global wires are excluded.

As in all process steps, the cost impact of the multilevel metallization scheme had to be carefully considered. Although it made possible to manufacture more dies per wafer and reducing the cost per chip in that manner, it brought additional cost factors for the development, manufacturing, and the device reliability. For example: 1) new materials had to be used comprising significant R&D work, 2) process challenges meant some negative impact to the manufacturing yield, 3) new failure modes such as electromigration, corrosion, and hillock formation was expected to influence the circuit reliability. The question was whether the chip-size reduction and enhanced chip value will produce a margin of profit that is greater than the amount lost due to

additional incurred process costs and yield and reliability loss. Evidently, the multilevel metallization scheme became cost-effective and successful.

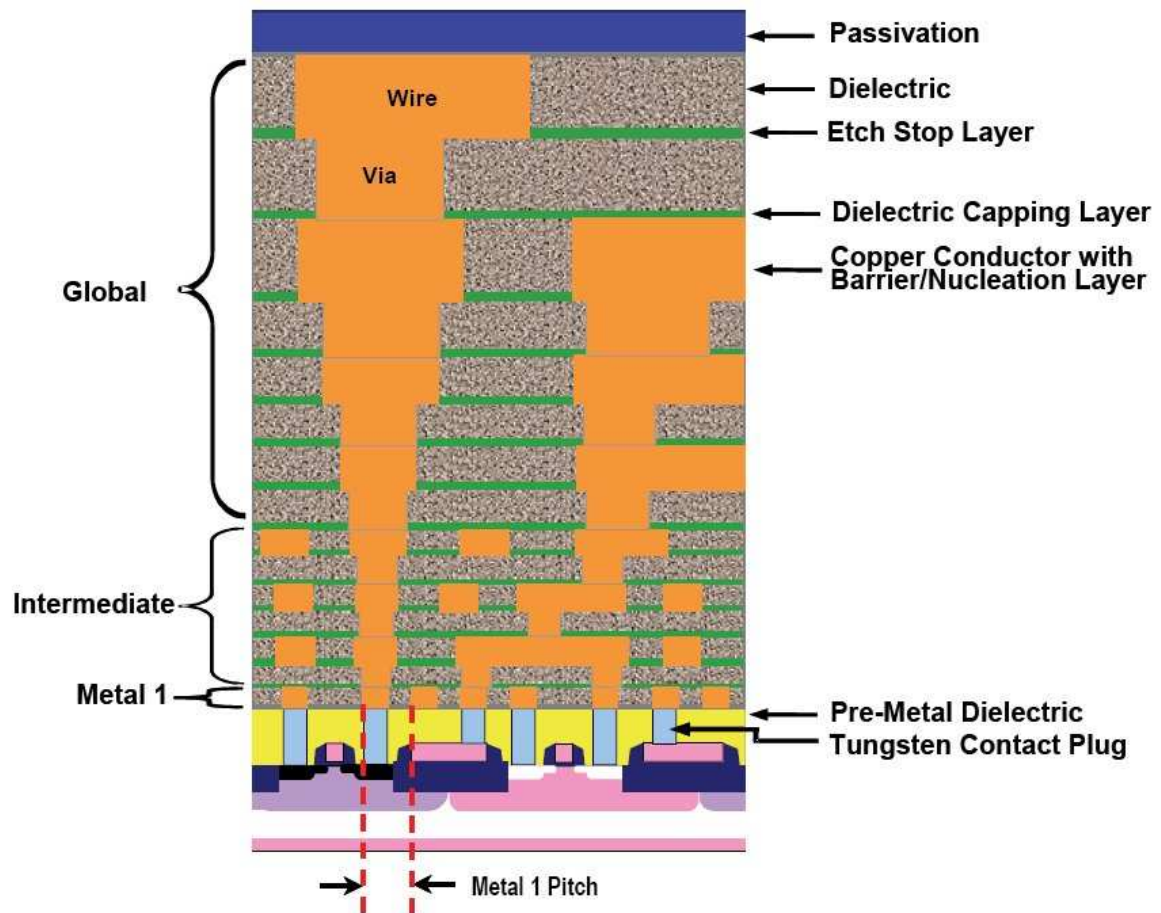


Figure 1. Cross-section of hierarchical scaling of MPU device.¹⁶

In late 1990s, it was found obvious that the increasing length of interconnects was leading to the increase in the resistance times capacitance (RC) time delay of interconnects, and in sub-quarter-micron device nodes the propagation delay passed the intrinsic delay that comprises the MOS transistor delay. The multilevel metallization was facing new challenges that required major changes in materials and the process flow. Minimization of the RC delay forced a transition from aluminium-copper (Al-Cu), tungsten (W), and silicon dioxide (SiO₂)-based interconnects to the Cu metal and the low-dielectric constant (κ) insulator metallization scheme.

In addition to the RC delay, conventional aluminum metallization was facing overwhelming challenges because aluminum is sensitive for electromigration, also

known as “electron wind effect”. When the current density increases, aluminum atoms can move in the lattice and cause severe device failures such as voids and “hillocks”.¹⁷ In the worst case, the wire will be open or shorting with other wire. Alternative metals such as tungsten, silver and gold were considered since they have better electromigration properties. However, tungsten has about twice as high electrical resistivity than pure aluminum, and gold and silver have a high cost. Copper metal was found to be an attractive option because of its high electromigration resistance and low bulk resistivity ($1.7 \mu\Omega \text{ cm}$ versus $2.7 \mu\Omega \text{ cm}$ for aluminum). After all, one of the most important reasons for a successful breakthrough of the copper metallization was the great progress achieved in the process development of robust and cost-effective copper deposition and patterning.

Because the copper metallization comprised entirely new process flow and new materials, new diffusion barrier for copper was needed. Atomic Layer Deposition (ALD) technique was seen as one of the most promising techniques to deposit copper diffusion barrier for future devices, when the design node was shrinking.

Discussion in this thesis is presented in chronological order. The discussion in the chapter of Background is limited to the publications that were available when the experimental work was done. Publications which have become available later are discussed in the chapter of New Discoveries.

2. Motivation for the Present Study

Since most of the work was done in ASM, Inc. which is a tool and process supplier for the IC manufacturers, motivation for this work was based on possible business opportunities in the metallization market. The copper diffusion barrier process is perceived as a part of back-end-of the line market that is the biggest market sector in the IC equipment market. Entire capital spending on IC equipment in year 2007 totaled \$44.5 billion.¹⁸ The reason for bigger back-end-of the line market is very obvious because the MPU devices require 9-12 metallization layers multiplying the need of process equipments. Contrary to back-end-of the line manufacturing process, the manufacturing process of the transistors is often needed only once, which is a

characteristic for all front-end-of the line processes. The back-end-of the line market has been dominated by the companies named Applied Materials, Tokyo Electron, ASML, and Novellus.

In 1999, the consequences of increase in the number of transistors per chip were expected to increase the need for new diffusion barrier process in the near future. The consequences comprised a new interconnect material and continuously shrinking interconnects, which was eventually expected to make physical vapor deposited (PVD) diffusion barrier inadequate for metallization. Acknowledging the limitations of PVD films, the IC industry was expected to choose the chemical vapor deposited (CVD) or ALD diffusion barrier instead for future devices.

Because of the above business factors being closely involved with this work, the application was well defined prior to studies. The scope of this study has been in the process integration challenges, which minimizes the risk for spending money and resources on processes that may fail in the process integration.

3. Background

3.1. Diffusion Barriers Prior to Copper Metallization

The diffusion barrier layer is used to stop diffusion between two different materials. In the IC metallization the barrier is used to separate the insulators and conductors that used to be silicon dioxide (SiO_2)-based dielectrics and aluminum and tungsten metals. Because the diffusion has a negative impact to the device performance regardless the direction of diffusion, the barrier must work towards both directions.

Barrier materials can be categorized according to the diffusion barrier mechanism.¹⁹ Three major mechanisms are: 1) passive barrier: layer which is immiscible and does not react chemically with other materials; 2) stuffed barrier: a passive barrier with structural defects like grain boundaries, which are stuffed by another materials; 3) sacrificial barrier: a material which reacts chemically with other materials. During chemical reaction interdiffusion is prevented, but the barrier fails as soon as the

material is completely consumed. Historically, polycrystalline liners tend to yield the poorest barrier performance and are thus the least desirable for diffusion barrier applications.²⁰ This generalization is particularly justified when the film has a columnar structure where the grain boundaries extend throughout the entire film thickness, thus providing an effective pathway for diffusion. Consequently, in the light of crystallinity a desirable diffusion barrier has amorphous or nano-crystalline structure that makes diffusion path complex for atoms and molecules.

Horizontal conductors of the IC devices are mainly made with aluminum metallization. Since the film is deposited on nearly flat surface, there are no high surface morphology requirements, and the film can be deposited with PVD techniques. However, tungsten is often used in vertical vias having higher morphology requirements depending on aspect ratio (AR) of the via. Consequently, tungsten metal is deposited with the CVD technique that offers a better step coverage for the film than the PVD techniques.

Titanium (Ti) and titanium nitride (TiN) diffusion barrier (film stack for aluminum: TiN/Ti/Al/Ti/TiN) made by PVD has been a “work horse” for the aluminium metallization having effective barrier properties against Al, W, and Si diffusion.^{19, 21} It is also adhesion promoter by improving wettability of aluminium interconnect and by enhancing its mechanical stability. Because of this multipurpose they are often called liners. In tungsten plug Ti/TiN reduces contact resistance and improves tungsten adhesion. Titanium nitride has an important role to protect elemental Ti and SiO₂ surface from WF₆ that is often used in the tungsten nitride deposition by CVD. Tungsten hexafluoride reacts with Ti and SiO₂ and forms gaseous TiF₄ and SiF₄, which can leave behind drastic surface damages (Figure 2).

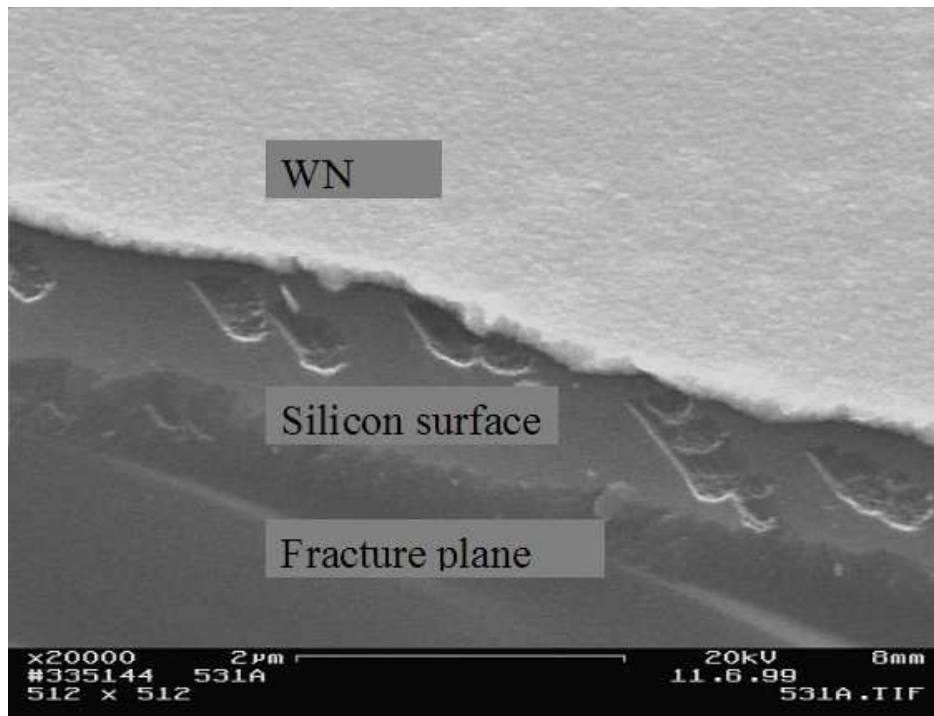


Figure 2. “Worm holes” on silicon surface caused by tungsten hexafluoride [II].

As mentioned earlier, PVD-TiN has been the technique of choice in the IC industry. Although CVD-TiN has some major advantages like a good step coverage, it has also major disadvantages compared to PVD-TiN. Currently, those disadvantages are more significant for the IC industry than its advantages. One disadvantage of CVD-TiN is its relatively high deposition temperature ($> 550\text{ }^{\circ}\text{C}$) that is required to obtain the film with a low impurity content. The CVD-TiN film often contains some amount of halide or carbon residues depending on which metal precursor was used. Those mobile residues, which can diffuse in the device and degrade its performance, worry the IC industry a lot. Furthermore, there is often extensive growth of ammonium chloride (NH_4Cl) in cold walls of the CVD reactor. This is raising particle and impurity concerns.

Because the resistivity of diffusion barrier material is higher than that of aluminum or tungsten metal, the thickness of diffusion barrier should be as low as possible to reduce the overall resistance of metal wires. Nevertheless, the diffusion barrier must fulfill its primary mission as a barrier, which limits how thin barrier film can be used.

When tungsten is used to fill vias, a TiN layer of 50Å is enough to protect underlying surface in the bottom of via.²²

Today, few of the most common techniques used for the PVD-barrier depositions are ionized magnetron sputtering and ionized metal plasma (IMP). Whereas the collimator and long-throw techniques faced major difficulties already with AR of 3:1, the IMP technique offered significant improvement and further extend to smaller design nodes of the IC industry. In IMP technique the sputtered atoms are ionized between the target and the substrate. Since the substrate is biased, the ionized atoms will be accelerated and controlled in certain direction resulting in collision of high yield of atoms to the substrate in perpendicular angle. In ionized magnetron sputtering, the atoms are controlled by magnetic field. Effective utilization of sputtered atoms makes these techniques even more attractive cost-wise comparing to the collimator and long-throw techniques.

3.2. Copper Metallization

In 1997 IBM announced that it had developed circuitry where aluminum was replaced with copper metallization. IBM called its technology CMOS 7S and it was a major milestone in semiconductor technology. Six level copper metallization was materialized by using planarization technique called chemical-mechanical polishing (CMP) and electrochemically deposited (ECD) copper.²³ Instead of metal etching, vias and trenches were etched directly in an insulator. Patterned surface was filled by copper and excess copper was removed by CMP. A technique where vias and trenches were made simultaneously for chip wiring was called a dual damascene process. Few years later Intel Corporation was developing their production capability for dual-damascene processing, and the CPU production with the copper metallization was launched for 130 nm process technology node.²⁴ Copper and dual damascene processing on 300-mm-wafers was quickly establishing its position in the IC industry. Nowadays, industry has moved towards 45 nm process technology node and the copper metallization is facing challenges of increasing resistance due to electron scattering^{25,26}, which leads to increasing thermal budget of circuitry. Although copper metal was chosen over aluminum based on its good electromigration properties,

copper wires are still sensitive for stress migrations and electromigration particularly at interfaces.²⁷

3.2.1. Process Flow

In this chapter, the process flow of copper metallization is presented generally offering reasonable understanding of the process steps before and after the diffusion barrier deposition. As mentioned before, the insulators and etchstopper layers are deposited prior to metallization. An insulator, which is made of silicon oxide or silicon oxide based or made of silicon based low-k or other low-k materials, is etched with conventional wet etching techniques or dry etching. In dual damascene process etchstopper layer, e.g. silicon nitride or silicon carbide, is used to obtain a particular shape of via and trench. Once etching has been performed the pattern of wiring is ready and open copper metal contact of underlying metal layer can be seen in the bottom of via. Prior to the diffusion barrier deposition on patterned features, the surface of insulator and the copper contact must be cleaned. When the cleaning is accomplished, the diffusion barrier is deposited followed by copper seed deposition. The copper seed layer, which is often deposited by IMP technique, is required for the ECD copper process. Then ECD-Cu is used to fill trenches and vias. Excess copper and the diffusion barrier on the top horizontal surface are removed with the CMP technique ensuring that the wires are not shorting. After the surface cleaning the next layer of insulator is deposited for the next metallization level. To avoid reoxidation of copper surface after its reduction it would be an advantage to be able to integrate some of these processes. The next chapters discuss the process integration requirements of the diffusion barrier process comprising the cleaning step prior to the barrier deposition and the copper seed deposition on the diffusion barrier (Figure 3).

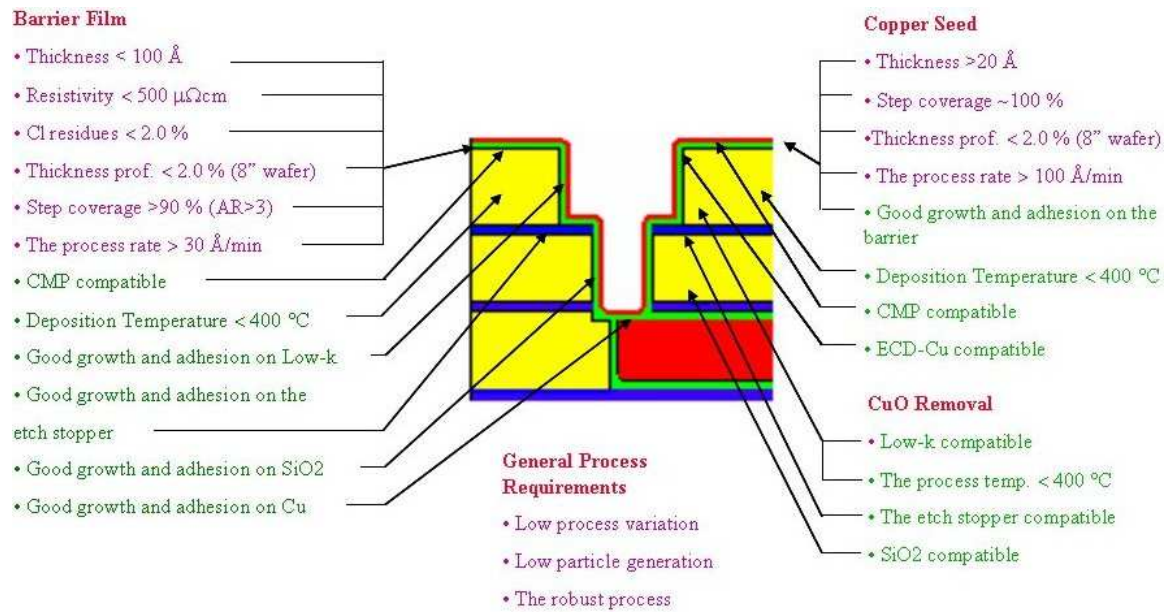


Figure 3. Process requirements for the diffusion barrier and copper seed layer integration to the copper metallization.²⁸

3.2.2. Surface Cleaning and Reduction

After lithography the surface of insulators and the copper contact in the bottom of via contain various residues from the etching process and copper surface is oxidized. Wet²⁹ as well as plasma cleaning processes have been developed for the surface cleaning. Conventionally, the copper oxide as well as etching residues are removed by argon ion sputtering. One of the major disadvantages of this method is the resputtering of copper from the bottom of via to the side walls of via. Possible Cu agglomeration on side walls is a reliability issue. Alternative methods, such as H₂/Ar plasma have been developed.^{30, 31}

3.2.3. Copper Diffusion Barrier

The choice of copper diffusion barrier material was based on several factors: 1) material properties, 2) process performance, 3) material and process compatibility with the process integration, and 4) overall cost.

Material properties.—In 2001, copper diffusion barrier was expected to be thinner than 10 nm in the near future. Decreasing thickness was a natural development in improving the RC delay of metal wiring. Limitations of material thickness were the barrier properties and the step coverage. Resistivity was expected as low as possible, max: 500 $\mu\Omega\text{cm}$. Typically, resistivity is measured on the film surface by four-point-probe, which gives an idea about the resistivity in horizontal trench wiring and sidewalls of via. However, in the bottom of via current flow is perpendicular to film surface and the resistance of copper wire and barrier layer are in series and have to be added.³² Impurities such as halide and carbon residues should be less than 2.0 %. Impurities that often result from precursors used in the barrier deposition are equally unfavorable when they degrade electrical properties of wiring or they are mobile causing impurities to spread out to metal wiring.

Naturally, it was a great challenge to find a material with the best diffusion barrier properties against copper diffusion. One of the challenges in the diffusion barrier evaluation has been non-standardized measurement techniques. Since barrier properties are measured using various techniques, a critical consideration and comparison of different materials and the same materials in different studies have been very challenging. The following techniques were mostly used: 1) Barrier followed by copper film is deposited on silicon substrate after native oxide is removed. The film stack is heated at the elevated temperature in vacuum. If copper diffuses through the barrier film, it reacts with silicon and forms copper silicide (CuSi_x). The formation can be observed by microscope³³, XRD³⁴, AES³⁵, and SEM^{36, 37}. 2) Copper silicide formation can also be verified by “Secco” eth test.³⁸ 3) Barrier followed by copper film is deposited on thermally grown silicon oxide. Metal-Oxide-Semiconductor (MOS) structure without barrier is made for the reference. Structure is exposed to bias temperature stress (BTS) ageing. Copper drifting is observed in capacitance voltage (C-V) curves.^{39, 40} Barrier performance was also studied with etch resistance experiments where barrier on via structure was exposed to HF solution. If the barrier failed in sidewalls of via, underlying silicon was etched. It was often discussed by Process Engineers of IC manufacturers how well this experiment represents the diffusion barrier properties in an actual device.

The process rate must meet the expectation of production capacity. If the process is slow, more deposition equipments are needed to fulfill the capacity requirements and the cost of ownership is higher. The process rate was expected to be higher than 3 nm/min that corresponds a throughput of 10 wafers/hour in single wafer reactor (the target thickness ≈ 10 nm). This is very minimum throughput in the IC industry where 20 wafers/hour is not abnormal. Expectation of step coverage requirements changed with the copper metallization since the dual damascene process flow was used. The increase of AR in dual damascene structure has been moderate in new design nodes. Step coverage $> 90\%$ was needed as soon as AR was higher than three. Thickness uniformity cross the wafer was becoming more and more important factor of process performance when the wafer size was increasing. The uniformity of the barrier film was expected to be below 2 % (standard deviation, 1 sigma) with 4 mm edge-exclusion.

Various transition metals, their binary and ternary compounds have been suggested for the copper barrier application. The compounds of W, Ta and Ti are the most studied comprising desirable physical, chemical, and electrical properties. Particularly, polycrystalline and amorphous phases of metal nitrides, carbides,⁴¹ and borides have been a subject of interest. Amorphous ternary compounds ($M_xSi_yN_{1-x-y}$) have proved to be promising candidates as a copper barrier. Material compatibility with copper has been widely studied improving the understanding of thermodynamical stability of these compounds as well as an influence of their crystal structure to diffusion.²⁰

Tantalum nitride (TaN_x) deposited by PVD technique has been mainly the choice of industry. The PVD technique comprises relatively good methods to control N/Ta ratio. Good methods are needed since tantalum nitride has more than 11 different known phases and one of the most desirable of these phases ($N/Ta \approx 1$) is metastable.^{42, 43} However, as is the case with tantalum, tantalum nitride is stable thermodynamically with copper being an effective barrier against copper diffusion.

3.2.4. Compatibility Requirements of the Diffusion Barrier

In addition to previous film property requirements, the copper diffusion barrier process must fulfill several compatibility requirements in the process integration. Although film properties are promising, process integration may fail due to lack of compatibility of one or several subjects. Since all other process steps around diffusion barrier process are the result of extensive R&D work and financial investments, the IC manufacturers are not usually so eager to change existing processes or materials made in the processes although new diffusion barrier material would require it. There is also a risk that the changes of existing processes or materials would generate new compatibility issues in other processes, and thus escalating the problems. In other words, even one compatibility issue can be the dead-end of new interesting barrier material due to reliability/yield factors, process development time, production/sales objectives, and eventually the cost.

When diffusion barrier is deposited on patterned dual-damascene features, the film must adhere and grow at least on three different surface materials. Because the starting surface is known to be a critical factor for the film growth, the process integration is challenging. The film must grow on insulators in sidewall, etch stopper (e.g. SiN and SiC) between via and trench, and copper surface on the bottom of via. To obtain the same thickness of film everywhere, the growth rate cannot differ significantly on different materials.

When the deposition on insulator is studied, various materials must be considered including conventional silicon oxide. In addition to copper metal, the switching speed can be improved with reducing parasitic capacitance over wiring. This can be done with insulators that have lower dielectric constant than silicon dioxide ($\kappa= 3.9$), thus called as low-k materials. There are commercially available various low-k materials such as fluorine and carbon doped silicon dioxide, porous silicon dioxide, porous carbon doped silicon dioxide, organic polymers made by spin-on coating, and porous organic polymers. Fluorinated silicate glass (FSG) was the choice of Intel Corp. for 130 nm process technology node decreasing the dielectric constant to 3.6.²⁴ In the following nodes (65nm and 45 nm) their process was integrated to low-k material

called AuroraTM which is a carbon doped silicon oxide by ASM International. Carbon doping that is also carried out in Applied Materials' Black Diamond and Novellus Systems' Coral, decreases the dielectric constant down to 3.0. Spin-on coated organic polymers, for instance, polyimide, benzocyclobutene, and PTFE have not achieved as much attention as previous materials primarily because of their weak thermal stability and mechanical strength. Nevertheless, there is a significant interest for organic polymers, which, however, limits the deposition temperature of the diffusion barrier below 400 °C.

Porous low-k materials are known to bring new integration challenges: 1) the patterning of porous materials is difficult,⁴⁴ 2) the materials suffer from a low mechanical strength, 3) the depositions of the diffusion barrier and the copper seed layer on porous low-k can be problematic. If conventional diffusion barrier deposited by PVD technique is used, porous sidewalls of vias and trenches make diffusion barrier discontinuous. In other words, the CVD technique with a good surface controlled process, and particularly ALD, can offer a clear advantage when porous insulators are considered. The integration feasibility depends on shape and size of pores. Good step coverage properties of ALD technique can be a concern. The diffusion barrier film can penetrate deep into the sidewall degrading the insulator or inductively generate current to the next wire or even a short (Figure 4). Since the horizontal distance between wires is only few hundred nanometers, even minor penetration can degrade the device performance. This issue has been tried to be addressed in many different ways. One such approach has been to concentrate on engineering of pores in a way that pore size has been decreased and pores are closed forming discontinuous holes for hindering CVD precursors to penetrate into the insulator. Donohue *et al.* introduced a technique where *in situ* dry stripping is made on insulator after the plasma etching.⁴⁵ Stripping removes the photo resist and makes the sidewall of trench smoother and denser, thus providing the diffusion barrier film with no penetration. Raaijmakers *et al.* developed a method where the pores are lined in vertical direction. The pore opening on the top is closed for example by melting.⁴⁶ Another alternative method comprises the combination of the PVD and ALD methods where the PVD film is used to cover the holes prior to the ALD deposition.



Figure 4. Schematic picture of barrier penetration into the porous low-k dielectric.²⁸

In the bottom of via the barrier is deposited on underlying copper metal. Copper surface is covered by etching residues due to the via opening step. Furthermore, the surface has oxidized when it is exposed to air. Consequently, the copper surface must be cleaned prior to the barrier deposition. The etching residues are often cleaned with the Ar plasma in addition to the hydrogen plasma that is known as an effective method to remove oxidized surface.⁴⁷ After appropriate cleaning the diffusion barrier is deposited on copper. If CVD technique is used, one must ensure that the precursors used in the deposition are chemically compatible with copper as well as the by-products of the surface reaction. The adhesion on copper must be very good to make sure that the interface does not open when high current density is driven over the interface. Evidently, it would be more preferable if there is no barrier at all between copper interface, which increases switching speed and makes the circuit more vulnerable. The concept of having selective ALD deposition on the dual damascene structure where the barrier growth does not take place on the copper surface has been considered.⁴⁸ In addition to previous compatibility requirements, the diffusion barrier must be compatible with the CMP process. When surplus growth of copper on the top of trench is removed with CMP, the diffusion barrier must tolerate the process.

3.2.5. Copper Seed and Copper Metal

Electrochemical deposition (ECD) was universally chosen as a method to deposit copper. It is low temperature, acid-based, relatively simple and a cost-effective deposition method that can offer bottom-up coverage once it is well optimized. However, the ECD process requires a highly conductive starting surface to obtain uniform copper film cross the wafer. The conductive surface, called seed layer, is usually physical vapor deposited-copper (PVD-Cu) with a thickness of approximately 100 nm. Whereas ECD-Cu was seen as a method of copper filling in next design nodes, the seed layer was a subject of concerns. In order to deposit 10 nm copper on the sidewall of via, one must deposit 100 nm thick film on the top surface. Because of a non-conformal growth of PVD-Cu, there is overhang growth of the top edge of via. Thicker film on the edge causes locally higher current density in the ECD process resulting in a higher growth rate at this spot, and eventually leaving a void in the middle of the via. This subject of concern was a driving force in search for an alternative seed layer process with better step coverage properties.

Only copper metal was considered as a seed material for the ECD-Cu deposition. Low resistivity of copper offered good current distribution across the wafer minimizing “terminal effect” that is the result of lower current density in the middle wafer making the film thicker in the edge and thinner in the middle.⁴⁹ Consequently, excess copper was deposited on the edge of wafer making the copper thick enough at the middle of the wafer. The following CMP step became more challenging because more copper removal was required on the edge than the middle of the wafer. Because the cathode contacts were in the edge of wafer in the ECD process, it was clear that increasing wafer size brought more challenges for the terminal effect. In addition to low resistivity, it was obvious that copper seed layer offered the best adhesion for ECD-Cu. One additional reason why no other seed layer materials were considered was the copper interface reliability. There was a concern that the interface was not stable enough thus allowing two materials the possibility to react/diffuse with each other and cause void formation in a high current density. This concern was relevant since copper is known to react with many materials.

3.3. Atomic Layer Deposition

Atomic Layer Deposition is one of the Chemical Vapor Deposition techniques that was developed in Finland in the mid 1970s by Dr. Tuomo Suntola and his co-workers. One of the objectives in this work was to find a deposition technique which could be used to manufacture thin film electroluminescent (TFEL) flat panel displays. After extensive development work with ALD, called Atomic Layer Epitaxy (ALE) at the beginning, the technique was used in high volume manufacturing (HVM) of TFEL displays at Finlux Display Electronics, which later became Planar Systems, Inc (Figure 5). Although one of the earliest papers that describe an ALD type of a technique was published in 1965,⁵⁰ the development work that resulted in the first patent of an ALD technique was granted in the mid 1970s.⁵¹ The early phases of ALD development in Finland and Russia has been reviewed by Puurunen.⁵²

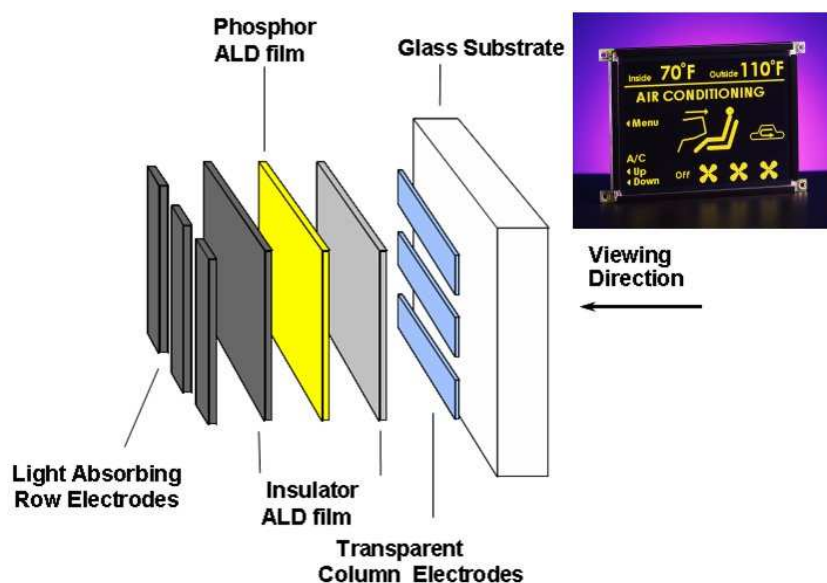


Figure 5. Electroluminescent flat panel displays of Planar Systems, Inc.

Over two decades ALD technique was hardly used for any other industrial applications. However, it obtained significant academic interest resulting in publications and Ph.D. dissertations. At the end of the 1990s the IC industry became interested in ALD as a result of shrinking feature sizes. In 2006, Intel launched HVM of the first commercial microprocessor (Intel® Core microarchitecture for a 45 nm

design node) that used high-k material deposited by ALD for the gate oxide of CMOS transistor (Figure 6). Recently, the high visibility of ALD has exponentially added interest towards the method, continuously bringing up more applications where the ALD technique could be considered for use. According to some views, the growth of interest towards ALD could even be considered "hype" since quite often production worthy techniques are still conventional deposition techniques in many applications. Increasing interest has also been seen in R&D where new ALD type of techniques have materialized as a deposition system, e.g. plasma-enhanced (PE) ALD, radical-assisted (RA) ALD.

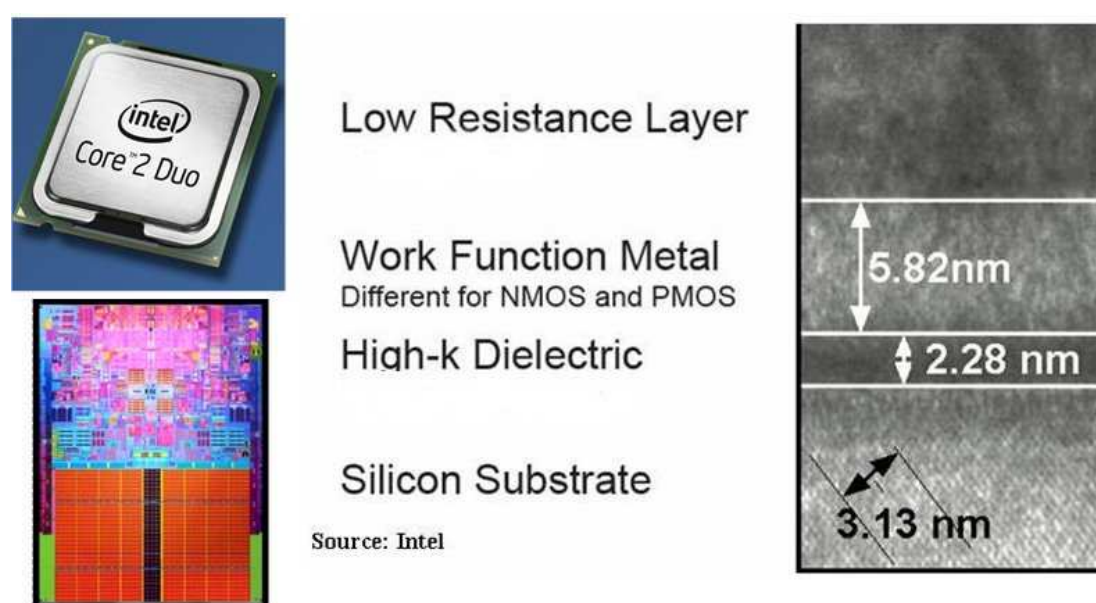


Figure 6. Intel's Core microarchitecture MPU with detailed structure of the transistor.⁵³

3.3.1. Principle of ALD

ALD is based on sequential self-saturated surface reactions, leading to the controlled layer-by-layer growth of thin film at the molecular level.^{54, 55} The ALD cycle comprises at least two material pulses with a purging pulse or evacuation step after each material pulse. Effective purging step is an absolute requirement of ALD to separate the highly reactive precursors in the gas phase. Figure 7 is often presented as

proof of ALD growth where the growth rate saturates as a function of the precursor pulse length.

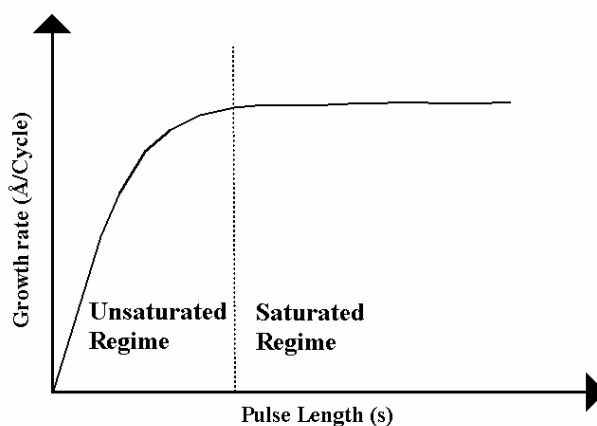


Figure 7. Characteristic curve of ALD where the growth per cycle saturates as a function of pulse length of precursor [VII].

3.3.2. ALD Deposition Equipments

Because the influence of the reactor design to the film uniformity of the diffusion barrier was studied in great detail, some background of the ALD reactor design is discussed here [VII]. Ten years ago there were only few ALD tool suppliers available whereas today there are dozens of tool suppliers and continuously more are entering to share the rapidly increasing market. Consequently, this topic has become very broad and thus it is touched here only briefly.

Since the principle of ALD supports scalability for multiple substrates, ALD reactors were based on batch processing at the beginning to improve their throughput and thus making the production of TFEL displays cost-effective. However, there were research reactors made to handle some small substrates. A need to integrate the ALD process with other process steps by the cluster system brought forth single-wafer reactors. Single wafer processing was also preferred in the IC production. The batch systems in the middle of the process flow would have increased the intermediate storage and decreased the overall yield. The batch system, however, are coming to the IC

manufacturing as a result of never-ending cost reduction. Evidently, the future of ALD processing in production use relies on the development of ALD batch reactors.

Most of ALD reactors are flow-type reactors where the carrier/purging gas is introduced over the substrate as a continuous flow. When the reactor design is good, the flow-type reactor offers an effective purging of the reactor volume making the cycle time short and throughput reasonable. There are also non-flow-type reactors available. In these reactors the substrate is exposed to the precursors while pumping and purging are stopped. The purging step in these reactors takes longer, even minutes in the worst case, and evidently the throughput suffers. Furthermore, the surface chemistry can differ between these reactor types.

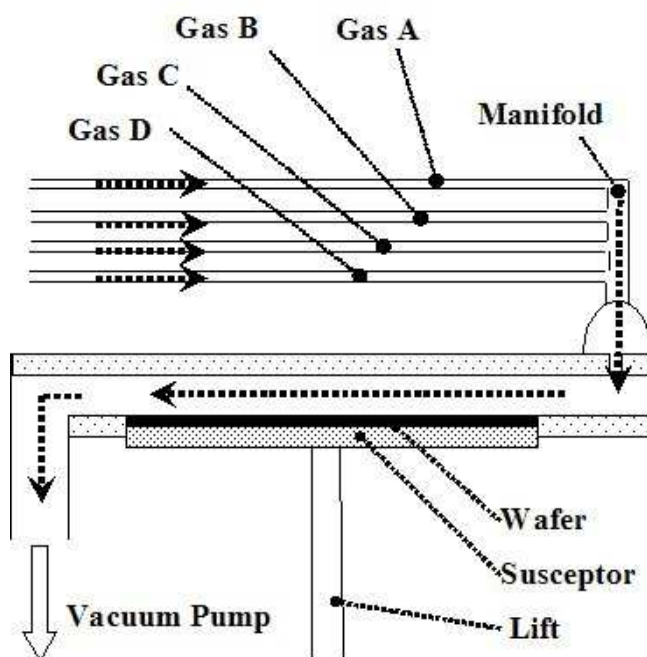


Figure 8. A schematic of the single wafer cross-flow reactor that comprises four gas inlets and a lift mechanism for the wafer transfer [VII].

When the flow is introduced to one end of the substrate and it ends up at the opposite end of substrate, the reactor is called a cross-flow reactor (Figure 8). Nearly all reactors made in the first two decades were of this type. Again, the principle of ALD offers a good explanation why the use of the cross-flow reactor in ALD should be straight forward whereas perpendicular flow is preferred in CVD. The perpendicular

flow that is often carried out with the showerhead on the top of the substrate was also implemented with ALD reactors during the 1990s. Since many traditional CVD tool suppliers began manufacturing ALD reactors, the showerhead was the obvious choice. This particular design, however, faced multiple problems. Small showerhead holes were restricting the flow such that it took very long time to purge the volume inside showerhead. If the purging was not efficient, highly reactive ALD precursors reacted in the gas phase generating particles and clogging the holes. Secondly, since CVD reactors were also traditionally cold-wall reactors, the showerhead were at significantly lower temperature than the substrate. Consequently, precursor condensation and the particle formation inside the showerhead followed. The differences of perpendicular and cross-flow are further discussed in the chapter “Film Uniformity of the Diffusion Barriers”.

3.3.3. Copper Diffusion Barrier Deposition by ALD

3.3.3.1 Titanium Nitride

The background of the ALD-TiN processes has been extensively reviewed in Juppo's dissertation⁵⁶ and Kim's review article⁵⁷. In nearly all studies ammonia was used as a nitrogen source excluding few exceptions. Titanium precursors were the following: TiCl_4 ,^{58, 59, 60} TiI_4 ,⁶¹ $\text{Ti}[\text{N}(\text{C}_2\text{H}_5\text{CH}_3)_2]_4$ (TEMAT),⁶² $\text{Ti}[\text{N}(\text{CH}_3)_2]_4$ (TDMAT).⁶³ Since it is known that tetrakis(dialkylamino)titanium compounds suffer from weak thermal stability,⁶⁴ it leaves only few options which can be seriously considered for the ALD-TiN process. Consequently, there have been more studies recently where the fundamental growth mechanism^{65, 66, 67} and the process integration⁶⁸ for some applications have been explored. Since the growth mechanism studies often require *in situ* characterization, most of the studies have been made in customized characterization system in which the precursor can be introduced in ALD manner. In other words, the films are not deposited in well designed ALD reactors. Consequently, it can be seen that the analysis of the characterization results can become quite complicated when there are for instance thermal decomposition of precursor, overlapping pulses, and impurity sources from the environment present.⁶⁷ Fortunately, there are well designed systems available nowadays where the characterization

equipment can be integrated into the ALD reactor. It is also possible to have a cluster system where the samples are transferred under vacuum between various characterization equipment and the ALD reactor.

When the TiN process from metal halides and ammonia is considered, the following overview can be made: 1) depositions are made between 300 °C and 500 °C, 2) the films are polycrystalline having columnar grain structure, 3) halide impurity level stay below 4 at.-% when the deposition temperature is above 350 °C, 4) resistivity of the film is below 500 $\mu\Omega\text{cm}$ and, 5) growth rate is 0.05-0.37 Å/cycle.

3.3.3.2. Tungsten Nitride

The ALD- W_xN processes were studied significantly less than the TiN processes prior to our studies. Tungsten hexafluoride (WF_6), used for the W_xN deposition widely in CVD, was a challenging tungsten precursor for the ALD reactors made from quartz parts. The reaction by-product, hydrogen fluoride, was an effective etching agent of quartz and caused devastating damage to the reactor. Consequently, these experiments were made in reactors with metal body.

Klaus *et al.* have published two papers about ALD- W_xN studies.^{69, 70} The film was deposited from tungsten hexafluoride and ammonia on high surface area silica powder comprising *in situ* FTIR spectroscopy studies. According to their paper and our knowledge, films were deposited in the non-flow-type reactor where the substrate is exposed to each material pulse for tens of minutes. Based on the results it has been suggested that the surface chemistry can be quite different in the flow-type and the non-flow-type reactor. However, this claim is very weakly studied and not well understood. Starting surface was very carefully treated to make Si-NH₂ terminated surface that resulted in tungsten nitride growth of ~2.5 Å/cycle at 327-527 °C. The growth rate matches that of the W_2N monolayer. Since metal nitrides deposited in flow-type-reactors usually have the growth rate far below monolayer, a high growth rate has been considered to be caused by the reactor type. The film was smooth, polycrystalline (with strong cubic W_2N peaks) with the estimated grain size of 11 nm.

The film had a low content of impurities, and its resistivity was $4500 \times 10^3 \mu\Omega\text{cm}$. The resistivity of W_xN was observed to increase drastically when the nitrogen content exceeded 32 %.⁷¹

The FTIR studies revealed that the WF_6 half-reaction left $-\text{WF}_x$ terminated surface, and the ammonia half-reaction left $-\text{NH}_2$ terminated surface. Furthermore, it was observed that the surface reaction was limited in the half-reaction of ammonia when the deposition temperature was 227 °C. Only 60 % of the $-\text{WF}_x$ species were removed in the ammonia pulse. Consequently, the nitrogen content decreased. The nitrogen content played an important role with the diffusion barrier property where the failure of barrier occurred due to the release of nitrogen when the film was heated up to 850 °C.⁷¹ In other words, the film was deposited above 327 °C to obtain the best diffusion barrier properties.

3.3.4. Seed Layer for ECD-Cu

Copper film was found to be very challenging to deposit in any Chemical Vapor Deposition methods and its good adhesion on all different surface materials in dual-damascene structure was found to be even more challenging.

The ALD-Cu deposition was extensively reviewed by Juppo.⁵⁶ All studies show a high sensitivity to the substrate material where the surface can have a catalytic influence to the film growth. The material sensitivity of the copper deposition raises a concern how the deposition can be done on several surface materials of the dual-damascene structure. Furthermore, process repeatability seems weak because some processes did not work so well in other type of reactors. Depending on whether the reactor is of flow-type or non-flow-type, difference can be seen. When metal film is deposited through the reduction of the metal precursor, the results suggest that it might be easier to deposit metals in the non-flow-type reactor. So far, ALD-Cu processes have not been proved to be production worthy.

4. Experimental

4.1. Film Growth

Most of film depositions were carried out with Pulsar[®] 2000 (for 200-mm-wafer) and Pulsar[®] 3000 (for 300-mm-wafer) reactors designed and manufactured by ASM Microchemistry Ltd. [I-IV,VI,VII] (Figure 9). Both reactors were designed for single-wafer ALD processing and they are flow-type reactors with a flow rate of 6-10 m/s. The flow is introduced cross the wafer. The operating pressure was maintained below 10 mbar with a dry pump and continuous nitrogen flow from each source line (~ 400 sccm). After reactive filtering, the impurity content of nitrogen was at the ppb level. The reaction chamber was not exposed to air between depositions. The wafer was introduced to the reactor through the load lock.



Figure 9. Pulsar[®] 2000 with stand-alone loader (left) and Pulsar[®] 3000 with Polygon[®] 8300 cluster platform (right).

Depositions were also made in a perpendicular flow reactor where the flow was introduced on the wafer through the showerhead [VII]. These single-wafer reactors for 300-mm-wafer were prototype reactors that were developed for both ALD and the PEALD processing. One reactor was manufactured by ASM Genitech Ltd. (Korea) and one by ASM Japan Ltd. The reactor of ASM Genitech was never commercialized

but a reactor type from ASM Japan, called Emerald was commercialized. The reactors were flow-type reactors where the pressure of ~ 3 torr was controlled with a throttle valve and continuous inert gas flow.

Previously mentioned reactors designed for both ALD and PEALD processing were used in the PEALD studies [VI]. 300-mm-wafer was exposed to direct plasma by exciting the plasma field between the showerhead and the wafer. The radical and ion formation were carried out using a 1 kW 13.56 MHz rf generator. Typical rf power was 100-400 W.

Copper oxide reduction experiments were made in a flow-type ALD reactor (model F-120) manufactured by ASM Microchemistry, Ltd [V]. The reducing agent was introduced with nitrogen gas over substrate as a continuous flow opening an isolation valve between the substrate and the source. The process temperature was controlled within an accuracy of ± 2 °C and the pressure of the reaction chamber was 5-10 mbar.

4.2. Film Characterization

In publications I-VI different characterization methods were employed and therefore the methods are described separately for each publication:

[I]: 1) Sheet resistance was measured by a four point probe, 2) transmission electron microscopy (TEM), 3) x-ray photoelectron spectroscopy (XPS), and 4) Rutherford backscattering spectroscopy (RBS).

[II]: 1) Wide angle XRD patterns were obtained using a Siemens D500 instrument equipped with a Ni-filtered Cu tube anode, and a scintillation detector, 2) Jandel's four-point probe was used for resistivity measurements, 3) film thickness, impurity content and pitting pictures were obtained using a Link ISIS energy dispersive X-ray spectrometer connected to a Zeiss DMS 962 scanning electron microscope (SEM), 4) high aspect ratio SEM images were taken by a Philips XL30 SEM.

[III]: Following characterizations were made: 1) sheet resistance uniformity, 2) film stress, 3) adhesion, 4) roughness, 5) composition analyzed by EELS, 6) step coverage was seen in the TEM images, and 7) cross-section pictures were made with FIB-SEM.

[IV]: 1) Jandel's four-point probe was used for resistivity measurements, 2) film thickness, impurity content and pitting pictures were obtained using a Link ISIS energy dispersive X-ray spectrometer connected to a Zeiss DMS 962 scanning electron microscope (SEM), 3) SEM images of the copper surface were taken by a Philips XL30 SEM, 4) TEM pictures were taken with an FEI Tecnai 12 working at 120 kV acceleration voltages, 5) TEM cross-section pictures of TiN film and $\text{WN}_x\text{C}_y/\text{TiN}$ film stack were obtained with a Philips CM30 operating at 200 kV acceleration voltages, and 6) Auger analysis of the nanolaminate structure was done with a Scanning Auger Microprobe PHI-4300.

[V]: Time-of-flight elastic recoil detection analysis (TOF-ERDA) was used in copper oxide reduction studies to measure the reduction efficiency. TOF-ERDA is an ion beam method in which the high-energy heavy ions ($53 \text{ MeV } ^{127}\text{I}^{10+}$) are used as projectiles which hit the sample and generate forward recoil sample atoms.⁷²

Resistance measurements were made with a simple setup where only major differences were measured. Resistance was measured with a Hewlett-Packard 34401 A multimeter.

[VI]: 1) Sheet resistance of 300 mm wafers was measured with a CDE Resmap using 49 points circular map with 4 mm edge exclusion, 2) film composition, thickness, and impurities were characterized by X-ray reflectometer (XRR), RBS, X-ray photoelectron spectroscopy (XPS), and energy dispersive spectroscopy (EDS), 3) film thickness, density and roughness of PEALD-TiN samples were analyzed with Panalytical X'pert PRO MRD model PW/3040, 4) RBS measurements were made with 2-MeV $^4\text{He}^+$ ions, and 5) SEM images of PEALD-TiN were made with field-emission-(FE)SEM, JEOL 890, operating at 10 keV.

In all studies thermodynamic calculations were made using various software versions of the HSC Chemistry for Windows (Outotec Oy).

5. Results

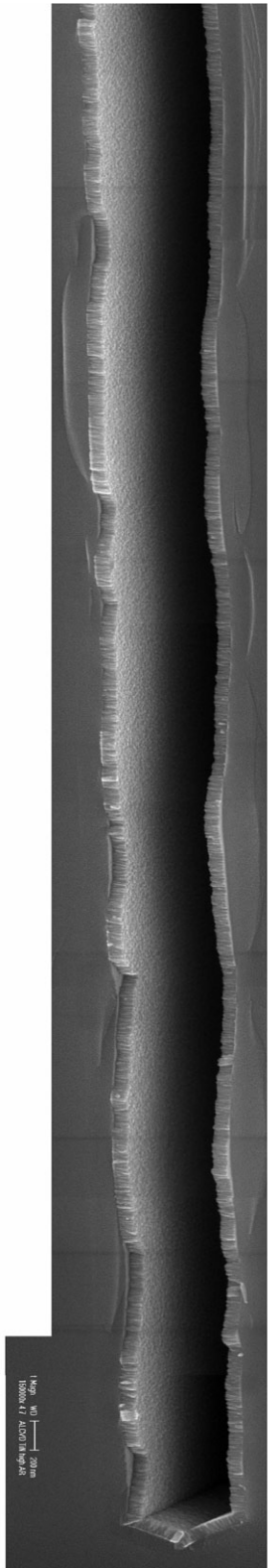
In the following chapters the results of this work are reviewed. Comprehensive understanding of experiments and the results can be obtained from corresponding papers [I-VII].

5.1. Copper Diffusion Barrier Deposition

5.1.1. Deposition of TiN Film

Titanium nitride films were deposited with a well-known process where TiCl_4 and ammonia are used as precursors.^{58, 59} Titanium tetrachloride is an attractive precursor because it is thermally very stable, it is liquid, and it has relatively high vapor pressure at room temperature. The surface saturation of TiCl_4 on the substrate can be obtained even with 50 ms pulse time that is close to maximum operation speed of commercial pulsing valve. However, the vapor pressure is not so high as to require cooling of the source. In other words, the precursor is ideal for ALD in many point of view. Nevertheless, TiCl_4 requires careful handling because it reacts aggressively with the moisture of air forming hydrogen chloride gas that is dangerous and highly corrosive for the reactor hardware.

Titanium nitride films were deposited at 300-400 °C using nitrogen as a carrier and purging gas with an overall flow of ~400 sccm. The growth rate was as low as previously reported (0.17 Å/cycle) at 400 °C, which was a concern to obtain a reasonable throughput in the TiN process. When the deposition temperature was lowered to 300 °C, the growth rate decreased linearly down to 0.12 Å/cycle. The film was close to stoichiometric, its composition being slightly nitrogen rich (N:Ti = 1.16). Oxygen and carbon residues were found only on the surface. The chlorine residue content was 1.2 at.-% when deposition temperature was 400 °C and increased when temperature was lowered being already 7.0 at.-% at 300 °C.



Films were polycrystalline and continuous in the deposition temperature range. Even though the grains were very closely packed, there was a clear columnar grain structure. The grain size was 15-20 nm. Film density was high, (10.8×10^{22} at./cm³) close to the bulk density, which was suggesting very narrow boundaries.⁷³ When the film was deposited in ultra high aspect ratio trench where the aspect ratio was as high as 85, the film growth took place with nearly 100 % step coverage (Figure 10), which is a characteristic for the ALD growth.

Film resistivity was below 200 $\mu\Omega\text{cm}$ when the deposition temperature was 400 °C. However, resistivity was drastically increasing when film thickness was less than 20 nm. The sample with 5 nm thick film had resistivity already as high as 790 $\mu\Omega\text{cm}$ [III]. Rapid change in electrical properties was the result of the mean free path of conductive electrons. When film thickness became less than the distance of grain boundaries, the change was rapid.

Films deposited at 350-400 °C were very smooth (RMS: 3-5 Å) but exhibited slightly high intrinsic stress. Tensile stress of ~ 1.4 GPa was measured as a wafer bowing for ~ 5 nm thick film. Adhesion on silicon dioxide was found to be good with a simple Scotch tape test. Adhesion was also tested on silicon dioxide and copper with a 4-point bend technique that showed 60-25 J/m² (to SiO₂ – to Cu) [III].

Generally, it can be concluded that the ALD-TiN process is a quite simple when TiCl₄ and NH₃ are used as precursors. Since the process suffers from relatively low growth per cycle, the deposition tool must be well designed to ensure the shortest possible cycle length. Furthermore, when the tool is well designed, there are no contamination problems in the TiN film. The challenges of the process integration are discussed in the following chapters.

Figure 10. ALD-TiN deposited into ultra high aspect ratio trench (AR=85). Picture shows the bottom of trench.

5.1.1.1. *In situ* Reduction of TiCl_4

A deposition technique that doubled the growth per cycle of the ALD- TiN film was developed.⁷⁴ The technique was based on *in situ* reduction of TiCl_4 when it was introduced to the reaction chamber. Titanium tetrachloride became reduced before being chemisorbed on the substrate when it was exposed to titanium metal at moderate temperature. Figure 11 shows a schematic concept of the ALD- TiN process with an *in situ* reduction of TiCl_4 .

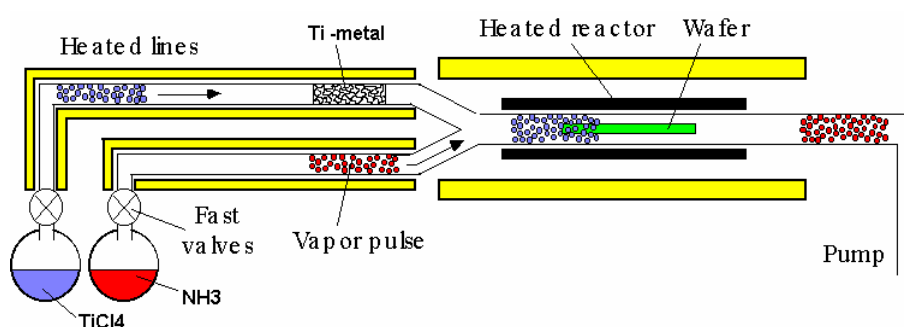


Figure 11. Schematic picture of *in situ* reduction process of ALD- TiN in cross-flow reactor.

The growth rate of TiN was $\sim 0.35 \text{ \AA/cycle}$ when the deposition temperature was 400°C . Growth rate decreased linearly with temperature such that it was $\sim 0.30 \text{ \AA/cycle}$ at 350°C and $\sim 0.15 \text{ \AA/cycle}$ at 300°C . In other words, the difference in growth rate between standard and *in situ* processes became smaller at lower temperature. No differences were found in the chlorine residue content between standard and *in situ* processes. The content was approximately the same at $300 - 400^\circ\text{C}$. When the deposition temperature was lowered the change of content was more linear in the *in situ* than in the standard process (Figure 12). No differences were found in electrical properties.

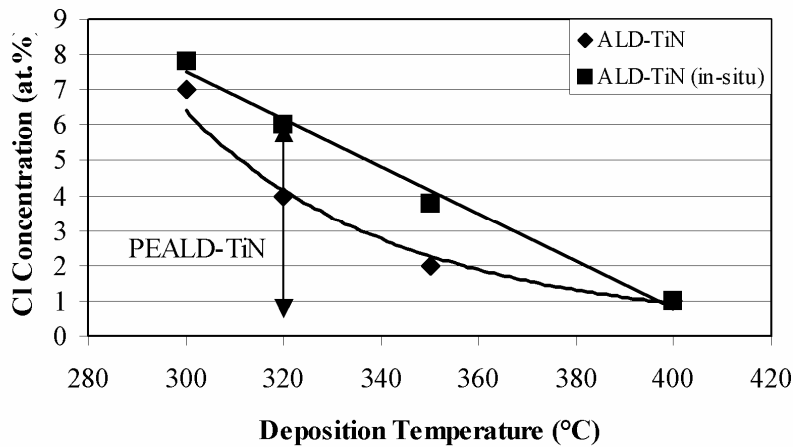


Figure 12. Chlorine content in TiN film versus deposition temperature.

No further studies were made to understand the fundamentals of the mechanism of increased growth rate. However, the mechanism was speculated with thermodynamic calculations. Change in the growth rate was believed to occur via titanium trichloride (TiCl_3) [1] and/or dimeric, dititanium hexachloride (Ti_2Cl_6) [2] formation on the hot titanium metal surface. Additional calculations also suggested that both TiCl_3 and Ti_2Cl_6 could be more reactive with ammonia than TiCl_4 .



There was no commercial interest for this technique and consequently no further development or studies were done. However, the technique was easy and the depositions were repeatable. Hopefully, there will be further studies made in the future.

5.1.1.2. Comparison of ALD- and PEALD-TiN

The PEALD studies are out of scope of this thesis. The topic of PEALD or RE (radical enhanced) ALD is extensive and comprises multiple dissertations itself. If the

reader is interested in this topic, following references can be recommended.^{75, 76} However, the results of TiN film deposited from direct plasma with the results of TiN films deposited from a conventional ALD are compared here [VI].

PEALD-TiN films were deposited at 270-370 °C using N₂ (10 sccm) and H₂ (100 sccm) radicals and TiCl₄. The growth rate of PEALD-TiN was 0.30 Å/cycle at 320 °C that is nearly three times higher than that of conventional ALD-TiN at the same temperature (Figure 13). It was also observed that growth per cycle was very linear from at the very beginning in the PEALD process, which suggests that reactive N*/H* species could modify the reactive sites of the substrate.

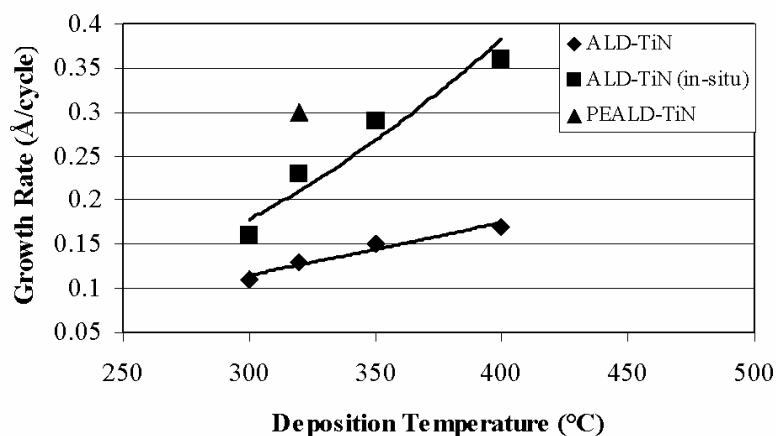


Figure 13. Growth rate in three different TiN processes between 300 and 400 °C.

Generally, the composition of ALD film (N:Ti = 1.16 at 400 °C) cannot be adjusted with the pulsing parameters, but in the PEALD process the film composition was possible to be adjusted with the plasma power. When the plasma power was 100 W, the N:Ti ratio was ~0.92 and it went up to ~1.1 if the power was increased to 400 W. Slight saturation in the film composition was observed if the power was increased more. Plasma pulsing parameters were also possible to use for controlling chlorine content in the film. Both the rf power and the rf pulse length changed the Cl content. When the film was deposited at 320 °C, rf power was 200 W, and rf pulse length was 6 s, the Cl content was as low as ~0.5 at.-%. If the rf pulse length was 1 s, Cl content went up to ~5.8 at.-%. Results suggest that the reaction kinetics is slow at 320 °C, and long plasma exposures are required to complete the surface reaction.

The surface roughness of PEALD-TiN film was measured with XRR and AFM. PEALD-TiN seemed to be rougher than ALD-TiN. When the ALD-TiN film was 5 nm thick, RMS roughness was ~ 4 Å. Correspondingly, RMS for PEALD-TiN film was ~ 13 Å. The roughness of the PEALD-TiN film increased linearly, and RMS roughness was already ~ 25 Å for 80 nm thick film. PEALD process was assumed to be more aggressive to the surface than a conventional ALD process promoting rougher surface of the PEALD film.

The resistivity of the PEALD-TiN film was below $150 \mu\Omega\text{cm}$ when film thickness was above 30 nm and the film was deposited at 320°C . Resistance of PEALD-TiN film saturated already with rf pulse of 2 s when rf power was 200 W. In other words, the conductivity of the film was not limited by the chlorine residues when the content was below 3 at.-%. Grain boundary scattering was expected to limit conductivity for both PEALD- and ALD-TiN films.

5.1.2. Deposition of W_xN Film

Tungsten nitride film was deposited from tungsten hexafluoride (WF_6) and ammonia at 350°C [II, IV]. Growth rate was high (0.42 Å/cycle) compared to TiN. The film was polycrystalline comprising WN and W_2N phases exhibiting columnar grain structure. W:N ratio was found to be 1.62, which supports the previous observation about the mixture of phases. Although fluorine residues from WF_6 were only 2.4 at.-%, resistivity was as high as $4500 \mu\Omega\text{cm}$, which is far above the acceptable value of $500 \mu\Omega\text{cm}$. Evidently, the resistivity of W_xN is not limited by halide residues but rather by the high oxidation state of tungsten.

5.1.3. Deposition of WN_xC_y Film

High resistivity of W_xN and its suggested source was a driving force to introduce the third precursor for the reduction of tungsten. Triethylboron ($\text{B}(\text{C}_2\text{H}_5)_3$), TEB, was

used as a reducing agent. It is a liquid and has relatively high vapor pressure such that no extra heating is needed. TEB was pulsed after the WF_6 pulse at the beginning but it was soon noticed that the process was more copper compatible when TEB was pulsed after the ammonia pulse. Thus, the pulsing sequence of $\text{WF}_6/\text{NH}_3/\text{TEB}$ was chosen.

Depositions were made at 300-350 °C where TEB did not decompose yet. Although it was expected that no atoms of TEB would incorporate to the deposited films, a significant amount of carbon was found. The XPS studies revealed the composition of W:N:C to be 55:15:30. The XRD studies suggested that carbon is bound in the form of metal carbide.⁷⁷ The W:N:C ratio was almost constant when the deposition temperature was varied between 275 °C and 350 °C. The growth rate of the film was approximately 0.8 Å/cycle when deposition temperature was 300-350 °C. Fluorine content was below 1 at.-%, no boron was found in the film, and the oxygen residues in the film bulk were less than 1 at.-% indicating good barrier properties against oxygen diffusion. Figure 14 depicts the content of oxygen and fluorine when deposition temperature is varied between 225 °C and 400 °C.

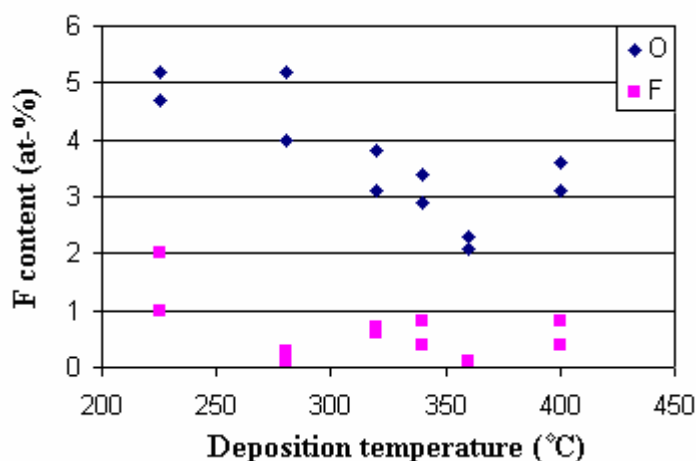


Figure 14. Fluorine and oxygen content in WN_xC_y films.

The N:C ratio was possible to adjust slightly with TEB and ammonia pulses, which also changed electrical properties of the WN_xC_y film. It was noticed that elongation of the TEB pulse decreased resistivity whereas the elongation of ammonia pulse increased resistivity. Using optimal pulsing parameters resistivity was as low as 210

$\mu\Omega\text{cm}$, which offered further proof that carbon was not present as an impurity in the film. When film thickness was reduced to 7 nm, resistivity went up to 600-900 $\mu\Omega\text{cm}$. A similar observation was made with the TiN film when film thickness was below 20 nm [III].

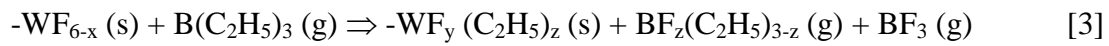
5.2. Process Integration

5.2.1. Barrier Compatibility with Copper and SiO₂

No compatibility issues were found in the deposition of TiN on the SiO₂ surface. When TiN was deposited on ECD-Cu, extensive pitting was found on the copper surface. The holes on the copper surface had the diameter of $\sim 1\ \mu\text{m}$ and their density was quite high ($\sim 1\ \text{hole}/17\ \mu\text{m}^2$). The pitting took place in a wide temperature range, from 250 °C to 400 °C. Regardless of pitting, film growth on copper occurred with normal growth rate. Since the source of pitting was unknown, the copper surface was exposed separately to both precursors (TiCl₄ and NH₃) to see whether the precursors themselves caused the damage. No pitting was observed and it was speculated that pitting must be caused by the reaction by-products of the TiN growth, namely HCl gas that is known to be highly corrosive.

The deposition of W_xN was found to be problematic on both SiO₂ and the copper surface. In the ALD process, the substrate is exposed to the precursor for a relatively long period of time until the surface is fully covered by deposited film. Consequently, surface materials must be compatible with the precursors. When WF₆ is introduced on a native SiO₂, it is possible that volatile WOF₄ is formed. As soon as the native oxide layer is consumed, WF₆ reacts with the silicon surface giving rise to volatile SiF₄, which results in so called “worm holes” on the silicon surface. The copper pitting was also observed in the W_xN process although it was not as aggressive as in the TiN process. It was observed again that the pitting was not caused directly by the precursors. The HF by-product was suggested to be the source of pitting.

WN_xC_y process exhibited a good compatibility on both SiO₂ and copper surfaces. Since the same tungsten precursor was used in the W_xN deposition, two of explanations can be considered so as to find why the “worm holes” were not observed on the SiO₂ surface: 1) The growth rate of the WN_xC_y film is twice as high than that of the W_xN film. Consequently, the WN_xC_y film covers the substrate faster and shortens the time when the substrate is exposed to WF₆. 2) The worm holes are created by the HF by-product that is formed with a lower content in the WN_xC_y process than in the W_xN process. The copper compatibility was also explained with the HF formation, which was believed to be minimized when TEB was used as a reducing agent [3]:



5.2.3. Deposition of W_xN/TiN and WN_xC_y/TiN Nanolaminates

A method of using WN_xC_y film as a protective layer of copper for TiN deposition was tested. When the WN_xC_y film was approximately 40-Å-thick, no copper pitting occurred after TiN deposition. The pitting came gradually back if the thickness of WN_xC_y film was reduced.

Dual layer structure was extended to the multilayer structure. One reason for this approach was a concern of columnar grain structure of TiN and W_xN films. Since the grain boundaries are the most probable diffusion paths of copper, neither TiN or W_xN films looked promising diffusion barriers. The idea of multilayer structure was based on discontinuous grain boundaries that might be the result of interrupted film growth by chancing deposited materials. If the grain boundaries were not continuous, they would generate more complicating diffusion paths for copper and thus become better diffusion barriers. Two different types of nanolaminate film stacks were deposited:

- (1) TiN (10 nm) + 8 x (W_xN (2 nm) + TiN (2 nm)) + TiN (10 nm)
- (2) 9 x (WN_xC_y (2 nm) + TiN (2 nm))

Figure 15 shows stack number one which was deposited at 360 °C. Film resistivity was approximately 600 $\mu\Omega\text{cm}$ and the fluorine and chlorine residues were 2.6 at.-% and 2.4 at.-%. The resistivity of stack number two was 1420 $\mu\Omega\text{cm}$ when the film was deposited at 350 °C. Correspondingly, fluorine and chlorine residues were 2.5 at.-% and 0.1 at.-%. Continuity of grain boundaries was difficult to conclude from TEM cross-section images.

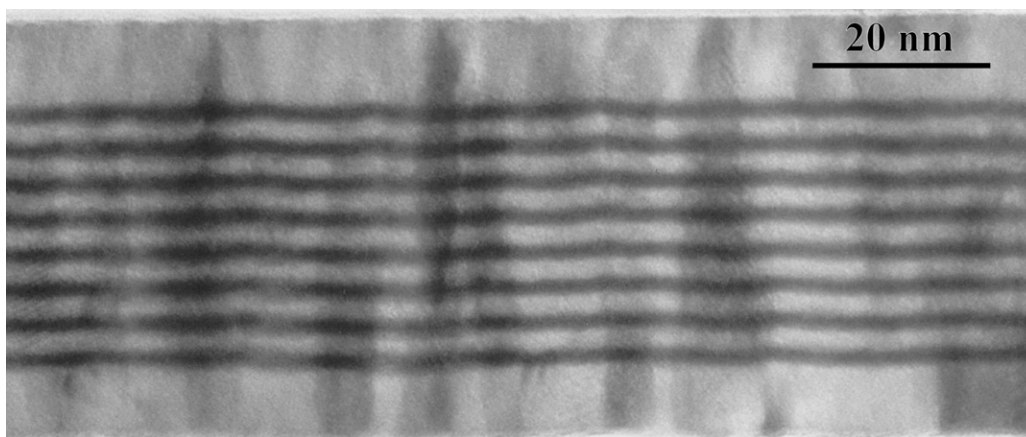


Figure 15. Nanolaminate film stack of TiN (10 nm) + 8 x (WxN (2 nm) + TiN (2 nm)) + TiN (10 nm).

5.2.4. Compatibility of TiN with Low-k and an Etch Stopper

TiN barrier was deposited on low-k insulator which was a carbon doped silicon oxide called Aurora® (ASM International) and trimethylsilane (3MS) based low-k [II]. Integration was done on a single damascene scheme. The barrier was also deposited on SiC that can be used as an etch stopper in the copper metallization. When TiN film was deposited on low-k insulator at 400 °C, continuous film growth did not occur. Some individual islands were possible to observe reminding more or less particle formation. The low-k material (Aurora®) was known to have a carbon content of 20% making material more hydrophobic and less favorable of having hydroxyl groups on the surface. Since the surface did not have any alternative reactive sites for the chemisorption, the ALD-TiN growth did not take place. Observed particle formation can be a result of locally oxidized sites.

The surface of Aurora® was made more favorable for having hydroxyl groups with oxidizing the surface. Oxidation was carried out with two different types of plasma treatments. The first treatment consisted of high concentration of oxygen in O₂/N₂ plasma. The second treatment consisted of Ar/C₄F₈/O₂ followed by a low concentration of oxygen in the N₂/O₂ plasma. The first treatment (30 s and 120 s) was made at high temperature and high pressure, and the second one was made at low temperature and low pressure.

The treatments were successful in the formation of hydroxyl groups. The TiN growth was very similar on the low-k material as it was on SiO₂ exhibiting equivalent resistivity values. However, differences were seen in film density. Whereas density of the TiN film on SiO₂ (PECVD) was 10.8×10^{22} at./cm³ it was only $\sim 7.3 \times 10^{22}$ at./cm³ on plasma treated low-k material. The difference was explained with the low density of the low-k material, which was a result of carbon removal in the plasma treatment.

Although the hydroxyl group formation was successful and the TiN growth took place, a significant disadvantage was seen in the process integration using the oxygen plasma treatment for oxidation of the low-k surface. It has been observed in many occasions that the plasma species have a tendency to penetrate deeper into the lattice. Consequently, the oxidation occurs also below the surface. In these experiments the oxidized layer was 100-350 nm thick even though the shortest treatment was only 30 s. In the oxidized layer carbon content was below 1 at.-% and the composition corresponded SiO₂ (33 at.-% Si and 67 at.-% O). In addition to changes in the film composition, film thickness of low-k material was significantly reduced and the film density increased due to the plasma treatment. A composition change causes the increase of k-value, and the shrinking changes the surface feature dimensions. Neither one of these issues cannot be accepted in the process integration. When the plasma treatment was made with a low oxygen concentration, only few nanometer thick oxidized layer and no shrinking of the low-k material were observed. In other words, when the process is well optimized, plasma treatment could be an acceptable option.

The TiN growth on SiC was good even without plasma treatment. This was most probably caused by the oxidation of SiC surface at ambient air. However, plasma treatment of SiC slightly improved film resistivity. Film density of TiN was approximately as high as on the low-k material after the plasma treatment. Nevertheless, based on this study there was no particular advantage to introduce plasma treatment for SiC. Integration on single damascene scheme was successful. TiN film was deposited on the SiC, Si-O-C, and SiO₂ side walls of the dielectric stack.

5.2.5. TiN and WN_xC_y Films in Dual-Damascene Structure

Barrier integration was tested with the dual-damascene structure and Kelvin via resistance, via chain resistance, leakage current, and line resistance was also measured [III]. Since the barrier thickness was only 5-7 nm, resistivity was relatively high. However, with regard the device, the vertical conductivity over barrier is playing more important role than the resistivity. The via resistance on the actual device was much lower than that of PVD-Ta. The WN_xC_y film (~50 Å) exhibited about half of the via resistance of PVD-Ta (>250 Å) being below 0.5 Ω in 0.25 μm via. The yield of 9000 vias in chain was excellent.

When the TiN film was deposited on the dual-damascene structure followed by copper metallization, a void formation took place in the copper via and the underlying copper layer. It was suggested that the void formation occurred due to the copper pitting observed in the TiN process. Whether these two phenomena are connected to each other, cannot be concluded with certainty. However, a similar issue was not observed with the WN_xC_y process where nearly 100 % step coverage was possible to observe by TEM.

The Biased Temperature Stress (BTS) studies of TiN showed good leakage current properties after the test structure was stressed in 2 MV/cm at 200 °C for various periods of times. Failure analysis showed that breakdown eventually occurred at the interface between the SiO₂ dielectric and the passivation layer. In other words, the

breakdown was not the result of copper-contaminated dielectric and thus, it was concluded that TiN was an effective barrier against copper diffusion in stressed conditions and the BTS performance was comparable to that of PVD-Ta.

5.2.6. Film Uniformity of the Diffusion Barrier

Although film uniformity is less of a concern in R&D, it is often one of the most employing factors of Process Engineers in the production, and consequently, a major concern of the scalability of a reactor [VII]. The principle of ALD offers a good explanation why good uniformity of the ALD film should be characteristic property and relatively easy to scale up for larger substrate size. In practice, it has been often proved to be so. For example, ALD processes have been used to manufacture thin film electroluminescent (TFEL) flat panel displays which can reach the size of about 2000 cm².⁷⁸ When glass substrates are processed in batches of 42 pieces, the overall surface area to be coated in one run is 8.4 m². Silicon wafers can also be coated in batch reactors that are commercially available for the IC industry. These reactors can be used for 300 mm wafers and more than 100 wafers can be processed in one run coating about 20 m² of the flat surface. When the wafer surface have deep trenches, the area to be coated can easily become hundreds of square meters. The most extreme examples can be found from catalytic applications where the ALD films are coated on porous high surface area silica powder. In these substrates the surface area easily reaches the size of football field in few grams of powder. However, the film uniformity in the flat surface and powder cannot be compared so easily. Nevertheless, the ALD method is evidently easier to scale up for larger substrates and the batch processing than the PVD or CVD methods.

Most ALD studies are based on small research reactors where the substrate size is less than 100 cm². Even if small reactors and small substrates are used, an ALD reactor must fulfill certain design rules to produce acceptable ALD growth. Although film uniformity might be difficult to analyze from a small substrate, the non-functionality of the reactor can often be seen in other film properties which are the result of partial CVD growth. When the reactor and substrate sizes are increased, the influence of the reactor design becomes more detectable as a non-uniform film.

The most usual sources of non-uniformity are: 1) overlapping material pulses, 2) non-uniform gas distribution, and 3) thermal self-decomposition of the precursor. Overlapping material pulses is a result of simultaneous presence of more than one precursors in the gas phase near the substrate. This can cause CVD-type of growth locally in some areas of the substrate making film thicker there than true ALD growth. There are several hardware-related possible reasons for overlapping pulses such as: a) dead gas pockets, b) bad location of pulsing valves, c) too low temperature in the reaction chamber and the source delivery lines, d) oversized reaction chamber, e) insufficient pumping, and f) degassing from the source delivery line.

Non-uniform gas distribution becomes a problem only if some areas of substrate are not exposed to all different precursors. Because precursors are often introduced to the reaction chamber from individual source delivery lines, and the lines are brought together to a common in-feed line prior to the substrate, the flows can set up a diffusion barrier for the precursor flowing from a different precursor delivery line. Without appropriate gas mixing in common in-feed line prior to the substrate, film uniformity can degrade and be non-characteristic for the gas flow pattern (Figure 16).

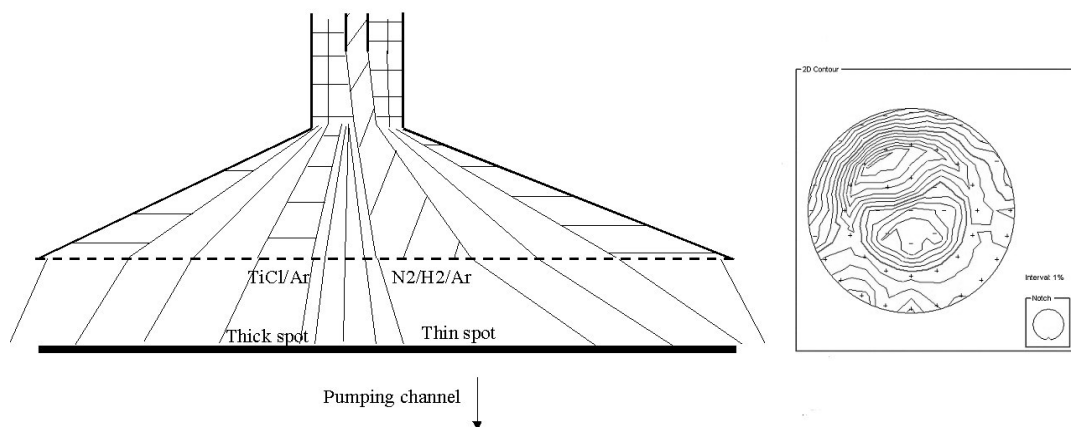


Figure 16. A schematic of the showerhead reactor where inadequate gas mixing causes non-uniform precursor distribution in the PEALD-TiN film (left), which results in an abnormal sheet resistance uniformity on a 300 mm wafer (right).

Thermal self-decomposition is a subject of concern particularly when organometallic and metal-organic compounds are used. Generally, these compounds often begin to decompose at 200-400 °C which is also the desirable deposition temperature. Despite the fact that these precursors are often thermally unstable, they have very attractive properties such as high vapor pressure, non-corrosive nature including their by-products of the surface reaction, and high reactivity. Nevertheless, most of earlier ALD studies were made with transition metal halides because of their good thermal stability.

Earlier studies of ALD-TiN were based on small substrates ($<100\text{ cm}^2$). According to our knowledge, one of the first experiments to deposit ALD-TiN on a 200 mm and 300 mm silicon wafers were made as a part of this work. These studies were made in flow-type cross-flow reactor where the carrier/purging gas is introduced over the substrate as a continuous flow. Uniform gas distribution in the cross-flow reactor was made with a hole plate that acts like a two-dimensional showerhead. Thus, the gas distribution is based on an increased pressure region upstream from the plate.

The TiN films exhibited a non-uniformity of the magnitude of $\sim 10\%$ (standard deviation, 1 sigma) on a 200 mm wafer, and $\sim 10\text{-}13\%$ on a 300 wafer at the very beginning of the studies. Non-uniformity took place in flow direction in a manner that the leading edge was thicker and the back-end of the wafer was thinner, however, being symmetrical in perpendicular to the flow direction. Although the magnitude of non-uniformity was not excessive, it was significantly (about 2-3 times) higher than any transition metal oxide films deposited on wafers of these sizes at the same reactor. Extensive R&D work was made to isolate possible hardware related reasons for the film non-uniformity. Like transition metal oxide studies at the same reactor already suggested, no reasons were found which could cause the film non-uniformity. The chemistry of TiN process was suggested to be the source of non-uniformity.

A concept was considered where the by-products of the surface reaction may interact with the surface,⁷⁹ and thus the role of by-products could become more important with increasing substrate size. The concentration of by-product increases in the direction of flow in the cross-flow reactor, which could explain the form of non-uniformity.

However, it was not understood why the chemistry of $\text{TiCl}_4/\text{NH}_3$ was so different resulting in significantly worse uniformity than other processes. The HCl gas forms during both precursor pulses when the deposition temperature is below $300\text{ }^\circ\text{C}$.⁸⁰ Figure 17 shows a series of possible surface reaction mechanisms that depict so called poisoning phenomenon in the cross-flow reactor. The HCl formed during the TiCl_4 pulse can react with reactive sites in downstream direction of the substrate. Chlorinated sites remain inactive towards subsequent TiCl_4 molecules, and will not be activated until the next NH_3 pulse. In addition to poisoning phenomenon [4], it was also considered whether HCl could etch the TiN film, which seemed to be possible based on thermodynamic calculations [5].

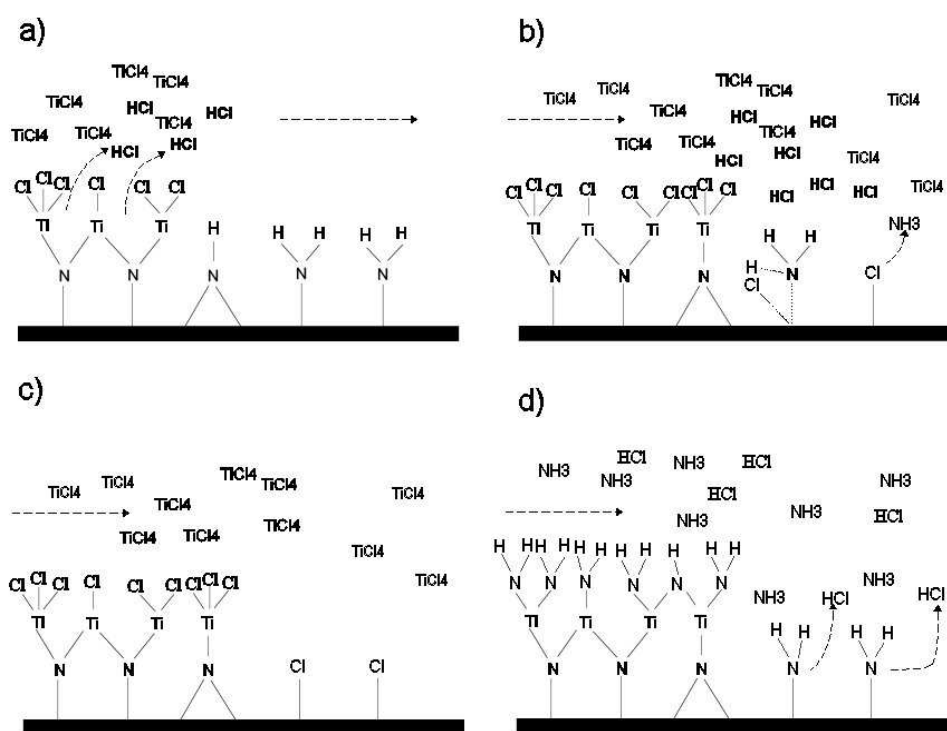
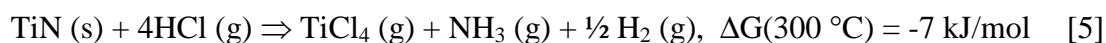
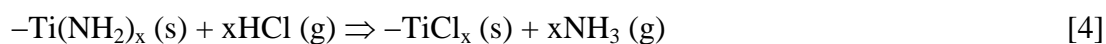


Figure 17. Non-uniformity caused by HCl formation: a) HCl formation during the TiCl_4 pulse occurs via surface reaction between TiCl_4 and $-\text{NH}_x$ sites. b) Partial pressure of HCl increases in the flow direction and HCl reacts with active $-\text{NH}_x$ sites. c) Chlorinated surface remains inactive to TiCl_4 . c) Chlorine is replaced by active site during the next NH_3 pulse.



Assuming that TiCl_4 and HCl are competing molecules to react with $-\text{NH}_2$ sites, it would be important that the HCl concentration was the same cross the wafer to obtain uniform film. Furthermore, it would be important that as many TiCl_4 molecules as possible reach the $-\text{NH}_2$ site prior to the HCl molecules to decrease the number of poisoned sites and thus improve the growth rate of the TiN film. This theory was possible to study by the showerhead reactor (Figure 18) where the perpendicular flow to the wafer was introduced from the sources through the showerhead holes making the HCl concentration even cross the wafer. In the showerhead reactor, the film uniformity of TiN was repeatedly below 2 % (standard deviation, 1 sigma) on 300-mm-wafer. Furthermore, the growth rate was as high as 0.30 \AA/cycle whereas it was only 0.17 \AA/cycle in the cross-flow reactor. This could be explained with the temperature of the showerhead which was significantly lower (at $100\text{-}150^\circ \text{C}$) than the flow channels in the cross-flow reactor (at $\sim 300^\circ \text{C}$) resulting in less HCl prior to substrate.

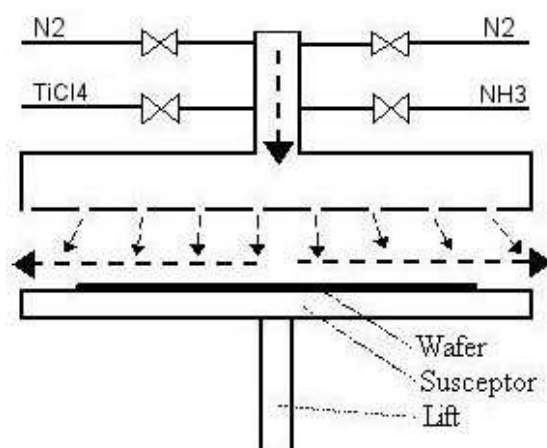


Figure 18. The schematic picture of a showerhead reactor for a 300 mm wafer.

Whereas the TiN film suffered from non-uniformity, the WN_xC_y film exhibited excellent uniformity (1-2 %) on 300-mm-wafer in both cross-flow and showerhead

reactors [IV]. Consequently, it can be assumed that in WN_xC_y process interaction of the film surface and the by-products is very weak.

5.3. Reduction of Copper Oxide Film to Elemental Copper

The basis for this ALD-Cu process was an assumption made in 1999. In this assumption it was speculated that ALD-Cu deposition most probably cannot become a production worthy process. Although some ALD-Cu studies were made, scalability to other systems was suffering and the process parameters (like minutes of cycle time) were far from the expectations for production use. Earlier experience of production worthy processes had shown that the process must possess high robustness from the very beginning.

Although the industry was not ready to consider other than copper metal as a seed layer that time, alternative materials were already considered in year 2004. Feasible ALD processes were developed for noble metals.⁸¹ Particularly, ruthenium metal was found to improve the adhesion of copper.^{82, 83} Ruthenium was considered as a seed layer and even as a copper diffusion barrier.

Alternative methods were looked for to deposit copper metal. Based on the fact that there were several metal oxides made successfully by ALD including copper oxide,^{84, 85} we were considering an option to deposit copper metal through the reduction of Cu_xO .

However, it was clear that the method can only be successful if there was a good reduction process available. It was also speculated that the oxidation of barrier may occur in the copper oxide deposition. Four specifications were set for the reducing agent: 1) it must be capable of reducing thick copper oxide film without etching it, 2) it must be capable of reducing Cu_xO below 400 °C to meet the compatibility requirements of the low-k process, 3) it should have favorable vapor pressure, and 4) it should be safe and easy to handle. In addition to our primary object, we identified a possibility to develop new, non-plasma process step for Cu_xO reduction [V].

Studies were very simple; at first the ECD-Cu samples were oxidized in the convection oven, and then these samples were exposed to various reducing agents in a vacuum chamber at elevated temperature. The success of reduction was characterized with time-of-flight elastic recoil detection analysis (TOF-ERDA) and electrical resistance measurements.

Reducing agents such as methanol, ethanol, isopropanol, tert-butanol, butylaldehyde, acetone, formic acid, and acetic acid were tested with changing duration of the reduction and the process temperature. The diffusion of oxygen in copper lattice was found very intense. The film oxidized in less than one minute in the depth of 300-400 nm forming a Cu_2O film.

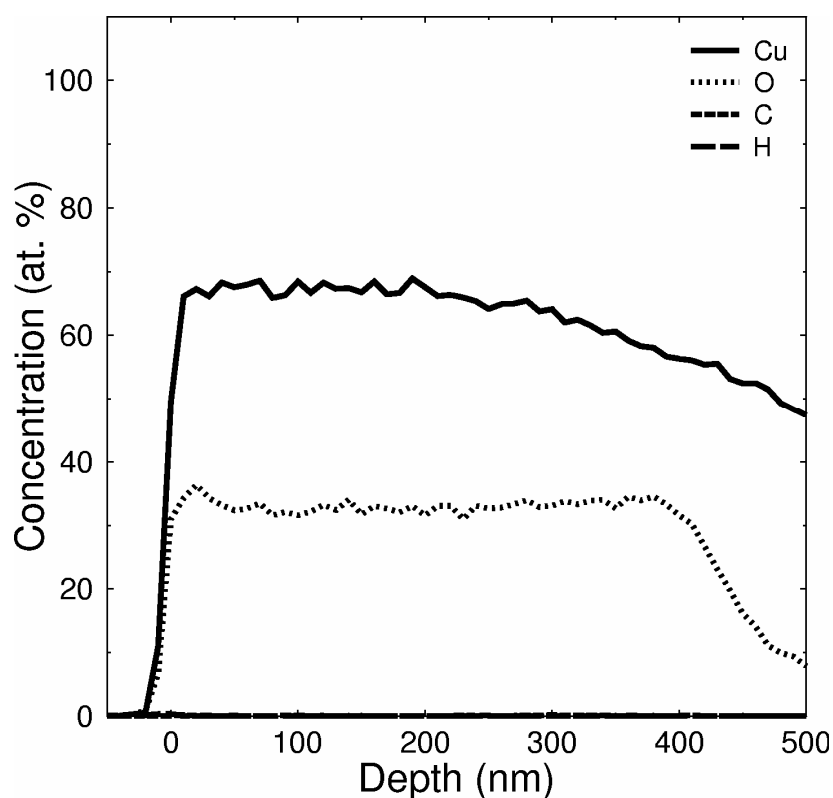


Figure 19. Oxidized copper sample depicts the formation of Cu_2O phase.

The reduction experiments were made between 310 °C and 385 °C varying exposure time from 5 to 60 minutes. In alcohols, the reduction power decreased the more complex the molecule became (primary \Rightarrow secondary \Rightarrow tertiary) to an extent that

tert-butanol did not reduce copper oxide at 385 °C even after 60 min exposure. A weak reduction power of tertiary alcohols can be explained by the carbon atom, to which the hydroxyl group bonds, does not have the hydrogen atom to be eliminated. Aldehydes and ketones showed better reduction power than tertiary alcohol but they were also found to be weak reducing agents. Carboxyl acids, formic acid, and acetic acid, showed the same pattern than alcohols and aldehydes. The smaller the molecule was the more effective reduction took place. The reduction process was successful and our approach seemed a promising method to produce a copper seed layer.

ALD-TiN film was tested as a seed layer for the ECD-Cu deposition in year 2000. The concept was attractive because TiN film could function as a seed and barrier layer resulting in significant cost savings in the production. Depositions were carried out with an innovative anode structure where several anodes were possible to be controlled individually improving the current density in the middle of wafer. Copper metal was grown on TiN and its adhesion was good. However, regardless of innovative anodes, the film suffered from the terminal effect. Very soon after these studies first conference paper was published where direct plating was tested on the PVD barriers.⁸⁶ Similar types of challenges were observed as with ALD-TiN. Since this concept has not made its breakthrough yet, it probably was not successful after all.

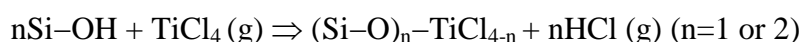
Next two chapters introduce the results of other work on the subject matter, made after our studies. The introduction includes the discussion of the author.

6. New Discoveries of the TiN Process

Satta *et al.* studied a very early phase of the ALD-TiN growth deposited from TiCl_4 and ammonia on thermal SiO_2 using RBS and low-energy ion scattering (LEIS).⁸⁷ The LEIS measurements were made with 3 keV $^4\text{He}^+$ beam and an ion dose of 0.2×10^{15} ions/cm². The information depth of LEIS is limited to one atomic layer due to low-energy noble gas ions that scatter from the outmost layer. Ion which penetrate deeper have a high neutralization probability and are not seen in the scattered ion spectrum.

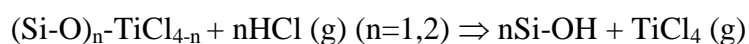
Three different phases were recognized in the TiN growth: I) growth takes place on SiO₂ utilizing hydroxyl groups on the surface, II) growth occurs on SiO₂ surface but more preferably on predeposited TiN, III) limited lateral growth. The first phase, where the coverage increases linearly, lasts only eight cycles at 400 °C and 25 cycles at 350 °C corresponding with a layer coverage of ~ 8 %. The growth occurs two-dimensionally forming Si-O-TiCl_x terminated surface. Three-dimensional growth is characteristic for the second phase. For some unknown reason growth takes place more likely on -TiCl_x and -NH_x terminated surface than on the substrate. Transition to the third phase occurs through the island coalescence that causes a slow-down of the lateral in favor of the vertical growth of clusters. The change of the growth rate from phase II to III is small. Minimum number of cycles to reach the closure of the surface is 100 at 400 °C and 150 cycles at 350 °C corresponding to the film thickness of 24±3 Å and 34±3 Å. In later studies a difference was found depending on whether TiN was deposited on chemically deposited SiO₂, thermally deposited SiO₂ or SiC.⁶⁵ The closure of the starting surface was the fastest for chemically deposited SiO₂ (29±3 Å / 100 cycles) and the slowest for SiC (45±9 Å / 200 cycles). Choi *et al.* studied TiN growth on SiO₂, HfSiO_x, and HfO₂. They suggested that an initial growth of TiN on SiO₂ surface is more three-dimensional than two-dimensional.⁸⁸ The growth on HfO₂ was found to be more two-dimensional and better nucleation was explained by catalytic dissociation of the precursors. Estimated thicknesses of the surface closure were 24 Å on SiO₂, 12 Å on HfSiO_x, and 6 Å on HfO₂.

Snyder *et al.* investigated early phase of the TiN growth from TiCl₄ and ammonia using *in situ* Fourier transform infrared spectroscopy (FTIR) technique.⁶⁶ The film was deposited on silica powder at 400 °C. In the first half cycle of TiCl₄ the reaction was found to be rapid and complete suggesting the following overall reaction:



In the second half of cycle, the powder was exposed to ammonia for three minutes and then the chamber was evacuated. Results suggested formations of M-NH₂ bonds and the removal of the Ti-Cl_x bonds. In addition to the TiN formation in the half cycle of ammonia a decrease of Si-O-Ti bonds and a re-emerge of Si-OH bonds was

observed, being 28 % from original intensity of silanol group. The formation of Si–OH bonds in the following cycles were observed to decrease rapidly, and in the third to sixth cycles, no Si–OH regeneration was observed anymore. It was concluded that the formation of Si–OH bonds was a result at cleavage of (SiO)_nTiCl_{4-n} (n= 1 or 2) leaving Si–O bond to the surface that is then hydrogenated by ammonia.⁶⁶ The cleavage was assumed to be caused by ammonia. The authors have not further discussed how the cleavage could occur. It is probably assumed that some Ti(NH_x)Cl_{4-n} molecule with a reasonable high vapor pressure would form and leave the surface. One other suggestion could be that the cleavage of (SiO)_nTiCl_{4-n} (n= 1 or 2) is caused by HCl by-products making reversal reaction for the TiCl₄ pulse:



Evidently, the reformation of Si–OH could explain the low growth rate at the very beginning on the SiO₂ wafer. It could also be speculated that the reformation of Si–OH could have something to do with the 3D-growth of TiN on SiO₂ wafers. However, according to previous papers the closure of the SiO₂ surface does not occur until film thickness is ~24 Å that is more than 3-6 growth cycles. Nevertheless, it could be possible that Si–OH formation could last longer than six cycles, but the formation occurs below the detection limit.

It was speculated in paper VII that the film non-uniformity of TiN could be a result of HCl by-products reacting with –NH_x sites during the TiCl₄ pulse. Based on previous results it could also be speculated that the film non-uniformity is formed prior to the film closure. During the ammonia pulse increasing HCl concentration in the flow direction enhances the formation of Si–OH bonds on the surface and consequently decreases the growth rate of TiN.

Early phase of the ALD-TiN growth was simulated with quantum chemical calculations by Lu *et al.*⁸⁹ The calculations were based on hybrid density functional theory. The (SiH₃O)₃Si–OH cluster was considered as a starting surface and the reaction pathways were constructed by a potential energy surface (PES) scan. The calculations were made with the Gaussian 03 quantum chemistry program. Results

demonstrated the formation of $\text{SiO}_2\text{-O-TiCl}_3$ terminated surface in the TiCl_4 pulse. The chemisorption of TiCl_4 occurs between an empty d-orbital of a Ti atom and the oxygen lone-pair electrons. The electron donation from oxygen to titanium weakens the Ti-Cl bonds. Correspondingly, the $\text{SiO}_2\text{-O-Ti(NH}_2\text{)}_{3-x}\text{-Cl}_x$ terminated surface is formed during the ammonia pulse. Eventually, all chlorine is removed but it becomes more difficult for the second and third one. The reaction is endothermic and required energy to remove chlorine is increasing (1. Cl: 0.58 eV, 2. Cl: 0.79 eV, 3. Cl: 0.94 eV) suggesting that the reaction is not thermodynamically or kinetically favorable. The results show that the adsorption of both TiCl_4 and ammonia are more probable than dissociation as a result of reaction. Consequently, longer pulses are needed to maintain high gaseous pressure on the surface, which will minimize desorption of the adsorbed molecules from the surface and offer time for a complete surface reaction. Both precursors formed relatively stable chemisorbed states with formation energies of 0.46 eV and 0.70 eV. The stable states were seen to hinder the surface reactions being also a source of chlorine residues in the film. Consequently, higher deposition temperature was required to reduce the stability of the chemisorbed molecules and make the dissociation more complete.⁸⁹ Lu *et al.* did not discuss the source of 3D growth or possible secondary reactions of by-products. However, the results supported well the experimental results of the ALD-TiN studies and adequately explained, for instance, why excess ammonia with long exposure is often needed to get the best material properties of TiN.

Tiznado *et al.* studied the ALD-TiN growth with XPS transferring the sample between deposition chamber and XPS system under vacuum.^{67, 90} Depositions were carried out with a high volume (~5 L) cold-wall reaction chamber that is not recommended for the ALD studies [VII]. Consequently, the chamber caused overlapping pulses and significant amount of impurities. Results suggested that the reduction of $\text{Ti}^{(+4)}\text{Cl}_4$ to $\text{Ti}^{(+3)}\text{Cl}_3$ could occur via dissociative adsorption in the $-\text{NH}_x$ sites instead of ammonia exposure.

Six-step-cycle was used by Cheng and Lee to get better film properties of TiN.⁹¹ In addition to purging, the reaction chamber was evacuated between the material pulse and the purge step. The resistivity, the Cl residues, and the surface roughness were

measured. The improvements in the film properties were explained with increasing partial pressure of by-products in the evacuation step, which decreases the Cl content (~2 at.-% at 300 °C).⁹¹ Because only one data point was presented, the results are not explicit. The evacuation step between precursor pulses is known to reduce overlapping pulses when there are some dead gas pockets in the deposition system [VII].

Li *et al.* studied the grain boundary formation of the ALD-TiN film with a high-resolution transmission microscopy (HRTEM).⁹² It was interesting to notice that their observations were slightly different from previously reviewed results and they did not discuss any results or used any references published after year 2000. Film was deposited on PECVD-SiO₂ (300 nm) at 390 °C from TiCl₄ and ammonia. They suggested, based on HRTEM images, that the film grows epitaxially in the first ten monoatomic layers stacking on (200) planes and then split into two crystals with a small angle of 3°. Small angle disorientation is believed to occur due to stacking error and geometric feature. Geometrically, very small misorientation can occur due to two-dimensional convex surface with a small curvature. At the beginning, the misorientation is expected to be negligible and the film growth has pseudo-epitaxial characteristic. The gap is increasing until it is close to atomic size. In the 11th monoatomic layer the gap was still smaller than the diameter of the atom forming a discontinuous layer. The studies reveal that the width of boundaries is an atomic scale regardless of what structures the grain boundaries have. Consequently, the boundaries are not believed to be an effective diffusion channel for copper. Small angle boundaries were often observed in (200) epitaxy growth areas while the large angle boundaries appeared in the areas with (111) close-packed stacking configuration. The tilt and twist grain boundaries with the width of atomic scale are two main characteristics of large grain boundaries.⁹² It would have been very interesting too see the discussion about earlier studies.^{65, 87, 88} For example, whether the small angle disorientation could generate a channel for ion beam of LEIS implying uncovered SiO₂ surface or could the closure of SiO₂ surface be a result of an atom filling the gap of small angle boundary when the film thickness is about 25 Å?

The ALD-TiN growth on low-k material was also found troublesome when TDMAT was used as a titanium source.⁶⁸ Depositions were made on SILK (Dow Chemical) that is an aromatic polyphenylene polymer comprising primarily phenyl groups. Because of poor nucleation of the TiN growth from TDMAT and ammonia, ALD- Al_2O_3 nucleation layer was used as a starting surface on SILK. Since SILK does not contain hydroxyl groups that could react with TMA, more favorable growth of Al_2O_3 than TiN on SILK was not fully understood. It was suggested that the nucleation of Al_2O_3 on SILK may result from the reaction of TMA and water that is diffused in SILK from atmosphere because SILK is known to be porous. Furthermore, it was suggested that water molecules near the surface of SILK could react with TMA generating small Al_2O_3 clusters embedded in the polymer network.⁶⁸ It is acknowledged that this integration scheme comprises a possible issue. The Al_2O_3 layer would decrease the effective area of metallization, it would increase the k-value of insulator if penetrating to porous SILK, and it would increase the contact resistivity in the bottom of via. However, it is suggested that negative effects of Al_2O_3 would remain minimal because the film thickness was only 10-13 Å.

7. New Discoveries of W_xN and WN_xC_y Processes

7.1. W_xN Process

As an alternative tungsten source bis(tert-butyylimido)-bis(dimethylamido)tungsten ($(^t\text{BuN})_2(\text{Me}_2\text{N})_2\text{W}$) was used for the W_xN deposition.⁹³ Film growth took place via decomposition of the precursor that was activated by ammonia or pyridine. Suggested β -hydrogen elimination occurred in the range of 250-350 °C where the carbon residues remained below detection limit. The film composition of $\text{WN}_{1.1\pm0.1}$ was believed be a result of strong imido bonds, and the film showed good diffusion barrier properties up to 600 °C.⁹⁴ Film growth was 0.5 Å/cycle at 300 °C and resistivity was ~3000 $\mu\Omega\text{cm}$ prior to annealing. Film deposition was also made on porous low-k material where the pores were sealed prior to deposition.⁹⁵

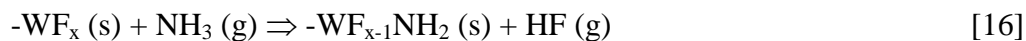
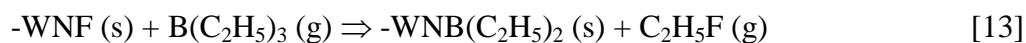
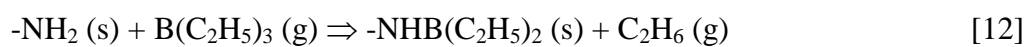
Bystrova *et al.* studied very complex W_xN process,⁹⁶ where silane and ethane were used as reducing agents. Kim *et al.* from Hynix Semiconductor and authors from Novellus Systems developed the process where diborane (B_2H_6) was used as an additional reducing agent in the W_xN deposition.⁹⁷ The process resembled the WN_xC_y process of ASM where boron-based reducing agent was used.⁹⁸ The depositions were made at 300 °C in commercial ALD reactor (Concept2 AltusTM) of Novellus Systems, Inc. The ALD characteristics were presented with the saturation curves that indicate the required pulse length for diborane. The growth rate saturates in three seconds. Another interesting feature of the saturation curves is seen with ammonia. The growth rate of the process where only WF_6/B_2H_6 were pulsed, seems slightly higher than in the $WF_6/B_2H_6/NH_3$ process. Surprisingly, there is no discussion about this observation in the paper. It could be possible that diborane as a strong reducing agent is forcing tungsten into a nearly metallic phase like disilane does for tungsten hexafluoride.⁶⁹ Ammonia could function as a weak oxidizer. The nature of ammonia is further discussed in the following paragraph. High growth rate of the W_xN film (2.8 Å/cycle) suggests that the deposition system is either that of a non-flow-type or that of a low-flow-type reactor but it cannot be confirmed from the experimental description. Film resistivity saturated to the level of ~335 $\mu\Omega\text{cm}$ and the slope of resistivity versus the film thickness suggests very small grains for the W_xN film. XRD results support this suggestion.

7.2. WN_xC_y Process

The N:C ratio was found to vary in the WN_xC_y film depending on the pulsing parameters and temperature. It was also noticed that film properties were slightly better if the pulsing sequence was $TEB/WF_6/NH_3$ instead of $NH_3/WF_6/TEB$ when the deposition temperature was 300 °C. The N:C ratio clearly increased in the second sequence.

Pulsing Order	W (at.-%)	C (at.-%)	N (at.-%)
(1) $NH_3/WF_6/TEB$	47-55	30-45	2-10
(2) $TEB/WF_6/NH_3$	52-58	20-30	10-20

Li *et al.* explained possible reaction mechanisms of WN_xC_y growth when the pulsing sequence was $B(C_2H_5)_3/WF_6/NH_3$.⁹⁹ They suggested that during the triethyl boron pulse bonding takes place with $-NH_2$ (s) and $-WNF$ (s) sites where $-B-N-$ bonding is formed (Eqs. 12, 13). In the following WF_6 pulse the partial reduction of tungsten is expected as well as the formation of tungsten carbide (Eqs. 14, 15). When ammonia is introduced in the last step, fluorine is partially removed and WN_xC_y film is formed (Eq. 16). Furthermore, ammonia has an important role in the forming of reactive sites for the next triethylboron pulse.



Previous results have revealed that as a reducing agent, TEB is significantly more effective than ammonia. However, the changes in N:C ratio are difficult to explain if both ammonia and TEB are purely reducing tungsten. In the combined PEALD and ALD studies it was possible to observe that ammonia can function as an oxidizer in the right environment. Tantalum precursor was reduced to metallic tantalum in the PEALD process using radicals. At the end of each process cycle, ammonia was introduced to tantalum metal surface forming TaN_{-1} that is metastable phase⁴² and challenging to obtain by ALD. Based on this experiment it was concluded that if the metal or its compound has become very eager to oxidize, ammonia can function as a weak oxidizer, which explains the formation of TaN_{-1} instead of Ta_3N_5 . The oxidation tendency of tungsten after the TEB reduction was also observed when the ammonia pulse was left out and the W_xC film was deposited. As a result of oxidation the film contained 10 at.-% oxygen after it was exposed to air. Reflecting this idea against WN_xC_y studies it can be suggested that ammonia can weakly oxidize a WC_{y+q} compound to form WN_xC_y with low nitrogen content when the deposition sequence is $NH_3/WF_6/TEB$. Correspondingly, ammonia is functioning as reducing agent in the pulsing sequence of $TEB/WF_6/NH_3$ introducing higher nitrogen content at the expense

of carbon. In paper IV, we suggested that ethyl radicals are formed from TEB, but how the ethyl molecule degrades and forms carbide is unknown.

Chen *et al.* studied the diffusion barrier performance of ALD-WN_xC_y films and compared it to PVD-Ta on 0.25- μ m-dual damascene structure.¹⁰⁰ WN_xC_y film of 25 Å thickness exhibited highest yield and lowest average via resistance in the 0.25 μ m via chain (with 1080 vias). Ultra-thin 15 Å WN_xC_y film was also tested but the yield dropped suggesting the minimum thickness for the barrier. In the EM performance test, the T₅₀ lifetime of a WN_xC_y barrier (25 Å) was an order of magnitude higher than that of the PVD-Ta. Process integration to porous methyl silsesquioxane (MSQ) based low-k material was studied. Although barrier penetration into MSQ was 500 Å, it was found to block copper diffusion. Penetration of WN_xC_y film to MSQ (pore diameter: 4-5 nm) was also observed by Besling *et al.*¹⁰¹ Correspondingly, WN_xC_y penetration into porous SiCOH was confirmed as well.¹⁰² The studies comprised WN_xC_y depositions on plasma sealed SiCOH surface.

The use of WN_xC_y film (30 cycles) was seen to improve the RC delay ~48 % when it was compared to I-PVD deposited film stack (TaN (5 nm)/Ta (20 nm)).¹⁰³ The size of RC delay of 90 cycles WN_xC_y film was 377 ps and 30 cycles was 300 ps per 1 mm conductor length. Travaly *et al.* studied electronic density of interfaces of WN_xC_y/SiO₂, WN_xC_y/plasma treated porous low-k, and WN_xC_y/SiC. The studies show the increase in electronic density of N₂ plasma treated low-k surface in the dept of 20-30 nm, which is comparable to the one of SiO₂. When WN_xC_y/SiO₂ and WN_xC_y/SiC interfaces were studied, a decrease was observed in electronic density of WN_xC_y/SiO₂ interface. This was believed to be caused by the surface reaction that made the surface porous. No decrease was seen in the WN_xC_y/SiC interface. Li *et al.* reported 18 surface materials that were studied concerning their WN_xC_y compatibility.¹⁰⁴ LEIS studies suggested that a full coverage of substrate took place between 10-20 cycles corresponding with a 9-18 Å thick film. The film density of 14 g/cm³ was reported for ~10 nm thick film.

Schuhmacher *et al.* studied the process integration of WN_xC_y barrier to dual damascene oxide module.¹⁰⁵ Instead of low-k dielectrics, PECVD silicon dioxide was

used as an insulator. The studies comprised four splits of underlying copper cleanings and I-PVD deposited TaN/Ta was used as a reference the WN_xC_y barrier. Removal of WN_xC_y barrier by CMP was studied on blanket wafer with commercial barrier and copper slurry. The erosion appeared at different locations on the wafers depending on the presence of patterns at the metal level underneath. However, the electrical characteristics were comparable to an *in situ* I-PVD barrier (TaN/Ta)/Cu seed metallization approach. The argon plasma cleaning gave the lowest via resistance values. The yield of via chain (1 million) was good for both Ar plasma cleaning and the split of no cleaning at all. The *in situ* ethanol cleaning in the same reaction chamber where the WN_xC_y barrier was deposited, resulted in a higher via resistance, and barrier thickness was reduced on the trench sidewall. Schuhmacher *et al.* suggested that the problems with ethanol could be related to the use of the same reactor for both process steps and some interaction of ethanol and the precursors used in the WN_xC_y deposition. The resistivity of the WN_xC_y barrier on the bottom of via was about $375 \mu\Omega\text{cm}$.

Galvanic corrosion, which is one of the corrosion mechanisms in the CMP process, was studied for the WN_xC_y barrier.¹⁰⁶ Slurry, as an electrolyte, was playing important role in the corrosion. Maleic and nitric acid was studied as an etcher and H_2O_2 was used as the oxidizing agent in the solutions. Three different electrode setups (Cu/Ta, Cu/W, Cu/ WN_xC_y) were investigated. Cu/Ta system exhibited the lowest current. Cu/ WN_xC_y system was significantly better than Cu/W but not as good as Cu/Ta system. The presence of carbon and nitrogen in the film appeared to strengthen it against galvanic coupling with copper.

Kim *et al.* reported that coalescence of the WN_xC_y nanocrystals occurs beyond ten ALD cycles.¹⁰⁷ The nucleation and growth was suggested to occur simultaneously at the early stages of WN_xC_y deposition. The ammonia plasma treatment was found to improve the film nucleation on PECVD SiO_2 . The C-V measurements after BTS showed that barrier thickness of 5.2 nm (50 ALD cycles) was enough to hinder copper diffusion. When WN_xC_y film was heated up to 700 °C for one hour in vacuum, no changes in crystal structure were observed with XRD.¹⁰⁸ However, several new peaks were formed as soon as the sample was heated to 800 °C. Comparative failure

temperature study shows excellent barrier properties of the WN_xC_y film against copper diffusion. The grain structure was considered to improve barrier properties compared to ALD-TiN. The HRTEM images revealed nanocrystalline structure with the grain size of 3-7 nm. Nanocrystals with the size of only few nanometers were also observed. When the diffusion barrier property was tested with etch-pit test, the failure of Cu/ALD- WN_xC_y /Si structure was observed at 600 °C.

Hoyas *et al.* studied the WN_xC_y deposition on SiC surface.¹⁰⁹ Since SiC film was known to oxidize in atmosphere, different ageing of SiC samples (fresh, two days old, two months old) were investigated. No significant differences were observed between samples. However, it was noticed that a long exposure (> 1 s) of TEB prior to the deposition enhanced the film growth, and it was important to have TEB as the first precursor pulsed on the surface. It was also suggested that TEB reacts with SiO_2 surface leaving it carbon terminated and thus the film growth on SiO_2 and SiC are similar. Hoyas *et al.* studied also the WN_xC_y growth on methyl terminated surface.¹¹⁰ Volders *et al.* compared the WN_xC_y , WN_x , and WC_x films.¹¹¹ They found that the WN_xC_y film is more prone to galvanic corrosion than binary compounds. It was also observed that the WN_xC_y film grows better on PECVD oxide than thermal oxide which is opposite of what is seen for WN_x .

8. Conclusions

The ALD-TiN film showed encouraging properties as copper diffusion barrier meeting some material and process integration requirements. However, several requirements were not met: 1) the content of halide residues remained acceptable only when deposition temperature was 400 °C, 2) the film uniformity was far from an acceptable limit in the cross-flow reactor, and 3) film growth rate was too low. Generally, low film growth per deposition cycle can be acceptable if the growth rate can be compensated by fast pulsing and purging, which was possible with this reactor design. However, the process chemistry required long ammonia exposures to accomplish the surface reaction and minimize the residue content in the film. Consequently, the length of deposition cycle could not be shortened. Since the growth

rate has direct influence to the process throughput and the costs, it is not a requirement which can be easily compromised.

Although amorphous structure was not a requirement for the barrier film, the polycrystalline structure of ALD-TiN with columnar grain boundaries was seen as a possible source of copper diffusion. Even high film density and good BTS results of the TiN film were not able to diminish the concern.

The issues related to ALD-TiN deposition on materials (e.g. Aurora[®]) which lack active sites, were well-predicted before they were proved in our studies. However, these issues were seen more or less as engineering challenges which can eventually be solved. However, in our studies, aggressive pitting of copper surface was seen as a fundamental issue that would be nearly impossible to avoid without changing precursors. Based on our results, ALD-TiN film deposited from TiCl₄ and ammonia was not seen as a good candidate for copper diffusion barrier applications.

ALD-WN_xC_y film exhibited excellent properties as a copper diffusion barrier exceeding the properties of TiN film in most cases. Particularly, good compatibility with copper metal and excellent results in dual-damascene integration made ALD-WN_xC_y film an excellent candidate for copper diffusion barrier applications.

Although nanolaminate structures were demonstrated as a good method to protect the substrate from incompatible process, it was seen to be a slightly too complicated method compared to the single layer deposition of the diffusion barrier. Furthermore, since the thickness of the barrier film was not expected to be more than tens of atomic layers in the future, nanolaminate structures would be difficult to make.

Film uniformity studies demonstrated some most common non-uniformity sources in the ALD process including less known secondary reactions of the by-products. Since non-uniformity have often very characteristic patterns in the cross-flow reactor, the uniformity studies are easier to carry out in a cross-flow than a showerhead reactor. Cross-flow reactor can be considered to be more educative, particularly when non-uniformity is caused by reactor hardware. However, when the reactor hardware is

well-optimized, most uniform films can be obtained in a showerhead reactor that is more forgiving for thermally sensitive precursors and the secondary reactions of the by-products.

Although the copper oxide reduction process was successful, the copper seed deposition via copper oxide reduction has not been a successful method so far. Like copper deposition by ALD, copper oxide deposition was found very challenging. Copper oxide reduction prior to barrier deposition with only alcohol was not successful because the removal of lithography residues also requires other cleaning methods like the plasma cleaning. However, the process of copper oxide reduction was seen as a valuable process in the applications where only the copper oxide removal was an objective.

Today, year 2008, when advanced MPU devices are made with the design node of 45 nm, the ALD diffusion barriers have not established their position in the IC industry. The PVD-TaN barrier is still the choice of industry, and the process has held its position longer than it was expected in the market analysis five years ago. The cost driven factors discussed in the introduction to this study must be taken into account. Although there is a feasible barrier process available, the IC industry is not eager to move towards new technology as long as there is some way to extend the life cycle of existing technologies. The more design nodes can be made with the same equipments the more profitable the business is for the IC manufacturer who is often forced to buy new equipments and build new factories when the design node is shrunk.

Indeed, ALD diffusion barriers came closer to IC production when Intel began HVM of ALD deposited high-k transistors in year 2006. Evidently, the ALD technique has now established its position in the IC production making it easier for new processes to establish themselves.

Favorable design rules of metallization have made it possible to continue using the PVD diffusion barrier. Surface feature requirements for copper dual-damascene structure have remained very moderate because AR no higher than 2 is expected in the near future.¹⁶ Evidently, this raises the question whether new diffusion barrier processes are needed for conventional MPU devices in the future. Equipment/process

suppliers are optimistic that new diffusion barriers are eventually required to improve the reliability of the diffusion barrier film. Furthermore, it is possible that ALD barriers for the copper metallization are needed in memory devices and MEMS prior to MPUs.

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