

Sub-Millimeter and Terahertz-Wave Packaging for Large Chip-Width MMICs

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Abstract—We present novel waveguide packaging for sub-millimeter and terahertz-wave devices, which is suitable for large chip-width MMICs and doesn't require any additional fabrication process. With full electromagnetic simulation, we analyze possible wave modes in a rectangular waveguide with thin E-plane slits formed for inserting large-width MMICs into the split waveguide block and show that parasitic modes can be well suppressed by lossy and high-dielectric material. For a 1.1-mm-wide test IC in the 260–320 GHz band, measured transition loss is around 1 dB with more than 60 dB inter-port isolation.

Index Terms—Integrated E-plane probe, terahertz wave, waveguide package.

I. INTRODUCTION

IN the last couple of decades, attention to the last remaining region in the terahertz (THz) frequency band has been steadily growing for its possible adoption in various application fields, such as imaging, spectroscopy, security, and wireless communications [1], [2]. Such strong interest from science and engineering research communities has accelerated the development of device technologies for THz-wave systems and applications. The cut-off frequencies of state-of-the-art compound semiconductor electron devices on InP or GaAs substrates have already exceeded 1 THz [3], and researchers with Northrop Grumman Corporation have recently presented an amplifier that provides approximately 10 dB power gain at 1 THz [4].

Along with the progress in device technologies, there have been various investigations on packaging THz MMIC devices. Though concepts based on commercial ceramic technologies for compact and lightweight packaging in practical applications have been reported with promising results [5], [6], the use of metallic split blocks with rectangular waveguides (WGs) for THz signal ports is still considered the most valid approach because of superior loss performance in many applications. In those WG packages at THz frequencies, monolithically integrated electromagnetic probes or couplers have mainly been demonstrated [7]–[9]. Thanks to the thin substrate for suppress-

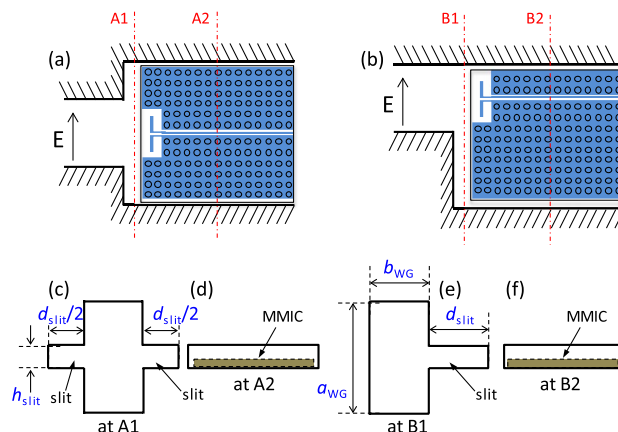


Fig. 1. (a) and (b) Cross-sectional diagrams of split block WG package with slits on the E-plane for large-width MMICs. (c)–(f) Cross-sectional views at A1, A2, B1, and B2 in (a) and (b).

ing parasitic substrate modes, the integrated transitions, such as E-plane probes and dipole transitions, provide quite large operation bandwidth with low loss even on high-permittivity substrate. However, they limit the width of the MMICs, which limits the design area for active circuits, such as power amplifiers. In order to avoid this problem, a deep dry-etching process is used to remove the substrate beside the integrated transitions so that the probes fit into the WG [10], [11].

Here we present an integrated coplanar waveguide (CPW)-to-WG E-plane transition for THz MMICs, which provides a large degree of design-area freedom with no etching process, and experimentally demonstrate low loss and acceptable isolation in the 300-GHz band.

II. WAVE MODES IN RECTANGULAR WG WITH E-PLANE SLITS

If thin air gaps or slits are formed on the E-plane of the split blocks, even with no substrate removal, we can put a large-width MMIC with dipole EM probes in the WG package as shown in Fig. 1. Depending on the location of the probe, just a single slit would be no problem. The problems are whether, even with the slits, the TE₁₀ mode can be coupled into the dipole probe or not and how the slits affect to the wave transition between the WG and MMIC.

In the structures shown in Fig. 1, the TE₁₀ mode waves propagating in the rectangular WG toward the MMIC will encounter the slits before they are coupled with the on-chip transition. The slits are likely to distort the dominant wave mode, TE₁₀, and cause excitation of multi-modes in the structure. However, interestingly, according to our FEM simulations with Ansys

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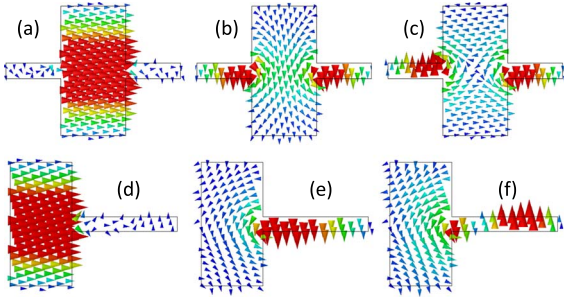


Fig. 2. Simulated E-field distribution of the first three possible modes in the WG with dual and single side slits when slit depth is $1.7 \cdot b_{\text{WG}}$. (a) and (d) TE10; (b) and (e) Q-TE01; (c) and (f) Q-TE02.

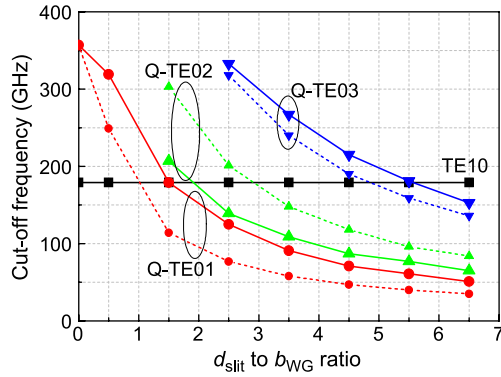


Fig. 3. Simulated cut-off frequencies of first four dominant modes in slit WGs as a function of the ratio of slit depth to E-plane width in the WR3.4 WG. Solid and dashed lines are for dual and single slit structures shown in Fig. 1(c) and (e), respectively. In the simulation, slit height was set to $110 \mu\text{m}$.

HFSS, the characteristic impedance and cut-off frequency of the TE10 mode in the slit WGs shown in Fig. 1(c) and (e) are almost identical to those in the standard WG with no slit and remain constant regardless slit depth d_{slit} . This implies we would be able to pick up the TE10 modes with ordinary on-chip dipole probes even with the slits.

In addition, from the simulations, it was observed that the slits generate a certain series of wave modes. Fig. 2 shows the E-field distributions of the first three possible modes in the dual- and single-slit WG when $d_{\text{slit}} = 1.7 \cdot b_{\text{WG}}$, where b_{WG} is the E-plane width of the ordinary waveguide (see Fig. 4). In this report, we refer to these parasitic modes as quasi-TE0 n (Q-TE0 n) modes (n : integer) on the basis of the geometric coordinate in the standard WG. As can be seen in Fig. 2, the undesired modes are mostly concentrated in the slits. Moreover, the cut-off frequencies of the Q-TE0 n modes decrease as d_{slit} increases, while those of other higher-order modes change little. Fig. 3 shows the simulated cut-off frequencies of the first four dominant modes in the WR3.4 WG with single and dual slits. In the simulation, slit height h_{slit} was fixed to $110 \mu\text{m}$. As can be seen in Fig. 3, if d_{slit} is larger than $2.5 \cdot b_{\text{WG}}$, the TE10 mode will become the third in terms of cut-off frequency. Considering the slits are assumed to be thin at the operating frequencies, modes other than Q-TE0 n are expected to rarely exist in the operating frequency band, and this agrees with the simulated results, at least for up to $d_{\text{slit}} = 6.5 \cdot b_{\text{WG}}$ or $d_{\text{slit}} \sim 2.7 \text{ mm}$ in the WR3.4 band.

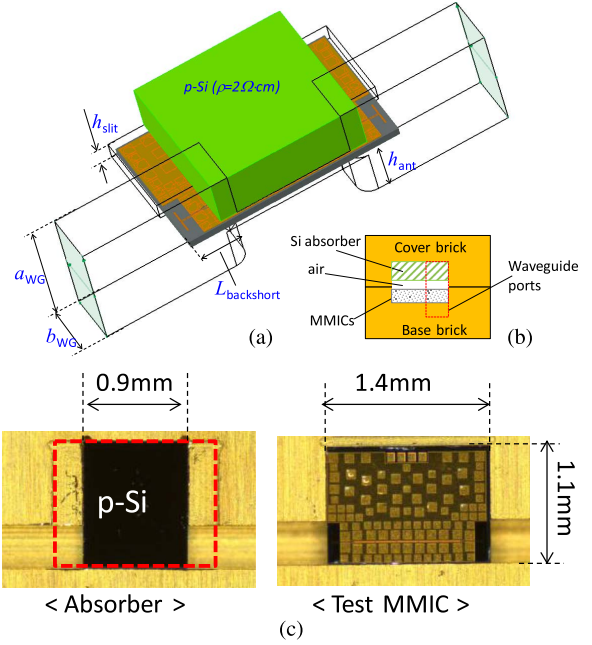


Fig. 4. (a) Schematic and (b) cross-sectional diagram of WR3.4 WG package with single slit and p-type Si block as absorber ($a_{\text{WG}} = 864 \mu\text{m}$, $b_{\text{WG}} = a_{\text{WG}}/2$, $L_{\text{backshort}} = 340 \mu\text{m}$, $h_{\text{ant}} = 350 \mu\text{m}$, $h_{\text{slit}} = 110 \mu\text{m}$) and (c) photographs of mounted silicon absorber and test MMIC in the split WG block.

For practical packaging, we should avoid the undesired modes bypassing an MMIC through the thin air gap above it to ensure that inter-port isolation is good enough for stable and reliable operation. If we insert high-permittivity dielectric material in the cover brick and form a partially loaded WG in the E-plane above the MMIC as shown in Fig. 4(b), the Q-TE0 n modes will be converted into longitudinal section electric modes and effectively confined in the dielectrics [12]. Therefore, lossy material will absorb the parasitic modes and improve the isolation performance of the package.

III. EXPERIMENT AND RESULTS

To verify the signal transition between a WG and CPW on a large chip-width MMIC, we fabricated a test IC consisting of two dipole antennas on the corner of the MMIC for in/output coupling, dense substrate vias, and CPW lines on a $50\text{-}\mu\text{m}$ -thick InP substrate. In this work, the width of the MMIC was 1.1 mm , around $2.5 \cdot b_{\text{WG}}$ in the WR3.4 waveguide. The diameter of the substrate vias was in the range of $60\sim 80 \mu\text{m}$. In this work, we followed a design flow and rule for the dipole probes similar to those described in [9]. As an absorber, we used a p-type silicon wafer with nominal bulk resistivity of $2 \Omega \cdot \text{cm}$. According to the HFSS simulations, bulk resistivity less than $10 \Omega \cdot \text{cm}$ showed good absorption performance. A bare p-type Si wafer was thinned down to $250 \mu\text{m}$ and diced into appropriate dimensions. In order not to disturb the mode transition from TE10 to the CPW mode, we set the length of the p-type silicon block slightly shorter than that of the MMIC so that the absorber wouldn't cover the space right above the dipole probes.

Fig. 4 shows a schematic diagram of the WR3.4 WG package with a single slit and the Si absorber and photographs of the fabricated split WG package. The h_{slit} was set to $110 \mu\text{m}$. Thus,

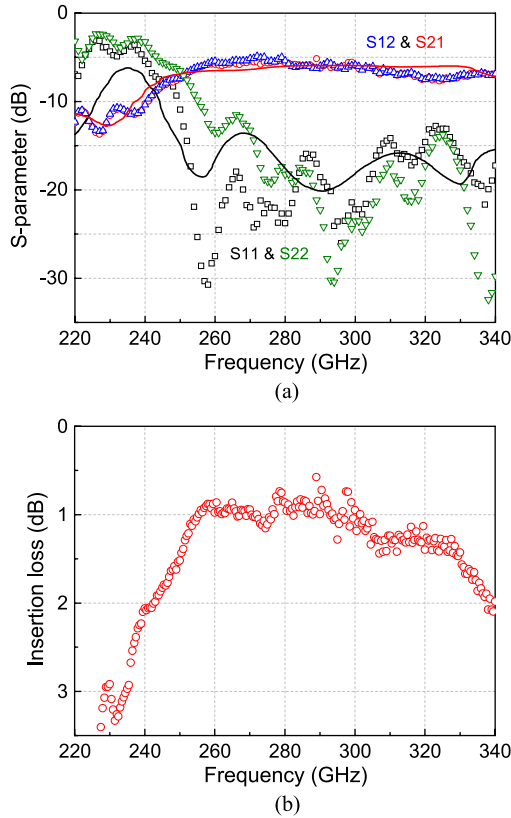


Fig. 5. (a) Measured (scatter) and simulated (line) S-parameters of test module with an approximately 8-mm WG feed for each in/output. (b) Estimated insertion loss per single dipole antenna.

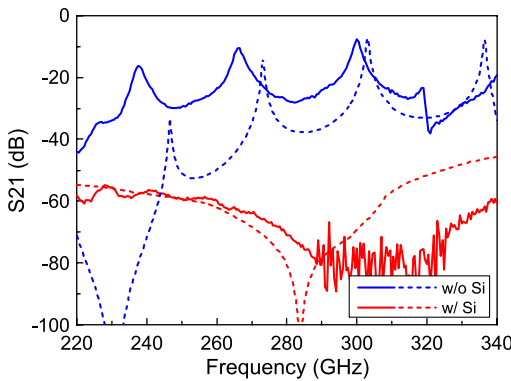


Fig. 6. Measured (solid line) and simulated (dashed line) isolation with no test MMIC in the package.

after the MMIC is placed in the package, the remaining air gap would be slightly less than $60 \mu\text{m}$. In the design, nominal tolerances of chip dicing ($< \pm 15 \mu\text{m}$) and mechanical milling ($< \pm 50 \mu\text{m}$) were considered and all fabricated modules had around a $20\text{--}30\text{-}\mu\text{m}$ gap at every sidewall between the MMICs and absorber chips and packages.

Fig. 5 shows the measured and simulated S-parameters of the fabricated module with an 8-mm WG feed for in/output ports. As can be seen, flat transmission and small return loss were observed from 260–320 GHz. An on-wafer TRL measurement was conducted to subtract the insertion loss of the CPW line ($w/g = 10/10 \mu\text{m}$) from that of the entire module and finally estimate the loss per transmission. In the operating frequency

range, approximately 3.2–3.6 dB insertion loss was measured for the $900\text{-}\mu\text{m}$ CPW line. From that, nominal insertion loss per probe was estimated to be around 1 dB, which is comparable to the performance with a similar technique but with no slit. To verify the isolation performance of the module and effect of the Si absorber, we conducted another S-parameter measurement with no test IC in it. Fig. 6 shows the measured results with and without the silicon absorber. First, for the module without the absorber, inter-port isolation of around 10~30 dB was obtained in the WR3.4 band. The peaky characteristics must be related to resonances in the space for the MMIC. However, the other module with the absorber exhibited dramatic improvement in isolation. Across the whole WR3.4 band, isolation was better than 60 dB.

IV. CONCLUSION

A WR3.4 WG packaging technique with on-chip E-plane probes provides large freedom in design area with no etching process in MMIC fabrication. Though E-plane slits in the split WG block for large chip-width may induce a series of Q-TE $0n$ modes in the package, the parasitic modes can be effectively absorbed with lossy and high-permittivity material. In the experimental demonstration, 1 dB coupling loss per probe and 60 dB isolation were achieved in the 260–320 GHz band.

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