# SCIENTIFIC REPORTS

Received: 24 November 2014 Accepted: 26 June 2015 Published: 29 July 2015

## **OPEN** Ubiquitous Graphene Electronics on Scotch Tape

Yoonyoung Chung<sup>1,\*</sup>, Hyun Ho Kim<sup>2,\*</sup>, Sangryun Lee<sup>3</sup>, Eunho Lee<sup>2</sup>, Seong Won Kim<sup>2</sup>, Seunghwa Ryu<sup>3</sup> & Kilwon Cho<sup>2</sup>

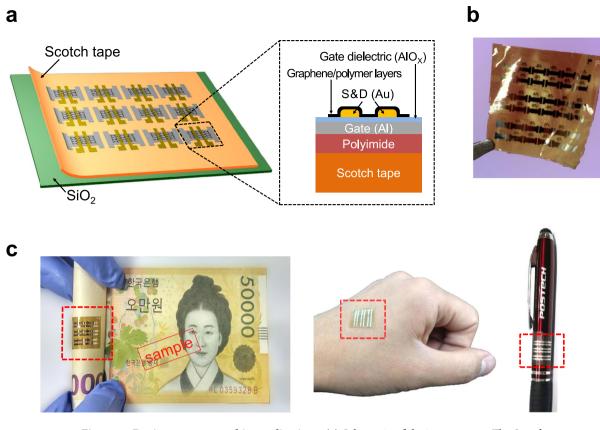
We report a novel concept of graphene transistors on Scotch tape for use in ubiquitous electronic systems. Unlike common plastic substrates such as polyimide and polyethylene terephthalate, the Scotch tape substrate is easily attached onto various objects such as banknotes, curved surfaces, and human skin, which implies potential applications wherein electronics can be placed in any desired position. Furthermore, the soft Scotch tape serves as an attractive substrate for flexible/foldable electronics that can be significantly bent, or even crumpled. We found that the adhesive layer of the tape with a relatively low shear modulus relaxes the strain when subjected to bending. The capacitance of the gate dielectric made of oxidized aluminum oxide was  $1.5 \mu$ F cm<sup>-2</sup>, so that a supply voltage of only 2.5V was sufficient to operate the devices. As-fabricated graphene transistors on Scotch tape exhibited high electron mobility of 1326 ( $\pm$ 155) cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup>; the transistors still showed high mobility of 1254 ( $\pm$ 478) cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup> even after they were crumpled.

Recent advances in flexible device technology have changed the paradigm of electronics from rigid objects to flexible form factors<sup>1</sup>. Flexible displays<sup>2</sup>, sensors<sup>3,4</sup>, circuits<sup>5,6</sup>, solar cells<sup>7</sup>, and batteries<sup>8</sup> have become popular subjects in both academia and industry, and such components have facilitated the development of bendable consumer products. One of the most popular approaches for making flexible devices is to use flexible plastic substrates, such as polyimide and polyethylene terephthalate, and to fabricate electronic components on them at a low temperature at which substrate deformation does not occur<sup>9</sup>. Alternatively, flexible and conformable substrates such as polydimethylsiloxane and a commercial tattoo can also be used on which a thin layer of electronic devices is laminated<sup>5,10</sup>. Flexible devices can also be directly prepared onto nonconventional substrates including banknotes and papers<sup>11-13</sup>. These methods have gradually expanded the use of electronics.

In this study, we developed a method for flexible and conformable electronic devices on Scotch tape. Scotch tape, which serves as a remarkably flexible substrate, is simply attached on various objects as long as the adhesive of the tape adheres; as a result, Scotch tape electronics can be utilized to accomplish ubiquitous electronic systems for applications of interest. Another advantage of such a Scotch tape substrate is that the adhesive layer of the tape relaxes the strain when subjected to bending. We analyzed the mechanical strain applied to a bent Scotch tape substrate. Because of its soft layers, transistors on top of the Scotch tape, i.e., non-adhesive side, experience a significantly lower tensile strain as compared to regular polyimide under the same bending condition. We used graphene as the channel material. Graphene is not only one of the most representative flexible electronic materials<sup>14,15</sup>, but also a promising candidate for signal conditioning in electronics<sup>16,17</sup>. In particular, graphene devices are widely studied for the radio-frequency technology, which enables wireless communication<sup>18,19</sup>. Thus, the fabrication of graphene transistors on Scotch tape would be a significant step toward realizing ubiquitous electronics.

The device structure is shown in Fig. 1. Graphene field-effect transistors (GFETs) were fabricated on Scotch tape attached on a silicon dioxide (SiO<sub>2</sub>) wafer (Fig. 1a). After fabrication, the Scotch tape substrate

<sup>1</sup>Department of Electrical Engineering, Pohang University of Science and Technology, Pohang 37073, Korea. <sup>2</sup>Department of Chemical Engineering, Pohang University of Science and Technology, Pohang 37073, Korea. <sup>3</sup>Department of Mechanical Engineering, Korea. Advanced Institute of Science and Technology, Daejeon 34141, Korea. \*These authors contributed equally to this work. Correspondence and requests for materials should be addressed to K.C. (email: kwcho@postech.ac.kr)



**Figure 1. Device structure and its applications.** (a) Schematic of device structure. The Scotch tape substrate was attached on a silicon dioxide (SiO<sub>2</sub>) wafer during fabrication. (b) After device fabrication, the Scotch tape substrate was easily peeled off from the wafer. (c) The Scotch tape device was then attached on nonconventional objects such as banknote (# 50,000 Korean won), human skin, and pen (Copyright 2013 Pohang University of Science and Technology).

.....

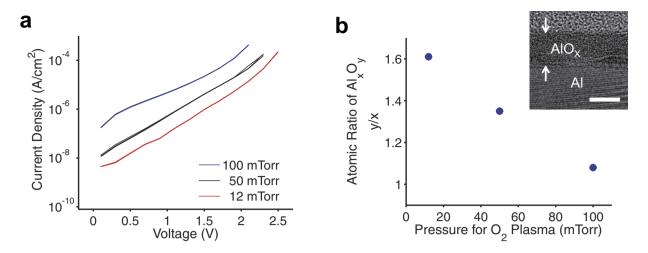
was peeled off from the wafer and ready to be placed onto various nonconventional surfaces (Fig. 1b). As shown in Fig. 1c, the GFETs on the Scotch tape were easily attached on a banknote, human skin, and a pen without any adverse effects on the electrical properties. Scotch tape as a substrate is superior to widely used polyimide for flexible/foldable electronics; the Young's modulus of the Scotch tape in this study is approximately 0.4 GPa as compared to 2.5 GPa for polyimide<sup>20</sup>. However, Scotch tape exhibits a lower operating temperature, less chemical resistance, and more outgassing in a vacuum chamber than polyimide, thereby requiring mild fabrication procedures to prevent any defects in the delicate substrate.

The gate dielectric is one of the most important components in field-effect transistors (FETs). Especially, high capacitance with a low leakage current is essential for low-power electronic devices that can be operated by portable batteries. Several methods have been used to meet the dielectric requirements for flexible transistors: atomic layer deposition (ALD) of aluminum oxide  $(AlO_X)^{21,22}$ , ion-gel dielectrics<sup>23,24</sup>, and oxidation of aluminum thin films<sup>25</sup>. Among these approaches, the oxidation of aluminum thin films with oxygen plasma, which does not require high temperature, solvent, or high-purity gas, is a feasible process for a Scotch tape substrate. Previously, oxygen plasma treatment on aluminum was demonstrated to form a high-capacitance  $AlO_X$  gate dielectric for flexible organic transistors; however, an additional self-assembled monolayer (SAM) prepared by soaking in a solution was required on  $AlO_X$  or else the leakage current through the dielectric increased significantly<sup>25</sup>. As solution-processed SAMs are not suitable for Scotch tape substrates, we improved the fabrication process for oxidized  $AlO_X$  by optimizing the plasma conditions so that a single  $AlO_X$  layer could be used as the gate dielectric for GFETs.

In a plasma system, the amount and movement of plasma particles are affected by power and pressure<sup>26</sup>. In particular, the kinetic energy of plasma ions is related to pressure, as shown in Equation 1, which describes the mean free path of a gaseous particle

$$\lambda = \frac{k \cdot T}{\sqrt{2} \pi \cdot d^2 \cdot P} \tag{1}$$

where k is the Boltzmann constant, T is the temperature, d is the collision diameter of the molecule, and P is the pressure. Therefore, oxygen radicals can penetrate the aluminum surface more effectively with a higher kinetic energy under lower pressure. We oxidized the surface of aluminum thin film (30 nm)



**Figure 2.** Analysis on oxidized aluminum (AlO<sub>x</sub>) thin film. (a) Leakage current of  $AlO_x$  under different pressure conditions during plasma treatment. As the pressure decreased, the leakage current through  $AlO_x$  was reduced, and the breakdown voltage increased. (b) X-ray photoelectron spectroscopy (XPS) data of  $AlO_x$  prepared under different pressure conditions. The relative ratio of oxygen to aluminum increased as the oxygen pressure during plasma treatment decreased. A higher oxygen ratio in  $AlO_x$  resulted in a better insulating property. Inset shows the cross-sectional transmission electron microscopy image of  $AlO_x$  prepared by oxygen plasma treatment on a thin aluminum film at 12 mTorr. The thickness of the AlOx layer was estimated to be 5.7 nm. Scale bar, 5 nm.

.....

deposited on a SiO<sub>2</sub> wafer in an oxygen plasma chamber for 7 min. During plasma treatment, three different oxygen pressure values were used: 12, 50, and 100 mTorr. The electrical properties of the oxidized  $AlO_x$  were tested after the deposition of the gold top electrode. The  $AlO_x$  samples prepared using different oxygen pressures had an almost identical capacitance of 1.5 ( $\pm$ 0.1)  $\mu$ F cm<sup>-2</sup>, which is equivalent to the capacitance of 2.3-nm-thick SiO<sub>2</sub>. However, there was a considerable difference in the leakage current of the three  $AlO_x$  samples. As the oxygen pressure for plasma treatment decreased, the leakage current through the  $AlO_x$  layer decreased, and the breakdown voltage increased (Fig. 2a). These results indicate that lower oxygen pressure facilitates a denser oxide film with better quality. Because of the large capacitance, only 1-1.5 V is sufficient to operate FETs by using the plasma-treated AlO<sub>x</sub> as the gate dielectric. In a previous study in which the ALD of  $AlO_x$  with a SAM was employed<sup>27</sup>, the capacitance of the gate dielectric (total thickness of 6.4 nm) was approximately  $0.5 \mu F \text{ cm}^{-2}$ , and its leakage current was on the order of  $10^{-7}$ A cm<sup>-2</sup> at 3 V. Applying 3 V to the  $0.5 \mu$ F cm<sup>-2</sup> capacitor induces an amount of charges equal to that from our  $1.5 \mu F \text{ cm}^{-2} \text{ AlO}_X$  capacitor with only 1 V. In Fig. 2a, the gate leakage current through AlO<sub>x</sub> (12 mTorr oxygen) at 1 V is on the order of  $10^{-8}$  A cm<sup>-2</sup>, an order of magnitude lower than that in the previous study. We performed X-ray photoelectron spectroscopy (XPS) on the  $AlO_x$ samples to investigate their chemical composition. The inelastic mean free path of electrons in  $AlO_x$  is less than 5 nm at 1420 eV—the maximum electron kinetic energy in this XPS measurement<sup>28</sup>. Therefore, the angle between the photoelectron detector and the sample stage was tilted by 80° to ensure that all of the measured photoelectrons came from  $AlO_x$ . The atomic ratio of  $AlO_x$  as a function of oxygen pressure is shown in Fig. 2b; lower oxygen pressure during the plasma resulted in a higher relative ratio of oxygen. (Note that the oxygen ratio was overestimated to some degree because oxygen and water molecules adsorbed on the AlO<sub>x</sub> surface cannot be completely removed even under high-vacuum conditions.) Thus, the insulating property of  $AlO_x$  is improved with the increase in the oxygen ratio. The thickness of AlO<sub>x</sub> fabricated at an oxygen pressure of 12 mTorr was measured to be 5.7 nm by transmission electron spectroscopy (TEM), as shown in the inset of Fig. 2b. By assuming a dielectric constant of 9.5 for the  $AlO_x$  layer, the measured thickness is in good agreement with the capacitance value above.

We fabricated GFETs on a Scotch tape made of polytetrafluoroethylene (PTFE,  $50\mu$ m). First, the Scotch tape substrate was attached on a SiO<sub>2</sub> wafer for ease of fabrication. The as-purchased Scotch tape had a large surface roughness, so a thin polyimide layer ( $9\mu$ m) was spin-coated on the tape; the polyimide layer significantly reduced the roughness of Scotch tape, as shown in Fig. 3. To create gate electrodes, aluminum was evaporated using a shadow mask on the sample. Then, the gate dielectric was formed on the aluminum layer by oxidizing the surface by oxygen plasma at 12 mTorr, as described above. Gold source/drain electrodes were evaporated on the AlO<sub>X</sub> gate dielectric using a shadow mask. Finally, a graphene channel with polymeric protective layers was transferred onto the top by using the water-free transfer of graphene, as described in our previous study<sup>22</sup>. The sample was exposed to neither solvent nor temperatures of more than 150 °C during fabrication. The device structure is shown in Fig. 1a.

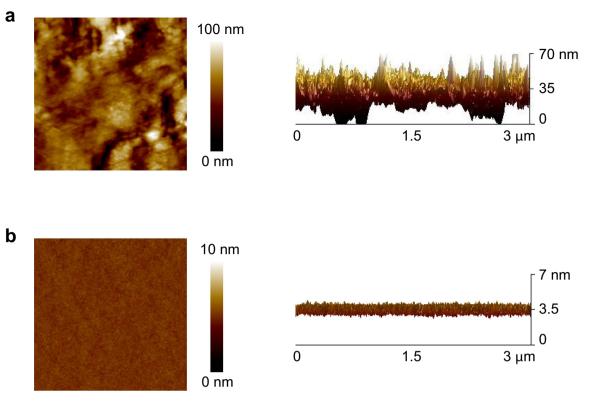


Figure 3. Height profile of Scotch tape surface measured by atomic force microscopy. The scan size is  $3 \times 3 \mu m$ . (a) As-purchased Scotch tape exhibited considerably high surface roughness. Root-mean-square roughness: 28.1 nm. (b) After spin coating of a thin layer of polyimide (9 $\mu$ m) on the Scotch tape, the surface roughness was significantly reduced to be similar as silicon wafer. Root-mean-square roughness: 0.225 nm.

First, we tested the  $AlO_x$  gate dielectric layer on the Scotch tape substrate. The measured capacitance was 1.5 (±0.3)  $\mu$ F cm<sup>-2</sup>, which is almost the same as that of the AlO<sub>x</sub> layer made on a SiO<sub>2</sub> substrate. The leakage current through the gate dielectric was an order of magnitude higher, and the breakdown voltage was approximately 0.5 V lower as compared to AlO<sub>x</sub> on SiO<sub>2</sub> (see Supplementary Information Fig. S1). These degraded insulating properties can be attributed to the soft substrate surface, which results in a rough bottom aluminum layer. Nonetheless, the  $AlO_x$  gate dielectric prepared on Scotch tape exhibited sufficient electrical performance such that it can be used in low-voltage GFETs with a negligible gate leakage. After fabricating the GFETs on the Scotch tape substrate (GFETs/Scotch), the GFETs/Scotch were separated from SiO<sub>2</sub> and attached on a banknote by using the adhesive remaining on the backside of Scotch tape (Fig. 4a). The electrical performance of the samples was measured, and the field-effect mobility ( $\mu_h$  for holes;  $\mu_e$  for electrons) values were extracted from a diffusive transport model of GFET (see Supplementary Information Table S1 for detailed parameters)<sup>29</sup>. As summarized in Fig. 4a,b, the electrical performance of the GFETs/Scotch did not appreciably change after being transferred onto a banknote. Another set of samples was separated from the SiO<sub>2</sub> wafer and attached on office paper. The paper was crumpled and flattened, and the electrical performance of the GFETs/Scotch was measured. As shown in Fig. 4c, GFETs/Scotch still exhibited satisfactory operation after extreme bending and showed only a slight decrease in mobility. In a previous study, a significantly thin layer of plastic foil substrate  $(2\mu m)$  was used to make crumpled organic transistor arrays<sup>30</sup>. The notable bending property was attributed to the remarkably low foil thickness, which can sometimes cause difficulties in handling it appropriately. However, the GFETs/Scotch prepared in the present work exhibited sufficient rigidity for facile use and attachment on various objects. The electrical performance of GFETs/Scotch under three different substrate conditions is summarized in Fig. 4d (see Supplementary Information Fig. S2 for drain current vs. drain-to-source voltage curves).

Excessive surface strain induces the formation of cracks or irreversible deformation when a flexible device is bent beyond its limit, which in turn results in permanent device failure. Therefore, the range of feasible bending radii is determined by the maximum surface strain exerted on the active layer. The maximum strain at the top layer of the bent GFETs/Scotch was obtained by employing a finite element analysis with two-dimensional (2D) plain strain condition<sup>31</sup>. As shown in Fig. 5a, two model structures were studied: Scotch tape attached on a sheet of office paper (Fig. 4c) and a commonly used polyimide film as a control sample. When an oxidized  $AIO_X/AI$  sample on polyimide was folded, the insulating property of  $AIO_X$  was completely lost, and crease marks remained. We imposed displacements on the bottom of the

а

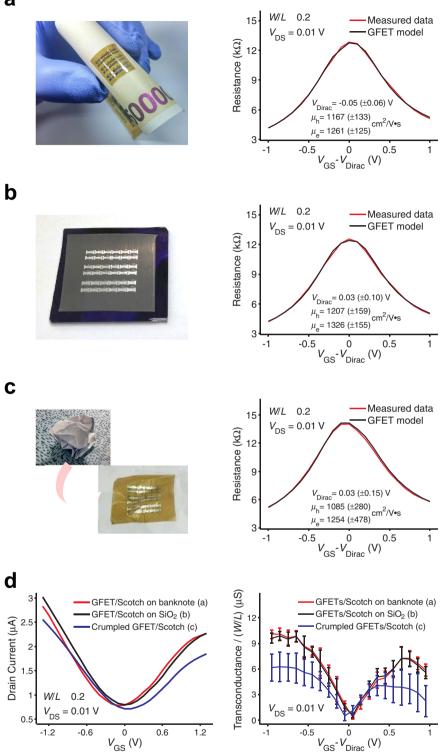


Figure 4. Electrical measurement data of graphene field-effect transistors on Scotch tape (GFETs/ Scotch). The channel width was fixed to  $85\,\mu$ m, and the width-to-length ratio (*W/L*) values were 0.2 and 0.45. (a–c) Transistor channel resistance vs. gate-to-source voltage curves for GFETs/Scotch attached on different substrates. (a) GFETs/Scotch samples were attached on a banknote. While the samples were bent with a bending radius of 0.5 cm, the electrical properties remained the same (the maximum surface strain was less than 1%, see Fig. 5). (b) As-fabricated GFETs/Scotch on a SiO<sub>2</sub> wafer. (c) The GFETs/Scotch on a paper were crumpled, flattened, and measurements were performed. (d) Performance summary of the GFETs/Scotch on the three different substrates. All measurements were performed in ambient air, and more than 10 devices were measured for each sample set.



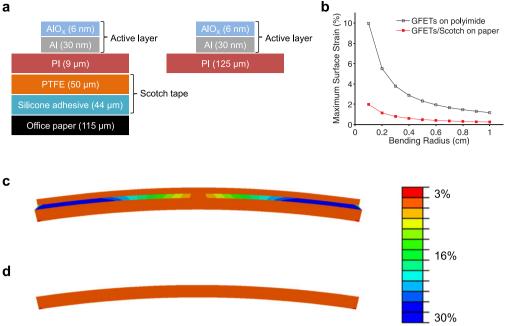


Figure 5. Finite element analysis on graphene transistors on Scotch tape. (a) Model structure for surface stain calculation [left: GFETs/Scotch on office paper; right: GFETs on a polyimide (PI) film]. (b) Surface strain data as a function of bending radius. Although the thickness of the GFETs/Scotch on the office paper is approximately twice that of the GFETs on polyimide, the surface strain on the GFETs/Scotch is five times lower. This result is attributed to the soft silicon adhesive interlayer, which relaxes the strain applied to the top surface. (c,d) Assuming the model structure in (a) is bent with a bending radius of 0.5 cm, the distribution of shear strain is calculated by using a finite element analysis. (c) GFETs/Scotch on office paper. The shear strain is concentrated in the silicone adhesive interlayer where the shear modulus is the lowest. (d) GFETs on a polyimide film. The shear strain is uniformly distributed.

structures corresponding to bending radii and measured the lateral strain at the center of the top layer. In Fig. 5b, the Scotch tape sample exhibits a significantly lower surface strain compared to regular polyimide sample by a factor of five at a given bending radius. This numerical analysis can be understood in light of a 2D shear-lag model, which describes strain propagation in multilayers<sup>32</sup>. When the bottom layer is subject to a uniform strain  $\varepsilon_{\text{bottom}}$ , the shear-lag model predicts the maximum strain at the top by Equation 2

$$\varepsilon_{\text{top, max}} = \varepsilon_{\text{bottom}} \cdot \left( 1 - \frac{1}{\cosh\left(\frac{L_{\text{top}}}{2\Lambda}\right)} \right)$$
(2)

where  $L_{top}$  is the lateral dimension of the top layer, and  $\Lambda$  is a parameter proportional to the  $\sqrt{\text{thickness/shear modulus of the middle layer. The reduced strain in the Scotch tape sample is attributed}$ to its soft silicone adhesive interlayer with a relatively low shear modulus, where mechanical load is not effectively transferred (see Fig. 5c,d). Therefore, the GFETs/Scotch on the office paper can be crumpled with a high degree of bending even though the total film thickness is greater than that of a typical polyimide sample. The effects of the strain-releasing adhesive layer are further corroborated by consecutive bending tests as shown in Fig. 6. A thin layer of aluminum deposited on the two substrate samples (Scotch tape attached on office paper and polyimide film) was bent and released consecutively with a bending radius of 1 mm. In Fig. 6, the aluminum layer on the Scotch tape substrate shows much less resistance increase against the mechanical strain from the bending and releasing, compared with the polyimide substrate. The less change on the resistance of the Scotch tape sample is attributed to its adhesive layer, which reduces the mechanical strain on the top.

We demonstrated flexible GFETs on a Scotch tape substrate. The GFETs/Scotch was easily laminated onto diverse nonconventional substrates, such as a pen, human skin, and a banknote, using Scotch tape adhesive. The soft nature of Scotch tape allows for the sample to be crumpled without leading to device failure. From mechanical calculations, we found that the Scotch tape adhesive with a low Young's modulus relaxes the strain applied to the top surface when the GFETs/Scotch sample is bent. For practical low-power electronic applications, high-quality AlOx was fabricated as the gate dielectric of the GFETs by oxygen plasma treatment. The AlO<sub>x</sub> exhibited a negligible gate leakage current, and a supply voltage of only 2.5 V was sufficient to operate the GFETs because of its high capacitance of  $1.5 \,\mu\text{F}\,\text{cm}^{-2}$ . We envision

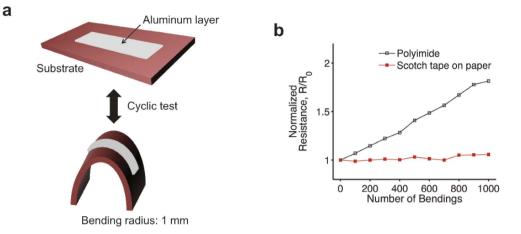


Figure 6. Resistance change of metal thin film against consecutive mechanical strain. (a) Schematic of device structure and experiment. A thin layer of aluminum (thickness: 300 nm; length: 2 cm; width: 0.2 cm) was deposited on a Scotch tape attached on office paper and a polyimide film. Detailed substrate structure is shown in Fig. 5(a). (b) Normalized resistance data of the aluminum layer as a function of the number of bendings. Electrical measurements were performed while the sample was flat. As explained in Fig. 5, the adhesive layer of the Scotch tape relaxes the strain applied to the top; therefore, the aluminum layer on Scotch tape exhibits much less increase on its resistance value against mechanical strain than the aluminum on the regular polyimide substrate.

that such a device concept for flexible graphene transistors on Scotch tape can be exploited and extended to ubiquitous electronic applications wherein electronics can be easily placed in any desired position.

#### Methods

**Fabrication of graphene transistors on Scotch tape.** Scotch tape (3M<sup>TM</sup>, 5480) was attached on a silicon dioxide wafer piece. A polyimide solution (VTEC<sup>TM</sup>, PI-1388) was coated onto the Scotch tape sample at 3000 rpm for 30 s, followed by sequential baking at 60 and 150 °C for 10 min. An aluminum layer (30 nm) as gate electrodes was deposited in a thermal evaporator with a shadow mask. The aluminum surface was oxidized in an oxygen plasma chamber with an RF power of 250 W for 7 min to form the gate dielectric layer. During plasma treatment, the oxygen pressure was set to the lowest possible value while maintaining the plasma; the lowest pressure value was 12mTorr in our plasma chamber. Source/drain electrodes (40-nm-thick gold on 5-nm-thick titanium) were deposited in a thermal evaporator using a shadow mask. Finally, a graphene channel with polymeric protective bilayers was laminated on the top of the sample by employing the water-free transfer method as described in our previous study<sup>22</sup>. Poly(methyl methacrylate) and polybutadiene were used for supporting bilayers of graphene transfer and for passivation against detrimental ambient species to prevent Fermi level change33-35 and charge-impurity scattering<sup>36</sup>.

#### References

- 1. Wong, W. S. & Salleo, A. Flexible electronics: materials and applications. (Springer, 2009).
- 2. Gelinck, G. H. et al. Flexible active-matrix displays and shift registers based on solution-processed organic transistors. Nat Mater 3, 106-110 (2004).
- 3. Someya, T. et al. A large-area, flexible pressure sensor matrix with organic field-effect transistors for artificial skin applications. P Natl Acad Sci USA 101, 9966-9970 (2004).
- 4. Liu, X. T. et al. Flexible, Low-Voltage and High-Performance Polymer Thin-Film Transistors and Their Application in Photo/ Thermal Detectors. Adv Mater 26, 3631-3636 (2014).
- 5. Sun, Q. et al. Transparent, Low-Power Pressure Sensor Matrix Based on Coplanar-Gate Graphene Transistors. Adv Mater 26, 4735-4740 (2014).
- 6. Sekitani, T. et al. Organic Nonvolatile Memory Transistors for Flexible Sensor Arrays. Science 326, 1516-1519 (2009).
- 7. Kim, M. et al. Lateral Organic Solar Cells with Self-Assembled Semiconductor Nanowires. Adv Energy Mater 5, 1401317, (2015). 8. Chen, Z. et al. A Three-Dimensionally Interconnected Carbon Nanotube-Conducting Polymer Hydrogel Network for High-
- Performance Flexible Battery Electrodes. Adv Energy Mater 4, 1400207 (2014). 9. Ziemelis, K. Putting it on plastic. Nature 393, 619-620 (1998).
- 10. Kim, D. H. et al. Epidermal Electronics. Science 333, 838-843 (2011).
- 11. Andersson, P. et al. Active matrix displays based on all-organic electrochemical smart pixels printed on paper. Adv Mater 14, 1460 - 1464 (2002)
- 12. Zschieschang, U. et al. Organic Electronics on Banknotes. Adv Mater 23, 654 (2011).
- 13. Khan, M. A., Bhansali, U. S. & Alshareef, H. N. High-Performance Non-Volatile Organic Ferroelectric Memory on Banknotes. Adv Mater 24, 2165-2170 (2012).

- 14. Avouris, P. Graphene: Electronic and Photonic Properties and Devices. Nano Lett 10, 4285-4294 (2010).
- 15. Bae, S. et al. Roll-to-roll production of 30-inch graphene films for transparent electrodes. Nat Nanotechnol 5, 574–578 (2010).
- 16. Wang, H., Nezich, D., Kong, J. & Palacios, T. Graphene Frequency Multipliers. IEEE Electron Device Letters 30, 547-549 (2009).
- 17. Lee, E., Lee, K., Liu, C. H., Kulkarni, G. S. & Zhong, Z. H. Flexible and transparent all-graphene circuits for quaternary digital modulations. *Nat Commun* **3**:1018, doi: 10.1038/ncomms2021 (2012).
- 18. Schwierz, F. Graphene transistors. Nat Nanotechnol 5, 487-496 (2010).
- 19. Chen, C. Y. et al. Graphene mechanical oscillators with tunable frequency. Nat Nanotechnol 8, 923-927 (2013).
- DuPont Fluoroproducts, Teffon<sup>®</sup> PTFE fluoropolymer resin: Properties Handbook. (DuPontTM Technical Report H-37051-3, 1996); DuPontTM Kapton<sup>®</sup> HN Technical Data Sheet. (2011) Available at: http://www.dupont.com/content/dam/assets/products-and-services/membranes-films/assets/DEC-Kapton-HN-datasheet.pdf (Accessed: 7th October 2014).
- Lee, J. et al. 25 GHz Embedded-Gate Graphene Transistors with High-K Dielectrics on Extremely Flexible Plastic Sheets. ACS Nano 7, 7744–7750 (2013).
- 22. Kim, H. H., Chung, Y., Lee, E., Lee, S. K. & Cho, K. Water-Free Transfer Method for CVD-Grown Graphene and Its Application to Flexible Air-Stable Graphene Transistors. *Adv Mater* 26, 3213–3217 (2014).
- 23. Kim, B. J. et al. High-Performance Flexible Graphene Field Effect Transistors with Ion Gel Gate Dielectrics. Nano Lett 10, 3464–3466 (2010).
- 24. Thiemann, S. et al. Cellulose-Based Ionogels for Paper Electronics. Adv Funct Mater 24, 625-634 (2014).
- 25. Klauk, H., Zschieschang, U., Pflaum, J. & Halik, M. Ultralow-power organic complementary circuits. *Nature* 445, 745–748 (2007).
- 26. Lieberman, M. A. & Lichtenberg, A. J. Principles of plasma discharges and materials processing. 2nd edn (Wiley-Interscience, 2005).
- 27. Chung, Y., Murmann, B., Selvarasah, S., Dokmeci, M. R. & Bao, Z. N. Low-voltage and short-channel pentacene field-effect transistors with top-contact geometry using parylene-C shadow masks. *Appl Phys Lett* **96**, 133306 (2010).
- Powell, C. J. & Jablonski, A. Evaluation of calculated and measured electron inelastic mean free paths near solid surfaces. J Phys Chem Ref Data 28, 19–62 (1999).
- 29. Kim, S. et al. Realization of a high mobility dual-gated graphene field-effect transistor with Al2O3 dielectric. Appl Phys Lett 94, 062107 (2009).
- 30. Kaltenbrunner, M. et al. An ultra-lightweight design for imperceptible plastic electronics. Nature 499, 458 (2013).
- 31. Bathe, K.-J. r. Finite element procedures. (Prentice Hall, 1996).
- 32. Sun, J. Y. et al. Inorganic islands on a highly stretchable polyimide substrate. J Mater Res 24, 3338-3342 (2009).
- 33. Kim, H. H. et al. Substrate-Induced Solvent Intercalation for Stable Graphene Doping. ACS Nano 7, 1155-1162 (2013).
- Kim, H. *et al.* Doping Graphene with an Atomically Thin Two Dimensional Molecular Layer. *Adv Mater* 26, 8141 (2014).
   Lee, S. K. *et al.* Inverse Transfer Method Using Polymers with Various Functional Groups for Controllable Graphene Doping.
- ACS Nano 8, 7968–7975 (2014).
  36. Lee, W. H. *et al.* Control of Graphene Field-Effect Transistors by Interfacial Hydrophobic Self-Assembled Monolayers. *Adv Mater* 23, 3460 (2011).

#### Acknowledgements

This work was supported by the Center for Advanced Soft Electronics under the Global Frontier Research Program (2012M3A6A5055728) of the Ministry of Science, ICT and Future Planning and by the Basic Science Research Program (NRF-2013R1A1A2012046) through the National Research Foundation of Korea funded by the Ministry of Education. The authors thank Professor Bong Koo Kang for discussions.

### **Author Contributions**

Y.C. and H.H.K. conceived the idea and performed experiments and measurements. S.L. and S.R. conducted mechanical simulations. E.L. and S.W.K. performed experiments on strained aluminum films. K.C. directed the research project. Y.C. wrote the paper. All authors discussed the results and commented on the manuscript.

#### Additional Information

Supplementary information accompanies this paper at http://www.nature.com/srep

Competing financial interests: The authors declare no competing financial interests.

How to cite this article: Chung, Y. et al. Ubiquitous Graphene Electronics on Scotch Tape. Sci. Rep. 5, 12575; doi: 10.1038/srep12575 (2015).

This work is licensed under a Creative Commons Attribution 4.0 International License. The images or other third party material in this article are included in the article's Creative Commons license, unless indicated otherwise in the credit line; if the material is not included under the Creative Commons license, users will need to obtain permission from the license holder to reproduce the material. To view a copy of this license, visit http://creativecommons.org/licenses/by/4.0/