Novel Methods of Utilization, Elimination, and Description of The Distortion Power in Electrical Circuits

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This thesis is dedicated to

My Parents, who sacrificed a lot for me and inspired me the meaning of sacrifice and success

My wife, who is the source of happiness in my life and my companion to the way of success

My brother, and sisters who helped me in my life

My children, who make my life full of beauty

My friends, and my ancestors city (Kirkuk)

To all people who I love

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Novel Methods of Utilization, Elimination, and Description of The Distortion Power in Electrical Circuits

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Abstract

Firstly, this thesis investigates the electrical power harmonics in an attempt to utilize harmonic current and its distortion power in a novel idea to reconvert the distortion power into useful power. This is done, in order to feed different DC or AC loads in single and three-phase power system by using passive or active filters and accordingly, develop a new topology of hybrid active power filter (HAPF). In addition, this circuit can be considered as a power factor corrector (PFC) because it reduces the total harmonic distortion (THD) and improves the power factor (PF).

Secondly, this thesis works on a new design of active power factor correction (APFC) circuit presenting two circuits with the same design principle: the first design consists of two active switches without an external complex control circuit, while the second design contains a single active switch with an additional control circuit. The main contribution of this circuit is 98% reduction of the inductor's value used in the newly proposed PFC circuit in comparison with the conventional boost converter which may lead to a huge reduction in size, weight and the cost of the new PFC circuit.

Also, the active switches depend on a carefully designed switching pattern that results in an elimination of the third order harmonic from the input source current which decreases the value of total current harmonic distortion (THD_I) to (14%) and improves the input PF to (0.99). Consequently, the simplicity of the design without requiring a complex control circuit and without a snubber circuit plus the minimum size of inductor, gives the newly proposed circuit the superiority on other PFC circuits.

Thirdly, this research aims to describe the distortion power through submitting two novel power terms called effective active power (P_{ef}) & reactive power (Q_{ef}) terms with a new power diagram called Right-Angled Power Triangle (RAPT) Diagram. In addition, a novel definition of total apparent power (S_t) has been submitted in order to illustrate the physical meaning of (S_t) in non-sinusoidal systems.

The new RAPT Diagram is based on the orthogonality law and depends on geometrical summation to describe the relationship between different aspects (apparent-active-reactive) of power, and different components (total-fundamental-distortion), drawing a bridge to connect the time domain with the frequency domain in a two-dimensional diagram.

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Chapter 1

Introduction

1.1 Background of Thesis

The electrical power grid has been designed to be compatible with linear loads and sinusoidal currents and voltages. However, the existence of non-linear loads and non-sinusoidal currents and voltages compel researchers to use additional equipment in order to make the electrical systems consistent with the variety of loads [1]. The power system harmonic is a subject of continuous research since first identified as a problem in the power grid system in 1892 in [2]. This was the first time a problem that affects an electric equipment had been addressed using harmonic analysis as a tool. This happened when a distorted power was observed as a distorted voltage and current waveforms in the power grid [3].

In the past, the amount of distortion in a power system has been non-significant, because of the lack of using variable frequency equipment. However, with the invention of power electronics (PE) devices and a large number of applications which are used in daily life, the level of harmonic currents and voltages in a distribution power system is highly considerable, and poses a serious problem to the power grid. Therefore, nowadays any power system requires careful analysis of the harmonics generation and measurements. Also, requires a comprehensive

study on the deleterious effects, methods of controlling and reducing the harmonics amount to an acceptable level [1].

Since the last decade of the 19th century until today, electrical engineers worked intensively to successfully invent several methods to eliminate harmonics and distortion power from the system in order to dispose of the harmful effects of the harmonics on system equipment, and on the power quality in general [3].

On the other hand, harmonic power had been used as a useful element in many electrical applications and engineers tended to take advantage of the harmonic as it is a fixed part in the power system [4], [5]. The first part of this research investigates a novel idea to take benefit of harmonic current in order to feed different electrical loads.

At present, the design of the majority of contemporary digital and electronic appliances contain AC/DC power conversion circuits within their architectures, and is widely used in adjustable speed drives (ASD), switch mode power supplies (SMPS) and uninterrupted power supplies (UPS) equipment [6]. These devices are non-linear loads and result in the generation of harmonics at the source side. Therefore, researchers have invented many solutions in order to decrease the THD, obtain the unity PF at the input side and achieve regulated output voltage at the output side [7]. However, the size, cost and design simplicity are always comparative parameters among power factor correction (PFC) circuits.

The second part of this research has been dedicated to the design of a new PFC circuit using a simple design without external complex control circuit, and a small size inductor (less than 98% of the inductor used in a traditional boost convert).

The distortion power (D), was first defined in 1927 [8] with the beginning of the first power theory. Since then, researchers have tried to redefine the distortion power in many forms using time and frequency domains in order to describe it accurately as it is an important component to understand the characteristics of the non-sinusoidal electrical system. Accordingly, two new power terms called

effective active power (P_{ef}) and effective reactive power (Q_{ef}) with a novel power diagram called right-angled power triangle (RAPT) Diagram and new definition of total apparent power (S_t) in non-sinusoidal power systems have been presented in the third part of this thesis.

1.2 Overview of Distortion Power

The losses of power quality under non-sinusoidal conditions was characterized by non-useful power called the distortion power (D), which has been introduced as equation 1.1, by Budeanu in 1927 [8]. Distortion Power was defined as:

$$D^2 = S^2 - P^2 - Q^2 \tag{1.1}$$

S: The apparent power (VA).

P: The active (Real) power (Watt).

Q: The reactive power (Var).

1.2.1 Definition of Power Harmonics

According to [9], harmonics can be defined as "a sinusoidal wave (current or voltage), having frequencies that are integer multiples of the frequency at which the supply system is designed to operate". Distorted waveforms can be produced by merging harmonics with the fundamental wave [10].

1.2.2 Definition of Total Harmonic Distortion (THD)

Total harmonic distortion can be defined as: "The ratio of the summation of root-mean-square of the harmonic contents to the root-mean-square value of the fundamental quantity, expressed as a percent of the fundamental" as described

in [10]. THD, can be described as in equation 1.2:

$$THD = \sqrt{\frac{\sum \text{of squares of amplitudes of all harmonics}}{\text{Square of the amplitude of the fundamental}}} \text{x } 100\% \tag{1.2}$$

1.2.2.1 Equations for Common Harmonic Indices

RMS voltage in presence of harmonics can be written as the following equations [1]:

$$V_{rms} = \sqrt{\sum_{h=1}^{h=\infty} V_{h,rms}^2} \tag{1.3}$$

And similarly, the expression for the current is:

$$I_{rms} = \sqrt{\sum_{h=1}^{h=\infty} I_{h,rms}^2} \tag{1.4}$$

The total distortion factor for the voltage is:

$$THD_V = \frac{\sqrt{\sum_{h=2}^{h=\infty} V_{h,rms}^2}}{V_{1,rms}} \tag{1.5}$$

Where $V_{1,rms}$ is the fundamental voltage. This can be written as:

$$THD_V = \sqrt{(\frac{V_{rms}}{V_{1,rms}})^2 - 1} \tag{1.6}$$

or

$$V_{rms} = V_{1,rms}\sqrt{1 + THD_V^2} \tag{1.7}$$

Similarly,

$$THD_I = \frac{\sqrt{\sum_{h=2}^{h=\infty} I_{h,rms}^2}}{I_{1,rms}} = \sqrt{(\frac{I_{rms}}{I_{1,rms}})^2 - 1} \tag{1.8}$$

$$I_{rms} = I_{1,rms}\sqrt{1 + THD_I^2} \tag{1.9}$$

Where $I_{1,rms}$ is the fundamental current.

1.2.3 Interharmonics

IEC-61000-2-1 Standards in 1990, defines interharmonic as follows: "Between the harmonics of the power frequency voltage and current, further frequencies can be observed which are not an integer of the fundamental. They can appear as discrete frequencies or as a wideband spectrum" [11].

Harmonics and interharmonics of a waveform can be defined regarding its spectral components in the quasi-steady state over a scope of frequencies. Table (1.1) supplies an ordinary, yet efficient mathematical definition:

Table 1.1: Harmonics types

Harmonic	f = h x f_1	where h is an integer > 0
DC	f = 0 Hz	f = h x f, where (h) = 0
Interharmonic	f ≠ h x f_1	where h is an integer > 0
Sub-harmonic	f > 0 Hz & f < f_1	f_1 is the fundamental power system frequency

The term sub-harmonic is a special case of interharmonic for frequency components less than the system frequency.

1.2.3.1 Sources of Interharmonics

The main source among interharmonic sources is the cycloconverter. Cycloconverters are well-established, reliable units used in a variety of applications from rolling-mill and linear motor drives to static-var generators [11]. Other sources of interharmonics are:

1. Induction motors (wound rotor and sub-synchronous converter cascade).
2. Induction furnaces.
3. Integral cycle control (heating applications).
4. Low frequency power line carrier (ripple control).

1.2.4 Definition of Power Factor

Power factor (PF) is defined as: "the ratio of the real power (P) to apparent power (S)", as shown in equation 1.10; or it is the cosine (for pure sine wave for both current and voltage) of the phase angle between the current and voltage waveforms.

$$PF = \frac{\text{Real Power}}{\text{Apparent Power}} \tag{1.10}$$

Real power (watts) produces a real work; this is the energy transfer element. Reactive power is the required power to generate the magnetic fields to enable the real work to be done, where apparent power is considered the total power that the power company supplies. This total power is the power supplied by the power mains to produce the required amount of real power [12].

If the current and the voltage are both sinusoidal and in phase, the power factor (PF) is unity. If both are sinusoidal but not in phase, the power factor is the cosine of the phase angle. In elementary courses in electricity, this is sometimes taught as the definition of the power factor, but it applies only in the special case,

where both the current and voltage are pure sine waves. This occurs when the load is composed of resistive, capacitive and inductive elements and all are linear (invariant with current and voltage) [12].

As a result of the input circuitry, switched-mode power supplies (SMPS), present a non-linear impedance to the mains. The input circuit normally consists of a half-wave or a full-wave rectifier followed by a storage capacitor.

Assuming an ideal sinusoidal input voltage source, the power factor can be expressed as the product of the distortion factor and the displacement factor. The distortion factor (K_d), is the ratio of the fundamental root-mean-square (RMS) current (I_{1rms}) to the total RMS current (I_{rms}). The displacement factor (k_θ) is the cosine of the displacement angle (ϕ) between the fundamental input current and the input voltage. For sinusoidal voltage and non-sinusoidal current, equation 1.11 can be expressed as:

$$PF = \frac{V_{rms} I_{1rms} \cos\phi}{V_{rms} I_{rms}} = \frac{I_{1rms}}{I_{rms}} \cos\phi \tag{1.11}$$

The distortion factor (K_d) is given by the following equation:

$$K_d = \frac{I_{1rms}}{I_{rms}} \tag{1.12}$$

The displacement factor (K_θ) is given by the following equation:

$$K_\theta = \cos\phi \tag{1.13}$$

$$\therefore PF = K_\theta . K_d \tag{1.14}$$

$$\therefore PF_{Total} = PF_{displacement} . PF_{distortion} \tag{1.15}$$

The displacement factor (K_θ) can be easily made unity with a capacitor or inductor, but making the distortion factor (K_d) unity is more difficult. When a converter has less than unity power factor, it means that the converter absorbs apparent power higher than the active power. This means that the power source has a higher VA rating than what the load needs. In addition, the harmonic currents generated by the converter in the power source affects other equipment [1].

1.3 Relationship Between PF & THD

The following equations link total current harmonic distortion to power factor.

$$THD(\%) = \sqrt{(\frac{1}{K_d^2} - 1)} \times 100\% \tag{1.16}$$

$$K_d = \frac{1}{\sqrt{1 + (\frac{THD(\%)}{100})^2}} \tag{1.17}$$

Therefore, when the fundamental component of the input current is in phase with the input voltage, $K_\theta = 1$. Then, in this case: PF $= K_d.K_\theta = K_d$

Then:

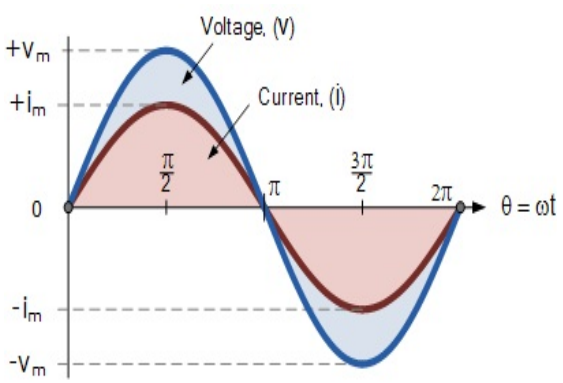
$$PF = \frac{1}{\sqrt{1 + (\frac{THD_I(\%)}{100})^2}} \tag{1.18}$$

The purpose of the power factor correction circuit is to minimize the input current distortion and make the current in phase with the voltage.

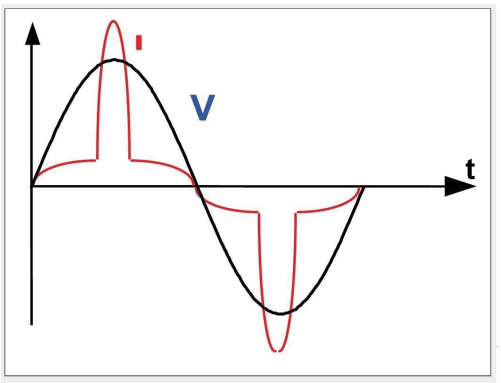
When the power factor is not unity, the current waveform does not follow the voltage waveform. Consequently, power losses may increase and may transfer to the neutral line and damage other equipment connected to the line [1].

1.4 Reason of Harmonics

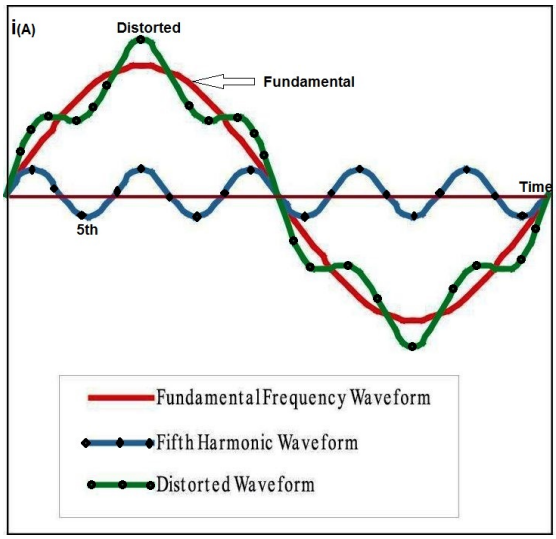
PE devices which represent non-linear loads are the main reasons for harmonic existence in the power grid. Harmonics are generated when non-linear devices inject current with recursive pulses. As a result of harmonics current, non-linear voltage drops happened at the point of common coupling (PCC) in the power system [1]. A linear component in power grids is an item that draws a current waveform which is same as the voltage as shown in figure 1.1a. On the other hand, the current waveform on a non-linear load is not the same as the voltage as shown in figure 1.1b.



(a) Waveforms at linear load



(b) Waveforms at non-linear load



(c) Input waveform at non-linear load

Figure 1.1: Waveforms of linear, non-linear and harmonic components

Regular examples of non-linear loads include rectifiers, uninterruptable power supply (UPS) units, discharge lighting, adjustable speed motor drives, electric ballast, vapour mercury, halogen spotlight, halogen with dimmer and arcing equipment. The current drawn by non-linear loads is not sinusoidal but is periodic. Periodic waveforms can be defined mathematically as a series of sinusoidal elements that have been summed together as shown in figure 1.1c. The sinusoidal elements are integer multiples of the fundamental frequency (50 Hz) [13].

As previously mentioned, PE apparatus are the main sources of the harmonics. However, the economic gains of using PE devices are much more important than losses caused by harmonics which may be produced by these apparatus. As a result of this growing, the harmonics generation rate extremely increased to be higher than its elimination rate in the distribution system [14].

1.5 Harmful Effects of Harmonics

The effect of non-linear loads causes a discontinuous current which shapes harmonic current on power systems. This harmonic current, affect the electrical grid negatively and lead to different problems. The general problems focused on thermal overloading, disruption, and dielectric stressing [15]. According to [16–18], high degrees of stress or harmonic distortion can lead to problems for the utility's power grid distribution, ineffective power system and many drawbacks on the grid equipment. In general, these effects can be summarized as below [19]:

1. A reactive power overload, resonance, and harmonic amplification may cause a capacitor bank failure. This would cause nuisance fuse operation.

2. Excessive losses, heating, harmonic torques, and oscillations in induction and synchronous machines, which may give rise to torsional stresses.

3. Increase in negative sequence current loading of synchronous generators,

endangering the rotor circuit and windings.

4. Generation of harmonic fluxes and increase in flux density in transformers, eddy current heating, and consequent derating.

5. Over voltages and excessive currents in the power system, resulting from resonance.

6. Derating of cables due to additional eddy current heating and skin effect losses.

7. Inductive interference with telecommunication circuits.

8. Signal interference in solid-state and microprocessor-controlled systems.

9. Relay malfunction.

10. Harmonics interference with ripple control and power line carrier systems, causing misoperation of the systems, which accomplish remote switching, load control, and metering.

11. Unstable operation of firing circuits based on zero-voltage crossing detection and latching.

12. Interference with large motor controllers and power plant excitation systems.

13. The possibility of sub-synchronous resonance.

1.6 Harmonic's Effect on Equipments

Harmonics have deleterious effects on electrical equipment; these problems can be summarized as the following:

1. Capacitors: Harmonic components cause additional heating and higher dielectric stress on the capacitors, which would cause a nuisance fuse operation. Harmonics also, cause capacitor bank failure because of a reactive power overload, and an increasing of harmonic distortion [19]. A large current or voltage at the resonance frequency would be produced if an additional capacitor tuned to the system near a harmonic frequency [20].

2. Circuit Breakers and Fuses: There are many proofs show that the harmonic distortion of the current can affect the cut-off ability of circuit breakers. The authors in [21] describe 15 kV breaker failures due to harmonic currents. The author in [22], has described how a distortion can affect the current sensing ability of thermal magnetic breakers.

3. Conductors: Harmonic currents can cause heating in conductors which are greater than expected based on the RMS value of the current. This happens because of two reasons: Firstly, the current redistribution within the conductor and this include the skin effect and the proximity effect. In [23], Rice presents formulas and tables for the effective or AC conductor resistances due to skin and proximity effects. The second reason is due to generating a significant amount of 3rd harmonic currents because of using some non-linear loads.

4. Electronic Equipment: Several phenomena show the effects of harmonic distortion on electronic equipment. The first effect is the multiple voltage zero crossing problem, which is usually used for timing purposes [20]. Furthermore, PE switches should work at zero crossing voltage point in order to decrease electromagnetic interference (EMI) and inrush current [24].

However, harmonic distortion causes multiple zero crossings which may disrupt the operation of the electronic equipment (e.g. a household digital clock) [20]. Electronic power supplies use peak voltage of the waveform to maintain the filter capacitors at full charge. Harmonic voltage distortion can increase or flatten the waveform peak, and with a severe distortion, equipment operation may be disrupted [20].

Fractional and sub-harmonics can affect video displays or televisions. The authors in [25] have found that even 0.5 % of a fractional harmonic (referred to the rated terminal voltage) produces periodic enlargement and reduction of the image of the cathode ray tube.

5. Lighting: Incandescent lamps, are sensitive to varying operating voltage levels. Therefore, a possibility of loosing these lamps will significantly increase when operated with distorted voltages. In [26], the author presents an expression shows that a lamp life will decrease 47 %, if a continuous operation reached 105 % rated RMS voltage.

6. Meters: Modern RMS responding voltmeters and ammeters are relatively immune to the influences of waveform distortion as it uses an electronic multiplier. However, average responding meters and peak responding meters are not suitable in the presence of harmonic distortion because they were calibrated in RMS value. For example, with a chopped sine wave signal at a firing angle of 45°, an absolute averaging meter will indicate an RMS value about 13% less than the true RMS value due to the effect of harmonics [20].

7. Protective Relays: Waveform distortion may reduce the performance of protective relays. For low magnitude faults, the load may consist of a large part of the load current and distortion can become a significant factor. Distortion can prevent a relay trip under fault conditions, or it may cause nuisance tripping when no fault exists. Varying the phase angle between the fundamental and harmonic components of a voltage or current waveform can also

affect the response of the relay [27], [28].

8. Rotating Machines: Adjustable speed drivers (ASD) are fed by inverters that usually produce significant voltage distortion. However, non-sinusoidal voltages applied to electric machines may cause overheating, pulsating torques, or noise [20].

   Rotor over heating is the main problem associated with voltage distortion. An increase in motor operating temperature will cause a reduction in the motor operating life [29]. Pulsating torques are produced by an interaction between the air gap flux (mainly the fundamental component), and the fluxes produced by the harmonic currents in the rotor [30].

   The authors in [31], conclude that audible noise is produced by the difference among time-harmonic frequencies. Therefore, inaudible high frequency harmonics can also contribute to audible noise.

9. Telephone Interference: The proximity of telephone wires and power lines on utility poles creates opportunities for power frequency interference with telephone communication. Power system harmonic frequencies can present greater problems than fundamental frequency because a human hearing sensitivity and telephone response peak is near one kHz [20].

10. Transformers: The elementary effect of power system harmonics on transformers is the additional heat generated by the losses caused by the harmonic content of the load current.

    The probability of resonance between the transformer inductance and system capacitance may cause another problem. The mechanical insulation stresses due to temperature cycling is another bad effect of harmonics on transformer [32].

    The additional heating caused by system harmonics may reduced the transformer's life as a result of operating above rated temperatures [20].

11. Synchronous generators: According to [33], the voltage regulation of a synchronous generator under various load conditions is related to different levels of harmonic distortion produced by the non-linear load. Furthermore, the additional power losses incurred by harmonics affected the overall temperature rise and local overheating.

1.7 Thesis Aims and Construction

Generally, this thesis discuss the ability of utilization the harmonics power, explores the characteristics of the distortion power, reduces the THD_I & improves the input PF and reduces the value of the main inductor of PFC circuit. This research, consists of three main branches as presented in figure 1.2.

The first branch, concentrated on the utilization of harmonic current which has been drawn at the high-frequency side of the passive filter and causes distortion power. This idea can be implemented by re-converting the distortion power into a useful power (sinusoidal), in order to feed different DC or AC loads in single and three-phase power system. This is achieved by using passive or active filters and can be considered a power factor corrector (PFC) as it reduces THD value and improves the PF.

The second branch of this research, focused on presenting two new circuits of active power factor correction (APFC). The main contribution of this project is to reduce the inductor's value of a PFC circuit more than 98% in comparison with the conventional boost converter which may lead to a reduction of size, weight and the cost of the PFC circuits, decreasing the value os THD_I and improving the input PF into 0.99 .

The first design consists of two switches without an additional control circuit, and the second circuit uses the same idea but with a single switch and the additional control circuit. Consequently, the simplicity of the design as it doesn't require a

complex control circuit or a snubber circuit, together with the main advantages, gives the newly proposed circuit priority over other PFC circuits.

The third branch of this thesis aims to re-describe the distortion power in two-dimensional diagram instead of using Budeanu's three-dimensional diagram depending on the orthogonality law among power components. This two-dimensional power diagram has been designed through submitting two novel power terms called effective active power (P_{ef}) & effective reactive power (Q_{ef}) terms with novel power diagram called Right-Angled Power Triangle (RAPT) Diagram.

Also, a novel definition of total apparent power (S_t) has been submitted in order to illustrate the physical meaning of apparent power (S_t) in non-sinusoidal systems more precisely and overcome the shortcomings of existing definitions. The new RAPT Diagram and the new power terms, may help to understand and describe the physical meaning of the distortion power and opens the door for new methods for calculating the power components in non-sinusoidal power systems.

This thesis is organised into five chapters as following: Chapter 2 presents the first branch of the thesis illustrating the ability to feed electrical loads via utilization of harmonic current and harvest the distortion power instead of losing it. This chapter, contains a literature review, three different circuits representing three methods to implement this idea together with the assessment of results, and the conclusion have supported the validation of the idea.

Chapter 3 offers the second branch of the thesis which is the investigation of APFC in the systems using AC to DC converters. This chapter starts with a literature review and continues with two methods achieving high input PF, low THD_I, more than 98% reduced value of inductor in comparison with traditional boost converter at the same power ratings and flexible output ripple.

Chapter 4 describes the distortion power by inventing two new power terms and a new power diagram containing all the power components in non-sinusoidal systems.

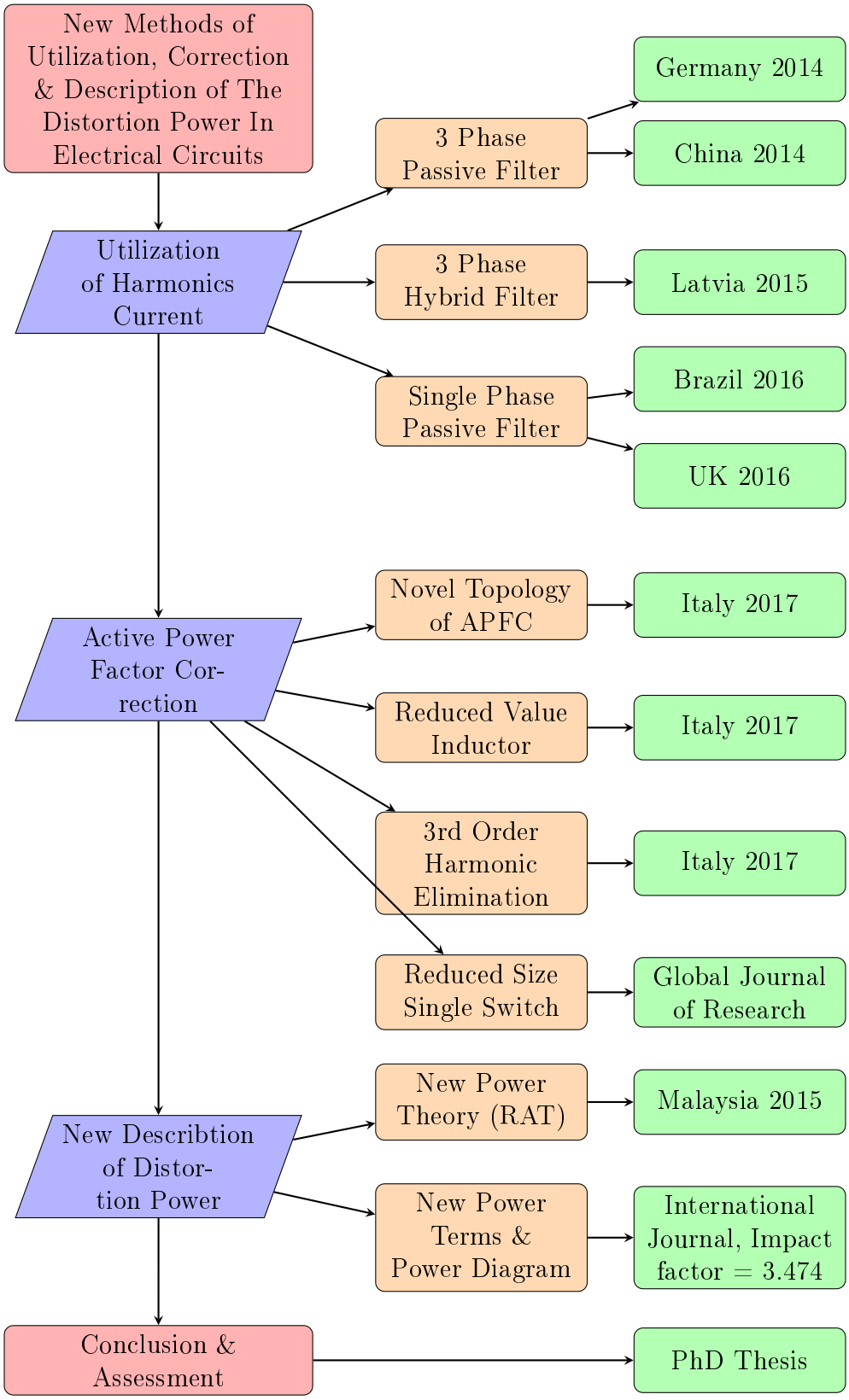


Figure 1.2: Thesis Structure & Publications

This chapter consists of an overview of the most well-known power theories and corresponding literature in order to justify the newly proposed power diagram. Furthermore, a new definition of the apparent power in non-sinusoidal power systems has been proposed. A description of the orthogonality law leads us to derive and show mathematically the relationship between the geometrical summation ($P_{ef.}$) and the arithmetical summation ($P_{avg.}$) of power. Finally, examples have been presented in order to prove the new RAPT Diagram. Chapter 5 explains the perspectives of future work of each branch of study.

1.8 Contribution to Knowledge

1. **Utilize Harmonics as a Load Feeder & Power Factor Corrector**:

   The main aims of this chapter were to investigate the ability to benefit harmonic current and harvest the distortion power (i.e. it's non-invested power) through conversion to useful (sinusoidal) power and feed different electrical loads. In addition, it can be considered as a power factor corrector (PFC) because it reduces the THD_I. The proposed circuits in Chapter (2) contribute to the power system in many aspects:

   (a) Utilizing the non-invested power and feed electrical loads. The net utilized power amount is small (2 Watt) but its extracted from a distortion ratio of 43.35% without drawing additional source current. By using a single-phase passive filter and RL-load, practically small load can be used (e.g. a string of lighting emitting diodes (LEDs)).

   Note that without a doubt, the amount of utilized power (output power) is increases proportionally with the type of harmonic source (non-linear load) and the harmonics amount produced.

   (b) Developing a new topology of three-phase HAPF which adds a new functionality to the HAPF which is by utilizing the distortion power

and converting it to useful power, in addition to HAPF's original functions. The utilized power (P_u) is 34.2 kW (when R = 1 Ω), and (P_u) is 4.84 kW (when R = 10 Ω). However, this design is not efficient practically because of the high current source and has restrictions on load types (only resistive) and load value limitations.

(c) Consequently, the THD_I% of the system has been decreased from 43.35% to 2.1% in a single-phase model and from 74% to 1.9% for a three-phase HAPF model. Consequently, the input and output PF improve dramatically.

These contributions are presented by the author and published in :

- H. Al-bayaty, M. Ambroze, and M. Z. Ahmed, "A Novel Idea to Benefit of The Load Sides Harmonics," in 16th International Conference on Electrical and Power Engineering (ICEPE, 2014).
- H. Al-bayaty, M. Ambroze, and M. Z. Ahmed, "Taking advantage of the harmonics at the load side using passive filters," in Systems and Informatics (ICSAI), 2014 2nd International Conference on, Nov 2014, pp. 169 - 174.
- H. Al-bayaty, M. Ambroze, and M. Z. Ahmed, "The benefit of harmonics current using a new topology of hybrid active power filter," in 2015 IEEE 5th International Conference on Power Engineering, Energy and Electrical Drives (POWERENG), May 2015, pp. 330 - 336.
- H. Al-bayaty, M. Ambroze, and M. Ahmed, "Utilization of harmonics current in single phase system," in 2016 17th International Conference on Harmonics and Quality of Power (ICHQP), Oct 2016, pp. 443 - 447.
- H. Al-bayaty, M. Ambroze, and M. Ahmed, "Feeding loads via harmonics utilization in ac circuit systems," in 2016 International Conference for Students on Applied Engineering (ICSAE), Oct 2016, pp. 224-227.

2. **Novel Design of Active Power Factor Correction (APFC)**:

   A new method of APFC has been presented in order to eliminate third order harmonic current from the input source side which decreases the value of THD_I and improves the input PF to 0.99 .

   The main contribution of this project is to reduce the inductor's value of PFC circuit more than 98% in comparison with the conventional boost converter. The proposed design has many advantages:

   (a) The simplicity of the design, because it does not require an external control circuit and does not need a snubber circuit.

   (b) The flexibility of changing the output ripple voltage value (in wide range of voltage), presents the proposed circuit as a successful alternative for power factor pre-regulator in two-stage AC/DC converters.

   (c) Low losses and high power conversion efficiency of around 98%.

   (d) The small size, light weight and low cost.

   These contributions have been accepted and presented in 17th international IEEE conference on environment and electrical engineering 2017 in Italy:

   - "A Novel Topology For Single Phase Active PFC Circuit," IEEE 17th International Conference on Environment and Electrical Engineering and 1st Industrial and Commercial Power Systems Europe, Italy, 2017.
   - "A New Design For PFC Circuit With Reduced Size Inductor," IEEE 17th International Conference on Environment and Electrical Engineering and 1st Industrial and Commercial Power Systems Europe, Italy, 2017. (Accepted and presented).
   - "Third Order Harmonic Elimination Technique For APFC Circuit," IEEE 17th International Conference on Environment and Electrical Engineering and 1st Industrial and Commercial Power Systems Europe, Italy, 2017. (Accepted and presented).

- "Reduced Size Single Switch Power Factor Correction Circuit" in Global Journal of Researches in Engineering in GJRE Volume 17 Issue 5 Version 1.0 .

3. **Two Novel Power Terms, and Apparent Power Definition Using a New RAPT Diagram**:

   (a) The main aim is to find a new simple two dimensional diagram instead of using Budeanu's theory as he uses three dimensional power diagram. The new RAPT Diagram has been structured based on the orthogonality law between all power components including total, fundamental & distortion components, in the non-sinusoidal situation.

   (b) Create two new power terms called effective active power (P_{ef}) term and effective reactive power (Q_{ef}) term which may help in defining and calculating the total apparent power (S_t) in non-sinusoidal system depending on the orthogonality law.

   (c) The new RAPT Diagram and the new power terms, may help to understand and describe power components and opens the door for new methods of calculating power components in non-sinusoidal power systems. This is done in order to illustrate more precisely the physical meaning of (S_t) in non-sinusoidal systems and overcome the shortcomings of the existing definitions as explained in Chapter Four.

These contributions are presented by the author and published in:

- Al-bayaty H, Ambroze M, Ahmed MZ. A new power theory (right-angled triangle theory). In: IEEE conference on energy conversion (CENCON), October 2015. p. 451 - 456.
- H. Al-bayaty, M. Ambroze, and M. Z. Ahmed, "New effective power terms and right-angled triangle (rat) power theory," International Journal of Electrical Power & Energy Systems, vol. 88, pp. 133 - 140, 2017.

Chapter 2

Utilize Harmonics as a Load Feeder & Power Factor Corrector

2.1 Literature Review of Harmonics Elimination

The electrical power system has been designed to work with a sinusoidal voltage and current at a constant frequency. Non-linear loads, introduce random harmonic components on the electrical grid, resulting in undesirable voltage and current waveform [34]. The harmonic distortion is an old phenomenon though it has been discovered since the 19th century [3]. The main issue at that time was the effect of harmonics on electrical machines and interference with telephone lines.

However, harmonics have become an increasingly important issue as more facilities have begun to use more variable frequency drives (VFDs) creating a significant burden on our utility grid, due to the effects of harmonics mentioned previously in the first chapter. The invention of power electronics (PE) devices and rapidly increasing use of (VFDs) in many devices have a significant effect on the power quality of the AC power system raising concerns and causing serious problems for public utilities, distribution systems the customers because of the harmonics increasing [1].

Different methods have been used to eliminate harmonics current from the power system [35, 36]. Due to the simplicity of it's design, ease of control, low cost and variety of types, the use of a passive filter is one of the most popular methods. However, this depends on the principle of providing a low impedance path through X_L (for low frequencies) and low impedance through X_C (for high frequencies) in order to take out the harmonic current and isolating it [37].

The total harmonic distortion (THD) is restricted by IEEE-standards limitation for each subsystem. However, for a huge power system with high power ratings (MW) (especially, with the rapid increase of non-linear loads in our daily life), the total harmonic current will increase rapidly. Accordingly, we can conclude that the system loses every day a non-invested harmonic power (in kW) and hundreds of harmonic current in total by isolating it.

As an example, if we have a power supply with a non-linear load that draws fundamental current ($I_1 = 70$ A) and harmonics current ($I_h = 20$ A), so the supply has to feed total supply current $I_t = 72.8$ A, because $I_t^2 = I_1^2 + I_h^2$, and $THD_I = 28.5\%$. In this case the useful current is I_1 and the non-invested (lost) current which is going to be isolated, is I_h. In this case, 20 A is the targeted current as a non-invested power which can be converted to a useful sinusoidal current in order to feed different loads by using conventional methods (rectifier plus inverter or active front end).

The next section summarises concisely, the harmonics elimination methods which have been invented and developed over more than one century. Later on, a brief discussion will be provided to show the attempts that have been developed in the area of utilization of harmonics in different topics in the electrical system.

2.1.1 Literature of Harmonics Elimination Methods

Different methods have been used to eliminate the harmonics from the power system, which vary from changing the design of VFDs to adding new equipment to perform the same aim. These methods can be summarized as follows:

1. Steinmetz work: Steinmetz, proposed many solutions to overcome the harmonics problem. Some of these solutions were:

   (a) Reducing the system frequency, which was 125 Hz at that time, to one-half of its original value of 62.5 Hz [3].

   (b) Re-stacking iron laminations in the motor, to withstand the higher operating voltage [3].

   (c) Δ Connection: This method consists of connecting reactances in delta configuration. This set is commonly known as the Steinmetz circuit, whose design aims to obtain reactance values to symmetries consumed currents [38].

2. Multipulse Converters: The prime multiphase converter is a six-pulse unit. Theoretically, input current harmonics for rectifier circuits are a function of pulse number and can be expressed as: $h = (n \times p) \mp 1$

   where n= 1, 2, 3,... etc., and p= number of pulses,

   Third-order harmonic will be eliminated in a six-pulse rectifier. For a twelve-pulse system, 3rd, 5th and 7th harmonics will be eliminated [39]. In the same way, in an 18-pulse front end converter [40, 41] and 24-pulse front end converter [42], have been used in order to reduce the harmonic orders.

   However, although this method reduces the magnitude of the harmonics, it does not eliminate them. The disadvantages of this method are the high cost and bulky design which requires an auxiliary transformer to achieve

the 30 ° phase shifting. This method also, decreases the efficiency rate due to voltage drop associated with the design requirement [43].

3. ($\Delta - \Delta$) and (Δ - Y) Transformers: This method uses two separate transformers with equal non-linear loads. The design is similar to the previously mentioned 12 pulse converter circuit with the same drawbacks [39].

4. The Magnetic Flux Compensation Method: This method has been proposed to eliminate normal harmonics and abnormal harmonics in a transformer core [44]. However, this method is limited to transformer applications.

5. Zigzag Transformer: This type of transformer has been used for creating a neutral line, and reduces the heating effect of the harmonic current in a three-phase distribution system [45, 46].

6. DC-Choke: This is merely a series inductance on the DC side of the bridge circuit on the front end of the adjustable frequency drive (AFD)and before the capacitor, as designed in [47].

   The DC-Choke method has many advantages such as:

   (a) Being integrally packaged to the AFD.

   (b) Can provide a moderate reduction in voltage and current harmonics.

   (c) Has less voltage drop than an equivalent line reactor.

   (d) Cost effective way.

   On the other hand, some of the drawbacks are:

   (a) Less protection than other methods for the AFD input semiconductors.

   (b) May not reduce harmonic levels to below IEEE 519-1992 guidelines.

7. AC Line Reactor: This is an AC series choke, placed in front of the rectifier on the source side. The line reactor may result in a voltage drop and due to being inductive, the series impedance and hence voltage drop is larger; therefore, the frequency is higher [35].

   The advantages of The AC-line reactor can be summarized as, a low cost approach, which can reduce the current distortion efficiently ($THD_I = 35\%$), and adds protection to the rectifiers. In addition, it works as a buffer for surges and other transients.

   On the other hand, it has some drawbacks, as it is impractical in large drives, larger than DC-choke, increase losses as it causes a voltage drop, and do not meet harmonic limit standards.

   Both AC line reactors and DC link chokes help to smooth out the flow of current to the VFDs and thereby reduce the level of harmonics [35].

8. Third-order Harmonic Injection Technique: The 3rd order harmonic injection technique in controlled converters, was first introduced in 1969, in order to reduce the harmonic current at the source side [48]. The principle is to injects 3rd orders in 180 ° phase shift in order to cancel the 3rd order harmonic at the input side [49]. This method has been used with uncontrolled converters in [50].

9. Active Front End (AFE): Active front end rectifier, is a bridge controlled rectifier used to minimize the amount of THD by drawing nearly sinusoidal current from the power grid. It has many categories like 12-pulse, 18-pulse and 24 pulse rectifiers which reduce switching frequency [36]. AFE, has been regarded as a very effective suppression of harmonics, and an excellent power factor supplier. Moreover, it has the ability to feed energy back to the grid, and it is insensitive to network unbalance [51]. In spite of its advantages, AFE has many drawbacks which limited its popularity. These disadvantages [35] can be summarized as:

(a) The active rectifier must transmit full load power.

(b) A large and complex design.

(c) The Switch ripple on grid side and higher switch ripple on motor side due to boost voltage.

(d) High losses and expensive (due to using active switches in high frequencies).

(e) Impossible to retrofit.

10. Unipolar and Bipolar Switching: It's one of the methods which is used to reduce the total harmonic distortion (THD) of any controlled circuit is by changing the waveform to be more sinusoidal. According to [52], the PWM switching control can be achieved by using Unipolar and Bipolar switching techniques. In [53] a set of transcendental equations have been formulated in order to determine the times (i.e. angles) in an electrical cycle for turning the switches ON and OFF in a full wave bridge inverter. In [54], a programmed harmonic elimination method has been submitted as the switching angles are chosen and programmed to eliminate specific harmonics.

11. Passive Filters: This method is still the most convenient method used due to its simplicity of design, ease of control, low cost and variety of types [14]. The main idea of using passive filters is to benefit from the characteristics of the inductor and the capacitor, by providing low impedance path through X_L (for low frequencies) and low impedance through X_C (for high frequencies) in order to take out the harmonic current and grounding it [37,55]. However, these filters suffer from some drawbacks such as:

(a) The amplification of harmonic currents on the source side at specific frequencies. This is because of the parallel resonance between filter and source impedances that cause additional losses.

(b) The series resonance between filter and source impedances, may also cause voltage distortion which creates extreme harmonic currents flowing through the filter [14].

(c) For high power applications, the passive filter needs to be designed with a high current capability because both the harmonics and the fundamental current components flow into the filter; therefore, the passive filter consumes high power as losses at low frequency [56].

(d) The compensation characteristics of the passive filters can be affected by frequency variation of the AC source. As a result, the size of the components in each tuned branch becomes impractical if the frequency variation is significant [57].

12. Active Power Filter (APF): In order to overcome the problems associated with passive filters, active power filters were invented in 1976 by Gyugyi [58]. Active power filters (APF), have different topologies and multiple categories, but mostly they use voltage source converters. APF has a voltage source at the DC bus, which is usually a capacitor as an energy storage device.

    In recent years, APF has become popular because of its accurate reactive power compensation and current harmonics elimination ability [59]. Also, according to [60], APF has many advantages such as:

    (a) APF can calculate and subtract the harmonics current.

    (b) APF does not spend any real power because the power consumption is not more than its requirement for internal losses.

    (c) APF, is able to work with variable load states.

    (d) Having immediate response features and adequate bandwidth in order to compensate for different harmonic currents.

    (e) Involving state of the art power semiconductor devices and tools; therefore, it is reliable and compact.

Unfortunately, APF suffers from many problems which include high initial set-up costs, high running costs and requires high power converter ratings. The input and output power rating are limited by power supply voltages and sometimes this is very close to load ratings [57]. According to [61], a single active filter does not provide a complete solution for compensation in many cases of non-linear loads due to the presence of both voltage and current power quality problems.

13. Unified Power Quality Conditioner (UPQC): UPQC, is the only correct filter to provide perfect compensation. It is a combination of two APF's (Series and shunt). The role of series APF is to isolate the voltage harmonics between the source and the load, and it regulates the voltage. In addition, it compensates the flicker and voltage unbalances at the PCC [62], while the purpose of shunt APF is to compensate the load current harmonics, the reactive current and the unbalanced currents [63]. However, this combination is very complex to control and results in high-cost equipment and is the costliest filter [64].

14. Hybrid Active Power Filter (HAPF): HAPF, is one of the harmonic elimination methods. It has been invented in order to collect all the advantages of other types of filters and overcome their limitations. It is a combination of a passive filter with an active power filter together in one system. This method is described thoroughly in the next section.

2.1.1.1 Literature Review of HAPF

Since the first installation of a tuned filter in the mid-1930's, the use of filters to solve harmonic problems has been an area of continuing research [65]. Active components were proposed as early as 1976 [58]. Many incremental progressions have been made and hybrid active filters were developed with detailed attention. The paper by Gyugi [58] in 1976 denotes and presents a spectrum of topologies. Reviews of active filters for power quality improvements [57–59, 61, 66, 67], are beginning to appear and are important in the classification and selection of such devices.

The HAPF, has already been an effective and widely-used method for power quality improvement [67]. HAPF was first proposed by M. Takeda in 1988 [68] and was invented in order to collect the advantages of other types of filters and overcome their limitations. It is a combination of a passive filter with an active power filter in one system as defined by the author in [57], the design and structures which will be explained in the next subsections.

In many cases, APFs can provide effective compensation, but their ratings and costs are much higher compared to the HAPF [69]. The rating of the APF element in the HAPF's combination can be reduced as little as 5% and less than 20% in some cases [70]. Additionally, HAPF is less sensitive to variations in the parameters than passive filters when used alone [71].

In recent years, a series of hybrid filters have evolved and used extensively in practice as a cost-effective solution for the compensation of non-linear loads [72]. Moreover, these hybrid active power filters (HAPFs) are found to be more effective in providing a complete compensation of various types of non-linear loads [72].

HAPFs are more attractive in harmonic filtering than pure APFs from both the viability and economical view points [73]. Furthermore, the unified power quality converter (UPQC), has been developed in order to achieve the best performance. However, this remains a very complex and expensive approach [74].

Multi functional HAPFs were unknown until 2005. In the period between 1976 to 2005, HAPF was mostly used for industrial traditional use [67]. New areas have been the centre of research after 2005. These areas are the progress of industrial applications, optimum design and dynamic reactive power compensation. Many researchers [75–77], have talked over the viability of HAPF in railways and renewable sources such as wind farms and PV cells. The initial costs and operating losses of PE switches restrain the efficiency and readiness of HAPF; therefore, some methods of more optimal design have been proposed in several areas. For example, parameter selection [78], control method [79], and structures.

The authors in [61], have presented a comprehensive literature review on HAPF configurations and classified them into many categories and described them under many conditions such as: control approaches, state of the art design considerations, selection criteria, potential application, future development and their comparative features; there exist more than 150 research publication at present on the HAPF.

In 2000 [80], the authors have ordered the categories of HAPF in five sections, namely: power rating and response speed, configuration and connection, compensated system parameters, control methods, and reference signal estimating technique.

In 2005, the performance of three types of HAPFs had been debated minutely. Namely, the hybrid of an active shunt and a passive series, the hybrid of an active series and a passive shunt, and a transformerless LC-HAPF [81].

In 2012, the author of [82], split 10 HAPFs into 2 parts: shunt filter and series filter. In the same article, five basic control techniques were also debated, and these were termed: Fourier transform, synchronous reference frame, p-q theory, HPF method, LPF method, and adaptive linear neurons control method.

In 2013, the authors of [72] classified all HAPFs according to topology, converter configuration, supply system, passive filter type and listed some new control meth-

ods in harmonic detecting and controller techniques.

The authors in 2015 [67], attempted to exhibit the progress of HAPF's structure historically. The functions and structures are the two main criteria have been relied on in the discussion.

2.1.1.1.1 The Review of HAPF's Functionality :

The historical periods of the development of HAPF function have been divided into three stages: origin (inception) stage, developing (evolution) stage and mature (ripening) stage as mentioned in [67]. The figure 2.1 can explain the historical development of the purposes of the use of HAPF.

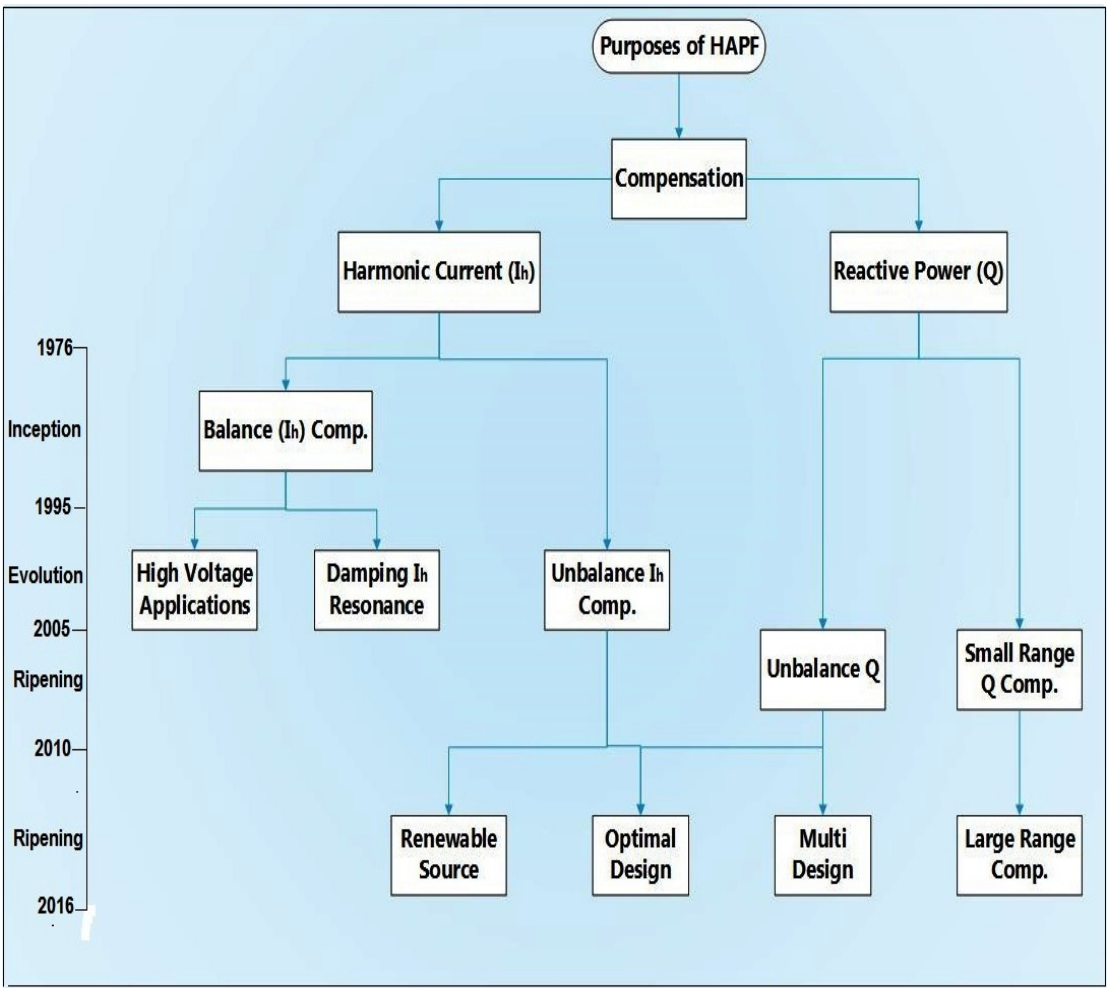


Figure 2.1: Development of the functionalities of HAPF

1. Harmonic Current (I_h) Compensation:

   The first purpose of using HAPF is the (I_h) Compensation. The time between 1976 and 1995 represents the inception stage. Researchers, used HAPF for damping the balance (I_h) and harmonic resonance. However, a medium voltage system was the maximum value which can be used for HAPF at that time [83].

   The role of harmonic compensation came into an evolution period in the second interval which starts from 1996 until 2005. This period had been expanded into three main routes; high-voltage application, damping harmonic resonance, and unbalance harmonic compensation [67].

   The third interval starts with 2005 till 2016, can be called the ripening period. Most of the published articles concentrated on three characteristics to include: renewable source, multi-function, and optimal design. Other researchers work on the (I_h) compensation on some new applications, such as high-speed railways [75], photo-voltage (PV) generators [77] and wind farms [76].

2. Reactive Power (Q) Compensation:

   Var generators can be used for reactive power (Q) compensation. The progress of this function has started late (since 2005) because engineers thought that (Q) compensation would only be possible with low power ratings and the use of power factor correction (PFC) circuits is one of the requirements [84].

   The author of [85] in 2005, was the first who combined additional roles such as harmonic current, a small range of dynamic and unbalance reactive power, for medium and low-voltage applications [67].

   Afterwards, during the period 2009 to 2016, many types of research concentrated on the multi-purposes of HAPF in different applications and variable

usages, as listed in [86]. With the extension of the range of (Q) compensation, the combination of shunt HAPF and other controllable (Q) compensating circuit were all presented in [87].

2.1.1.1.2 The Review of HAPF's Structures :

The authors in [67] classified the HAPF structure based on the type of devices mixture. The structures of the HAPF were divided into four routes: parallel APF and parallel passive element; parallel APF series with a passive element; b-shape HAPF; neutral-line compensation structure. Figure 2.2 shows a summary of the evolution of the HAPF structure in the last few decades.

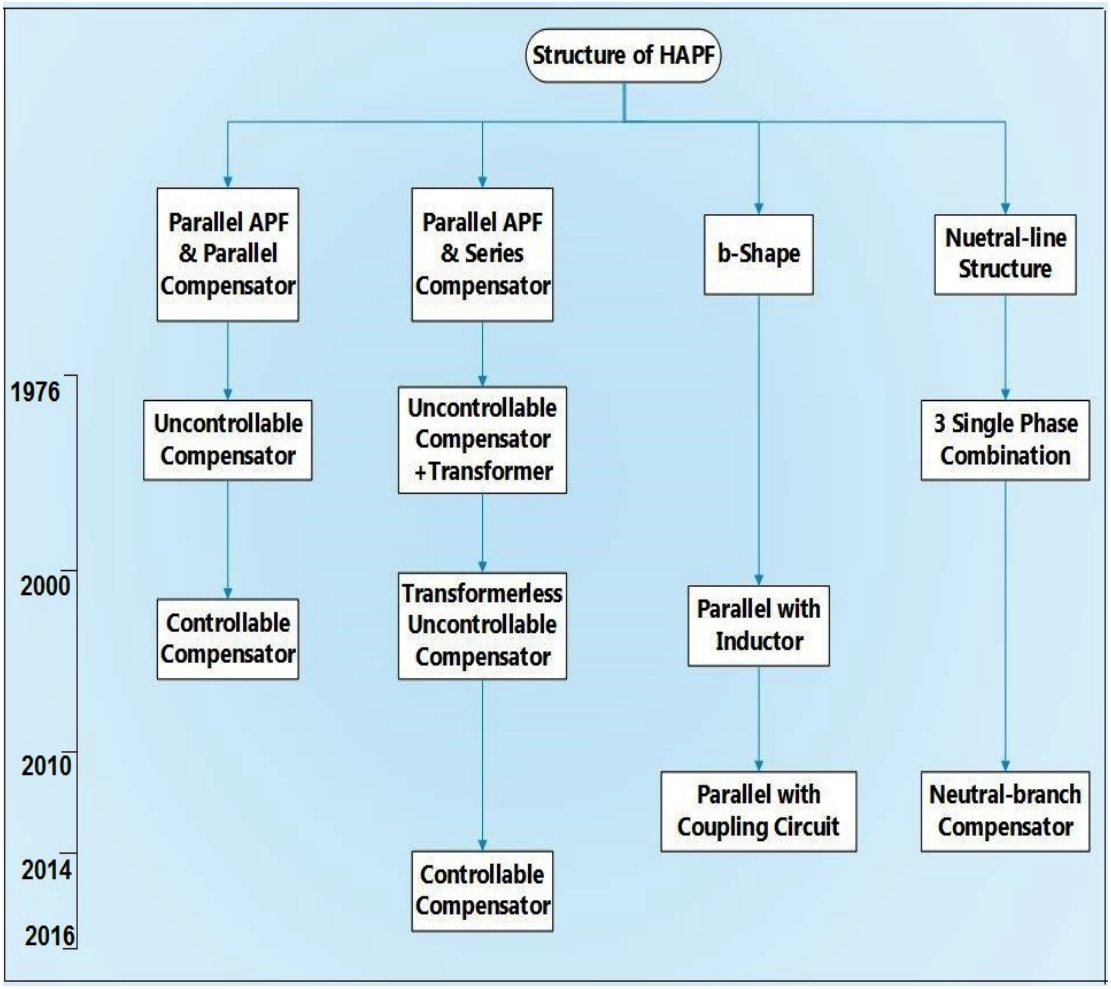


Figure 2.2: Development of the Structures of HAPF

1. Parallel APF and parallel compensator

   This construction can be divided into two intervals based on the ability to control the parallel compensator portion. The main benefit of this structure is the stability as both components are independent of each other.

   (a) Non-controllable Parallel Compensator

   The time between 1976 and 2001, can be termed the period of the uncontrollable parallel compensator. This structure is a mixture of parallel APF and passive power filter (PPF) [88]. The aim of modelling APF part is to compensate high-order current harmonics, while the aim of using the PPF part is to compensate the larger-capacity and low-order harmonics. Unfortunately, this design has two drawbacks: the first is the high operating losses and the second is the high initial costs.

   (b) Controllable Parallel Compensator

   The time between 2002 and 2016, can be termed the period of the controllable parallel compensator. In this interval, many controllable devices such as a full-bridge converter and TCR, etc. have used instead of a traditional uncontrollable devices. In comparing with uncontrollable elements, the controllable parallel components give a better performance for dynamic compensating.

   In 2012, the author of [89] suggested a mixture of low and high frequency HAPF to operate in parallel in order to achieve better performance. This design has a wide harmonic compensating range with less switches.

   In addition, the authors in [87] presented a structure of parallel APF and a parallel TCR circuit in 2013. This structure can be useful for asymmetrical and non-linear loads in the function of current harmonic.

2. Parallel APF + Series Device

The structure of a parallel APF in series with the compensator has a low operating loss, each part of the configuration affecting each other. Based on the series part, there are three essential historical periods for this structure type, classified as a transformer and a parallel component.

(a) Uncontrollable Series Compensator + Transformer

The design of LC-HAPF has been used by many researchers with a transformer structure during the interval from 1990 to 2000 [90]. In this structure, the APF has been connected with a coupling LC part in series with a transformer. It is suitable for medium and high voltage applications, as the passive component decreases the fundamental voltage applied to switches.

(b) Uncontrollable Transformerless Series Compensator

The style of HAPF has been amended with the presence of high voltage IGBT during the time between 2001 to 2013, with the evolution of performance PE switches [91]. The initial cost has been decreased hugely during this interval, because of the APF which can directly linked to a passive filter without any transformer.

The typical transformerless HAPF was proposed in 2003 [91] and this design extensively used in industry. The compensating range of (Q) is restricted to the fixed LC circuit, but it is effective in harmonic and (Q) compensating.

In 2013 a combination of a parallel insulated-gate bipolar transistor (IGBT) converter and a parallel metal oxide semiconductor field-effect transistor (MOSFET) converter was proposed in [92]. The IGBT converter supports the fundamental voltage and compensates the fundamental (Q). The MOSFET converter fulfills the function of (I_h) compensation [92]. Although, this structure has a wide compensating

range, the 12 switches which have been used in this topology add a drawback to the design in terms of high initial cost.

(c) Controllable Transformerless Series Compensator

During the years 2014 - 2016, a new topology of a controllable series compensator has been proposed. A combined system of a thyristor controlled reactor, and a shunt hybrid power filter was first proposed in 2014 in [93]. This topology has a larger Q compensating range than the last generation, by utilize the TCR circuit.

3. b-Shape HAPF

A new structure of two external passive filters linked together in series but when one of them is connected in parallel with an APF, then this combination is termed (b-shape HAPF). The current rating of the APF is less than normal due to the parallel element. Whereas the harmonic portion of the compensating current will flow into the external part.

(a) Parallel With Inductor

During the interval 1999 - 2008, the regular b-shape topology form an APF connected with a combination of a series linked capacitor with a parallel inductor. In 1999, the authors proposed the b-shape HAPF [94]. The parallel part can hugely decrease the rating of the APF due to the small value of the inductor. While it requires a big value of inductor for fundamental Q compensation.

(b) Parallel With Fundamental Coupling Circuit

Between 2009 and 2016, a novel b-shape HAPF was presented [95]. This structure was termed injection-HAPF. The injection circuit of this topology is a combination of a series capacitor and a parallel connected fundamental coupling circuit. This system has a very low DC voltage as the parallel branch can reduce the fundamental voltage largely. This

topology cannot compensate the dynamic (Q) because the fundamental voltage of the APF is almost zero.

4. Neutral Line Compensation Structure

   The harmonic in the neutral line for 3-phase 4-wire systems, should be considered. There are essentially three regular and widely accepted topologies:

   (a) Combination of Single Phase Compensator

   Between 1976 and 1994, many researchers use multiple combination of single-phase HAPF to compensate the harmonic current (I_h) in a 3-phase 4-wire system as explained in [96].

   This topology has good performance in unbalance (I_h) compensating without the use of a complex control method. However, this topology requires a big number of switches which causes a very high initial cost and operating loss.

   (b) Neutral-Branch Compensator

   The time between 1995 to 2016, has been called the interval of neutral-branch compensator [67]. Two new topologies, midpoint 4-wire and 4-pole, 4-wire HAPFs were presented and widely used in 3-phase, 4-wire system with fewer switches [97]. The neutral harmonic current can be compensated by an external bridge; terefore, the 4-pole HAPF is accommodated to a medium-voltage application.

2.1.2 Literature of Harmonics Utilizations

Researchers had tried to invest in the harmonics phenomenon through using it in some applications in order to address some problems, such as:

1. **Islanding Detection**: Islanding has many adverse effects on the power grid as described in [98]. According to IEEE standards-1547.1 [99]. The island is

defined as "the condition in which a portion of an electric power system is energised solely and separated from the rest of the power system; therefore, distributed generation has to detect the loss of mains and disconnect as soon as possible" [4]. Several techniques using both passive and active methods have been proposed for islanding detection.

According to [98], islanding can be detected by measuring the harmonics which have been generated by the over modulating inverter. In the active method, odd order harmonics can be injected within limited values of less than 5% THD in order to detect islanding [100].

2. **Power Exchanger in DPFC**: One of the components within the Flexible AC Transmission System (FACTS) family, is the Distributed Power Flow Controller (DPFC). The DPFC can be considered as a unified power flow controller (UPFC), with an eliminated common DC link. The main principle of DPFC is in using the third harmonic frequency as an active power exchanger between the shunt and series converters instead of the common DC link [101, 102].

3. **Identification of Problems**: An accurate measurement of harmonics and an on-line analysis of the system's harmonics, are necessary to properly identify the cause of problems and to recommend appropriate solutions. This usually involves a harmonic analysis of the current or voltage waveforms observed in the electrical system [5].

4. **Improving Inverter Utilization**: Harmonic injection enables an improvement in the DC bus utilization for the multiphase voltage source inverter (VSIs). A generalized concept of (n_{th}) harmonic order injection for n-phase inverter was presented in [103]. The linear modulation range is extended by injecting the (n_{th}) harmonic order. This increases the maximum fundamental output voltage without moving into the over-modulation region [103].

   In addition, a third order harmonic component was proposed to increase the

utilization of the inverters in [104]. Also, according to [105], the addition of a third harmonic component may be used to suppress the peak of the reference sine wave in order to extend the operating range of the inverter.

5. **Losses Reduction Method**: The overall harmonic structure of the waveform may be favourably rearranged in order to reduce motor losses. The authors in [106] proposed a new technique to add a third harmonic order to the PWM reference signal before modulation to alter the harmonic spectrum of sinusoidal PWM inverters and thus reduce motor losses. The most effective level of third-harmonic distortion can be determined by considering the adverse influence voltage harmonics can have on motor performance [106].

2.1.3 The Novelty of Harmonics Utilizations (The Gap in Knowledge)

As previously described, harmonics have often been cited as the source for a great variety of problems. Engineers have attempted to specify the harmonic limits for bus bar loads, in order to solve this problem. IEEE-519-1992 standards [107], provides a guideline for total harmonic distortion (THD) limits that are being increasingly enforced by utility companies around the world, in an attempt to maintain power quality for their customers [107].

In the last century, researchers have invented the aforementioned methods in order to cancel, mitigate or eliminate harmonic currents and voltages. However, to this present time and to the best of the author's knowledge, researchers have not focus on harmonics as an exploitable power, and they have not intended to invent a method for harvesting harmonic current and voltage which is called harmonic power or Distortion power (D), in order to use this power for feeding electrical loads.

This research proposes a sustainable idea to invest harmonic power instead of

grounding and wasting it by using two methods in order to utilize harmonics power as a useful power supply in order to feed different loads.

This thesis presents a novel idea to take advantage of harmonics current instead of wasting the harmonic power. The author proposes as a first method, to use passive filters to extract the harmonics from the system by offering low impedance HPF for high frequencies of more than 50 Hz and convert these harmonics to a DC current and then reconvert it to a sinusoidal AC current to feed small loads. More descriptions will be provided in the methodology's section of this chapter.

The second method presents a novel configuration of 3-phase HAPF connecting the capacitor branch of LPF in parallel with a shunt APF in order to compensate the harmonics current and convert it to sinusoidal current.

In comparing with the existing configurations of the HAPF in [61], researchers have not designed a HAPF in this configuration. In addition, the newly proposed HAPF topology presents a new functionality for the HAPF, which is feeding electrical loads through utilization of distortion power by compensating harmonics in order to feed electrical loads.

2.2 Methodology of Harmonics Utilization

In this chapter, two methods have been proposed in order to investigate the goal of the research in single and three-phase systems. These circuits have been designed and tested using the Matlab-Simulink program.

1. Using a passive filter in order to take the harmonics current out of the circuit and convert it to a DC power as a first step and then using a voltage source inverter (VSI) in order to produce a sinusoidal AC current to feed electrical loads.

2. Using an active filter in combination with a passive filter leads to construct

a new topology of Hybrid Active Power Filter (HAPF). This filter can be used to reduce harmonics current, and consequently, increases the input PF remarkably resulted in unity PF. The main reason for the newly proposed HAPF is to utilize harmonics power and feed electrical loads.

2.2.1 Using Passive Filters

This method uses a passive filter in order to draw harmonic current by using HPF, and convert it to DC current as a first step through using a bridge rectifier and a capacitor as a reservoir element. This DC power can be used to feed DC loads (e.g. LEDs) or charge DC batteries. For the second step, a voltage source inverter (VSI) can be used to invert DC power into AC current in a sinusoidal form and unity PF to feed AC loads.

Passive filter method has been designed and investigated by using the Simulink-Matlab program. Firstly, in 3-phase systems in order to judge the performance of this system, and secondly, working on a single-phase method in order to simplify the circuit.

2.2.1.1 Three Phase Passive Filter Method

The idea of taking advantage of harmonics power and feed electrical loads via using passive filters has been applied to a 3-phase system.

A simplified schematic diagram of the circuit is shown in figure 2.3; the circuit consists of a three-phase 11 kV power source, connected in series with (point 1) with a 3-phase step down (11/0.4) kV transformer in (Y - Δ) connection.

This circuit also contains a low pass filter (LPF) at point 2. The duty of the LPF is to mitigate harmonics above 50 Hz at the source side and isolate load side harmonics. Here, an LPF will connect in shunt with a three-phase non-linear load at point 3 which produces harmonic currents. The non-linear load in this

circuit has been represented by a single-phase AC voltage source working on 150 Hz (represents a distortion power source) in between two phases together with a back to back thyristor ($\alpha = 90$) in another phase connected with three phases RL-load.

LPF only passes the fundamental wave current (50 Hz) towards the source and blocks all the frequencies above 50 Hz which form the harmonics at the load side. A low impedance, high pass filter (HPF) has been connected in parallel (point 4) to draw all the harmonic currents in 150 Hz and above.

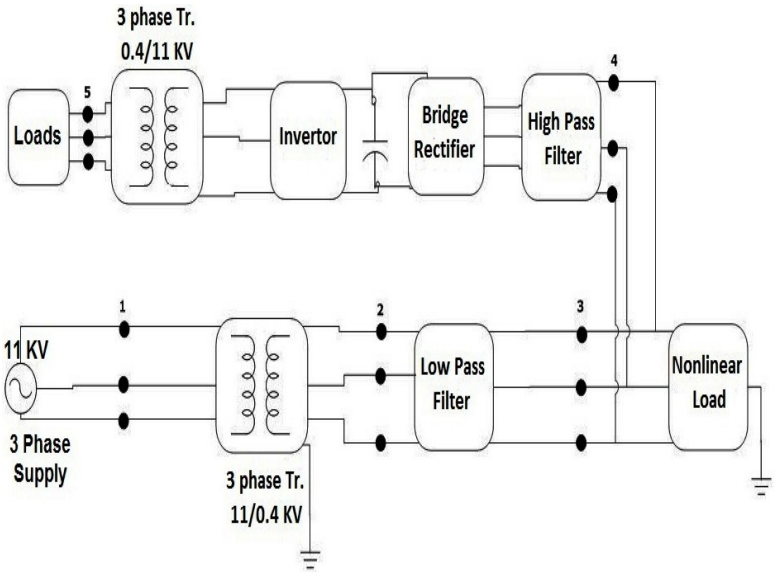


Figure 2.3: Schematic Diagram of 3 phase circuit

At the same time, HPF has been connected in series with a three-phase full wave bridge rectifier in order to convert distorted AC currents in different frequencies into (zero frequency) DC current. The produced DC power can feed small DC loads (e.g. LEDs) however, the output waveform of the DC current has the maximum ripple value which can affect the electronic equipment because of the high ripple.

The next step, requires a conversion of DC current to AC current on the fundamental frequency of 50 Hz by connecting a three-phase 6-pulses inverter which is controlled by a PWM circuit in series with the circuit. Finally, in order to benefit

from this new current, a 3-phase step up (0.4/11) kV transformer in $(\Delta - \Delta)$ connection can be linked in series (optional) to raise the voltage and feed AC loads.

2.2.1.1.1 Cases to Study :

The system has been tested twice both without and with a HPF circuit. The results and figures were collected and classified to make a comparison between two cases in the following cases:

1. First Case: A 3-phase source was connected in series with (LPF) and non-linear load as described in the previous section. Figure 2.4 shows the circuit without adding HPF.

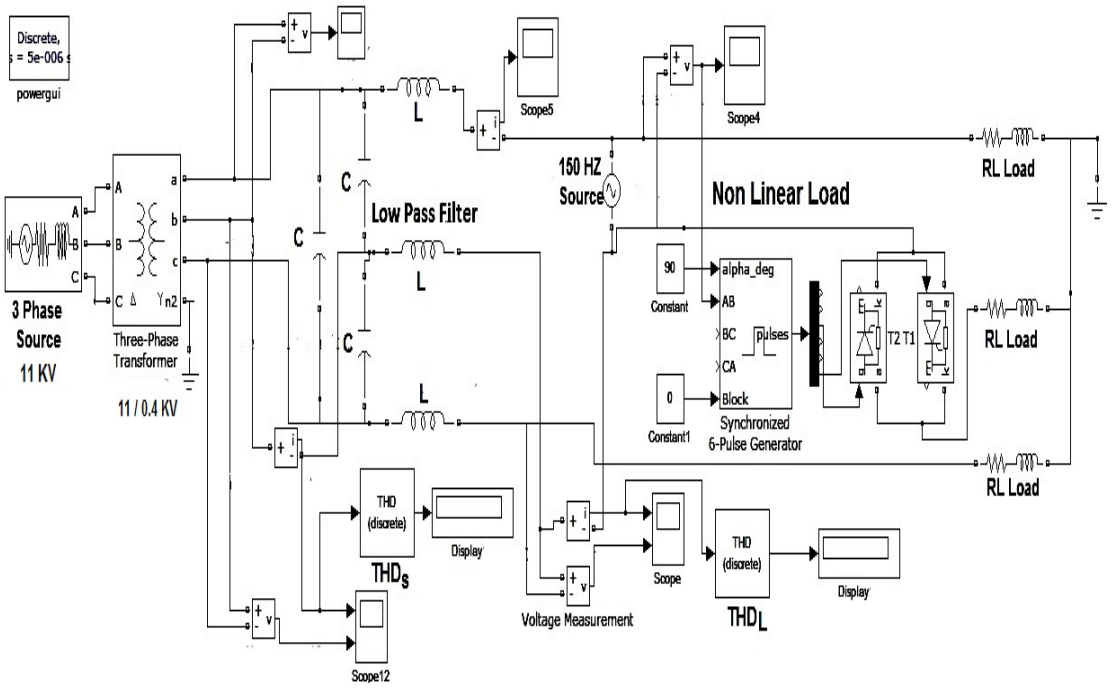


Figure 2.4: Normal Circuit Without HPF

Below, figure 2.5 shows the load voltage illustrating the defects on the waveform because of the harmonics at the load side.

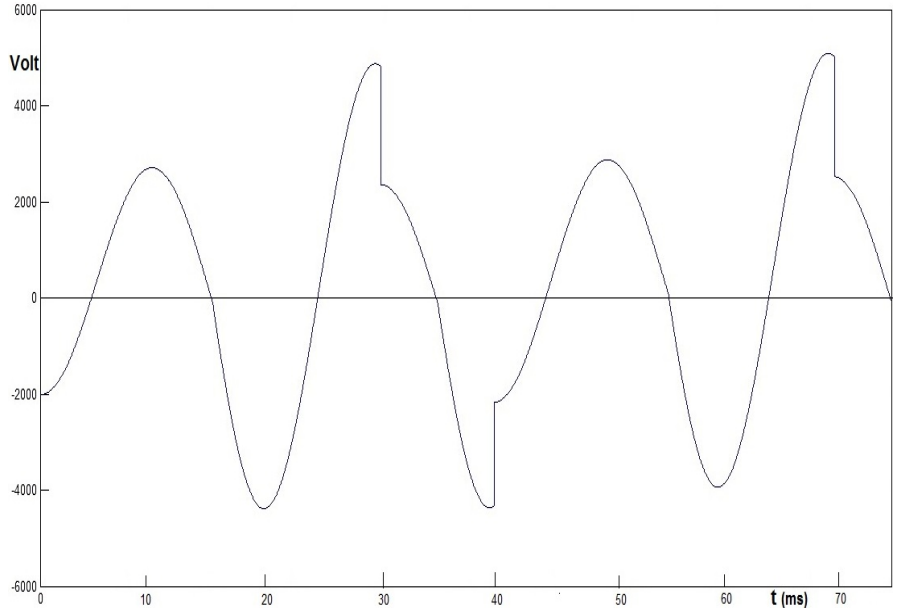


Figure 2.5: Load Voltage Without HPF

2. Second Case: The same circuit in the first case was connected in parallel with additional high pass filter (HPF) working at 150 Hz. This circuit has been tested and simulated by the Matlab-Simulink program.

   The figure 2.6, shows the harmonic current (I_h) after the (HPF) when the 150 Hz voltage source which represents the non-linear load or the source of harmonics (V_h) = 5000 volt.

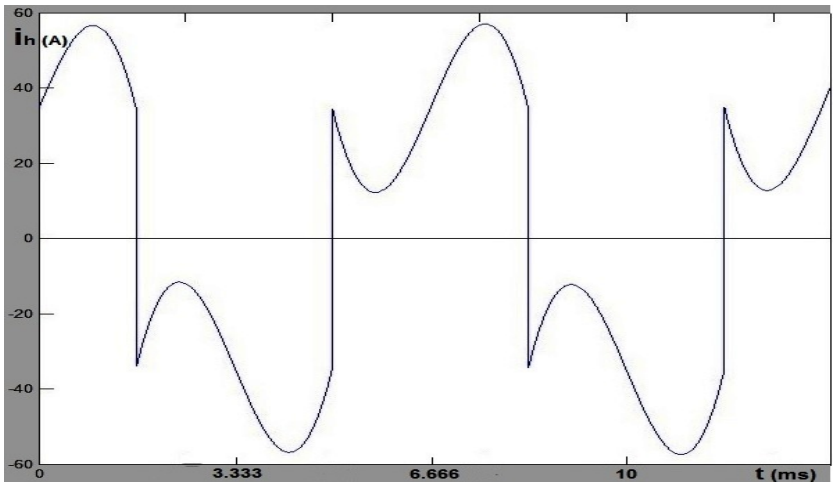


Figure 2.6: Harmonic Current When V_h = 5000 V

The full circuit diagram with HPF is shown below in figure 2.7.

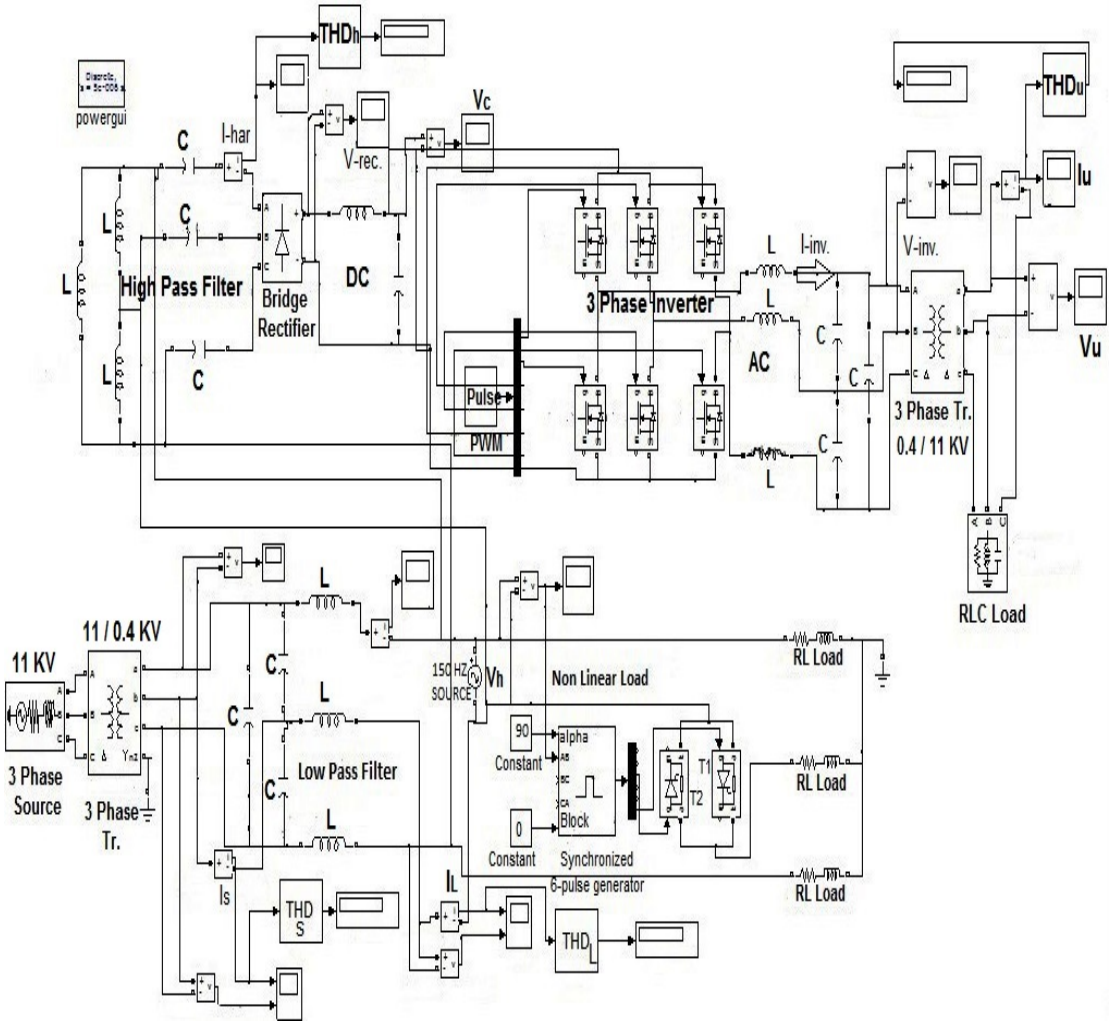


Figure 2.7: Full Circuit with HPF

Figure 2.8 shows the output voltage of the inverter ($Vinv.$) when harmonic voltage is 5 kV, the waveform has 50 Hz frequency and a quite sinusoidal.

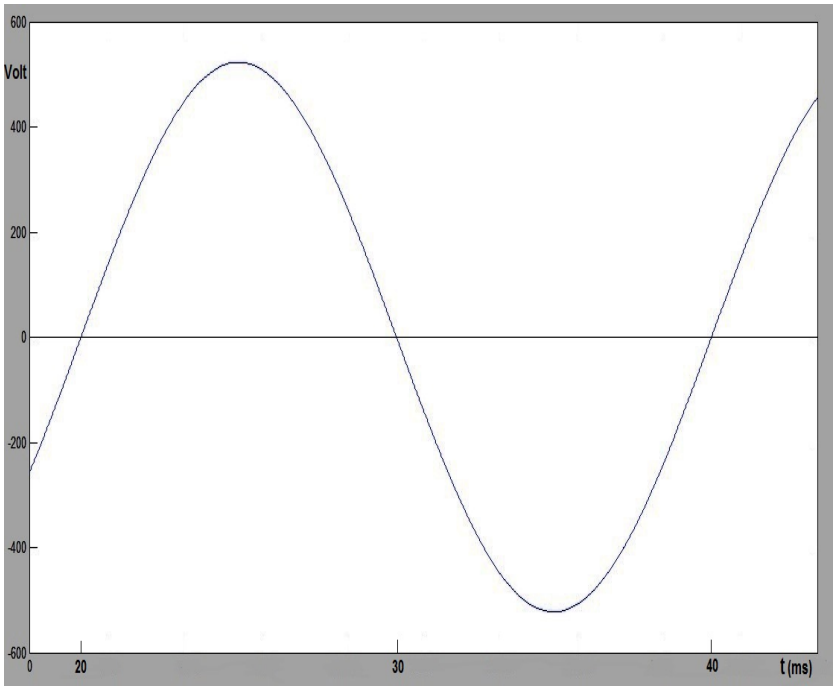


Figure 2.8: Inverter output voltage when $V_h = 5$ kV

2.2.1.1.2 DC Voltage Calculation :

In the case of using a three-phase full wave bridge rectifier, six pulses will be applied on each cycle, this means that there is a pulse every 60° in one full cycle. In order to calculate the DC voltage, which is the output of the bridge rectifier (V_{rect}), the average voltage can be calculated by using the following equation:

$$V_{rect.} = V_{avg.} = \frac{6}{2\pi} \int_{\pi/3}^{2\pi/3} V_{max} . \sin(wt).dwt = 0.955\, V_{max} = \text{DC Voltage} \quad (2.1)$$

2.2.1.1.3 The Design Specification :

The simulation has been performed on a three-phase non-linear load with the parameters shown in Tables 2.1, 2.2, 2.3, 2.4 & 2.5:

$\because V_{peak} = \sqrt{2}$ x $V_{rms} \Rightarrow \therefore 220V_{rms}$ x $\sqrt{2} = 311V_{peak}$ (primary side)

$11kV_{rms}$ x $\sqrt{2} = 15.6kV_{peak}$ (secondary side)

$\because V_{line} = \sqrt{3} \times V_{phase} \Rightarrow \therefore V_{line} = 311V_{phase} \times \sqrt{3} = 539V_{peak}$

Table 2.1: System Parameters

3-phase input voltage source	15.6 kV_{peak}
3-phase input voltage transformer	15.6 kV_{peak} /$(311V_{peak} \times \sqrt{3})$
3-phase output voltage transformer	$(311V_{peak} \times \sqrt{3})$/ 15.6 kV_{peak}
System frequency	50 Hz
Utilized load power	100 kW, 1 kVar
Utilized load voltage	15.6 kV_{peak}

The utilized load power at the output side is a fixed-power load represented by a three-phase RLC parallel load.

Table 2.2: RL-load Parameters, Before HPF

RL-Load power	10 kW
RL-Load voltage	381 V_{rms}
R-Load	12 Ω
L-Load	1.5 mH

Table 2.3: Low Pass Filter Parameters

Inductor	100 mH
Capacitor	0.1 mF
Filter impedance	31.6 Ω
Tuning frequency	50 Hz

Table 2.4: High Pass Filter Parameters

Inductor	225 µH
Capacitor	5 mF
Filter impedance	0.2 Ω
Tuning frequency	150 Hz

Table 2.5: Outer Transformer Filter Parameters

Inductor	10 mH
Capacitor	1 mF
Filter impedance	3.1 Ω
Tuning frequency	50 Hz

2.2.1.1.4 Results Assessment of 3-Phase Passive Method :

Tables 2.6 & 2.7, present all the results of the simulation with a comparison among the changes of the non-linear load which represented by a harmonic voltage supply (V_h) which produces 150 Hz voltage waveform from 5 to 5000 volt.

The first column of table 2.6, shows different values of V_h from 5 up to 5000 volt. The second column shows the extracted harmonic current (I_h) by the HPF, while the third column shows the extracted apparent power by the HPF (or the harmonic power S_h). The fourth, fifth and sixth columns present the source current (I_{s1}), the apparent source power (S_{s1}) and the source total harmonic current distortion ($THD_{Is1}\%$) respectively from the first case (without adding HPF). The seventh, eighth and ninth columns present the source current (I_{s2}), the apparent source power (S_{s2}) and the source total harmonic current distortion ($THD_{Is2}\%$) respectively at the second case (with adding HPF).

The apparent power at source side can be calculated by multiplying the RMS value of the source ($\sqrt{3} \times 220 = 381 V_{rms}$) with the RMS value of the measured source current (I_S) in different cases.

Second case			First case			Second case		
V_h (V)	Ih2 (A)	S(VA) (HPF)	Is1 (A)	S1(VA) Source	THD_I S1(%)	Is2 (A)	S2(VA) Source	THD_I S2(%)
5	0.06	0.3	22.3	8496	0.18	101	38481	0.16
10	0.1	1	22.3	8496	0.36	101	38481	0.33
20	0.4	8	22.3	8496	0.7	101	38481	0.5
50	0.66	28.5	22.3	8496	1.65	101	38481	1.2
100	1.5	150	22.4	8535	3.3	101	38481	2.4
200	2.2	440	23.5	8954	6.6	103	39243	5.7
300	3.3	990	24	9144	10	105	40005	9
400	4.5	1800	24.5	9335	13.3	107	40767	12.2
500	5.7	2850	25	9525	16.7	109	41529	15.6
1000	11.5	11500	28	10668	33.7	121	46101	33
2000	22.8	45600	39	14859	74.6	150	57150	69
3000	34	102000	47.5	18098	116.5	177	67437	106
4000	45	180000	56	21336	162	200	76200	145
5000	58	290000	65	24765	211.4	235	89535	186

Table 2.6: Simulation results with various values of (V_h)

The actual readings which have been taken locally by the authors in [108] show the large values of THD_I and big differences in values of current THD between different buses and phases. The real data of a system study, shows that THD_I values reached more than 200% in many cases of that study [108]. For this reason, it is reasonable to expand the range of current simulation study results to 211% as stated on the last row when $V_h = 5$ kV. The value of harmonic voltage power supply of 150 Hz increased up to 5000 volt as a maximum value as a non-linear load which produces 356% of THD_I at the load side in the second case as shown in table 2.7.

V_h (V)	THD_I L1(%)	THD_I L2(%)	I(inv.) (A)	V(inv.) (V)	S(inv.) $=S_u$(VA)	I_u (A)	V_u (V)	$V_{rect.}$ (V)
5	0.74	0.36	0.257	0.6	0.154	0.005	19.2	4.77
10	1.4	0.7	0.515	1.2	0.618	0.01	38	9.55
20	2.8	1.96	1.03	2.5	2.57	0.02	79	19.1
50	3.86	2.9	2.57	5.2	13.38	0.05	193.4	47.7
100	6.6	5.6	5.15	10.5	54	0.1	360	95.5
200	15.45	11.5	10.3	21	216	0.2	767	191
300	25.67	19.4	15.43	31	478.5	0.3	1148	286
400	34	23	20.58	42.6	876.7	0.4	1555	382
500	42	32	25.7	52.8	1358	0.5	1936	477
1000	71.75	56.4	51.5	105	5402	1	3851	955
2000	183.6	120.2	103	205	21093	2	7655	1910
3000	251	173	154.3	309	47691	3	11709	2865
4000	307	221	205.8	411	84579	4	15559	3820
5000	356	267	257	522	134277	5	19310	4775

Table 2.7: Simulation results with various values of (V_h)

The first column of table 2.7 shows a non-linear load represented by voltage power supply (V_h) working at 150 Hz increasing from 5 volt up to 5000 volt. The second column shows, the total current harmonic distortion at the load side ($THD_{IL1}\%$) for the first case (without HPF). The third column shows the total current harmonic distortion at the load side ($THD_{IL2}\%$) for the second case with HPF. The fourth, fifth and sixth columns present the inverter AC current ($I_{inv.}$), the inverter AC voltage ($V_{inv.}$) and the output apparent power of the inverter ($S_{inv.}$) which is the same value of the utilized output apparent power (S_u), respectively. The seventh, eighth and ninth columns present, the transformer AC current or the utilized current (I_u), transformer AC voltage or the utilized voltage (V_u) and the average value of the bridge rectifier's voltage (V_{dc}), respectively. In order to explain the circuit, it is necessary to understand tables 2.6 and 2.7 and explain the data using diagrams.

It is recognized that when the non-linear load represented by a voltage source (V_h) is equal to 5 Volt, THD_{IL1} is equal to 0.74%, and THD_{IL} in the second case =

0.36%. It can be concluded that, the adding of a HPF circuit to the system has decreased THD_{IL}. The difference in THD_{IL} after connecting the HPF circuit, $\Delta THD_I = 0.4\%$.

ΔTHD_{IL} is the difference between THD_I at the load side with and without adding the high pass filter (HPF), ($\Delta THD_{IL} = THD_{IL2}$ - THD_{IL1}). The same approach can be used to calculate the values of ΔTHD_{IS} for each value.

When the non-linear load increases to $V_h = 20$ volt, then ΔTHD_{IL} increases to 0.84%, and when $V_h = 50$ volt then ΔTHD_{IL} increases to 0.97%. This rate of increase of ΔTHD_I continuously expanding linearly until it reaches the last value of $V_h = 5000$ volt which produces 356% THD_{IL}. However, after using the HPF circuit ΔTHD_{IL} decreases 90% which is considerably a huge reduction of THD_I value at the load side.

Simultaneously, the harmonic current (I_h) which was drawn by using a low impedance ($Z_f = 0.2\Omega$) of (HPF) tuned to 150 Hz, increases proportionally with the increase of the harmonic voltage source (which represents the non-linear load). The increasing begins from 0.06 Ampere (when $V_h = 5$ volt), ending with 58 Ampere (when $V_h = 5000$ volt), and with a rectifier voltage ($Vrect.$) = 4.77 V_{dc} (when $V_h =$ 5 volt) and increases to reaches 4775 V_{dc} (when $V_h = 5000$ volt). Also, the output inverter voltage ($V_{inv.}$) = 0.52 volt (when $V_h = 5$ volt) and increases to reach 522 volt (when $V_h = 5000$ volt). Whereas the value of THD_I of the output load after the output transformer which is the utilized load (at point 5 in figure 2.3) remains constant small value at all the cases on the value of 0.02%.

Figure 2.9 below shows the sinusoidal utilized harmonic current after the VSI which is the output load current.

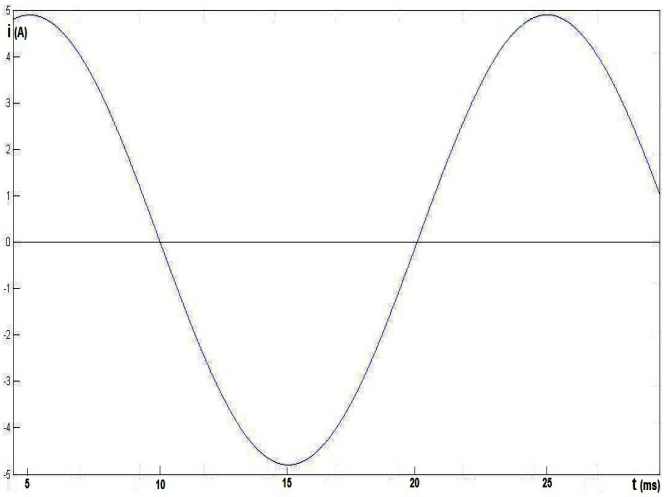


Figure 2.9: The output load current when V_h = 5000 V

Figure 2.10 presents the curve of $THD_{IL}\%$ in the two cases illustrated with the increasing of harmonic voltage (V_h). It is obvious that the gap between the two curves is expanding with the increasing of harmonic voltage (V_h). Consequently, the effect of adding HPF circuit to the system increases proportionally with the increase of harmonics (V_h) and decreasing THD_{IL2} value. This proves the contribution of this method in reducing the THD_I at the load side effectively in all values.

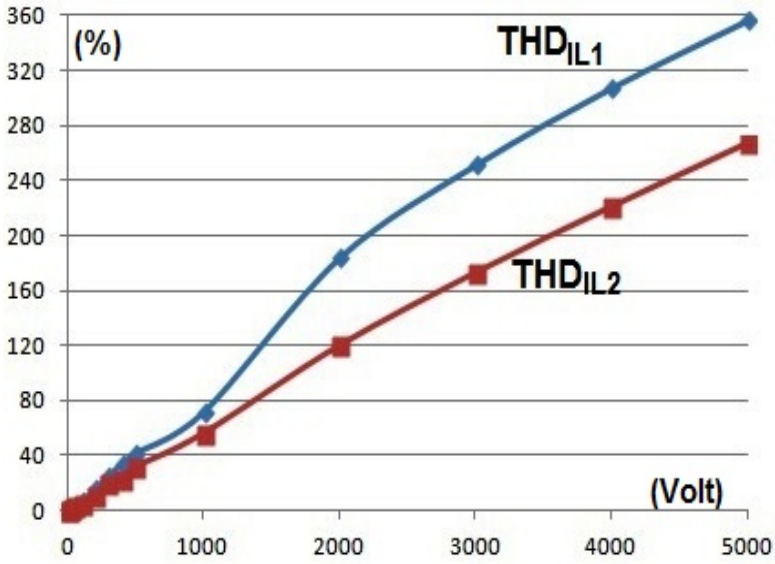


Figure 2.10: THD_{IL1} Curve Vs. THD_{IL2} Curve

Figure 2.11 below presents the curve of $THD_{IS}\%$ in two cases in accordance with the increase of harmonic voltage (V_h). The values of THD_{IS1} are always greater than THD_{IS2}. This evidence proves the contribution of this method to reduce THD_I at the source side effectively in all values, and consequently, improving input PF and power quality at the source side. The values of THD_{IL2} & THD_{IS2} are less than values of THD_{IL1} & THD_{IS1} because of the existence of the HPF.

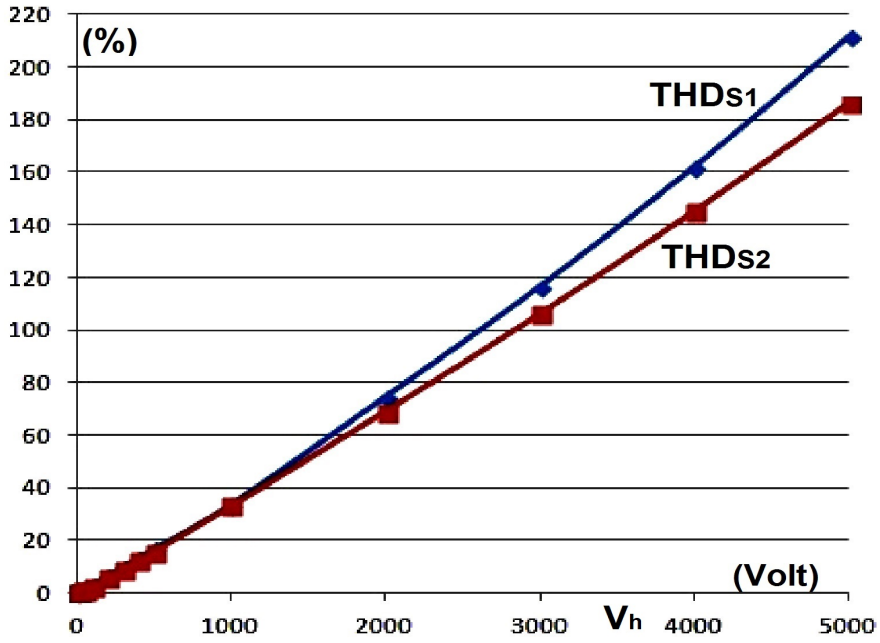


Figure 2.11: THD_{IS1} Vs. THD_{IS2} Curves

However, the source current (I_{S2}) in the second case is always greater than (I_{S1}) in the first case as shown in figure 2.12, while I_{S1} is always greater than the extracted harmonic current (I_h) at all values.

From the aforementioned details, it can be easily concluded that the values of THD_{IL}, THD_{IS} are increasing proportional to the harmonic voltage (V_h). This increase happens in both cases both without and with adding HPF circuits, but the results in the first case are higher than the second case for the same harmonic voltage in all cases.

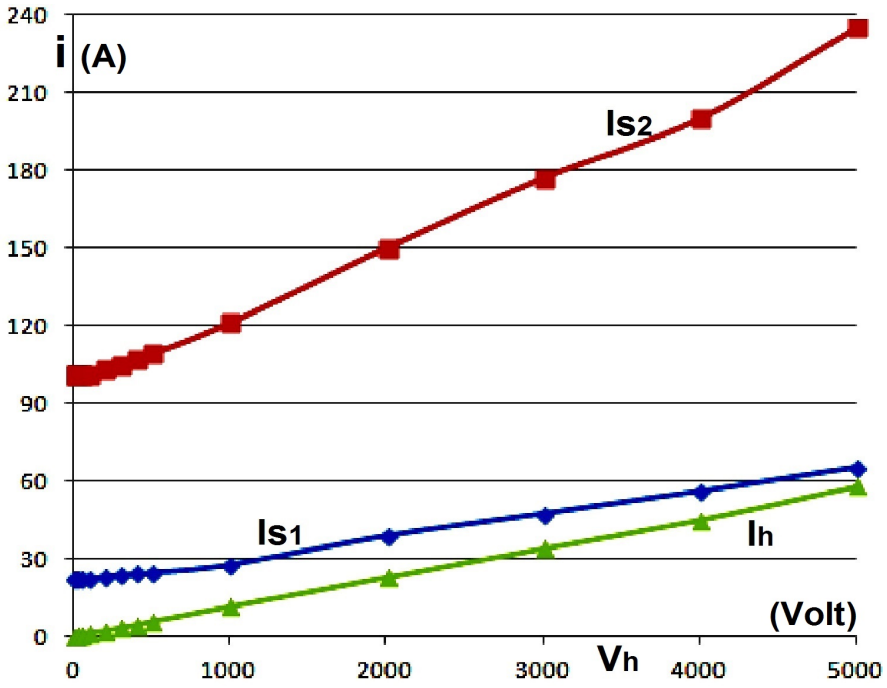


Figure 2.12: I_{S1}, I_{S2} & I_h Curves

Figure 2.13 below shows the different values of the apparent power of the harmonics ($S_h = I_h.V_h$) which has been extracted by the HPF and the values of the output apparent power of the 3-phase utilization inverter ($S_{inv.}$).

Figure 2.13 shows that S_h is always greater than $S_{inv.}$. This is logical because the utilized power (S_u) which is the same value of $S_{inv.}$, has been produced completely from the harmonics power (S_h) which has been drawn from the non-linear load via HPF.

In addition figure 2.13, shows the total apparent power at the second case S_2 is always greater than the total power without filter S_1 which is compatible with the increasing values of I_{s2} over I_{s1}.

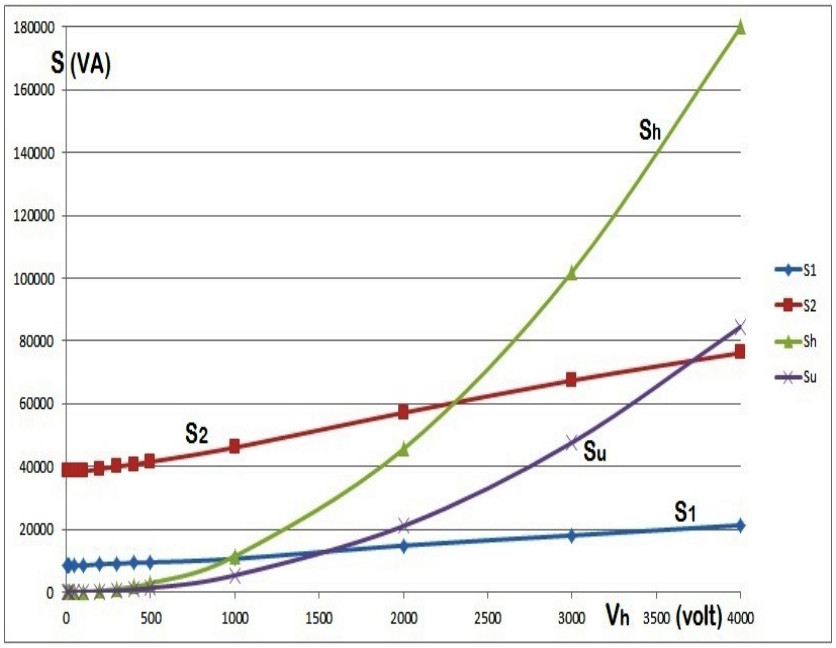


Figure 2.13: S_1, S_2, S_h & S_u Curves

Finally, according to the simulation results, tables & figures, the idea of taking advantage of harmonic power and harvesting these harmonics through converting it to useful sinusoidal power, in order to feed RLC-load, has been proved to be successful. However, additional current has been drawn from the source in all values of (V_h), which is regarded as a limitation for this design.

In addition, other goals of this work which were in decreasing the harmonics at the source and load side and improving the input PF and power quality have been achieved. The results prove that the value of THD_I decreased at both the source and the load sides in all cases and the produced power at the output side (point 5 in figure 2.3) has a sinusoidal wave and low THD_I of 0.02%.

2.2.1.1.5 Conclusion of 3-Phase Passive Filter Method :

This method presents a novel idea to take benefit of the harmonic currents and voltages which are produced as a result of non-linear loads. This method reduces THD_I values by filtering out the harmonics power and reuses it as a DC power

supply to feed RLC-loads in three-phase systems.

From the results of the simulation, it can be concluded that harmonic currents can be drawn by using a 150 Hz high pass filter from the load side, and that reduces the THD_I value at both load and source sides.

The simulation results showed that the THD_{IL} value has been reduced almost 90%, and the THD_{Is} has been reduced more than 25% when V_h is 5000 volt. These harmonic currents have been converted to a useful power with a very small THD_I of about 0.02%, by converting them to DC voltage and then reconvert it to AC voltage at the fundamental frequency of 50 Hz.

2.2.1.1.6 Advantages of 3-Phase Passive Filter method :

1. The idea of gaining benefit of harmonics power (S_h) and feed electrical (RLC) loads has been applied successfully on a three-phase system. However, it draws additional (I_S) current.
2. The low impedance (HPF) reduces the THD_I at both load and source sides for all values of (V_h) and extract the harmonics current.
3. Consequently, the input PF and the power quality of the circuit improved in general and RLC-load has been fed.

2.2.1.1.7 Limitations of 3-Phase Passive Filter Method :

1. Use of additional equipment like (high pass filter, full wave bridge rectifier, PE switches and voltage source inverter), make it bulky and not feasible.
2. The large number of parameters used in the design, increases the cost and the weight of the proposed circuit.
3. The additional elements used in this circuit increases the complexity of the design.

4. The additional passive filter and utilization circuit require additional source current, increases the input source power and increase the losses which make it impractical.

2.2.1.2 Single Phase Passive Filter Method

In order to simplify the previously proposed 3-phase circuit and reduce the cost and complexity of the design, a new method of a single-phase passive filter has been proposed in order to eliminate harmonics current on the power systems. This method can be used to bring a benefit of the harmonics current which has been produced on the source side because of the existing of non-linear loads in single-phase systems and convert it to useful sinusoidal power which can be used to feed different electrical loads.

In addition, this circuit contributes to a huge reduction of the total current harmonic distortion THD_I and improves PF. This design can utilize the distortion power by drawing harmonics current via using a low pass filter (LPF) and a full wave bridge rectifier to convert the drawn harmonics current to DC current. This reconverted to AC sinusoidal current by using single-phase inverter controlled by pulse width modulation (PWM) circuit in order to feed different loads.

It can be concluded from the results of the simulation, that the utilized current (I_u) can be created by rectifying harmonics current or can called filter current (I_f) which has been drawn by an LPF. This is a simple design and a low-cost circuit and with the most important advantage that this circuit can feed RL-load without requiring any additional source current.

Unfortunately, no mathematical formula can control the amount of utilized power (P_u) because the degree of the generated harmonics in every circuit changes according to many factors. A number of studies have been conducted to investigate the factors that can affect the harmonics produced by non-linear loads [109]. In [110] attenuation, which refers to the interaction of voltage and current distor-

tions due to shared system impedance, and diversity, which refers to the partial cancellation of harmonic currents due to phase angle diversity, are discussed. The effects of mixing single and three-phase non-linear loads on harmonic cancellation are also discussed in [111]. Harmonic cancellation due to different single-phase non-linear loads is illustrated in [112]. In [113], voltage, impedance and frequency variations effects on the harmonics generated from a single PC are discussed. Attempts to quantify the effect of linear loads on the generated harmonics are given in [114]. The authors in [109] concluded that many factors affect the degree of generated harmonics including the background voltage distortion and percentage of non-linear load to the total load.

2.2.1.2.1 System Description :

A simplified schematic diagram of the circuit is shown in figure 2.14. The circuit consists of a single-phase 220 V AC source connected in series with low pass frequency side of the passive (LC) filter which is (100 mH) inductor and in parallel (but not grounded) with high-frequency side which is a small size (0.1 mF) capacitor. This capacitor will take out all harmonics current (over 50 Hz) and passes it into the newly proposed utilization circuit which consists of full wave bridge rectifier and 4-pulses single-phase inverter. The output power offers a sinusoidal current and voltage; therefore, it can be used to feed different electrical loads.

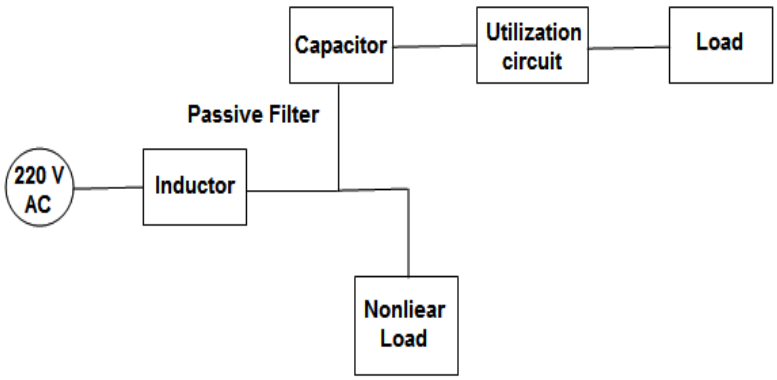


Figure 2.14: Schematic Diagram of Single-phase Circuit

2.2.1.2.2 Cases to Study :

The following three cases show the differences in the results between a single-phase circuit connected to non-linear load without filter and the same circuit with conventional LPF and the same circuit with different topology of LPF with a full bridge rectifier plus a VSI. The results and figures have been collected and classified to make a comparison among these cases in the following items:

1. First case: A power supply of 220 AC volt, connected to non-linear load (a single diode with RL-load) produces $THD_{Is} = 43.35$ %, without using passive filter as shown below in figure 2.15. The value of THD_{Is} can be changed with the size and the type of the non-linear load.

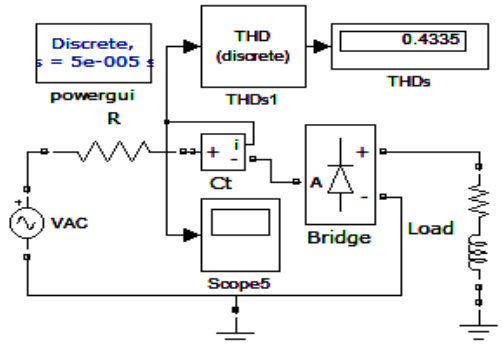


Figure 2.15: First case circuit

2. Second case: In addition to the circuit in figure 2.15, a traditional low pass filter (LPF) has been connected with a non-linear load. The inductor (L_1) has been connected in series with the power supply and the capacitor (C_1) has been connected in parallel with the load. A small value resistor has been added in series with (C_1) in order to measure the THD_I. The circuit in second case is shown in figure 2.16 below.

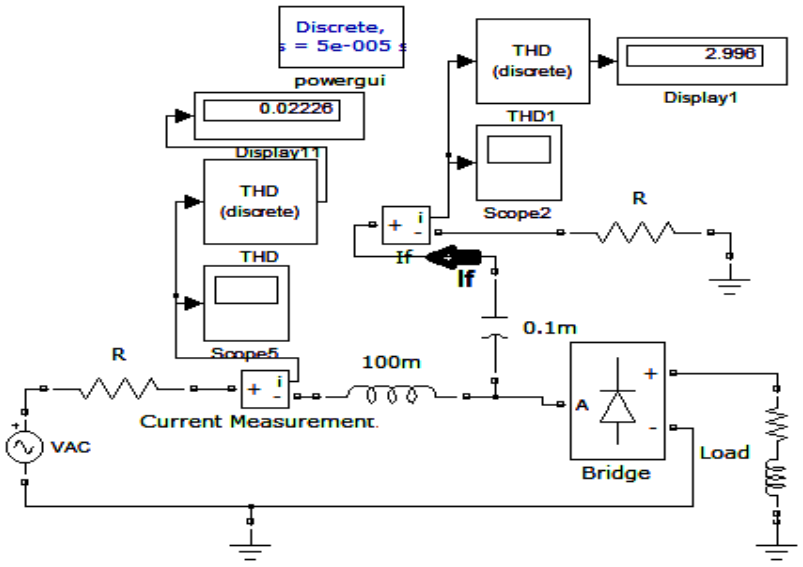


Figure 2.16: Second case circuit

The value of THD_I at the input side has decreased to 2.2%. The source current (I_s) is 7.2 A, and filter current (I_f) (in the capacitor branch) is 2.1 A (distorted current) and THD_I = 300% at the capacitor's branch. The figure 2.17, shows the filter current waveform or can be called the extracted harmonics current in the case of using LPF.

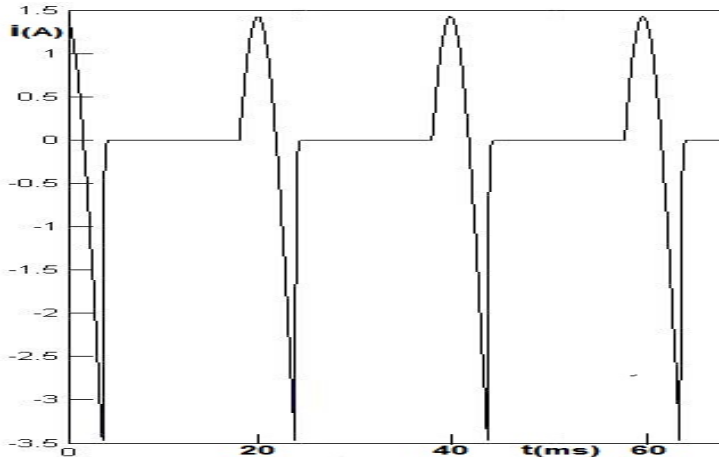


Figure 2.17: Filter current in the second case

3. Third case: The same circuit of the second case has been connected in addition to the utilization circuit and RL-load is shown in figure 2.18.

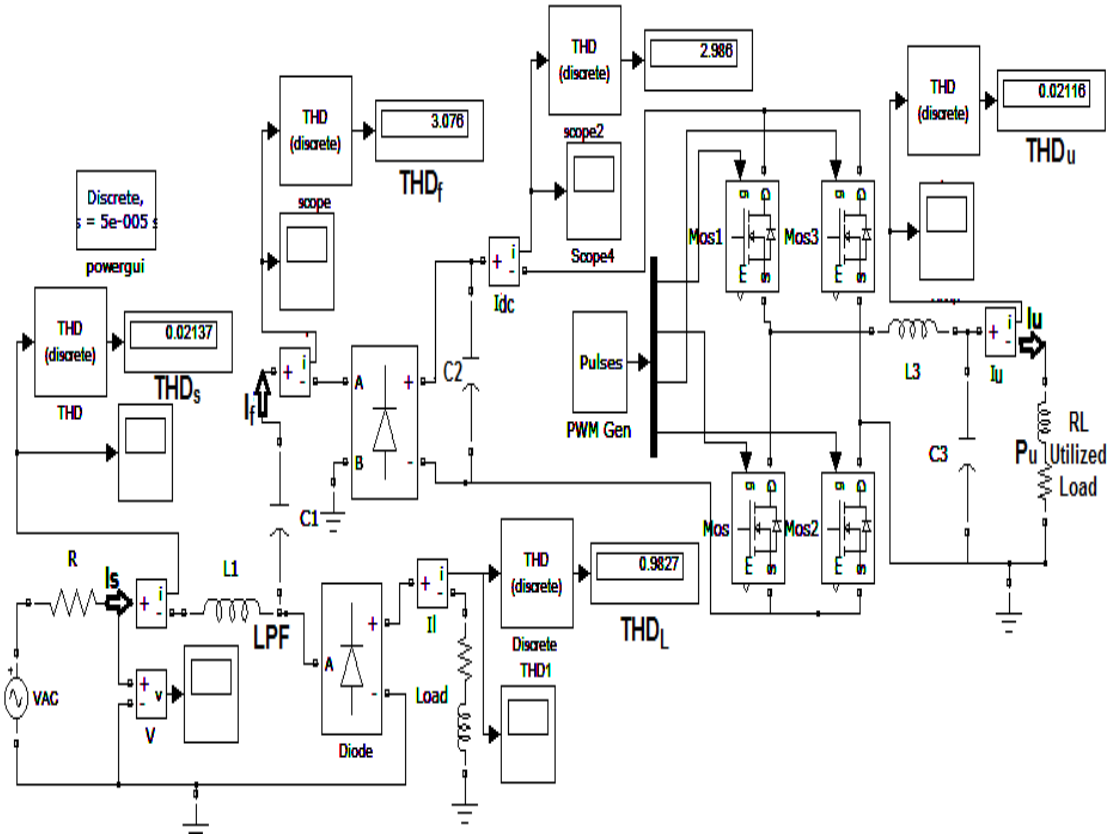


Figure 2.18: Third case circuit

The utilization circuit consists of a bridge rectifier with four pulses single-phase inverter controlled by PWM controller, the inverter is connected to RL-load as a utilized load. The capacitor (C_2) which located after the bridge rectifier, has been used as a dc voltage storage, and its value can be chosen as (1) mF or higher depending on the load current, load voltage and also depending on the required value of total harmonics after the utilization circuit (THD_u). The source current (I_s) has been shown in figure 2.19 has a value of (THD_s) = 2.2 %.

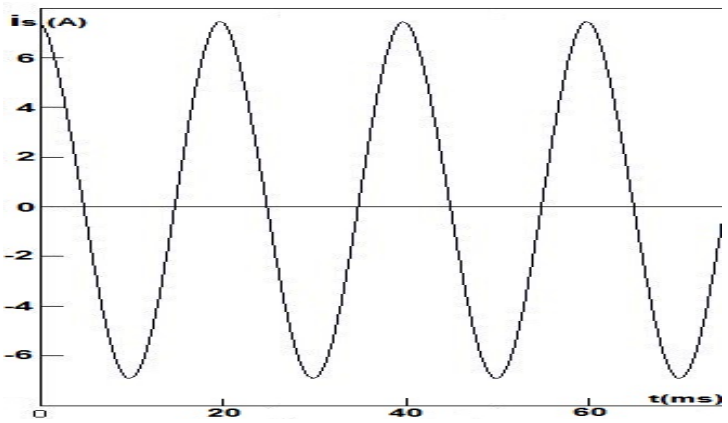


Figure 2.19: Source current (I_S) in the third case

The output utilized current waveform (I_u) = 1.4 Amp. is a sinusoidal wave as shown in figure 2.20, with a very small value of THD_I = 2.1 % and the source current (I_s) remains (7.2) A, without drawing any extra current.

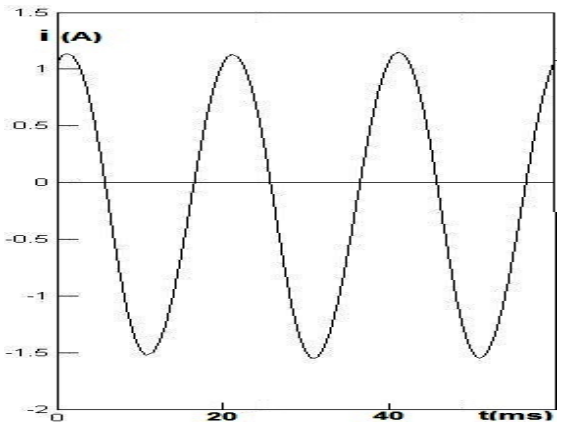


Figure 2.20: Utilization current (I_u) waveform

2.2.1.2.3 The Design Specification :

The simulation has been performed on a single-phase non-linear load with parameters shown below in table (2.8):

Table 2.8: System Parameters

Input voltage source	220 V_{rms}
Passive filter	L_1 = 100 mH, C_1 = 0.1 mF, f = 50 Hz
Non-linear Load	P = 100 W , Q = 10 var
After rectifier capacitor	C_2 = 2.2 mF
After inverter capacitor	C_3 = 2.2 mF
After inverter inductor	L_3 = 10 mH
Utilized Load (Z_u)	L = 1 mH, R = 1 Ω

2.2.1.2.4 Simulation Results and Assessment :

In order to simplify the whole circuit, the following figure 2.21 shows the summary of the third case when the utilization circuit has been added to the passive filter in order to utilize harmonics and improve the power factor at the source side.

(V_s) represents the voltage source, (V_h) is the non-linear load represents a source of harmonics, (L_1) is the inductor which works as a low impedance at low frequency (50 Hz), (C_1) is the capacitor which works as a low impedance at high frequency (150 Hz) and above, the utilization circuit (AC/DC) rectifier converts the harmonics into DC power and the (DC/AC) inverter converts to AC sinusoidal current, while (C_2) is the reservoir for DC voltage. Finally, the utilized load is a small RL-load.

This study presented three cases for studying and comparing the results of each case. The first case shows a single-phase voltage source in series with a single diode and inductive load as a non-linear load. For this case THD_{Is} = 43.35% without using any filter.

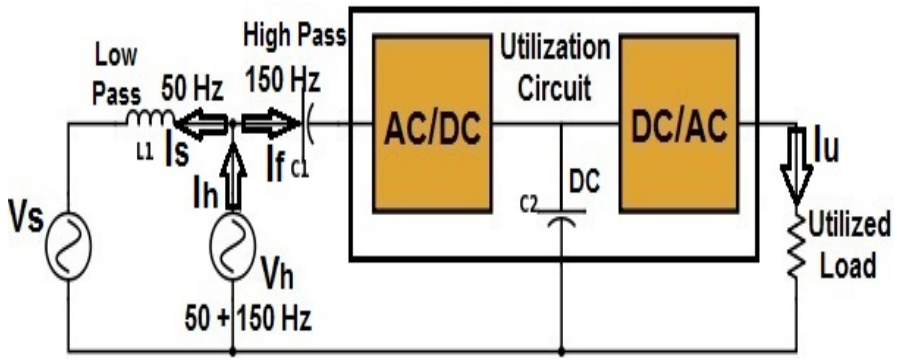


Figure 2.21: The schematic diagram of the third case

The second case is the same circuit adding a conventional LPF with (L) = 100 mH, (C_1) = 0.1 mF and tuning frequency = 50 Hz. THD_I of the source has decreased to 2.2% and the source current (I_S) in this case is 7.2 A, while the harmonic current or filter current (I_f) at the high-frequency (capacitor) branch is highly distorted as shown in figure 2.17.

The third case shows the full circuit adding a utilization circuit consisting of a full wave bridge rectifier and a single-phase inverter controlled by PWM circuit in series with the utilized load (RL-load). (I_S) and (I_f) remained at the same value. However the result of using the utilization circuit, a new current will appear on the output of the inverter, which is the utilized current (I_u) = 1.4 A, that feeds the RL-load. This (I_u) current has been created from the rectification of the harmonics current into a sinusoidal AC current in a very small value of THD_I = 2.1% at the RL-load side.

The table 2.9 below displays the values of (I_S), (I_u), the utilization ratio ($\frac{I_u}{I_S}$), utilized power, distortion at the source side (THD_s) & distortion at the high-frequency side of the filter (THD_f). These values change against specific values of (L_1) and (C_1) of the filter which have been chosen in a way that can investigate the (50 Hz) tuning frequency for LPF but in different filter impedances (Z_f).

Table 2.9: Simulation results in different values of Z_f

Case	L1 (mH)	C1 (mF)	Z_f (Ω)	Is (A)	Iu (A)	$\frac{I_u}{I_S}\%$	P_u (W)	THD% (Source)	THD% (Filter)
1st	0	0	0	1.1	0	0	0	43.35	0
2nd	100	0.1	31.6	7.2	0	0	0	2.2	300
3rd	100	0.1	31.6	7.2	1.4	19	2	2.1	305
3rd	50	0.2	15.8	21	4	19	16	3.2	246
3rd	18	0.56	5.67	38	13.7	36	188	5.6	180
3rd	10	1	3.16	61	22	36	484	8.8	164
3rd	1	10	0.31	120	43	36	1849	27	133
3rd	0.5	20	0.16	130	47	36	4489	31	126

(Z_f) is the impedance of filter at the fundamental frequency, ($\frac{I_u}{I_S}\%$) is the percentage of the utilization ratio of the source current, (P_u) is the utilized power at the RL-load, (THD_s) is the total harmonic current distortion of the source, (THD_f) is the total harmonic current distortion for high-frequency side of the passive filter.

The first row shows the value of ($THD_s = 43.35\%$) in the first case, because of the non-linear load without adding any filter with a peak value of source current (I_S) = 1.1 A. The second row shows that the peak value of (I_S) has increased to 7.2 AC ampere because adding the passive filter; therefore, the value of THD_s for source decreased to 2.2% with high $THD_f = 300\%$ on the capacitor's branch of LPF. These values reflect the effectiveness of the LPF to draw the harmonics current.

The 3rd, 4th, 5th, 6th, 7th & 8th rows show the values of (Z_f), (I_S), (I_u), $\frac{I_u}{I_S}\%$, (P_u), THD_s & THD_f, respectively in the third case when using a utilizing circuit in six different values of (L_1), (C_1) and Z_f which tunes the LPF's frequency at the 50 Hz fundamental frequency.

However, the third row shows that (I_S) remains at the same value (7.2 A) while the utilized current (I_u) produced (1.4 A) from the utilization circuit as a result of the rectification and utilization process of harmonics current.

Figure 2.22, presents the values of (L_1) & (C_1) against filter impedance (Z_f) in the third case. It shows that the filter impedance (Z_f) increases with the inductance value and decreases with the capacitance value of LPF.

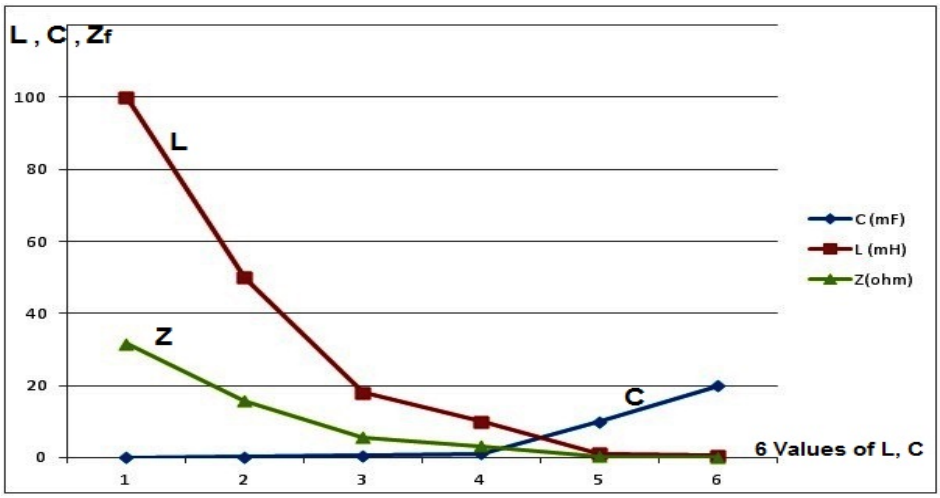


Figure 2.22: The values of L_1, C_1 & Z_f in 6 values in 3rd case

Figure 2.23, shows a comparison between THD_s & THD_f in six different values of the filter impedance (Z_f) at the third case.

It can be concluded from table (2.9), figure 2.22, figure 2.23, and figure 2.24 that, (THD_s) is increases proportionally with (C_1) but decreases proportionally with (THD_f), (L) and (Z_f). The source provides additional current when the value of main capacitor (C_1) increases; therefore, the value of THD_s increases while the value of THD_f decreases.

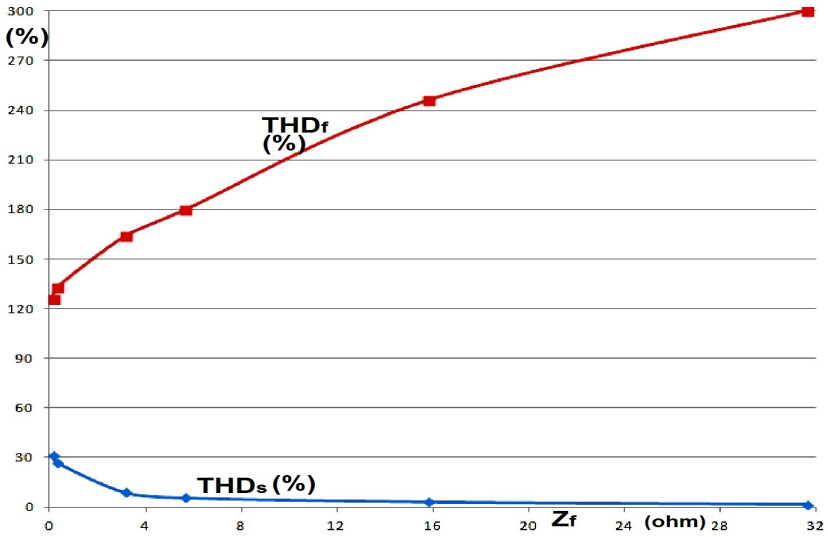


Figure 2.23: Comparison between THD_s & THD_f with Z_f values

On the other hand, figure 2.24 shows a comparison between (I_S) and (I_u) values in the 3rd case when the values of (L) and (C_1) change in six different values of Z_f. the results prove that (I_S) and (I_u) are increase proportionally with (C_1) value and inversely with (L) and (Z_f) values, because bigger value of (C_1) will cause in smaller impedance (Z_f) which requires bigger current. This phenomenon means that, the low impedance of LPF will cost the source additional current, however at the same time, additional (I_u) will be produced after utilization circuit.

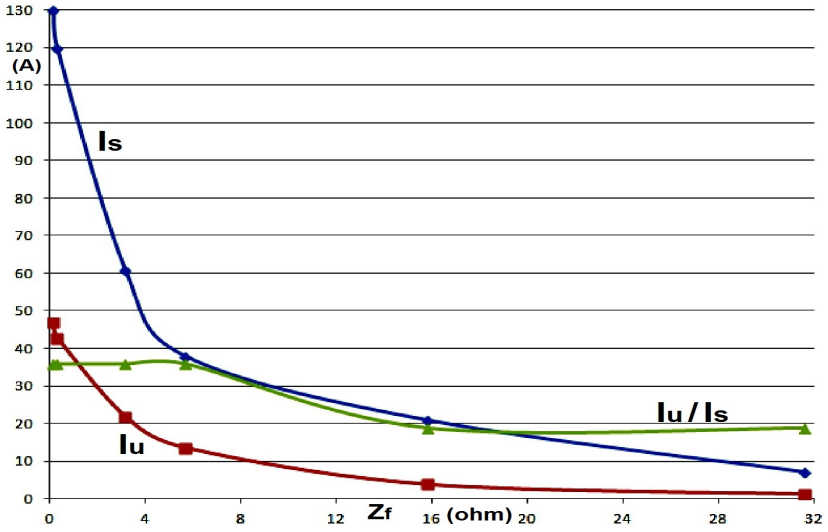


Figure 2.24: Comparison between (I_S), (I_u) & $(\frac{I_u}{I_S}\%)$ with Z_f values

The chosen value of impedance filter (Z_f) = 31.6 Ω in the third row, when (L) = 100 mH and (C_1) = 0.1 mF is the best value for this circuit, because a sinusoidal utilization current (I_u) = 1.4 Amp. and P_u = 2 watt, has been produced on the output (load side) from the rectification of harmonics current without requiring additional source current.

2.2.1.2.5 Conclusion of Single Phase Passive Method :

This chapter presented a single phase LPF with a full bridge rectifier and voltage source inverter (VSI) using a simple designed circuit in order to utilize harmonics current in single-phase systems by filtering out the harmonics current (I_f) via LPF and passing it through a utilization circuit which consists of full wave bridge rectifier and 4-pulses inverter controlled by PWM circuit in order to rectify the distorted current (I_f) and convert it into sinusoidal current called (I_u) and feed the RL-load.

Three cases have been assessed and compared using the Matlab-simulink program. It can be concluded from the results of the simulation, that a utilized current (I_u) can be created by rectifying harmonics current (I_f) with a simple cost and without requiring any additional source current (I_S) and a simple RL-load can be fed by utilized power (P_u). In addition, the value of THD_s has decreased. Consequently, the input PF and the output utilized load are both have a unity PF values.

2.2.1.2.6 The Advantages of Single Phase Passive Filter method :

1. It has the ability to reduce the harmonics distortion at both the source and load sides and thus can works as a power factor corrector, reduce the bad effects of harmonics on the utilities, increase the PF and consequently, improves the power quality.

2. Offers a new idea to take benefit of the harmonics current, especially with the increasing of non-linear loads and THD values at the load side.

3. The design is simple and without complex control circuit.

4. Uses a small value of capacitor (0.1 mF) which reduces the size and cost.

5. The circuit at a specific values of LPF parameters, feed (1.4) ampere and almost (2 Watt) output power without drawing additional source current. The utilized power can be changed according to the utilized load.

2.2.1.2.7 The Limitations of Single Phase Passive Filter Method :

1. The big value of the inductor (100 mH) when (Z_f) is (31.6Ω), and the utilization circuit are considered expensive in comparing with a small amount of the utilized power.

2. From the results, the source current (I_S) increases when the value of (C_1) increases, which increases the losses and limits the design parameters.

3. Many criteria can limit the design parameters, like (Z_f), the amount of a non-linear load and distorted harmonics and the quality of the passive filter.

2.2.2 Using of Active + Passive Filters

In order to improve the performance of the passive circuit, by applying the idea of taking advantage of harmonics power and feed electrical loads, a traditional active filter has been accompanied with a passive filter in a 3-phase system constructing a novel topology of HAPF.

2.2.2.1 3-Phase Hybrid Active Power Filter (HAPF) Method

The invention of a new additional configurations of a HAPF will provide better alternatives to existing applications and will explore a number of newer applications [61]. This method presents the design and simulation of a new topology of a 3-phase HAPF circuit using the shunt low pass filter (LPF) connected in parallel with active power filter (APF).

The main aim of this new topology of HAPF is to take benefit from the extracted distorted harmonics current via modifying I_h into a sinusoidal waveform in order to feed different electrical loads. In addition, the newly proposed HAPF has the same functions and advantages of other HAPF topologies (e.g. reactive power compensation, elimination of high order frequencies and harmonic current compensation, and improves the power factor).

There are many methods to design a control algorithm for active filtering. According to [115], the p-q theory forms a quite efficient basis for designing active filter controller; therefore, the control circuit has been designed based on the instantaneous reactive power theory [116]. This algorithm determines the compensation characteristics of the shunt active filter. The p-q theory requires the use of Clarke transformation equations [117], and hysteresis current control technique [118], [119], to be used in the design. The proposed circuit provides a good harmonic current compensation and power quality improvement. The non-linear load is represented by a three-phase full wave bridge rectifier and a MOSFET

switched by PWM circuit at 150 Hz switching frequency in series with a small resistive load.

The voltage source inverter (VSI) has been chosen in the design as it's very common in researches because of it's lower running loss in compared to current source inverter (CSI) [88].

2.2.2.1.1 Analysis of The New Proposed Circuit :

The new HAPF is a combination of shunt APF connected in shunt with the capacitor in high-frequency branch of the low passive filter (LPF). A single line diagram of the newly proposed circuit is shown in figure 2.25.

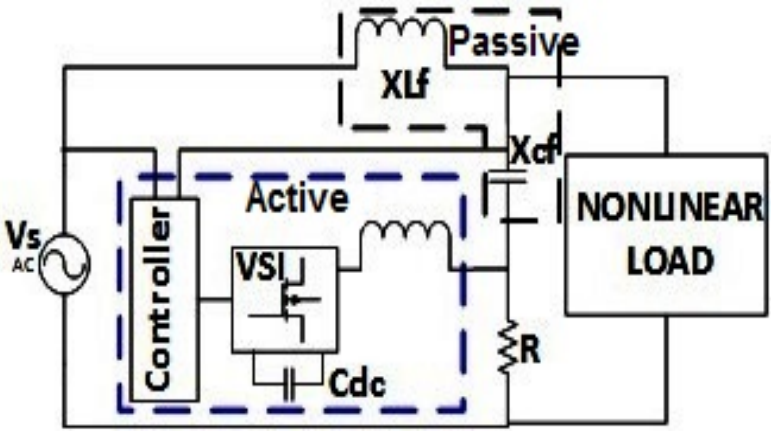


Figure 2.25: Single Line Diagram of The New HAPF

Commonly, a parallel APF has been considered as a current source, and the nonlinear load as a harmonic source. The compensation method is based on the concept of injecting harmonic current into the AC system with a same amplitude of capacitor current but at a 180 phase shift. The figure 2.26 below shows the single-phase equivalent circuit of newly proposed HAPF.

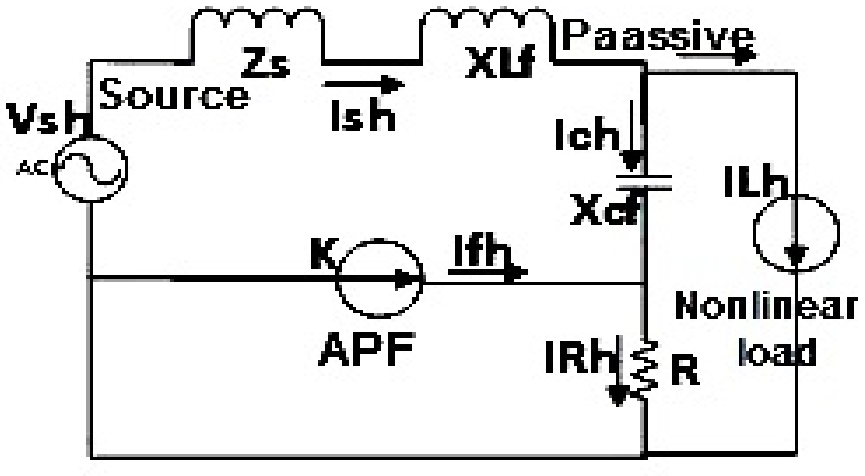


Figure 2.26: Equivalent Single Line Diagram of Harmonics Current of The Circuit

$$I_{sh} = I_{ch} + I_{Lh} \tag{2.2}$$

I_{sh} : The harmonics current of the source.

I_{ch} : The harmonics current of the capacitor branch.

I_{Lh} : The harmonics current of the non-linear load

$$I_{ch} = I_{Rh} - I_{fh} \tag{2.3}$$

I_{Rh} : The harmonics current of the resistive load.

I_{fh} : The harmonics current of the APF.

$$I_{fh} = KI_{ch} \tag{2.4}$$

K: The equivalent transfer function, this value is adjustable factor in control circuits.

$$V_c = I_c.X_c \tag{2.5}$$

From equations 2.3 and 2.4:

$$I_{Rh} = I_{ch} + KI_{ch} = I_{ch}(1 + K) \tag{2.6}$$

$$I_{ch} = \frac{I_{Rh}}{(1 + K)} \tag{2.7}$$

By applying Kirchhoff's voltage law (KVL):

$$V_{sh} = I_{sh}(Z_s + X_L) + I_{ch}X_c + I_{Rh}R \tag{2.8}$$

From equation 2.2:

$$V_{sh} = (I_{ch} + I_{Lh})(Z_s + X_L) + I_{ch}X_c + I_{Rh}R \tag{2.9}$$

From equation 2.3:

$$V_{sh} = (I_{Rh} - I_{fh} + I_{Lh})(Z_s + X_L) + (I_{Rh} - I_{fh})X_c + I_{Rh}R \tag{2.10}$$

From equation 2.4:

$$V_{sh} = (I_{Rh} - KI_{ch} + I_{Lh})(Z_s + X_L) + (I_{Rh} - KI_{ch})X_c + I_{Rh}R \tag{2.11}$$

From equation 2.7:

$$V_{sh} = (I_{Rh} - (\frac{K}{1 + K})I_{Rh} + I_{Lh})(Z_s + X_L) + (I_{Rh} - (\frac{K}{1 + K})I_{Rh})X_c + I_{Rh}R \tag{2.12}$$

$$V_{sh} = I_{Rh}[(1 - \frac{K}{1+K})(Z_s + X_L) + (1 - \frac{K}{1+K})X_c + R] + I_L(Z_s + X_L) \quad (2.13)$$

$$I_{Rh} = \frac{V_{sh} - I_{Lh}(Z_s + X_L)}{(1 - \frac{K}{1+K})[Z_s + X_L + X_c] + R} \quad (2.14)$$

According to [57], the source impedance ($Z_s = 0$) should present a negligible amount of impedance at the fundamental frequency ($Z_s = 0$), then Z_s does not cause any noticeable fundamental voltage drop. So that $Z_s = 0$ and then, in order to get a sinusoidal source waveform $V_{sh} = 0$, and when K = 1 :

$$I_{Rh} = \frac{-I_{Lh}X_L}{0.5(X_L + X_c) + R} \quad (2.15)$$

If $X_L << 1 \Rightarrow \therefore I_{Rh} = 0$ & $I_{sh} = 0$ (waveform is sinusoidal)

Therefore, this design requires small value of inductor and big value of capacitor.

2.2.2.1.2 Instantaneous Reactive Power Theory :

The instantaneous reactive power (p-q) theory has been formulated by Akagi [120], it is based on the Clarke transformation as stated in [121], in order to convert voltages and currents in three-phase systems (abc) coordinates into (α, β , 0) orthogonal coordinates.

In three-phase three-wire systems, splitting the zero-sequence component from the abc components is the most distinctive feature of applying (p-q) theory and that leads to simplification of the equations [115].

The Clarke transformation, has the form:

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{2.16}$$

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{2.17}$$

With the voltages and currents have transformed to the α and β coordinates, the real and imaginary powers are given by:

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ v_\beta & -v_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{2.18}$$

Where (p) is the real power and represents the total energy flow per time, (q) is the imaginary power and gives the measure of the quantity of current or power that flows in each phase without transporting energy at any time [115].

This control method senses capacitor currents (i_a, i_b, i_c) and line voltages (v_a, v_b, v_c) to create reference currents $(I_{ref.})$ and then compare resistor current as a feedback (I_f) with $(I_{ref.})$ in order to control pulses of VSI's switches.

$$p = v_\alpha i_\alpha + v_\beta i_\beta = p_{av} + p_{os} \tag{2.19}$$

p_{av} : Represents the fundamental energy transferred from source to load (mean value of instantaneous power $(p_{ins.})$).

p_{os} : Represents the exchanged or oscillated energy between source and load, this part must be compensated because it's produced in a result of distorted current as harmonics.

The instantaneous imaginary (reactive) power (q) is given as:

$$q = -v_\alpha i_\beta + v_\beta i_\alpha = q_{av} + q_{os} \tag{2.20}$$

q_{av} : The mean value of ($Q_{ins.}$) which represents the fundamental reactive power exchanged between source and load (this part must be compensated as it's not active power).

q_{os} : The oscillating part of $Q_{ins.}$ which represents the exchanged energy between phases and load (this part also must be compensated).

The instantaneous active current i_p is defined in the α and β coordinates as:

$$i_{\alpha p} = \frac{v_\alpha}{v_\alpha^2 + v_\beta^2} p \tag{2.21}$$

$$i_{\beta p} = \frac{v_\beta}{v_\alpha^2 + v_\beta^2} p \tag{2.22}$$

The instantaneous reactive current,i_q is defined in the α and β coordinates as:

$$i_{\alpha q} = -\frac{v_\beta}{v_\alpha^2 + v_\beta^2} q \tag{2.23}$$

$$i_{\beta q} = \frac{v_\alpha}{v_\alpha^2 + v_\beta^2} q \tag{2.24}$$

Let the instantaneous powers in the α axis and the β axis be p_α and p_β , respectively. They are given by the conventional definition as follows:

$$\begin{bmatrix} p_\alpha \\ p_\beta \end{bmatrix} = \begin{bmatrix} v_\alpha & i_\alpha \\ v_\beta & i_\beta \end{bmatrix} = \begin{bmatrix} v_\alpha & i_{\alpha p} \\ v_\beta & i_{\beta p} \end{bmatrix} + \begin{bmatrix} v_\alpha & i_{\alpha q} \\ v_\beta & i_{\beta q} \end{bmatrix} \tag{2.25}$$

The instantaneous real power in the three-phase circuit (p) is given as follows:

$$p = p_\alpha + p_\beta = \frac{v_\alpha^2}{v_\alpha^2 + v_\beta^2}p + \frac{v_\beta^2}{v_\alpha^2 + v_\beta^2}p + \frac{-v_\alpha v_\beta}{v_\alpha^2 + v_\beta^2}q + \frac{v_\alpha v_\beta}{v_\alpha^2 + v_\beta^2}q \tag{2.26}$$

$i_{L\alpha}$ represents the reference current in the α coordinate is defined as:

$$i_{L\alpha} = i_{\alpha p} + i_{\alpha q} \tag{2.27}$$

$i_{L\beta}$ represents the reference current in the β coordinate is defined as:

$$i_{L\beta} = i_{\beta p} + i_{\beta q} \tag{2.28}$$

i_{ref} represents the reference current in the abc coordinates is calculated as:

$$\begin{bmatrix} i_{refa} \\ i_{refb} \\ i_{refc} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ \frac{-1}{2} & \frac{\sqrt{3}}{2} \\ \frac{-1}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \end{bmatrix} \tag{2.29}$$

The aforementioned equations were explained previously in details in [115].

2.2.2.1.3 Hysteresis Current Control :

Hysteresis current control is a common PWM control used in voltage source inverters (VSI) to force these inverters to behave as controlled ac current source to the power system [115]. This technique depends on generating the required triggering pulses by comparing the feedback signal with the reference current, and it is used for controlling the voltage source inverter [119]. This method controls the switches of the voltage source inverter asynchronously to swing the current through the inductor up and down so that it follows the reference current.

In general, hysteresis regulation has the advantages that it is unconditionally

stable, does not require detailed plant data and can achieve high rates of change in the controlled variable. These advantages are attractive in APF application where the reference can have sharp transitions. The fast response of the following errors of hysteresis control signals is advantageous in APF applications.

Hysteresis current control (HCC) is the simplest control technique to apply in the time domain [122]. Memory block uses to implement a delay by major integration time step. Relay block or hysteresis block is important to operate the ON/OFF switching controller when there is a difference of (+0.01) and (-0.01) between two values of (I_{ref}&I_f). Figure 2.27 shows the hysteresis current control circuit (HCC) designed in the Matlab-Simulink program :

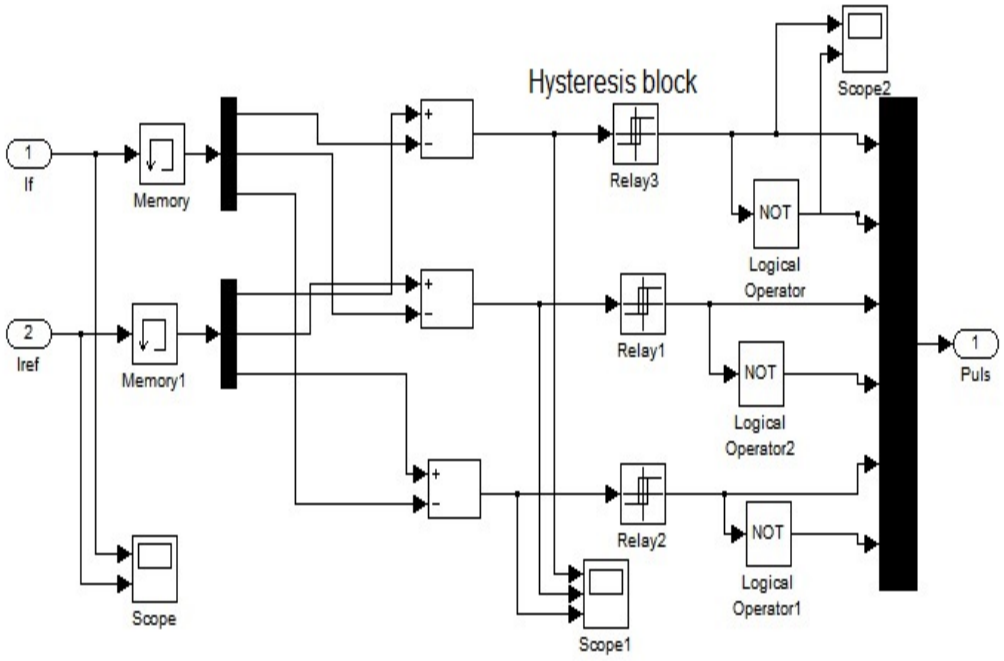


Figure 2.27: Hysteresis Current Controller Circuit

2.2.2.1.4 The System Configuration :

The system configuration has been described and investigated in three steps as:

1. The first step represents an initial circuit consists of a 3-phase voltage source (20 volt) connected in series with a 3-phase full wave bridge rectifier in series with a 150 Hz pulsating MOSFET switch (represented the non-linear load) as shown in figure 2.28.

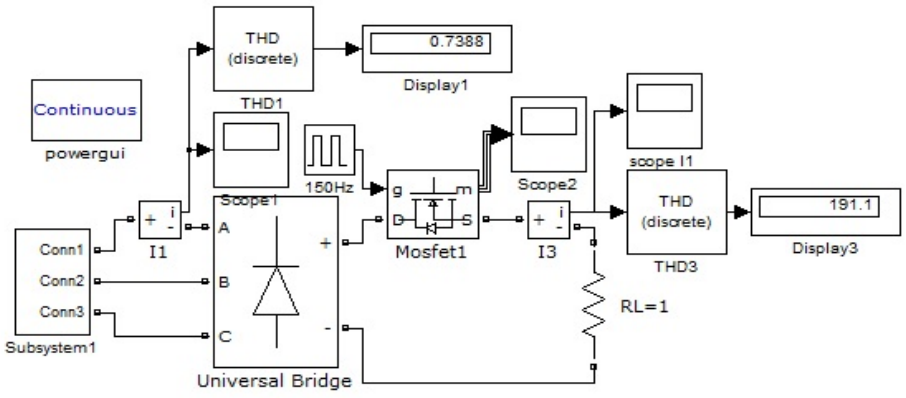


Figure 2.28: Traditional Circuit Without Filters

2. The second circuit consists of a 3-phase voltage source, connected in series with non-linear load and a passive low pass filter (LPF) its resonance frequency is 50 Hz, $L = 1.35mH, C = 7.5mF, Z_{filter} = 0.42\Omega$ (Low impedance) with a resistive load (1Ω) , the resistor can be used in order to adjust the tuning frequency sharpness [37].

   The role of the LPF is to eliminate the harmonics from the source, and force the harmonic current to pass through the low impedance branch of LPF which (RC). The circuit is shown below in figure 2.29.

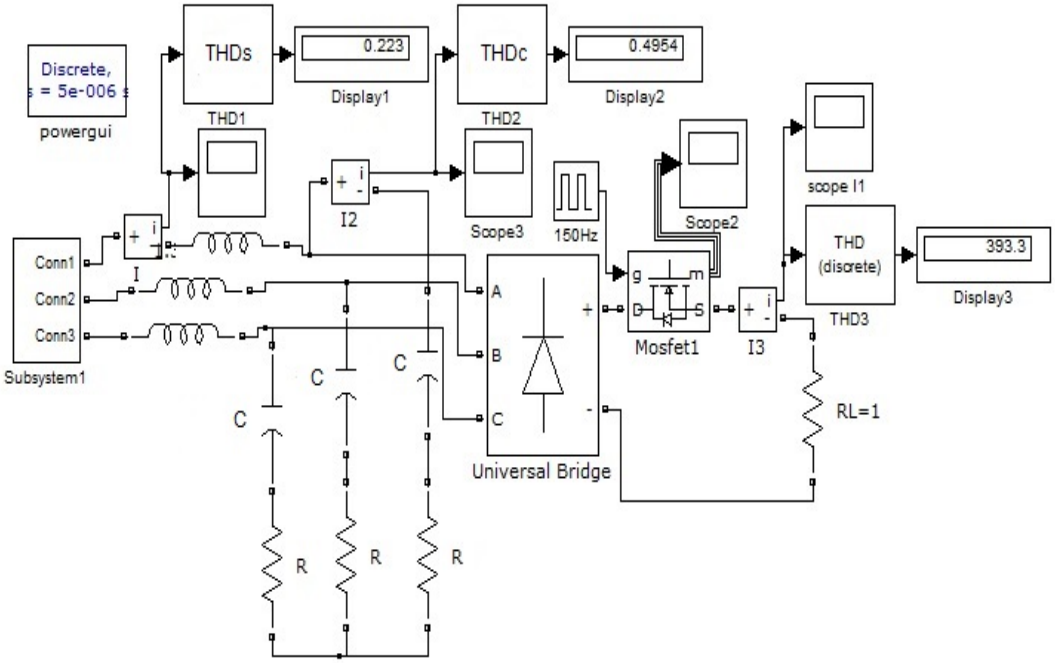


Figure 2.29: Circuit With Low Pass Filter

The effects of harmonics is obvious in figure 2.30 which shows the filter current waveform in the Capacitor's branch before adding APF.

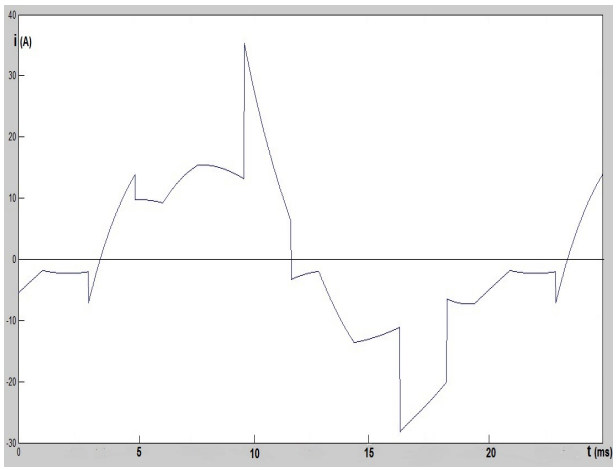


Figure 2.30: C-branch's Current before adding APF

3. The third case circuit represents the newly proposed circuit. This HAPF has been produced by adding a 3-phase shunt active power filter between the capacitor and the resistor in order to compensate the eliminated harmonics

in the RC-branch and in the source current. The circuit is shown below in figure 2.31.

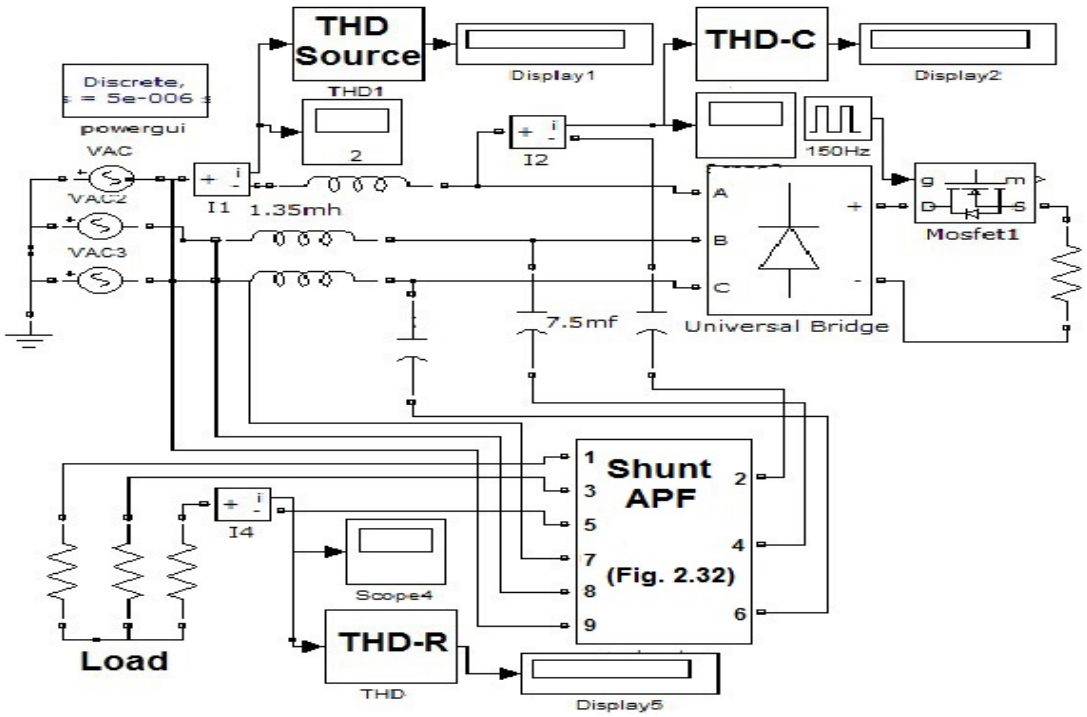


Figure 2.31: New Proposed HAPF

The shunt active power filter (APF) has been designed and tested according to [115] by using The instantaneous reactive power theory, Clarke Transformation and Hysteresis Current Control (HCC) method which is mostly preferred in APF control schemes to control inverter's pulses.

Figure 2.32 shows the design of the APF, figure 2.33 illustrates the control steps which used in the APFs design and figure 2.34 shows the APFs control circuit.

The main aim of this design is to harvest the active (real) power from the distortion power; therefore, the control circuit focuses on compensating the oscillatory part of the real power (P_{os}) as it is produced in a result of the harmonics.

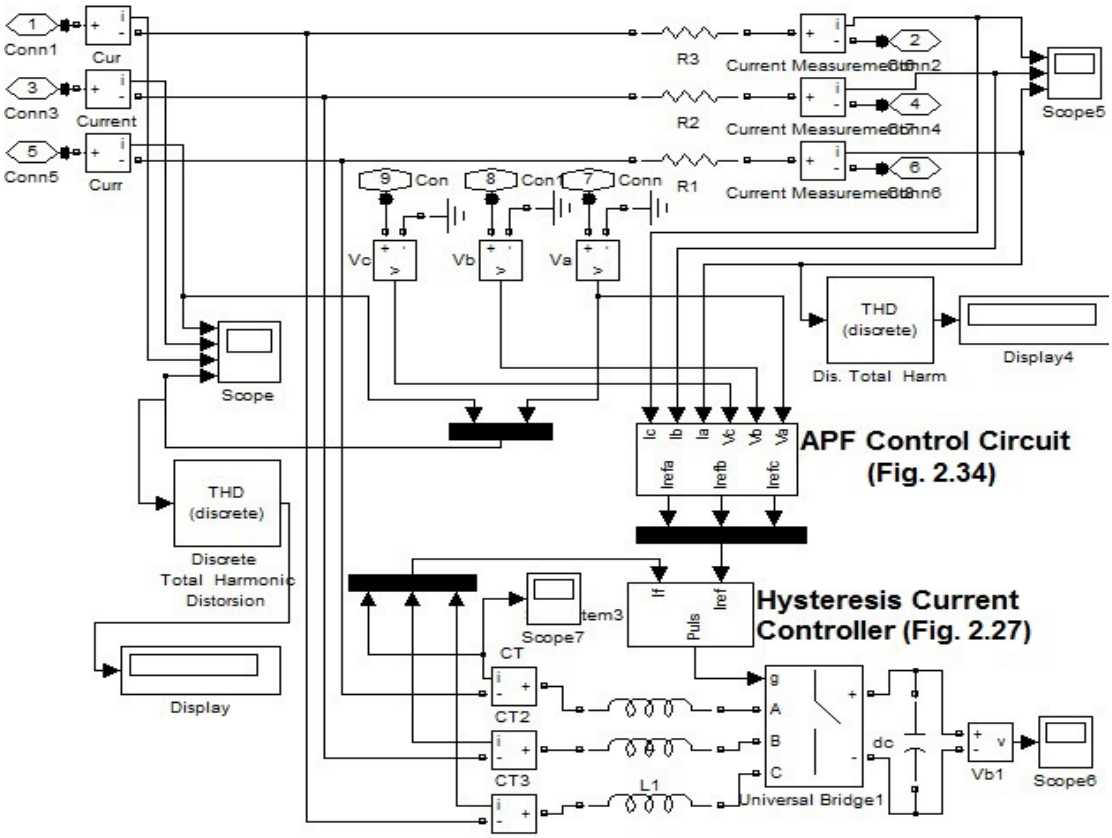


Figure 2.32: Active Power Filter Design

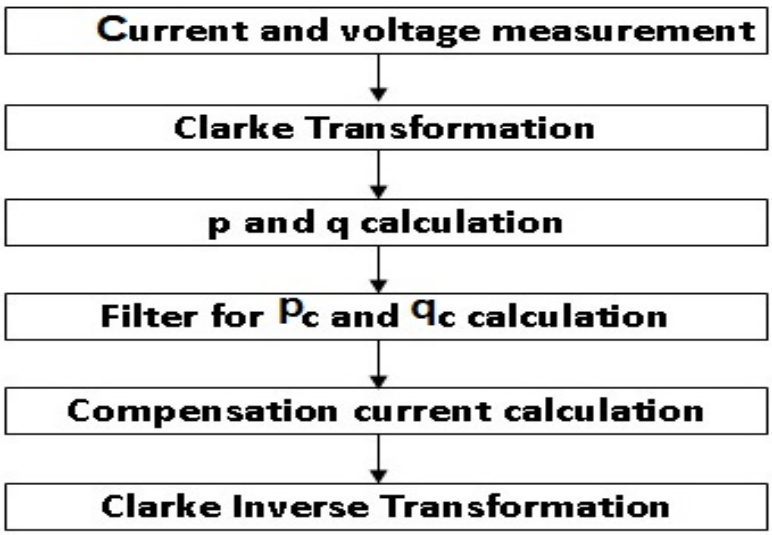


Figure 2.33: APF Control Steps

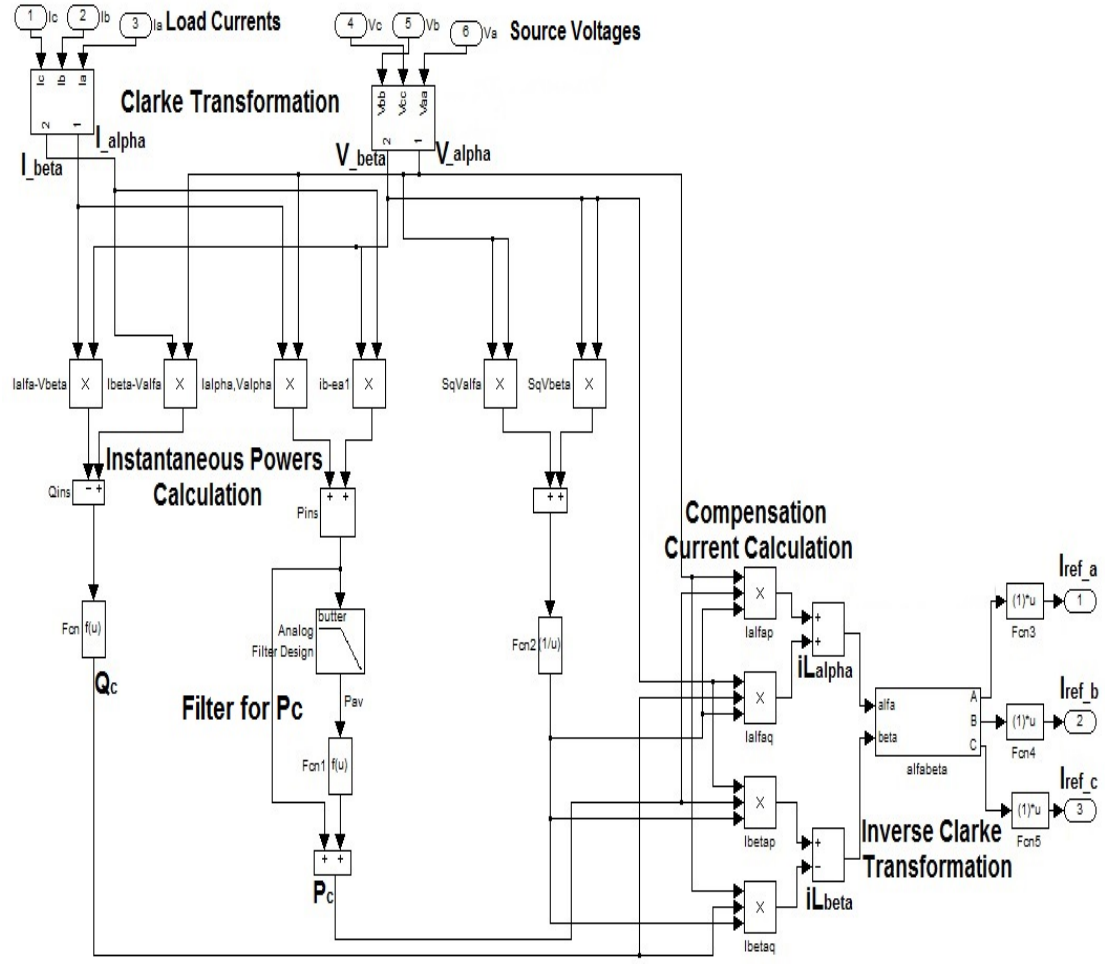


Figure 2.34: APF Control Circuit

2.2.2.1.5 The Design Specification :

Simulation is performed on a three-phase balanced non-linear load as shown below in tables 2.10, 2.11 and 2.12:

V_{Source}	20 AC Volt
system frequency	50 Hz
Load resistor	1 Ω
MOSFET Switching Frequency	150 Hz

Table 2.10: System Parameters

Inductor	1.35 mH
Capacitor	7.5 mF
Resistor	1 Ω

Table 2.11: Low Pass Filter Parameters

Inductor	0.5 mH
DC link capacitor	2.2 mF
Line resistor	1 Ω
Filter impedance	0.42 Ω
F_{tune}	50 Hz

Table 2.12: Active Power Filter Parameters

2.2.2.1.6 HAPF's Method Simulation Results :

All three circuits have been modeled and simulated successfully in the Matlab-Simulink program. The table 2.13 below summarizes the results of the simulation with a comparison between the values of current total harmonic distortion percentage (THD_I%) of three aforementioned circuits.

Case	$R_u(\Omega)$	THD_S	THD_c	THD_R	I_S(A)	I_f(A)	I_u(A)	P_u(kW)
1st	—	74%	—	—	300	—	—	—
2nd	1	22.3%	49.5%	49.5%	330	180	—	—
3rd	1	1.9%	9.7%	8%	500	450	185	34.2
3rd	10	1.6%	4.8%	9%	505	500	22	4.84

Table 2.13: Comparison Among Three Cases

In the first circuit (Without filter), THD_I percentage value was 74% (Because of the performance of the MOSFET). The Low pass filter (LPF) has reduced the value of THD-Source in the second circuit (With LPF) to 22.3%, which shows the effectiveness of the LPF, but the THD of the RC branch became more than 49.5%. In the third case proposed HAPF, the value of THD-Source has reflected the excellent performance of the newly proposed HAPF which reduced THD-Source to 2% and the value of THD-LPF_C has reduced to 9.7%, and the value of THD-LPF_R has reduced to 8%.

Figure 2.35 shows the source current before using filtering process. Figure 2.36 shows the source current after using the proposed HAPF, and figure 2.38 presents the Fast Fourier Transform (FFT) spectrum analysis of the LPF-Resistor branch current waveform after using the newly proposed HAPF. Figure 2.37 shows the waveform of I_R after filtering, the small spikes which are displayed on the waveform represent the effects of harmonics which are reduced in comparing with the waveform shown previously in figure 2.30 which shows the filter current waveform before adding the shunt APF.

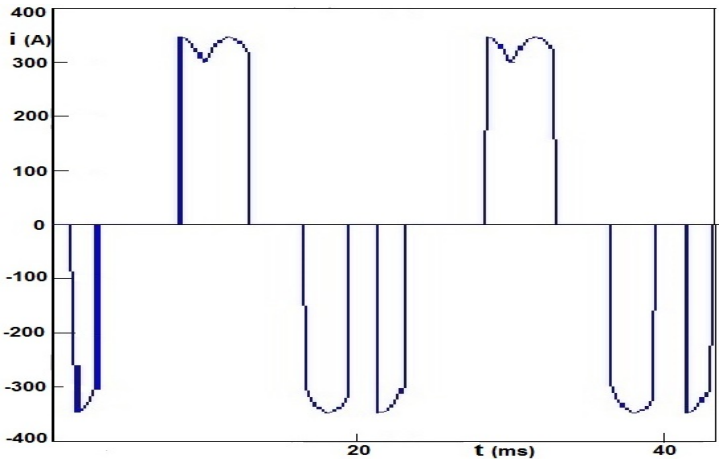


Figure 2.35: Source Current Before Filtering

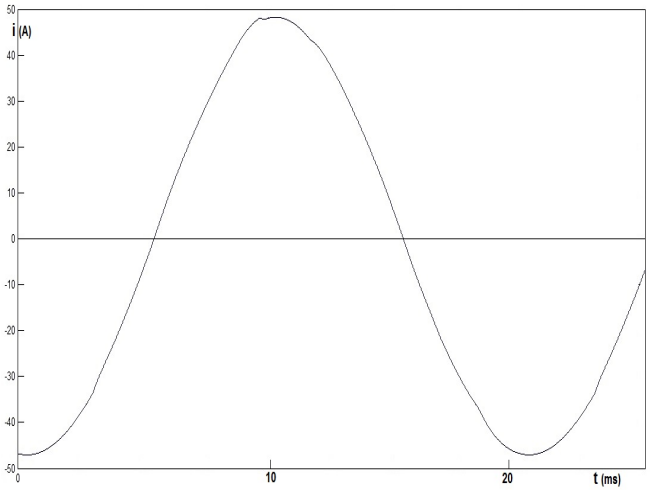


Figure 2.36: Source Current After Filtering

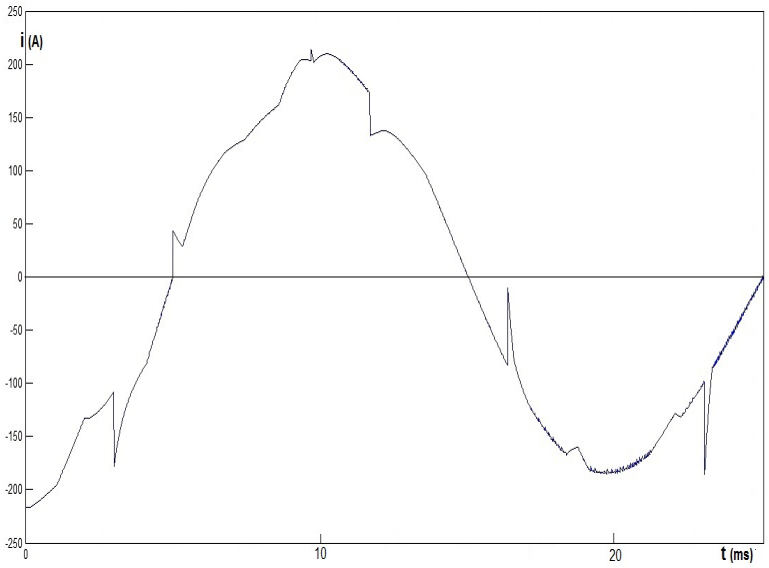


Figure 2.37: The current of resistive load after filtering

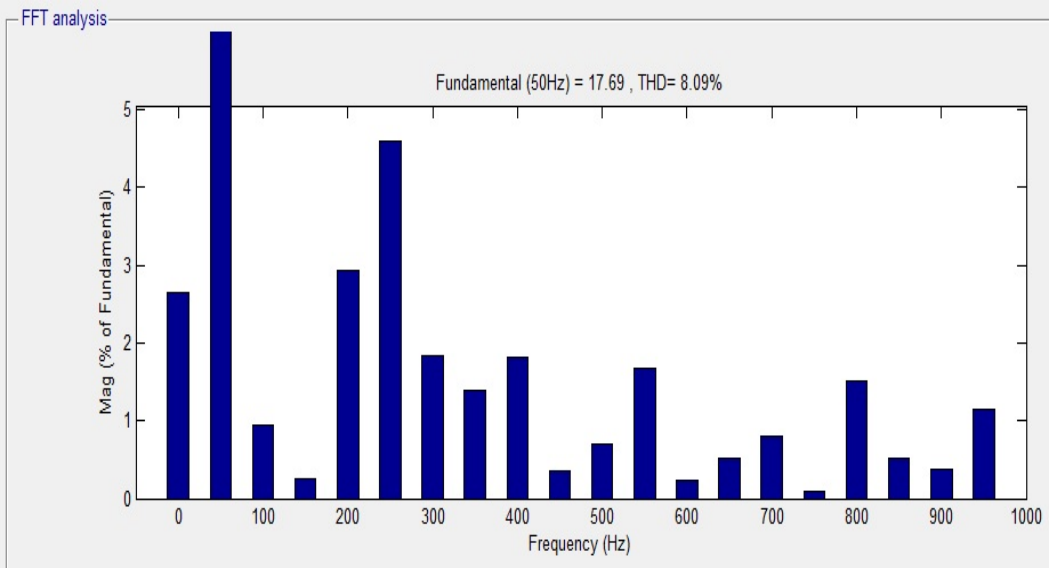


Figure 2.38: FFT spectrum of current of R_{filter} in new HAPF

It can be easily concluded, from the results and waveforms that the $THD_I\%$ in the source and LPF branches has decreased hugely, especially, in the LPF-Resistor branch from 49.5% to 8% and that's prove the ability of using the modified current as a power supply and feed some loads because it contains relatively low THD_I value.

2.2.2.1.7 HAPF's Method Conclusion :

This methodology has presented a new topology of a 3-phase HAPF. The system has been designed, tested and simulated by the Matlab-Simulink program in three steps; firstly, without using filters, secondly, with LC-LPF; finally, using LPF in combining with APF which represent HAPF. After a comparison between the values of total harmonic distortion ($THD_I\%$) in three aforementioned circuits, the results of the simulation have confirmed the effectiveness of the proposed HAPF because of the huge decrease in the THD value (i.e. high rate elimination of the harmonics). The proposed HAPF offers a reactive power compensation for the circuit because of using a shunt APF. Consequently, the power quality of the circuit will improve.

This method has submitted a new idea to benefit of eliminated harmonic current in an RC-branch of the LPF through using the APF in shunt with the RC branch of LPF and compensate high-frequency currents in order to use it as a power supply to feed different loads. In this method, a resistive load has been presented as an invested load. However, in a practical life and laboratory experiments more beneficial loads could be applied.

2.2.2.1.8 The benefits of using HAPF method :

1. Generally, active methods can solve the resonance problem which usually happens between passive filters and the system at specific values.
2. Reduction of harmonic current distortion (Reduced from 49% to 8%) for a utilized load.
3. The utilized power (P_u) is 34.2 kW (when R = 1 Ω), and P_u is 4.84 kW (when R = 10 Ω).

2.2.2.1.9 The limitations of using HAPF method :

1. High initial cost; including active switches, inverter, and PWM control circuit, and high switching losses.
2. Complex control circuit.
3. Requires additional elements which make it bulky.
4. The produced utilization current can only feed resistive loads in very limited values (which is not common).
5. The output current (I_u) waveform has lower PF and higher THD_I of 8%, in comparing with passive filter solution of 2% THD_I .
6. This design is impractical because its draw high source current and works only on small values of resistive loads (1 - 10) Ω.

2.2.3 Comparison & Discussion Between Two Methods

The idea of taking advantage of harmonics current in order to feed electrical loads, and working as a passive power factor corrector (PPFC) have been presented firstly for a three-phase system passive filter as a high voltage model. However, this model suffers from a high source current and a complex design. In order to simplify the design and overcome the drawbacks of 3-phase model, a single-phase system using passive filters has been designed.

Passive Filter Method	**HAPF Method**
Small size (for low power ratings)	Larger size (bulky)
Simple design and control	Complex control circuit and requires additional parameters
No need to use active switches (except for inverter)	Additional cost and losses of active switches
Cheap passive elements and low running cost	Expensive, because of the high initial cost and running cost
Utilization current (I_u) can feed any type of loads	Utilization current (I_u) can only feed capacitive and resistive loads (very limited value of loads)
Does not provide reactive power compensation	Provides reactive power compensation
May suffers of resonance problem between the system and filter	Can solve the resonance problem
The value of THD_I at the output side (Z_u) is 2.1% and the waveform is sinusoidal as shown in figure 2.20	The value of THD_I at the output side is 8% and I_u is almost sinusoidal but with small spikes as shown in figure 2.37
The value of THD_I at the input side reduced from 43.3% to 1.7%	The value of THD_I at the input side reduced from 74% to 2%
In spite of the utilized power is small (2 Watt) but it's extracted without drawing additional (I_S)	The utilized power is 34.2 kW (when R=1Ω), and 4.84 kW (when R=10Ω) but with high (I_S)
Can be applied practically in spite of design limitations and low output power	Not efficient practically because of the high (I_S) and restrictions on load types (only resistive) and load values

Table 2.14: Comparison Between Two Methods (Passive & Active)

This model consists of fewer elements and does not require additional source current for specific value of the passive filter and can harvest the distortion power to feed small loads. In addition, THD_I has been reduced and PF increased at both source and load sides.

The next subsection, presents a three-phase active filter in combination with a passive filter constructing a novel topology of a HAPF as a second method. The utilized power (P_u) is 34.2 kW (when R = 1 Ω), and P_u is 4.84 kW (when R = 10 Ω). However, this design is not efficient practically because of the high current

source and has restrictions on load types (only resistive) and load value limitations (1 - 10) Ω.

A table of comparison can be made between the results of two approaches in terms of achieving lower THD_I, higher PF and lower number and size of parameters which affects the cost and size of the utilization circuit and producing higher power without drawing additional current from the source.

2.2.3.0.1 Summary of Chapter Two :

A comparison has been made in table 2.14 between passive and active methods, according to the simulation results. These points show the priority of the single-phase passive method on the active method in terms of the size, simplicity of design, losses power, cost, limitation of loads, output THD_I, no extra I_S, and applicability in practice life. In addition the output waveform of the utilized current of HAPF looks semi-sinusoidal with spikes, these spikes can cause problems of the power quality like oscillation and may affect other electronic equipment because of the sudden change in current.

All aforementioned points prove that the passive method is more efficient and applicable than the active method in the harmonics utilization.

Chapter 3

Novel Design of Active Power Factor Correction (APFC)

3.1 Introduction

Traditionally, AC/DC converters, which are also called rectifiers, are developed using diodes and thyristors to provide controlled or uncontrolled DC power with unidirectional or bidirectional power flow [6]. Single phase diode rectifiers are extensively used for industrial utilizations. Many conventional switching power supplies in data processing equipment and low power motor drive systems operate by rectifying the input AC line voltage and filtering by using large electrolytic capacitors. The capacitor draws high current in short pulses prefaces several problems including attrition in the available power and increase losses. The capacitor voltage retains the peak voltage of the input sine wave until the next peak comes along to recharge it again [7].

In such situation, the capacitor draws a current from the input source just at the peaks of the input waveform, and this pulse of current must contain enough energy to sustain the load until the next peak. This process can be achieved by dumping a large energy into the capacitor during a short time, after which the

capacitor slowly discharges the energy into the load until the cycle repeats. The current pulse takes 10% to 20% of the cycle duration, meaning that the current during the pulse must be 5 to 10 times of the average current and increases its r.m.s. value [7]. This process involves both non-linear and storage elements and results in the generation of harmonics in the line current. The non-linear characteristics of loads such as computers, printers and variable speed motor drives (used in washing machines or air-conditioning) have made a harmonic distortion in electrical distribution systems. However, when operating in large numbers, the cumulative effect of these loads has the capability of causing serious harmonic distortions. This may lead into a poor power quality, high THD, poor power factor at input ac mains, voltage distortion, slowly varying rippled DC output at the load side and low power efficiency [123]. The non-ideal character of these input currents creates a number of problems for the power distribution network and for other electrical apparatus in the neighbourhood of the rectifier systems. This approach has many drawbacks, including high-input harmonic current components, a low rectifier efficiency due to large RMS value of the input current, input ac mains voltage distortion because of the associated peak currents and a maximum input power factor is approximately 0.6, while a larger filter inductor is required for a high-input power factor [59].

Because of the strict requirement of power quality at the input AC mains, several standards have been developed and are being enforced on the consumers. Because of the severity of power quality problems some other options such as passive filters, active filters, and HAPFs along with typical rectifiers, have been extensively developed especially in high power ratings and already existing installations [80].

However, these filters are expensive, heavy, and bulky and have reasonable losses which reduce the overall efficiency of the complete system. Under these conceptions, it is considered a better option to include PFC converters as an inherent part of the system of AC/DC conversion, which provides a reduced size, a higher efficiency, and well controlled and regulated DC to provide a comfortable and

flexible operation of the system [6].

Nowadays, the expansion of using the electronics devices has resulted in a larger need to guarantee that the input current harmonic ratio of each apparatus connected to the power grid is limited to satisfy the regulatory standards. This important condition can be investigated by merging some form of PFC circuits in order to form the input phase currents so that they are sinusoidal in nature and are in phase with the input phase voltages. The researchers invented many solutions in order to decrease the THD, get the unity PF at the input side and achieve regulated output voltage at the output side [7].

PFC circuit is substantial for AC/DC converters in order to be interrogated with the requirements of international standards, such as IEC61000-3-2 and IEEE-519. In addition, PFC can increase the power conversion efficiency and capacity of power systems. Consequently, can decrease the utility bill for the customers [80].

The PFC technology has been developed now at a reasonably matured level for AC/DC conversion with reduced harmonic currents, high power factor, low electromagnetic interference (EMI) and radio frequency interference (RFI) at input AC mains and well-regulated and good quality DC output in order to feed loads ranging from a fraction of Watt to several hundred kilowatts power ratings in large number of applications. In the last 40 years, a huge number of research of different topologies, control methods, active switch devices, various configurations of reactive elements, multilevel with unidirectional and bidirectional power flow architectures have been designed and implemented [123].

3.2 Literature Review of PFC

Single phase AC/DC rectifiers with a large electrolytic capacitor are commonly used for manufacturer and business issues. The main purpose to use diode rectifiers is to operate the switching power supply in data processing apparatus and to operate low power motor drive systems.

The large capacitor draws current in short pulses, which brings in a lot of problems including decreasing in the available power, increasing losses and reduction of the efficiency. In the conventional way of design, the capacitor voltage preserves the peak voltage of the input sine wave until the next peak comes along to recharge it [123]. The only way to recharge the capacitor is by drawing the current from the input source at the peaks of the source waveform as a long pulse which includes an adequate amount of energy to nourish the load until the next peak. This happens when the capacitor draws a large charge during a short time, after the slowly discharge of the capacitor into the load. Therefore, the capacitor's current draws 5 to 10 times of the average current in 10% or 20% of the cycle period. Consequently, the source current has narrow and long pulses and the effective (R.M.S.) value increases [7].

The major drawbacks of conventional AC/DC converters are:

1. Poor power quality.
2. Poor power factor at input ac side which reduces maximum power capability.
3. Very slow varying rippled dc at the load side.
4. Produces high loss which causes low efficiency.
5. Larg size components of AC and DC side filters (bulky design).

Several issues must be taken into account when determining which type of PFC's is the most recommended topology, like: robustness, power density, efficiency,

cost, weight, size and complexity [124].

The search of novel topologies came as imminent effort to introduce PFC with the following specifications:

1. High PF rectifier with reduced harmonics at the input AC side.
2. Reduced size and weight of magnetics.
3. Minimized electromagnetic interference (EMI) levels.
4. Low losses and a high power conversion efficiency.
5. Increased robustness.
6. Good line and load regulation.
7. Universal input voltage operation.
8. Low part count and low cost.

3.2.1 Power Factor Correction (PFC) Circuits

PFC circuits can significantly minimize losses and costs associated with the generation and distribution of the electric power with significantly improved power quality. Therefore, nowadays PFC is receiving more and more attention because of the widespread use of electrical applications that draw non-sinusoidal current from the electric power systems. There are several methods to reduce the harmonic contents of the line current in single-phase systems.

The classification of single-phase PFC Methods is shown in figure 3.1. The diode bridge rectifier has no sinusoidal line current. This is because most loads require a supply voltage (V_s) with low ripple, which is obtained by using a correspondingly large capacitance of the output capacitor. Consequently, the conduction intervals of the rectifier diodes are short and the line current consists of narrow pulses with important harmonic contents.

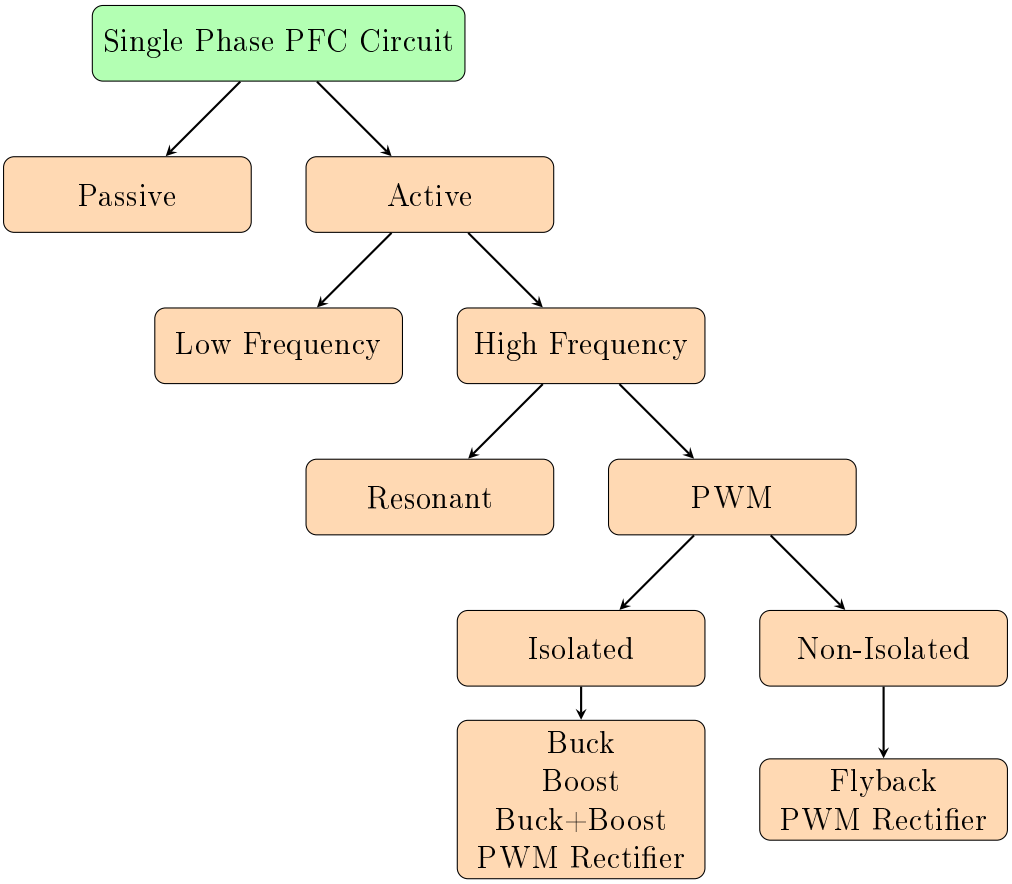


Figure 3.1: Single Phase PFC Methods

3.2.1.1 Passive Methods of PFC

Wide range of literature available regarding using reactive elements on AC side (before rectifier) or DC side (after rectifier), and in general have common advantages and disadvantages [125].

3.2.1.1.1 Advantages of Passive PFC :

1. Simple system implementation and easy to design and understand.
2. Fewer components.
3. Smaller size than active for low power (less than 200 watt).
4. Higher reliability and robustness.
5. Absence of active switches and control circuitry.
6. Clear of noise and electromagnetic interference (EMI) [125].

3.2.1.1.2 Disadvantages of passive PFC :

1. Difficult for passive circuit to reach (0.6 - 0.7) power factor without using big size of reactive elements which means big value of THD (more than 150%).
2. Lack of voltage regulation and poor dynamic response.
3. Suitable for limited operating conditions. When the operating condition (such as the input or output voltage) changes, the passive PFC may no longer satisfy the required voltage.
4. Passive PFC, can not utilize the full energy potential of the AC line.
5. Only suitable for low power supply system (less than 200 watt), because the capacitor becomes bulky when the power is more than 150 watt.

6. As the size of passive elements increase, it's not economical due to the weight and cost increasing for high power ratings.

7. Even though, line current harmonics are reduced, the fundamental component shows an excessive phase shift which reduces the power factor.

8. Lack of flexibility [125].

3.2.1.2 Active Methods of PFC

The active methods of PFC, which involve the shaping of the line current, using switching devices such as MOSFETs and IGBTs, is a result of advances in power semiconductor devices.

3.2.1.2.1 Advantages of APFC :

The use of active techniques of PFC results in one or more of the following advantages:

1. Lower harmonic contents in the input current in comparison to the passive techniques, can remarkably diminish THD (10 - 30)%.

2. Reduced r.m.s current rating of the output filter capacitor.

3. Unity power factor is possible to achieve.

4. For higher power levels, active techniques of PFC will result in size, weight and cost benefits over passive techniques of PFC.

5. Successfully used in high power application (greater than 250 watt).

6. Capable of use the full range of input voltage [126].

3.2.1.2.2 Disadvantages of APFC :

1. Requires additional, accurate and more expensive components like active switches (MOSFET) and complex circuitry for the active devices.
2. Reduction in typical efficiency (5% to 10%), due to additional losses of conducting and switching losses.
3. Problems produced because of using power electronics devices (including EMI and diode recovery problems).
4. The size and cost of reactive elements still an issue of concern with the need of using minimum size devices [126].

3.2.1.2.3 Classification of APFC Based on Switching Frequency :

1. Low-Frequency Active PFC.
2. High-Frequency Active PFC.

3.2.1.2.4 Classification of DC/DC Converters Based on Structure

1. Buck converter [127].
2. Boost Converter [128].
3. Buck-Boost Converter [129].
4. Forward converter [130].
5. Push-pull converter [131].
6. Bridgeless converter [132].
7. Half-bridge converter [133].

8. Full-bridge converter [134].
9. PWM converter [135].
10. Resonant converter [136].
11. Flyback Converter [137].
12. Single Ended Primary Inductor Converter (SEPIC) [138].
13. Cuk converter [139].
14. Zeta converter [140], [141].

3.2.1.2.5 Boost Converter :

Boost converters which operating in continuous current mode (CCM), have become particularly the most popular converter, because of the reduced electromagnetic interference (EMI) levels results from its utilization in power electronics applications.

3.2.1.2.6 Boost Converter Topologies :

The Boost converter has many topologies and each type has its advantages and disadvantages. The most public Boost topologies can be gathered in the following points as mentioned in [142]:

1. Conventional boost converter (CBC) [143].
2. Bridgeless boost converter (BBC) [144], [145].
3. Interleaved boost converter (IBC) [146].
4. Three level boost converter (3LBC) [147].
5. Half-bridge and Full-bridge boost converter (HBBC) [148], [149].

6. Voltage doubler boost converters based on three static switching cell (VDBC3SSC) [150].

Each topology has its own advantages and disadvantages. A comprehensive qualitative comparison among these topologies and the newly proposed PFC circuit, will be shown in the next result assessment section in table 3.11.

3.2.1.2.7 Disadvantages of Boost Converter :

Generally, each topology has its own advantages and disadvantages. The most common topology is the conventional boost converter (CBC). However, CBC suffers from many drawbacks as mentioned below:

1. A large duty ratio is required for a large voltage boost, which places a practical limit on the achievable voltage step-up due to the large volume and weight of the required capacitance. Therefore, in order to maintain acceptably small output ripple voltages, a prohibitively large capacitance is required to ensure that the output voltage does not sag as the stored energy is supplied by the main capacitor (C) during the duration (D).

2. Requires large value of inductor (mH) Since both (DC and AC) currents are being sourced through the inductor; therefore, the inductor must be designed such that the cores will not saturate during high power operation.

3. An elevated temperatures typically lower the saturation flux threshold of the inductor core material, making this requirement a more significant design consideration.

4. It requires a large output capacitor to reduce the current ripple and it is not suitable for a high power conversion [151].

5. The boost converter requires high switching frequency in order to achieve high power density and faster transient. However, as the switching frequency

increases, the output diode operated in high voltage provides a significant reverse- recovery loss in a hard switching converter which causes additional turn-on losses (unless uses additional snubber circuit). In addition, reverse recovery problem causes different problems like EMI increasing and requires additional thermal management.

6. A reduction in efficiency and increasing of conduction losses due to continuity of current flowing through at least 3 semiconductor elements (depending on the design) in each cycle. [124]

3.2.1.2.8 Classification of PFC Based on Stages number :

Generally, the active PFC converters can be divided into two categories: the two-stage approach and the single-stage approach.

1. Two stage converter (Power Factor Pre-regulator (P.F.P) + DC/DC converter).

2. Single stage converter.

3.2.1.2.8.1 Two-Stage Converter :

The two-stage approach is the most commonly used approach [152]. In this approach, an APFC stage is adopted as the front-end to force the line current tracking the line voltage. A DC/DC output stage provides the isolation and the tightly regulated output voltage to meet the load requirement. However, this approach suffers from some drawbacks in low-power cost-effective applications because it requires additional PC components (at least two active switches with two control circuits and bulky capacitor to reserve the unregulated energy and control the output DC voltage) which increase size, weight and cost and the complicate PFC control circuit (increases complexity). Thus it has additional losses and less efficiency [153].

On the other hand, two-stage model is probably the best option for AC-DC converters due to the following reasons:

1. Sinusoidal line current guarantees the compliance of any regulation.
2. It gives a good performance under universal line voltage.
3. It offers many possibilities to implement both the isolation between line and load, and the hold-up time.
4. The penalty on the efficiency due to the double energy processing is partially compensated by the fact that the voltage on the storage capacitor is controlled. The fact of having a constant input voltage allows a good design of the second stage.
5. The output is tightly regulated and low ripple factor.

3.2.1.2.8.2 Single-Stage Converter :

As an alternative and a cost-effective solution to the problems of the 2-stage converter, the single-stage PFC approach has been proposed [154]. The main idea is to integrate the active PFC stage with the isolated high-quality output DC/DC stage into one stage. In this approach, the PFC switch and its controller are saved while the converter still has fair input current and an isolated high-quality output. Normally, it is expected that the single-stage PFC converter will have lower cost than the 2-stage PFC converters, however, it depends on the different applications.

In [153], a general comparative manufacturing and cost analysis of the different PFC approaches is presented.

In the following, the advantages of single stage PFC converter:

1. One circuit with single input and output (expected less size and cost).

2. A single switch shapes the input current and regulate the output voltage at the same time (easy to design).

3. The PFC function is automatically achieved based on the principle of the circuit operation instead of using additional controller (simpler control).

4. Single control circuit (controls the output voltage).

5. It has a high bandwidth so the output voltage is tightly regulated [153].

Disadvantages of Single-stage PFC Converter:

1. The input voltage (which is the main capacitor's voltage) has very wide range. That is very undesirable, because its very hard to optimize the DC/DC stage and at the same time requires a huge high voltage bulky capacitor to meet the hold-up time requirement ($C_{\text{single-stage}} = 7$ x $C_{\text{two-stage}}$).

2. Uses additional inductor to achieve the continuous current mode (CCM) function.

3. Adding an active clamped circuit (ACL) reset circuit to achieve the maximum duty cycle in order to overcome the disadvantage of low bus voltage at low line.

4. The unity power factor is not achievable as the tight controlled V_{out} is required.

5. The produced I_{rms} on the switch in a single stage is higher than the sum of two switches of the 2-stage. Then, the switch is larger in size and the losses are bigger. Therefore, the efficiency in single stage converter is less than 2-stage converter [153].

Consequently, after all these disadvantages of single-stage PFC, the two-stage converter seems to be the best approach in comparing with single-stage PFC. However, the drawbacks of two-stage still need to be addressed.

3.2.1.2.9 The Gap in Knowledge :

Each point of the aforementioned disadvantages of the conventional boost converter and 2-stage approach is an important problem and needs to be addressed. However, in the practical life; the cost, the size, and the weight are essential points for each component with the proliferation of new technology devices. This chapter, investigates the reduction of the inductor's size (from mH into µH) via designing a new APFC circuit.

The newly proposed PFC circuit has the ability to solve almost all the problems and disadvantages of 2-stage converters; therefore, it can be successfully the best alternative for the first stage of the two-stage PFC approach which is power factor pre-regulator (P.F.P.) as shown in figure 3.2.

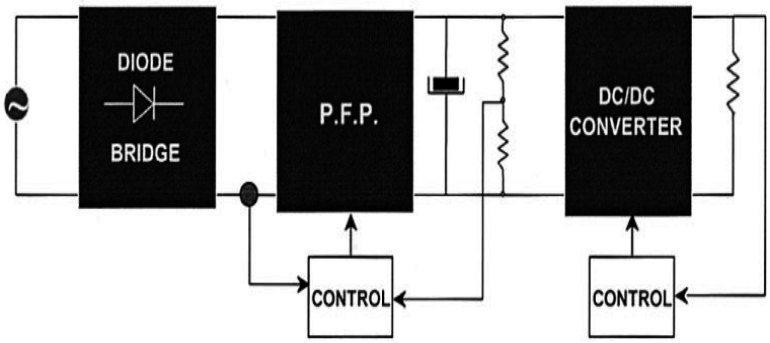


Figure 3.2: Two-stage AC/DC PFC converter

The new circuit decreases the value of the inductor into (1 x L/54) which is equal to more than 98% reduction in comparison with the inductor in the traditional boost converter. This reduction solves the issue of the size and the cost in 2-stage approach. In addition, the style of switching the MOSFET may eliminate the third order harmonic current from the input waveform which reduces the THD_I to less than 14% and increases the input PF to (0.99). At the same time, this pattern of switching gives the flexibility in controlling the output voltage and current and gives the output wide range of tolerance. Furthermore, the new PFC circuit has been tested successfully for different loads and output power (up to 45

kW) and the circuit was applicable in high efficiency in all the cases (more than 95%) even with high power ratings.

3.2.1.3 The Value of Inductors in Different PFC Topologies

Achieving the minimum amount of magnetics and decreasing the size and volume of the inductors in PFC circuits design have the priority for the engineers with the increasing of consumer's trend to use a minimum size device.

The authors in [142], have made a comparison among different boost converters in many points of assessment. One of the presented points was the number and value of the filter inductors used in every design. Clearly, it can be concluded that (VDBC3SSC) uses the smallest size inductor (among CCM boost converters) when uses one reduced size inductor (1 x L/16). This reduction of the inductor's value it will effectively contribute in reducing the size, weight and the cost of the converter. However, this topology requires additional autotransformer, four active switches and four diodes operating at a high frequency which increase the size, weight and the cost of the converter.

The newly proposed PFC circuit uses the smaller value of inductance when it uses one small size inductor (1 x L/54) which is (10 µH) at the same power ratings. At the same time, the new design uses just two active switches and one diode operating at high frequency without using additional autotransformer. The inductor's value used in the literature in [155] for a (3 kW) output power and high-frequency switching (100 kHz) for an interleaved boost converter was (L/2 = 270 µH). The value of inductor (L) in the conventional boost converter (CBC) is (540 µH), and the value of (L) in (VDBC3SSC) is (34 µH) for the same power ratings.

3.2.1.4 Elimination of The Third Order Harmonic

The third order harmonic current is the most significant component in single-phase systems; therefore, it has the major bad effects on the electrical equipment. For this reason, many methods have been designed and implemented in order to eliminate the 3rd order harmonics from the input current by using different application including PFC converters [156], [157]. On the other hand, the idea of active filters has been used for re-injection 3rd order harmonic to the electrical grid in order to reduce THD and get the unity power factor for PFC rectifiers [158]. However, all the solution of 3rd order harmonic elimination depends on adding new reactive elements to the circuit which increases the size, cost and complexity of the design.

The newly proposed design depends on switching a MOSFET in a specific way that leads to reducing the operation time of the main capacitor and preventing it of charging and drawing high current from the source while the waveform at the peak value in order to avoid the sinusoidal current turning into short time pulses. This pattern of switching prevents the third order harmonic and shifts the harmonic current into higher frequencies (5th and 7th) orders which apparently, have less effect on the grid and improves the input PF without adding additional or bulky elements to the circuit.

In a similar way, the authors in [159] used a new architecture of AC/DC rectifier with reduced size capacitor in order to get high input PF (0.94). The control scheme which governs the action of the switches has divided the operation time of the rectifier into three regions depending on the reference DC level of the capacitor. The capacitor just working on the two terminal of the waveform. However, the design uses two active switches and two additional diodes with carefully designed external control circuit, third order harmonic current still the most significant order among other orders and the unity input PF has not been achieved.

3.3 Methodology

3.3.1 Using Two Switches APFC

3.3.1.1 Circuit's Description

The circuit schematic of the new PFC circuit is shown in figure 3.3. The input (V_S), is a single-phase AC source. (V_S) connected to a full-wave bridge rectifier with one freewheeling diode (FWD), two switches SW_1 & SW_2 represent PE devices (MOSFETs) which can work in different modes and different switching frequencies, (L) inductor, (C_1) main capacitor and small valued capacitor C_2. These elements are all connected in parallel with a resistive load.

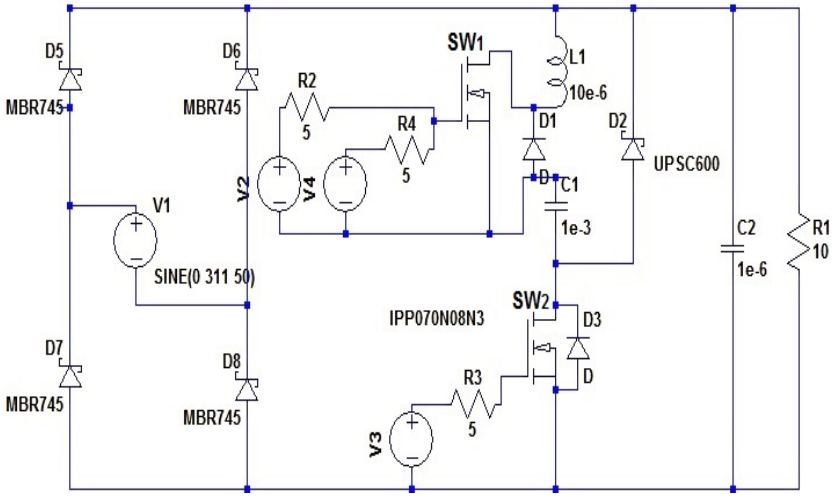


Figure 3.3: New proposed PFC circuit

3.3.1.2 Operation Topology

The newly designed circuit can change the value of the input power factor (PF), the value of THD_I of the source current waveform and the value of the output ripple load voltage by using two MOSFETs SW_1 & SW_2 and series LC-circuit connected in parallel with the load and with the input power supply.

The proposed circuit has been designed depending on the principle of dividing the

working time of the main capacitor (C_1) via switching MOSFET-1 in 50 Hz, but chopped its current into three regions: ON, OFF, ON and maintaining the duty cycle of SW_1 to works in a fixed time periods.

Accordingly, SW_1 prevents (C_1) from working in the (OFF) time (which is the peak value of the waveform), that will result in decreasing the effect of C_1 on the input current, eliminates the third order harmonic component and in result, it improves the input PF. At the same time, SW_1 will shift all the harmonics components to the high-frequency region which reduces the probability of using a bulky low-frequency filter as the frequency inversely proportions with the square of LC; therefore, the design would require less number of components and smaller values. Consequently, reduces the size, weight and the cost of the newly designed circuit.

SW_2, reduces the effect of the inductor current's spikes and reduces the charging time of main capacitor current (I_{C1}) which decreases the losses and improves the efficiency, at the same time helps to improve the output waveform and reduce the ripple DC voltage.

(C_2), is an optional small value capacitor (not compulsory). The duty of (C_2) is to suppress the high-frequency spikes at the output load waveform.

The freewheeling diode (FWD) offers a unidirectional way for inductor current (I_L); therefore, (I_L) will remain on a positive value. Accordingly, (FWD) prevent the negative part of (I_L) and helps (C_1) to act as a snubber circuit in order to discharge in (C_1) and prevent inductor voltage (V_L) of increasing more than rated value of the source voltage. This is equal to the negative value of voltage of the active switch MOSFET-2 (V_{sw2}) when SW_2 is OFF, and protects the circuit in general and specially the MOSFET switches from being burned in a result of the high voltage spikes.

3.3.1.3 Control Topology

The control circuit of chopping process of the current of MOSFET-1 which controls the working period of (C_1) has been designed simply (without needing external complex control circuit), by using two parallel sources work in different periods (these periods are flexible and easy to change desirably) as explained below in the piecewise equations. On time periods (T_{on}) of SW_1 are specified as 3ms at the beginning of the cycle and 3m at the end of the cycle when switching frequency is $f_{sw2} = 200$ kHz and $t_2 = 5\mu s$. The duty cycle is 60% in total for SW_1. The duty cycle of SW_2 has been specified as 40%.

$$SW_1 = \begin{cases} \text{ON} & 0 < t < 3 \text{ ms} \\ \text{OFF} & 3 \text{ ms} \leq t < 7 \text{ ms} \\ \text{ON} & 7 \text{ ms} \leq t < 10 \text{ ms} \end{cases}$$

$$SW_2 = \begin{cases} \text{ON} & 0 \leq t < 2\,\mu\,\text{sec} \\ \text{OFF} & 2\,\mu\,\text{sec} \leq t < 5\,\mu\,\text{sec} \end{cases}$$

3.3.1.4 The Design Principle

The use of a single capacitor in parallel with the source without any additional component in series with the main capacitor ideally is impractical because the inrush current of the main capacitor (I_{C1}) when (t = 0) is (∞), as $I_{C1} = C\frac{dV_c}{dt}$, and $V_{c1} = 0$ when switch closes then a short circuit will be applied on the terminals of the source and may burn the diodes and switch. However, practically ESR value of (C) and internal conductance of diodes will prevent this, but with big values of enormous values of capacitors that could be happened.

In order to avoid that, an additional element has to connect in series with the capacitor (C_1). Therefore, using of an inductor in series with the main capacitor

is the best choice as it is reservoir component and don't consume additional power (e.g. resistor).

One of the requirements of the capacitor voltage (V_{C1}) used in PFC circuits is to be least ripple and high smoothness as it represents the minimum value of the output DC waveform. Therefore, $\frac{dV_{c1}}{dt}$, must be on a minimum value (ideally zero). In this design, ΔV_{c1} has been chosen as (0.04), (for design specification).

In order to calculate a suitable value for (C_1), let suppose a (5 kW) output load and R = 10 Ω, then I_{Load} = 22.36 A r.m.s, because (P = I^2 . R). The capacitor should be charged with the same I_{Load} current in order to be able to feed the load sufficiently. When $I_{Lmax} = Ic_{max}$ = 22.36 A, duty cycle (D_2) = 40% ,

and f_{sw2} = 200 kHz, then: C = $\frac{I_c.\text{duty cycle}}{\Delta V_{c1}.f_{sw2}}$ = 1 mF.

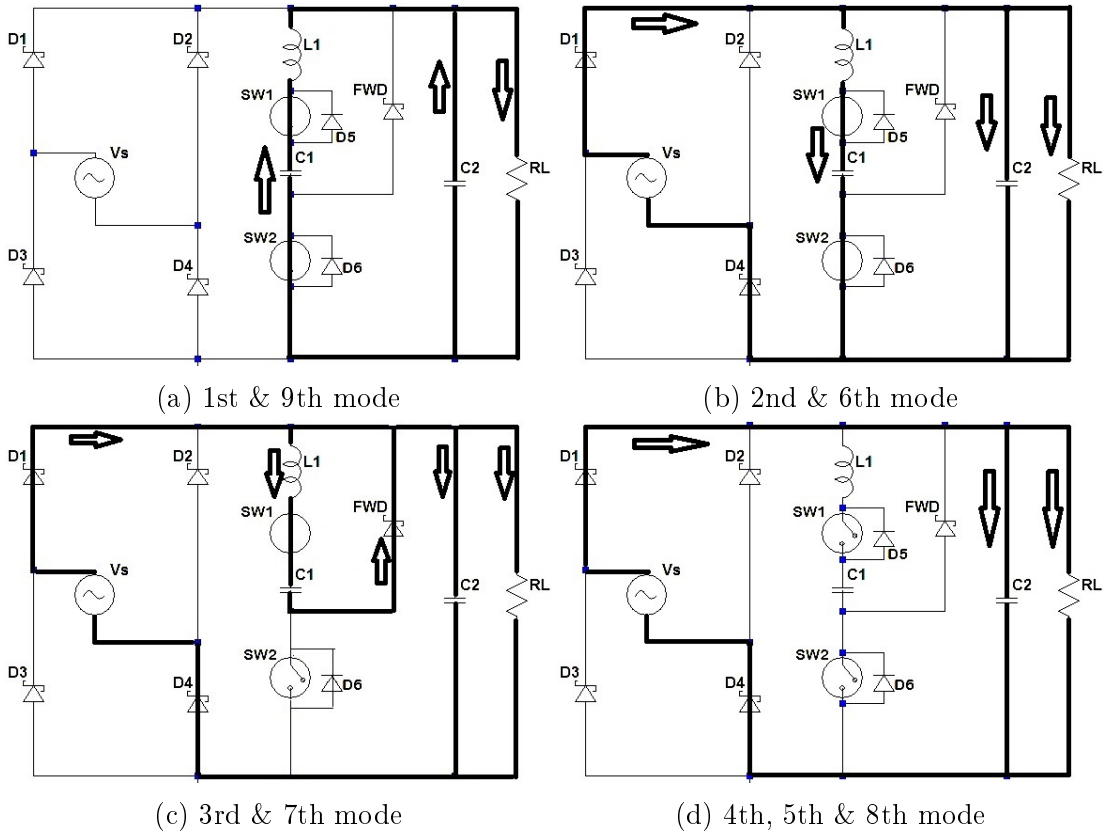
On the other hand, in the worst case, when V_{c1} is zero, then the output waveform is as same as the output of full wave bridge rectifier, and $V_S = V_L$. According to the design requirements, for duty cycle (D_2) = 40%, the switch-1 turns off at 30% of the first half cycle which is corresponding with 54° of the waveform, then in the worst case $V_S = V_L$ = 178 rms volt. In order to calculate the value of (L) this equation 3.1 can be used:

$$\because V_L = L\frac{di_L}{dt} \quad \rightarrow \quad \therefore L = \frac{V_L.\text{duty cycle}}{I_L.f_{sw2}} = 15.9\,\mu\text{H} \tag{3.1}$$

Accordingly, for an accurate design, the value of the main inductor (L_1) can be chosen around 10 µH to 20 µH.

3.3.1.5 Operation Stages

1. First mode: For the time period $0 \leq t < t_1$, when $V_{C1} > V_s$. SW_1-ON and SW_2-ON/OFF, while (t_1) is the moment when V_S is equal or bigger than V_{C1}. The circuit shown in figure 3.4, illustrates the active path of the current at this mode:



(a) 1st & 9th mode (b) 2nd & 6th mode

(c) 3rd & 7th mode (d) 4th, 5th & 8th mode

Figure 3.4: Circuit diagram in different time modes

$(C_1), (L_1)$ & (C_2) are discharging while the R-load is fed by (C_1).

$I_{L1} = I_{C1} = C_1 \frac{dV_1}{dt}$ because (L_1) and (C_1) are in series.

$I_{L1} + I_{C2} = I_R$

$\therefore I_{L1} = \frac{V_{out}}{R} - C_2 \frac{dV_{C2}}{dt}$

$V_{C2} = V_R = V_{out} = V_{C1} + V_{L1}$

$\because V_{L1} = L_1 \frac{di_{L1}}{dt}$,; therefore, the value of V_{L1} is approximately zero because

the value of (L_1) is very small (few micro henres).

$\therefore V_{C2} \approx V_{C1}$

2. Second mode: For the time period $t_1 \leq t < t_2$, when $V_s > V_{C1}$, SW_1 is ON and SW_2 is ON. (t_2) is the moment when SW_1 turns off. The circuit shown in figure 3.4a, illustrates the active path at this mode.

   In this mode, (C_1), (C_2) and (L_1) are charging in high frequency switch pulses of SW_2; therefore, short time current spikes appear on the input current waveform because the inductor current is charging in presence of switching. The load is fed by the source.

   $V_s = V_{C1} + V_{L1} = V_{C2} = V_R = V_{out}$

   $\therefore V_s = V_{C2} = V_{C1} + L_1 \frac{di_L}{dt}$

   $I_s = I_{L1} + I_R + I_{C2}$

   $I_{L1} = I_s - C_2 \frac{dV_{C2}}{dt} - \frac{V_{out}}{R}$

3. Third mode: For the time period $t_1 \leq t < t_2$, when $V_s > V_{C1}$, SW_1 is ON and SW_2 is OFF until (t_d) msec. (t_d) is the moment when (I_{L1}) discharges to zero ampere. The circuit is shown in figure 3.4b.

   At this mode, (L_1) discharges its current to (C_1) until being zero (at the t_d moment), while the inductor voltage (V_{L1}) is equal to V_{C1} and remains charged.

   $\because V_{L1} = V_{C1}$ & $I_{L1} = I_{C1} = C_1 \frac{dV_{C1}}{dt}$ $\therefore X_L = X_C$

   $2\pi f L_1 = \frac{1}{2\pi f C}$ $\therefore f_r = \frac{1}{2\pi\sqrt{LC}} = 1.59kHz$

   (f_r) is the resonance frequency.

   At this mode, the load is fed by the source.

   $V_{L1} = L_1 \frac{di_{L1}}{dt} = V_{C1}$

   $V_s = V_{C2} = V_R = V_{out}$

$\because V_{C2} = V_{C1} - V_{L1} + V_{D6}$

$\therefore V_{C2} = V_{D6}$

$\because I_s = I_{C2} + I_R$

$\therefore I_s = C_2 \frac{dV_{C2}}{dt} + \frac{V_{out}}{R}$

and $I_{L1} = I_{C1} = C_1 \frac{dV_{C1}}{dt}$

4. Fourth mode: For the time period $t_1 \leq t < t_2$, when $(V_s) > V_{C1}$, SW_1 is ON and SW_2 is OFF, from (t_d) until the next ON-pulse for SW_2. The bold line of the circuit shown in figure 3.4c, clarifies the current's path.

   At this mode, the inductor current (I_{L1}) supposed to remain zero ampere. However, the internal capacitance of the diodes combines with stray inductance which form resonant circuit called parasitic resonant (w_p). Due to this parasitic resonance, a sinusoidal current can flow into the inductor (L_1) in a very high frequency (about 1.54 MHz) called self resonant (or parasitic) frequency (f_p). At the same time, V_{L1} follows I_{L1} waveform and oscillate around zero. as shown in figure 3.5:

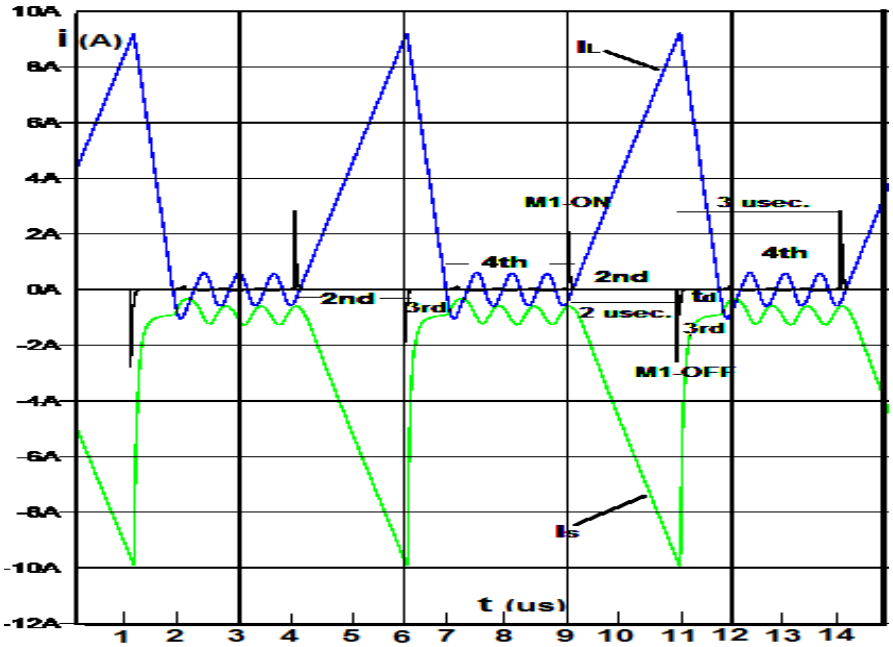


Figure 3.5: I_{L1} & I_S in (2nd, 3rd & 4th) modes

$V_{C2} = V_{C1} + V_{L1} + V_{D6}$

V_{C1} remains charged and considered as a constant value due to the value of I_{C1} is approximately zero, then the value of $\frac{dV_{C1}}{dt}$ would be very small.

$I_{L1} = I_0 . \cos(w_r t)$

$w_p = 2\pi f_p \approx 9.5$ M rad/sec.

(I_0) is approximately 0.5 Amp. For the ideal conditions, the internal capacitance of diodes is zero; therefore, the parasitic resonance and I_0 can be considered as zero ampere.

The 2nd, 3rd and 4th modes are repeating themselves every ON/OFF pulse with frequency switching of SW_2. figure 3.6, shows the zoom of $V_{C1}, V_{C2}, V_{L1}\&V_{D6}$ waveforms in the 2nd, 3rd and 4th modes.

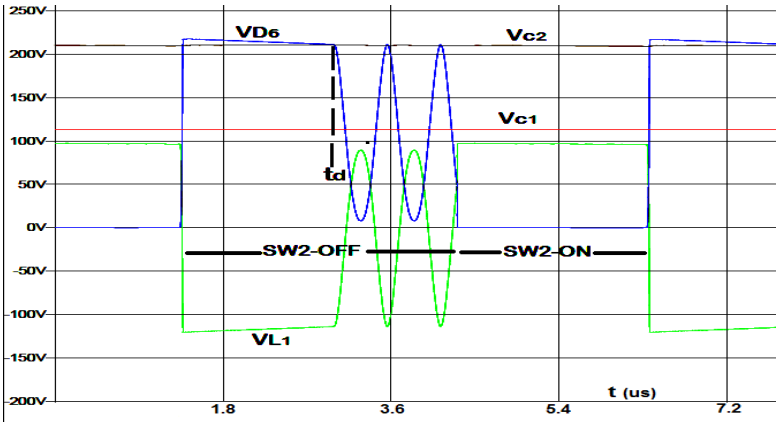


Figure 3.6: The zoom of $V_{C1}, V_{C2}, V_{L1}\&V_{D6}$ with SW_2 pulses

The figure 3.7, shows the full picture of $(V_{C1}), (V_{C2}), (V_{L1})\&(V_{D6})$ waveforms. V_{C1} is in red color, V_{C2} is in brown color, V_{L1} is in green color, and V_{D6} is in blue color.

5. Fifth mode: For the time period $t_2 \leq t < t_3$, when SW_1 is ON and SW_2 is ON/OFF. (t_3) is the moment when SW_1 turns OFF. The circuit shown in figure 3.4d, illustrates the active path of current at this mode. Even when SW_2 is ON, FWD is revers biased.

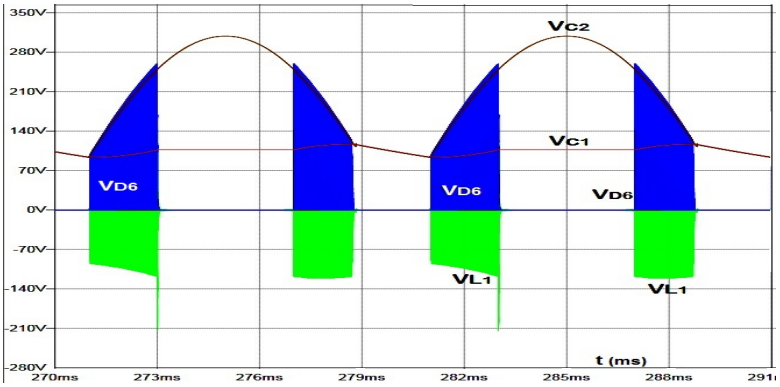


Figure 3.7: $V_{C1}, V_{C2}, V_{L1}\&V_{D6}$ waveforms

Due to $V_S > V_{C1}$; therefore, (C_1) and (L_1) are considered as disconnected (open circuit), because they are reverse biased when SW_1 is OFF and then (D_6) and FWD diodes are OFF.

Therefore, (C_1) and (L_1) are neither charging nor discharging, then $I_{L1} = I_{C1} =$ Zero, $V_{L1} =$ Zero but V_{C1} is a constant value.

$$V_s = V_{C2} = V_R = V_{out}$$

$$I_s = I_{C2} + I_R$$

$$\therefore I_s = C_2 \frac{dV_{C2}}{dt} + \frac{V_{out}}{R}$$

$$\therefore I_s = C_2 \frac{dV_{C2}}{dt} + \frac{V_{out}}{R}$$

Just (C_2) is charging in this case and the load is fed by the source. Therefore, the input current waveform will be a quit sinusoidal.

6. Sixth mode: For the time period $t_3 \leq t < t_4$, when $(V_s) > (V_{C1})$, SW_1 is ON and SW_2 is ON. (t_4) is the moment when V_{C1} is greater than V_S. The circuit is shown in figure 3.4b.

   At this mode, (C_1), (C_2) and (L_1) are charging and the load is fed by the source. All the derived equations in the 2nd mode are valid for this mode.

7. Seventh mode: For the time period $t_3 \leq t < t_4$, when $(V_S) > (V_{C1})$, SW_1 is OFF and SW_2 is ON until (t_d). The circuit is shown in figure 3.4c.

At this mode, (C_1) and (C_2) are charging while (V_{L1}) is equal to (V_{C1}) until (L_1) fully discharges its current into zero ampere at the time of (t_d).

All the derived equations in the 3rd mode are valid for this mode.

8. Eighth mode: For the time period $t_3 \leq t < t_4$, when $V_s > V_{C1}$, SW_2 is OFF, for period (t_d) until the next ON-pulse for SW_2. The circuit is shown in figure 3.4d.

   At this mode, the inductor current (I_{L1}) supposed to remain zero amp. However, the internal capacitance of the diodes combines with stray inductance can form a resonant circuit called (parasitic resonant). Due to this parasitic resonance, a sinusoidal current can flow into the inductor (L) in a very high frequency (about 1.54 MHz) called self resonant frequency (or parasitic frequency (f_p)).

   V_{C1} remains charged and considered as a constant value due to the value of I_{C1} is approximately zero, then the value of $\frac{dV_{C1}}{dt}$ would be very small.

   $I_{L1} = I_0 . \cos(w_p . t)$

   $w_p = 2\pi f_p \approx 9.5$ M rad/sec.

   (I_0) is equal to approximately (0.5) Amp. For ideal conditions, the internal capacitance of diodes is zero; therefore, the parasitic resonance and (I_0) can considered as zero amp. The 6th, 7th and 8th modes are repeating itself every ON/OFF switching of SW_2.

9. Ninth mode: For the time period $t_4 \leq t < 10$ msec., when $V_{C1} > V_s$. SW_2-ON/OFF and SW_1 is ON, the circuit is shown in figure 3.4a:

   (C_1), (L_1) & (C_2) are discharging while the R-load is fed by the main capacitor (C_1).

   $\therefore I_{L1} = \frac{V_{out}}{R} - C_2 \frac{dV_{C2}}{dt}$

   $V_{C2} = V_R = V_{out} = V_{C1} + V_{L1}$

3.3.1.6 System Parameters

The proposed circuit has been simulated in LT-spice program and the parameters have been specified as the following table 3.1:

Table 3.1: System Parameters

Inductor (L) = 10 µH	$R_{\text{Internal Ser.}}$ = 2.236 m Ω	$R_{\text{Internal Par.}}$ = 1413 Ω
Capacitor (C) = 1 mF	ESR = 0.035 Ω	ESL = 0 Ω
MOSFET	IPP070N8N3, N-channel	V_{ds} = 80 V, R_{ds} = 7m Ω
Freewheeling diode	Schottky, (UPSC600)	$V_{\text{Breakdown}}$ = 600 V
Parallel diode	Schottky, (MBR745)	$V_{\text{Breakdown}}$ = 45 V
Load	Resistive	10 Ω

The specific details and current ratings of the MOSFET has been clarified in the appendix (E).

Continuous drain current of Mosfet (I_D) = 80 Amp.

Pulsed drain current of Mosfet ($I_{D,pulse}$) = 320 Amp.

3.3.1.7 Simulation Results & Assessment

The proposed design is shown as an electrical circuit with V_S = 311 V_{peak} = 220 V_{rms}, L = 10 µH, C_1 = 1 mF, C_2 = (1 µF) and has been designed and investigated using Lt-spice simulink program.

Duty cycle of SW_1 = 60% in two time intervals. The first period is ($0 \leq t < t_2$) = 30% of full period, and the second period is ($t_3 \leq t <$ 10ms.) = 30% of full period. Duty cycle of SW_2 = 40% with switching frequency f_{sw2} = 200 kHz.

1. R-load, The main inductor (L), the duty cycle of SW_1 (D_1), the switching frequency of SW_2 and (D_2) which is the duty cycle of SW_2, are the five main parameters in this circuit which could be changed in different values in order to examine the validity of the proposed circuit and find out the optimum design and values of the parameters in order to get minimum input THD_I,

maximum unity input PF and low output ripple voltage, cost effective, non-bulky, small size converter.

2. The table 3.2, shows the relationship between different load values comparing it with fundamental input current I_1, THD_I, input PF, P_{in}, P_{out}, η and main capacitor voltage (V_{C1}), when L = 10 µH and the duty cycle (D_2) of SW_2 is 40% and V_{out} is 309 V_{peak}.

Table 3.2: Comparison of load with THD_I, PF, η and V_{out}

Load(Ω)	**I-1**(A)	**THD**(%)	**PF**	P_{in}(W)	P_{out}(W)	η(%)	V_{C1}**(V)**
1	211.6	6.8	0.998	46574	44368	95.3	91
10	22.6	14	0.99	4982	4908	98.5	107
20	11.62	21	0.98	2556.5	2514.8	98.3	124
50	4.9	33.2	0.95	1078	1047	97.1	148
100	2.61	43.8	0.916	574.2	543	94.6	165
200	1.55	61.6	0.85	339.4	282.6	83.3	181.8
500	0.74	84	0.76	161.7	119	73.6	200
1000	0.5	110.7	0.67	110	61.5	56	210

Power factor has been calculated by using equation 3.2, mentioned in [160]:

$$PowerFactor = \frac{1}{\sqrt{1 + (THD_I)^2}} \tag{3.2}$$

the values of I_1 & I_h are essential to calculate the total source current of the circuit for each case as shown in equations 3.3 & 3.4:

$$I_h = I_1 \times THD_I \tag{3.3}$$

$$I_t = \sqrt{I_1^2 + I_h^2} \tag{3.4}$$

The input power is almost 5 kW when R-load = 10 Ω and I_1 = 22.6 A, and the output power is more than 4.9 kW, thus the efficiency is more than 98%.

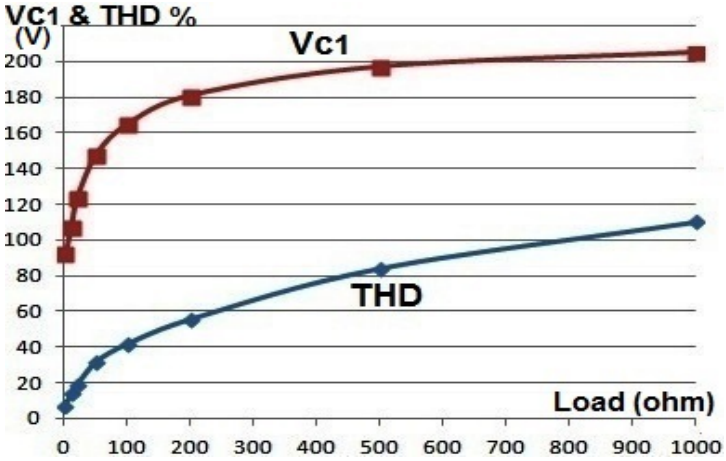


Figure 3.8: Different load values with THD_I and V_{C1}

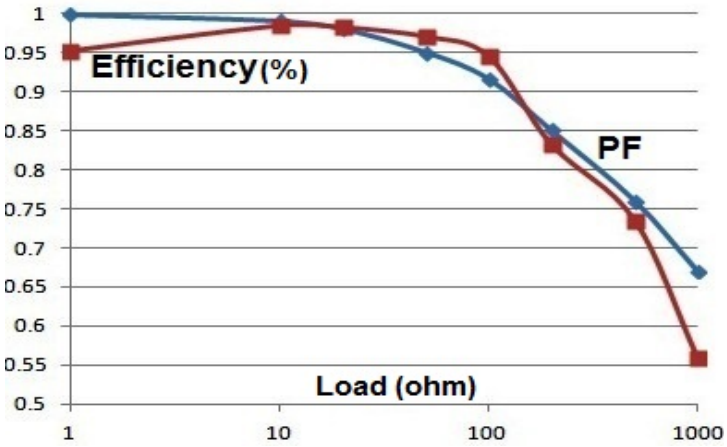


Figure 3.9: Different load values with (η) and PF

It can be concluded from table 3.2, figure 3.8 and figure 3.9 that, the values of THD_I and capacitor voltage (V_{C1}) are approximately exponentially proportional with the resistive load value and inversely with the input power factor and efficiency.

3. Table 3.3, shows the relationship between different inductor values comparing with THD_I, input PF, P_{in}, P_{out}, η and main capacitor's voltage V_{c1}, when R-load = 10 Ω and $D_2 = 40\%$.

Table 3.3: Comparison of (L) with THD_I, PF, η and V_{out}

L(uH)	**I-1**(A)	**THD**(%)	**PF**	P_{in}(W)	P_{out}(W)	η(%)	V_{C1}(V)
0.1	28.5	66.2	0.83	6241	5676	91	231
1	25	40.7	0.926	5498.7	5300.5	96.4	173
10	22.6	14	0.99	4982	4908	98.5	107
20	22.46	12.2	0.992	4938	4871	98.6	95
50	22.4	9.5	0.995	4925.4	4856.3	98.6	95
100	22.3	8.9	0.996	4906	4838	98.6	92.6
200	22.3	8.7	0.996	4905	4843	98.73	89
500	22.2	8.5	0.996	4882	4831	98.95	83.3
1000	22.1	7.5	0.997	4861	4811	98.97	78.8

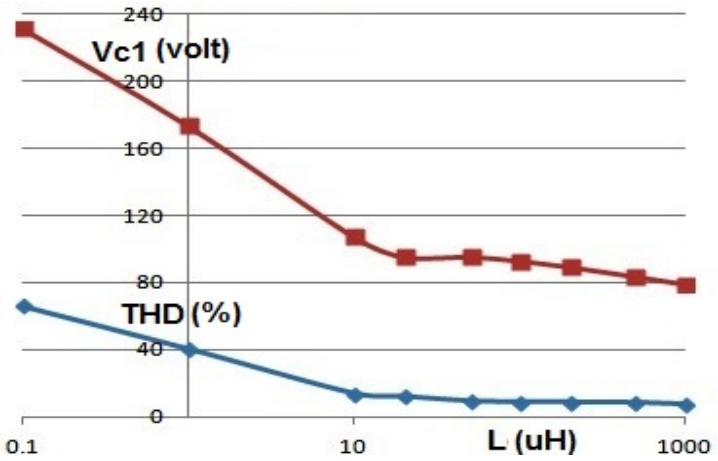


Figure 3.10: Different (L) values with THD_I and V_{C1}

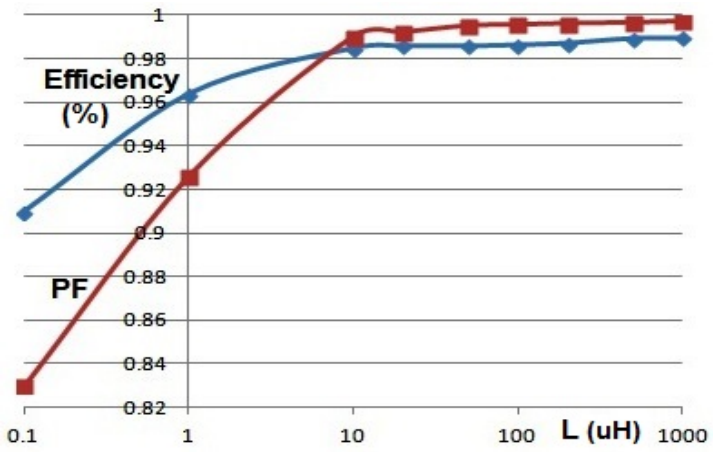


Figure 3.11: Different (L) values with (η) and PF

It can be concluded, from table 3.3, figure 3.10 and figure 3.11, that the value of inductor (L) is approximately exponentially proportional with the input PF and efficiency values and inversely proportional with the values of THD_I and V_{C1}. A value of (L) more than 50 µH, can cause a high V_L due to high f_{sw2} which causes high $\frac{di_L}{dt}$ at the same time, the output voltage ripple will increase with the increasing of (L).

4. Table 3.4, shows the relationship between different duty cycles of SW_2 comparing with THD_I, input PF, P_{in}, P_{out}, η and the main capacitor voltage (V_{C1}), when R-load = 10 Ω.

Table 3.4: Comparison of (D_2) with THD_I, PF, η and V_{out}

D2(%)	**I-1**(A)	**THD**(%)	**PF**	P_{in}(W)	P_{out}(W)	η(%)	V_{C1}(V)
10	21.9	3.8	0.999	4816.7	4773.5	99.1	52
20	22.1	7.2	0.997	4860	4811	99	75.3
30	22.4	10.9	0.994	4927.5	4859	98.6	92.7
40	22.6	14	0.99	4982	4908	98.5	107
50	23	18.6	0.983	5059.3	4975	98.3	121
60	23.7	28.2	0.963	5217	5090	97.6	146
70	24.6	37.7	0.936	5413.7	5231.5	96.6	171
80	26	53.6	0.88	5711	5394.6	94.5	197
90	28.4	67.7	0.83	6262.5	5600.7	89.4	222

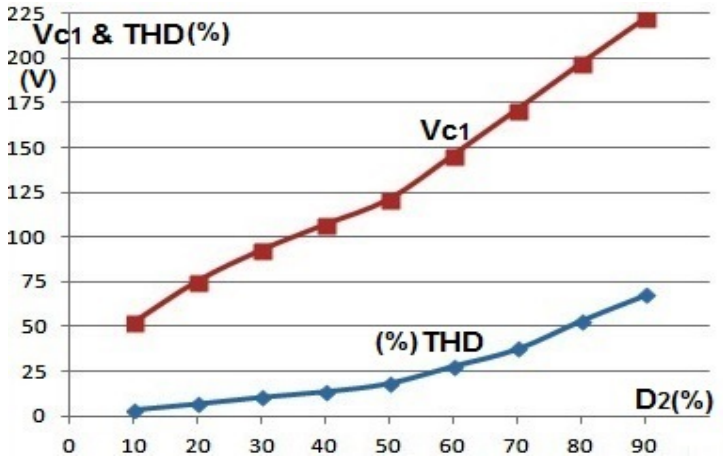


Figure 3.12: Values of duty cycle for SW_2 vs. THD_I & V_{C1}

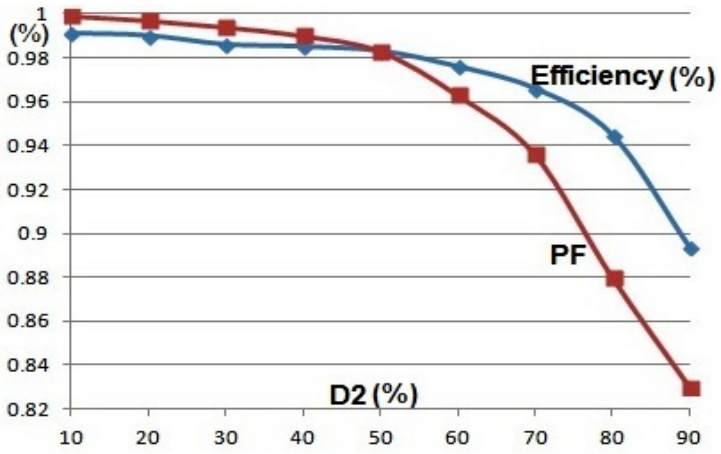


Figure 3.13: Values of duty cycle for SW_2 vs. (η) and PF

It can be concluded from table 3.4, figure 3.12 and figure 3.13 that, the values of THD_I and output voltage V_{C1} are approximately exponentially proportional with the value of (D_2) and inversely with the input power factor and efficiency. It's better to keep the value of (D_2) less than 50% in order to get a unity PF at the input side when (L) is 10 µH and the output power is almost 5 kW.

5. Table 3.5, shows the relationship between different duty cycles of SW_1 with equal off periods ($\frac{D_1}{2}$ at the beginning = $\frac{D_1}{2}$ at the end of each period) from zero to (t_2) and from (t_3) to ($\frac{T}{2}$). These values have been compared with THD_I, input PF, P_{in}, P_{out}, η and V_{C1}, for each case when R-load = 10 Ω and L = 10 µH.

Table 3.5: Comparison of (D_1) with THD_I, PF, η and V_{out}

D1(%)	**I-1**(A)	**THD**(%)	**PF**	P_{in}(W)	P_{out}(W)	η(%)	V_{C1}(V)
10	21.6	0	1	4799.3	4756	99.1	18.4
20	21.8	2.7	0.999	4793	4762	99.3	37.3
30	21.9	5.6	0.998	4816	4779	99.2	57.3
40	22.1	8.4	0.996	4859.6	4808	98.96	73.6
50	22.3	10.9	0.994	4905.4	4854.8	98.96	93.4
60	22.6	14	0.99	4982	4908	98.5	107
70	23	17	0.986	5060.7	4980.7	98.4	121.3
80	23.4	19.2	0.982	5147.7	5059	98.28	134.7
90	23.8	21.3	0.98	5246	5145	98.1	147.7
100	24.3	23	0.97	5321	5226	98.2	160

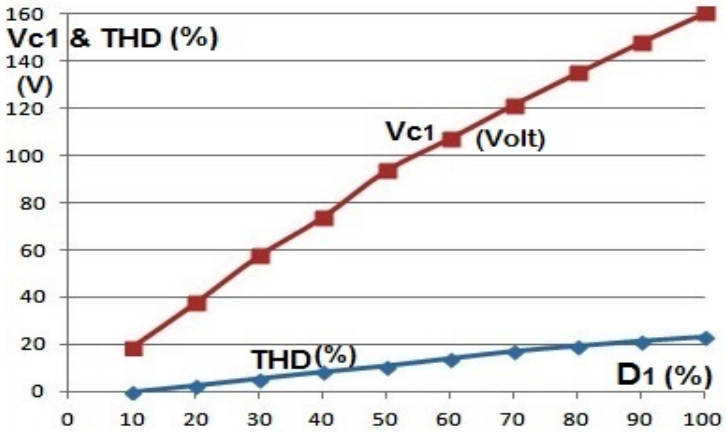


Figure 3.14: Values of duty cycle for SW_1 vs. THD_I and V_{out}

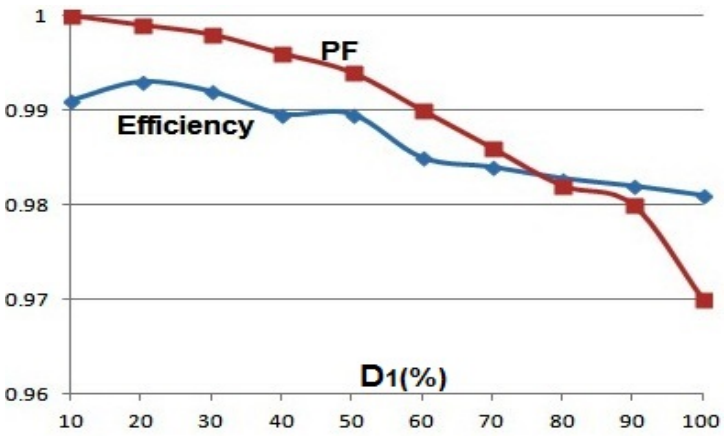


Figure 3.15: Values of duty cycle for SW_1 vs. (η) and PF

Its good to keep the value of (D_1) less than 70% in order to get a unity PF at the input side when (D_2) is 40%, and 4.9 kW output load power.

It can be concluded from table 3.5, figure 3.14 and figure 3.15 that, the values of THD_I and V_{C1} are approximately exponentially proportional with the value of (D_1) and inversely with the input PF and efficiency.

The value of $(t_1 - t_2)$ is increases proportionally with the increasing of duty cycle of SW_1 and the value of THD_I and inversely with the PF values.

6. Table 3.6 shows the relationship between different SW_2 frequencies comparing it with fundamental input current I_1, THD_I, input PF, P_{in}, P_{out}, η and output voltages (V_{C1}), when $R_L = 10\Omega$, L = 10 µH and the duty cycle (D_2) of SW_2 is 40% and $V_{max.}$ is almost 309 V_{peak}.

Table 3.6: Comparison of (f_{SW2}) with THD_I, PF, η and V_{out}

f-sw2(kHz)	**I-1**(A)	**THD**(%)	**PF**	P_{in}(W)	P_{out}(W)	η(%)	V_{C1}(V)
5	27.12	62.5	0.85	5980.5	5587	93.4	209.6
10	26	51.4	0.89	5724	5449.7	95.2	191.5
50	23.6	27.2	0.96	5165.4	5118	99	144
100	23.1	20	0.98	5079	4997.6	98.4	124.4
150	22.82	16.5	0.986	5017	4945	98.56	115
200	22.66	14	0.99	4982	4908	98.5	107
250	22.53	13	0.991	4955	4888.7	98.66	102
300	22.53	12.8	0.992	4957	4885.5	98.55	101.3
350	22.52	12.7	0.992	4954	4880.5	98.5	101
400	22.48	12.3	0.992	4943	4875.7	98.6	100.3
500	22.47	12	0.993	4944	4878.7	98.68	99.2

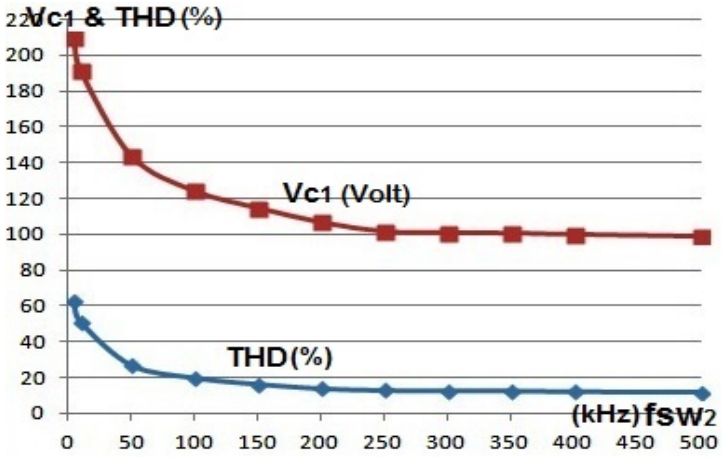


Figure 3.16: Different load values with THD_I and $V_{min.}$

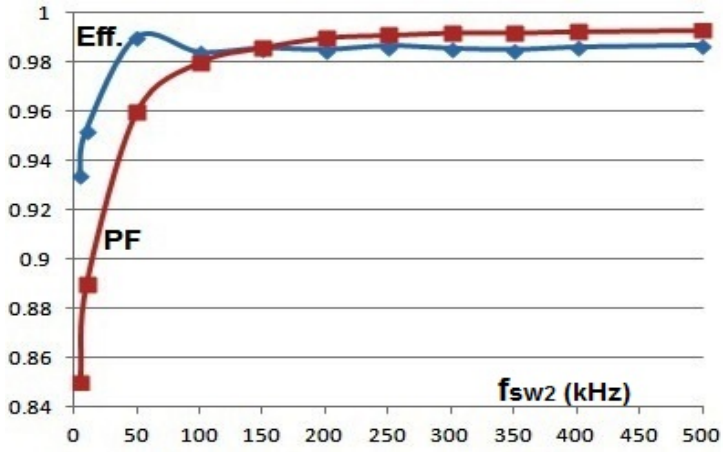


Figure 3.17: Different load values with (η) and PF

It can be concluded, from table 3.6 figure 3.16, and figure 3.17, that the input PF and efficiency are approximately exponentially proportional with the switching frequency of SW_2 and inversely with the values of THD_I and capacitor voltage (V_{C1}). In addition, table 3.6 shows that, the optimum value of f_{SW2} might be more than 50 kHz, in order to get a unity PF at the input side when (L) is 10 µH and approximately 5 kW output power, as the harmonics increase with low switching frequency.

From the aforementioned tables (3.2, 3.3, 3.4, 3.5 & 3.6), it's easy to find out the optimum values of the proposed circuit (including f_{sw2}, D_1, D_2 & L)

when R-load = 10Ω which can achieve (0.99) power factor and minimum magnetics value.

7. Figure 3.18 below shows the input source current waveform (I_S) with the different time modes for each cycle:

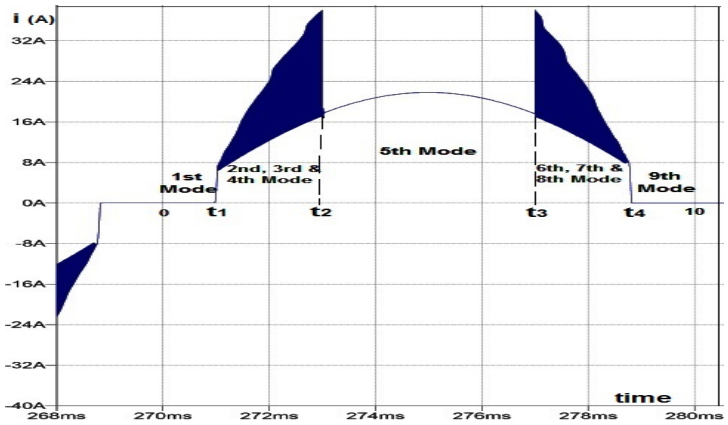


Figure 3.18: The input source current

The FFT spectrum of the source current has been shown in figure 3.19. The total current harmonic distortion (THD_I) is 14%, then the input power factor is almost unity (0.99).The third order harmonic has been eliminated, the 5th and 7th orders are the most predominant orders due to the switching pattern which turns OFF the main capacitor (C_1) from 3 ms. to 7 ms. and the load was fed by the source.

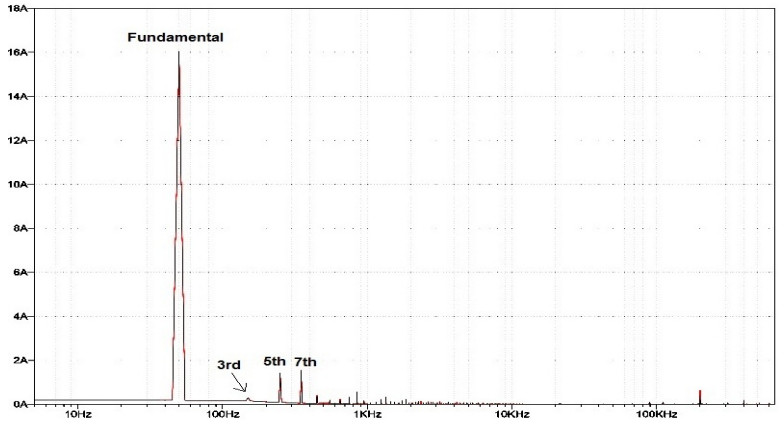


Figure 3.19: FFT Spectrum of the input current

The spikes shown on the waveform of (I_S) reaches up to (2 I_{peak}) and is one of the limitations of this design. However, the effect is restricted because it appears in 50% of each half cycle in two separate periods and not exist at the peak value.

Generally, the effects of these spikes can be summarized as the followings:

(a) Produces high electromagnetic interference (EMI) value and affect other devices, which may requires additional filter on the input side in order to isolate or eliminate the high frequency orders.

(b) Could burn the active switches because of the stress on MOSFETs (V_S+V_L), because ($V_L = L\frac{di}{dt}$), especially with high switching frequency which causes high switching losses in addition.

(c) Sudden changes in MOSFET's current or capacitor's current (I_c) causes variable in the voltage between drain and source (V_{DS}) which may causes an oscillation in the circuit and affect other devices.

8. For time intervals $t_1 \leq t < t_2$ and $t_3 \leq t < t_4$ (which represent the 2nd and 6th modes), the equation of the inductor's voltage is: $V_L = L\frac{di_L}{dt} = \frac{L.di_L.f_{sw2}}{D}$

   (D_2) is the duty cycle of SW_2 and because of the switching frequency of SW_2 (f_{sw2}) is (200 kHz); therefore, V_L would be a very large value at this moment. Consequently, V_L may be reason of huge spikes on SW_1's terminals and may burn the switch. However, the value of V_L can kept small and less than the rated voltage because (L) value is very small (10 µH) and thats will decrease inductor voltage tremendously.

9. For whatever reason, if the designer needs to use a high value of (L) then the value of V_L would be high again with the presence of high frequency switching of SW_2 because of the high change in $\frac{di}{dt}$.

   For this situation, a snubber circuit could be proposed as a solution to suppress the high frequency spikes and to protect the MOSFET switch.

However in this circuit, the main capacitor (C_1) would act as a snubber circuit because of the existence of the freewheeling diode (FWD), which make V_{C1} charge in the negative value of V_L and prevent high voltage on th SW_1 when its in open status.

10. The waveform of the main capacitor's voltage (V_{C1}) looks concave when its charging when $t_1 < t \leq t_2$ while it looks convex shape when $t_3 < t \leq t_4$.

    The interpretation for this phenomenon is as follows:

    $\because I_{C1} = C_1 \frac{dV_{C1}}{dt} \quad \Rightarrow \quad \therefore V_{C1} = \frac{1}{C_1} \int I_{C1}(t)dt$

    The original waveform of $I_{C1}(t)$ is a sine wave:

    $I_{C1}(t) = I_{C1} \sin(wt)$

    $V_{C1} = \frac{1}{C_1} \int I_{C1}(t)dt$

    For: $t_1 < t \leq t_2$

$$V_{C1} = \frac{1}{C_1} \int_{\frac{180t_1}{0.01}}^{\frac{180t_2}{0.01}} I_{C1}(t)dt$$

$$V_{C1} = \frac{I_{C1}}{C_1} \int_{\frac{180t_1}{0.01}}^{\frac{180t_2}{0.01}} \sin(wt)dwt$$

$$V_{C1} = \frac{I_{C1}}{C_1} \big[-\cos(wt) \big] \Big|_{\frac{180t_1}{0.01}}^{\frac{180t_2}{0.01}}$$

    The waveform is a concave shape at this time period.

    For: $t_3 < t \leq t_4$

$$V_{C1} = \frac{1}{C_1} \int_{\frac{180t_3}{0.01}}^{\frac{180t_4}{0.01}} I_{C1}(t)dt$$

$$V_{C1} = \frac{I_{C1}}{C_1} \int_{\frac{180t_3}{0.01}}^{\frac{180t_4}{0.01}} \sin(wt)dwt$$

$$V_{C1} = \frac{I_{C1}}{C_1}\big[-\cos(wt)\big]\Big|_{\frac{180t_3}{0.01}}^{\frac{180t_4}{0.01}}$$

The waveform is in a convex shape at this period.

Obviously, the integral of different phase angles results in a different part of the (-cos) waveform shape and that's explain the reason of being V_{C1} in different wave shapes in these two periods in spite of they both represent the charge period for C_1.

The same interpretation is valid for the shape of V_L waveform because C_1 and L in series so I_{C1} is equal to I_L.

$I_{C1}(t) = I_L(t) = I_{C1}\sin(wt)$

$V_L(t) = L.\frac{di_L}{dt} = L.I_{C1}\cos(wt)$

The output load voltage V_{out} is shown in figure 3.20.

V_{out} which is V_{C2} swings between $V_{max.}$ and $V_{min.}$.

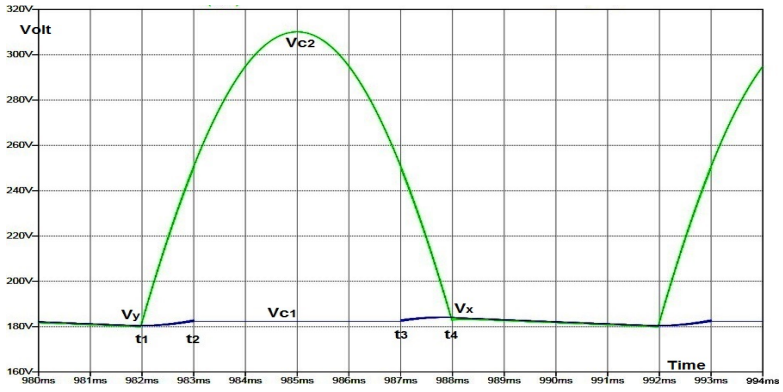


Figure 3.20: Output Voltage V_{C2} and V_{C1} waveforms

V_x which is the higher value of the minimum output voltage is corresponds with t_4, while V_y which is the lower value of the minimum output voltage is corresponds with t_1. The length of the slope line $(V_x - V_y)$ changes with the value of D_2 as seen in the simulation's result.

11. The inductor's current (I_L) in 4th and 8th modes is in discontinuous conduction mode (because of the parasitic resonance) which could causes high

reverse inductor voltage (V_L) because of the very high $\frac{di}{dt}$. However, as shown in figure 3.21, the (V_L) does not increases more than 140 V_{P-P} in spite of that the source voltage is $311V_{P-P}$, because of the small value of (L).

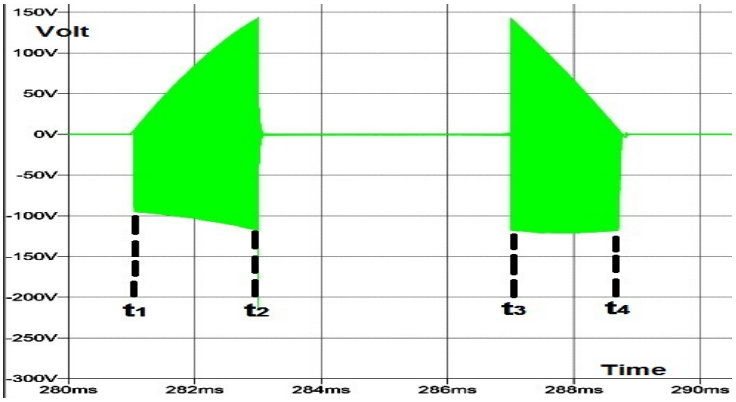


Figure 3.21: The waveform of V_L

12. Figure 3.22, shows the inductor current (I_L), which is at the same time, the capacitor current (I_{C1}) (because (L) is connected in series with C_1) with the pulses of SW_1 when $V_S = 220\ V_{rms}$, R-load = 10 Ω. The power delivered to the load is about 5 kW, $THD_I = 14\%$ and input PF = 0.99.

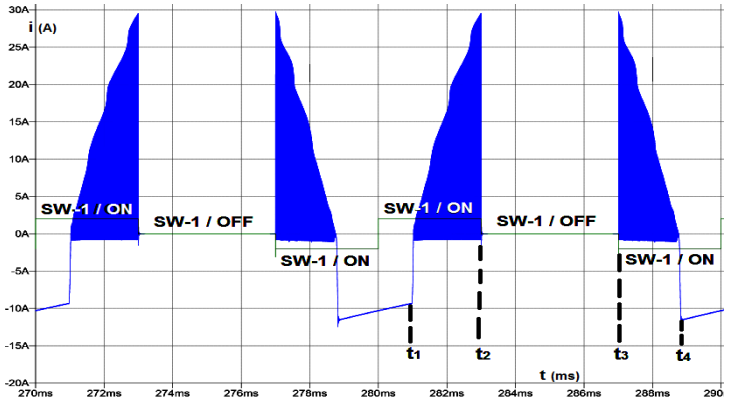


Figure 3.22: I_L with SW_1 pulses

13. Other important aspect to be investigated in this circuit, is the size of the inductor. The required value of the inductance for the same voltage and power ratings in the three level boost converter is (L), while the size would be doubled with the using of two inductors (2x2L) for the interleaved boost

converter and the inductance would be doubled again (4L) for the conventional boost converter [161].

The inductor's value used in the literature in [155] for 3 kW output power and 100 kHz switching frequency using interleaved boost converter was (270 µH), while the value of inductor (L) in the newly proposed circuit is (10 µH) for the same power which means 98% less than regular boost converter. This reduction of the inductor's value will effectively contribute in reducing the size, weight and the cost of the converter.

14. Usually, DC/DC converters are categorized as buck, boost and buck-boost converters according to the output gain. That's happens because, inductor current (I_L) is related 100% to the supply voltage throughout the waveform. However, this relation can limit the design margin of choosing the components. The current (I_{C1}) is independent in the half of the time period of each cycle, this attribute can gives the designer a big tolerance to reduce the value of (L) into few micro henres and avoid high V_L values.

15. The main inductor L_1, is acting as a choke or current limiter due to the high negative value of V_{L1} as its in counter direction of capacitor voltage V_{C1}.

    L_1 charges in the time period $t_1 \leq t < t_2$ because $V_s > V_{C1}$. On the other hand, for the time period$t_2 \leq t < t_3$, I_{L1} is zero because L_1 and C_1 are reverse biased (disconnected). While, for the time period $t_3 \leq t < t_4$, L_1 discharges as a positive current because $V_s > V_{C1}$.

    However, for time period $t_4 \leq t < t_1$ of the next period, L_1 discharges as a negative current because $V_{C1} > V_s$ and the R-load would be fed by I_{L1} which is the same capacitor's current ($I_{C1} = I_{L1}$).

    It is required to separate all the operation modes into their time intervals, in order to understand the full function of (I_{L1}). Full time period (T) for output waveform is 10 msec., because the frequency is 100 Hz for full wave bridge rectifier.

$$I_{L1} = \begin{cases} I_R - I_{C2} & 0 < t \leq t_1 \\ & t_1 < t \leq t_2 \\ I_s - I_{C2} - I_R & S_2\text{-ON} < t \leq S_2\text{-OFF} \\ I_{C1} & S_2\text{-OFF} < t \leq t_d \\ I_0 . \cos(w_r t) & t_d < t \leq S_2\text{-ON} \\ \text{Zero} & t_2 < t \leq t_3 \\ & t_3 < t \leq t_4 \\ I_s - I_{C2} - I_R & S_2\text{-ON} < t \leq S_2\text{-OFF} \\ I_{C1} & S_2\text{-OFF} < t \leq t_d \\ I_0 . \cos(w_r t) & t_d < t \leq S_2\text{-ON} \\ I_R - I_{C2} & t_4 < t \leq 10 \end{cases}$$

The same process might be applied on V_{C1} and V_{out} which are the voltages of C_1 and C_2 respectively, in order to fully understand the performance of the circuit.

$$V_{C1} = \begin{cases} V_{C2} - V_{L1} & 0 < t \leq t_1 \\ & t_1 < t \leq t_2 \\ V_{C2} - V_{L1} & S_2\text{-ON} < t \leq S_2\text{-OFF} \\ V_{C2} + V_{L1} - V_{D6} & S_2\text{-OFF} < t \leq t_d \\ V_{C2} - V_{L1} - V_{D6} & t_d < t \leq S_2\text{-ON} \\ \text{Constant value} & t_2 < t \leq t_3 \\ & t_3 < t \leq t_4 \\ V_{C2} - V_{L1} & S_2\text{-ON} < t \leq S_2\text{-OFF} \\ V_{C2} + V_{L1} - V_{D6} & S_2\text{-OFF} < t \leq t_d \\ V_{C2} - V_{L1} - V_{D6} & t_d < t \leq S_2\text{-ON} \\ V_{C2} - V_{L1} & t_4 < t \leq 10 \end{cases}$$

$$V_{C2} = \begin{cases} V_{C1} + V_{L1} & 0 < t \leq t_1 \\ & t_1 < t \leq t_2 \\ V_{C1} + V_{L1} & S_2\text{-ON} < t \leq S_2\text{-OFF} \\ V_{C1} - V_{L1} + V_{D6} & S_2\text{-OFF} < t \leq t_d \\ V_{C1} + V_{L1} + V_{D6} & t_d < t \leq S_2\text{-ON} \\ V_s & t_2 < t \leq t_3 \\ & t_3 < t \leq t_4 \\ V_{C1} + V_{L1} & S_2\text{-ON} < t \leq S_2\text{-OFF} \\ V_{C1} - V_{L1} + V_{D6} & S_2\text{-OFF} < t \leq t_d \\ V_{C1} + V_{L1} + V_{D6} & t_d < t \leq S_2\text{-ON} \\ V_{C1} + V_{L1} & t_4 < t \leq 10 \end{cases}$$

The piecewise equations above illustrate the relationship between inductor

current (I_{L1}), capacitor voltage (V_{C1}) and output voltage (V_{C2}) with the different parameters of the circuit which can change the design of the circuit according to the desired results.

3.3.1.8 Conclusion of Double Switches Method

According to the simulation's results, the newly proposed PFC circuit was able to reduce the THD_I to 14% with approximately unity power factor at the input side. The topology of reducing the conduction time of the main capacitor C_1 via dividing the waveform into three regions ON-OFF-ON, can improve the power factor and reduce the THD_I at the input side.

In addition, preventing C_1 from work in the middle of the time period for about half of the time will eliminate the third order harmonic and shift the harmonics current to the high-frequency region and that's will contribute in reducing the size of magnetics due to the small value of the inductor 10 µH which produces a small amount of losses. Accordingly, the small inductor will effectively reduce the size and weight, so the rectifier is not bulky any more, and reduce the cost of the converter.

Furthermore, the snubber circuit is not compulsory for this design, because of the presence of freewheeling diode. In addition, the design is considered as a high efficient design due to minimum number and small values of components and simple circuit design because its not require an external complex control circuit.

The performance of this circuit has flexibility because the output ripple voltage and the input power factor can be improved via controlling the values of duty cycles of SW_1&SW_2, L_1 and C_1.

From graphical waveforms and tables analysis for different values of R-load, L_1 and Duty cycle of SW_2, it can be concluded that the increasing of inductor value (L_1) and R-load value is required in order to get a constant unity power factor, small THD_I and low output ripple voltage.

The advantages of this design:

1. The main contribution of this project is the reduction of the inductor's value of PFC circuit more than 98% in comparison with the conventional boost converter.
2. A new method to eliminate third order harmonic current from the input source side which decreases the value of THD_I into 14% and improves the input PF into 0.99 .
3. A good solution for medium and high power (0.5 - 5) kW. However, less power ratings decreases the PF and efficiency of the circuit.
4. The simplicity of the design, because it doesn't require an external control circuit and don't need a snubber circuit.
5. The flexibility of changing the output ripple voltage value (in wide range of voltage).
6. The low losses and high power conversion efficiency (minimum 95%).
7. The small size, light weight and low cost.

The limitations of this design:

1. High spikes on the waveform of (I_S) reaches to (2 I_{peak}). However, considered as limited effect because it appears in 60% of the first half in two separate periods and not exist at the peak value.
2. Two active switches with 200 kHz has been used which increase the switching losses and the initial cost.
3. The ripple of output waveform is high (34%), which results in poor regulated voltage.
4. The capacitor value (1mF) considered as high value for low power ratings.

3.3.2 Using Single Switch APFC

This section presents a modified design of active power factor correction (APFC) circuit inspired from the first methodology. However, it reduces the number of active switches into one and decreases the switching frequency into 20 kHz. The proposed circuit provides almost a unity input power factor (PF) which contributes significantly to a reduction of the THD_I as it eliminates the third harmonic component effectively from the input current.

The most important attribute of this circuit is the small size and numbers of components (one switch, small size (L & C) and a diode), which have been designed to get a unity PF at the AC source side. Therefore, the new circuit is cheaper, smaller size and lighter than other conventional PFC circuits.

In addition, the newly proposed circuit is a snubber-less and uses reasonably low switching frequency which reduces switching losses and increases efficiency. The circuit has been designed and simulated using Lt-spice Simulink program.

3.3.2.1 Circuit's Description

The schematic circuit of the newly proposed PFC circuit is shown below in figure 3.23.

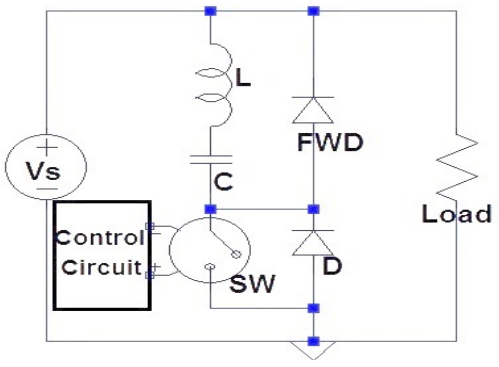


Figure 3.23: Single Switch APFC Circuit

The voltage source (V_S), is the input DC source (represents an AC single-phase

connected to a full wave bridge rectifier), connected in parallel with a LC resonant branch and a MOSFET switch (SW) in parallel with the load. A control circuit has been designed in order to control the switching process.

3.3.2.2 Operation Topology

The newly proposed circuit has the ability to control the working period of the capacitor. Consequently, the value of the input power factor, THD_I of the source current waveform and the ripple value of the (V_{out}) can be controlled as well through using one switching components.

The main idea of this design is depending on the distributing of the working time periods of the capacitor into two intervals, at the beginning (0 - t_1) and at the end ($t_4 - \pi$) via using control circuit. This smart switching pattern would eliminate the third order harmonic component and improves the input PF as the 3rd order is the most significant component in single-phase systems.

This design uses a minimum number of components, and minimum values of L & C as capacitor turned off in the middle of each cycle. This pattern may move the harmonics orders to higher frequencies. Accordingly, decreases the size and the cost of the newly proposed circuit.

This circuit is a snubber-less circuit because the freewheeling diode (FWD) presents an alternative path for the discharge current of inductor (I_L), so can the capacitor keep charged. Consequently, (FWD) may avoid the negative part of I_L and assists the capacitor to act as a snubber circuit. Then (C) can prevent the inductor's voltage (V_L) to increase more than rated value of the source voltage. In this way, (C) will protect the MOSFET switch from being burned to the effect of the high voltage spikes which may happen without the FWD.

3.3.2.3 Control Circuit

A simple designed control circuit as shown in figure 3.24, has been investigated in order to derive the active MOSFET switch and control the switching frequency and duty cycle.

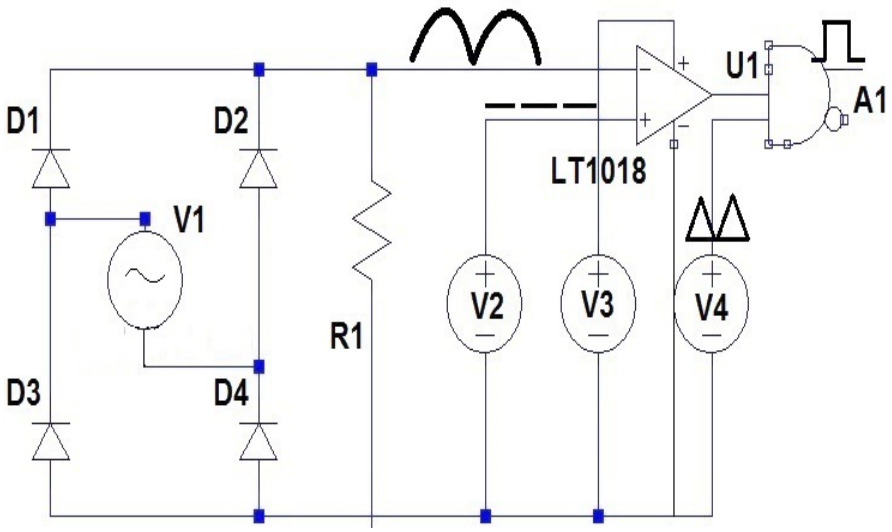


Figure 3.24: Control circuit

V_1 : is 10 volt AC source.

V_2 : is 9 volt DC supply.

V_3 : is 8 volt DC supply.

V_4 : is 9 volt triangle wave generator, f_{sw} = 20 kHz.

Briefly, the circuit consists of a dual input comparator which compares two signals (the first signal is the output of full wave rectifier and the second is a dc voltage source). The output of the comparator, which is a square wave, would be combined in a logic (and gate) circuit with a triangular wave of 20 kHz frequency. The output of and gate will go directly to the gate of the MOSFET.

3.3.2.4 Operation Stages

1. First mode: This mode describes the time period $0 \leq t < t_1$, when $V_C > V_S$. SW is ON/OFF, while t_1 is the moment when V_S is equal or bigger than V_C. (C & L) are discharging and feed the load.

   $I_C = C\frac{dV_C}{dt} = I_L = I_{Load} = \frac{V_{out}}{R}$

   because (L) & (C) and the load are series in this mode.

   $\therefore V_{Load} = V_{out} = V_C + V_L$

   $\because V_L = L\frac{di_L}{dt}$, then the value of V_L is approximately zero because the value of L_1 is very small (few micro henres). $\therefore V_{out} \approx V_C$.

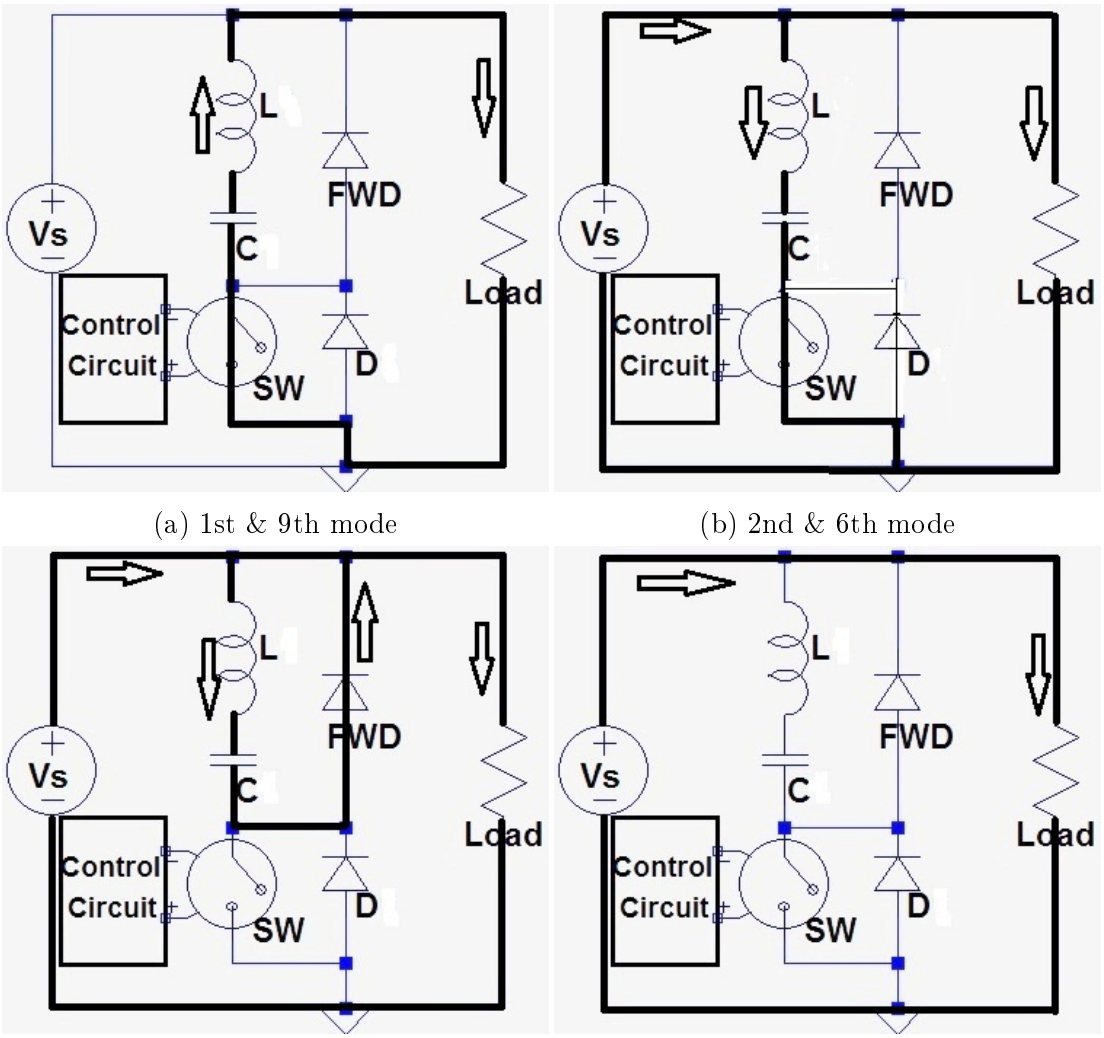
   The circuit shown in figure 3.25a, illustrates the path of the current at this mode:

2. Second mode: For the time period $t_1 \leq t < t_2$, when $V_S > V_{C1}$, and (SW) is ON. t_2, is the moment when the pulses turn off. The circuit shown above in figure 3.25b, the bold line illustrates the active path in this mode.

   In this mode, the load, (C) & (L) are all connected to the source and charging with frequency pulses (20 kHz), as a result, high values and short time current spikes appear on the input current waveform because of the capacitor current. $V_S = V_{Load} = V_{out}$

   $V_S = V_C + V_L = V_C + L.\frac{di_L}{dt}$

   $I_S = I_C + I_{Load} = C.\frac{dV_C}{dt} + I_{Load}$



(a) 1st & 9th mode

(b) 2nd & 6th mode

(c) 3rd & 7th mode

(d) 4th, 5th & 8th mode

Figure 3.25: Circuit diagram in different time modes

3. Third mode: For the time period $t_1 \leq t < t_2$, when $V_S > V_{C1}$. This mode covers the interval time from switching OFF moment until (t_d) ms. (t_d) is the moment when I_L or I_C discharge to a small value swinging around zero ampere on each pulse. The circuit is shown above in figure 3.25c.

   At this mode, (L) discharges its current to (C) until being zero (at the (t_d) moment), while the inductor voltage (V_L) is equal to (V_C) and remains charged. This topology dose not require a snubber circuit as (V_L) has been prevented.

$\because V_L = V_C \quad \& \quad I_L = I_C = C\frac{dV_C}{dt} \quad \therefore X_L = X_C$

$2\pi fL = \frac{1}{2\pi fC} \quad \therefore f_r = \frac{1}{2\pi\sqrt{LC}} = 1.59kHz$

(f_r) is the resonance frequency.

At this mode, the load is fed by the source.

$V_L = L\frac{di_L}{dt} = V_C$

$I_S = I_{Load} = \frac{V_{out}}{R}$

4. Fourth mode: For the time period $t_1 \leq t < t_2$, when $V_S > V_C$, SW is OFF (from (t_d) until the next ON-pulse). The bold line in the circuit shown above in figure 3.25d, clarifies the source current's path.

   At this mode, the inductor current (I_L) supposed to remain zero amp. However, the internal capacitance of the diodes combines with stray inductance which form resonant circuit called parasitic resonant. Due to this parasitic resonance, a sinusoidal current can flow into the inductor (L) in a very high frequency (about 1.54 MHz) called self resonant (or parasitic) frequency (f_p). At the same time, V_L follows I_L waveform and oscillate around zero. as shown in figure 3.26:

Figure 3.26: I_L & I_S in the 2nd, 3rd & 4th modes

(V_C) remains charged and considered as a constant value due to the value of (I_C) which is approximately zero, then the value of $\frac{dV_C}{dt}$ is very small value.

$I_L = I_0.\cos(w_p.t)$

$w_p = 2\pi f_p \approx 9.5$ M rad/sec.

(I_0) is 0.5 Amp. For ideal conditions, the internal capacitance of diodes is zero; therefore, the parasitic resonance and (I_0) can considered as zero amp.

5. Fifth mode: For the time period $t_2 \leq t < t_3$, when pulses are ON/OFF. t_3 is the moment when SW turns OFF. The circuit shown in figure 3.25d, illustrates the active path of current at this mode:

   Due to $V_S > V_C$; therefore, (C) and (L) are considered as disconnected (open circuit), because they are reverse biased when SW is OFF and and FWD is reverse biased.

   Therefore, C and L are neither charging nor discharging, then $I_L = I_C =$ Zero, $V_L =$ Zero but V_C is a constant value.

6. Sixth mode: For the time period $t_3 \leq t < t_4$, when $V_S > V_C$, SW is ON. t_4 is the moment when V_C is greater than V_S. The circuit is shown in figure 3.25b.

   At this mode, (C) and (L) are charging and the load is fed by the source. All the derived equations in the 2nd mode are valid for this mode.

7. Seventh mode: For the time period $t_3 \leq t < t_4$, when $V_S > V_C$. The circuit is shown in figure 3.25c.

   At this mode, (C) is charging while V_L is equal to V_C until (L) discharges its current until reaches small value (0.5) ampere at the time of (t_d) and remains oscillating around zero.

   All the derived equations in the 3rd mode are valid for this mode.

8. Eighth mode: For the time period $t_3 \leq t < t_4$, when $V_S > V_{C1}$, SW is OFF, for period (t_d) until the next ON-pulse for SW_2. The circuit is shown in figure 3.25d.

(V_C) remains charged and slightly charging but approximately constant due to very small $\frac{dV_C}{dt}$.

V_{C1} remains charged and considered as a constant value due to the value of I_{C1} is approximately zero, then the value of $\frac{dV_{C1}}{dt}$ would be very small.

$I_{L1} = I_0.\cos(w_p.t)$

$w_p = 2\pi f_p \approx 9.5$ M rad/sec.

The modes (6,7,8) repeat themselves every ON/OFF pulse of the MOSFET switching.

9. Ninth mode: For the time period $t_4 \leq t < 10$ ms., when $V_C > V_S$. SW-ON/OFF, the circuit is shown above in figure 3.25a.

   (L) & (C) are discharging while the R-load is fed by the main capacitor.

   $\therefore I_L = \frac{V_{out}}{R}$

   $V_{Load} = V_{out} = V_C + V_L$

   All the derived equations in the first mode are valid for this mode.

3.3.2.5 System Parameters

The proposed circuit has been simulated in LT-spice program and the parameters have been specified as the following table (3.7):

Table 3.7: System Parameters

Inductor (L) = 10 µH	$R_{\text{Internal Ser.}} = 2.236$ m Ω	$R_{\text{Internal Par.}} = 1413$ Ω
Capacitor (C) = 0.5 mF	ESR = 0.035 Ω	ESL = 0 Ω
MOSFET	IPP070N8N3, N-channel	$V_{ds} = 80$ V, $R_{ds} = 7$m Ω
Freewheeling diode	Schottky, (UPSC600)	$V_{\text{Breakdown}} = 600$ V
Parallel diode	Schottky, (MBR745)	$V_{\text{Breakdown}} = 45$ V
Load	Resistive	20 Ω

3.3.2.6 Simulation Results & Assessment

An electrical circuit with $V_S = 311$ $V_{peak} = 220$ V_{rms}, L = 20 µH, C = 0.5 mF and MOSFET switch works in f_{sw} = 20 kHz controlled by a control circuit, has been designed and investigated by using Lt-spice Simulink program.

1. R-load, inductor (L) and switching frequency of the MOSFET, are three main parameters in this circuit which could be changed in different values in order to find out the optimum design and parameters values in order to get low input THD_I, unity input PF, high efficiency, cheap, not bulky, small size and light converter.

2. Table 3.8 shows the relationship between different load values comparing it with fundamental input current P_{in}, P_{out}, η, THD_I and input PF when L = 20 µH and the switching frequency (f_{sw}) is 20 kHz.

Table 3.8: Comparison of load with THD_I, PF, η and V_{out}

Load(Ω)	**I-1**(A)	**THD-I**	**PF**	P_{in}(W)	P_{out}(W)	η(%)	V_{C1}(V)
1	210.6	5	0.999	46354.5	44260	95.48	67.6
10	22.35	11.6	0.994	4920.27	4851.5	98.6	96
20	11.4	17	0.986	2506.1	2473	98.68	111
50	4.72	28.4	0.96	1038	1021	98.36	134
100	2.47	37	0.938	543.48	525	96.6	150
200	1.33	52.4	0.886	292.68	269.6	92.1	166
500	0.64	83.2	0.77	141	110.75	78.55	185
1000	0.41	111.7	0.667	90.2	56.1	62.2	195

Power factor has been calculated by using equation in [160], P.F = $\frac{1}{\sqrt{1+(THD_I)^2}}$

$$I_t = \sqrt{I_1^2 + I_h^2}$$

The total input power, has been calculated via below equation:

$$P_{in} = V_t \times I_t \times PF$$

The maximum efficiency is 98.68% when input power is 2.5 kW when R-load = 20 Ω and (L) is 20 µH.

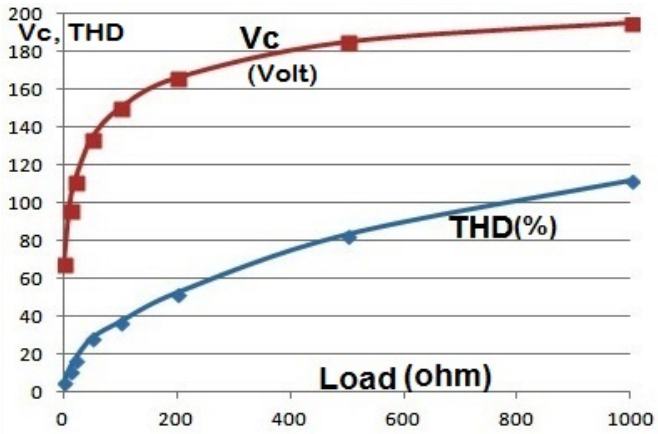


Figure 3.27: Different load values with THD_I and V_c

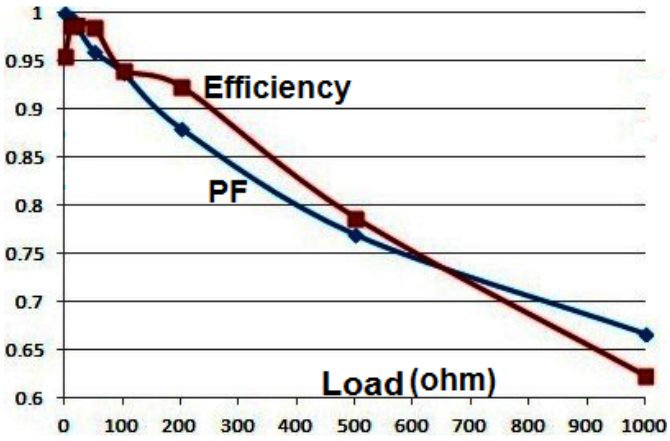


Figure 3.28: Different load values with PF and η

It can be concluded, from table 3.8, figure 3.27 and figure 3.28 that the values of THD_I and capacitor voltage (V_{C1}) are approximately exponentially proportional with the resistive load value and inversely with the input power factor and efficiency.

3. Table 3.9 shows the relationship between different inductor values comparing with with P_{in}, P_{out}, η and input PF, when R-load = 20 Ω and f_{sw} = 20 kHz.

Table 3.9: Comparison of (L) values with THD_I, PF, η and V_{out}

L(uH)	**I-1**(A)	**THD-I**	**PF**	P_{in}(W)	P_{out}(W)	η(%)	V_{C1}(V)
1	12.98	55	0.876	2854.9	2679.4	93.86	173
10	11.63	24	0.972	2557.5	2510	98.1	107
20	11.4	17	0.986	2508.3	2473	98.6	95
50	11.17	10.5	0.994	2456	2434	99.1	95
100	11.07	7.2	0.997	2434.38	2415.5	99.2	92.6
200	11	4.9	0.999	2420.48	2403.7	99.3	89
500	10.97	3.5	0.999	2412	2395	99.3	83.3
1000	10.95	2.5	0.999	2407.3	2391.8	99.36	78.8

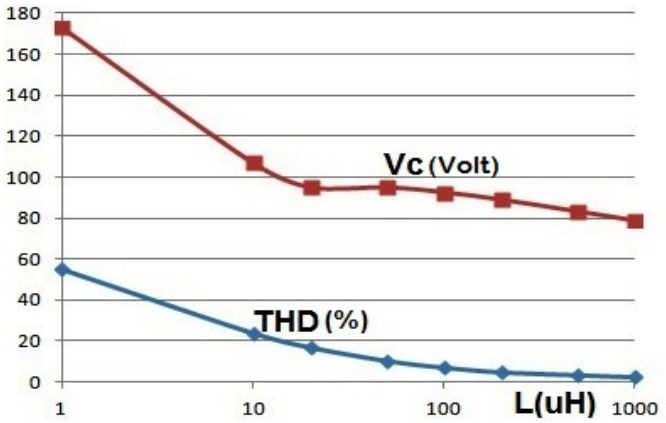


Figure 3.29: Different (L) values with THD_I and V_c

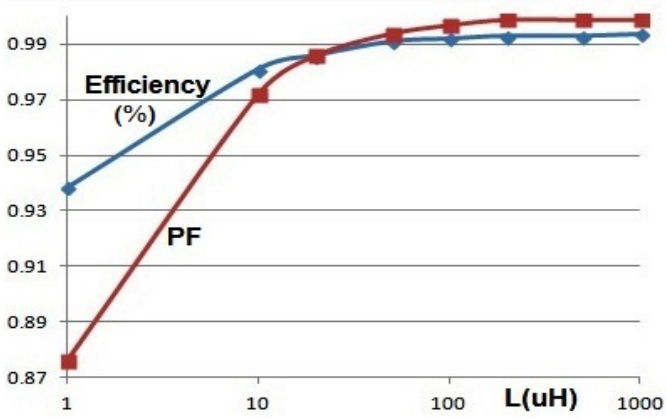


Figure 3.30: Different (L) values with PF and η

It can be concluded, from table 3.9, figure 3.29 and figure 3.30, that the value of inductor (L) is approximately exponentially proportional with the input PF and efficiency values and inversely proportional with the values of THD_I and V_{C1}.

4. Table 3.10 shows the relationship between different switching frequencies of MOSFET comparing with P_{in}, P_{out}, η and input PF when R-load = 20 Ω and (L) is 20 µH.

Table 3.10: Comparison of (f_{sw}) values with THD_I, PF, η and V_{out}

fsw(kHz)	**I-1**(A)	**THD-I**	**PF**	P_{in}(W)	P_{out}(W)	η(%)	V_{C1}(V)
5	12	33	0.95	2641	2574.8	97.5	150
10	11.64	23.8	0.973	2561	2515	98.2	131
20	11.4	17	0.986	2506	2473	98.6	111
50	11.17	10.6	0.994	2456.3	2434.2	99.1	90
100	11.08	7.6	0.997	2437.3	2415.8	99.1	76
200	11	5.6	0.998	2418.9	2405	99.4	64
500	10.98	3.9	0.999	2415	2397.2	99.2	51
1000	10.98	3.7	0.999	2414.8	2396.2	99.2	49

It can be concluded from table 3.10, figure 3.31 and figure 3.32 that, the values of η and PF are approximately exponentially proportional with the value of f_{sw} and inversely proportional with the values of THD_I and V_{C1}.

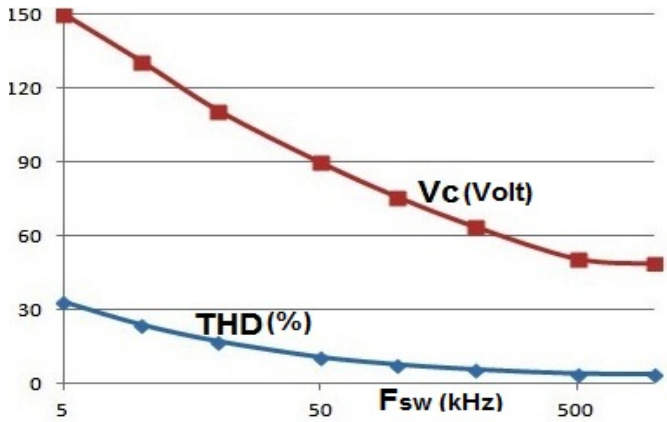


Figure 3.31: Different f_{sw} values with THD_I and V_c

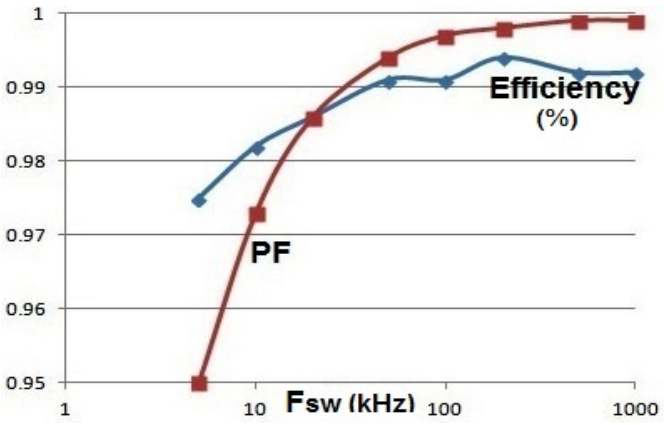


Figure 3.32: Different f_{sw} values with PF and η

It can be concluded that, f_{sw} can be kept around (10 - 20) kHz in order to get approximately unity PF (0.98) at the input AC side when (L) is 20 µH for 2.5 kW output power.

5. The input source current waveform (I_S) is shown below in figure 3.33 with nine time modes:

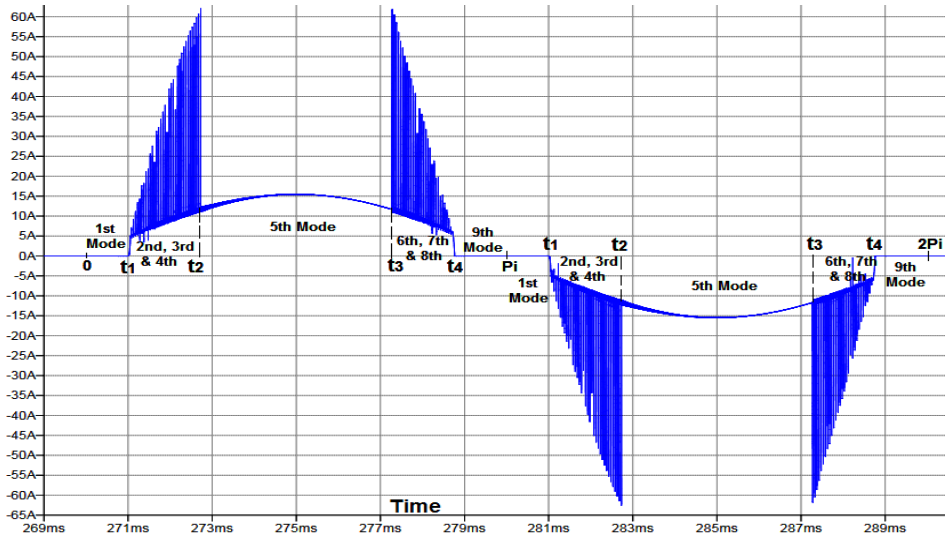


Figure 3.33: The input source current

Figure 3.34, shows the FFT spectrum of the input source current. The total current harmonic distortion (THD_I) is 17%, then the input power factor is almost unity (0.986).

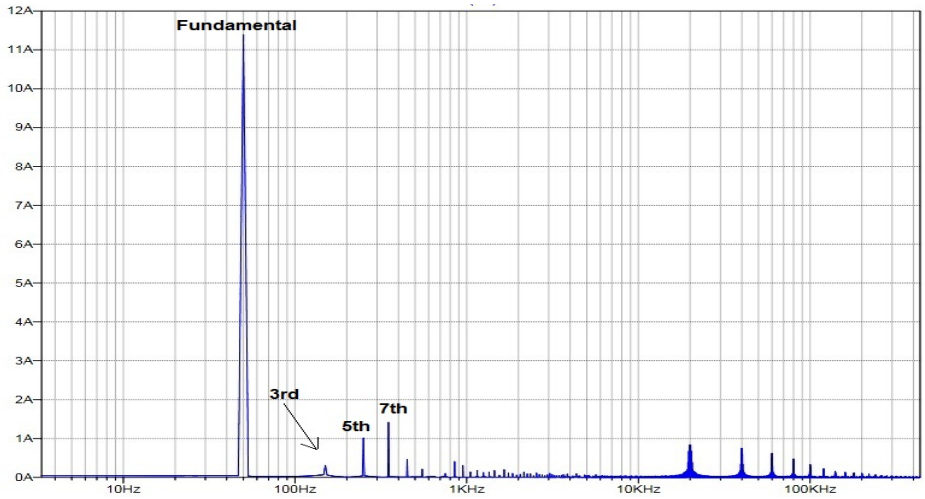


Figure 3.34: FFT Spectrum of the input current

As it is shown in figure 3.34, the third order harmonic does not exist at the input current waveform, and the only harmonic orders shown are the 5th and 7th order harmonics. This is because (C) was OFF at the middle of the waveform $(t_2 - t_3)$ and the load was fed by the source.

6. In the case of the absence of freewheeling diode in the time intervals $t_1 \leq t < t_2$ and $t_3 \leq t < t_4$ (which represent the 2nd and 6th modes), the equation of inductor's voltage is:

   $V_L = L\frac{di_L}{dt} = \frac{L.di_L.f_{sw}}{D}$

   (D), is the duty cycle of (SW) and because of the switching frequency (f_{sw}) is (20 kHz); therefore, V_L would be a very large value at this moment. Consequently, V_L may be a reason for huge spikes on MOSFET's terminals and may burn the switch.

7. Generally, in this situation, a snubber circuit would be proposed as a solution to suppress the high-frequency spikes and to protect the MOSFET switch. However, in this circuit, the main capacitor (C) would act as a snubber circuit because of the existence of the freewheeling diode (FWD), which makes V_C charges on the negative value of V_L and prevent the high voltage

to be applied on the terminals of the MOSFET when its in open status.

8. The required value of the inductance for the same voltage and power ratings in a 3-level boost converter is (L). However, the size would be double with the using of two inductors (2x2L) for the interleaved boost converter, on the other hand, the inductance would be doubled again (4L) for the conventional boost converter [161].

   The inductor's value used in the literature in [155] for a (3 kW) output power using interleaved boost converter was (270 µH), while the value of inductor (L) in the newly proposed circuit is (20 µH) for the same power ratings. This reduction of the inductor's value will effectively contribute in reducing the size, weight and the cost of the converter.

9. One of the significant features of this design is that the inductor's current is not fully related to the value of source voltage as usually happens in PFC circuits, except in the 2nd and 6th mode which covers almost 50% of the waveform according to the design specification. This advantage can be utilized in order to reduce the value of (L) into few micro henrys and avoid high V_L values. Consequently, can reduce the size, weight and the cost effectively.

10. The inductor works like a proper choke or current limiter due to the high negative value of inductor voltage (V_L) as its in counter direction of capacitor voltage (V_C).

    The inductor (L) has been charged in the time period $t_1 \leq t < t_2$ because $V_S > V_C$. On the other hand, for the time period$t_2 \leq t < t_3$, I_L is zero because L and C are reverse biased. While, for the time period $t_3 \leq t < t_4$, (L) discharges as a positive current because $V_S > V_C$.

    However, for time period $t_4 \leq t < t_1$ of the next period, L discharges as a negative current because $V_C > V_S$ and the R-load would be fed by I_L which is the same capacitor's current ($I_C = I_L$).

3.3.2.7 Conclusion of Single Switch Method

According to the simulation's results, the newly proposed PFC circuit was able to reduce the THD_I to 17% with a unity power factor (0.986) at the input side and increases the efficiency to 98.68%.

The topology of reducing the conduction time of the main capacitor via dividing the waveform into three regions ON-OFF-ON, can improve the efficiency, the input PF and reduce the THD_I on the input side.

In addition, preventing the capacitor (C) from working in the middle of the period for about a half of the time, will cause in third order harmonic elimination. Also, will shift the harmonics current to the high-frequency region which may contribute to reducing the size of magnetics due to the small value of the inductor 20 µH, and produces few losses. Accordingly, the small inductor will effectively reduce the size and weight as used just one MOSFET, so the rectifier is not bulky any more, and that reduces the cost of the converter.

Another advantage of this circuit is that the snubber circuit is not compulsory because of the presence of freewheeling diode. In addition, the design is considered as a high efficient design due to minimum number and small values of components and simple circuit design due to uses single switch.

The performance of this circuit has a wide range of flexibility because, the output ripple voltage, the input PF and THD_I can be improved via controlling the values of duty cycles of (SW), (L) and (C).

From graphical waveforms and tables of results analysis for different values of R-load, inductor (L), and switching frequency, can be concluded that the increasing of inductor value (L) and R-load values is required in order to get a constant unity power factor, small THD_I and high efficiency.

The advantages of this design:

1. The main contribution of this project is to reduce the inductor's value of PFC circuit (96%) in comparison with the conventional boost converter.
2. A new method to eliminate third order harmonic current from the input source side which decreases the value of THD_I into 17% and improves the input PF into 0.986 .
3. The simplicity of the design, because it consists of one active switch and don't need a snubber circuit.
4. The low switching and conduction losses, because it uses single active switch with lower switching frequency (20 kHz). Therefore, high power conversion efficiency (more than 98%) is possible.
5. The small size, light weight and low cost.

The limitations of this design:

1. High spikes on the waveform of (I_S) reaches to (2 I_{peak}). However, considered as limited effect because it appears only in 50% of each half in two separate periods and not exist at the peak value.
2. The ripple of output waveform is high (39%), which results in poor regulated voltage.

3.3.2.8 Summary of Chapter 3

3.3.2.8.1 Comparison Among PFC Converter Topologies :

A qualitative comparison has been made in [142] among high input PF boost converters as they are the most public boost converters with the two newly proposed circuits.

Table 3.11: Qualitative comparison among high PF boost converters

Parameters	**CBC**	**BBC**	**IBC**	**3L-BC**	**HB-BC**	**VD-BC3 SSC**	**2-SW.**	**1-SW.**
Number & inductance of filter inductor	1 x L	1 x L	2 x $\frac{L}{2}$	1 x L	1 x L	1 x $\frac{L}{16}$	1 x $\frac{L}{54}$	1 x $\frac{L}{27}$
Voltage doubler characteristic	No	No	No	Yes	No	Yes	No	No
Operation freq. of the magnetic elements	f_s	f_s	$2f_s$	f_s	f_s	$2f_s$	$2f_s$	$2f_s$
Use of auto-transformer	No	No	No	No	No	Yes	No	No
No. of diodes which I_S flows through	3	2	3	3	1	2	2	2
No. of active SW operating at high freq.	1	2	2	2	2	4	2	1
No. of diodes operating at high freq.	1	4	2	2	2	4	2	2
Voltage value across the main switch	V_o	V_o	V_o	V_o	$2.V_o$	V_o	V_o	V_o
Bridgeless structure?	No	Yes	No	Yes	Yes	Yes	No	No

Table 3.11, compares many important parameters which may help to assess the exist topologies and compare it with the newly proposed PFC circuit. Table 3.11, presents different parameters in a comprehensive comparison among different topologies of boost converters, which is regarded as the most common type of the PFC circuits due to its advantages, with the two proposed circuits. The significant features of the proposed circuits have been added on the last two columns in order to compare and show the superiority of the new circuits.

3.3.2.8.2 The Best Solution :

Because the two-stage approach is the most commonly used approach [152] as stated before, and main drawbacks of this approach are using at least two active switches with two control circuits and bulky passive elements, which increases the complexity, the size and the cost of the circuit, then the newly proposed PFC circuit that gives almost unity PF would match with the two-stage approach as it addresses the problems of two-stage approach because reduces the value of inductor (98% - 96%) in comparing with traditional boost converter and can either works with two active switch without external control circuit or works with a single active switch and a single control circuit.

The flexibility of changing the output ripple voltage value (in wide range of voltage), presents the proposed circuit as a successful alternative for power factor pre-regulator (PFP) in two-stage AC/DC converters.

3.3.2.8.3 Comparison Between Simulation & Experimental Study :

Engineers in every field continually strive to make models to better predict actual outcomes. For power systems engineers, models are critical to the planning and economic design of the massive infrastructure that keeps our lights on [162].

Today's power systems engineers are equipped with tools that harness incredible computing resources to model every aspect of the power grid. In a single simulation, tens of thousands of power transmission lines are connected with their respective substations, including representations of power producers and consumers [162].

Thousands of possible line and generator outages can be automatically simulated to determine whether any one outage could result in a loss of power to consumers. These tools and others help power system planners and equipment designers optimize their designs and most importantly ensure that our complex electric network continues to operate reliably and efficiently [162].

The simulation programs prove there preciosity in design and work, because of the results of simulation are always identical or very consistent with the actual results as many researchers support that in their articles after a comparison between simulation and experimental results in these references [163–170].

Chapter 4

Two Novel Power Terms, and Apparent Power Definition Using a New RAPT Diagram

4.1 Introduction

Power electronics (PE) researchers are conversant with the description of apparent (S), active (P) and reactive (Q) power and power factor (PF) in a single-phase sinusoidal circuits and in balanced three-phase circuits. Unfortunately, the generalization of this description into other types of circuits (e.g. non-linear loads or non-sinusoidal systems) can lead to a misinterpretation of the understanding the physical meaning of these components.

A long dispute around the meaning of these power components in the non-sinusoidal conditions has been had along the electrical engineers since at least 1916 [171] when Steinmetz, discussed the problem of power components in sinusoidal and non-sinusoidal conditions. With the inevitable diffusion of PE devices, in the practical life of power engineering, and the problems which have been produced in

a result of the harmonics, a new debate has been revived in the last 40 years [172]. All that time, these efforts have been made in order to find new definitions for the power components with the increasing of frequency and new terms have been invented (e.g. non-active power (N)).

Some researchers have dedicated their entire academic lives to this purpose, even a number of schools of diverse elucidations have been launched for decades. The supporters of these schools abide by them frequently with a type of religious enthusiasm more than scientific evidences [173].

Generally, the author of every new definition shows the contradictions and limitations of other definitions, and claim that his proposal is finally right and will solve all the troubles related to the power components definitions in non-sinusoidal condition.

Unfortunately, there is still no consensus in the power community between the engineers on an interpretation of power phenomena of circuits with non-sinusoidal voltages and currents, in spite of this controversy has been continued for decades. The researchers, Attributed the reason to two reasons. Firstly, because the argument on what constitutes the (reactiveness) of reactive power. Secondly, the argument on the physical interpretation of apparent power [174].

This chapter is a new attempt to describe the relationship between power components in non-sinusoidal system depending on the idea of orthogonality law and applying the geometric sum on all power categories instead of using arithmetic sum. In addition, two novel power terms called effective active power (P_{ef}) and effective reactive power (Q_{ef}) have been suggested.

This research, has multiple contributions which can be summarized as follow:

- It proves the validity of right-angled power triangle RAPT Diagram for all power components (total, fundamental, and distortion) and all power categories (S, P & Q) for non-sinusoidal systems.

- It refutes Budeanu's power theory and its three dimensional power diagram.
- Proves the ability to employ the orthogonality law on all power components in non-sinusoidal, and using the geometric sum instead of arithmetic sum.
- presents two novel power terms called (P_{ef}) and (Q_{ef}).
- Submit a new comprehensive definition for total apparent power in non-sinusoidal systems which can explain the physical meaning of apparent power.

4.1.1 Overview on Power Theories

The researchers in the electrical engineering community since the end of the 19th century were seeking for a power theory in order to describe the power flow within electric networks under non-sinusoidal conditions. Power theory, is a group of true statements can describe the power system properties and components, without conflict with the principles of electricity. The spread of PE devices in electrical systems provides added motivation to find such a theory. In spite of many power theories have been proposed regarding non-sinusoidal operation, an adequate solution is yet to be found [175]. The challenge of developing a unified power theory for electric networks suitable for sinusoidal and non-sinusoidal conditions can be traced back to 1892 when Steinmetz showed that in circuits with electric arcs the active power is smaller than the apparent power [2]. This section presents an overview of the most famous power theories in the literature.

4.1.1.1 Budeanu's Theory

This theory has been proposed by Budeanu in 1927 [8] based on frequency domain. The active power (P_t) in a non-sinusoidal system was defined as the arithmetic summation of active power for all harmonic orders as shown below in equation 4.1:

$$P_t = \sum_{n=1} P_n = \sum_{n=1} V_n I_n \cos\theta_n \tag{4.1}$$

where (V_n) and (I_n) are the RMS-values of the voltage and current harmonics of order (n), and (θ_n) is the phase angle difference between them. Therefore, according to Budeanu, the reactive power is the arithmetic summation of reactive power for all harmonic orders as shown below in equation 4.2:

$$Q_t = \sum_{n=1} Q_n = \sum_{n=1} V_n I_n \sin\theta_n \tag{4.2}$$

This equation does not oppose with the power triangle equation $S^2 = P^2 + Q^2$, since the system is sinusoidal and the load is linear. However, when the load is non-linear or the system is non-sinusoidal then a new quantity named distortion power (D) was added in [8] as: $D^2 = S^2 - P^2 - Q^2$

However, the definition according to Budeanu is not considered as a useful term for any practical applications [176], [177]. Furthermore, reactive power is not a quantity defined by any single physical phenomenon but a mathematically defined quantity that has some very useful characteristics and physical interpretations at sinusoidal conditions.

The most important characteristics of reactive power at sinusoidal conditions have been concluded from [178], as following:

1. The peak value of the purely bidirectionally pulsating instantaneous power through a point in a power system is always equal to the reactive power.

2. The power factor will be unity, if the reactive power is decreased to zero.
3. The reactive power completes the power triangle, $S^2 = P^2 + Q^2$.
4. The sum of all reactive powers in any node of a power system is zero.
5. Reactive power can be described by the terms V, I and $\sin\theta$.
6. Reactive power can be positive or negative and the sign shows whether a load is inductive or capacitive.
7. If an inductive or capacitive elements have been inserted to the system, the reactive power can be decreased to zero.
8. The reactive power in transmission lines is proportional with the voltage drop of power system.

All these features are firmly related in the sinusoidal case and depend directly on the phase angle between the voltage and the current [179]. All the above features are valid for the equation $Q = V.I.\sin\theta$, in sinusoidal situations. For non-sinusoidal signals, the Budeanu definition does not always agree with the characteristics 2, 3, 7.

The main advantage of this definition is that the sum of all reactive powers into a point in a power grid is zero. The main drawbacks are that the PF will not be always unity even if the Q using this definition is reduced to zero and that the reactive power can not be totally compensated by inserting inductive or capacitive components [179]. The drawbacks and the limitation of this theory, will be discussed in details in the next section.

4.1.1.2 Fryze's Theory

The power theory suggested by Fryze in 1931 [180], is depending on a time domain analysis. The current is divided into two portions. The first portion, (i_a), is a current of the same wave shape and phase angle as the voltage. The amplitude of the expression ($I_a \,.\, V$) is equal to the active power. The second portion of the current is just a residual term named (i_r). The two currents an be calculated by using the following equations, equation 4.3 and equation 4.4 as stated in [173]:

$$i_a = \frac{P}{V^2}.v \tag{4.3}$$

$$i_r = i - i_a \tag{4.4}$$

i, i_r and i_a: are instantaneous values of current.

The reason behind this division is that the current (i_a) is the current of a purely resistive load that would develop the same power as the load measured on. Accordingly, if (i_r) can be compensated, the source will see a purely resistive load and the PF will be unity [173]. Therefore, we can assure that (i_a) and (i_r) are orthogonal components and then the RMS values can be estimated by using equation 4.5:

$$I^2 = I_a^2 + I_r^2 \tag{4.5}$$

It can be calculated that, Fryze's theory doesn't present a fourth power component and when the (Q = zero), then the (PF = 1) which can regarded as a main benefit of this theory. The main drawbacks of this theory is that the sum of the reactive power according to Fryze (Q_F) in a node of a power grid is not equal to zero; therefore, it can't be used in power flow measurements for non-sinusoidal systems. In addition, in spite of (PF = 1) when (Q_F) decreased to zero. However, this can't be investigated by using only capacitors or inductors. At the same time, (Q_F)

doesn't tell us how to compensate it by using passive elements [181].

4.1.1.3 Shepherd and Zakikhani's Theory

A new power theory has been suggested in 1972 [172]. This theory was depended on a frequency domain analysis. A common and non-common harmonics will be produced in a result of using a non-linear load with a sinusoidal voltage source. Both (V_n) and (I_n) are corresponding, when using the common harmonic of order (n) and non-zero. While only one of the (V_n) and (I_n) is non-zero, when the non-common harmonic of order (n) is applied . Then the apparent power (S) can be stated as equation 4.6:

$$S^2 = \left(\sum_{n\in N} V_n^2 + \sum_{m\in M} V_m^2\right).\left(\sum_{n\in N} I_n^2 + \sum_{p\in P} I_p^2\right) \tag{4.6}$$

where (N) is the set of all common harmonic orders and (M) and (P) represent all the non-common, non-zero, harmonic orders of the voltage and the current respectively. (M) is the set of orders for which the voltage harmonics are non-zero, while the symmetrical current harmonics, are zero. Shepherd then, proposed a split of apparent power into (S_R), (S_X) & (S_D) as equations 4.7, 4.8 & 4.9:

$$S_R^2 = \sum_{n\in N} V_n^2 \sum_{n\in N} I_n^2 \cos^2\theta_n \tag{4.7}$$

$$S_X^2 = \sum_{n\in N} V_n^2 \sum_{n\in N} I_n^2 \sin^2\theta_n \tag{4.8}$$

$$S_D^2 = \sum_{n\in N} V_n^2 \sum_{p\in P} I_p^2 + \sum_{m\in M} V_m^2.\left(\sum_{n\in N} I_n^2 + \sum_{p\in P} I_p^2\right) \tag{4.9}$$

which yields, equation 4.10:

$$S_t^2 = S_R^2 + S_X^2 + S_D^2 \tag{4.10}$$

(S_R) is the real part of apparent power but not equal to the active power, (S_X) is the imaginary part of apparent power, and S_D is the distortion part of apparent power.

The main disadvantage of this theory is that, the active power (P) is not given in the power equations and $S_R \neq$ P.

4.1.1.4 Sharon's Theory

This power theory in 1973 [182] was also depended on a frequency domain analysis. It is a small but significant development of the Shephered's theory. It begins with the same division into common and non-common harmonic components. Then (S) can be expressed as same as equation 4.6.

Sharon then suggests an apparent power component according to equation 4.11:

$$S_Q^2 = V_{rms}^2 \sum_n I_n^2 \sin^2 \theta_n \tag{4.11}$$

and a rest term, equation 4.12:

$$S_C^2 = \sum_{m \in M} V_m^2 \sum_{n \in N} I_n^2 \cos^2 \theta_n + V_{rms}^2 . \sum_{p \in P} I_p^2 + \frac{1}{2} \sum_{\beta \in N} \sum_{\gamma \in N} (V_\beta I_\gamma l \cos \theta_\gamma - V_\gamma I_\beta l \cos \theta_\beta) \tag{4.12}$$

which yields, equation 4.13:

$$S_t^2 = P^2 + S_Q^2 + S_C^2 \tag{4.13}$$

There are two important differences between this definition and the definition

based to Shepherd and Zakikhani. The first difference is presenting (P) as one of the power components and not separately defined. The second difference is the calculation of S_Q as it's derived by a multiplication by the total RMS voltage and not only the RMS voltage of the common harmonic orders.

4.1.1.5 Kusters and Moore's Theory

This power theory in 1980 [183], was depended on a time domain definition. The definition of Fryze has been extended by using a further split of the residual current into two orthogonal components. However, this division is made bases on whether the load is mainly a capacitive or an inductive load. The three currents achieved by this division are then named active current (i_p), capacitive reactive current (i_{qc}) or inductive reactive current (i_{ql}) and the residual reactive current, which results in an apparent power sum:

$S^2 = P^2 + Q^2 = P^2 + Q_c^2 + Q_{cr}^2 = P^2 + Q_l^2 + Q_{lr}^2$

The active current is (as by Fryze) defined by equation 4.14:

$$i_p = \frac{P}{V^2}.v = \frac{\frac{1}{T}\int v.idt}{V^2}.v \tag{4.14}$$

and the capacitive reactive current is similarly defined as equation 4.15:

$$i_{qc} = v_{der}.\frac{\frac{1}{T}\int_T V_{der}idt}{V_{der}^2} \tag{4.15}$$

and the inductive reactive current as equation 4.16:

$$i_{ql} = v_{int}.\frac{\frac{1}{T}\int V_{int}idt}{V_{int}^2} \tag{4.16}$$

where (v_{der}) and (v_{int}) are the periodic part of the derivative and integral of the (instantaneous) voltage, respectively. V_{der} and V_{int} are the corresponding RMS

values. Both of these currents can then be shown orthogonal to the residual current in the same way as i_p. Because of the orthogonality, P, Q_c and Q_l can be determined by the equations:

$$P = V.I_p \tag{4.17}$$

$$Q_c = V.I_{qc} = \frac{V}{V_{der}}.\frac{1}{T}\int v_{der}.idt \tag{4.18}$$

$$Q_l = V.I_{ql} = \frac{V}{V_{int}}.\frac{1}{T}\int v_{int}.idt \tag{4.19}$$

The definition by Kusters and Moore has an advantage in comparing with the Fryze decomposition, because it identifies the part of the current that can be compensated with a shunt capacitor or inductor, and that characteristic 6 and 7 are fulfilled for Q_c and Q_l. However, it's only valid with ideal sources.

4.1.1.6 Czarnecki's Theory

This theory is bases on a frequency domain definition in 1985 [184]. The author criticized the previously proposed definitions. He proves that if the source impedance is not negligible, then a single shunt reactance can be completely ineffective compensator even at moderate levels of harmonics (10%). This would make the definition depending on Kusters and Moore less efficient. He also shows the shortcoming of the Shepherd and Zakikhani's definition, that ($S_R \neq$P). The active current (i_a) for linear loads, has been defined in the time domain according to Fryze. However, Czarnecki proposed a new definition based on time domain [179]. The instantaneous value of a periodic voltage can be expressed as a complex Fourier series in equation 4.20:

$$v = \sqrt{2}Re\sum_n V_n(e^{jn\omega_1 t}) \tag{4.20}$$

where (ω_1) is the fundamental angular frequency, and (n) is a harmonic order for which (V_n) is non-zero. In a power system this voltage may be connected to a linear load with the admittance: $Y_n = G_n + jB_n$, that is, both (G) and (B) can be dependent on the frequency. The current will then be as in equation 4.21:

$$i = \sqrt{2}Re\sum_n V_n(G_n + jB_n).e^{jnw_1t} \tag{4.21}$$

Assuming that all the power is absorbed by a (frequency invariant) conductance (G_e), as in the power definition according to Fryze, this conductance can be determined by: $G_e = \frac{P}{V^2}$

When exposed to the voltage (V), the current through this conductance will be equal to the active current (i_a). The residual current can then be calculated by equation 4.22:

$$i - i_a = \sqrt{2}Re\sum_n (G_n - G_e + jB_n)V_n.e^{jnw_1t} \tag{4.22}$$

This current can further be divided into ($i_s \& i_r$) as equation 4.23:

$$i_s = \sqrt{2}Re\sum_n (G_n - G_e)V_n e^{jnw_1t} \tag{4.23}$$

which is called scatter current by Czarnecki, and equation 4.24:

$$i_r = \sqrt{2}Re\sum_n jB_n V_n e^{jnw_1t} \tag{4.24}$$

which is denoted as a reactive current. All these currents are orthogonal; therefore, the RMS-values of the currents can be expressed by equation 4.25:

$$I_t^2 = I_a^2 + I_s^2 + I_r^2 = \frac{P^2}{V^2} + \sum_n (G_n - G_e)^2 V_n^2 + \sum_n B_n^2 V_n^2 \tag{4.25}$$

4.1.1.7 Other Power Theories

The problem of describing the different power components in non-sinusoidal systems is quite old, during this period a huge number of researchers have tried to invent a power theory suitable for non-sinusoidal systems. However, presenting all the work accumulated over more than a century attempting to solve this problem might be the subject of a large textbook. Therefore, a list of the most influential authors is provided below:

1. A. Nabae and T. Tanaka - Powers based on instantaneous space vector [185].
2. H. Akagi - The instantaneous reactive power (p-q) theory [115].
3. M. Depenbrock - Fryze-Buchholz-Depenbrock (FBD) Power Theory [186].
4. M. A. Slonim and J. D. Van Wyk - Definition of active, reactive and apparent powers [187].
5. A. E. Emanuel - Definitions of apparent power for 3-phase system [188].
6. F. Z. Peng and J. S. Lai - Generalized instantaneous reactive power theory [189].
7. Ferrero, Superti-Furga - The Park power theory [190].
8. L. Rossetto and P. Tenti - Instantaneous orthogonal currents [191].
9. Peng - generalized non-active power theory for STATCOM [192].
10. Willems - Instantaneous voltage and current vectors [193].
11. P. S. Fillipski - Elucidation of apparent power and power factor [194].
12. Watanabe, Akagi, Aredes - Generalised theory of instantaneous powers α-β-0 transformation [195].
13. F. Ghassemi - Definition of apparent power based on modified voltage [196].

14. N. LaWhite, M. D. Ilic - Vector space decomposition of reactive power [197].

15. J. Cohen, F de Leon and K M Hernandez - Time-domain representation of powers [198].

16. H. Lev-Ari and A. M. Stankovic - Reactive power definition via local Fourier transform [199].

17. M. T. Haque - Single phase p-q theory [200].

18. Zhang, N. Huang - Universal instantaneous power theory [201].

19. A. Menti, T. Zacharias, and J. Milias-Argitis - The Geometric Algebra for representing non-sinusoidal power theory [202].

20. X. Dai, L. Guohai and G. Ralf - Generalised theory of instantaneous reactive power for multiphase system [203].

21. M. Castilla, J. C. Bravo, M. Ordonez, J. C. Montano, A. Borras, A. Lopez, and J. Gutierrez - Non-active power multivector by using Geometric Algebra [204].

22. Shin-Kuan Chen and G W Chang - Instantaneous power theory using 3-phase active filter [205].

4.2 The Proofs of Validity of The Orthogonality Law

Electrical engineers are well acquainted with the concepts of average power, reactive power, apparent power, and power factor to describe sinusoidal single-phase circuits and balanced sinusoidal three-phase circuits. However, attempts to generalize these concepts, can be misleading for other types of circuits (e.g. non-linear loads or non-sinusoidal systems).

A controversy over the meanings of various types of powers involving non-sinusoidal waveforms has been had with the electric power community since at least 1927 [8]. With the pervasive impact of harmonics related problems on the practice of power engineering, a new dispute has been revived in the last 40 years [172]. Throughout the last century, new definitions appear with increased frequency concern the definition of the apparent power (S) and reactive power (Q) or the nonactive power (N) in non-sinusoidal situations.

The author of every new definition points to the inconsistencies in other proposals, and claim that his proposal is finally right and will solve all the problems associated with the reactive power definitions. In spite of the fact that this discussion has been continued for almost hundred years, there is still no consensus.

According to [182], apparent power (S) is not a vector, but it is the product of the magnitude of two vectors : S $=|i||v|=$ I V .

So, when (i) and (v) are sinusoidal waveforms and the load is linear, it is possible to directly associate the real and reactive components of the current with those of the apparent power, namely real (active) power (P) and reactive power (Q). However, if (i) or (v) are non-sinusoidal or/and the load is non-linear, a new term will present called the harmonics distortion power (P_h) or (D) [182].

On the other hand, (i) and (v) remain vectors in non-sinusoidal system permitting vector summation of the harmonics. Since then, distortion power can be analyt-

ically decomposed into active and nonactive components. However, because of the phase shift of non-sinusoidal current depends on the frequency; therefore, the sinusoidal system associated by geometric summation [182].

In the following, some important points which either support the idea of geometric sum for all power components or deny the conventional (arithmetic sum) of power components, and these points are sufficient to justify the orthogonality law and the newly proposed power terms and power diagram:

1. Budeanu's theory for non-sinusoidal condition [8] which is defining the reactive power Q_b as the arithmetic sum of Q_h

$$Q_b = \sum_{h=1} V_h I_h \sin\theta_h$$

was strongly rejected by lots of researchers throughout 90 years of researches as mentioned in the following:

a. Fryze in 1931 [180], objected Budeanu's theory and he described the necessity to the voltage and current harmonic decomposition before the reactive power could be calculated and relied on the time domain approach.

b. Shepherd and Zakikhani in 1972 [172], assured that the Budeanu reactive power (Q_B) is not a real physical quantity and they suggested another quantity to be chosen as a reactive power.

c. Czarnecki in 1987 [206], objected strongly Budeanu's theory and proved that this theory does not possess the attributes which could be related to the power phenomena in the circuit and does not express any distinct energy phenomenon.

Moreover, Budeanu's values do not provide any information necessary for the design of compensating circuits. Also, the value of distortion power (D) is not related to the waveform distortion.

Also (D) is not equal to zero when the current and voltage waveforms are identical but shifted in time. However, D can be equal to zero even when the voltage and current waveforms are not identical.

In additioin, the same author in 1997 [181] has concluded that, the distortion power (D) in single-phase non-linear circuits has nothing in common with waveform distortion, similarly as Budeanu's reactive power equation has nothing in common with energy oscillation. Thus, Budeanu's power theory misinterprets power phenomena in electrical circuits.

d. Budeanu's definitions have been refused by Slonim in 1988 [187]. The author has confirmed that Q_B is just an arbitrary mathematical implication and it has no physical interpretation.

e. Filipski in 1993 [207], approved that Budeanu's definitions of reactive and deformation powers, do not reflect properly the energetic relation in non-sinusoidal conditions. Also, the same author in [208] has proved with illustrated examples that Budeanu's definition of reactive power in non-sinusoidal system has many shortcomings.

Filipski proved that the calculated reactive power according to Budeanu's definition, may be zero even though there is a reciprocating energy flow between the source and the load at different frequencies.

Also, he showed that one can still completely compensate a reactive load to unity power factor even when Budeanu's reactive power is zero.

Moreover, Reactive power as defined according to Budeanu (arithmetic sum of Q) has no physical significance in non-sinusoidal circuits.

The use of Q_B in non-sinusoidal situations is misleading because merely reducing Q to zero does not result in optimum power factor compensation. Hence, compensation of the reactive power as defined according to Budeanu alone may be useless for power factor improvement.

2. Reactive power definition proposed by Fryze [180] in 1931 is based on the division of the current into two terms as the active current (I_a) and the reactive current (I_r), considering that these terms are orthogonal, then:

   $\frac{1}{T}\int_0^T i_a i_r dt = 0$ (as the inner product is zero).

   Similarly, (P_{avg}) for different frequencies is zero due to orthogonality (P_{13}, P_{15} or P_{35}....etc.), as:

   $P_{35} = \frac{1}{T}\int_0^T V_3 I_5 dt = 0$

   Consequently, harmonic currents and voltages of different frequencies are all orthogonal with each other and effective active power can be expressed as following in equation 4.26:

   $P_{ef}^2 = P_{11}^2 + P_{33}^2 + P_{55}^2 + P_{77}^2$+.....etc.

$$\therefore P_{ef}^2 = P_{11}^2 + \sum_{h=3} P_{hh}^2 \tag{4.26}$$

3. Depenbrock in [209] & [210], has supported Fryze's model which says: ($I = I_a + I_b$), and claimed that the total current is consisting of fundamental and harmonic parts: ($i = i_1 + i_h$).

   Therefore, we can conclude that when $I_{a1} = I_1 \cos\theta_1$, $I_{ah} = I_h \cos\theta_h$:

   $\therefore I_a = \sqrt{I_{a1}^2 + I_{ah}^2} = I\cos\theta$

   $\because P = VI_a = V\sqrt{I_{a1}^2 + I_{ah}^2}$

   $\therefore P_{ef}^2 = P_{a1}^2 + P_{ah}^2 = P_{fundamental}^2 + P_{harmonics}^2$

   Notice that this allegation supports the idea of a geometric sum of power components for the active power.

4. Since the non-linear load is always polluted, then the active part of the distortion power (D) which consists of P_{33}, P_{55} and P_{77} are negative values some times (depending on the load nature). However, the total P_{hh} should be positive because, an amount of energy is being dissipated. Accordingly,

the total result will be positive always when the geometric sum is using instead of the arithmetic sum.

thus: $P_{hh} = \sqrt{P_{33}^2 + P_{55}^2 + P_{77}^2 + ...etc.}$

5. Slonim, concluded in 1988 [187] that there is no accepted, clear definition of reactive and distortion power. Also, he confirmed that there is no physical interpretation for reactive, distortion and apparent power. Accordingly, he claimed that:

$$S_t^2 = \sum_{k=0}^{\infty} P_k^2 + \sum_{k\neq n}^{\infty} P_{kn}^2 + \sum_{n=0}^{\infty} Q_k^2 + \sum_{k\neq n}^{\infty} Q_{kn}^2$$

$$\therefore S^2 = \sum_{n=1}^{\infty} P_n^2 + \sum_{n=1}^{\infty} Q_n^2$$

Obviously, this equation confirms the idea of geometric sum because, $(P_{\sum}^2)$ and $(Q_{\sum}^2)$ are the geometric sum of active and reactive power components, respectively.

6. Czarnecki in [173], has presented a new power theory. His method was meant to improve on the limitation of Fryze's model. He has a collective reactive power, Unlike Budeanu's reactive power:

$Q_r = VI_r = V\sqrt{\sum (B_h V_h)^2}$.

This allegation supports the idea of geometric sum to be used for the total reactive power calculation because: $Q_t = \sqrt{\sum Q_n^2}$.

This type of summation has the attribute of getting a positive result always (bigger than zero) and that's mathematically and practically truthful to the actual oscillation of energy.

7. Each of the current harmonics I_h can be decomposed into two orthogonal component $(I_h \cos\theta_h \;\&\; I_h \sin\theta_h)$, since all current harmonics are mutually orthogonal. Thus, the square of the RMS current (geometric sum) is:

$$\sum_{n=1} I_n^2 = I_1^2 + \sum_{h=2} I_h^2$$

$$\sum_{n=1} I_n^2 = \left[I_1^2 \cos^2\theta_1 + I_1^2 \sin^2\theta_1\right] + \left[\sum_{h=2} I_h^2 \cos^2\theta_h + \sum_{h=2} I_h^2 \sin^2\theta_h\right]$$

Therefore, if there is a reciprocating energy transmission between the source and the load then the term $\sum Q_n^2$ (but not $\sum Q_n$) is responsible for the source apparent power's increase [211].

8. According to Shepherd and Zand in [211], the equation:

$$Q = \sum_{h=1} V_h I_h \sin\theta_h$$

does not correctly define the reactive power in non-sinusoidal system. Because, in non-sinusoidal supply situation, the fluctuations of the stored capacitive and inductive energies are not synchronous such that the pulsating power to be delivered by the source does not correspond to the difference of both energy components.

Consequently, there is no justification for simply adding (arithmetic sum) the reactive powers corresponding to different frequencies as its done in Budeanu's reactive power concept [211].

9. In mathematical laws, quantities x(t) and y(t) are orthogonal if one of three cases has been applied, and one of these cases is when x & y are harmonics in different orders:

$x = x_r.\sin(rw_1t - \alpha)\ ,\quad y = y_s.\sin(sw_1t - \theta)$

(when $r \neq s$), and that's including all the harmonics components, thus:

$I_t^2 = I_1^2 + I_3^2 + I_5^2 + \ldots\ldots\ldots\ldots + I_n^2$

$V_t^2 = V_1^2 + V_3^2 + V_5^2 + ... + V_n^2$

$S_t^2 = S_1^2 + S_3^2 + S_5^2 + ... + S_n^2$

$P_t^2 = P_1^2 + P_3^2 + P_5^2 + ... + P_n^2$

$Q_t^2 = Q_1^2 + Q_3^2 + Q_5^2 + ... + Q_n^2$

Which basically means the geometrical sum of power components

10. According to the orthogonality law, two components are orthogonal if the inner product of them is equal to zero.

    In order to prove the geometric sum of active power, the orthogonality of (P_1) with (P_h) should be tested when, $P_1 = V_1 I_1 \cos\theta_1$ and $P_h = V_h I_h \cos\theta_h$:

    The inner product $= \frac{1}{2\pi}\int_0^{2\pi} P_1 P_h dwt$

    $= \frac{1}{2\pi}\int_0^{2\pi} I_1 V_1 \cos wt \,.\, I_h V_h \cos(hwt - \theta_h) dwt$

    $= \frac{I_1 V_1 I_h V_h}{2\pi}\int_0^{2\pi} \frac{1}{2}\big[\cos(wt - hwt + \theta_h) + \cos(wt + hwt - \theta_h)\big] dwt$

    $= \frac{I_1 V_1 I_h V_h}{4\pi}\big[\sin(wt(1-h) + \theta_h) + \sin(wt(1+h) - \theta_h)\big]\Big|_0^{2\pi}$

    $= \frac{I_1 V_1 I_h V_h}{4\pi}\big[\sin(2\pi(1-h) + \theta_h) + \sin(2\pi(1+h) - \theta_h) - \sin(0(1-h) + \theta_h) - \sin(0(1+h) - \theta_h)\big] = Zero$

    Therefore (P_1) & (P_h) are orthogonal components and the geometric should be used in order to calculate the total active power.

11. The benefit of using the geometric sum instead of the arithmetic sum in active and reactive power calculations is the increasing of the dependency on the fundamental component and decreasing the effect of harmonics component. This is because, the fundamental component is originally greater than the harmonics component. Also, the squaring of the values make the difference huge between the fundamental and the harmonic component.

    According to the author in [212], the philosophy of separating the main (fundamental) component from the pollution (non-fundamental) components and their cross terms is successful because:

a. Utilities generate and distribute nearly perfect fundamental sinusoidal voltage.

b. The consumer expects fundamental sinusoidal voltage.

c. Generally, more than 99% of the total active power flowing in the network is fundamental active power (P_1).

The author in [209] concluded that, its better to separate (P_1) and (Q_1) from the rest of the power components, because the power apparent, active, and reactive components are essential factors for the power system. A distribution system cannot perform without reactive power and the useful fundamental magnetizing flux in transformers and AC motors is separated by the fundamental current.

12. The author in 1987 [206], concludes that the phenomena of the reciprocating energy transmission at harmonic frequencies does not affect the source current RMS value and its apparent power (S) in the manner suggested by Budeanu's model. Namely, each of the current harmonics (I_n) can be decomposed into two orthogonal components:

$I_n^2 = I_n^2 \cos^2 \theta_h + I_n^2 \sin^2 \theta_h$

Since all current harmonics are mutually orthogonal, thus the square of the RMS value of the current is:

$$I_{rms}^2 = \sum_{n=1} I_n^2 = \sum (\frac{P_n}{V_n})^2 + \sum (\frac{Q_n}{V_n})^2$$

$$\therefore S_t^2 = \sum_{n=1} (P_n)^2 + \sum_{n=1} (Q_n)^2$$

Therefore, if there is a reciprocating energy transmission between the source and the load, then the terms ($\sum P_n^2$) and ($\sum Q_n^2$) not ($\sum P_n$)^2 and ($\sum Q_n$)^2 are responsible for the source apparent power increase.

13. Emanuel in 1990 [213], has approved that the total reactive power (Q_t) is composed of four distinctive types of elementary reactive powers:

$$Q_t^2 = \sum_{h=1} Q_{Bh}^2 + \sum_{h=1} Q_{Bmn}^2 + \sum_{m\neq n} Q_{Dh}^2 + \sum_{m\neq n} Q_{Dmn}^2$$

$$\therefore Q_t^2 = Q_1^2 + \sum_{h=1} Q_h^2$$

From these equations, it is obvious that the author has agreed indirectly with the idea of geometric sum for the reactive power components.

14. The last update of IEEE-standards 2010 [12] has been mentioned verbally in page (37) :"The fact that harmonic reactive powers of different orders oscillate with different frequencies reinforces the conclusion that the reactive powers should not be added arithmetically (as recommended by Budeanu)". However, the standards did not mention clearly (through equations) the geometric sum of reactive power components.

4.3 Description of The Orthogonality Law And New Power Terms

Depending on the outcomes have been concluded from the previewed literature in the previous section, the power components in different categories and frequencies are all orthogonal and should be calculated using the geometric (not arithmetic) sum, then a new power terms called effective active (P_{ef}) and reactive (Q_{ef}) power terms can be invented in order to understand the characteristics and relations between different power components and to calculate the total apparent power in non-sinusoidal situation.

Lets consider: $V_t^2 = V_1^2 + V_h^2 \quad \& \quad I_t^2 = I_1^2 + I_h^2 \quad \Rightarrow \quad S_t^2 = V_t^2 I_t^2$

$$\therefore S_t^2 = I_1^2 V_1^2 + V_1^2 \sum_{n=3} I_n^2 + I_1^2 \sum_{m=3} V_m^2 + \sum_{m=n=3} V_m^2 I_n^2 + \sum_{m \neq n} V_m^2 I_n^2 \tag{4.27}$$

n: is the harmonic orders of current.

m: is the harmonic orders of voltage.

$$D_I^2 = V_1^2 \sum_{n=3} I_n^2 \tag{4.28}$$

$$D_V^2 = I_1^2 \sum_{m=3} V_m^2 \tag{4.29}$$

$$D_{mn}^2 = \sum_{m \neq n} I_m^2 V_n^2 \tag{4.30}$$

$$S_h^2 = \sum_{m=n=3} I_m^2 V_n^2 = \sum_{h=3} I_h^2 V_h^2 \tag{4.31}$$

$$S_t^2 = S_1^2 + S_h^2 + D_I^2 + D_V^2 + D_{mn}^2 \tag{4.32}$$

$$\therefore S_t^2 = (\text{Fundamental})^2 + (\text{Harmonic})^2 + (\text{Non-active})^2$$

$$\therefore S_t^2 = P_1^2 + Q_1^2 + P_h^2 + Q_h^2 + D_I^2 + D_V^2 + D_{mn}^2 \tag{4.33}$$

This result shows in equation 4.33 that (S_t) can be represented either as a many-dimensional vector, or as a two dimensional vector.

$$S_t^2 = S_1^2 + S_N^2 \tag{4.34}$$

$$S_1^2 = P_1^2 + Q_1^2 \tag{4.35}$$

$$S_N^2 = P_h^2 + D_h^2 \tag{4.36}$$

$$D_h^2 = D^2 + Q_h^2 \tag{4.37}$$

$$D^2 = D_I^2 + D_V^2 + D_{mn}^2 \tag{4.38}$$

$$S_h^2 = P_h^2 + Q_h^2 \tag{4.39}$$

$$P_h^2 = \sum_{h=3} V_h^2 I_h^2 \cos^2 \theta_h \tag{4.40}$$

$$Q_h^2 = \sum_{h=3} V_h^2 I_h^2 \sin^2 \theta_h \tag{4.41}$$

Active power (P) : is the average value of the instantaneous power during a time period. (represents the arithmetic sum).

Effective active power (P_{ef}) : is the active part of the apparent power which the line or load can utilize and cause thermal power. (represents the geometric sum).

Reactive power (Q) : The amplitude of the oscillating instantaneous power. (represents the arithmetic sum).

Effective reactive power (Q_{ef}) : The non-active part of the apparent power. (represents the geometric sum).

Budeanu's distortion power (D_B) definition represents (S_t) as a three dimensional

vector as in equation 4.42:

$$S_t = i.P + j.Q_B + k.D_B \tag{4.42}$$

Budeanu's definition creates different problems, one of them is the necessity to use a new power unit for the distortion power (D_B) [183].

However as Czarnecki stated, the distortion power has the same physical nature as reactive power, then the power unit of (D) must be VAR [184]. This allows us to conclude that all the components of apparent power (S_t) in frequency domain may contains active power (P_t) and reactive power (Q_t) components [187]. The orthogonality law allows us to use only standard units, VA, W and VAR without needing to invent extra units.

$$\because S_t^2 = S_1^2(\cos^2\theta_1 + \sin^2\theta_1) + S_N^2(\cos^2\theta_N + \sin^2\theta_N) \tag{4.43}$$

$$\& \quad \because S_t^2 = P_1^2 + Q_1^2 + P_h^2 + D_h^2 \tag{4.44}$$

$$\& \quad \because S_t^2 = P_{ef}^2 + Q_{ef}^2 = S_{ef}^2 \tag{4.45}$$

$$\therefore P_{ef}^2 = P_1^2 + P_h^2 \tag{4.46}$$

$$\& \quad Q_{ef}^2 = Q_1^2 + D_h^2 \tag{4.47}$$

4.4 New Definition of The Apparent Power in Non-sinusoidal System

The apparent power (S) in non-sinusoidal system has been described in IEEE-standards in 1988 [214], as **"It is numerically equal to the maximum active power that exist at given points of entry with the given effective value of the sinusoidal current and the potential difference and hence is directly related to the size of the required equipment and to the generation and transmission losses"**. This definition of apparent power has a physical interpretation, as it's described the maximum power and transmission losses.

However, Czarnecki in 1994 [215], rejected the idea of a physical interpretation for the apparent power concept, even in single-phase sinusoidal situations, and Filipski asserts in 1993 [174], that the non-sinusoidal apparent power is an artificial quantity without any physical meaning and that there is neither theoretical nor practical justification for the electrical power application. The author has depended in his claims on the current definitions of the apparent power.

The IEEE standard states that the ratio $PF = \frac{P}{S}$ is a factor that indicates the degree of utilization of the line. Such statement indicates a physical interpretation; however, how can a quantity have physical interpretation when its definition involves another quantity that has no physical interpretation? Either it is accepted that the apparent power concept has physical significance, which will lead the power factor concept to claim its physical significance, or it is accepted that the apparent power does not have a physical interpretation which will yield a lack of physical interpretation for the power factor concept [175].

In spite of the justification of physical interpretation of apparent power, the definition still has defect because mathematically can be described as:

$S = P_{max}$, & $S = I_{rms}V_{rms}$

Suppose a non-linear load supplied by a sinusoidal voltage $v(t) = \sqrt{2}V_1 \sin(wt)$

and the current is: $i(t) = \sum \sqrt{2} I_h \sin(hwt + \theta_h)$.

The active power is equal to: $P = V_1 I_1 \cos\theta_1$.

Its maximum value is equal to: $(P_{max} = V_1 I_1)$ rather than $(V_{rms} I_{rms})$.

Assume that (S) is equal to the maximum active power. In this case, (S) is equal to the replacement of the actual load by an equivalent resistive load, drawing a sinusoidal current rather than non-sinusoidal current. The limitation of this definition, is that its describes the power for equivalent load rather than the actual load [207].

The definition of apparent power for non-sinusoidal system according to IEEE-Standards in 2010 [12], has defined as: **(It's the amount of active power that can be supplied to a load or a cluster of loads under ideal conditions (the ideal condition may assume sinusoidal supply voltage and current with linear loads))** but still has a serious limitation.

This (ideal) condition constitute a big limitation for the apparent power interpretation, because in the practical life most of the loads are non-linear and draw non-sinusoidal current. In addition, this condition is mathematically wrong because its neglected the effects of harmonics and the frequency on the power system as the inductive or capacitive loads are based on the frequency, and even the skin effect of resistors is dependent on the frequency.

Obviously, there is no unanimously accepted Apparent power definition until now; therefore, it's useful to find a new definition covers the general aspects for power systems and all practical (not just the resistive) loads. Therefore, the total apparent power can be defined as **(The geometric sum of the active powers (P_t) in all harmonic orders (all frequencies) plus the geometric sum of the non-active powers (Q_t) in all (sinusoidal and non-sinusoidal) conditions)**, or **(It is the geometric sum of any consumed energy and any stored energy going forth and back in the electrical network)**.

Operating on (RMS) value rather than on (max.) value is more reasonable because the RMS values are usually more relevant in practice life (i.e., they can be related to the size of the wiring, breakers, heat, etc....). This practical point of view leads us to accept the RMS form of the apparent power.

The physical interpretation of the new definition and the new RAPT Diagram including new power terms show that the apparent power (S) is an effective value (RMS), as the effective values are calculated using the magnitudes of harmonics terms. Because of the harmonic currents are mutually orthogonal; therefore, the geometric sum has been used to calculate the total apparent power in non-sinusoidal conditions. Accordingly, the newly proposed RAPT Diagram using the geometric summation can represent the non-sinusoidal system efficiently.

4.5 The Explanation of Two-Dimensional RAPT Diagram

Six of the previously derived equations 4.34, 4.35, 4.36, 4.45, 4.46, and 4.47 constitute the power triangles of the newly proposed power diagram. The power triangle (S - P - Q) has been introduced firstly in time domain by Fryze [180] in 1931, when he defined (i_{aF}) as the active current and (i_{rF}) as the reactive current as a part of the time domain description. However, the right-angled triangle power diagram is the first attempt to apply (total - fundamental - harmonics) power triangle in the frequency domain in combination with the time domain (S-P-Q) power triangle.

Due to the non-active power (D_h) is the geometric sum of (D_I, D_v, D_{mn} & Q_h), then: $Q_{ef}^2 = Q_1^2 + D_h^2$, (D_h is mutually orthogonal on Q_1), because of the orthogonality between fundamental and harmonic components.

Simultaneously, (P_h) is orthogonal on (D_h) but not in-phase with Q_1 because they represent different frequencies, because of the orthogonality between (P &

Q), (sin & cos) components.

In the same way, (P_1) is orthogonal on (Q_1) but not in-phase with (D_h) because it is in different frequency. Consequently, (P_h) is orthogonal on (P_1).

The structure of the new diagram RAPT can be formed by gathering six equations which are (4.35, 4.46, 4.47, 4.36, 4.34 and 4.45) respectively. These equations represent six right-angled triangles as shown in figure 4.1.

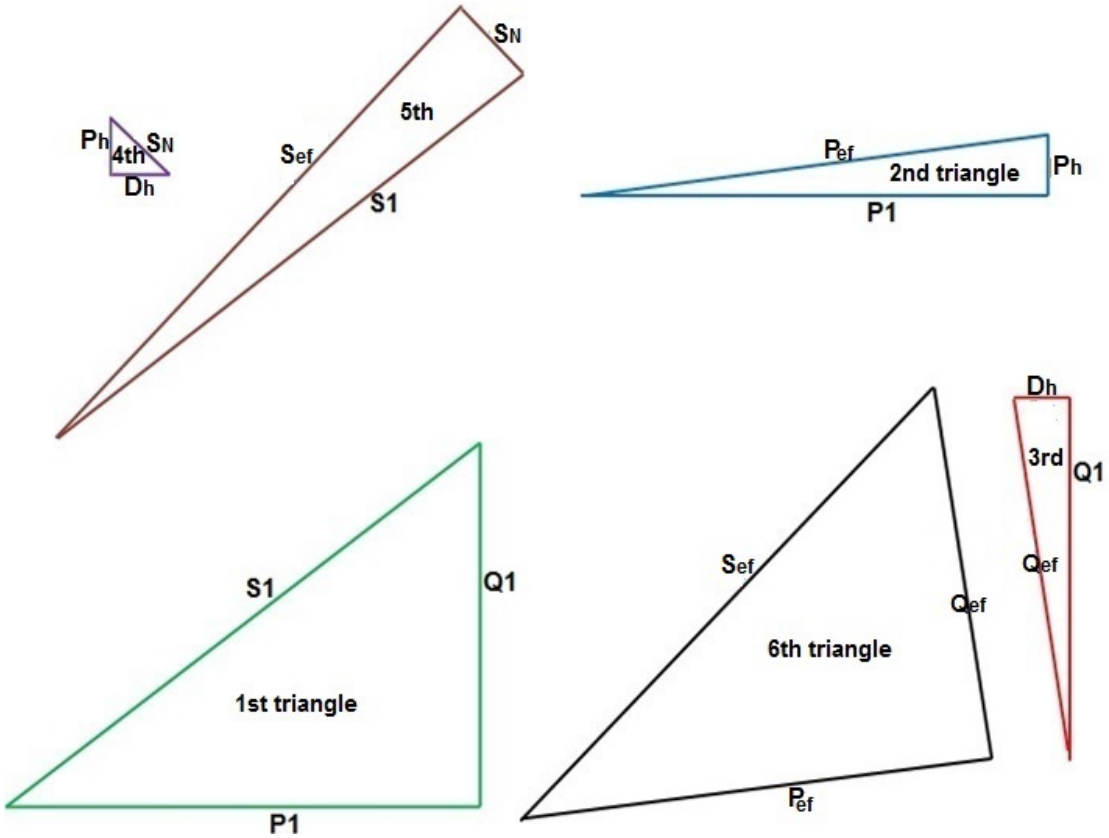


Figure 4.1: Six right-angled triangles

These triangles are formed based on the notion of the orthogonality law. The distortion power (D_h) component is always perpendicular with the fundamental power component, because it held the same characteristic of the reactive power.

In sum, the aggregation of these six triangles produced a new power diagram called RAPT Diagram, this diagram is shown in figure 4.2.

For whatever reason, if the distortion power (D_h) increases, then S_N and the apparent power (S_{ef}) also will increase depending on equation 4.33.

$$S_t^2 = P_1^2 + Q_1^2 + P_h^2 + D_h^2 = S_{ef}^2$$

According to RAPT Diagram and orthogonality law, the power triangles has to form a 90 ° angle between distortion and fundamental components. However, the line S_N in figure 4.2 will not be perpendicular with the line of S_1 after increased. Therefore, in order to reconstruct the right-angled triangle and investigate the angle 90 °, the line S_N has to rotate until been 90 ° angle with the line S_1.

Consequently, the line of S_{ef} will extend also in order to complete the right-angled triangle. The value of S_{ef}, will increase exactly as the equation 4.34 says.

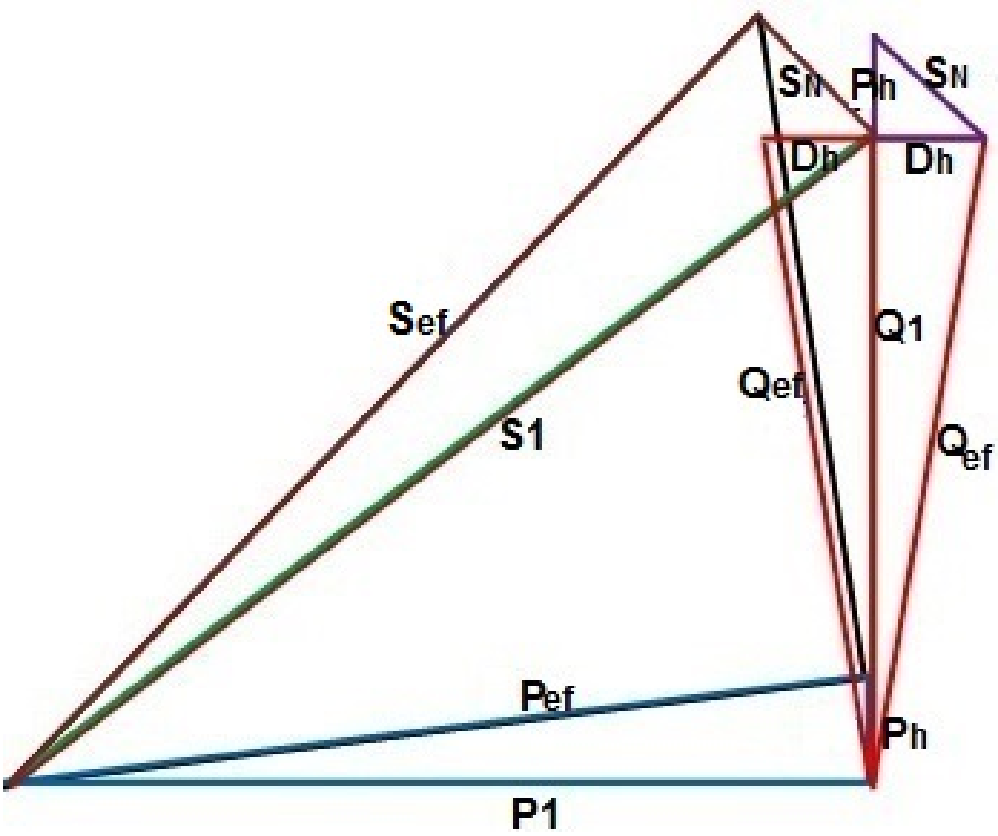


Figure 4.2: New RAPT Diagram

In the following, three steps explain and simplify the understanding of Right-angled triangle diagram formation.

- First step: The basis of the diagram is the first triangle which is the fundamental power (S_1, P_1, Q_1), and then the second triangle is the active power triangle (P_{ef}, P_1, P_h) should be placed and P_1 is identical in both triangles. Then the third triangle is the reactive power triangle (Q_{ef}, Q_1, D_h) will be placed in reverse and perpendicular way to the second triangle. In order to simplify the proposed diagram, the third triangle should be placed twice and in symmetry with Q_1.

- Second step: The fourth triangle, is the distortion power triangle (S_N, P_h, D_h), should be in line above the third triangle and D_h is identical in both triangles. the fifth triangle,the apparent power triangle (S_{ef}, S_1, S_N), has been placed on the S_1 line of the first triangle and same S_N of the fourth triangle and thats will produce S_{ef} component.

- Third step: Finally, the total power triangle (S_{ef}, P_{ef}, Q_{ef}), will be formed automatically by gathering (S_{ef}) line of the fifth triangle with (P_{ef}) line of the second triangle and (Q_{ef}) from the third triangle.

This diagram has the attribute of the simplicity in comparing with the Budeanu's 3-dimension diagram because it has only two dimensions and that gives it the ability to be easily applicable to find the relationships between the different components with there angles $(\theta_t, \theta_1 \& \theta_h)$ and even the calculation of the amplitude value of the power parameters.

4.6 The Mathematical Relationship Between (P_{ef}) & (P_{avg})

This section submits the algebraic relationship between arithmetical summation which represents (P_{avg}) and geometrical summation which represents (P_{ef}) of power components in non-sinusoidal systems.

In algebra equations, Lagrange's identity was described in [216] and [217] as equation 4.48:

$$(\sum_{k=1}^{n} a_k b_k)^2 = (\sum_{k=1}^{n} a_k^2)(\sum_{k=1}^{n} b_k^2) - \sum_{i=1}^{n-1} \sum_{j=i+1}^{n} (a_i b_j - a_j b_i)^2 \tag{4.48}$$

or :

$$(\sum_{k=1}^{n} a_k b_k)^2 = (\sum_{k=1}^{n} a_k^2)(\sum_{k=1}^{n} b_k^2) - \frac{1}{2} \sum_{i=1}^{n} \sum_{j=1, j\neq i}^{n} (a_i b_j - a_j b_i)^2 \tag{4.49}$$

when: $P_h = V_h I_h \cos\theta_h \quad \& \quad P_h = a_k b_k$

$$a_k = V_h = \left(V_1^2 + \sum_{n=1} V_n^2\right)^{\frac{1}{2}}$$

$$b_k = I_h \cos\theta_h = \left((I_1^2 \cos^2\theta_1 + \sum_{n=1} I_n^2 \cos^2\theta_n)\right)^{\frac{1}{2}}$$

$$\begin{aligned} \therefore (\sum_{h=1} V_h I_h \cos\theta_h)^2 = (\sum_{h=1} V_h^2)(\sum_{h=1} I_h^2 \cos^2\theta_h) - \\ \frac{1}{2} \sum_{m=1} \sum_{n=1, n\neq m} (V_m I_n \cos\theta_n - V_n I_m \cos\theta_m)^2 \end{aligned} \tag{4.50}$$

When: h = Corresponding harmonic orders.

m, n = Non corresponding harmonic orders ($m \neq n$).

V_m, V_n : Harmonic voltage, I_m, I_n : Harmonic current.

θ_m, θ_n : Phase shift between corresponding voltage and current waveforms of harmonic orders.

$$\therefore (\sum_{h=1} V_h I_h \cos\theta_h)^2 = (V_1^2 + \sum_{n=1} V_n^2)(I_1^2 \cos^2\theta_1 + \sum_{n=1} I_n^2 \cos^2\theta_n)$$
$$-\frac{1}{2}\sum_{m=1}\sum_{n=1,n\neq m} (V_m I_n \cos\theta_n)^2 - (V_n I_m \cos\theta_m)^2 - 2(V_m V_n I_m \cos\theta_m I_n \cos\theta_n) \tag{4.51}$$

When : h = 1,2,3,4,5 , m = 1,2,3,4,5 & n = 1,2,3,4,5

$$(\sum_{h=1} V_h I_h \cos\theta_h)^2 = (V_1^2 + V_2^2 + V_3^2)(I_1^2 \cos^2\theta_1 + I_2^2 \cos^2\theta_2 + I_3^2 \cos^2\theta_3)$$
$$-\frac{1}{2}\sum_{m=1}\sum_{n=1,n\neq m} (V_m I_n \cos\theta_n)^2 - (V_n I_m \cos\theta_m)^2 - 2V_m I_m \cos\theta_m V_n I_n \cos\theta_n \tag{4.52}$$

After further steps of mathematical simplification, the above equation 4.52 can be represented as the following equation:

$$(\sum_{h=1} P_h)^2 = \sum_{h=1}(P_h)^2 + 2\Big(P_1P_2 + P_1P_3 + P_1P_4 + P_1P_5 + P_2P_3 + P_2P_4 + P_2P_5 + P_3P_4 + P_3P_5 + P_4P_5\Big) \tag{4.53}$$

The algebraic relation between arithmetical and geometrical sum is shown as:

$$(\sum_{h=1} P_h)^2 = \sum_{h=1}(P_h)^2 + 2\sum_{m=1}\sum_{n=1,n\neq m} P_m P_n \tag{4.54}$$

When : $P_h = V_h I_h \cos\theta_h$

$P_m = V_m I_m \cos\theta_m$ & $P_n = V_n I_n \cos\theta_n$

$$\therefore \sum_{h=1}(P_h)^2 = (\sum_{h=1} P_h)^2 - 2\sum_{m=1}\sum_{n=1,n\neq m} P_m P_n \tag{4.55}$$

$P_{ef}^2 = \sum_{h=1}(P_h)^2$ is the geometrical sum of active power in all orders.

$P_{avg}^2 = (\sum_{h=1} P_h)^2$ is the square of arithmetic sum of active power in all orders.

4.7 Evidence Examples

This section presents some examples of simple electrical circuits in order to investigate and prove the orthogonality law and the validity of RAPT Diagram.

1. **Example 1**: In this example, randomly chosen values has been applied in order to examine the validity of the newly proposed RAPT Diagram:

   Let: $P_1 = 10$ & $Q_1 = 5 \Rightarrow\therefore S_1 = 11.18$ (equation 4.35)

   Let: $P_h = 2, \because P_1 = 10 \Rightarrow\therefore P_{ef} = 10.2$ (from equation 4.46)

   Let: $D_h = 1, \because Q_1 = 5 \Rightarrow\therefore Q_{ef} = 5.1$ (from equation 4.47)

   $\because P_h = 2$ & $D_h = 1 \Rightarrow\therefore S_N = 2.236$ (from equation 4.36)

   $\because S_1 = 11.18$ & $S_N = 2.236 \Rightarrow\therefore S_t = 11.4$ (from equation 4.34)

   $\because P_{ef} = 10.2$ & $Q_{ef} = 5.1 \Rightarrow\therefore S_{ef} = S_t = 11.4$ (from equation 4.45)

   This example shows the coherence of the equations and the consistency of the values of power components through one diagram and prove the validity of the new RAPT Diagram.

2. The arithmetic sum Q_h can be equal to zero at nonzero values of terms Q_h despite the reciprocating energy transmission between the source and the load.

   Example 2: Suppose the circuit, shown in figure 4.3:

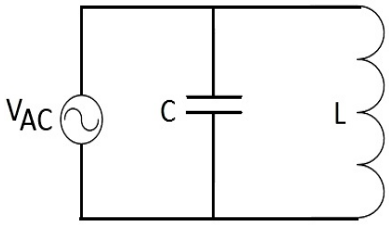


Figure 4.3: LC - circuit

The load has impedance Z_1 = j 20 in the fundamental component and for the 3rd order harmonic Z_3 = - j 1.25 , ω = 1 rad / sec . If the supply voltage is : $v(t) = (200 \sin wt + 50 \sin 3wt)V$

Then the load current is equal to :

$i(t) = [10 \sin(wt - 90) + 40 \sin(3wt + 90)]A.$

The arithmetic sum of reactive power is :

$Q_t = Q_1 + Q_3$ = 2000 - 2000 = 0 VAr

However, there is energy oscillation in this circuit and the total reactive power should be more than zero because instantaneous power P(t) has a negative part in figure 4.3 that's mean, the energy flows back to the source when it is negative and it causes losses in the transmission line.

While, the geometric sum is :

$Q_t = \sqrt{(2000)^2 + (2000)^2}$ = 2825.4 VAr

By using the geometric sum in reactive power calculation, its guaranteed to get a positive reactive power as long as there is reciprocating energy in the circuit.

3. **Example 3**: This following example has been proposed previously in [12] (pp. 36-38) : P_1 = 8660 w, P_3 = -13.94 w, P_5 = -11.78 w and P_7 = -1.74 w

   In order to test the validity of equation 4.55 and test the orthogonality among active power components:

$$\sum_{h=1}^{7} P_h^2 = P_1^2 + P_3^2 + P_5^2 + P_7^2 = 74995936.12W$$

$\therefore P_{ef} = \sqrt{P_h^2} = 8660.02$ watt = Geometrical sum

$$(\sum_{h=1}^{7} P_h)^2 = (P_1 + P_3 + P_5 + P_7)^2 = 74520746.85$$

$$P_{avg.} = \sum_{h=1}^{7} P_h = 8632.54w$$

$$\sum_{h=1}^{7} P_m P_n = 2(P_1P_3 + P_1P_5 + P_1P_7 + P_3P_5 + P_3P_7 + P_5P_7)$$

= -237594.64

From equation 4.55:

$$\sum_{h=1}(P_h)^2 = (\sum_{h=1} P_h)^2 - 2\sum_{m=1}\sum_{n=1,n\neq m} P_m P_n$$

$$\therefore \sum_{h=1}^{7}(P_h)^2 = 74520746.85 + 475189.28 = P_{ef}^2$$

$\therefore P_{ef} = 8660.02$ watt

This example proves the validity of equation 4.55.

The total value of apparent power which has been calculated in this example from this equation: $S_t^2 = S_1^2 + S_N^2$ was 10517.5 VA.

By applying equation 4.45, the power triangle should give the same result of S_{ef}^2. The geometric sum of P_t which is already $P_{rms} = P_{ef} = 8660.02$ W

In order to find Q_{ef} :

$Q_{ef} = \sqrt{Q_1^2 + Q_3^2 + Q_5^2 + Q_7^2 + D_I^2 + D_v^2 + D_{mn}^2}$

$Q_t = 5968$ VAr $= Q_{ef}$

From (equation 4.45): $S_t^2 = (5968)^2 + (8660.02)^2 \Rightarrow S_t = 10517.3 = S_{ef}$

However, the arithmetic sum of P_t is :

$P_t = P_1 + P_3 + P_5 + P_7 = 8632.54$ watt

If: $S_t = \sqrt{P_t^2 + Q_t^2} \Rightarrow then, \quad S_t = 10494.65$ VA

This value is different from S_t value resulted from $S_1^2 + S_N^2$ in the same example. Consequently, the arithmetic sum does not support the power triangle. Therefore, the new power terms are necessary to investigate the power triangles. IEEE-2010 standards are correct because they used the geometric sum for (S_t) calculation, but the power triangles could not be applied without using P_{ef} & Q_{ef} terms.

4.7.1 Conclusion of The New Power Diagram

This chapter presented two new power terms called effective active (P_{ef}) and effective reactive (Q_{ef}) power terms. These two terms are useful because they show the relationship between all power components (total, fundamental & distortion) in all power categories (S, P & Q) in non-sinusoidal system.

In addition, these two terms are useful to investigate and prove the ability to apply the principle of orthogonality law and the right-angled power triangle diagram. This diagram shows the orthogonality between fundamental and distorted components for all power categories (S, P and Q), considered as a bridge between time and frequency domains.

The right-angled power triangle is a compulsory condition to calculate the total apparent (S_t) in the non-sinusoidal system in the right way and its compatible with the equations of IEEE-2010 standards.

A comprehensive literature review has been presented in section II in order to justify the use of the geometric sum of power components. This section also, shows

that Budeanu's power definition has been refuted by a big number of valuable researchers and its no longer can be used.

This chapter also, offers a new definition for the apparent power as effective value (S_{ef}) at the non-sinusoidal situation and compares it with the previous power definitions which have serious limitations.

Moreover, this chapter shows a new power diagram representing all power components in a single diagram consisting of six right-angled triangles called the right-angled power triangle (RAPT) Diagram.

The notion of new power terms and new power right-angled power triangle (RAPT) Diagram, have the following interesting advantages:

1. The expressions and symbols which have been used in this chapter, are the same symbols and units have been used in IEEE standards-2010.

2. The vectors mentioned in the power diagram can be represented in phasor diagram.

3. The conventional units which used, are the traditional units (W, VAr and VA), thus no new power units have been added.

4. Defining the power components in two dimensional diagram without the need of sophisticated mathematical equations or three dimensional shapes as used before in Budeanu's theory.

5. Finally, proving the RAPT Diagram, investigates the right-angled power triangle (S-P-Q) which bases on the orthogonality principle between different components.

Chapter 5

Suggested Future Work

In order to develop this research and treat it's limitations, particularly the main three (2nd, 3rd & 4th) chapters, the following modification and improvements could be implemented in a future work:

5.1 Chapter 2

Regarding the utilizing of the distortion power as a load feeder and the ability to reduce the THD and improve PF for both sides (source and load), the single-phase passive filter method is the best approach because of its advantages on other circuits (according to the simulation results). However, this method still have some limitations and drawbacks. Therefore, the future optimization should focus on solving these limitations.

1. One of the limitations, is the unregulated output DC voltage of the bridge rectifier, which causes high ripple value and oscillation of the input value to the (VSI). This problem can be solved by adding DC/DC converter before the inverter, but the complexity, cost and the size of the design will be increased.

2. The bulky size, the large values of elements and using additional tools are another drawbacks of the proposed circuit in chapter 2. In order to avoid this problem, the newly proposed single-switch PFC (in chapter 3) can be the best choice to add after the passive filter instead of the utilization circuit, because of the small value of the inductor. This solution lead us to eliminate the voltage source inverter from the design and stick with the DC output and DC loads. Consequently, the design complexity, the number of parameters, the weight, the size and the cost may reduce.

5.2 Chapter 3

The main two problems of the proposed new PFC design in chapter 3, are the high spikes on the waveform of the input (I_S) and the high ripple factor value on the output waveform. In addition, minor effected problems can be exist like the small (I_o) values of inductor (as explained before in chapter 3). The internal capacitance of the diodes combines with stray inductance can form a resonant circuit called (parasitic resonant). Due to this parasitic resonance, a sinusoidal current can flow into the inductor (L) in a very high frequency (about 1.54 MHz) called self resonant frequency (or parasitic frequency (f_p)).

1. In order to solve the problem of high ripple values of the output voltage, A DC/DC converter can be added to the proposed PFC circuit in consistent with the two-stage approach.

2. The internal capacitance of the diodes combines with a stray inductance and forms a resonant circuit called parasitic resonant. Many methods are existing in order to attenuate this resonance, but most of them had some bad effects on the performance of the circuit like controlling the rising time (t_r) or the falling time (t_f) which reduces the power efficiency [218], or adding a

damper circuit or using clamping diodes and that requires additional components and add complexity to the design [219].

Practically, the damper circuit (R = 5Ω & C = 1 nF) can be connected in parallel with the freewheeling diode in order to eliminate the resonance current (I_0) totally, however, less than 0.1 % of total power can be increased as losses in the circuit as a circuit of 5 kW output power, has only 3 Watt losses in the damper circuit which is negligible.

5.3 Chapter 4

The old disputation among researchers about the meaning of power components and trying to find a general power definition and theory for both sinusoidal and non-sinusoidal systems never ends as every scientist claim that his theory is the ground breaker. Therefore, the suggestions of improving the proposed definition and RAPT Diagram will definitely continue by the future researchers until an optimum approach emerges.

Bibliography

[1] J. Das, *Power system harmonics and passive filter designs.* John Wiley & Sons, 2015.

[2] C. P. Steinmetz, "Does phase displacement occur in the current of electric arcs?" *ETZ*, vol. 587, 1892.

[3] E. Owen, "A history of harmonics in power systems," *Industry Applications Magazine, IEEE*, vol. 4, no. 1, pp. 6–12, Jan 1998.

[4] S.-I. Jang and K.-H. Kim, "An islanding detection method for distributed generations using voltage unbalance and total harmonic distortion of current," *Power Delivery, IEEE Transactions on*, vol. 19, no. 2, pp. 745–752, 2004.

[5] J. J. Toth and D. J. Velazquez, "Benefits of an automated on-line harmonic measurement system," *Industry Applications, IEEE Transactions on*, vol. IA-22, no. 5, pp. 952–963, Sept 1986.

[6] M. H. Rashid, *Power electronics: circuits, devices, and applications.* Pearson Education India, 2009.

[7] H. Azazi, E. El-Kholy, S. Mahmoud, and S. Shokralla, "Review of passive and active circuits for power factor correction in single phase, low power ac-dc converters," in *Proceedings of the 14th International Middle East Power Systems Conference (MEPCON'10)*, 2010, pp. 217–224.

[8] C. Budeanu, "Puissances réactives et fictives. institut romain de i'energte. bucharest," *Romania*, 1927.

[9] Y. Alhazmi, "Allocating power quality monitors in electrical distribution systems to measure and detect harmonics pollution," 2010.

[10] L. Cividino, "Power factor, harmonic distortion; causes, effects and considerations," in *Telecommunications Energy Conference, 1992. INTELEC '92., 14th International*, Oct 1992, pp. 506–513.

[11] E. W. Gunther, "Interharmonics in power systems," in *2001 Power Engineering Society Summer Meeting. Conference Proceedings (Cat. No.01CH37262)*, vol. 2, July 2001, pp. 813–817 vol.2.

[12] "Ieee standard definitions for the measurement of electric power quantities under sinusoidal, nonsinusoidal, balanced, or unbalanced conditions," *IEEE Std 1459-2010 (Revision of IEEE Std 1459-2000)*, pp. 1–50, March 2010.

[13] S. E. G. Mohamed and A. Y. Mohamed, "Study of load side harmonics sources effects and elimination," in *Zaytoonah University International Engineering Conference on Design and Innovation in Infrastructure 2012 (ZEC Infrastructure 2012)*, 2012, pp. 18–20.

[14] L. Czarnecki, "An overview of methods of harmonic suppression in distribution systems," in *Power Engineering Society Summer Meeting, 2000. IEEE*, vol. 2, 2000, pp. 800–805.

[15] C. Wang, J. Yang, and L. Wei, "Research on causes of harmonic currents and solitating problem," in *Electric Information and Control Engineering (ICEICE), 2011 International Conference on.* IEEE, 2011, pp. 2480–2483.

[16] W. M. Grady and S. Santoso, "Understanding power system hannonics," *Power Engineering Review, IEEE*, vol. 21, no. 11, pp. 8–11, Nov 2001.

[17] B. Acarkan and O. Kiliç, "Electrical harmonics modeling of office equipments using matlab and simulink."

[18] A. Zobaa, "Harmonic problems produced from the use of adjustable speed drives in industrial plants: case study," in *Harmonics and Quality of Power, 2004. 11th International Conference on*, Sept 2004, pp. 6–10.

[19] "The effects of power system harmonics on power system equipment and loads," *IEEE Transactions on Power Apparatus and Systems*, vol. PAS-104, no. 9, pp. 2555–2563, Sept 1985.

[20] V. Wagner, J. Balda, D. Griffith, A. McEachern, T. Barnes, D. Hartmann, D. Phileggi, A. Emannuel, W. Horton, W. Reid, R. Ferraro, and W. Jewell, "Effects of harmonics on equipment," *Power Delivery, IEEE Transactions on*, vol. 8, no. 2, pp. 672–680, Apr 1993.

[21] F. Lembo and V. D'Onofrio, "Distribution harmonics cause breaker problems," *Electrical World*, pp. 121–122, 1981.

[22] J. P. Brozek, "The effects of harmonics on overcurrent protection devices," in *Industry Applications Society Annual Meeting, 1990., Conference Record of the 1990 IEEE.* IEEE, 1990, pp. 1965–1967.

[23] D. E. Rice, "Adjustable speed drive and power rectifier harmonics-their effect on power systems components," *IEEE Transactions on Industry Applications*, vol. IA-22, no. 1, pp. 161–177, Jan 1986.

[24] A. A. Girgis, J. W. Nims, J. Jacomino, J. G. Dalton, and A. Bishop, "Effect of voltage harmonics on the operation of solid-state relays in industrial applications," *Industry Applications, IEEE Transactions on*, vol. 28, no. 5, pp. 1166–1173, 1992.

[25] E. Fuchs, D. Roesler, and K. Kovacs, "Sensitivity of electrical appliances to harmonics and fractional harmonics of the power system's voltage. part ii:

Television sets, induction watthour meters and universal machines," *Power Delivery, IEEE Transactions on*, vol. 2, no. 2, pp. 445–453, 1987.

[26] J. E. Kaufman, H. Haynes *et al.*, *IES lighting handbook; reference volume and application volume*, 1981.

[27] P. S. R. Committee, "The impact of sine-wave distortions on protective relays," *IEEE Transactions on Industry Applications*, vol. IA-20, no. 2, pp. 335–343, March 1984.

[28] W. F. Horton and S. Goldberg, "The effect of harmonics on the operating points of electromechanical relays," *IEEE Transactions on Power Apparatus and Systems*, vol. PAS-104, no. 5, pp. 1178–1188, May 1985.

[29] C. J. Erickson, "Motor design features for adjustable-frequency drives," *Industry Applications, IEEE Transactions on*, vol. 24, no. 2, pp. 192–198, 1988.

[30] J. Murphy and M. G. Egan, "A comparison of pwm strategies for inverter-fed induction motors," *Industry Applications, IEEE Transactions on*, no. 3, pp. 363–369, 1983.

[31] R. J. Belmans, D. Verdyck, W. Geysen, and R. D. Findlay, "Electromechanical analysis of the audible noise of an inverter-fed squirrel-cage induction motor," *Industry Applications, IEEE Transactions on*, vol. 27, no. 3, pp. 539–544, 1991.

[32] E. Fuchs, D. Roesler, and K. Kovacs, "Aging of electrical appliances due to harnmonics of the power system's voltage," *Power Delivery, IEEE Transactions on*, vol. 1, no. 3, pp. 301–307, 1986.

[33] A. Samra and K. Islam, "Harmonic effects on synchronous generators voltage regulation," in *Southeastcon '95. Visualize the Future., Proceedings., IEEE*, Mar 1995, pp. 376–380.

[34] S. E. G. Mohamed and A. Y. Mohamed, "Study of load side harmonics sources effects and elimination."

[35] J. Persson, "Comparing harmonics mitigation techniques," 2014.

[36] J. Rodriguez, J. Pontt, R. Huerta, and P. Newman, "24-pulse active front end rectifier with low switching frequency," in *Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual*, vol. 5. IEEE, 2004, pp. 3517–3523.

[37] A. Nassif, W. Xu, and W. Freitas, "An investigation on the selection of filter topologies for passive filter applications," *Power Delivery, IEEE Transactions on*, vol. 24, no. 3, pp. 1710–1718, July 2009.

[38] C. Arendse and G. Atkinson-Hope, "Design of a steinmetz symmetrizer and application in unbalanced network," in *Universities Power Engineering Conference (UPEC), 2010 45th International*, Aug 2010, pp. 1–6.

[39] K. M. Hink, "Harmonic mitigation of 12-pulse drives with unbalanced input line voltages," *MTE Corporation, W147*, no. 9525, 2002.

[40] Hink and K. M, "18-pulse drives and voltage unbalance," *MTE Corporation*, 2010.

[41] S. Kocman and V. Styskala, "Reduction of harmonics by 18-pulse rectifier," *Advances in Electrical and Electronic Engineering*, vol. 7, no. 1-2, pp. 137–139, 2011.

[42] J. Rodriguez, J. Pontt, R. Huerta, and P. Newman, "24-pulse active front end rectifier with low switching frequency," in *Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual*, vol. 5, June 2004, pp. 3517–3523 Vol.5.

[43] L. Wei, N. Guskov, R. Lukaszewski, and G. Skibinski, "Mitigation of current harmonics for multipulse diode front-end rectifier systems," *Industry Applications, IEEE Transactions on*, vol. 43, no. 3, pp. 787–797, May 2007.

[44] H. Sasaki and T. Machida, "A new method to eliminate ac harmonic currents by magnetic flux compensation-considerations on basic design," *Power Apparatus and Systems, IEEE Transactions on*, no. 5, pp. 2009–2019, 1971.

[45] P. P. Khera, "Application of zigzag transformers for reducing harmonics in the neutral conductor of low voltage distribution system," in *Industry Applications Society Annual Meeting, 1990., Conference Record of the 1990 IEEE*. IEEE, 1990, pp. 1092–vol.

[46] L. H. Beverly, R. D. Hance, A. L. Kristalinski, and A. T. Visser, "Method and apparatus for reducing the harmonic currents in alternating-current distribution networks," Nov. 19 1996, uS Patent 5,576,942.

[47] B. Wu, S. Rizzo, N. Zargari, and Y. Xiao, "An integrated dc link choke for elimination of motor common-mode voltage in medium voltage drives," in *Industry Applications Conference, 2001. Thirty-Sixth IAS Annual Meeting. Conference Record of the 2001 IEEE*, vol. 3, Sept 2001, pp. 2022–2027 vol.3.

[48] B. Bird, J. Marsh, and P. McLellan, "Harmonic reduction in multiplex convertors by triple-frequency current injection," *Electrical Engineers, Proceedings of the Institution of*, vol. 116, no. 10, pp. 1730–1734, 1969.

[49] S. Kim, P. Enjeti, P. Packebush, and I. Pitel, "A new approach to improve power factor and reduce harmonics in a three phase diode rectifier type utility interface," in *Industry Applications Society Annual Meeting, 1993., Conference Record of the 1993 IEEE*. IEEE, 1993, pp. 993–1000.

[50] B. M. Saied and H. I. Zynal, "Minimizing current distortion of a three-phase bridge rectifier based on line injection technique," *Power Electronics, IEEE Transactions on*, vol. 21, no. 6, pp. 1754–1761, 2006.

[51] J. Dixon, J. Contardo, and L. Moran, "A fuzzy-controlled active front-end rectifier with current harmonic filtering characteristics and minimum sensing variables," *Power Electronics, IEEE Transactions on*, vol. 14, no. 4, pp. 724–729, July 1999.

[52] J. Chiasson, L. M. Tolbert, K. McKenzie, and Z. Du, "A complete solution to the harmonic elimination problem," in *Applied Power Electronics Conference and Exposition, 2003. APEC'03. Eighteenth Annual IEEE*, vol. 1. IEEE, 2003, pp. 596–602.

[53] H. S. Patel and R. G. Hoft, "Generalized techniques of harmonic elimination and voltage control in thyristor inverters: Part i–harmonic elimination," *Industry Applications, IEEE Transactions on*, no. 3, pp. 310–317, 1973.

[54] N. Mohan and T. M. Undeland, *Power electronics: converters, applications, and design.* John Wiley & Sons, 2007.

[55] M. Tostes, U. Bezerra, R. Silva, J. Valente, C. de Moura, and T. Branco, "Impacts over the distribution grid from the adoption of distributed harmonic filters on low-voltage customers," *Power Delivery, IEEE Transactions on*, vol. 20, no. 1, pp. 384–389, Jan 2005.

[56] T. Sekar and B. Rabi, "A review and study of harmonic mitigation techniques," in *Emerging Trends in Electrical Engineering and Energy Management (ICETEEEM), 2012 International Conference on*, Dec 2012, pp. 93–97.

[57] L. Chen, Y. Xie, and Z. Zhang, "Comparison of hybrid active power filter topologies and principles," in *Electrical Machines and Systems, 2008. ICEMS 2008. International Conference on.* IEEE, 2008, pp. 2030–2035.

[58] L. Gyugyi and E. C. Strycula, "Active ac power filters," in *Proc. IEEE/IAS Annu. Meeting*, vol. 19, 1976, pp. 529–535.

[59] B. Singh, K. Al-Haddad, and A. Chandra, "A review of active filters for power quality improvement," *Industrial Electronics, IEEE Transactions on*, vol. 46, no. 5, pp. 960–971, Oct 1999.

[60] P. Enjeti, W. Shireen, and I. Pitel, "Analysis and design of an active power filter to cancel harmonic currents in low voltage electric power distribution systems," in *Industrial Electronics, Control, Instrumentation, and Automation, 1992. Power Electronics and Motion Control., Proceedings of the 1992 International Conference on*, Nov 1992, pp. 368–373 vol.1.

[61] B. Singh, V. Verma, A. Chandra, and K. Al-Haddad, "Hybrid filters for power quality improvement," *Generation, Transmission and Distribution, IEE Proceedings-*, vol. 152, no. 3, pp. 365–378, May 2005.

[62] M. El-Habrouk, "A new configuration for shunt active power filters," Ph.D. dissertation, Brunel University, 1998.

[63] M. Basu, S. P. Das, and G. K. Dubey, "Comparative evaluation of two models of upqc for suitable interface to enhance power quality," *Electric Power Systems Research*, vol. 77, no. 7, pp. 821–830, 2007.

[64] H. Fujita and H. Akagi, "The unified power quality conditioner: the integration of series and shunt-active filters," *Power Electronics, IEEE Transactions on*, vol. 13, no. 2, pp. 315–322, 1998.

[65] C. B. Aiken, "Two-mesh tuned coupled circuit filters," *Proceedings of the Institute of Radio Engineers*, vol. 25, no. 2, pp. 230–272, Feb 1937.

[66] F. Z. Peng, "Harmonic sources and filtering approaches," *IEEE Industry Applications Magazine*, vol. 7, no. 4, pp. 18–25, Jul 2001.

[67] Y.-W. Wang, M.-C. Wong, and C.-S. Lam, "Historical review of parallel hybrid active power filter for power quality improvement," in *TENCON 2015 - 2015 IEEE Region 10 Conference*, Nov 2015, pp. 1–6.

[68] M. Takeda, K. Ikeda, A. Teramoto, and T. Aritsuka, "Harmonic current and reactive power compensation with an active filter," in *Power Electronics Specialists Conference, 1988. PESC'88 Record., 19th Annual IEEE.* IEEE, 1988, pp. 1174–1179.

[69] F. Z. Peng, H. Akagi, and A. Nabae, "A new approach to harmonic compensation in power systems-a combined system of shunt passive and series active filters," *Industry Applications, IEEE Transactions on*, vol. 26, no. 6, pp. 983–990, 1990.

[70] F. Z. Peng, "Application issues of active power filters," *Industry Applications Magazine, IEEE*, vol. 4, no. 5, pp. 21–30, 1998.

[71] J.-C. Wu, H.-L. Jou, Y.-T. Feng, W.-P. Hsu, M.-S. Huang, and W.-J. Hou, "Novel circuit topology for three-phase active power filter," *Power Delivery, IEEE Transactions on*, vol. 22, no. 1, pp. 444–449, 2007.

[72] T. Demirdelen, M. Inci, K. C. Bayindir, and M. Tumay, "Review of hybrid active power filter topologies and controllers," in *Power Engineering, Energy and Electrical Drives (POWERENG), 2013 Fourth International Conference on.* IEEE, 2013, pp. 587–592.

[73] A. Nakajima, K. Oku, J. Nishidai, T. Shiraishi, Y. Ogihara, K. Mizuki, and M. Kumazawa, "Development of active filter with series resonant circuit," in *Power Electronics Specialists Conference, 1988. PESC '88 Record., 19th Annual IEEE*, April 1988, pp. 1168–1173 vol.2.

[74] V. Khadkikar, "Enhancing electric power quality using upqc: A comprehensive overview," *IEEE Transactions on Power Electronics*, vol. 27, no. 5, pp. 2284–2297, May 2012.

[75] K. W. Lao, M. C. Wong, N. Dai, C. K. Wong, and C. S. Lam, "A systematic approach to hybrid railway power conditioner design with harmonic compen-

sation for high-speed railway," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 2, pp. 930–942, Feb 2015.

[76] K. N. B. M. Hasan, K. Rauma, A. Luna, J. I. Candela, and P. RodrÃguez, "Harmonic compensation analysis in offshore wind power plants using hybrid filters," *IEEE Transactions on Industry Applications*, vol. 50, no. 3, pp. 2050–2060, May 2014.

[77] A. Blorfan, P. Wira, D. Flieller, G. Sturtzer, and J. MercklÃ©, "A three-phase hybrid active power filter with photovoltaic generation and hysteresis current control," in *IECON 2011 - 37th Annual Conference of the IEEE Industrial Electronics Society*, Nov 2011, pp. 4316–4321.

[78] A. F. Zobaa, "Optimal multiobjective design of hybrid active power filters considering a distorted environment," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 1, pp. 107–114, Jan 2014.

[79] W. H. Choi, C. S. Lam, M. C. Wong, and Y. D. Han, "Analysis of dc-link voltage controls in three-phase four-wire hybrid active power filters," *IEEE Transactions on Power Electronics*, vol. 28, no. 5, pp. 2180–2191, May 2013.

[80] M. El-Habrouk, M. Darwish, and P. Mehta, "Active power filters: A review," *IEE Proceedings-Electric Power Applications*, vol. 147, no. 5, pp. 403–413, 2000.

[81] H. Akagi, "Active harmonic filters," *Proceedings of the IEEE*, vol. 93, no. 12, pp. 2128–2141, Dec 2005.

[82] S. Rahmani, A. Hamadi, and K. Al-Haddad, "A comprehensive analysis of hybrid active power filter for power quality enhancement," in *IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society*, Oct 2012, pp. 6258–6267.

[83] N. Balbo, D. Sella, R. Penzo, G. Bisiach, D. Cappellieri, L. Malesani, and A. Zuccato, "Hybrid active filter for parallel harmonic compensation," in *1993 Fifth European Conference on Power Electronics and Applications*, Sept 1993, pp. 133–138 vol.8.

[84] J. Dixon, L. Moran, J. Rodriguez, and R. Domke, "Reactive power compensation technologies: State-of-the-art review," *Proceedings of the IEEE*, vol. 93, no. 12, pp. 2144–2164, Dec 2005.

[85] V. F. Corasaniti, M. B. Barbieri, P. L. Arnera, and M. I. Valla, "Hybrid power filter to enhance power quality in a medium-voltage distribution network," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 8, pp. 2885–2893, Aug 2009.

[86] C. A. Silva, L. A. Cordova, P. Lezana, and L. Empringham, "Implementation and control of a hybrid multilevel converter with floating dc links for current waveform improvement," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 6, pp. 2304–2312, June 2011.

[87] A. Luo, S. Peng, C. Wu, J. Wu, and Z. Shuai, "Power electronic hybrid system for load balancing compensation and frequency-selective harmonic suppression," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 2, pp. 723–732, Feb 2012.

[88] S. Fukuda and T. Endoh, "Control method for a combined active filter system employing a current source converter and a high pass filter," *IEEE Transactions on Industry Applications*, vol. 31, no. 3, pp. 590–597, May 1995.

[89] A. Bhattacharya, C. Chakraborty, and S. Bhattacharya, "Parallel-connected shunt hybrid active power filters operating at different switching frequencies for improved performance," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 11, pp. 4007–4019, Nov 2012.

[90] M. Rastogi, R. Naik, and N. Mohan, "A comparative evaluation of harmonic reduction techniques in three-phase utility interface of power electronic loads," *IEEE Transactions on Industry Applications*, vol. 30, no. 5, pp. 1149–1155, Sep 1994.

[91] S. Srianthumrong and H. Akagi, "A medium-voltage transformerless ac/dc power conversion system consisting of a diode rectifier and a shunt hybrid filter," *IEEE Transactions on Industry Applications*, vol. 39, no. 3, pp. 874–882, May 2003.

[92] S. Kim and P. N. Enjeti, "A new hybrid active power filter (apf) topology," *IEEE Transactions on Power Electronics*, vol. 17, no. 1, pp. 48–54, Jan 2002.

[93] S. Rahmani, A. Hamadi, K. Al-Haddad, and L. A. Dessaint, "A combination of shunt hybrid power filter and thyristor-controlled reactor for power quality," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 5, pp. 2152–2164, May 2014.

[94] S. Park, J.-H. Sung, and K. Nam, "A new parallel hybrid filter configuration minimizing active filter size," in *30th Annual IEEE Power Electronics Specialists Conference. Record. (Cat. No.99CH36321)*, vol. 1, Aug 1999, pp. 400–405 vol.1.

[95] A. Luo, C. Tang, Z. K. Shuai, W. Zhao, F. Rong, and K. Zhou, "A novel three-phase hybrid active power filter with a series resonance circuit tuned at the fundamental frequency," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 7, pp. 2431–2440, July 2009.

[96] C. L. Chen, C. E. Lin, and C. L. Huang, "An active filter for unbalanced three-phase system using synchronous detection method," in *Power Electronics Specialists Conference, PESC '94 Record., 25th Annual IEEE*, Jun 1994, pp. 1451–1455 vol.2.

[97] C. A. Quinn and N. Mohan, "Active filtering of harmonic currents in three-phase, four-wire systems with three-phase and single-phase nonlinear loads," in *Applied Power Electronics Conference and Exposition, 1992. APEC '92. Conference Proceedings 1992., Seventh Annual*, Feb 1992, pp. 829–836.

[98] A. Massoud, K. Ahmed, S. Finney, and B. Williams, "Harmonic distortion-based island detection technique for inverter-based distributed generation," *Renewable Power Generation, IET*, vol. 3, no. 4, pp. 493–507, 2009.

[99] "Ieee standard conformance test procedures for equipment interconnecting distributed resources with electric power systems," *IEEE Std 1547.1-2005*, pp. 1–62, July 2005.

[100] V. Sule and A. Kwasinski, "Active anti-islanding method based on harmonic content detection from overmodulating inverters," in *Applied Power Electronics Conference and Exposition (APEC), 2011 Twenty-Sixth Annual IEEE*. IEEE, 2011, pp. 637–644.

[101] Z. Yuan, S. de Haan, J. Ferreira, and D. Cvoric, "A facts device: Distributed power-flow controller (dpfc)," *Power Electronics, IEEE Transactions on*, vol. 25, no. 10, pp. 2564–2572, Oct 2010.

[102] M. G. Ujwala and K. R. Reddy, "Mitigation of voltage sag and swell for power quality improvement using distributed power flow controller."

[103] A. Iqbal, E. Levi, M. Jones, and S. Vukosavic, "Generalised sinusoidal pwm with harmonic injection for multi-phase vsis," in *Power Electronics Specialists Conference, 2006. PESC'06. 37th IEEE*. IEEE, 2006, pp. 1–7.

[104] J. Jose, G. Goyal, and M. Aware, "Improved inverter utilisation using third harmonic injection," in *Power Electronics, Drives and Energy Systems (PEDES) & 2010 Power India, 2010 Joint International Conference on*. IEEE, 2010, pp. 1–6.

[105] D. Grant, "Technique for pulse dropping in pulse-width modulated inverters," in *IEE Proceedings B (Electric Power Applications)*, vol. 128, no. 1. IET, 1981, pp. 67–72.

[106] J. Boys and S. Walton, "A loss minimised sinusoidal pwm inverter," in *IEE Proceedings B (Electric Power Applications)*, vol. 132, no. 5. IET, 1985, pp. 260–268.

[107] T. Blooming and D. Carnovale, "Application of ieee std 519-1992 harmonic limits," in *Pulp and Paper Industry Technical Conference, 2006. Conference Record of Annual*, June 2006, pp. 1–9.

[108] M.-Y. Chan, K. K. Lee, and M. W. Fung, "A case study survey of harmonic currents generated from a computer centre in an office building," *Architectural Science Review*, vol. 50, no. 3, pp. 274–280, 2007.

[109] M. J. H. Rawa, D. W. P. Thomas, and M. Sumner, "Background voltage distortion and percentage of nonlinear load impacts on the harmonics produced by a group of personal computers," in *2014 International Symposium on Electromagnetic Compatibility*, Sept 2014, pp. 626–630.

[110] A. Mansoor, W. M. Grady, A. H. Chowdhury, and M. J. Samotyi, "An investigation of harmonics attenuation and diversity among distributed single-phase power electronic loads," *IEEE Transactions on Power Delivery*, vol. 10, no. 1, pp. 467–473, Jan 1995.

[111] S. Hansen, P. Nielsen, and F. Blaabjerg, "Harmonic cancellation by mixing nonlinear single-phase and three-phase loads," *IEEE Transactions on Industry Applications*, vol. 36, no. 1, pp. 152–159, Jan 2000.

[112] W. M. Grady, A. Mansoor, E. F. Fuchs, P. Verde, and M. Doyle, "Estimating the net harmonic currents produced by selected distributed single-phase loads: computers, televisions, and incandescent light dimmers," in *2002*

IEEE Power Engineering Society Winter Meeting. Conference Proceedings (Cat. No.02CH37309), vol. 2, 2002, pp. 1090–1094 vol.2.

[113] M. J. H. Rawa, D. W. P. Thomas, M. Sumner, and J. X. Chin, "Source voltage, frequency and impedance variation effects on the harmonics generated from a personal computer," in *6th IET International Conference on Power Electronics, Machines and Drives (PEMD 2012)*, March 2012, pp. 1–6.

[114] M. J. H. Rawa, D. W. P. Thomas, and M. Sumner, "Harmonics attenuation of nonlinear loads due to linear loads," in *2012 Asia-Pacific Symposium on Electromagnetic Compatibility*, May 2012, pp. 829–832.

[115] H. Akagi, E. H. Watanabe, and M. Aredes, *Instantaneous power theory and applications to power conditioning*. John Wiley & Sons, 2007, vol. 31.

[116] H. Akagi, Y. Kanazawa, and A. Nabae, "Instantaneous reactive power compensators comprising switching devices without energy storage components," *Industry Applications, IEEE Transactions on*, vol. IA-20, no. 3, pp. 625–630, May 1984.

[117] E. Clarke, *Circuit analysis of AC power systems*. Wiley, 1943, vol. 1.

[118] A. Plunkett, "A current-controlled pwm transistor inverter drive," in *Conf. Rec. IEEE-IAS Annu. Meeting*, 1979, pp. 785–792.

[119] B. K. Bose, "An adaptive hysteresis-band current control technique of a voltage-fed pwm inverter for machine drive system," in *Proceedings.14 Annual Conference of Industrial Electronics Society*, vol. 3, Oct 1988, pp. 684–690.

[120] H. Akagi, Y. Kanazawa, K. Fujita, and A. Nabae, "Generalized theory of instantaneous reactive power and its application," *Electrical engineering in Japan*, vol. 103, no. 4, pp. 58–66, 1983.

[121] E. Clarke, *Circuit Analysis of AC Power Systems.* J. Wiley & sons, Incorporated, 1950, vol. 2.

[122] J. Zeng, L. Jiao, Y. Ni, S. Chen, B. Zhang, C. Shen, and F. Wu, "A novel hysteresis current controller for active power filter with constant switching frequency," in *Power Electronics and Motion Control Conference, 2000. Proceedings. IPEMC 2000. The Third International*, vol. 2, 2000, pp. 692–697 vol.2.

[123] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of single-phase improved power quality ac-dc converters," *IEEE Transactions on Industrial Electronics*, vol. 50, no. 5, pp. 962–981, 2003.

[124] J. P. M. Figueiredo, F. L. Tofoli, and B. L. A. Silva, "A review of single-phase pfc topologies based on the boost converter," in *Industry Applications (INDUSCON), 2010 9th IEEE/IAS International Conference on*, Nov 2010, pp. 1–6.

[125] Y. Chen, "Digital implementation of current-mode control for power factor correction," Ph.D. dissertation, Auburn University, 2015.

[126] V. Grigore *et al.*, *Topological issues in single-phase power factor correction.* Helsinki University of Technology, 2001.

[127] J. Jalade, J. Marpinard, and M. Valentin, "Large signal design of a· buck convert. er for high power dc-ac conversion," *PESC-80, Atlanta, Georgia*, 1980.

[128] R. D. Middlebrook, "A continuous model for the tapped-inductor boost converter," in *1975 IEEE Power Electronics Specialists Conference*, June 1975, pp. 63–79.

[129] S. Rahman and F. C. Lee, "Nonlinear program based optimization of boost and buck-boost converter designs," in *1981 IEEE Power Electronics Specialists Conference*, June 1981, pp. 180–191.

[130] C. Van Velthooven and W. Hetterscheid, *The Forward and Double Forward Converter*. Philips Electronic Components and Materials, 1977.

[131] P. W. Clarke, "Converter regulation by controlled conduction overlap," Feb. 10 1976, uS Patent 3,938,024.

[132] U. Moriconi, "A bridgeless pfc configuration based on l4981 pfc controller," *Application Note AN*, vol. 1606, pp. 18–18, 2002.

[133] C. J. Wu, F. C. Lee, S. Balachandran, and H. L. Goin, "Design optimization for a half-bridge dc-dc converter," in *1980 IEEE Power Electronics Specialists Conference*, June 1980, pp. 57–67.

[134] I. Barbi and W. C. P. A. Filho, "A nonresonant zero-voltage switching pulse-width modulated full-bridge dc-to-dc converter," in *Industrial Electronics Society, 1990. IECON '90., 16th Annual Conference of IEEE*, Nov 1990, pp. 1051–1056 vol.2.

[135] F. E. Lukens, "Linearization of the pulse width modulated converter," in *1974 IEEE Power Electronics Specialists Conference*, June 1974, pp. 265–273.

[136] F. C. Schwarz, "A method of resonant current pulse modulation for power converters," *IEEE Transactions on Industrial Electronics and Control Instrumentation*, vol. IECI-17, no. 3, pp. 209–221, May 1970.

[137] H. Owen, T. Wilson, S. Feng, and F. Lee, "A computer-aided design procedure for flyback step-up dc-to-dc converters," *IEEE Transactions on Magnetics*, vol. 8, no. 3, pp. 289–291, Sep 1972.

[138] R. Massey and E. Snyder, "High voltage single-ended dc-dc converter," in *Power Electronics Specialists Conference, 1977 IEEE.* IEEE, 1977, pp. 156–159.

[139] S. Cuk and R. D. Middlebrook, "A new optimum topology switching dc-to-dc converter," in *1977 IEEE Power Electronics Specialists Conference*, June 1977, pp. 160–179.

[140] D. Martins, G. de Abreu, and I. Barbi, "Zeta-gepae pwm isolated dc/dc converter analysis," in *Proceedings of 1 COBEP'91 (Brazilian Power Electronics Conference)*, pp. 154–159.

[141] D. Martins and G. De Abreu, "Application of the zeta converter in switch-mode power supplies," in *Applied Power Electronics Conference and Exposition, 1993. APEC'93. Conference Proceedings 1993., Eighth Annual.* IEEE, 1993, pp. 214–220.

[142] D. D. C. Pereira, M. R. Da Silva, E. M. Silva, and F. L. Tofoli, "Comprehensive review of high power factor ac-dc boost converters for pfc applications," *International Journal of Electronics*, vol. 102, no. 8, pp. 1361–1381, 2015.

[143] M. M. Jovanovic and Y. Jang, "State-of-the-art, single-phase, active power-factor-correction techniques for high-power applications-an overview," *IEEE Transactions on Industrial Electronics*, vol. 52, no. 3, pp. 701–708, 2005.

[144] R. Martinez and P. N. Enjeti, "A high-performance single-phase rectifier with input power factor correction," *IEEE Transactions on Power Electronics*, vol. 11, no. 2, pp. 311–317, 1996.

[145] J.-W. Lim and B.-H. Kwon, "A power-factor controller for single-phase pwm rectifiers," *IEEE Transactions on Industrial Electronics*, vol. 46, no. 5, pp. 1035–1037, Oct 1999.

[146] B. A. Miwa, D. M. Otten, and M. E. Schlecht, "High efficiency power factor correction using interleaving techniques," in *Applied Power Electronics Conference and Exposition, 1992. APEC '92. Conference Proceedings 1992., Seventh Annual*, Feb 1992, pp. 557–568.

[147] B.-R. Lin and H.-H. Lu, "Single-phase three-level pwm rectifier," in *Power Electronics and Drive Systems, 1999. PEDS'99. Proceedings of the IEEE 1999 International Conference on*, vol. 1. IEEE, 1999, pp. 63–68.

[148] R. Srinivasan and R. Oruganti, "A unity power factor converter using half-bridge boost topology," *IEEE Transactions on Power Electronics*, vol. 13, no. 3, pp. 487–500, 1998.

[149] D. K. Jackson and S. B. Leeb, "A power factor corrector with bidirectional power transfer capability," in *Power Electronics Specialists Conference, 2000. PESC 00. 2000 IEEE 31st Annual*, vol. 1. IEEE, 2000, pp. 365–370.

[150] R. Da Camara, C. Cruz, and R. Torrico-Bascopé, "Generation of a multilevel multi-state t type switching cell," *Proceedings of PCIM South America, Saõ Paulo*, pp. 1–10, 2012.

[151] D. J. S. Newlin, R. Ramalakshmi, and S. Rajasekaran, "A performance comparison of interleaved boost converter and conventional boost converter for renewable energy application," in *Green High Performance Computing (ICGHPC), 2013 IEEE International Conference on*. IEEE, 2013, pp. 1–6.

[152] O. García, J. A. Cobos, R. Prieto, P. Alou, and J. Uceda, "Single phase power factor correction: A survey," *IEEE Transactions on Power Electronics*, vol. 18, no. 3, pp. 749–755, 2003.

[153] J. Zhang, M. M. Jovanovic, and F. C. Lee, "Comparison between ccm single-stage and two-stage boost pfc converters," in *Applied Power Electron-*

ics Conference and Exposition, 1999. APEC'99. Fourteenth Annual, vol. 1. IEEE, 1999, pp. 335–341.

[154] L. Huber and M. M. Jovanovic, "Design optimization of single-stage single-switch input-current shapers," *IEEE Transactions on Power Electronics*, vol. 15, no. 1, pp. 174–184, Jan 2000.

[155] B. AKIN, "Comparison of conventional and interleaved pfc boost converters for fast and efficient charge of li-ion batteries used in electrical cars," in *International Conference on Power and Energy Systems*, vol. 13, 2012.

[156] H. Akagi, "Modern active filters and traditional passive filters," *Bulletin of the Polish Academy of sciences, Technical sciences*, vol. 54, no. 3, 2006.

[157] G. Ye, M. Babar, and J. F. G. Cobben, "Performance comparison of different filter applications in three-phase pfc rectifier," in *2014 14th International Conference on Environment and Electrical Engineering*, May 2014, pp. 437–442.

[158] T. B. Soeiro, T. Friedli, and J. W. Kolar, "Design and implementation of a three-phase buck-type third harmonic current injection pfc rectifier sr," *IEEE Transactions on Power Electronics*, vol. 28, no. 4, pp. 1608–1621, April 2013.

[159] S. Al-Zubaidi, M. Ahmed, and P. Davey, "Design of single bidirectional switch single phase rectifier with reduced size dc side capacitor," in *Future Energy Electronics Conference (IFEEC), 2013 1st International*, Nov 2013, pp. 18–23.

[160] W. M. Grady and R. J. Gilleskie, "Harmonics and how they relate to power factor," *Proceedings of PQA93*, 1993.

[161] M. T. Zhang, Y. Jiang, F. C. Lee, and M. M. Jovanovic, "Single-phase three-level boost power factor correction converter," in *Applied Power Electronics*

Conference and Exposition, 1995. APEC '95. Conference Proceedings 1995., Tenth Annual, no. 0, Mar 1995, pp. 434–439 vol.1.

[162] A. Isaacs, "Simulation technology: The evolution of the power system network [history]," *IEEE Power and Energy Magazine*, vol. 15, no. 4, pp. 88–102, July 2017.

[163] M. J. H. Rawa, D. W. P. Thomas, and M. Sumner, "Experimental measurements and computer simulations of fl and cfl for harmonic studies," in *2014 UKSim-AMSS 16th International Conference on Computer Modelling and Simulation*, March 2014, pp. 335–339.

[164] D. W. P. T. M. J. H. Rawa and M. Sumner, "Power quality monitoring and simulation of a personal computer based on ieee 1459," in *2013 International Symposium on Electromagnetic Compatibility*, Sept 2013, pp. 671–675.

[165] H. Yanan, B. Liangeng, Z. Bin, Z. Yuanyuan, and H. Bin, "Analysis between simulation and measurement of commissioning tests on uhv system," in *2016 IEEE International Conference on Power System Technology (POWERCON)*, Sept 2016, pp. 1–5.

[166] F. Boukazouha, M. L. Tadjine, and M. Rguiti, "A longitudinal p191 single ceramic piezoelectric transformer: Comparison between 3d simulations and experimental results," in *2016 4th International Conference on Control Engineering Information Technology (CEIT)*, Dec 2016, pp. 1–4.

[167] M. A. Heidari, M. Jafari, and Z. Malekjamshidi, "Simulation and implementation of a 300 watt, cascade gama-lc resonant converter," in *2012 3rd Power Electronics and Drive Systems Technology (PEDSTC)*, Feb 2012, pp. 187–192.

[168] M. Ishizuka, S. Nakagawa, T. Hatakeyama, and Y. Nishino, "Comparison between experimental results and cfd simulations for air flows in a thin

electronics casing model," in *2010 12th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems*, June 2010, pp. 1–5.

[169] E. Bielejec, G. Vizkelethy, R. M. Fleming, W. R. Wampler, S. M. Myers, and D. B. King, "Comparison between experimental and simulation results for ion beam and neutron irradiations in silicon bipolar junction transistors," *IEEE Transactions on Nuclear Science*, vol. 55, no. 6, pp. 3055–3059, Dec 2008.

[170] C. Baudier and R. Dusseaux, "Scattering by rough surfaces: comparison between simulations and experimental radar data," in *IGARSS 2003. 2003 IEEE International Geoscience and Remote Sensing Symposium. Proceedings (IEEE Cat. No.03CH37477)*, vol. 1, July 2003, pp. 133–135 vol.1.

[171] C. P. Steinmetz and J. L. R. Hayden, *Steinmetz Electrical Engineering Library: Theory and calculation of alternating current phenomena (1916)*. McGraw-Hill, 1916, vol. 4.

[172] W. Shepherd and P. Zakikhani, "Suggested definition of reactive power for nonsinusoidal systems," *Electrical Engineers, Proceedings of the Institution of*, vol. 119, no. 9, pp. 1361–1362, 1972.

[173] L. S. Czarnecki, "Currents' physical components (cpc) in circuits with nonsinusoidal voltages and currents. part 1, single-phase linear circuits," *Electrical Power Quality and Utilisation. Journal*, vol. 11, no. 2, pp. 3–14, 2005.

[174] P. Filipski, "Apparent power-a misleading quantity in the non-sinusoidal power theory: Are all non-sinusoidal power theories doomed to fail?" *European Transactions on Electrical Power*, vol. 3, no. 1, pp. 21–26, 1993.

[175] M. Castro-Núñez, "The use of geometric algebra in the analysis of non-sinusoidal networks and the construction of a unified power theory for single

phase systems-a paradigm shift," Ph.D. dissertation, University of Calgary, 2013.

[176] L. S. Czarnecki, "Considerations on the reactive power in nonsinusoidal situations," *Instrumentation and Measurement, IEEE Transactions on*, vol. 1001, no. 3, pp. 399–404, 1985.

[177] Czarnecki and L. S, "What is wrong with the budeanu concept of reactive and distortion power and why it should be abandoned," *Instrumentation and Measurement, IEEE Transactions on*, vol. 1001, no. 3, pp. 834–837, 1987.

[178] P. S. Filipski and P. W. Labaj, "Evaluation of reactive power meters in the presence of high harmonic distortion," *IEEE Transactions on Power Delivery*, vol. 7, no. 4, pp. 1793–1799, Oct 1992.

[179] S. Svensson, *Power measurement techniques for nonsinusoidal conditions. The significance of harmonics for the measurement of power and other AC quantities.* Chalmers University of Technology, 1999.

[180] S. Fryze, "Active, reactive, and apparent power in non-sinusoidal systems," *Przeglad Elektrot*, vol. 7, pp. 193–203, 1931.

[181] L. Czarnecki, "Budeanu and fryze: Two frameworks for interpreting power properties of circuits with nonsinusoidal voltages and currents," *Electrical Engineering*, vol. 80, no. 6, pp. 359–367, 1997.

[182] D. Sharon, "Reactive-power definitions and power-factor improvement in nonlinear systems," *Electrical Engineers, Proceedings of the Institution of*, vol. 120, no. 6, pp. 704–706, 1973.

[183] N. Kusters and W. Moore, "On the definition of reactive power under nonsinusoidal conditions," *Power Apparatus and Systems, IEEE Transactions on*, no. 5, pp. 1845–1854, 1980.

[184] L. S. Czarnecki, "Considerations on the reactive power in nonsinusoidal situations," *Instrumentation and Measurement, IEEE Transactions on*, vol. 1001, no. 3, pp. 399–404, 1985.

[185] A. Nabae and T. Tanaka, "A new definition of instantaneous active-reactive current and power based on instantaneous space vectors on polar coordinates in three-phase circuits," *IEEE Transactions on Power Delivery*, vol. 11, no. 3, pp. 1238–1243, 1996.

[186] M. Depenbrock, "The fbd-method, a generally applicable tool for analyzing power relations," *IEEE Transactions on Power Systems*, vol. 8, no. 2, pp. 381–387, 1993.

[187] M. Slonim and J. Van Wyk, "Power components in a system with sinusoidal and nonsinusoidal voltages and/or currents," *Electric Power Applications, IEE Proceedings B*, vol. 135, no. 2, pp. 76–84, 1988.

[188] A. E. Emanuel, "Apparent power definitions for three-phase systems," *IEEE Transactions on Power Delivery*, vol. 14, no. 3, pp. 767–772, 1999.

[189] F. Z. Peng and J.-S. Lai, "Generalized instantaneous reactive power theory for three-phase power systems," *IEEE transactions on instrumentation and measurement*, vol. 45, no. 1, pp. 293–297, 1996.

[190] A. Ferrero and G. Superti-Furga, "A new approach to the definition of power components in three-phase systems under nonsinusoidal conditions," *IEEE Transactions on Instrumentation and Measurement*, vol. 40, no. 3, pp. 568–577, 1991.

[191] L. Rossetto and P. Tenti, "Evaluation of instantaneous power terms in multiphase systems: techniques and application to power-conditioning equipment," *International Transactions on Electrical Energy Systems*, vol. 4, no. 6, pp. 469–474, 1994.

[192] Y. Xu, L. Tolbert, J. Chiasson, J. Campbell, and F. Peng, "A generalised instantaneous non-active power theory for statcom," *IET Electric Power Applications*, vol. 1, no. 6, pp. 853–861, 2007.

[193] J. L. Willems, "A new interpretation of the akagi-nabae power components for nonsinusoidal three-phase situations," *IEEE Transactions on Instrumentation and Measurement*, vol. 41, no. 4, pp. 523–527, 1992.

[194] P. Filipski, "Polyphase apparent power and power factor under distorted waveform conditions," *IEEE transactions on power delivery*, vol. 6, no. 3, pp. 1161–1165, 1991.

[195] E. H. Watanabe, H. Akagi, and M. Aredes, "Instantaneous pq power theory for compensating nonsinusoidal systems," in *Nonsinusoidal Currents and Compensation, 2008. ISNCC 2008. International School on.* IEEE, 2008, pp. 1–10.

[196] F. Ghassemi, "New concept in ac power theory," *IEE Proceedings-Generation, Transmission and Distribution*, vol. 147, no. 6, pp. 417–424, 2000.

[197] N. LaWhite and M. D. Ilic, "Vector space decomposition of reactive power for periodic nonsinusoidal signals," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 44, no. 4, pp. 338–346, 1997.

[198] J. Cohen, F. De León, and L. M. Hernández, "Physical time domain representation of powers in linear and nonlinear electrical circuits," *IEEE Transactions on Power Delivery*, vol. 14, no. 4, pp. 1240–1249, 1999.

[199] H. Lev-Ari and A. M. Stankovic, "Defining reactive power in circuit transients via local fourier coefficients," in *Circuits and Systems, 2002. ISCAS 2002. IEEE International Symposium on*, vol. 5. IEEE, 2002, pp. V–V.

[200] M. T. Haque, "Single-phase pq theory," in *Power Electronics Specialists Conference, 2002. pesc 02. 2002 IEEE 33rd Annual*, vol. 4. IEEE, 2002, pp. 1815–1819.

[201] D. Zhang and N. Huang, "Universal instantaneous power theory for dc, single-phase ac sinusoidal and nonsinusoidal circuits," in *Power Electronics and Motion Control Conference, 2000. Proceedings. IPEMC 2000. The Third International*, vol. 3. IEEE, 2000, pp. 1442–1447.

[202] A. Menti, T. Zacharias, and J. Milias-Argitis, "Geometric algebra: A powerful tool for representing power under nonsinusoidal conditions," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 3, pp. 601–609, 2007.

[203] X. Dai, G. Liu, and R. Gretsch, "Generalized theory of instantaneous reactive quantity for multiphase power system," *IEEE Transactions on Power Delivery*, vol. 19, no. 3, pp. 965–972, 2004.

[204] J. Bravo, M. Castilla, J. Montaño, M. Ordoñez, M. Castillå, A. López, D. Borrás, and J. Gutiérrez, "Non-active power multivector," in *MELECON 2010-2010 15th IEEE Mediterranean Electrotechnical Conference*. IEEE, 2010, pp. 1021–1026.

[205] S.-K. Chen and G. W. Chang, "A new instantaneous power theory-based three-phase active power filter," in *Power Engineering Society Winter Meeting, 2000. IEEE*, vol. 4. IEEE, 2000, pp. 2687–2692.

[206] Czarnecki and L. S, "What is wrong with the budeanu concept of reactive and distortion power and why it should be abandoned," *Instrumentation and Measurement, IEEE Transactions on*, vol. 1001, no. 3, pp. 834–837, 1987.

[207] P. Filipski, "Apparent power-a misleading quantity in the non-sinusoidal power theory: Are all non-sinusoidal power theories doomed to fail?" *European Transactions on Electrical Power*, vol. 3, no. 1, pp. 21–26, 1993.

[208] P. Filipski, Y. Baghzouz, and M. Cox, "Discussion of power definitions contained in the ieee dictionary," *Power Delivery, IEEE Transactions on*, vol. 9, no. 3, pp. 1237–1244, 1994.

[209] A. E. Emanuel, *Power definitions and the physical mechanism of power flow*. John Wiley & Sons, 2011, vol. 22.

[210] J. Depenbrock, *Erwachaenen-Strafvollzug: die rechtlichen Grundlagen des Erwachsenen-Strafvollzuges und ihre Auswirkungen auf die ARbeit, das Wahlrecht und den Rechtsschutz des Strafangenen*. H. Bouvier, 1960, vol. 24.

[211] W. Shepherd and P. Zand, *Energy flow and power factor in nonsinusoidal circuits*. Cambridge University Press, 1979.

[212] R. Arseneau, Y. Baghzouz, J. Belanger, A. Braun, M. Cox, A. Emanuel, P. Filipski, E. Gunther, A. Girgis, D. Hartmann *et al.*, "Practical definitions for powers in systems with nonsinusoidal waveforms and unbalanced loads: a discussion," *Power Delivery, IEEE Transactions on*, vol. 11, no. 1, pp. 79–101, 1996.

[213] A. E. Emanuel, "Powers in nonsinusoidal situations-a review of definitions and physical meaning," *Power Delivery, IEEE Transactions on*, vol. 5, no. 3, pp. 1377–1389, 1990.

[214] J. Radatz, *The IEEE standard dictionary of electrical and electronics terms*. IEEE Standards Office, 1997.

[215] L. S. Czarnecki, "Misinterpretations of some power properties of electric circuits," *IEEE Transactions on Power Delivery*, vol. 9, no. 4, pp. 1760–1769, 1994.

[216] E. W. Weisstein, "Lagrange's identity," 2005.

[217] P. Pragacz and J. Ratajski, "Formulas for lagrangian and orthogonal degeneracy loci; the q-polynomials approach," *arXiv preprint alg-geom/9602019*, 1996.

[218] K. Kam, D. Pommerenke, F. Centola, C. Lam, and R. Steinfeld, "Method to suppress the parasitic resonance using parallel resistor and inductor combination to reduce broadband noise from dc/dc converter," in *EMC*, vol. 9, 2009, pp. 20–24.

[219] K. Harada and T. Ninomiya, "Optimum design of rc snubbers for switching regulators," *IEEE Transactions on Aerospace and Electronic Systems*, no. 2, pp. 209–218, 1979.

Appendix A

Published Papers

A.1 16th International Conference on Electrical and Power Engineering (ICEPE), September 2014, Germany

Title "A Novel Idea to Benefit of The Load Sides Harmonics"

A Novel Idea to Benefit of the Load Side's Harmonics

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***Abstract*—This paper presents a novel idea to show the ability to benefit of the harmonic currents which are produced on the load side of the power grid. The proposed circuit contributes in reduction of the total harmonic distortion (THD) percentage through adding a high pass filter (HPF) in order to draw harmonic currents (in 150 Hz and multiple frequencies) and convert them to DC current (zero frequency) and then reconvert it to AC current with the fundamental frequency in order to feed different loads. The circuit has been designed and simulated in the MATLAB, Simulink program. The results have been assessed and compared in two cases: firstly, the system before adding the new circuit. Secondly, the system after adding the new circuit.**

I. KEYWORDS

Harmonics Elimination, Passive Filters, Total Harmonic Distortion (THD)

II. INTRODUCTION

The problem of harmonics in the power system grid has been identified since 1893. It was the first time an electric application's problem has addressed using harmonic analysis as a tool, when distorted power was observed as a distorted voltage and current waveforms in the power grid [1]. In the past, the amount of distortion in power system has been non significant. However, the level of harmonic currents and voltages in the distribution power system is highly considerable nowadays, and grown to be a serious problem in the power grid [2].

According to [3], harmonics can be defined as a sinusoidal wave (current or voltage), having frequencies that are integer multiples of the frequency at which the supply system has designed to operate. Distorted waveforms can be produced by merging harmonics with the fundamental wave. Non-linear loads are the main reason of harmonic existence of the power system. As a result of current harmonics, non-linear voltage drops happened across the system impedance. The relationship between current and voltage waveforms, illustrate the meaning of (non-linear load) term, a non-linear load has a discrete current relationship that does not correspond to the applied voltage waveform. Because of the nature of the front end rectifier design is non-linear, all variable frequency devices cause non-linear waveforms, which are called harmonics. Typical examples of non-linear loads include rectifiers, TV's, Microwave oven, vapor mercury, adjustable speed motor drives, electric ballast, uninterruptable power supply (UPS) units, discharge lighting, halogen spot light, halogen with dimmer and arcing equipment [3].

As mentioned before, the power electronic apparatuses are the main sources of the harmonics, however the economic profits of using power electronic devices are much more observant than losses caused by harmonics which produced by these apparatuses. As a result of this growing, the harmonics generation rate extremely increased to be higher than its elimination rate in the distribution system [4].

The defects which are happening due to the effects of a three phase harmonics on circuits are alike to the defects happened in the human body due to stress and high blood pressure. High degrees of stress or harmonic distortion can lead to problems for the utility's power grid distribution, ineffective power system and many negative effects on the grid equipments such as, skin effect which increases with frequency, dielectric failure or breakdown the capacitor, false or fake operation and trips, destructing components, excessive overheating in the transformer windings, multiple zero crossings which change the timing of the voltage regulator and causes intervention, higher billings due to incorrect measurement records, failure of the commutation circuits of AC and DC drives [5].

There are different methods used to eliminate the harmonics from the power system, varied by changing the design of variable frequency drives (VFD) to adding new equipments to perform the same aim. They can be summarized as follows:

1) Delta connection: Steinmetz was the first who proposed delta connections for blocking third harmonic currents in three phase transformers [1].
2) Power system design: the non-linear load can be limited to 30 percent of the maximum transformer's capacity, and that's might be useful for harmonic ratio decreasing [2].
3) Twelve pulse converter front end: the bridge rectifier circuit uses twelve diodes instead of six. Theoretical input current harmonics for rectifier circuits are a function of pulse number and can be expressed as: $h = n \cdot p \mp 1$ where n= 1, 2, 3,... etc., and p = number of pulses, For a six - pulse rectifier, the input current will have harmonic components at the following multiples of the fundamental frequency. h = 5, 7, 11, 13, 17, 19, 23, 25,

29, 31,.. etc. For the twelve - pulse system, the input current will have theoretical harmonic components at the following multiples of the fundamental frequency: h = 11, 13, 23, 25, 35, 37,... etc. 12 - pulse converter eliminates the 5th and 7th harmonics. However, this method reduces the magnitude of the harmonics, but does not eliminate them. The drawbacks are cost and design which requires an auxiliary transformer to achieve the 30 degree phase shifting, also this design decreases the efficiency rating due to voltage drop associated with the design requirement [2].

4) Delta-Delta and Delta-Wye transformer: This method uses two separate transformers with equal non - linear loads. The design is similar to the previously mentioned 12 pulse converter circuit with the same drawbacks [6].
5) The magnetic flux compensation method: has been proposed to eliminate normal harmonics and abnormal harmonics in a transformer core [7].
6) A zigzag transformer: has been used for creating a neutral line, and reduces the heating effect of the harmonic current in three phase distribution system [8].
7) Line reactor: Both AC line reactors and DC link chokes help to smooth out the flow of current to Variable Frequency Drives (VFDs) and thereby reduce the level of harmonics [2].
8) Third harmonic injection technique: has been used in uncontrolled converters [9]. Third harmonic injection technique in the controlled converters, was first introduced in 1969, in order to reduce the harmonic currents at the source side [10].
9) Passive filters: This method has many advantages like simplicity, reliability, efficiency, and cost effective. However, these filters suffer of main drawback, which is the harmonic current's amplification on the source side at specific frequencies because of the parallel resonance between filter and source. The series resonance between filter and source may cause voltage distortion which creates extreme harmonic currents flowing through the filter [4].
10) Active filters: In order to conquer passive filters' problems, active filters were invented in 1976 by Gyugyi [11]. Active power filters (APF), have different topologies and multiple categories, but mostly use voltage source converters. APF has a voltage source at the DC bus, which is usually a capacitor, as an energy storage device. APF also, suffer from many problems which are the high initial costs and high running costs, need high power converter ratings, the input and output power rating is limited by the power supply voltages and always require a power for the active device [12].
11) Hybrid filter: Is a combination of passive filters with active filters. They are invented in order to gather all the advantages of two types of filters and overcome their limitations, however still the most expensive among them [12].

Previously, harmonics have often been cited as the source for a great variety of problems. Most of mentioned methods were invented in order to eliminate the harmonics and reduce their effects on the source side, but till now, at least to the author's knowledge, there is not any effective method to reduce these harmonics at the load side and convert it to useful AC power at the same time. Unfortunately, harmonics still present at the load side and the harmful power does not finish and still cause non-useful periodic waves which causes harmful effects on the costumer's equipments and effects power quality in general [13].

Firstly, the methodology has been presented and a schematic diagram has been designed, secondly, the circuit has been investigated and tested via Matlab-Simulink program, finally, the results have been assessed through comparing the data before and after adding the high pass filter.

III. System Description (Methodology)

A simplified schematic of the circuit is shown in the figure (1), the circuit consists of a three phase 11 Kv power generation source connected in series with (point 1) a three phase step down (11/0.4) KV transformer in Wye-Delta connection.

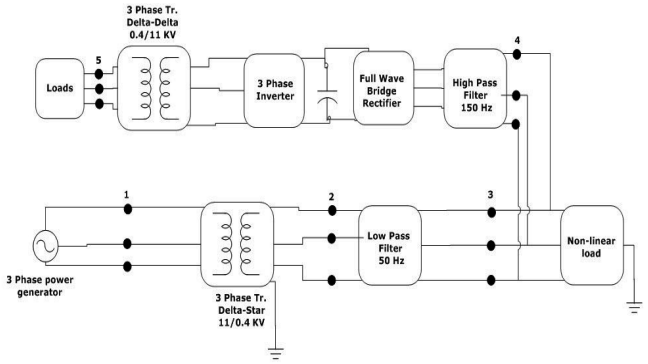

Fig. 1. Schematic diagram

This circuit also contains (point 2) a Low Pass Filter (LPF) in series with (point 3) a three phase non-linear load which produces harmonic currents, LPF passes the fundamental wave current 50 Hz and blocks all the frequencies above 50 Hz (which are forming the harmonics at the load side). A low impedance, high pass filter has been connected in parallel (point 4) to draw all the harmonic currents in 150 Hz and above. HPF has been connected in series with a three phase full wave bridge rectifier in order to convert AC currents in different frequencies to zero frequency DC current. The Next step, requires to convert the DC current to AC current on the fundamental frequency (50)Hz by connecting the three phase 6 - pulses inverter controlled by PWM technique in series with the circuit. Finally, in order to benefit from this new current, a three phase step up (0.4 / 11) KV transformer in Delta - Delta connection will be connected in series to raise the voltage and

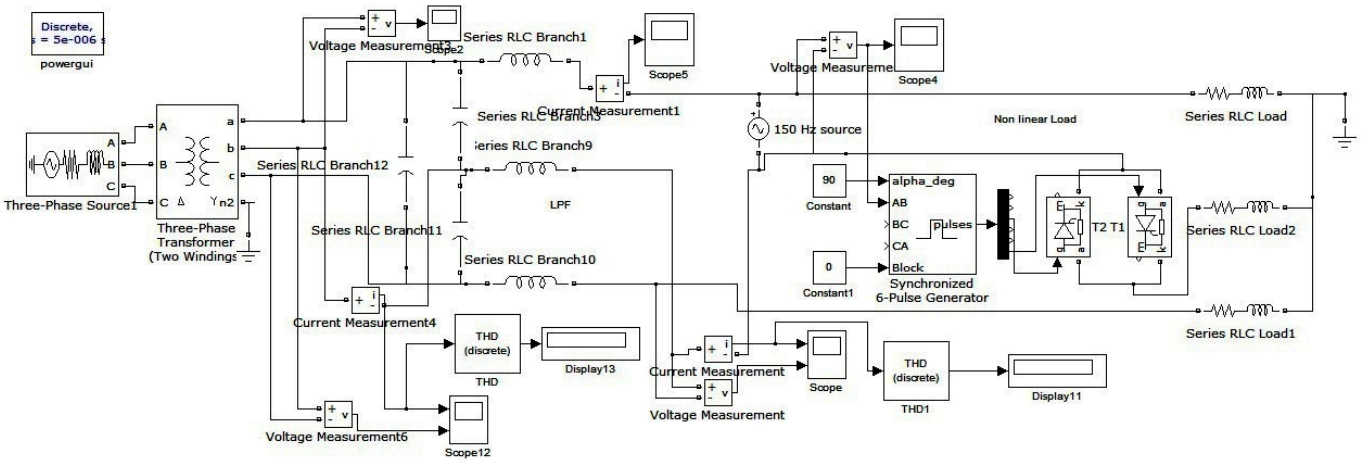

Fig. 2. Normal circuit without HPF

re-inject it to the generation side of the grid or use it as a normal power supply to feed different types of loads.

IV. Circuit design and simulation

An 11 Kv three phase voltage, 50 Hz generator has been chosen as a three phase power supply, Delta-Wye (11/0.4) Kv transformer is connected in series to decrease voltage to 400 volt as a line voltage. The non-linear load draws a non-linear current, consequently a drop voltage has been happening and an AC voltage in a multiple of 50 HZ frequency (with a majority of 150 Hz as a third harmonic waveform) has been produced on the load side. In order to represent the non-linear load on the circuit, an AC voltage source works on 150 Hz has been connected in series with a back to back thyristor (Alfa = 90) circuit has been connected as a non-linear load with three phases RL-load. A low pass filter (LPF) is connected between the transformer and the loads, an inductor (L) and a capacitor (C) values has been calculated according to this equation f=1/(2$\sqrt{LC}$), whereas (f) is the resonance frequency of the filter.

The low pass filter (LPF) permits the fundamental frequency waves to pass through the filter to the source side and blocks all other frequencies above 50 Hz. A high pass filter (HPF) has been connected in parallel between LPF and the loads. Using the same mentioned equation, HPF with 150 Hz resonance frequency, has to be designed as a low impedance (High capacitance and low inductance) filter in order to force the harmonic currents to follow through the HPF. Consequently, the harmonic currents will be eliminated and its effects on the load side will be reduced. In order to unify these eliminated harmonic currents which have different frequencies (the multiples of 50), A three phase - six diode full bridge rectifier has been connected in series with the HPF in order to convert these currents to DC current. The DC current can be stored in a capacitor and convert it to AC current in the fundamental frequency (50 HZ) by connecting a three phase six pulse inverter in series with the rectifier, consequently a useful power is produced at the end of the circuit. Finally, a Delta-Delta has been advised to connect with (0.4 / 11) turn ratio to increase the voltage and inject it to the source side of the distribution system or use it as a normal feeder to feed some auxiliaries or feed different kinds of loads.

V. DC voltage calculation

In the case of using three phase full wave bridge rectifier, six pulses has been occurring each cycle, that's meaning there is a pulse every 60 degrees in one full cycle. In order to calculate the DC voltage, the average voltage has to be calculated by using the following equation: $Vavg = \frac{6}{2\pi}\int_{\pi/3}^{2\pi/3} Vmax.\sin wt.dwt = 0.955Vmax = DCVoltage$

VI. Cases to study

The system has been tested twice (without extra circuit and with the extra circuit), the results and figures have been collected and classified to make a comparison between two cases in the following items :

1) First case: Normal circuit without connecting high pass filter (HPF) circuit, as shown below in figure 2.

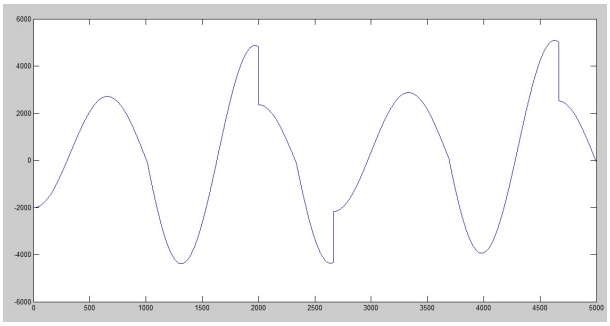

Fig. 3. Load Voltage without HPF

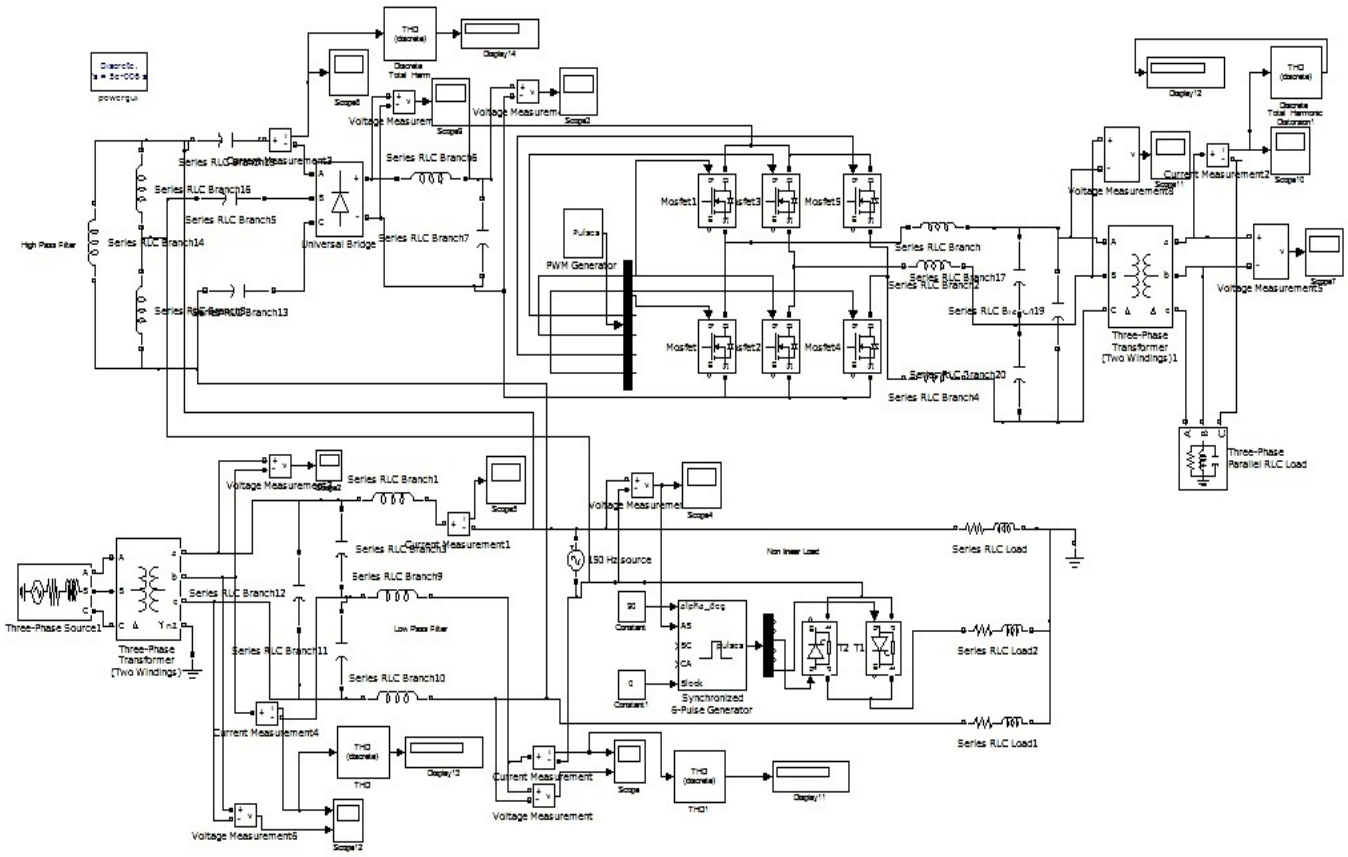

Fig. 4. Full circuit with HPF

Figure (3) shows the load voltage illustrated the defects on the waveform resulting of the harmonics in the load side.

2) Second case: Connecting high pass filter (HPF) circuit in parallel with the grid (at point 3 in fig 1). The final circuit is shown above in the figure 4:

Figure 5 shows the load voltage waveforms.It is so clear how the waveform is more sinusoidal in comparison with figure 3. The figure 6 shows the harmonic current (Ih) and figure 7 shows the output voltage of the inverter (Vinv.)when harmonic voltage is 5000 volt, the waveform is working on 50 Hz and so much sinusoidal :

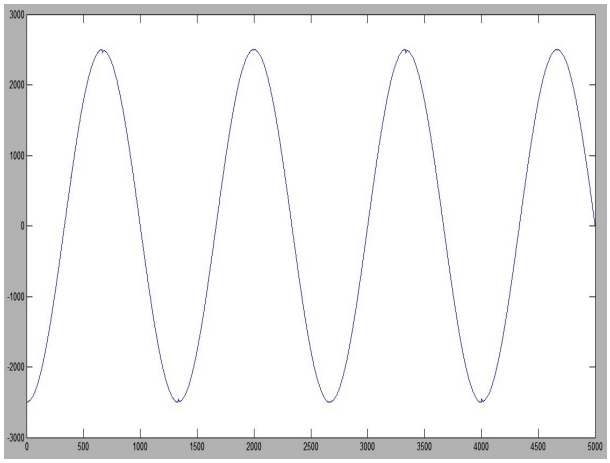

Fig. 5. Load voltage with HPF

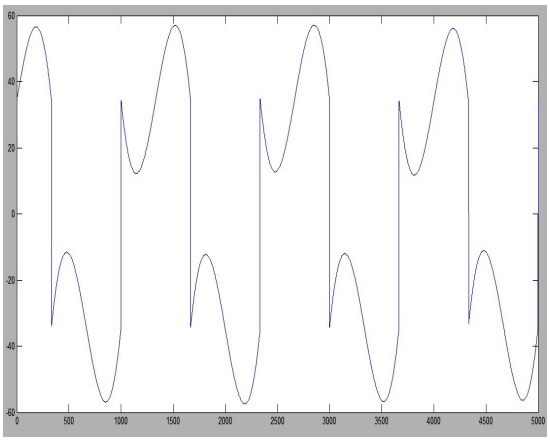

Fig. 6. Harmonic current when Vh = 5000 volt

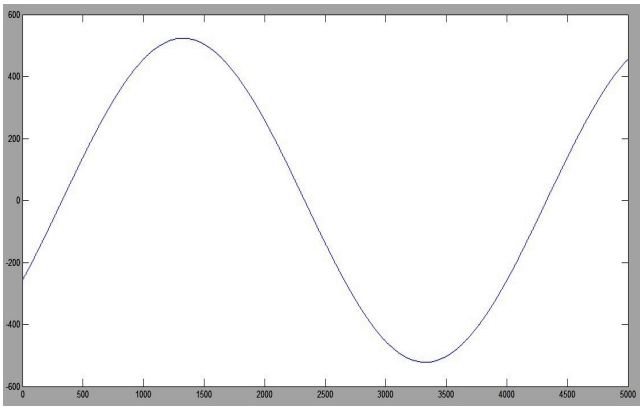

Fig. 7. Inverter output voltage when Vh=5000

VII. Results assessment

The table (1) below shows all the results of the simulation with a comparison between the changes in the non linear load represented in harmonic voltage power supply which produce (150 Hz), current THD1 percentage (at point 3), current THD2 percentage (at point 3), (Ih) harmonic current (at point 4), rectifier voltage (case 2) and inverter voltage (case 2). The actual readings which have been taken in [14], show the high differences between values of current THD between different buses and phases. In spite of many restrictions on the THD values, but the real data show that THD values reach 200 percentage [14]. For that reason and to expand the results range, the value of harmonic voltage power supply (150Hz) assumed to be increased up to 5000 volt as a maximum value as a nonlinear load. The first column of the table shows the nonlinear load represented by voltage power supply (Vh)(150 Hz) increasing from 5 volt up to 5000 volt. The second column shows THD-I percentage for the 1st case (without HPF), the third column shows THD-I percentage for the 2nd case(with HPF), the fourth column shows the harmonic current (Ih) drawn after HPF, the fifth column shows the output voltage of the bridge rectifier (Vrect.), the sixth column shows the DC to AC inverter voltage (Vinv) which is sinusoidal AC voltage (50Hz).

	1st case	2nd case	2nd case	2nd	2nd
Vh	THD-I	THD-I	Ih (A)	Vrect.	Vinv.
5	0.74	0.36	0.06	4.77	0.6
20	2.8	1.96	0.4	19.1	2.5
50	3.86	2.89	0.57	47.7	5.2
100	6.6	5.6	1.5	95.5	10.5
200	15.45	11.5	2.2	191	21
300	25.67	19.4	3.5	286.5	31
400	31.8	23	4.7	382	42.6
500	42	32	5.9	477.5	52.8
1000	71.75	56.4	11.5	955	105
2000	183.6	120.2	22.8	1910	205
3000	251	173	34.5	2865	309
4000	307.3	221	45.6	3820	411
5000	483.4	267	58	4775	522

In order to understand the table(1), we need to demonstrate the data in details, it is recognized that when the nonlinear load represented by voltage source (Vh) is equal to 2 Volt, the current total harmonic distortion in the first case (THD-I) is equal to 0.76 percent, and the current total harmonic distortion in the second case (THD-I) = 0.36 percent, that is meant the THD-I decreased 0.38 percent after connecting the HPF circuit. When the nonlinear load increases to Vh = 20 volt, the THD-I decreased 0.84 percent. When the nonlinear load Vh = 50 volt, THD-I decreased 0.97 and that decreasing continue linearly till the last case when the nonlinear load Vh = 5000 volt, THD-I decreasing reaches more than 216 percentage which is too high number and considered as a very good reduction of THD value.

Simultaneously, the harmonic current (Ih) which was drawn by the low impedance High pass filter (HPF) increases with the harmonic voltage source (non linear load) increasing begins from 0.06 Ampere (when Vh = 5 volt), ending with 58 Ampere (when Vh = 5000 volt) and rectifier voltage (Vrect.) = 4.77 Vdc (when Vh = 5 volt) and increases to reaches 4775 Vdc (when Vh = 5000 volt), also the output inverter voltage (Vinv) = 0.6 volt (when Vh = 5 volt) and increases to reaches 522 volt (when Vh = 5000 volt). Whereas the value of THD-I of the output circuit after transformer (at point 5 in figure 1) remains constant all the time on 0.02 percentage.

From the details mentioned before, it can be easily concluded that the (THD-I) is increasing linearly with the harmonic voltage increasing. This increasing is in both cases (without and with adding HPF circuit), but the results in the first case are higher than the second case for the same harmonic voltage in all data. The figure (8) shows the two cases curves illustrated THD-I percentages with the increasing of harmonic voltages, it is obvious that the gap between two curves is expanding with the harmonic voltage increasing, that means the effect of adding HPF circuit on the system is increased with the increasing of harmonics (by decreasing THD-I value).

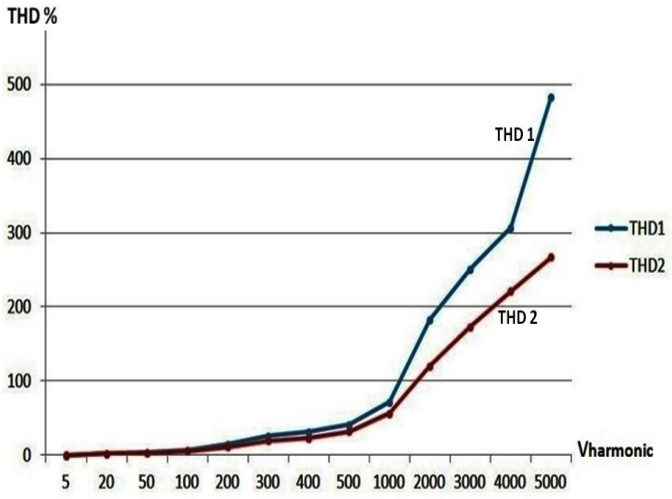

Fig. 8. THD1 curve and THD2 curve

Finally, according to the simulation results, this work proved its effectiveness because, the goal of this work was to find a new method to decrease the harmonics on the load side and to invest these harmonic currents through converting them to a useful power in order to benefit of this power to feed different loads. The results of the simulation work show that the THD percentage was decreased in all cases and the produced power at the output side (point 5 in figure 1) has a sinusoidal wave and low THD-I (0.02 percent).

VIII. Conclusion

This paper presents a novel idea to benefit of the harmonic currents and voltages on the load side, its present also a method to reduce harmonics' values by filtering out the harmonic currents in multiple of 50 HZ frequencies and use it as a power supply to feed different loads. From the results of the simulation, it can be concluded that the harmonic currents can be drawn by using a 150 Hz high pass filter from the load side and that's reduces the total harmonic distortion (THD) value. The simulation results show THD value can be reduced more than 216 percentage, when the nonlinear load is too high. These harmonic currents have been converted to useful power with too small THD about (0.02 percentage), by converting them to DC and reconvert it to AC with fundamental frequency.

These results open a new horizon to find out new more effective methods to benefit of a missed power like harmonic currents by converting it to usable power, at the same time, reduce the THD value on the load side and reduce its harmful effect on the electrical power system .

IX. ACKNOWLEDGEMENT

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References

[1] E. Owen, "A history of harmonics in power systems," *Industry Applications Magazine, IEEE*, vol. 4, no. 1, pp. 6–12, Jan 1998.

[2] C. Francisco, *Harmonics and power systems*. CRC press, 2006.

[3] Y. Alhazmi, "Allocating power quality monitors in electrical distribution systems to measure and detect harmonics pollution," 2010.

[4] L. Czarnecki, "An overview of methods of harmonic suppression in distribution systems," in *Power Engineering Society Summer Meeting, 2000. IEEE*, vol. 2, 2000, pp. 800–805.

[5] W. M. Grady and S. Santoso, "Understanding power system hannonics," *Power Engineering Review, IEEE*, vol. 21, no. 11, pp. 8–11, Nov 2001.

[6] K. M. Hink, "Harmonic mitigation of 12-pulse drives with unbalanced input line voltages," *MTE Corporation, W147*, no. 9525, 2002.

[7] H. Sasaki and T. Machida, "A new method to eliminate ac harmonic currents by magnetic flux compensation-considerations on basic design," *Power Apparatus and Systems, IEEE Transactions on*, no. 5, pp. 2009–2019, 1971.

[8] P. P. Khera, "Application of zigzag transformers for reducing harmonics in the neutral conductor of low voltage distribution system," in *Industry Applications Society Annual Meeting, 1990., Conference Record of the 1990 IEEE*. IEEE, 1990, pp. 1092–vol.

[9] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of three-phase improved power quality ac-dc converters," *Industrial Electronics, IEEE Transactions on*, vol. 51, no. 3, pp. 641–660, 2004.

[10] B. Bird, J. Marsh, and P. McLellan, "Harmonic reduction in multiplex convertors by triple-frequency current injection," *Electrical Engineers, Proceedings of the Institution of*, vol. 116, no. 10, pp. 1730–1734, 1969.

[11] L. Gyugyi and E. C. Strycula, "Active ac power filters," in *Proc. IEEE/IAS Annu. Meeting*, vol. 19, 1976, pp. 529–535.

[12] L. Chen, Y. Xie, and Z. Zhang, "Comparison of hybrid active power filter topologies and principles," in *Electrical Machines and Systems, 2008. ICEMS 2008. International Conference on*. IEEE, 2008, pp. 2030–2035.

[13] S. E. G. Mohamed and A. Y. Mohamed, "Study of load side harmonics sources effects and elimination."

[14] M.-Y. Chan, K. K. Lee, and M. W. Fung, "A case study survey of harmonic currents generated from a computer centre in an office building," *Architectural Science Review*, vol. 50, no. 3, pp. 274–280, 2007.

Appendices A.2 to A.8 have been removed due to copyright restrictions.

A.2 2nd International Conference on Systems and Informatics (ICSAI), (15-17) November 2014, China

Title "Taking Advantage of the Harmonics at the Load Side Using Passive Filters"

DOI: 10.1109/ICSAI.2014.7009280

A.3 IEEE 5th International Conference on Power Engineering, Energy and Electrical Drives (POWERENG), (11-13) May 2015, Latvia

Title "The benefit of harmonics current using a new topology of hybrid active power filter"

DOI: 10.1109/PowerEng.2015.7266339

A.4 IEEE Conference on Energy Conversion (CENCON), (19-20) October 2015, Malaysia

Title "A new power theory (right-angled triangle theory)"

DOI: 10.1109/CENCON.2015.7409587

A.5 17th International Conference on Harmonics and Quality of Power (ICHQP), (16-19) October 2016, Brazil

Title "Utilization of harmonics current in single phase system"

DOI: 10.1109/ICHQP.2016.7783468

PEARL (OA): http://hdl.handle.net/10026.1/10545

A.6 International Conference for Students on Applied Engineering (ICSAE), (20-21) October 2016, Newcastle-UK

Title "Feeding Loads Via Harmonics Utilization in AC Circuit Systems"

DOI: 10.1109/ICSAE.2016.7810192

A.7 IEEE 17th International Conference on Environment and Electrical Engineering (EEEIC), (6-9) June 2017, Italy

Title "A Novel Topology For Single Phase Active PFC Circuit"

DOI: 10.1109/EEEIC.2017.7977710

A.8 International Journal of Electrical Power & Energy Systems, Volume 88, June 2017, Pages 133-140

Title "New effective power terms and right-angled triangle (RAT) power theory"

ISSN: 0142-0615 , 1879-3517; DOI: 10.1016/j.ijepes.2016.12.009

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A.9 Global Journal of Researches in Engineering, GJRE Volume 17 Issue 5 Version 1.0

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Reduced Size Single Switch Power Factor Correction Circuit

By Hussein al-bayaty, Ali Hussein Al-Omari, Marcel Ambroze & Mohammed Zaki Ahmed

Plymouth University, United Kingdom

Abstract- This article presents a new design of active power factor correction (APFC) circuit that can be used in single phase rectifiers. The proposed circuit provides almost a unity input power factor (PF) which contributes significantly in reduction of the total current harmonic distortion (THDI) as it eliminates the third harmonic component effectively from the input current.

The most important attribute of this circuit is the small size and numbers of components (one switch, small size (L & C) and a diode), which have been designed to get a unity PF at the AC source side. Therefore, the new circuit is cheaper, smaller size and lighter than other conventional PFC circuits.

In addition, the new proposed circuit is a snubber-less and uses reasonably low switching frequency which reduces switching losses and increases efficiency. The circuit has been designed and simulated using Lt-spice simulink program.

Keywords: *active power factor correction (APFC), AC - DC converter, total harmonic distortion (THD).*

GJRE-F Classification: *FOR Code: 090607*

Strictly as per the compliance and regulations of:

Reduced Size Single Switch Power Factor Correction Circuit

Hussein al-bayaty [α], Ali Hussein Al-Omari [σ], Marcel Ambroze [ρ] & Mohammed Zaki Ahmed [ω]

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I. Introduction

Single phase AC/DC rectifiers with a large electrolytic capacitor are commonly used for manufacturer and business issues. The main purpose to use diode rectifiers is to operate the switching power supply in data processing apparatus and to operate low power motor drive systems [1].

The large capacitor draws current in short pulses, which brings in a lot of problems including decreasing in the available power, increasing losses and reduction of the efficiency. In the conventional way of design, the capacitor voltage preserves the peak voltage of the input sine wave until the next peak comes along to recharge it [2].

The only way to recharge the capacitor is drawing the current from the input source at the peaks of the source waveform as a long pulse which includes an adequate amount of energy to nourish the load until the next peak. This is happens when the capacitor draws a large charge during short time, after the slowly discharge of the capacitor into the load. Therefore, the capacitor's current draws 5 to 10 times of the average current in 10% or 20% of the cycle period. Consequently, the source current has narrow and long pulses and the effective (r.m.s.) value increases [3], [4].

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Customers with a large number of nonlinear loads also have large neutral current rich in third harmonics current. In order to increase the PF, decrease the losses and save the energy, then the input current harmonics (specially the third order harmonic) have to be eliminated. Several methods and techniques have been proposed to solve the problem of a poor power factor, which can be classified as active and passive methods [5].

Passive PFC circuits are generally simple, fewer components, smaller size and easy to design for small rating power (less than 200 watt). However, its bulky and not economical for large power ratings and the input power factor is (0.6 - 0.7) and THD = 150% in best conditions without using big size elements [6].

Active PFC circuits, can considerably diminish losses and costs associated with the generation and distribution of the electric power and significantly improved power quality. Therefore, APFC circuits are receiving more and more attention these days because of the widespread use of electrical appliances that draw non sinusoidal current from the electric power systems. However, PFC circuits require additional, more expensive and complex components [7]. The author in [8], designed a novel PFC circuit that depends on the principle of limiting the work of the main capacitor in a manner which can eliminate the third order harmonic and improve the input PF into 0.99. However, this design has been used two Mosfets and high switching frequency equal to 200 KHZ which may increase the switching losses and reduce the efficiency.

In this paper, a new design of PFC converter has been introduced and presented in figure (1). The new design is depending on the flexibility of the parameters' variation which produces low harmonics, high input PF and high efficiency.

The new proposed design, reduces the required number of components into one Mosfet switch with low switching frequency equal to 20 KHZ, and uses small value of inductor which is smaller more than 96% of the inductors used in conventional boost PFC circuits, because the new proposed design focuses on shifting the harmonics components to the high frequency region and consequently eliminating the third order harmonic current, therefore the cost, the weight and the size of the new circuit will be reduced hugely.

The description of the circuit, operation topology, control circuit and operation stages are all

described in section (II). The details of system's parameters are described in section (III). The discussion of simulation results and assessment are presented in section (IV), followed by an overall conclusion in section (V).

II. Operation Principles and Analysis of the New Proposed Circuit

a) Circuit's Description

The schematic circuit of the new proposed PFC circuit is shown below in figure (1).

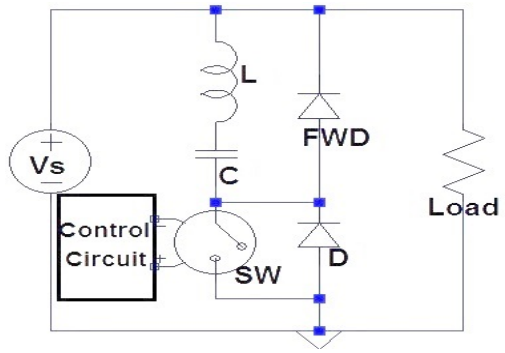


Fig. 1: New proposed APFC circuit

(V_S) is the input DC source (represents AC single phase connected to full bridge rectifier), connected in parallel with LC resonant branch and MOSFET switch (SW) in parallel with the load. A control circuit has been designed in order to control the switching process.

b) Operation Topology

The new proposed circuit has the ability to control the working period of the capacitor. Consequently, the value of the input power factor, THD_I of the source current waveform and the value of the output ripple voltage can be controlled as well through using one switching devices.

The principle of this design is depending on the distributing of the working time intervals of the capacitor into two regions, at the beginning (0 - t_1) and at the end (t_4 $-\pi$) via using control circuit. This smart switching pattern would eliminates the third order harmonic component and improves the input PF as the third order harmonic is the most significant component in single phase systems.

This design uses a minimum number of components and minimum values of (L) & (C) a s capacitor turned off on the middle of each cycle, which shift the harmonics components to higher frequencies. consequently, reduces the size and the cost of the new proposed circuit.

This circuit is snubber-less circuit, because the freewheeling diode (FWD) presents an alternative path for the discharge current of inductor (I_L), so can the capacitor keep charged. Accordingly, (FWD) can avoids the negative part of I_L and helps (C) to act as a snubber circuit in order to prevent the inductor's voltage (V_L) to increase more than rated value of the source voltage, in this way (C) will protect the MOSFET switch from being burned in the effect of the high voltage spikes which may happened without the FWD.

c) Control circuit

A simple designed control circuit, as shown in figure (2) has been investigated in order to derive the MOSFET switch and control the switching frequency and duty cycle.

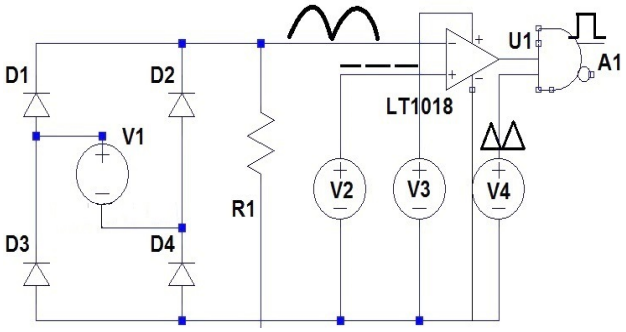


Fig. 2: Control circuit

Briefly, the circuit consists of a dual input comparator which compares two signals(the first signal is the output of full wave rectifier and the second is a dc voltage source). The output of the comparator, which is a square wave, would be combine in a logic (And gate) circuit with a triangular waveform in 20 KHz frequency. the output of and gate will go directly to the gate of the MOSFET switch.

d) Operation stages

1) First mode: This mode describes the time period $0 \leq t < t_1$, when the capacitor voltage $V_C > V_S$. SW-ON/OFF, while t_1 is the moment when V_S is equal or bigger than V_C. The circuit shown in figure (3-a), illustrates the path of the current at this mode:
In this period, (C & L) are discharging and feed the load.

$$I_C = C\frac{dV_C}{dt} = I_L = I_{Load} = \frac{V_{out}}{R}$$

because L, C and the load are series in this mode.

$$\therefore V_{Load} = V_{out} = V_C + V_L$$

$$\because V_L = L\frac{di_L}{dt}$$

then the value of V_L is approximately zero because the value of L_1 is very small (few micro henres).

$$\therefore V_{out} \approx V_C$$

The full time period of the input source current waveform (I_S) is shown in figure (4) with the details of nine time modes.

2) Second mode: For the time period $t_1 \leq t < t_2$, when $V_S > V_{C1}$, and SW is ON. t_2, is the moment when the pulses turns off. The circuit shown above in figure (3-b), the bold line illustrates the active path at this mode.

In this mode, the load, C & L are all connected to the source and charging with frequency pulses (20 KHz), as a result, high values and short time current spikes appear on the input current waveform because of the capacitor current. $V_S = V_{Load} = V_{out}$

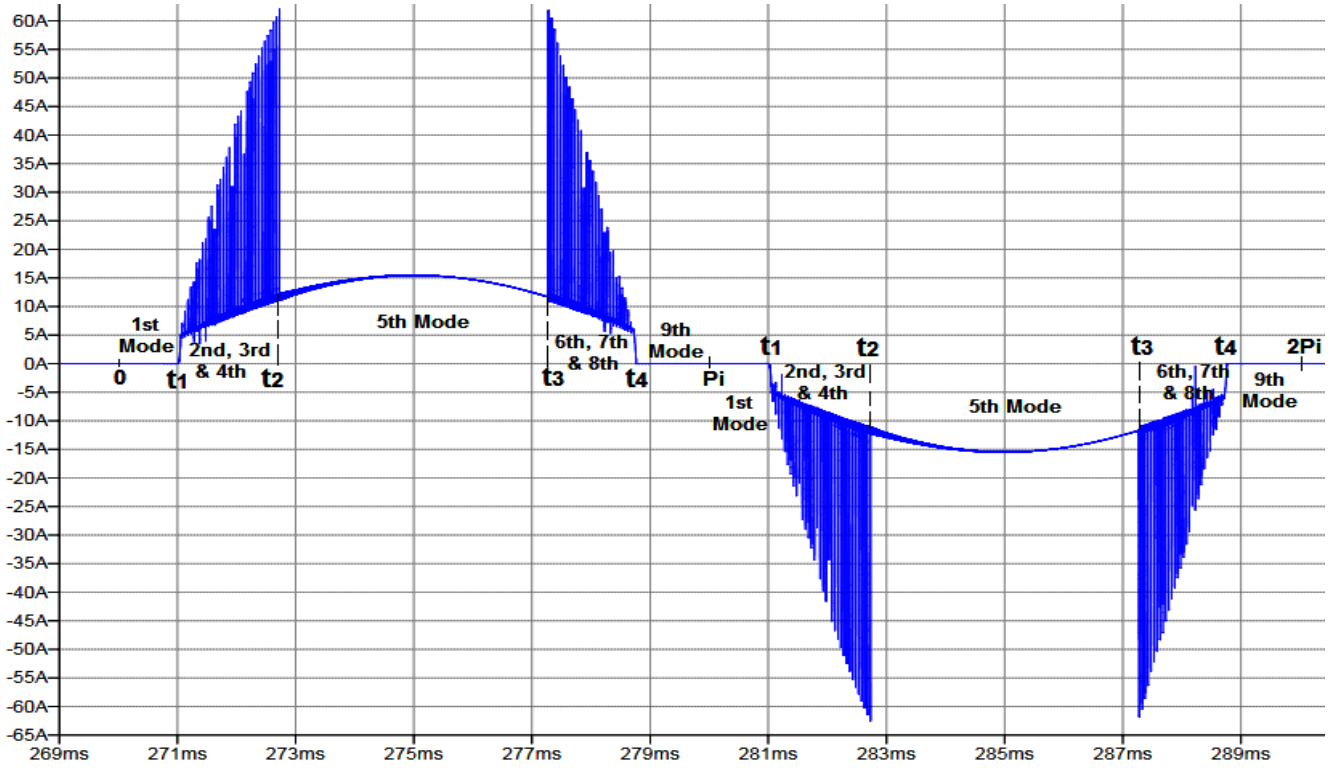


Fig. 4: The input source current

$$V_S = V_C + V_L = V_C + L.\frac{di_L}{dt} \quad I_S = I_C + I_{Load} = C.\frac{dV_C}{dt} + I_{Load}$$

3) Third mode: For the time period $t_1 \leq t < t_2$, when $V_S > V_{C1}$. This mode covers the interval time from switching OFF moment until (t_d) ms. t_d is the moment when I_L or I_C discharge to zero ampere for each pulse. The circuit is shown above in figure (3-c).

At this mode, (L) discharges its current to (C) until being zero (at the t_d moment), while the inductor voltage V_L is equal to V_C and remains charged. This topology dose not require a snubber circuit as V_L has been prevented.

$$\because V_L = V_C \quad \& \quad I_L = I_C = C\frac{dV_C}{dt} \quad \therefore X_L = X_C$$

$$2\pi fL = \frac{1}{2\pi fC} \quad \therefore f_r = \frac{1}{2\pi\sqrt{LC}} = 1.59KHz$$

f_r is the resonance frequency.

At this mode, the load is fed by the source.

$$V_L = L\frac{di_L}{dt} = V_C$$

$$I_S = I_{Load} = \frac{V_{out}}{R}$$

4) Fourth mode: For the time period $t_1 \leq t < t_2$, when $V_S > V_C$, SW is OFF (from (t_d) until the next ON-pulse). The bold line in the circuit shown above in figure (3-d), clarifies the source current's path.

At this mode, the inductor current (I_L) supposed to remain zero ampere. However, the internal capacitance of the diodes combines with stray inductance which form resonant circuit called parasitic resonant.

Due to this parasitic resonance, a sinusoidal current can flow into the inductor L_1 in a very high frequency (about 1.54 MHz) called self resonant (or parasitic) frequency (f_p).

At the same time, V_L follows I_L waveform and oscillate around zero. I_L & I_S values are variable and change in accordance to the values of L, C, f_{sw2}, $\frac{dv_c}{dt}$ and output load as it's clear from equations and shown in figures (4) and (5):

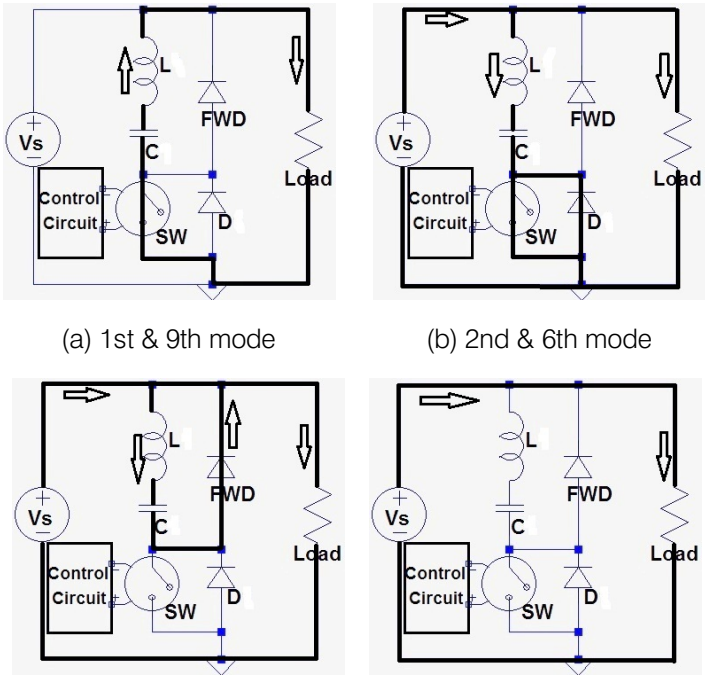
The capacitor voltage (V_C) remains charged and considered as a constant value due to the value of I_C which is approximately zero, then the value of $\frac{dV_C}{dt}$ is very small value.

$$I_L = I_0.\cos(w_p.t)$$

$$w_p = 2\pi f_p \approx 9.5 \text{ M rad/sec.}$$

(I_0) is approximately 0.5 Amp. For ideal conditions, the internal capacitance of diodes is zero, therefore the parasitic resonance and I_0 can considered as zero ampere.

Practically, a damper circuit (R=5 Ω & C=1 nF) can be connected in parallel with the freewheeling diode in order to eliminate the resonance current (I0) totally, however, 0.1 % of power losses can be increased in the circuit as a circuit of 3 kw output power, has only 3 watt losses in the damper circuit which is negligible. The modes (2,3,4) are repeating every ON/OFF switching pulse of SW.



(a) 1st & 9th mode (b) 2nd & 6th mode

(c) 3rd & 7th mode (d) 4th, 5th & 8th mode

Fig. 3: Circuit diagram in different time modes

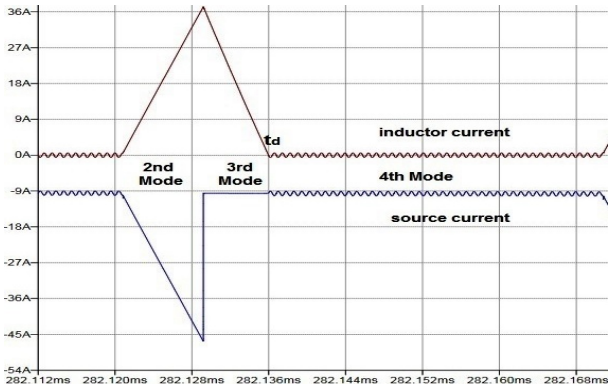


Fig. 5: IL & IS in the 2nd, 3rd & 4th modes

The figure (6), shows the full picture of V_C, V_{out}, V_L&V_D waveforms. V_C is in red color, V_{out} is in brown color, V_L is in green color, and V_D is in blue color.

5) *Fifth mode:* For the time period $t_2 \leq t < t_3$, when pulses are ON/OFF. t_3 is the moment when SW turns OFF. The circuit shown in figure (3-d), illustrates the active path of current at this mode:

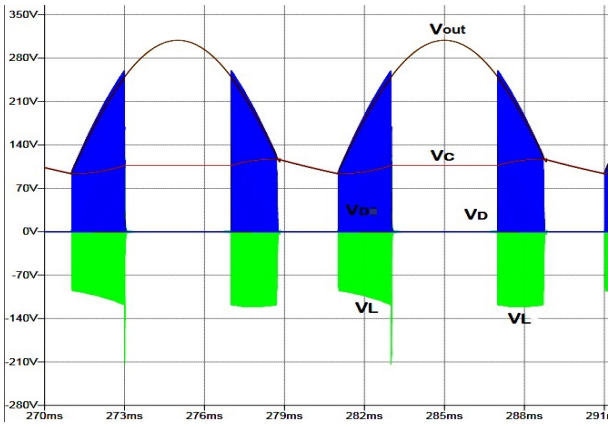


Fig. 6: V_C; V_{out}; V_L & V_D waveforms

Due to $V_S > V_C$, therefore *C* and *L* are considered as disconnected (open circuit), because they are reverse biased when SW is OFF and (FWD) is reverse biased.

Therefore, C and L are neither charging nor discharging, then $I_L = I_C$ = Zero, V_L = Zero but V_C is a constant value.

6) *Sixth mode:* For the time period $t_3 \leq t < t_4$, when $V_S > V_C$, SW is ON. t_4 is the moment when V_C is greater than V_S. The circuit is shown in figure (3-b).
At this mode, C and L are charging and the load is fed by the source. All the derived equations in the 2nd mode are valid for this mode.

7) *Seventh mode:* For the time period $t_3 \leq t < t_4$, when $V_S > V_C$. The circuit is shown in figure (3-c).
At this mode, (C) is charging while V_L is equal to V_C until *L* fully discharges its current into zero ampere at the time of (t_d).
All the derived equations in the 3rd mode are valid for this mode.

8) *Eighth mode:* For the time period $t_3 \leq t < t_4$, when $V_S > V_{C1}$, SW is OFF, for period (t_d) until the next ON-pulse for SW_2. The circuit is shown in figure (3-d).
V_C still charged and slightly charging but approximately constant due to very small $\frac{dV_C}{dt}$.
V_{C1} remains charged and considered as a constant value due to the value of I_{C1} is approximately zero, then the value of dVC1 would be very small.

$$I_{L1} = I_0 . \cos(w_p . t)$$

$$w_p = 2\pi f_p \approx 9.5 \text{ M rad/sec.}$$

The modes (6,7,8) repeat themselves every ON/OFF switching of the MOSFET.

9) *Ninth mode:* For the time period $t_4 \leq t < 10$ ms., when $V_C > V_S$. SW-ON/OFF, the circuit is shown above in Fig. (3-a).
L & C are discharging while the R-load is fed by the main capacitor.

$$\therefore I_L = \frac{V_{out}}{R}$$

$$V_{Load} = V_{out} = V_C + V_L$$

All the derived equations in the first mode are valid for this mode.

III. System Parameters

The proposed circuit has been simulated in LT-spice program and the parameters have been specified as the following table:

Table I: System Parameters

Inductor (L)	$R_{\text{Internal Ser.}}$ = 2.236 m Ω	$R_{\text{Internal Par.}}$ = 1413 Ω
Capacitor (C)	ESR = 0.035 Ω	ESL = 0 Ω
MOSFET	IPP070N8N3, N-channel	V_{ds} = 80 V, R_{ds} = 7m Ω
Freewheeling diode	Schottky, (UPSC600)	$V_{\text{Breakdown}}$ = 600 V
Parallel diode	Schottky, (MBR745)	$V_{\text{Breakdown}}$ = 45 V
Load	Resistive	20 Ω

IV. Simulation Results and Assessment

An electrical circuit with V_S = 311 V_{peak} = 220 V_{rms}, L = 20 μH, C = 0.5 mF and MOSFET switch works in f_{sw} = 20 Khz controlled by a control circuit, has been designed and investigated by using Lt-spice simulink program.

1) R-load, inductor (L) and switching frequency of the MOSFET, are three main parameters in this circuit which could be changed in different values in order to find out the optimum design and parameters values in order to get low input THD_I , unity input PF, high efficiency, cheap, not bulky, small size and light converter.
2) Table (I), shows the relationship between different load values comparing it with fundamental input current P_{in}, P_{out}, η, THD_I and input PF when L = 20 μH and the switching frequency (f_{sw}) is 20 Khz.

Table II: Different load values with THD_I, PF & η

R(Ω)	P_{in}(W)	P_{out} (W)	η(%)	THD(%)	PF
1	46354.5	44260	95.48	5	0.999
10	4920.2	4851.5	98.6	11.6	0.994
20	2506	2473	98.68	17	0.986
50	1038	1021	98.36	28.4	0.96
100	543.48	525	96.6	37	0.938
200	292.68	269.6	92.1	52.4	0.886
500	141	110.75	78.55	83.2	0.77
1000	90.2	56.1	62.2	111.7	0.667

Power factor has been calculated by using equation in [9], P.F = $\frac{1}{\sqrt{1+(THD_I)^2}}$

$$I_t = \sqrt{I_1^2 + I_h^2}$$

The total input power, has been calculated via below equation [10]:

$$P_{in} = V_t.I_t.PF$$

The maximum efficiency is 98.68% when input power is 2.5 kw when R-load = 20 Ω and (L) is 20 µH.

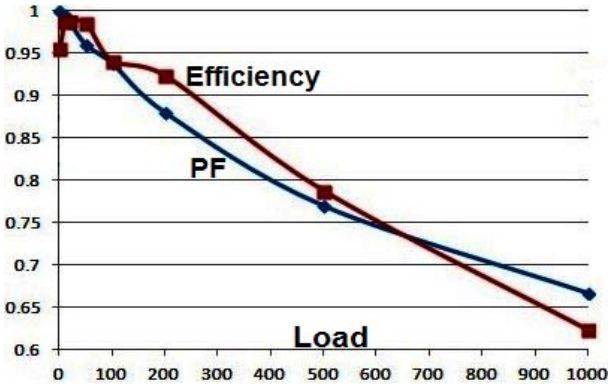


Fig. 7: Different load values with PF and η

It can be concluded, from table (I) and figure (7) that the values of (η) and input PF, inversely proportion with the increasing of the load value.

3) Table (II) shows the relationship between different inductor values comparing with with P_{in}, P_{out}, _ and input PF, when R-load = 20 Ω and f_{sw} = 20 Khz.

Table III: Different (L) values with THD_I, PF & η

L(uH)	P_{in}(W)	P_{out} (W)	η(%)	THD(%)	PF
1	2854.9	2679.4	93.86	55	0.876
10	2557.5	2510	98.1	24	0.972
20	2506	2473	98.68	17	0.986
50	2456	2434	99.1	10.5	0.994
100	2434.38	2415.5	99.2	7.2	0.997
200	2420.48	2403.7	99.3	4.9	0.999
500	2412	2395	99.3	3.5	0.999
1000	2407.3	2391.8	99.36	2.5	0.999

It can be concluded, from table (II) and figure (8) below, that the value of η and PF, directly proportion with the increasing of inductor value.

4) Table (III) shows the relationship between different switching frequencies of MOSFET comparing with P_{in}, P_{out}, η and input PF when R-load = 20 Ω and (L) is 20 µH.

It can be concluded from table (III) and figure (9) that, the value of η and PF directly proportion with the value of f_{sw}.

It can be concluded that, f_{sw} can be kept around (10 - 20) KHz in order to get approximately unity PF (0.98) at the input AC side when (L) is 20 µH for 2.5 kw output power.

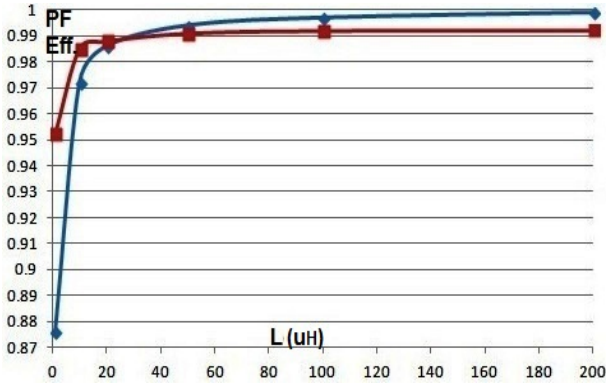


Fig. 8: Different (L) values with PF and η

Table IV: Variable (D) for (SW) with THD_I, PF & η

f_{sw}(K)	P_{in}(W)	P_{out} (W)	η(%)	THD(%)	PF
5	2641	2574.8	97.5	33	0.95
10	2561	2515	98.2	23.8	0.973
20	2506	2473	98.68	17	0.986
50	2456.3	2434.2	99.1	10.6	0.994
100	2437.3	2415.8	99.1	7.6	0.997
200	2418.9	2405	99.4	5.6	0.998
500	2415	2397.2	99.2	3.9	0.999
1000	2414.8	2396.2	99.2	3.7	0.999

5) The figure 10, shows the Fast Fourier Transform (FFT) spectrum of the input source current. The total current harmonic distortion (THD_I) is 17%, then the total input power factor is (0.986).
As it is shown in figure (10), the third order harmonic is not exist at the input current waveform, and the only harmonic orders shown are the 5th and 7th order harmonics. This is because (C) was OFF at the middle of the waveform ($t_2 - t_3$) and the load was fed by the source.

6) In the case of the absence of freewheeling diode in the time intervals $t_1 \leq t < t_2$ and $t_3 \leq t < t_4$ (which represent the 2nd and 6th modes), the equation of inductor's voltage is:

$$V_L = L\frac{di_L}{dt} = \frac{L.di_L.f_{sw}}{D}$$

(D) is the duty cycle of (SW) and because of the switching frequency (f_{sw}) is (20 KHz), therefore V_L would be a very large value at this moment. Consequently, V_L may be a reason for huge spikes on MOSFET's terminals and may burn the switch.

7) Generally, in this situation a snubber circuit would be proposed as a solution to suppress the high frequency spikes and to protect the MOSFET switch. However in this circuit, the main capacitor (C) would be act as a snubber circuit because of the existence of the freewheeling diode (FWD), which makes V_C charges on the negative value of V_L and prevent high voltage on the terminals of the MOSFET when its in open the status. As shown in figure (11), the inductor voltage does not increases more than 140 $V_{P\text{-}P}$ in spite of that the source voltage is 311 $V_{P\text{-}P}$, because of the small value of (L).

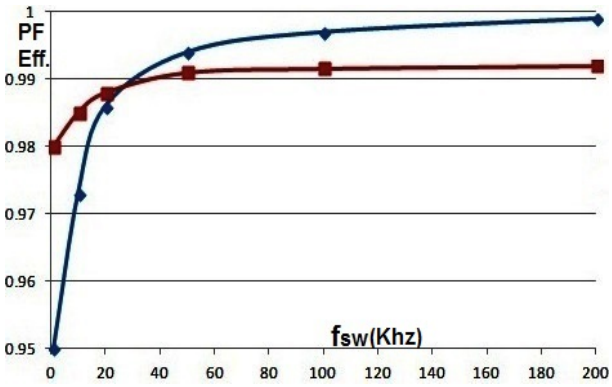


Fig. 9: Different f_{sw} values with PF and η

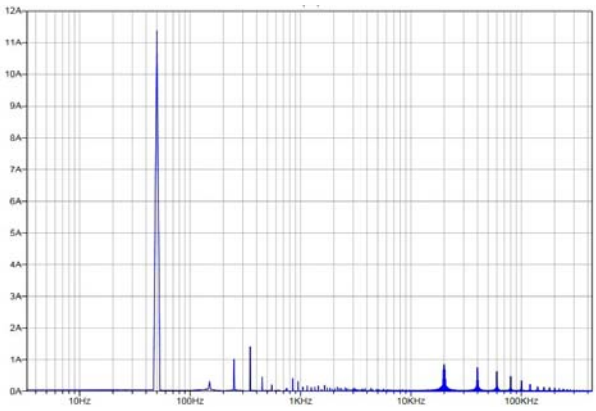


Fig. 10: FFT Spectrum of the input current

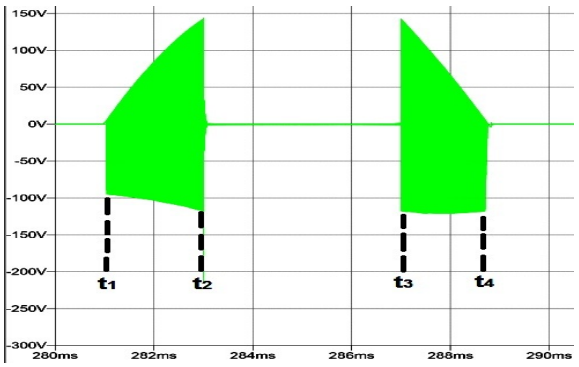


Fig. 11: The waveform of V_L

8) The required value of the inductance for the same voltage and power ratings in three level boost converter is (L), while the size would be doubled with the using of two inductors (2x2L) for the interleaved boost converter, on the other hand, the inductance would be doubled again (4L) for the conventional boost converter [11].

   The inductor's value used in the literature in [12] for a (3 kw) output power using interleaved boost converter was (270 μH), while the value of inductor (L) in the new proposed circuit is (20 μH) for the same power ratings. This reduction of the inductor's value will effectively contribute in reducing the size, weight and the cost of the converter.

9) One of the significant features of this design, is that the inductor's current is not related to the value of source voltage (except in the 2nd and 6th mode) as usually happens in PFC circuits. This advantage can be utilized in order to reduce the value of (L) into few micro henrys and avoid high V_L values. Consequently, can reduce the size, weight and the cost effectively.

10) Practically, the internal capacitor of the used diodes in the circuit would combine with the stray inductors and compose a parasitic resonant frequency (f_p). In order to get rid of the bad effects of (f_p), the rising time (t_r) or the falling time (t_f) can be changed, or alternatively a damper circuit can be added to the circuit or using clamping diodes and that's require additional components and complex design [13].

11) The inductor works like a proper choke or current limiter due to the high negative value of inductor voltage (V_L) as its in counter direction of capacitor voltage (V_C).

    (L) charges in the time period $t_1 \leq t < t_2$ because $V_S > V_C$. On the other hand, for the time period $t_2 \leq t < t_3$, *IL* is zero because L and C are reverse biased. While, for the time period $t_3 \leq t < t_4$, (L) discharges as a positive current because $V_S > V_C$. However, for time period $t_4 \leq t < t_1$ of the next period, *L* discharges as a negative current because $V_C > V_S$ and the R-load would be fed by I_L which is the same capacitor's current ($I_C = I_L$).

V. Conclusion

According to the simulation's results, the new proposed PFC circuit was able to reduce the THD_I to 17% with a unity power factor (0.986) at the input side and increases the efficiency to 98.68%.

The topology of reducing the conduction time of the main capacitor via dividing the waveform into three regions ONOFF-ON, can improve the efficiency, the input PF and reduce the THD_I at the input side.

In addition, preventing the capacitor (C) from work in the middle of the time period for about half of the time will eliminate the third order harmonic and shift the harmonics current to the high frequency region and that's will contribute in reducing the size of magnetics due to the small value of the inductor 20 μH which produces a small amount of losses. Accordingly, the small inductor will effectively reduce the size and weight as used just one MOSFET, so the rectifier is not bulky any more, and thats reduces the cost of the converter.

Another advantage of this circuit is that the snubber circuit is not compulsory because of the presence of freewheeling diode. In addition, the design

is considered as a high efficient design due to minimum number and small values of components and simple circuit design due to uses single switch.

The performance of this circuit has a wide range of flexibility because, the output ripple voltage, the input PF and THD_I can be improved via controlling the values of duty cycles of (SW), (L) and (C).

From graphical waveforms and tables of results analysis for different values of R-load, inductor (L), and switching frequency, can be concluded that the increasing of inductor value (L) and R-load values is required in order to get a constant unity power factor, small THD_I and high efficiency.

VI. Acknowledgment

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References Références Referencias

1. H. Al-bayaty, M. Ambroze, and M. Z. Ahmed, "Utilization of harmonics current in single phase system," in *2016 17th International Conference on Harmonics and Quality of Power (ICHQP),* Oct 2016, pp. 443–447.
2. B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of single-phase improved power quality ac-dc converters, "*IEEE Transactions on Industrial Electronics*, vol. 50, no. 5, pp. 962–981, 2003.
3. H. Al-bayaty, M. Ambroze, and M. Z. Ahmed, "Taking advantage of the harmonics at the load side using passive filters," in *Systems and Informatics (ICSAI), 2014 2nd International Conference on*, Nov 2014, pp. 169–174.
4. H. Azazi, E. El-Kholy, S. Mahmoud, and S. Shokralla, "Review of passive and active circuits for power factor correction in single phase, low power ac-dc converters," in *Proceedings of the 14th International Middle East Power Systems Conference (MEPCON'10)*, 2010, pp. 217–224.
5. H. Al-bayaty, M. Ambroze, and M. Z. Ahmed, "Feeding loads via harmonics utilization in ac circuit systems," in 2016 *International Conference for Students on Applied Engineering (ICSAE)*, Oct 2016, pp. 224–227.
6. S. Basu, *Single Phase Active Power Factor Correction Converters-Methods for Optimizing EMI, Performance and Costs.* Chalmers University of Technology, 2006.
7. J. P. M. Figueiredo, F. L. Tofoli, and B. L. A. Silva, "A review of singlephase pfc topologies based on the boost converter," in *Industry Applications (INDUSCON), 2010 9th IEEE/IAS International Conference on,* Nov 2010, pp. 1–6.
8. H. al bayaty, A. H. Al-Omari, M. Ambroze, and M. Z. Ahmed, "A novel topology for single phase active pfc circuit," in *2017 IEEE International Conference on Environment and Electrical Engineering and 2017 IEEE Industrial and Commercial Power Systems Europe (EEEIC / I CPS Europe)*, June 2017, pp. 1–6.
9. H. Al-bayaty, M. Ambroze, and M. Z. Ahmed, "New effective power terms and right-angled triangle (rat) power theory*, "International Journal of Electrical Power & Energy Systems,* vol. 88, pp. 133–140, 2017.
10. H. A. bayaty et al., "A new power theory (right-angled triangle theory), "in *2015 IEEE Conference on Energy Conversion (CENCON)*, Oct 2015, pp. 451–456.
11. M. T. Zhang, Y. Jiang, F. C. Lee, and M. M. Jovanovic, "Single-phase three-level boost power factor correction converter," in *Applied Power Electronics Conference and Exposition, 1995. APEC '95. Conference Proceedings 1995., Tenth Annual*, no. 0, Mar 1995, pp. 434–439 vol.1.
12. B. AKIN, "Comparison of conventional and interleaved pfc boost converters for fast and efficient charge of li-ion batteries used in electrical cars," in *International Conference on Power and Energy Systems,* vol. 13, 2012.
13. K. Harada and T. Ninomiya, "Optimum design of rc snubbers for switching regulators, *"IEEE Transactions on Aerospace and Electronic Systems*, no. 2, pp. 209–218, 1979.

Appendix B

Presented and Accepted Papers

B.1 IEEE 17th International Conference on Environment and Electrical Engineering (EEEIC), (6-9) June 2017, Italy

Title "A New Design For PFC Circuit With Reduced Size Inductor"

A New Design For PFC Circuit With Reduced Size Inductor

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***Abstract*—A new design of power factor correction (PFC) circuit has been presented in this paper. The new proposed circuit offers a reduced size of (98%) of the conventional PFC inductor (as the inductor's value decreased to $10\,\mu H$) therefore, the weight and the cost will be reduced tremendously.**

Consequently, the use of a minimum number of passive components and reducing the amount of magnetics can reduce the losses and the voltage spikes on the switches. In addition, this topology can be considered as a snubberless circuit due to the presence of freewheeling diode which avoids over current issues.

Simultaneously, the optimum values of low total current harmonic distortion (THD_I), high input power factor (PF), high efficiency and flexible output ripple voltage can be achieved when the switches pulses are manage to eliminate the 3rd order harmonics without needing to use an external control circuit.

This circuit has been designed and investigated using Ltspice-Simulink program. The optimum values can be concluded from the simulation results.

Keywords : AC - DC Converter, Active Power factor correction (APFC), Total Harmonic Distortion (THD).

I. INTRODUCTION

Nowadays, most of the modern electronic devices use some form of AC to DC power conversion within their architecture and, these power converters draw pulses of current from the AC power system which impact negatively on the network during each half cycle of the supply waveform [1].

The amount of power distortion caused by a single device (mobile phone for example) may be small, but this amount increased within a big population excluding other apparatus that drawing distortion power from the same phase supply, resulting in a significant amount of distorted current flow and generation of harmonics. The effect of poor power factor and harmonics generated by equipments that can be connected to the public mains network is an issue of concern nowadays [2].

Low power factor can cause serious problems for electric utility systems, such as lower power capacity, lower efficiency, interference with communication and control signals, errors in metering and additional heating [3].

Excessive harmonics, seriously deteriorate the power quality and efficiency of the power system. At higher power levels (200 watt and higher), these problems become even more sever and thus harmonics must be filtered [4].

PFC circuit, can significantly minimize losses and costs associated with the generation and distribution of the electric power with significantly improved power quality. Therefore, PFC circuit is receiving more and more attention these days because of the widespread use of electrical appliances that draw non sinusoidal current from the electric power systems [4].

The need of novel topologies comes as an important issue in order to introduce a PFC circuit has these specifications: High power factor rectifier with reduced harmonics at the input side, high efficiency, reduced size of magnetics, increased robustness [5].

The essential points regarding each structure of PFC circuit are: The complexity of design and control, conduction losses, inductor size, number of components, output voltage gain (ripple factor) [5].

In addition to reducing the size of the inductor for PFC, the proposed circuit has a unique advantage which is the ability to change the ripple value of the output DC current or voltage in accordance with the input PF and THD values without using an external control circuit.

In this paper, a new design of PFC converter has been introduced and presented in Fig. (1). The new design based on the flexibility of the parameters' variation which produces low ripple output voltage, high input PF and low input THD_I.

One of the main concerns of the pfc converters for high power or high voltage applications is the inductor's volume and weight, which can affect the converter cost and power density [6].

The new proposed design, reduces the amount of magnetics as the new design focuses on eliminating the third order harmonic current and shifts the harmonics to the high frequency region, therefore, the value of the inductor has been reduced more than 98% in comparison with the used inductors in the conventional boost converters.

The required value of the inductance for the same voltage and power ratings in the three level boost converter is (L), while the size would be doubled with the using of two inductors (2x2L) for the interleaved boost converter and the inductance would be doubled again (4L) for the conventional boost converter [6]. The inductor's value used in the literature in [7] for 3 kw output power using interleaved boost converter was ($270\,\mu H$) which is considered as a half value of conventional boost converters, while the value of inductor (L_1) in the new proposed circuit is ($10\,\mu H$) for the same power. This reduction of the inductor's value will effectively reduce the size, weight and the cost of the converter.

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The description of the circuit and operation topology are described in section (II). Simulation results and assessments are presented in section (III) followed by a conclusion in section (IV).

II. Operation principles of the proposed circuit

A. Circuit's Description

The circuit schematic of the new PFC circuit is shown in Fig. (1), where V_S is the input single phase AC source, which is connected to full bridge rectifier with one free-wheeling diode (FWD), switch SW_1, switch SW_2 (represent power electronic devices e.g. MOSFET) which can be work in different modes and different switching frequencies, (L) inductor, C_1 main capacitor and small valued capacitor C_2 are all connected in parallel with a resistive load.

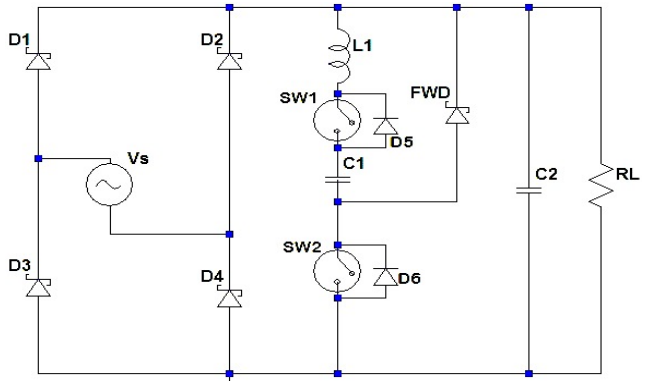

Fig. 1. New proposed PFC circuit

B. Operation Topology

The new designed circuit can changes the value of the input power factor (PF), THD_I of the source current waveform and the value of the output ripple load voltage by using two MOSFETs (SW_1 & SW_2) and series LC-circuit connected in parallel with the load and the input supply.

The new circuit has been designed depending on the principle of dividing the working time of the main capacitor C_1 via switching MOSFET-1 in 50 Hz, but chopped its current into three regions: ON, OFF, ON and maintaining the duty cycle of SW_1 to works in a fixed time periods. The control of chopping process of MOSFET-1 has been made simply (without external complex control circuit) by using two parallel sources work in different periods (this periods are flexible and easy to change desirably).

Accordingly, SW_1 prevents C_1 of working in the (OFF) time (which is the peak value of the waveform), that will result in decreasing the effect of C_1 on the input current, eliminates the third order harmonic component and improve the input PF. At the same time, SW_1 will shift all the harmonics components to high frequency region which reduces the probability of using bulky low frequency filter (as the frequency inversely proportion with square of LC), therefore the design would require less number of components and less values. Consequently, reduces the size, weight and the cost of the new designed circuit.

SW_2 reduces the effect of the inductor current's spikes and reduces the charging time of (I_{C1}) which decreases the losses and improves the efficiency, at the same time helps to improve the output waveform and reduce the ripple dc voltage.

C_2, is a small value capacitor (and its not compulsory). The duty of C_2 is to suppress the high frequency spikes at the output load waveform.

The freewheeling diode (FWD) offers a unidirectional way for (I_L), therefore I_L will remain on a positive value. Accordingly, (FWD) prevent the negative part of I_L and helps C_1 to act as a snubber circuit in order to prevent V_L (which is the negative value of V_{sw2} when SW_2 is OFF) to increase more than rated value of the source voltage, which protects the circuit in general and specially the MOSFET switches from being burned because of the high voltage spikes.

III. Simulation Results and Assessment

The proposed design is shown as an electrical circuit with V_S = 311 V_{peak} = 220 V_{rms}, L = 10 µH, C_1 = 1 mF, C_2 = (1 µF) and has been designed and investigated using Lt-spice simulink program.

Duty cycle of SW_1 = 60% in two time intervals. The first period is ($0 \leq t < t_2$) = 30% of full period, and the second period is ($t_3 \leq t <$ 10ms.) = 30% of full period. Duty cycle of SW_2 = 40% with switching frequency f_{sw2} = 200 KHz.

1) R-load, (L), the duty cycle of SW_1 (D_1), the switching frequency of SW_2 and (D_2) which is the duty cycle of SW_2, are the five main parameters in this circuit which could be changed in different values in order to examine the validity of the proposed circuit and find out the optimum design and values of the parameters in order to get minimum input THD_I, maximum unity input PF and low output ripple voltage, cost effective, non bulky, small size converter.

2) Table (I) shows the relationship between different load values comparing it with fundamental input current I_1, THD_I, input PF and main capacitor voltage (V_{C1}), when L = 10 µH and the duty cycle (D_2) of SW_2 is 40% and V_{out} is approximately 309 peak volt.

TABLE I
Different load values with I_1, THD_I, PF and V_{C1}

Load (Ω)	**I-1** (A)	**THD-I**(%)	**PF**	**Vc1**(V)
1	211.6	7	0.998	92.5
10	22.6	14	0.99	107
20	11.65	19	0.982	124
50	4.96	31.7	0.953	148
100	2.68	41.8	0.92	165
200	1.53	55.6	0.88	181
500	0.85	84	0.77	197
1000	0.62	110	0.67	205

Power factor has been calculated by using equation in [8], P.F = $\frac{1}{\sqrt{1+(THD_I)^2}}$

$$I_h = I_1 * THD_I$$

the values of I_1 & I_h are essential to calculate the total source current of the circuit for each case, [9].

$$I_t = \sqrt{I_1^2 + I_h^2}$$

The input power is almost 5 KW when R-load = 10 Ω and I_1 = 22.6 A, and the output power is more than 4.9 KW, thus the efficiency is more than 98%.

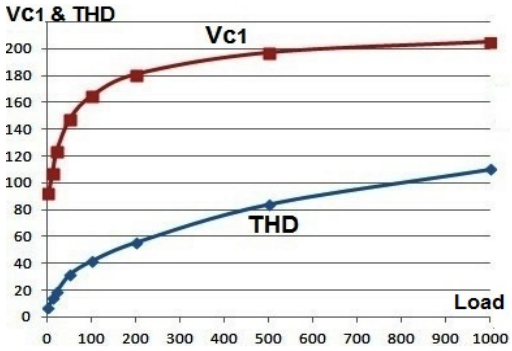

Fig. 2. Different load values with THD_I and V_{C1}

It can be concluded, from table (I) and Fig. (2), that the value of THD_I and capacitor voltage (V_{C1}) directly proportion with the resistive load value and inversely with the input power factor.

3) Table (II), shows the relationship between different inductor values comparing with THD_I, input PF and main capacitor's voltage V_{c1}, when R-load = 10 Ω and D_2 = 40%.

TABLE II
DIFFERENT (L) VALUES WITH THD_I AND $V_{c1}(V)$

L(uH)	**I-1** (A)	**THD-I** (%)	**PF**	**Vc1**(V)
0.1	28.5	66.2	0.83	231
1	25	40.7	0.926	173
10	22.6	14	0.99	107
20	22.46	12.2	0.992	95
50	22.4	9.5	0.995	95
100	22.3	8.9	0.996	92.6
200	22.33	8.8	0.996	89
500	22.2	8.5	0.996	83.3
1000	22.1	7.5	0.997	78.8

It can be concluded, from table (II) and fig. (3), that the value of (L) inductor directly proportion with the input PF value and inversely proportion with the values of THD_I and (V_{C1}).
A value of (L) more than 50 µH, can cause a high V_L due to high f_{sw2} which causes high $\frac{di_L}{dt}$ at the same time, the output voltage ripple will increase with the increasing of (L).

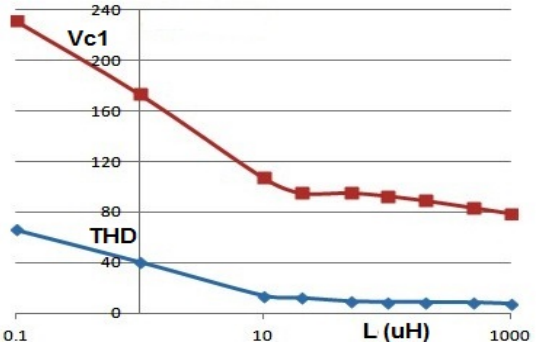

Fig. 3. Different (L) values with THD_I and V_{C1}

4) Table (III), shows the relationship between different duty cycles of SW_2 comparing with THD_I, input PF and the main capacitor voltage (V_{C1}), when R-load = 10 Ω.

TABLE III
VARIABLE DUTY CYCLES FOR SW_2 WITH THD_I AND V_{C1}

D2(%)	**I-1** (A)	**THD-I** (%)	**PF**	**Vc1**(V)
10	21.9	3.8	0.999	52.2
20	22.1	7.2	0.997	75.3
30	22.4	10.9	0.994	92.7
40	22.7	14	0.99	107
50	23	18.6	0.983	121.2
60	23.7	28.2	0.963	145.8
70	24.6	37.7	0.936	171.2
80	26	53.6	0.88	197
90	28.4	67.7	0.83	222

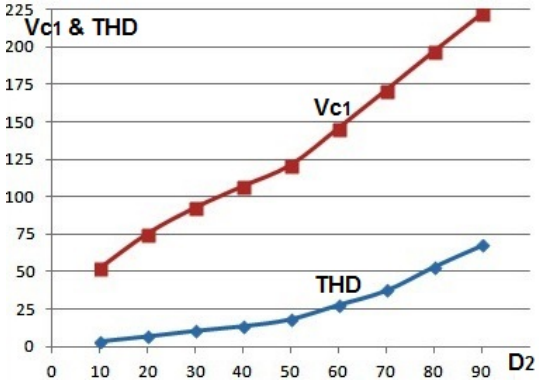

Fig. 4. Values of duty cycle for SW_2 vs. THD_I and V_{C1}

It can be concluded from table (III) and fig. (4) that, the value of THD_I and output voltage (V_{C1}) directly proportion with the value of D_2 and inversely with the input power factor. From the results, its better to keep the value of D_2 less than 50% in order to get a unity PF at the input side when (L) is 10 µH and approximately 5 kw output power.

5) Table (IV), shows the relationship between different duty cycles of SW_1 with equal off period from zero to t_2 and from t_3 to $\frac{T}{2}$. These values has been compared with

THD_I, input PF and (V_{C1}), for each case when R-load = 10 Ω and L = 10 µH.

TABLE IV
VARIABLE DUTY CYCLES FOR SW_1 WITH THD_I AND V_{C1}

D1(%)	I-1	THD (%)	PF	Vc1	(t1-t2)ms
10	21.6	0	1	18.5	0.19-0.5
20	21.8	2.7	0.999	37.3	0.38-1
30	21.9	5.6	0.998	57.3	0.55-1.5
40	22.1	8.4	0.996	73.6	0.72-2
50	22.3	10.9	0.994	93.4	0.86-2.5
60	22.6	14	0.99	107	1 - 3
70	23	17	0.986	121.3	1.1-3.5
80	23.4	19.2	0.982	134.7	1.2-4
90	23.8	21.3	0.98	147.7	1.3-4.5
100	24.3	23	0.97	160	1.4-5

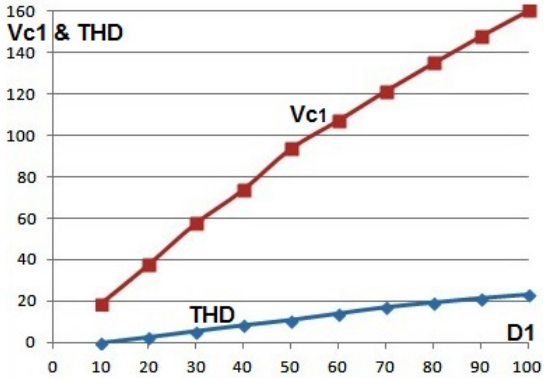

Fig. 5. Values of duty cycle for SW_1 vs. THD_I and V_{out}

Its good to keep the value of D_1 less than 70% in order to get a unity PF at the input side when D_2 is 40%, and 4.9 KW output load power.
It can be concluded from table (IV) and fig.(5) that, the value of THD_I and (V_{C1}) directly proportion with the value of D_1 and inversely with the input PF.
The value of $(t_1 - t_2)$ is directly proportion with the increasing of duty cycle of SW_1 and the value of THD_I and inversely with the PF values.

6) Table (5) shows the relationship between different SW_2 frequencies comparing it with fundamental input current I_1, THD_I, input PF and output voltages (V_{C1}), when $R_L = 10\Omega$, L = 10 µH and the duty cycle (D_2) of SW_2 is 40% and $V_{max.}$ is almost 309 peak volt.
It can be concluded, from table (V) and fig. (6), that the input PF and output ripple factor directly proportion with switching frequency of SW_2 and inversely with the value of THD_I and capacitor voltage (V_{C1}).
In addition, the table(V) shows that, the optimum value of f_{SW2} might be more than 50 Khz, in order to get a unity PF at the input side when (L) is 10 µH and approximately 5 kw output power, as the harmonics increase with low switching frequency.

TABLE V
DIFFERENT LOAD VALUES WITH THD_I AND $V_{C1}(V)$

f-sw2(KHz)	I-1 (A)	THD-I	PF	Vc1
5	27.12	62.5	0.85	209.6
10	26	51.4	0.89	191.5
50	23.6	27.2	0.96	144
100	23.1	20	0.98	124.4
150	22.82	16.5	0.986	115
200	22.66	14	0.99	107
250	22.53	13	0.991	102
300	22.53	12.8	0.992	101.3
350	22.52	12.7	0.992	101
400	22.48	12.3	0.992	100.3
500	22.47	12	0.993	99.2

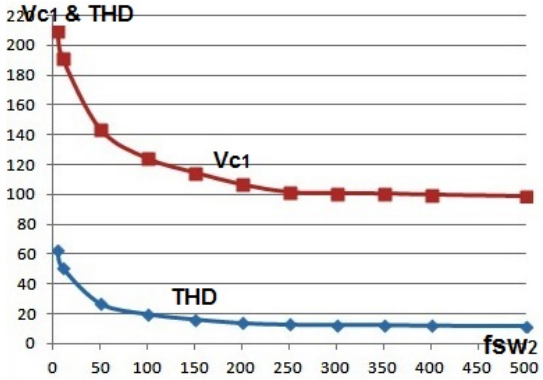

Fig. 6. Different load values with THD_I and $V_{min.}$

From the aforementioned tables (I, II, III, IV & V), it's easy to find out the optimum values of the proposed circuit (including $f_{sw2}, D_1, D_2 \& L$) when R-load = 10Ω which can achieve (0.99) power factor and minimum magnetics value.

7) Fig. (7) below shows the input source current waveform (I_S) with the different time modes for each cycle:

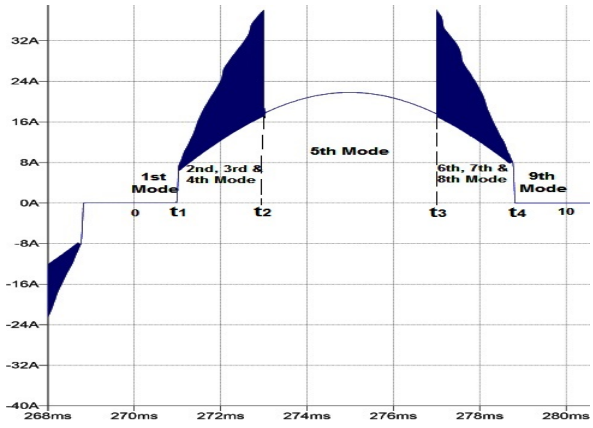

Fig. 7. The input source current

The FFT spectrum of the source current has been shown in Fig. (8). The total current harmonic distortion (THD_I) is 14%, then the input power factor is almost

unity (0.99).The third order harmonic has been eliminated, the 5th and 7th orders are the most predominant orders due to the switching pattern which turns OFF the main capacitor (C_1) from 3ms. to 7 ms. and the load was fed by the source.

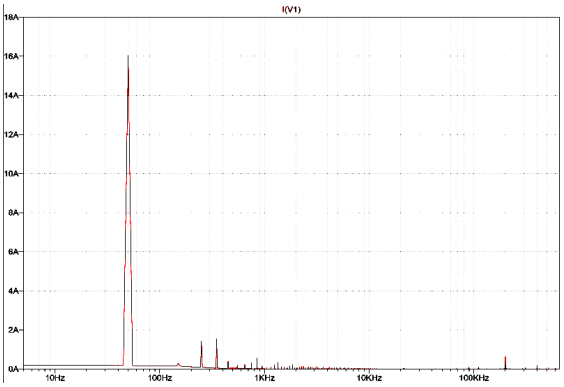

Fig. 8. FFT Spectrum of the input current

8) For time intervals $t_1 \leq t < t_2$ and $t_3 \leq t < t_4$ (which represent the 2nd and 6th modes), the equation of inductor's voltage is:

$V_L = L\frac{di_L}{dt} = \frac{L.di_L.f_{sw2}}{D}$

(D_2) is the duty cycle of SW_2 and because of the switching frequency of SW_2 (f_{sw2}) is (200 KHz), therefore V_L would be a very large value at this moment. Consequently, V_L may be reason of huge spikes on SW_1's terminals and may burn the switch. However, the value of V_L can kept small and less than the rated voltage because (L) value is very small (10 µH) and thats will decrease inductor voltage tremendously.

9) For whatever reason, if the designer needs to use a high value of (L) then the value of V_L would be high again with the presence of high frequency switching of SW_2 because of the high change in $\frac{di}{dt}$.
For this situation, a snubber circuit could be proposed as a solution to suppress the high frequency spikes and to protect the MOSFET switch. However in this circuit, the main capacitor (C_1) would act as a snubber circuit because of the existence of the freewheeling diode (FWD), which make V_{C1} charge in the negative value of V_L and prevent high voltage on th SW_1 when its in open status.

10) The waveform of the main capacitor's voltage (V_{C1}) looks concave when its charging when $t_1 < t \leq t_2$ while it looks convex shape when $t_3 < t \leq t_4$.
The interpretation for this phenomenon is as follows:

$\because I_{C1} = C_1\frac{dV_{C1}}{dt} \quad \Rightarrow \quad \therefore V_{C1} = \frac{1}{C_1}\int I_{C1}(t)dt$

The original waveform of $I_{C1}(t)$ is a sine wave:

$I_{C1}(t) = I_{C1}\sin(wt)$

$V_{C1} = \frac{1}{C_1}\int I_{C1}(t)dt$

For: $t_1 < t \leq t_2$

$$V_{C1} = \frac{1}{C_1}\int_{\frac{180t_1}{0.01}}^{\frac{180t_2}{0.01}} I_{C1}(t)dt$$

$$V_{C1} = \frac{I_{C1}}{C_1}\int_{\frac{180t_1}{0.01}}^{\frac{180t_2}{0.01}} \sin(wt)dwt$$

$$V_{C1} = \frac{I_{C1}}{C_1}\big[-\cos(wt)\big]\Big|_{\frac{180t_1}{0.01}}^{\frac{180t_2}{0.01}}$$

The waveform is a concave shape at this time period.

For: $t_3 < t \leq t_4$

$$V_{C1} = \frac{1}{C_1}\int_{\frac{180t_3}{0.01}}^{\frac{180t_4}{0.01}} I_{C1}(t)dt$$

$$V_{C1} = \frac{I_{C1}}{C_1}\int_{\frac{180t_3}{0.01}}^{\frac{180t_4}{0.01}} \sin(wt)dwt$$

$$V_{C1} = \frac{I_{C1}}{C_1}\big[-\cos(wt)\big]\Big|_{\frac{180t_3}{0.01}}^{\frac{180t_4}{0.01}}$$

The waveform is in a convex shape at this period.

Obviously, the integral of different phase angles results in a different part of the (-cos) waveform shape and that's explain the reason of being V_{C1} in different wave shapes in these two periods in spite of they both represent the charge period for C_1.

The same interpretation is valid for the shape of V_L waveform because C_1 and L in series so I_{C1} is equal to I_L.

$I_{C1}(t) = I_L(t) = I_{C1}\sin(wt)$

$V_L(t) = \frac{di_L}{dt} = L.I_{C1}\cos(wt)$

The output load voltage V_{out} is shown in fig. (9).
V_{out} which is V_{C2} swings between $V_{max.}$ and $V_{min.}$.

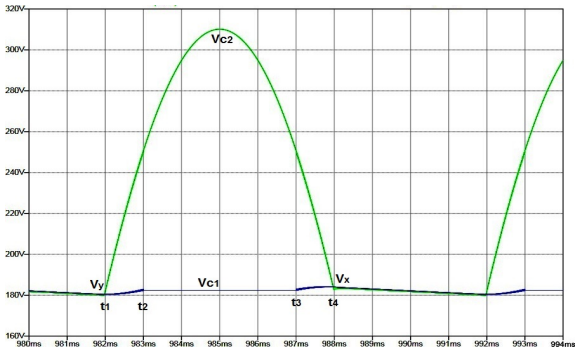

Fig. 9. Output Voltage V_{C2} and V_{C1} waveforms

V_x which is the higher value of the minimum output voltage is corresponds with t_4, while V_y which is the lower value of the minimum output voltage is corresponds with t_1.

The length of the slope line $(V_x - V_y)$ changes with the value of D_2 as seen in the simulation's result.

11) Other important aspect to be investigated in this circuit, is the size of the inductor. The required value of the inductance for the same voltage and power ratings in the three level boost converter is (L), while the size would be doubled with the using of two inductors (2x2L) for the interleaved boost converter and the inductance would be doubled again (4L) for the conventional boost converter [6].
The inductor's value used in the literature in [7] for 3 kw output power using interleaved boost converter was (270 µH), while the value of inductor (L) in the new proposed circuit is (10 µH) for the same power. This reduction of the inductor's value will effectively contribute in reducing the size, weight and the cost of the converter.

12) Another important advantage of this design, is that the inductor's current is not related to the value of source voltage (except in the 2nd and 6th mode) as usual, this attribute can gives the designer a big tolerance to reduce the value of (L) into few micro henres and avoid high V_L values.

13) The inductor's current I_L in 4th and 8th modes is in discontinuous conduction mode (because of the parasitic resonance) which could causes high reverse inductor voltage V_L because of the very high $\frac{di}{dt}$. However, as shown in Fig. (10), the inductor voltage does not increases more than 140 V_{P-P} in spite of that the source voltage is 311V_{P-P}, because of the small value of (L).

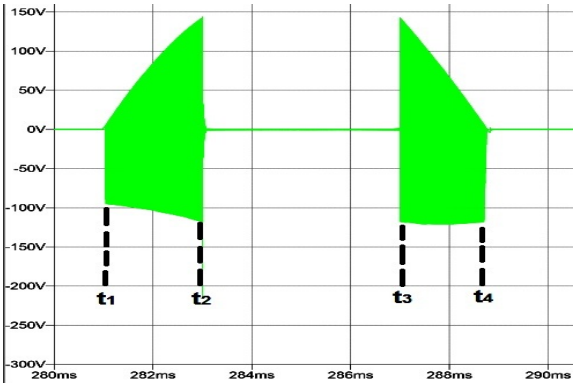

Fig. 10. The waveform of V_L

14) The internal capacitance of the diodes combines with stray inductance and form a resonant circuit called parasitic resonant. Many methods are existing in order to attenuate this resonance, but most of them had some bad effects on the performance of the circuit like controlling the rise time which reduces the power efficiency [10], or adding a damper circuit or using clamping diodes and that requires additional components and add complexity to the design [11].

15) Fig. (11), shows the inductor current (I_L), which is at the same time, the capacitor current (I_{C1}) (because (L) is connected in series with C_1) with the pulses of SW_1 when V_S = 220 V_{rms}, R-load = 10 Ω. The power delivered to the load is about 5 kw, THD_I = 14% and input PF = 0.99.

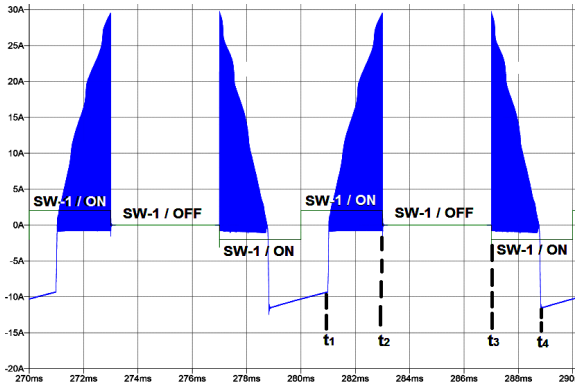

Fig. 11. I_L with SW_1 pulses

16) The main inductor (L) is acting as a choke or current limiter due to the high negative value of V_L as its in counter direction of capacitor voltage V_{C1}.
The inductor, charges in the time period $t_1 \leq t < t_2$ because $V_S > V_{C1}$. On the other hand, for the time period$t_2 \leq t < t_3$, I_L is zero because (L) and C_1 are reverse biased. While, for the time period $t_3 \leq t < t_4$, inductor (L) discharges as a positive current because $V_S > V_{C1}$.
However, for time period $t_4 \leq t < t_1$ of the next period, (L) discharges as a negative current because $V_{C1} > V_S$ and the R-load would be fed by I_L which is the same capacitor's current $(I_{C1} = I_L)$.
It is required to separate all the operation modes into their time intervals, in order to understand the full function of (I_L). Full time period (T) for output waveform is 10 msec, because the frequency is 100 Hz for full wave bridge rectifier.

$$I_L = \begin{cases} \frac{V_{out}}{R} - I_{C2} & 0 < t \leq t_1 \\ & t_1 < t \leq t_2 \\ I_s - I_{C2} - \frac{V_{out}}{R} & S_2\text{-ON} < t \leq S_2\text{-OFF} \\ C_1 \frac{dV_{C1}}{dt} & S_2\text{-OFF} < t \leq t_d \\ I_0 . \cos(w_r t) & t_d < t \leq S_2\text{-ON} \\ \text{Zero} & t_2 < t \leq t_3 \\ & t_3 < t \leq t_4 \\ I_s - I_{C2} - \frac{V_{out}}{R} & S_2\text{-ON} < t \leq S_2\text{-OFF} \\ C_1 \frac{dV_{C1}}{dt} & S_2\text{-OFF} < t \leq t_d \\ I_0 . \cos(w_r t) & t_d < t \leq S_2\text{-ON} \\ \frac{V_{out}}{R} - I_{C2} & t_4 < t \leq 10 \end{cases}$$

In order to fully understand the performance of the circuit, the same process of piecewise equations might be applied on (V_{C1}) and (V_{out}) which are the voltages of C_1 and C_2 respectively.

$$V_{C1} = \begin{cases} V_{C2} - V_L & 0 < t \leq t_1 \\ & t_1 < t \leq t_2 \\ V_{C2} - V_L & S_2\text{-ON} < t \leq S_2\text{-OFF} \\ V_{C2} + V_L - V_{D6} & S_2\text{-OFF} < t \leq t_d \\ V_{C2} - V_L - V_{D6} & t_d < t \leq S_2\text{-ON} \\ \text{Constant value} & t_2 < t \leq t_3 \\ & t_3 < t \leq t_4 \\ V_{C2} - V_L & S_2\text{-ON} < t \leq S_2\text{-OFF} \\ V_{C2} + V_L - V_{D6} & S_2\text{-OFF} < t \leq t_d \\ V_{C2} - V_L - V_{D6} & t_d < t \leq S_2\text{-ON} \\ V_{C2} - V_L & t_4 < t \leq 10 \end{cases}$$

$$V_{C2} = \begin{cases} V_{C1} + V_L & 0 < t \leq t_1 \\ & t_1 < t \leq t_2 \\ V_{C1} + V_L & S_2\text{-ON} < t \leq S_2\text{-OFF} \\ V_{C1} - V_L + V_{D6} & S_2\text{-OFF} < t \leq t_d \\ V_{C1} + V_L + V_{D6} & t_d < t \leq S_2\text{-ON} \\ V_S & t_2 < t \leq t_3 \\ & t_3 < t \leq t_4 \\ V_{C1} + V_L & S_2\text{-ON} < t \leq S_2\text{-OFF} \\ V_{C1} - V_L + V_{D6} & S_2\text{-OFF} < t \leq t_d \\ V_{C1} + V_L + V_{D6} & t_d < t \leq S_2\text{-ON} \\ V_{C1} + V_L & t_4 < t \leq 10 \end{cases}$$

The piecewise equations above illustrate the relationship between inductor current I_L, capacitor voltage V_{C1} and output voltage V_{C2} with the different parameters of the circuit which can change the design of the circuit according to the desired results.

IV. Conclusion

This paper presents a new topology of ac/dc PFC circuit. The results of the simulation proved the validity of the new proposed design and has the ability to deliver a controlled output current or voltage and reduce THD at the source side to 14% with almost unity (0.99) input PF.

The novel style of switching SW_1 depended on decreasing the operation time of the main capacitor (C_1) into 60% or less of each cycle in respectively (ON-OFF-ON) pattern. This pattern prevented (C_1) from drawing the source current at the peak of the period (which is the main reason of the non sinusoidal current). Consequently, the third order harmonic would be eliminated successfully and the PF improved.

Furthermore, the harmonics current would be shifted to the high frequency region which reduces the size of used filter and reduces the value of the main inductor to $10\,\mu$H which is (2%) of the size of the inductor used in the conventional boost PFC ($540\,\mu$H). The decreasing of the inductor size would decrease the produced losses. Accordingly, the new design will reduce the size, weight, and the cost of the converter tremendously.

The new circuit has many additional advantages, like the simplicity as it is a snubberless circuit (due to the use of freewheeling diode), and does not require an external control circuit.

Finally, this design gives the ability to the users to change the value of the output ripple flexibly in compromising with the input PF and THD values.

References

[1] H. Al-bayaty, M. Ambroze, and M. Z. Ahmed, "Feeding loads via harmonics utilization in ac circuit systems," in *2016 International Conference for Students on Applied Engineering (ICSAE)*, Oct 2016, pp. 224–227.

[2] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of single-phase improved power quality ac-dc converters," *IEEE Transactions on Industrial Electronics*, vol. 50, no. 5, pp. 962–981, 2003.

[3] H. Al-bayaty, M. Ambroze, and M. Z. Ahmed, "Utilization of harmonics current in single phase system," in *2016 17th International Conference on Harmonics and Quality of Power (ICHQP)*, Oct 2016, pp. 443–447.

[4] S. Basu, *Single Phase Active Power Factor Correction Converters-Methods for Optimizing EMI, Performance and Costs*. Chalmers University of Technology, 2006.

[5] J. P. M. Figueiredo, F. L. Tofoli, and B. L. A. Silva, "A review of single-phase pfc topologies based on the boost converter," in *Industry Applications (INDUSCON), 2010 9th IEEE/IAS International Conference on*, Nov 2010, pp. 1–6.

[6] M. T. Zhang, Y. Jiang, F. C. Lee, and M. M. Jovanovic, "Single-phase three-level boost power factor correction converter," in *Applied Power Electronics Conference and Exposition, 1995. APEC '95. Conference Proceedings 1995., Tenth Annual*, no. 0, Mar 1995, pp. 434–439 vol.1.

[7] B. AKIN, "Comparison of conventional and interleaved pfc boost converters for fast and efficient charge of li-ion batteries used in electrical cars," in *International Conference on Power and Energy Systems*, vol. 13, 2012.

[8] W. M. Grady and R. J. Gilleskie, "Harmonics and how they relate to power factor," *Proceedings of PQA93*, 1993.

[9] H. Al-bayaty, M. Ambroze, and M. Z. Ahmed, "New effective power terms and right-angled triangle (rat) power theory," *International Journal of Electrical Power & Energy Systems*, vol. 88, pp. 133–140, 2017.

[10] K. Kam, D. Pommerenke, F. Centola, C. Lam, and R. Steinfeld, "Method to suppress the parasitic resonance using parallel resistor and inductor combination to reduce broadband noise from dc/dc converter," in *EMC*, vol. 9, 2009, pp. 20–24.

[11] K. Harada and T. Ninomiya, "Optimum design of rc snubbers for switching regulators," *IEEE Transactions on Aerospace and Electronic Systems*, no. 2, pp. 209–218, 1979.

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Title "Third Order Harmonic Elimination Technique For APFC Circuit"

Third Order Harmonic Elimination Technique For APFC Circuit

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***Abstract*—This article presents a new design of active power factor correction (APFC) circuit that can be used in single phase rectifiers. The proposed circuit provides almost a unity input power factor (PF) which contributes significantly in reduction of the total current harmonic distortion (THD_I) as it eliminates the third harmonic component effectively from the input current.**

The most important attribute of this circuit is the small size and numbers of components (one switch, small size (L & C) and a diode), which have been designed to get a unity PF at the AC source side. Therefore, the new circuit is cheaper, smaller size and lighter than other conventional PFC circuits.

In addition, the new proposed circuit is a snubber-less and uses reasonably low switching frequency which reduces switching losses and increases efficiency. The circuit has been designed and simulated using Lt-spie simulink program.

Keywords : Active power factor correction (APFC), AC - DC Converter, Total Harmonic Distortion (THD).

I. Introduction

Single phase AC - DC rectifiers with a large electrolytic capacitor are commonly used for manufacturer and business issues. The main purpose to use diode rectifiers is to operate the switching power supply in data processing apparatus and to operate low power motor drive systems [1].

The large capacitor draws current in short pulses, which brings in a lot of problems including decreasing in the available power, increasing losses and reduction of the efficiency. In the conventional way of design, the capacitor voltage preserves the peak voltage of the input sine wave until the next peak comes along to recharge it [2].

The only way to recharge the capacitor is drawing the current from the input source at the peaks of the source waveform as a long pulse which includes an adequate amount of energy to nourish the load until the next peak. This is happens when the capacitor draws a large charge during short time, after the slowly discharge of the capacitor into the load. Therefore, the capacitor's current draws 5 to 10 times of the average current in 10% or 20% of the cycle period. Consequently, the source current has narrow and long pulses and the effective (r.m.s.) value increases [3].

Customers with a large number of nonlinear loads also have large neutral current rich in third harmonics current.In order to increase the PF, decrease the losses and save the energy, then the input current harmonics (specially the third order harmonic) have to be eliminated. Several methods and techniques have been proposed to solve the problem of a poor power factor, which can be classified as active and passive methods [4].

Passive PFC circuits are generally simple, fewer components, smaller size and easy to design for small rating power (less than 200 watt). However, its bulky and not economical for large power ratings and the input power factor is (0.6 - 0.7) and THD = 150% in best conditions without using big size elements [5].

Active PFC circuits, can considerably diminish losses and costs associated with the generation and distribution of the electric power and significantly improved power quality. Therefore, APFC circuits are receiving more and more attention these days because of the widespread use of electrical appliances that draw non sinusoidal current from the electric power systems . However, APFC requires additional, more expensive and complex components [6].

In this paper, a new design of PFC converter has been introduced and presented in Fig. (1). The new design is depending on the flexibility of the parameters' variation which produces low harmonics, high input PF and efficiency.

The new proposed design, reduces the required number of components and decreases the value of the inductor more than 96% of the inductors used in conventional boost PFC circuits, because the new proposed design focuses on shifting the harmonics components to the high frequency region and consequently eliminating the third order harmonic current, therefore the cost, the weight and the size of the new circuit will be reduced hugely.

The description of the circuit, operation topology, control circuit and operation stages are described in section (II). The discussion of simulation results and assessment are presented in section (III), followed by an over all conclusion in section (IV).

II. Operation principles and analysis of the proposed circuit

A. Circuit's Description

The schematic circuit of the new proposed PFC circuit is shown below in Fig. (1).

(V_S) is the input DC source (represents AC single phase connected to full bridge rectifier), connected in parallel with LC resonant branch and MOSFET switch (SW) in parallel with the load. A control circuit has been designed in order to control the switching process.

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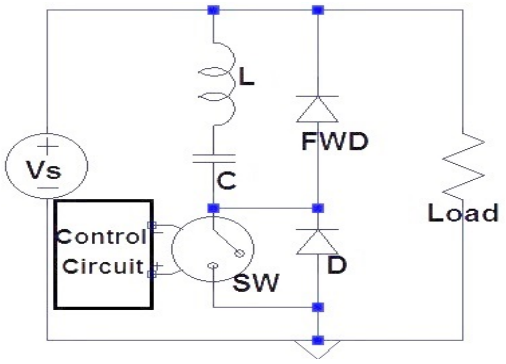


Fig. 1: New proposed APFC circuit

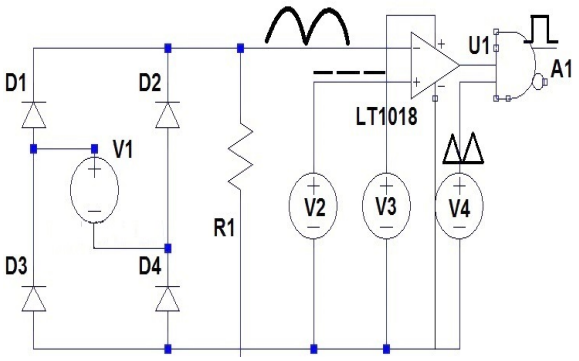


Fig. 2: Control circuit

B. Operation Topology

The new proposed circuit has the ability to control the working period of the capacitor. Consequently, the value of the input power factor, THD_I of the source current waveform and the value of the output ripple voltage can be controlled as well through using one switching devices.

The principle of this design is depending on the distributing of the working time intervals of the capacitor into two regions, at the beginning (0 - t_1) and at the end ($t_4 - \pi$) via using control circuit. This smart switching pattern would eliminates the third order harmonic component and improves the input PF as the 3rd order is the most significant component in single phase systems.

This design uses a minimum number of components and minimum values of (L) & (C) as capacitor turned off on the middle of each cycle, which shift the harmonics components to higher frequencies. consequently, reduces the size and the cost of the new proposed circuit.

This circuit is snubber-less circuit, because the freewheeling diode (FWD) presents an alternative path for the discharge current of inductor (I_L), so can the capacitor keep charged. Accordingly, (FWD) can avoids the negative part of I_L and helps (C) to act as a snubber circuit in order to prevent the inductor's voltage (V_L) to increase more than rated value of the source voltage, in this way (C) will protect the MOSFET switch from being burned in the effect of the high voltage spikes which may happened without the FWD.

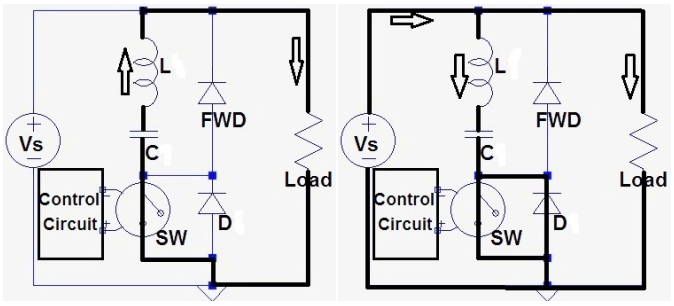
C. Control circuit

A simple designed control circuit, as shown in Fig. (2) has been investigated in order to derive the MOSFET switch and control the switching frequency and duty cycle.

Briefly, the circuit consists of a dual input comparator which compares two signals(the first signal is the output of full wave rectifier and the second is a dc voltage source). The output of the comparator, which is a square wave, would be combine in a logic (and gate) circuit with a triangular waveform in 20 KHz frequency. the output of and gate will go directly to the gate of the MOSFET switch.

D. Operation stages

1) First mode: This mode describes the time period $0 \leq t < t_1$, when $V_C > V_S$. SW-ON/OFF, while t_1 is the moment when V_S is equal or bigger than V_C. The circuit shown in Fig. (3-a), illustrates the path of the current at this mode:



(a) 1st & 9th mode

(b) 2nd & 6th mode

(c) 3rd & 7th mode

(d) 4th, 5th & 8th mode

Fig. 3: Circuit diagram in different time modes

(C & L) are discharging and feed the load.

$I_C = C\frac{dV_C}{dt} = I_L = I_{Load} = \frac{V_{out}}{R}$

because L, C and the load are series in this mode.

$\therefore V_{Load} = V_{out} = V_C + V_L$

$\because V_L = L\frac{di_L}{dt}$, then the value of V_L is approximately zero because the value of L_1 is very small (few micro henres). $\therefore V_{out} \approx V_C$

2) Second mode: For the time period $t_1 \leq t < t_2$, when $V_S > V_{C1}$, and SW is ON. t_2, is the moment when the pulses turns off. The circuit shown above in Fig. (3-b), the bold line illustrates the active path at this mode.
In this mode, the load, C & L are all connected to the source and charging with frequency pulses (20 KHz), as a result, high values and short time current spikes appear on the input current waveform because of the capacitor current. $V_S = V_{Load} = V_{out}$

$V_S = V_C + V_L = V_C + L.\frac{di_L}{dt}$ $I_S = I_C + I_{Load} = C.\frac{dV_C}{dt} + I_{Load}$

3) Third mode: For the time period $t_1 \leq t < t_2$, when $V_S > V_{C1}$. This mode covers the interval time from switching OFF moment until (t_d) ms. t_d is the moment when I_L or I_C discharge to zero ampere for each pulse. The circuit is shown above in Fig. (3-c).
At this mode, (L) discharges its current to (C) until being zero (at the t_d moment), while the inductor voltage V_L is equal to V_C and remains charged. This topology dose not require a snubber circuit as V_L has been prevented.

$\because V_L = V_C \quad \& \quad I_L = I_C = C\frac{dV_C}{dt} \quad \therefore X_L = X_C$

$2\pi f L = \frac{1}{2\pi f C} \quad \therefore f_r = \frac{1}{2\pi\sqrt{LC}} = 1.59KHz$

f_r is the resonance frequency.
At this mode, the load is fed by the source.

$V_L = L\frac{di_L}{dt} = V_C$

$I_S = I_{Load} = \frac{V_{out}}{R}$

4) Fourth mode: For the time period $t_1 \leq t < t_2$, when $V_S > V_C$, SW is OFF (from (t_d) until the next ON-pulse). The bold line in the circuit shown above in Fig. (3-d), clarifies the source current's path.
At this mode, the inductor current I_L supposed to remain zero amp. However, the internal capacitance of the diodes combines with stray inductance which form resonant circuit called parasitic resonant. Due to this parasitic resonance, a sinusoidal current can flow into the inductor L_1 in a very high frequency (about 1.54 MHz) called self resonant (or parasitic) frequency (f_p). At the same time, V_L follows I_L waveform and oscillate around zero. as shown in Fig. (4):
V_C remains charged and considered as a constant value due to the value of I_C which is approximately zero, then the value of $\frac{dV_C}{dt}$ is very small value.

$I_L = I_0.\cos(w_p.t)$

w_p = $2\pi f_p \approx$ 9.5 M rad/sec.

I_0 is approximately 0.5 Amp. For ideal conditions, the internal capacitance of diodes is zero, therefore the parasitic resonance and I_0 can considered as zero amp. Practically, a damper circuit (R = 5Ω & C = 1 nF) can be connected in parallel with the freewheeling diode in order to eliminate the resonance current (I_0) totally,

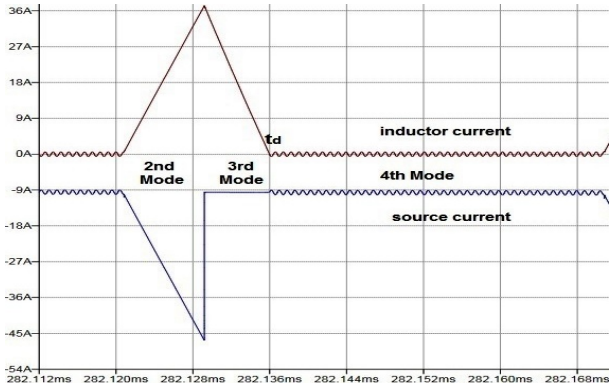


Fig. 4: I_L & I_S in the 2nd, 3rd & 4th modes

however, 0.1 % of power losses can be increased in the circuit as a circuit of 3 kw output power, has only 3 watt losses in the damper circuit which is negligible. The modes (2,3,4) are repeating every ON/OFF switching pulse of SW.

5) Fifth mode: For the time period $t_2 \leq t < t_3$, when pulses are ON/OFF. t_3 is the moment when SW turns OFF. The circuit shown in Fig. (3-d), illustrates the active path of current at this mode:
Due to $V_S > V_C$, therefore C and L are considered as disconnected (open circuit), because they are reverse biased when SW is OFF and and FWD is reverse biased. Therefore, C and L are neither charging nor discharging, then $I_L = I_C$ = Zero, V_L = Zero but V_C is a constant value.

6) Sixth mode: For the time period $t_3 \leq t < t_4$, when $V_S > V_C$, SW is ON. t_4 is the moment when V_C is greater than V_S. The circuit is shown in Fig. (3-b).
At this mode, C and L are charging and the load is fed by the source. All the derived equations in the 2nd mode are valid for this mode.

7) Seventh mode: For the time period $t_3 \leq t < t_4$, when $V_S > V_C$. The circuit is shown in Fig. (3-c).
At this mode, C is charging while V_L is equal to V_C until L fully discharges its current into zero ampere at the time of (t_d).
All the derived equations in the 3rd mode are valid for this mode.

8) Eighth mode: For the time period $t_3 \leq t < t_4$, when $V_S > V_{C1}$, SW is OFF, for period (t_d) until the next ON-pulse for SW_2. The circuit is shown in Fig. (3-d).
V_C still charged and slightly charging but approximately constant due to very small $\frac{dV_C}{dt}$.

V_{C1} remains charged and considered as a constant value due to the value of I_{C1} is approximately zero, then the value of $\frac{dV_{C1}}{dt}$ would be very small.

$I_{L1} = I_0.\cos(w_p.t)$

w_p = $2\pi f_p \approx$ 9.5 M rad/sec.

The modes (6,7,8) repeat themselves every ON/OFF switching of the MOSFET.

9) Ninth mode: For the time period $t_4 \leq t <$ 10 ms., when $V_C > V_S$. SW-ON/OFF , the circuit is shown above in Fig. (3-a).
L & C are discharging while the R-load is fed by the main capacitor.
$\therefore I_L = \frac{V_{out}}{R}$
$V_{Load} = V_{out} = V_C + V_L$

All the derived equations in the first mode are valid for this mode.

III. Simulation Results and Assessment

1) An electrical circuit with V_S = 311 V_{peak} = 220 V_{rms}, L = 20 µH, C = 0.5 mF and MOSFET switch works in f_{sw} = 20 Khz controlled by a control circuit, has been designed and investigated by using Lt-spice simulink program.

2) R-load, inductor (L) and switching frequency of the MOSFET, are three main parameters in this circuit which could be changed in different values in order to find out the optimum design and parameters values in order to get low input THD_I, unity input PF, high efficiency, cheap, not bulky, small size and light converter .

3) Table (I) shows the relationship between different load values comparing it with fundamental input current P_{in}, P_{out}, η, THD_I and input PF when L = 20 µH and the switching frequency (f_{sw}) is 20 Khz.

TABLE I: Different load values with THD_I, PF & η

R(Ω)	P_{in}(W)	P_{out} (W)	η(%)	**THD**(%)	**PF**
1	46354.5	44260	95.48	5	0.999
10	4920.2	4851.5	98.6	11.6	0.994
20	2506	2473	98.68	17	0.986
50	1038	1021	98.36	28.4	0.96
100	543.48	525	96.6	37	0.938
200	292.68	269.6	92.1	52.4	0.886
500	141	110.75	78.55	83.2	0.77
1000	90.2	56.1	62.2	111.7	0.667

Power factor has been calculated by using equation in [7], P.F = $\frac{1}{\sqrt{1+(THD_I)^2}}$

$$I_t = \sqrt{I_1^2 + I_h^2}$$

The total input power, has been calculated via below equation [8] :

$$P_{in} = V_t.I_t.PF$$

The maximum efficiency is 98.68% when input power is 2.5 kw when R-load = 20 Ω and (L) is 20 µH.

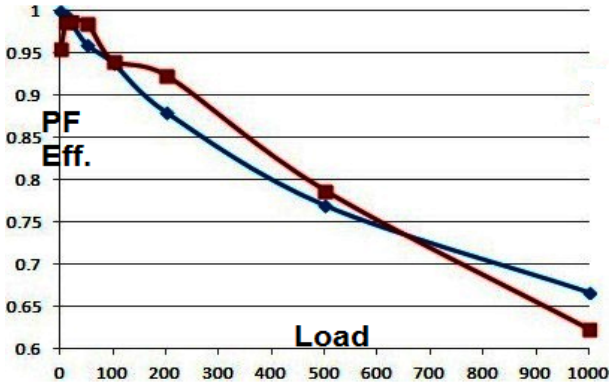


Fig. 5: Different load values with PF and η

It can be concluded, from table (I) and Fig. (5) that the values of (η) and input PF, inversely proportion with the increasing of the load value.

4) Table (II) shows the relationship between different inductor values comparing with with P_{in}, P_{out}, η and input PF, when R-load = 20 Ω and f_{sw} = 20 Khz.

TABLE II: Different (L) values with THD_I, PF & η

L(uH)	P_{in}(W)	P_{out} (W)	η(%)	**THD**(%)	**PF**
1	2854.9	2679.4	93.86	55	0.876
10	2557.5	2510	98.1	24	0.972
20	2506	2473	98.68	17	0.986
50	2456	2434	99.1	10.5	0.994
100	2434.38	2415.5	99.2	7.2	0.997
200	2420.48	2403.7	99.3	4.9	0.999
500	2412	2395	99.3	3.5	0.999
1000	2407.3	2391.8	99.36	2.5	0.999

It can be concluded, from table (II) and Fig. (6) below, that the value of η and PF, directly proportion with the increasing of inductor value.

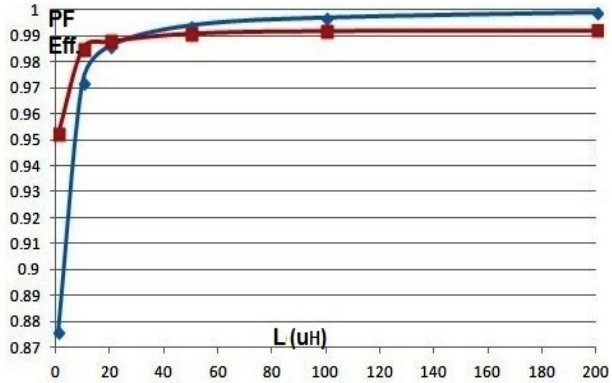


Fig. 6: Different (L) values with PF and η

5) Table (III) shows the relationship between different switching frequencies of MOSFET comparing with P_{in}, P_{out}, η and input PF when R-load = 20 Ω and (L) is 20 µH.

TABLE III: Variable (D) for (SW) with THD_I, PF & η

f_{sw}(K)	P_{in}(W)	P_{out} (W)	η(%)	**THD**(%)	**PF**
5	2641	2574.8	97.5	33	0.95
10	2561	2515	98.2	23.8	0.973
20	2506	2473	98.68	17	0.986
50	2456.3	2434.2	99.1	10.6	0.994
100	2437.3	2415.8	99.1	7.6	0.997
200	2418.9	2405	99.4	5.6	0.998
500	2415	2397.2	99.2	3.9	0.999
1000	2414.8	2396.2	99.2	3.7	0.999

It can be concluded from table (III) and Fig. (7) that, the value of η and PF directly proportion with the value of f_{sw}.

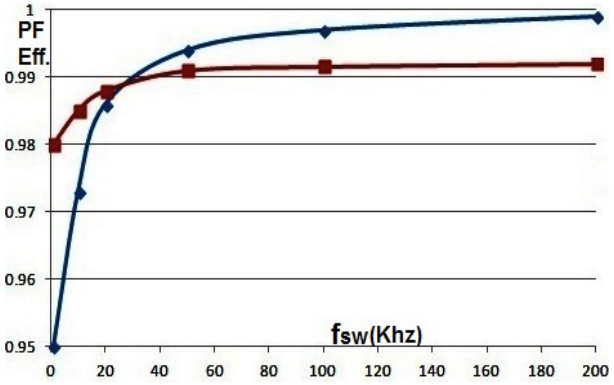


Fig. 7: Different f_{sw} values with PF and η

It can be concluded that, f_{sw} can be kept around (10 - 20) KHz in order to get approximately unity PF (0.98) at the input AC side when (L) is 20 µH for 2.5 kw output power.

6) The input source current waveform (I_S) is shown below in Fig.(8) with nine time modes:

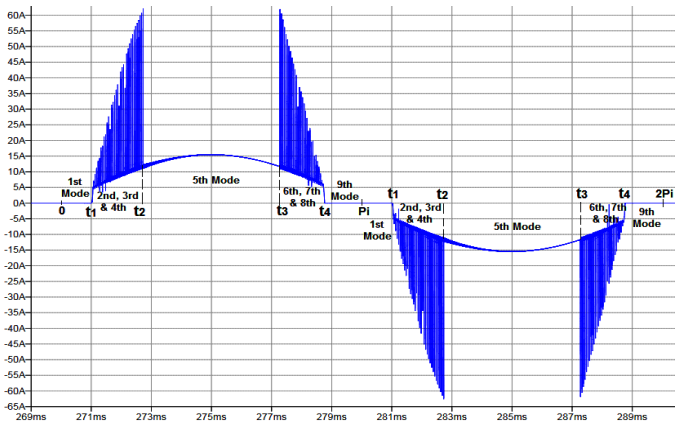


Fig. 8: The input source current

Fig. (9), shows the FFT spectrum of the input source current. The total current harmonic distortion (THD_I) is 17%, then the input power factor is almost unity (0.986).

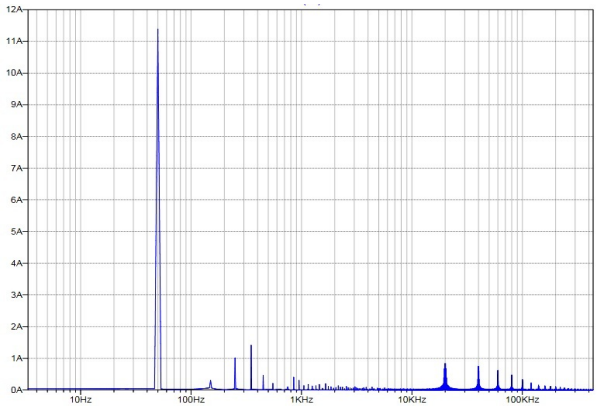


Fig. 9: FFT Spectrum of the input current

As it is shown in Fig. (9), the third order harmonic is not exist at the input current waveform, and the only harmonic orders shown are the 5th and 7th order harmonics. This is because (C) was OFF at the middle of the waveform ($t_2 - t_3$) and the load was fed by the source.

7) In the case of the absence of freewheeling diode in the time intervals $t_1 \leq t < t_2$ and $t_3 \leq t < t_4$ (which represent the 2nd and 6th modes), the equation of inductor's voltage is:

$$V_L = L\frac{di_L}{dt} = \frac{L.di_L.f_{sw}}{D}$$

(D) is the duty cycle of (SW) and because of the switching frequency (f_{sw}) is (20 KHz), therefore V_L would be a very large value at this moment. Consequently, V_L may be a reason for huge spikes on MOSFET's terminals and may burn the switch.

8) Generally, in this situation a snubber circuit would be proposed as a solution to suppress the high frequency spikes and to protect the MOSFET switch. However in this circuit, the main capacitor (C) would be act as a snubber circuit because of the existence of the freewheeling diode (FWD), which makes V_C charges on the negative value of V_L and prevent high voltage on the terminals of the MOSFET when its in open the status.

9) The required value of the inductance for the same voltage and power ratings in three level boost converter is (L), while the size would be doubled with the using of two inductors (2x2L) for the interleaved boost converter, on the other hand, the inductance would be doubled again (4L) for the conventional boost converter [9].
The inductor's value used in the literature in [10] for a (3 kw) output power using interleaved boost converter was (270 µH), while the value of inductor (L) in the new proposed circuit is (20 µH) for the same power ratings. This reduction of the inductor's value will effectively contribute in reducing the size, weight and the cost of

the converter.

10) One of the significant features of this design, is that the inductor's current is not related to the value of source voltage (except in the 2nd and 6th mode) as usually happens in PFC circuits. This advantage can be utilized in order to reduce the value of (L) into few microhenrys and avoid high V_L values. Consequently, can reduce the size, weight and the cost effectively.

11) Practically, the internal capacitor of the used diodes in the circuit would combine with the stray inductors and compose a parasitic resonant frequency (f_p). In order to get rid of the bad effects of (f_p), the rising time (t_r) or the falling time (t_f) can be changed, or alternatively a damper circuit can be added to the circuit or using clamping diodes and that's require additional components and complex design [11].

12) The inductor works like a proper choke or current limiter due to the high negative value of inductor voltage (V_L) as its in counter direction of capacitor voltage (V_C).
(L) charges in the time period $t_1 \leq t < t_2$ because $V_S > V_C$. On the other hand, for the time period$t_2 \leq t < t_3$, I_L is zero because L and C are reverse biased. While, for the time period $t_3 \leq t < t_4$, (L) discharges as a positive current because $V_S > V_C$.
However, for time period $t_4 \leq t < t_1$ of the next period, L discharges as a negative current because $V_C > V_S$ and the R-load would be fed by I_L which is the same capacitor's current ($I_C = I_L$).

IV. Conclusion

According to the simulation's results, the new proposed PFC circuit was able to reduce the THD_I to 17% with a unity power factor (0.986) at the input side and increases the efficiency to 98.68%.

The topology of reducing the conduction time of the main capacitor via dividing the waveform into three regions ON-OFF-ON, can improve the efficiency, the input PF and reduce the THD_I at the input side.

In addition, preventing the capacitor (C) from work in the middle of the time period for about half of the time will eliminate the third order harmonic and shift the harmonics current to the high frequency region and that's will contribute in reducing the size of magnetics due to the small value of the inductor 20 µH which produces a small amount of losses. Accordingly, the small inductor will effectively reduce the size and weight as used just one MOSFET, so the rectifier is not bulky any more, and thats reduces the cost of the converter.

Another advantage of this circuit is that the snubber circuit is not compulsory because of the presence of freewheeling diode. In addition, the design is considered as a high efficient design due to minimum number and small values of components and simple circuit design due to uses single switch.

The performance of this circuit has a wide range of flexibility because, the output ripple voltage, the input PF and THD_I can be improved via controlling the values of duty cycles of (SW), (L) and (C).

From graphical waveforms and tables of results analysis for different values of R-load, inductor (L), and switching frequency, can be concluded that the increasing of inductor value (L) and R-load values is required in order to get a constant unity power factor, small THD_I and high efficiency.

References

[1] H. Al-bayaty, M. Ambroze, and M. Z. Ahmed, "Utilization of harmonics current in single phase system," in *2016 17th International Conference on Harmonics and Quality of Power (ICHQP)*, Oct 2016, pp. 443–447.

[2] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of single-phase improved power quality ac-dc converters," *IEEE Transactions on Industrial Electronics*, vol. 50, no. 5, pp. 962–981, 2003.

[3] H. Azazi, E. El-Kholy, S. Mahmoud, and S. Shokralla, "Review of passive and active circuits for power factor correction in single phase, low power ac-dc converters," in *Proceedings of the 14th International Middle East Power Systems Conference (MEPCON'10)*, 2010, pp. 217–224.

[4] H. Al-bayaty, M. Ambroze, and M. Z. Ahmed, "Feeding loads via harmonics utilization in ac circuit systems," in *2016 International Conference for Students on Applied Engineering (ICSAE)*, Oct 2016, pp. 224–227.

[5] S. Basu, *Single Phase Active Power Factor Correction Converters-Methods for Optimizing EMI, Performance and Costs*. Chalmers University of Technology, 2006.

[6] J. P. M. Figueiredo, F. L. Tofoli, and B. L. A. Silva, "A review of single-phase pfc topologies based on the boost converter," in *Industry Applications (INDUSCON), 2010 9th IEEE/IAS International Conference on*, Nov 2010, pp. 1–6.

[7] H. Al-bayaty, M. Ambroze, and M. Z. Ahmed, "New effective power terms and right-angled triangle (rat) power theory," *International Journal of Electrical Power & Energy Systems*, vol. 88, pp. 133–140, 2017.

[8] H. A. bayaty et al., "A new power theory (right-angled triangle theory)," in *2015 IEEE Conference on Energy Conversion (CENCON)*, Oct 2015, pp. 451–456.

[9] M. T. Zhang, Y. Jiang, F. C. Lee, and M. M. Jovanovic, "Single-phase three-level boost power factor correction converter," in *Applied Power Electronics Conference and Exposition, 1995. APEC '95. Conference Proceedings 1995., Tenth Annual*, no. 0, Mar 1995, pp. 434–439 vol.1.

[10] B. AKIN, "Comparison of conventional and interleaved pfc boost converters for fast and efficient charge of li-ion batteries used in electrical cars," in *International Conference on Power and Energy Systems*, vol. 13, 2012.

[11] K. Harada and T. Ninomiya, "Optimum design of rc snubbers for switching regulators," *IEEE Transactions on Aerospace and Electronic Systems*, no. 2, pp. 209–218, 1979.

Appendix C

Mathematical Analysis of Harmonics Source Current For APFC

Fourier analysis is the process of converting time domain waveforms into their frequency components. The input source current $I_S(t)$ is a periodic waveform; therefore, the Fourier series has considered as the optimum way to analyze and find the frequency spectrum of this waveform in order to calculate the harmonics amount and find out which harmonics are the important ones, then the filter can be designed for that specific harmonic. Consequently, the optimum power factor and RLC component values can be obtained for the proposed circuit.

The Fourier series of a periodic function x(t) has the expression:

$$F(t) = a_0 + \sum_{n=1}^{m} (a_n \cos(n\omega t) + b_n \sin(n\omega t)) \tag{C.1}$$

where, $F(t)$ is the Fourier series function of $I_S(t)$ and $(\omega = 2\pi f)$.

a_0, a_n and b_n are amplitude coefficients of Fourier series and they are given by the

following equations:

$$a_0 = \frac{1}{T}\int_0^T I_S(t)dt \tag{C.2}$$

$$a_n = \frac{2}{T}\int_0^T I_S(t)\cos(n\omega t)dt \tag{C.3}$$

$$b_n = \frac{2}{T}\int_0^T I_S(t)\sin(n\omega t)dt \tag{C.4}$$

The representation of the frequency components as rotating vectors in the complex plane gives a geometrical interpretation of the relationship between waveforms in the time and frequency domains. The complex form of the Fourier series is:

$$C_n = a_n + j.b_n \tag{C.5}$$

$$\therefore f(t) = \sum_0^\infty C_n e^{jn\omega t} \tag{C.6}$$

$$\therefore C_n = \frac{2}{T}\int_0^T f(t)e^{-jn\omega t}dt \tag{C.7}$$

The circuit schematic of the newly proposed PFC circuit is shown in figure C.1, and was explained in details in chapter (3).

In this case, f(t) is the source current which is shown below in figure C.2:

The input source current $I_S(t)$ is divided into nine intervals and the piecewise equation is equal to the following succession segments over the full period from 0 $\rightarrow$ T interval. (T = 0.02 sec.)

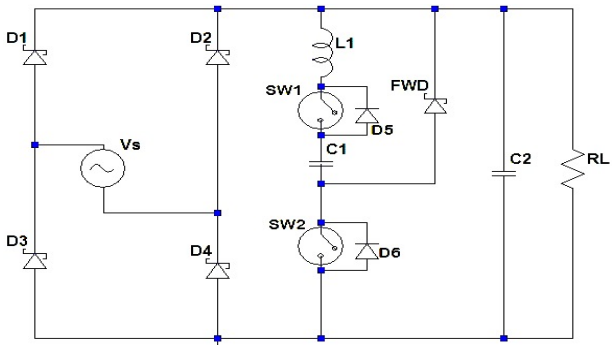


Figure C.1: New proposed PFC circuit

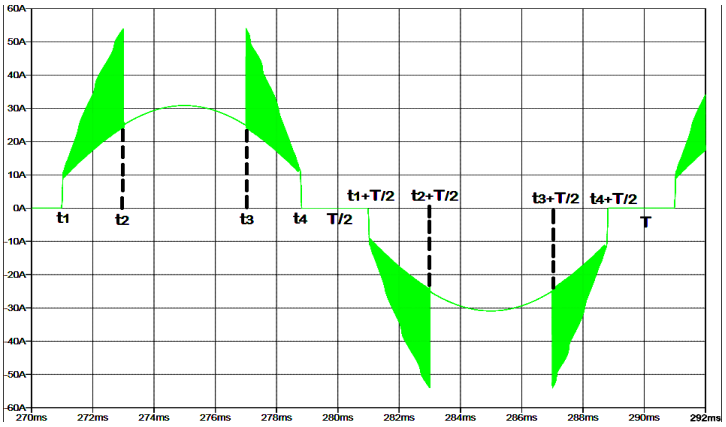


Figure C.2: Full cycle of source current

$$I_S = \begin{cases} \text{Zero} & 0 < t \leq t_1 \\ \frac{V_S}{R}.\sin(\omega t) + I_{C1}.\frac{(t-t_1)}{(t_2-t_1)} & t_1 < t \leq t_2 \\ \frac{V_S}{R}.\sin(\omega t) & t_2 < t \leq t_3 \\ \frac{V_S}{R}.\sin(\omega t) + I_{C1} - I_{C1}.\frac{(t-t_3)}{(t_4-t_3)} & t_3 < t \leq t_4 \\ \text{Zero} & t_4 < t \leq t_1 + \frac{T}{2} \\ \frac{V_S}{R}.\sin(\omega t) - I_{C1}.\frac{t-(t_1+\frac{T}{2})}{(t_2-t_1)} & t_1 + \frac{T}{2} < t \leq t_2 + \frac{T}{2} \\ \frac{V_S}{R}.\sin(\omega t) & t_2 + \frac{T}{2} < t \leq t_3 + \frac{T}{2} \\ \frac{V_S}{R}.\sin(\omega t) - (I_{C1} - I_{C1}.\frac{t-(t_3+\frac{T}{2})}{(t_4-t_3)}) & t_3 + \frac{T}{2} < t \leq t_4 + \frac{T}{2} \\ \text{Zero} & t_4 + \frac{T}{2} < t \leq \text{T} \end{cases}$$

The linear equation of (I_{C1}) in the second interval can be calculated by using the line equation: y = mx + b.

where: y = I_L, x = t, (m) is the tangent of the line = $\frac{y}{x} = \frac{di_{c1}}{dt} = \frac{I_{C1}}{t_2 - t_1}$.

and b = Zero (DC shift)

$\therefore I_{C1}(t) = I_{C1}\frac{t}{t_2 - t_1}$.

$$\because a_0 = \frac{1}{T}\int_0^T I_S(t)dt \tag{C.8}$$

$$\begin{aligned} a_0 = \frac{1}{T}\Big[&\int_0^{t_1} I_S(t) + \int_{t_1}^{t_2} I_S(t) + \int_{t_2}^{t_3} I_S(t) + \int_{t_3}^{t_4} I_S(t) + \int_{t_4}^{t_1+\frac{T}{2}} I_S(t) \\ &+ \int_{t_1+\frac{T}{2}}^{t_2+\frac{T}{2}} I_S(t) + \int_{t_2+\frac{T}{2}}^{t_3+\frac{T}{2}} I_S(t) + \int_{t_3+\frac{T}{2}}^{t_4+\frac{T}{2}} I_S(t) + \int_{t_4+\frac{T}{2}}^{T} I_S(t)\Big]dt \end{aligned}$$

$$\begin{aligned} \therefore a_0 = \frac{1}{T}\Bigg[&\int_0^{t_1} Zero + \int_{t_1}^{t_2} \Big[\frac{V_S}{R}.\sin(\omega t) + I_{C1}.\frac{(t-t_1)}{(t_2-t_1)}\Big]dt + \int_{t_2}^{t_3} \frac{V_S}{R}.\sin(\omega t)dt \\ &+ \int_{t_3}^{t_4} \Big[\frac{V_S}{R}.\sin(\omega t) + I_{C1}.\frac{(t_4-t)}{(t_4-t_3)}\Big]dt + \int_{t_4}^{t_1+\frac{T}{2}} Zero + \int_{t_1+\frac{T}{2}}^{t_2+\frac{T}{2}} \Big[\frac{V_S}{R}.\sin(\omega t) \\ &- I_{C1}\frac{(t-t_1-\frac{T}{2})}{(t_2-t_1)}\Big]dt + \int_{t_2+\frac{T}{2}}^{t_3+\frac{T}{2}} \frac{V_S}{R}.\sin(\omega t)dt + \int_{t_3+\frac{T}{2}}^{t_4+\frac{T}{2}} \Big[\frac{V_S}{R}.\sin(\omega t) \\ &- I_{C1}.\frac{(t_4+\frac{T}{2}-t)}{(t_4-t_3)}\Big]dt + \int_{t_4+\frac{T}{2}}^{T} Zero\Bigg] = Zero \end{aligned} \tag{C.9}$$

(a_0) equal to zero, because it is the mean value of the function (electrically is the DC component). Mathematically, is the average value of the area under the curve of the input current, and as the two periods of operational modes are symmetrical

above (for +ve cycle) and below (for -ve cycle) the horizontal axis of time domain over the periodic interval of T, then the value of a_0 equals to zero.

$$C_n = \frac{2}{T}\int_0^T I_S(t).e^{-jn\omega t}dt = \frac{2}{T}\Bigg[\int_{t_1}^{t_2}\Big[\frac{V_S}{R}.\sin(\omega t) + I_{C1}.\frac{(t-t_1)}{(t_2-t_1)}\Big].e^{-jn\omega t}dt$$
$$+\int_{t_2}^{t_3}\frac{V_S}{R}.\sin(\omega t).e^{-jn\omega t}dt + \int_{t_3}^{t_4}\Big[\frac{V_S}{R}.\sin(\omega t) + I_{C1}.\frac{(t_4-t)}{(t_4-t_3)}\Big].e^{-jn\omega t}dt$$
$$+\int_{t_1+\frac{T}{2}}^{t_2+\frac{T}{2}}\Big[\frac{V_S}{R}.\sin(\omega t) - I_{C1}\frac{(t-t_1-\frac{T}{2})}{(t_2-t_1)}\Big].e^{-jn\omega t}dt + \int_{t_2+\frac{T}{2}}^{t_3+\frac{T}{2}}\frac{V_S}{R}.\sin(\omega t).e^{-jn\omega t}dt$$
$$+\int_{t_3+\frac{T}{2}}^{t_4+\frac{T}{2}}\Big[\frac{V_S}{R}.\sin(\omega t) - I_{C1}.\frac{(t_4+\frac{T}{2}-t)}{(t_4-t_3)}\Big].e^{-jn\omega t}dt\Bigg]$$

$$C_n = \frac{2}{T}\Bigg[\frac{V_S}{R}\Big[\int_{t_1}^{t_4}\sin(\omega t).e^{-jn\omega t}dt + \int_{t_1+\frac{T}{2}}^{t_4+\frac{T}{2}}\sin(\omega t).e^{-jn\omega t}dt\Big]$$
$$+ I_{C1}.\Big[\int_{t_1}^{t_2}\frac{(t-t_1)}{(t_2-t_1)}.e^{-jn\omega t}dt - \int_{t_1+\frac{T}{2}}^{t_2+\frac{T}{2}}\frac{(t-t_1-\frac{T}{2})}{(t_2-t_1)}.e^{-jn\omega t}dt$$
$$+\int_{t_3}^{t_4}\frac{(t_4-t)}{(t_4-t_3)}.e^{-jn\omega t}dt - \int_{t_3+\frac{T}{2}}^{t_4+\frac{T}{2}}\frac{(t_4+\frac{T}{2}-t)}{(t_4-t_3)}.e^{-jn\omega t}\Big]dt\Bigg]$$

In order to simplify the solution of the equation of C_n, each integral function would be represented by a different letters, and then each integral would be solved separately.

$$\therefore C_n = \frac{2}{T}\Bigg[\frac{V_S}{R}\big[A_1 + B_1\big] + I_{C1}\big[A_2 - B_2 + A_3 - B_3\big]\Bigg] \tag{C.10}$$

$$A_1 = \int_{t_1}^{t_4}\sin(\omega t).e^{-jn\omega t}dt$$

$$A_1 = e^{-jn\omega t}.\frac{\cos(\omega t) + jn\sin(\omega t)}{(n-1)(n+1)\omega}\Bigg|_{t_1}^{t_4}$$

$$A_1 = \frac{1}{(n^2-1)\omega}\left[e^{-jn\omega t_4}.(\cos(\omega t_4) + jn\sin(\omega t_4)) - e^{-jn\omega t_1}.(\cos(\omega t_1) + jn\sin(\omega t_1))\right] \tag{C.11}$$

However, when n=1, the result of A_1 is infinity. Therefore, (n) could be substituted by (1) before the integration process happened, as A_1 is A_{1n} when (n=1):

$$A_{1n} = \int_{t_1}^{t_4} \sin(\omega t).e^{-j\omega t}dt$$

$$A_{1n} = \frac{-jt}{2} - \frac{e^{-2j\omega t}}{4\omega}\Bigg|_{t_1}^{t_4}$$

$$A_{1n} = \frac{-jt_4}{2} - \frac{e^{-2j\omega t_4}}{4\omega} + \frac{jt_1}{2} + \frac{e^{-2j\omega t_1}}{4\omega}$$

$$A_{1n} = \frac{j}{2}(t_1 - t_4) + \frac{1}{4\omega}(e^{-2j\omega t_1} - e^{-2j\omega t_4}) \tag{C.12}$$

$$B_1 = \int_{t_1+\frac{T}{2}}^{t_4+\frac{T}{2}} \sin(\omega t).e^{-jn\omega t}dt$$

$(B_1)\&(B_{1n})$ can be calculated in the same way:

$$B_1 = \frac{1}{(n^2-1)\omega}\big[e^{-jn\omega(t_4+\frac{T}{2})}.(\cos(\omega(t_4+\frac{T}{2})) + jn\sin(\omega(t_4+\frac{T}{2})))$$
$$- e^{-jn\omega(t_1+\frac{T}{2})}.(\cos(\omega(t_1+\frac{T}{2})) + jn\sin(\omega(t_1+\frac{T}{2})))\big] \tag{C.13}$$

$$B_{1n} = \frac{j}{2}(t_1 - t_4) - \frac{1}{4\omega}(e^{-2j\omega(t_1+\frac{T}{2})} - e^{-2j\omega(t_4+\frac{T}{2})}) \tag{C.14}$$

$$A_2 = \int_{t_1}^{t_2} \frac{(t-t_1)}{(t_2-t_1)}.e^{-jn\omega t}dt$$

$$A_2 = \frac{1}{(t_2-t_1)}\int_{t_1}^{t_2}\Big[t.e^{-jn\omega t} - t_1.e^{-jn\omega t}\Big]dt$$

$$A_2 = \frac{1}{(t_2-t_1)}\Big[\frac{e^{-jn\omega t}(1+jn\omega t)}{n^2.\omega^2} - \frac{e^{-jn\omega t}.jt_1}{n.\omega}\Big]\Bigg|_{t_1}^{t_2}$$

$$A_2 = \Big[\frac{e^{-jn\omega t} + jn\omega t.e^{-jn\omega t} - jn\omega t_1.e^{-jn\omega t}}{(t_2 - t_1)n^2.\omega^2}\Big]\Big|_{t_1}^{t_2}$$

$$A_2 = \Big[\frac{e^{-jn\omega t}}{(t_2 - t_1)n^2.\omega^2}(1 - jn\omega t_1 + jn\omega t)\Big]\Big|_{t_1}^{t_2}$$

$$A_2 = \frac{e^{-jn\omega t_2}}{(t_2 - t_1)n^2.\omega^2}(1 - jn\omega t_1 + jn\omega t_2) - \frac{e^{-jn\omega t_1}}{(t_2 - t_1)n^2.\omega^2}(1 - jn\omega t_1 + jn\omega t_1)$$

$$A_2 = \frac{1}{(t_2 - t_1)n^2.\omega^2}\Big[e^{-jn\omega t_2}(1 - jn\omega t_1 + jn\omega t_2) - e^{-jn\omega t_1}\Big] \tag{C.15}$$

$$A_{2n} = \frac{1}{(t_2 - t_1).\omega^2}\Big[e^{-j\omega t_2}(1 - j\omega t_1 + j\omega t_2) - e^{-j\omega t_1}\Big] \tag{C.16}$$

$$B_2 = \int_{t_1+\frac{T}{2}}^{t_2+\frac{T}{2}} \frac{(t - t_1 - \frac{T}{2})}{(t_2 - t_1)}.e^{-jn\omega t}dt$$

$$B_2 = \frac{1}{(t_2 - t_1)}\Big[\frac{e^{-jn\omega t}(1 + jn\omega t)}{n^2.\omega^2} - \frac{e^{-jn\omega t}.j(t_1 + \frac{T}{2})}{n.\omega}\Big]\Big|_{t_1+\frac{T}{2}}^{t_2+\frac{T}{2}}$$

$$B_2 = \Big[\frac{e^{-jn\omega t} + jn\omega t.e^{-jn\omega t} - jn\omega(t_1 + \frac{T}{2}).e^{-jn\omega t}}{(t_2 - t_1)n^2.\omega^2}\Big]\Big|_{t_1+\frac{T}{2}}^{t_2+\frac{T}{2}}$$

$$B_2 = \Big[\frac{e^{-jn\omega t}}{(t_2 - t_1)n^2.\omega^2}(1 - jn\omega(t_1 + \frac{T}{2}) + jn\omega t)\Big]\Big|_{t_1+\frac{T}{2}}^{t_2+\frac{T}{2}}$$

$$\begin{aligned} B_2 = &\frac{e^{-jn\omega(t_2+\frac{T}{2})}}{(t_2 - t_1)n^2.\omega^2}(1 - jn\omega(t_1 + \frac{T}{2}) + jn\omega(t_2 + \frac{T}{2})) \\ &- \frac{e^{-jn\omega(t_1+\frac{T}{2})}}{(t_2 - t_1)n^2.\omega^2}(1 - jn\omega(t_1 + \frac{T}{2}) + jn\omega(t_1 + \frac{T}{2})) \end{aligned}$$

$$B_2 = \frac{1}{(t_2 - t_1)n^2.\omega^2}\Big[e^{-jn\omega(t_2+\frac{T}{2})}(1 - jn\omega(t_1 + \frac{T}{2}) + jn\omega(t_2 + \frac{T}{2})) - e^{-jn\omega(t_1+\frac{T}{2})}\Big] \tag{C.17}$$

$$B_{2n} = \frac{1}{(t_2 - t_1).\omega^2}\Big[e^{-j\omega(t_2+\frac{T}{2})}(1 - j\omega(t_1 + \frac{T}{2}) + j\omega(t_2 + \frac{T}{2})) - e^{-j\omega(t_1+\frac{T}{2})}\Big] \tag{C.18}$$

$$A_3 = \int_{t_3}^{t_4} \frac{(t_4 - t)}{(t_4 - t_3)}.e^{-jn\omega t}dt$$

$$A_3 = \frac{1}{(t_4 - t_3)} \int_{t_3}^{t_4} \Big[t_4.e^{-jn\omega t} - t.e^{-jn\omega t} \Big] dt$$

$$A_3 = \frac{1}{(t_4 - t_3)} \Big[\frac{e^{-jn\omega t}.jt_4}{n.\omega} - \frac{e^{-jn\omega t}(1 + jn\omega t)}{n^2.\omega^2} \Big] \Big|_{t_3}^{t_4}$$

$$A_3 = \Big[\frac{j.n.\omega t_4.e^{-jn\omega t} - e^{-jn\omega t} - jn\omega t.e^{-jn\omega t}}{(t_4 - t_3)n^2.\omega^2} \Big] \Big|_{t_3}^{t_4}$$

$$A_3 = \Big[\frac{e^{-jn\omega t}}{(t_4 - t_3)n^2.\omega^2} (jn\omega t_4 - jn\omega t - 1) \Big] \Big|_{t_3}^{t_4}$$

$$A_3 = \frac{e^{-jn\omega t_4}}{(t_4 - t_3)n^2.\omega^2} (jn\omega t_4 - jn\omega t_4 - 1) - \frac{e^{-jn\omega t_3}}{(t_4 - t_3)n^2.\omega^2} (jn\omega t_4 - jn\omega t_3 - 1)$$

$$A_3 = \frac{1}{(t_4 - t_3)n^2.\omega^2} \Big[e^{-jn\omega t_3}(1 - jn\omega(t_4 - t_3)) - e^{-jn\omega t_4} \Big] \tag{C.19}$$

$$A_{3n} = \frac{1}{(t_4 - t_3).\omega^2} \Big[e^{-j\omega t_3}(1 - j\omega(t_4 - t_3)) - e^{-j\omega t_4} \Big] \tag{C.20}$$

$$B_3 = \int_{t_3+\frac{T}{2}}^{t_4+\frac{T}{2}} \frac{(t_4+\frac{T}{2}-t)}{(t_4-t_3)}.e^{-jn\omega t}dt$$

$$B_3 = \frac{1}{(t_4-t_3)}\Big[\frac{e^{-jn\omega t}.j(t_4+\frac{T}{2})}{n.\omega} - \frac{e^{-jn\omega t}(1+jn\omega t)}{n^2.\omega^2}\Big]\Big|_{t_3+\frac{T}{2}}^{t_4+\frac{T}{2}}$$

$$B_3 = \Big[\frac{jn\omega(t_4+\frac{T}{2}).e^{-jn\omega t} - e^{-jn\omega t} - jn\omega t.e^{-jn\omega t}}{(t_4-t_3)n^2.\omega^2}\Big]\Big|_{t_3+\frac{T}{2}}^{t_4+\frac{T}{2}}$$

$$B_3 = \Big[\frac{e^{-jn\omega t}}{(t_4-t_3)n^2.\omega^2}(jn\omega(t_4+\frac{T}{2}) - 1 - jn\omega t)\Big]\Big|_{t_3+\frac{T}{2}}^{t_4+\frac{T}{2}}$$

$$\begin{aligned} B_3 = {} & \frac{e^{-jn\omega(t_4+\frac{T}{2})}}{(t_4-t_3)n^2.\omega^2}(jn\omega(t_4+\frac{T}{2}) - 1 - jn\omega(t_4+\frac{T}{2})) \\ & - \frac{e^{-jn\omega(t_3+\frac{T}{2})}}{(t_4-t_3)n^2.\omega^2}(jn\omega(t_3+\frac{T}{2}) - 1 - jn\omega(t_4+\frac{T}{2})) \end{aligned}$$

$$\begin{aligned} B_3 = {} & \frac{-1}{(t_4-t_3)n^2.\omega^2}\big[(e^{-jn\omega(t_4+\frac{T}{2})}) + e^{-jn\omega(t_3+\frac{T}{2})} \\ & (jn\omega(t_3+\frac{T}{2}) - 1 - jn\omega(t_4+\frac{T}{2}))\big] \end{aligned} \tag{C.21}$$

$$B_{3n} = \frac{-1}{(t_4 - t_3).\omega^2}\big[(e^{-j\omega(t_4+\frac{T}{2})}) + e^{-j\omega(t_3+\frac{T}{2})} (j\omega(t_3 + \frac{T}{2}) - 1 - j\omega(t_4 + \frac{T}{2}))\big] \tag{C.22}$$

$$\because C_{1n} = \frac{2}{T}\bigg[\frac{V_S}{R}\big[A_{1n} + B_{1n}\big] + I_{C1}\big[A_{2n} - B_{2n} + A_{3n} - B_{3n}\big]\bigg]$$

$$\begin{aligned}\therefore C_{1n} = \frac{2}{T}\bigg[&\frac{V_S}{R}\big[j(t_1 - t_4) + \frac{1}{4\omega}(e^{-2j\omega t_1} - e^{-2j\omega t_4} + e^{-2j\omega(t_1+\frac{T}{2})} - e^{-2j\omega(t_4+\frac{T}{2})})\big] \\ &+ I_{C1}\bigg[\frac{1}{(t_2 - t_1).\omega^2}\Big[e^{-j\omega t_2}(1 - j\omega t_1 + j\omega t_2) - e^{-j\omega t_1} - e^{-j\omega(t_2+\frac{T}{2})} \\ &(1 - j\omega(t_1 + \frac{T}{2}) + j\omega(t_2 + \frac{T}{2})) + e^{-j\omega(t_1+\frac{T}{2})}\Big] + \frac{1}{(t_4 - t_3).\omega^2}\big[e^{-j\omega t_3} \\ &(1 - j\omega(t_4 - t_3)) - e^{-j\omega t_4} + (e^{-j\omega(t_4+\frac{T}{2})} + e^{-j\omega(t_3+\frac{T}{2})}(j\omega(t_3 + \frac{T}{2}) \\ &- 1 - j\omega(t_4 + \frac{T}{2})))\big]\bigg]\bigg]\end{aligned} \tag{C.23}$$

$$\therefore C_n = \frac{2}{T}\Bigg[\frac{V_S}{R}\Big[\frac{1}{(n^2-1)\omega}\big[e^{-jn\omega t_4}.(\cos(\omega t_4)+jn\sin(\omega t_4)) - e^{-jn\omega t_1}.(\cos(\omega t_1) + jn\sin(\omega t_1)) + e^{-jn\omega(t_4+\frac{T}{2})}.(\cos(\omega(t_4+\frac{T}{2}))+jn\sin(\omega(t_4+\frac{T}{2}))) - e^{-jn\omega(t_1+\frac{T}{2})}.(\cos(\omega(t_1+\frac{T}{2}))+jn\sin(\omega(t_1+\frac{T}{2})))\big]\Big] + I_{C1}\Big[\frac{1}{(t_2-t_1)n^2.\omega^2}\Big[e^{-jn\omega t_2}(1-jn\omega t_1+jn\omega t_2) - e^{-jn\omega t_1} - e^{-jn\omega(t_2+\frac{T}{2})}(1-jn\omega(t_1+\frac{T}{2}) + jn\omega(t_2+\frac{T}{2})) - e^{-jn\omega(t_1+\frac{T}{2})}\Big] + \frac{1}{(t_4-t_3)n^2.\omega^2}\big[e^{-jn\omega t_3}(1-jn\omega(t_4-t_3)) - e^{-jn\omega t_4} + (e^{-jn\omega(t_4+\frac{T}{2})}) + e^{-jn\omega(t_3+\frac{T}{2})}(jn\omega(t_3+\frac{T}{2}) - 1 - jn\omega(t_4+\frac{T}{2}))\big]\Big]\Bigg] \tag{C.24}$$

The figure C.3, shows the fft spectrum analysis of source current.

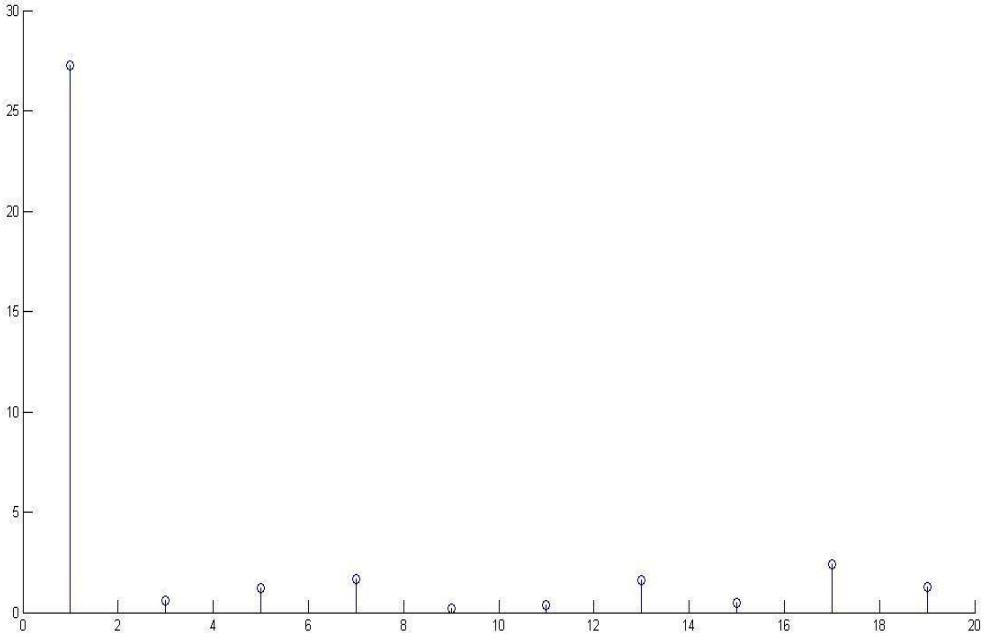


Figure C.3: Frequency spectrum Analysis of (I_S)

Appendix D

Matlab Coding of Current Source Harmonics Analysis

V = 220;

R = 20;

L = 0.00001;

C1 = 0.001;

C2 = 0.000001;

T = 0.02;

t1 = 0.001;

t2 = 0.003;

t3 = 0.007;

t4 = 0.009;

T2 = 0.000005;

td = 0.000001;

ton = 0.000002;

f = 50;

j = sqrt(-1);

Io = 0.5;

wr = 9500000;

clf

clc

for n = 1:2:19

for t = 0:0.001:0.02

$A1 = (1/(w*(n^2-1)))*(exp(-j*w*n*t4)*(\cos(w*t4)+(j*sin(w*t4)))-(exp(-j*w*n*t1)*(\cos(w*t1)+(j*n*sin(w*t1)))));$

A1n = (j*(t1-t4)/2)+((exp(-2*j*w*t1)-exp(-2*j*w*t4))/(4*w));

$B1 = (1/(w*((n)^2-1)))*(exp(-j*w*n*(t4+(T/2)))*(\cos(w*(t4+(T/2)))+(j*n*\sin(w*(t4+(T/2)))))-(exp(-j*w*n*(t1+(T/2)))*(\cos(w*(t1+(T/2)))+(j*n*\sin(w*(t1+(T/2))))))));$

B1n = (j*(t1-t4)/2)-((exp(-2*j*w*(t1+(T/2)))-exp(-2*j*w*(t4+(T/2))))/(4*w));

$A2 = (exp(-j*w*n*t2)*(1-(j*n*w*t1)+(j*n*w*t2))-exp(-j*n*w*t1))/((t2-t1)*(n)^2*(w)^2);$

$A2n = (exp(-j*w*t2)*(1-(j*w*t1)+(j*w*t2))-exp(-j*w*t1))/((t2-t1)*w^2);$

$B2 = (((exp(-j*w*n*(t2+(T/2)))*(1-(j*n*w*(t1+(T/2)))+(j*n*w*(t2+(T/2)))))-exp(-j*n*w*(t1+(T/2))))/((t2-t1)*w^2));$

$B2n = (((exp(-j*w*(t2+(T/2)))*(1-(j*w*(t1+(T/2)))+(j*w*(t2+(T/2)))))-exp(-j*w*(t1+(T/2))))/((t2-t1)*w^2));$

$A3 = ((exp(-j*w*n*t3)*(1-(j*n*w*(t4-t3)))-exp(-j*n*w*t4))/((t2-t1)*w^2));$

$A3n = ((exp(-j*w*t3)*(1-(j*w*(t4-t3)))-exp(-j*w*t4))/((t2-t1)*w^2));$

$B3 = ((exp(-j*w*n*(t4+(T/2)))) + (exp(-j*w*n*(t3+(T/2))) * ((j*n*w*(t3+(T/2))) - 1 - (j*n*w*(t4+(T/2))))))/((t3-t4)*n^2*w^2);$

$B3n = ((exp(-j*w*(t4+(T/2)))) + (exp(-j*w*(t3+(T/2))) * ((j*w*(t3+(T/2))) - 1 - (j*w*(t4+(T/2))))))/((t3-t4)*w^2);$

hold on

if n == 1;

C = abs((2/T)*((V/R)*(A1n + B1n)+((Ic)*(A2n-B2n+A3n-B3n))));

else

C = abs((2/T)*((V/R)*(A1 + B1))+((Ic)*(A2-B2+A3-B3)));

end

stem (n,C)

C

hold on

end

end

Appendix E

Data sheet of (IPP070N08N3) MOSFET

OptiMOS™3 Power-Transistor

Features

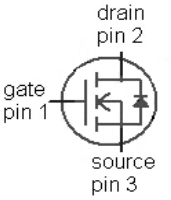
- Ideal for high frequency switching and sync. rec.
- Optimized technology for DC/DC converters
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- N-channel, normal level
- 100% avalanche tested
- Pb-free plating; RoHS compliant
- Qualified according to JEDEC[1] for target applications
- Halogen-free according to IEC61249-2-21

RoHS Halogen-Free

Product Summary

V_{DS}	80	V
$R_{DS(on),max\ (SMD)}$	6.7	mΩ
I_D	80	A

Type	IPP070N08N3 G	IPI070N08N3 G	IPB067N08N3 G
			
Package	PG-TO220-3	PG-TO262-3	PG-TO263-3
Marking	070N08N	070N08N	067N08N



Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	T_C=25 °C[2]	80	A
		T_C=100 °C	72	
Pulsed drain current[2]	$I_{D,pulse}$	T_C=25 °C	320	
Avalanche energy, single pulse[3]	E_{AS}	I_D=73 A, R_{GS}=25 Ω	150	mJ
Gate source voltage	V_{GS}		±20	V
Power dissipation	P_{tot}	T_C=25 °C	136	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

[1] J-STD20 and JESD22
[2] See figure 3 for more detailed information
[3] See figure 13 for more detailed information

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}		-	-	1.1	K/W
Thermal resistance, junction - ambient	R_{thJA}	minimal footprint	-	-	62	
		6 cm^2 cooling area[4)]	-	-	40	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	80	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=73 µA	2	2.8	3.5	
Zero gate voltage drain current	I_{DSS}	V_{DS}=80 V, V_{GS}=0 V, T_j=25 °C	-	0.1	1	µA
		V_{DS}=80 V, V_{GS}=0 V, T_j=125 °C	-	10	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	1	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10 V, I_D=73 A	-	5.8	7	mΩ
		V_{GS}=6 V, I_D=36 A	-	7.4	12.3	
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10 V, I_D=73 A, (SMD)	-	5.5	6.7	
		V_{GS}=6 V, I_D=36 A, (SMD)	-	7.1	12.0	
Gate resistance	R_G		-	1.9	-	Ω
Transconductance	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=73 A	46	91	-	S

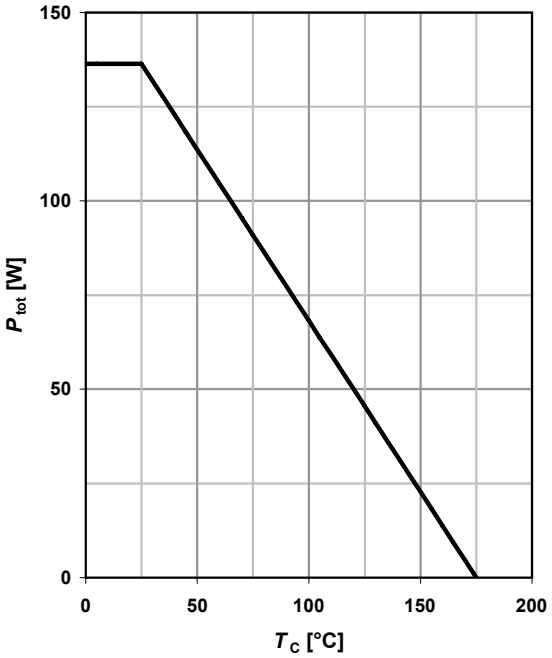
[4)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=40 V, f=1 MHz	-	2890	3840	pF
Output capacitance	C_{oss}		-	780	1040	
Reverse transfer capacitance	C_{rss}		-	30	-	
Turn-on delay time	$t_{d(on)}$	V_{DD}=40 V, V_{GS}=10 V, I_D=80 A, R_G=1.6 Ω	-	16	-	ns
Rise time	t_r		-	66	-	
Turn-off delay time	$t_{d(off)}$		-	31	-	
Fall time	t_f		-	8	-	
Gate Charge Characteristics[5)]						
Gate to source charge	Q_{gs}	V_{DD}=40 V, I_D=80 A, V_{GS}=0 to 10 V	-	15	-	nC
Gate to drain charge	Q_{gd}		-	9	-	
Switching charge	Q_{sw}		-	16	-	
Gate charge total	Q_g		-	42	56	
Gate plateau voltage	$V_{plateau}$		-	5.3	-	V
Output charge	Q_{oss}	V_{DD}=40 V, V_{GS}=0 V	-	56	75	nC
Reverse Diode						
Diode continous forward current	I_S	T_C=25 °C	-	-	80	A
Diode pulse current	$I_{S,pulse}$		-	-	320	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=73 A, T_j=25 °C	-	1.0	1.2	V
Reverse recovery time	t_{rr}	V_R=40 V, I_F=I_S, di_F/dt=100 A/µs	-	66	-	ns
Reverse recovery charge	Q_{rr}		-	135	-	nC

[5)] See figure 16 for gate charge parameter definition

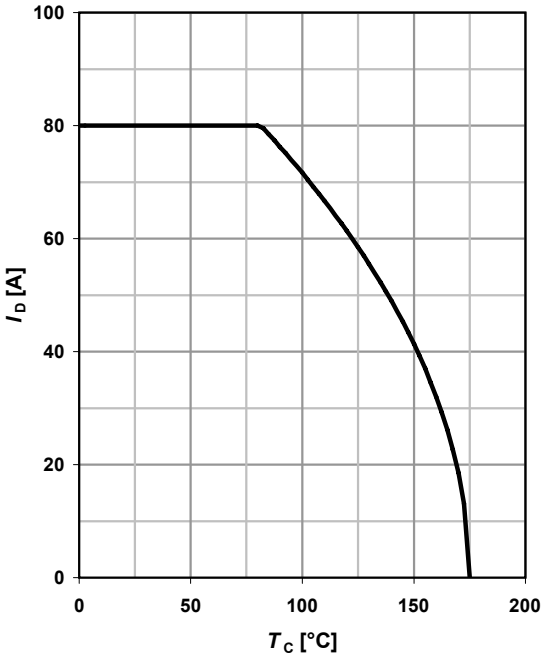
1 Power dissipation

$P_{tot}=f(T_C)$



2 Drain current

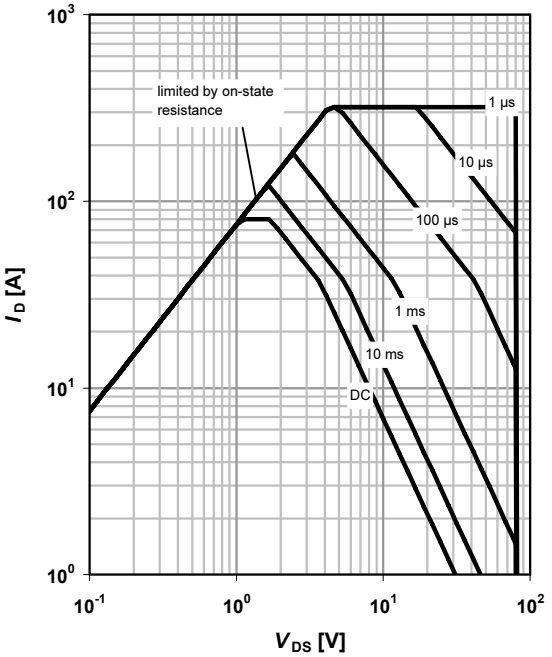
$I_D=f(T_C)$; $V_{GS}\geq 10$ V



3 Safe operating area

$I_D=f(V_{DS})$; T_C=25 °C; D=0

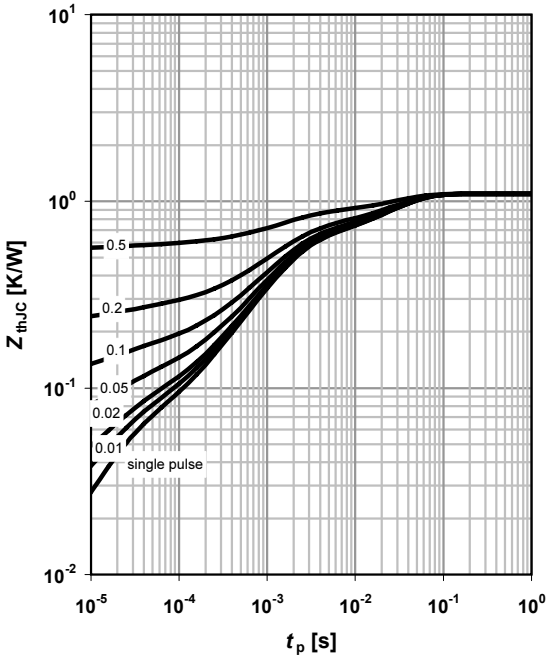
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC}=f(t_p)$

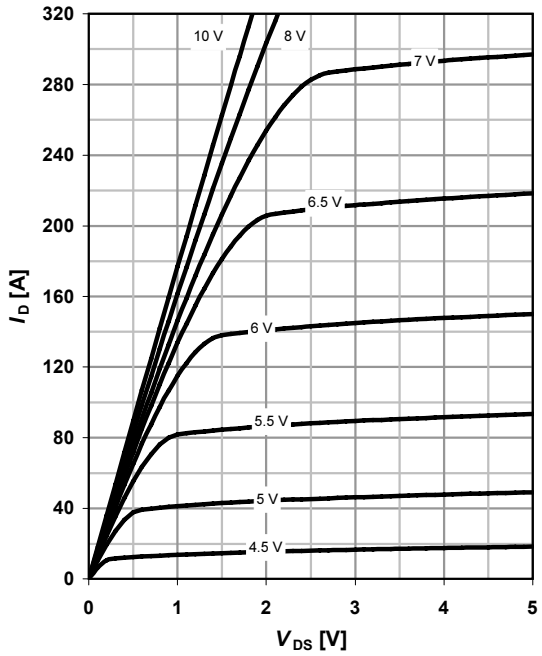
parameter: $D=t_p/T$



5 Typ. output characteristics

$I_D=f(V_{DS})$; $T_j=25$ °C

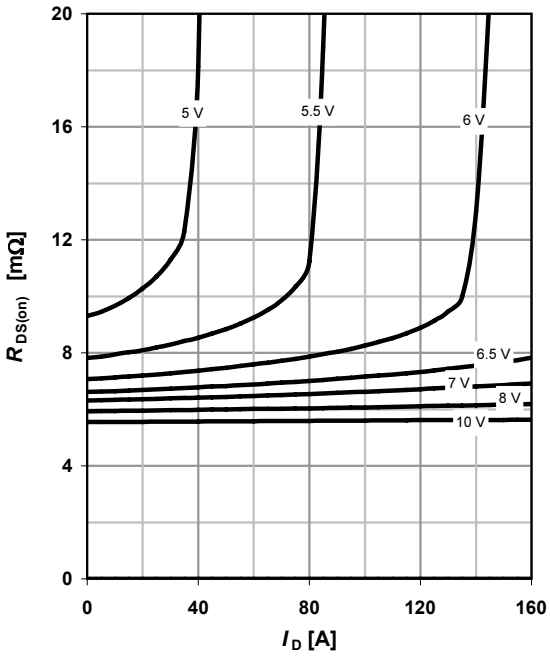
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)}=f(I_D)$; $T_j=25$ °C

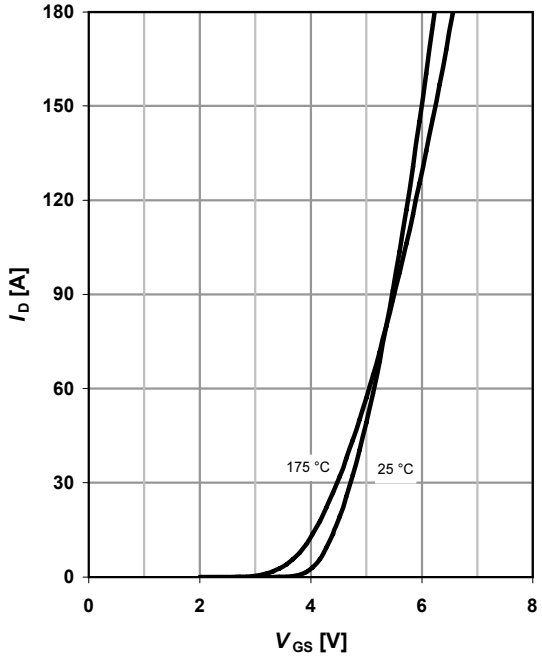
parameter: V_{GS}



7 Typ. transfer characteristics

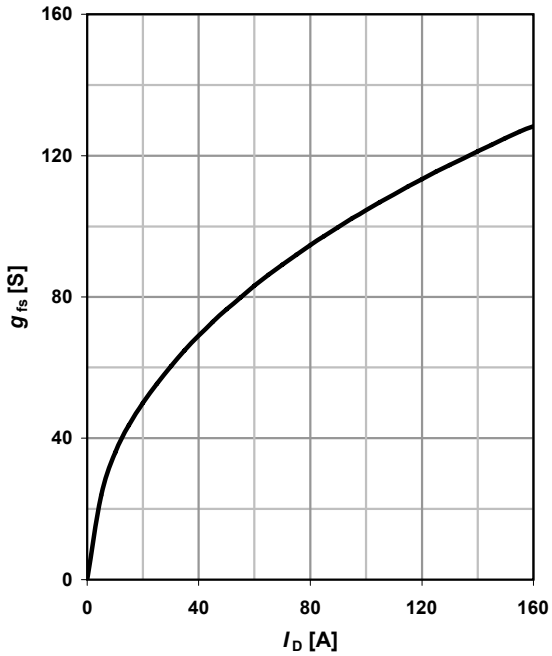
$I_D=f(V_{GS})$; $|V_{DS}|>2|I_D|R_{DS(on)max}$

parameter: T_j



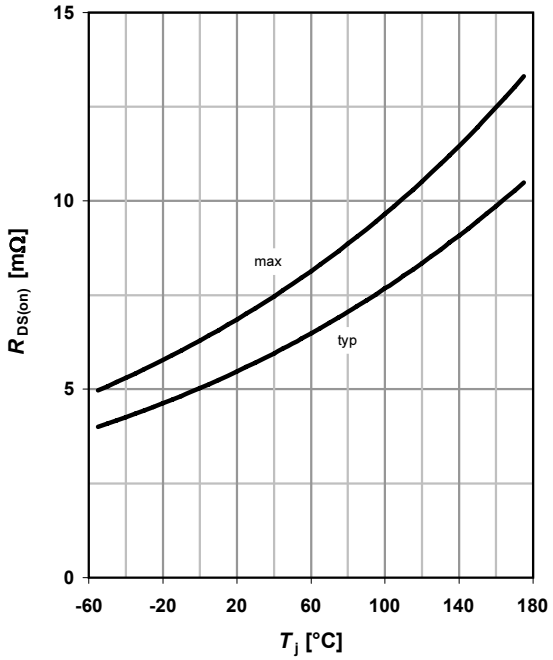
8 Typ. forward transconductance

$g_{fs}=f(I_D)$; $T_j=25$ °C



9 Drain-source on-state resistance

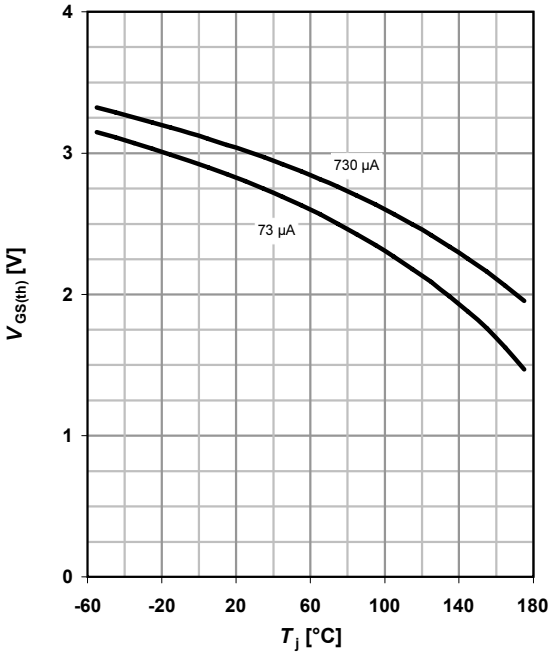
$R_{DS(on)}=f(T_j)$; $I_D=73$ A; $V_{GS}=10$ V



10 Typ. gate threshold voltage

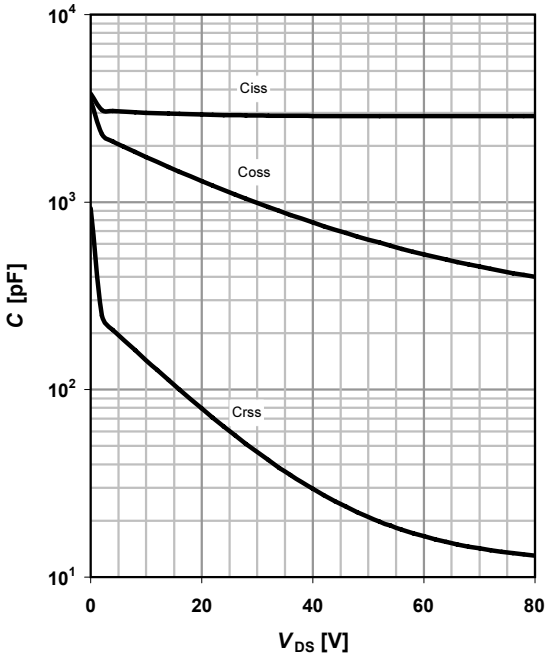
$V_{GS(th)}=f(T_j)$; $V_{GS}=V_{DS}$

parameter: I_D



11 Typ. capacitances

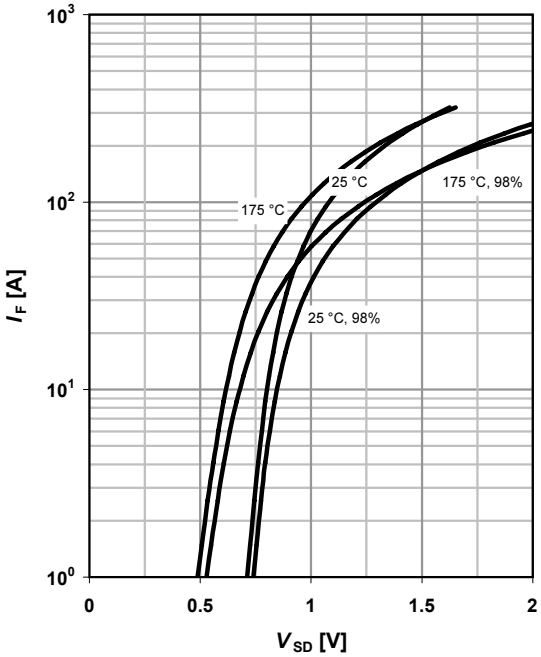
$C=f(V_{DS})$; $V_{GS}=0$ V; $f=1$ MHz



12 Forward characteristics of reverse diode

$I_F=f(V_{SD})$

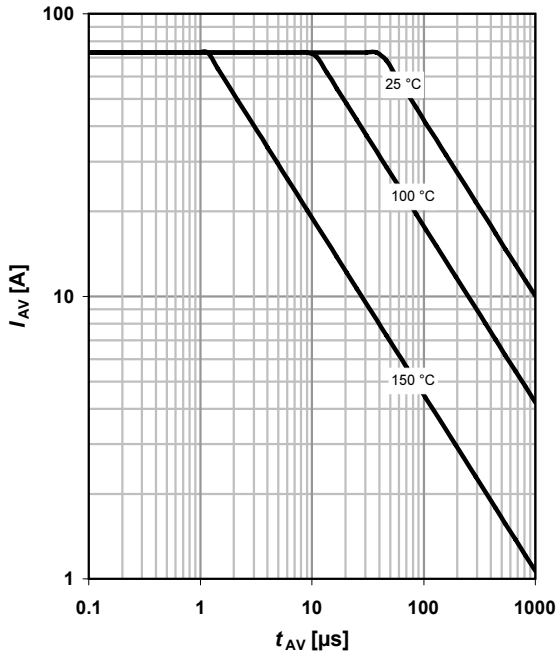
parameter: T_j



13 Avalanche characteristics

I_{AS}=f(t_{AV}); R_{GS}=25 Ω

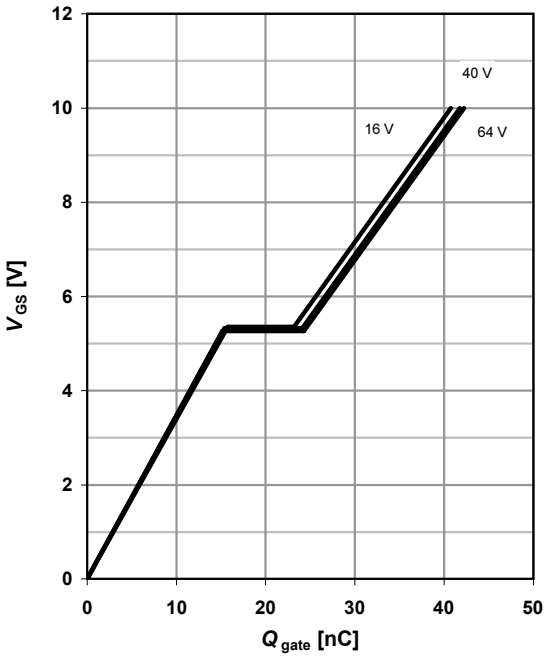
parameter: $T_{j(start)}$



14 Typ. gate charge

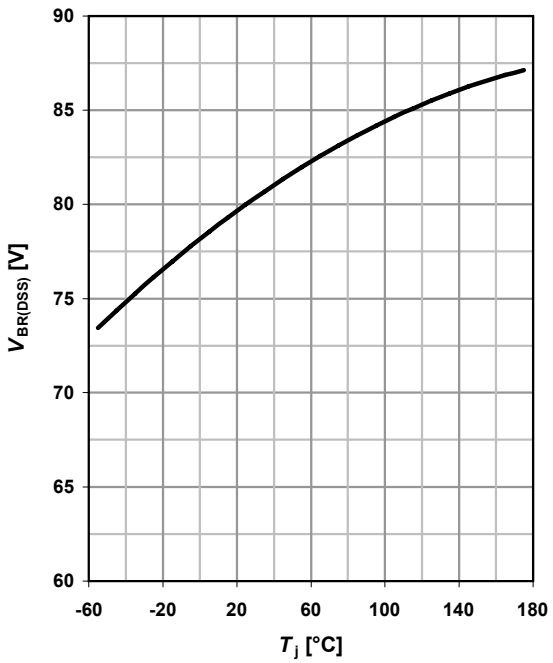
V_{GS}=f(Q_{gate}); I_D=80 A pulsed

parameter: V_{DD}

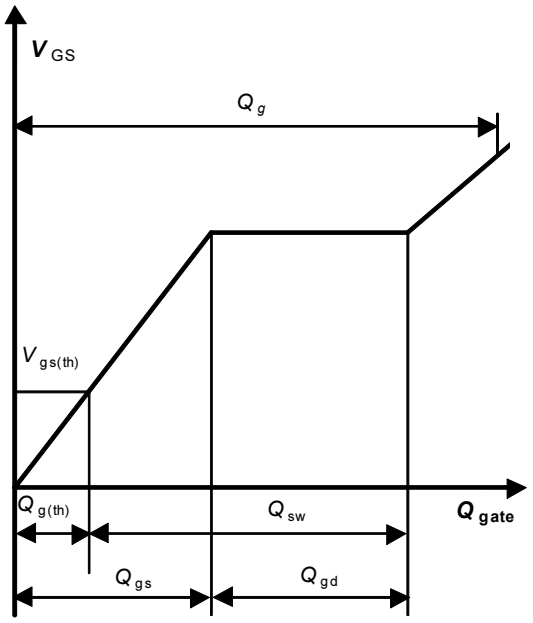


15 Drain-source breakdown voltage

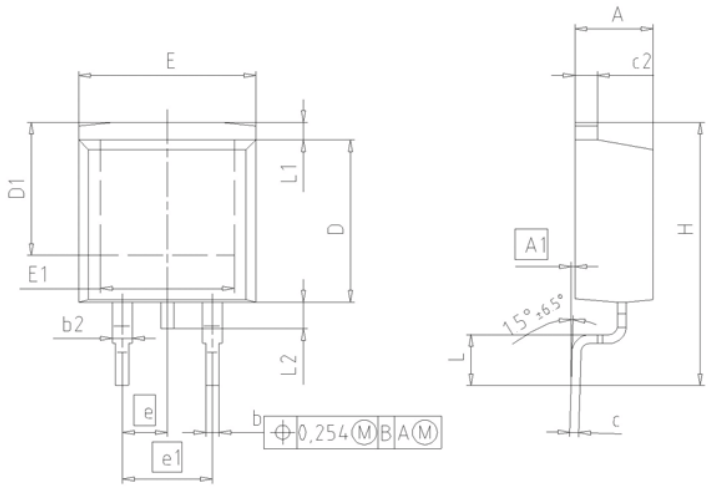
$V_{BR(DSS)}$=f(T_j); I_D=1 mA



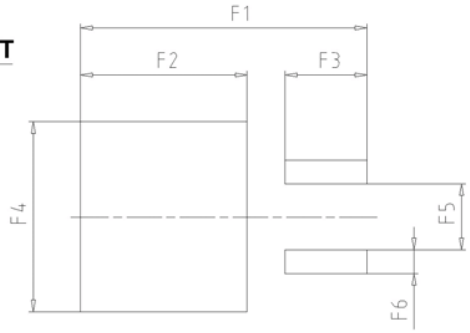
16 Gate charge waveforms



PG-TO263-3 (D²-Pak)



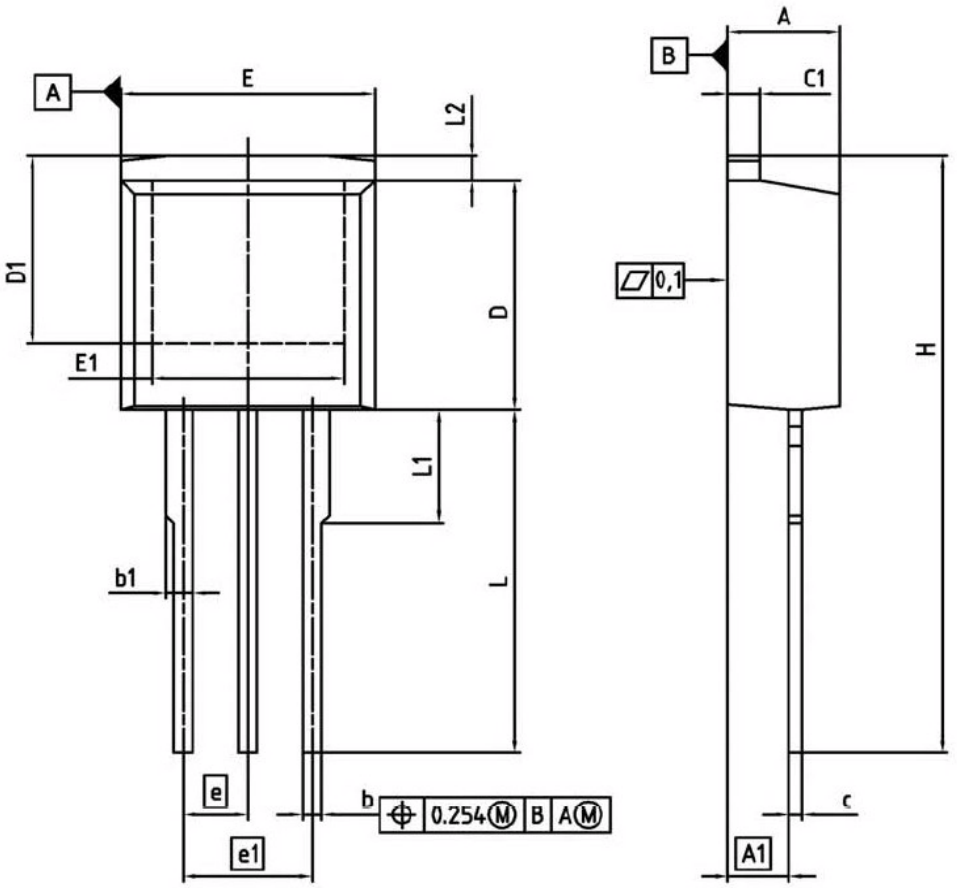
FOOTPRINT



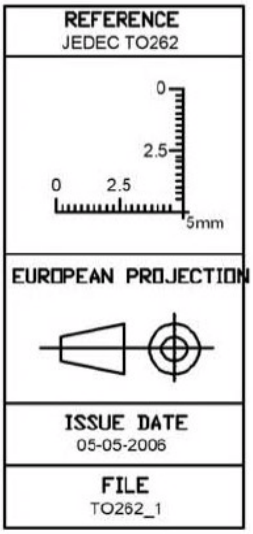
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	0.00	0.25	0.000	0.010
b	0.65	0.85	0.026	0.033
b2	0.95	1.15	0.037	0.045
c	0.33	0.65	0.013	0.026
c2	1.17	1.40	0.046	0.055
D	8.51	9.45	0.335	0.372
D1	7.10	7.90	0.280	0.311
E	9.80	10.31	0.386	0.406
E1	6.50	8.60	0.256	0.339
e	2.54		0.100	
e1	5.08		0.200	
N	2		2	
H	14.61	15.88	0.575	0.625
L	2.29	3.00	0.090	0.118
L1	0.70	1.60	0.028	0.063
L2	1.00	1.78	0.039	0.070
F1	16.05	16.25	0.632	0.640
F2	9.30	9.50	0.366	0.374
F3	4.50	4.70	0.177	0.185
F4	10.70	10.90	0.421	0.429
F5	3.65	3.85	0.144	0.152
F6	1.25	1.45	0.049	0.057

DOCUMENT NO. Z8B00003324
SCALE 0 5 5 7.5mm
EUROPEAN PROJECTION
ISSUE DATE 30-08-2007
REVISION 01

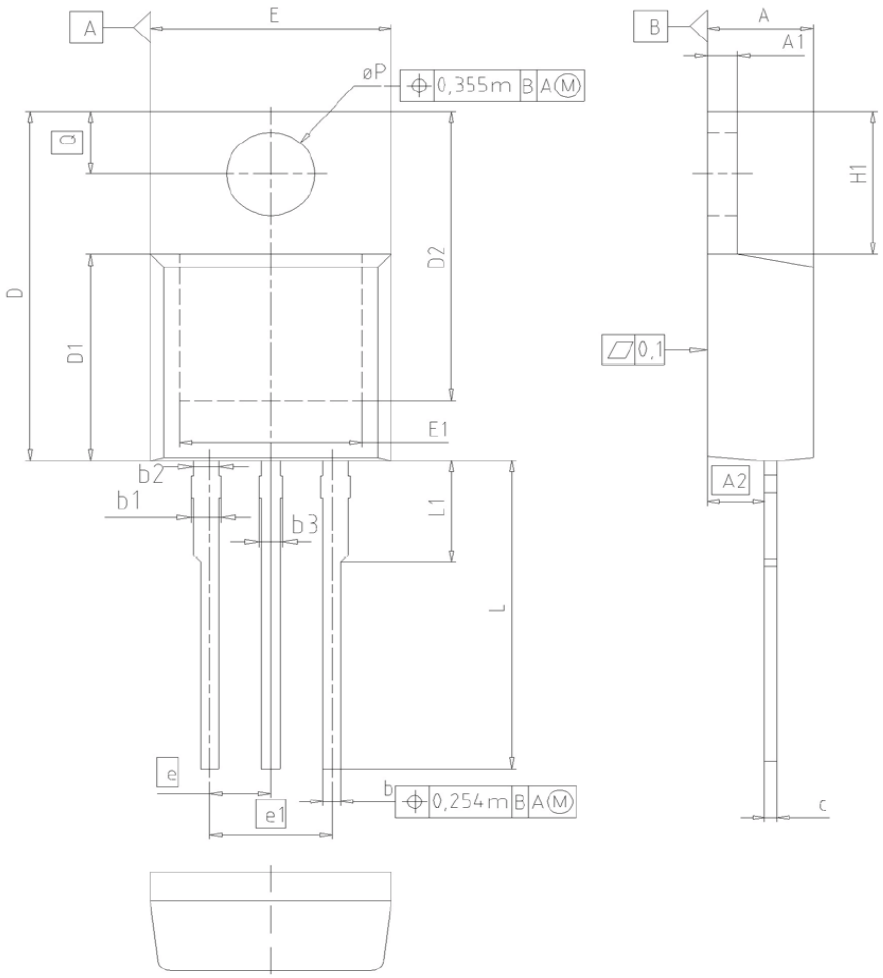
PG-TO262-3 (I²-Pak)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.300	4.572	0.169	0.180
A1	2.150	2.718	0.085	0.107
b	0.650	0.664	0.026	0.034
b1	0.635	1.400	0.025	0.055
c	0.330	0.600	0.013	0.024
c1	1.170	1.400	0.046	0.055
D	8.509	9.450	0.335	0.372
D1	6.900	-	0.272	-
E	9.700	10.363	0.382	0.408
E1	6.500	8.600	0.256	0.339
e	2.540		0.100	
e1	5.080		0.200	
N	3		3	
L	13.000	14.000	0.512	0.551
L1	-	4.800	-	0.189
L2	-	1.727	-	0.068



PG-TO220-3



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	1.17	1.40	0.046	0.055
A2	2.15	2.72	0.085	0.107
b	0.65	0.86	0.026	0.034
b1	0.95	1.40	0.037	0.055
b2	0.95	1.15	0.037	0.045
b3	0.65	1.15	0.026	0.045
c	0.33	0.60	0.013	0.024
D	14.81	15.95	0.583	0.628
D1	8.51	9.45	0.335	0.372
D2	12.19	13.10	0.480	0.516
E	9.70	10.36	0.382	0.408
E1	6.50	8.60	0.256	0.339
e	2.54		0.100	
e1	5.08		0.200	
N	3		3	
H1	5.90	6.90	0.232	0.272
L	13.00	14.00	0.512	0.551
L1	-	4.80	-	0.189
øP	3.60	3.89	0.142	0.153
Q	2.60	3.00	0.102	0.118

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