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Characterization, Operation and Wafer-level Testing of an ultra-fast 4k Pixel Readout ASIC for the DSSC X-ray Detector at the European XFEL

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Zusammenfassung

Das DEPFET sensor with signal compression (DSSC)-Konsortium entwickelt einen 1-Megapixel-Detektor für den Einsatz am europäischen Freie-Elektronen-Laser in Hamburg. Die Anforderungen für das Detektorsystem umfassen unter anderem eine Bildwiederholrate von 4.5 MHz, Auflösung von einzelnen Röntgenphotonen sowie einen hohen dynamischen Bereich. Hierzu wird ein hybrides System eingesetzt, bei dem jeder Pixel der nicht-linearen DEPFET-Sensoren mit einem Kanal auf dem Auslese-ASIC verbunden wird. Jeder der 4096 Pixel auf dem ASIC filtert das Eingangssignal, digitalisiert es und speichert den Wert lokal im Pixel, wodurch eine parallele Auslese der gesamten Sensormatrix erreicht wird. In dieser Arbeit wird das Design der Ausleseelektronik sowie deren Testumgebung und Verifikationsergebnisse erläutert mit Fokus auf mögliche Verbesserungen der Elektronik. Messungen an ersten vollformatigen Sensor- und ASIC-Baugruppen werden vorgestellt mit Fokus auf das geringe Rauschen bei einem hohen dynamischen Bereich. Zudem wird eine Prozedur für die Auswahl von ASICs in großer Zahl für den Einbau in das finale System veranschaulicht. Um den wissenschaftlichen Rahmen für das DSSC-System zu erläutern, ist eine Einführung in Freie-Elektronen-Laser sowie in den Nachweis von Photonen enthalten.

Abstract

The DEPFET sensor with signal compression (DSSC) project develops a megapixel X-ray camera dedicated for ultra-fast imaging at 4.5 MHz frame rate at the European X-ray free electron laser facility in Hamburg. Further requirements are single photon resolution for soft X-rays and a high dynamic range. The system concept includes a hybrid pixel detector, utilizing a non-linear DEPFET sensor. A dedicated readout ASIC allows full parallel readout of a 64 x 64 sensor pixel matrix by in-pixel filtering, immediate analog-to-digital conversion and storage. This thesis presents the ASIC working principle, architecture and the design of a test environment as well as test results of the electronics. Possible improvements of the circuits are highlighted. Measurements on sensor and ASIC assemblies are shown verifying the low noise and high dynamic range properties. The implementation of large scale tests for Known Good Die selection is reported. An introduction to free electron lasers and photon detection principles is included to put the DSSC system into the scientific context.

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1 Introduction

Deeper insights into the structure of matter have always been a motivation for scientists to develop better devices and technologies. Since their discovery by Roentgen in 1895 [1] X-rays had a vast impact on the fields of medicine, chemistry and physics. The most common source for X-rays for everyday applications are X-ray tubes, a vacuum tube in which electrons, accelerated to several 10 keV, hit a metal target and generate X-rays by bremsstrahlung or X-ray fluorescence. In 1985, for the first time, mankind used a high-energy photon source to investigate the structure of matter, in this case, the hands of Roentgen's wife and the chairman of the physical society.

Of special interest for today's researchers are light sources that emit waves with equal phase and frequency (*coherent light*). Recording the coherent light scattered by a sample allows studying the molecular properties of the sample. Lasers emit coherent light, but conventional lasers based on gas or solid mediums are only available in the spectrum from infrared to the ultraviolet regime. In order to resolve structures on a molecular scale, smaller wavelengths are required. Conventional lasers are unsuitable for this task, due to the large power needed for population inversion in the inner atomic levels corresponding to the needed wavelengths.

The first theoretical description of a way to reach smaller wavelengths was given by Motz in 1951 [2]. He described relativistic electrons emitting radiation in a periodic magnet array, today called undulator, following his theoretical work with experimental results in 1953 [3]. It took several decades to develop the scientific desire, but also the theoretical and technical prerequesites to build the first large-scale X-ray Free Electron Laser at the Stanford Linear Accelerator Laboratory (USA), that opened in 2009.

Each step for the radiation sources creates higher demands for detector parameters. The incredibly intense beams with high energy photons of today's sources make radiation hard detectors inevitable. High repetition rates allow for more statistics in the experiments, but impose new challenges on the detector readout and data storage side. To improve the quality of reconstruction algorithm results, high resolution detectors are needed both for the detection of large numbers of photons as well as for single photons.

Moreover, the repetition rate of the new European XFEL machine, under construction in Hamburg (Germany), calls for a full parallel readout of the sensor matrix, with immediate pixel-wise storage in the readout electronics. The desired single-photon detection and, at the same time, high dynamic range create the need for new sensor and readout concepts.

The DSSC (DEPFET Sensor with Signal Compression) is one of the three detector development projects for ultrafast 2D imagers at the European XFEL. The consortium intends to build a 1 megapixel camera with a sensor pixel size of 236x204 μm^2 specially designed to detect low energy X-rays with a 4.5 MHz frame rate. It is based on a novel DEPFET (Depleted Field Effect Transistor) type, featuring both low noise and a signal compression technique to expand the dynamic range. The full format readout ASIC is able to read a 64x64 sensor pixel matrix, digitize the input signal,

and store the result in a local memory, all fully parallelized. The in-pixel memory cells are read out during the 99 ms pause of the XFEL machine.

For the development and verification of the readout electronics, a suitable hardware setup had to be developed. The DSSC prototype test setup is a modular FPGA-based system, which allowed several mini matrix prototype ASICs and the first full format ASIC to be characterized, in a variety of environments including accelerator beamlines. Necessary FPGA firmware has been written for the control and readout of the device under test, sending the data to a custom control and visualization software connected through a USB interface.

This thesis focuses on characterization, test and operation of a main component of the DSSC detector system: the readout ASIC. First, the basics of photon generation in the EuXFEL machine are explained in chapter two. Chapter three contains the principles of photon detection and signal processing from detectors. The general concept of the DSSC detector system is presented in chapter four. Necessary hardware, software and methods for the electronics characterization are described in the fifth chapter, while measurement results and consequences for future designs are presented in chapter six. The following chapter shows the key results of this thesis, where assemblies of the reaodut ASIC mated with DSSC-style sensors allowed to measure the performance numbers of the readout ASIC. The last chapter gives more information about the wafer-level tests conducted on a large number of ASICs in order to select good dies for module assembly.

2
Synchrotron radiation sources

When charged particles like electrons moving at speeds close to the speed of light are forced on a curved trajectory, they emit electromagnetic radiation tangentially to their trajectory. In nature, this can be found by astronomers: In rapidly rotating and strongly magnetized neutron stars named pulsars, relativistic electrons are deflected in the magnetic field and emit synchrotron radiation along the magnetic axes. The radiation is detectable on earth when the beam axes align with position the position of our planet.

Over the course of the last century, the advances of human-made radiation sources have brought fundamental changes not only in medical diagnostics, where they were first used, but also in many other fields of science like chemistry and material sciences. The intensity provided by radiation sources based on accelerator structures was found to be far superior to conventional X-ray tubes, while the energy range covers a large range from the infrared and visible spectrum up to the soft and hard x-ray regime.

For several years, a new generation of light sources has been emerging: The Free Electron Laser (FEL). These typically km-long devices enable scientists to use not only a brilliance several orders of magnitude higher than previous sources, but also with a fixed phase relation. The fully coherent light, similar to conventional laser light, is a viable tool for science on the nanoscale.

An overview of the evolution of synchrotron radiation sources will be given in this chapter, as well as a summary of the basic principles of a free electron laser. A short introduction to the experimental techniques used nowadays is presented to put the detector systems into the scientific context. This chapter has been compiled using the publications by Bilderback [4], Wiedemann [5], Schmüser et al. [6] and Pellegrini [7].

2.1 History

Synchrotron radiation was first observed in 1947 at the General Electric synchrotron in the USA as a disturbance, causing energy loss of the particles to be accelerated. For years, synchrotron radiation was seen as a problem by the physicists, until the usefulness for imaging has been realized. Designed for high energy particle physics, the first storage rings were equipped with simple bending magnets to keep the particles on track. In the bending magnets, synchrotron radiation was emitted and could be extracted by holes in the beam pipes - a parasitic usage of the particle accelerators.

In the bending magnets of a storage ring, electrons moving with relativistic speeds are accelerated towards the center of the magnet, emitting synchrotron radiation. Usually, different electrons in a bunch radiate independently of each other, resulting in incoherent radiation. The radiation's frequency spectrum, depicted in figure 2.1, is continuous from zero to frequencies beyond the critical

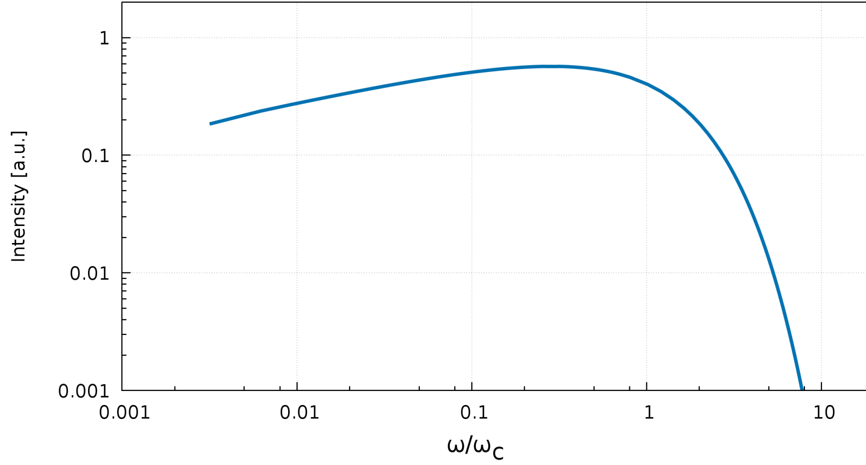

Figure 2.1: Frequency distribution of radiated energy in a bending magnet. The radiated energy covers a broad spectrum and drops quickly above the critical frequency.

frequency ω_c:

$$\omega_c = \frac{3}{2}\frac{c\gamma^3}{R} \tag{2.1}$$

where R is the radius of the bending magnet and γ is the relativistic Lorentz factor. The total energy radiated is divided in half by the critical frequency. The majority of the radiated power is centered inside a narrow cone for high energy particles, given by the opening angle of about $\pm 1/\gamma$. Note that the critical frequency is tunable by the particle energy represented by the Lorentz Factor. Expressed in commonly used quantities (particle energy and magnetic field) and units, the resulting critical photon energy can be written as

$$\hbar\omega_c[\mathrm{keV}] = 0.665\, E^2[\mathrm{GeV}]\, B[\mathrm{T}] \tag{2.2}$$

Typical storage rings built in the 1960s could reach the hard X-ray regime by an electron beam of around 5 GeV and a 6 T field.

In general, one of the most important parameters of a radiation source is its peak brightness. It is described by the *brilliance*, taking into account the spectral purity around the central frequency and the opening angle:

$$B = \frac{\Phi}{4\pi^2 \Sigma_x \Sigma_{\theta x} \Sigma_y \Sigma_{\theta y}} \tag{2.3}$$

where Φ is the spectral photon flux, defined as the number of photons per second and within a given relative spectral bandwidth. Typically, a bandwidth of 0.1% is used. Σ_x, $\Sigma_{\theta x}$ and the corresponding quantities in y direction describe cross-sectional area of the beam and its angular divergence, which are usually combined in the beam emittance in the two transversal planes ϵ_x and ϵ_y. In the literature, the terms brilliance, brightness and intensity are used synonymously.

The synchrotron light sources are, in a historic perspective, grouped into generations, where each new generation has made a leap forward in terms of brightness by at least one order of magnitude.

The first generation of synchrotrons was optimized for high particle energies or as many electron-positron collisions as possible. After the usefulness of the initially annoying synchrotron radiation has been realized, second generation synchrotrons were designed as photon sources. Apart from the dedication of a larger fraction of beamtime to photon scientists, the fundamental differences include a lower emittance to increase the brilliance (see equation (2.3)). As the emittance increases with the bending angle in dipole magnets, a smaller emittance of the beam could be reached by segmenting the bending magnets and adding focusing magnets in between them. The first storage rings to be operated solely to meet the demand for synchrotron radiation were commissioned in 1981, for example at the Synchrotron Radiation Source (SRS) in the UK or the National Synchrotron Light Source (NSLS) at Brookhaven National Laboratory. These already achieved brilliances on the order of 10^{14} to 10^{15} $\frac{\text{photons}}{\text{s mm}^2\,\text{mrad}^2\,0.1\%\text{BW}}$.

2.2 3rd generation synchrotron light sources

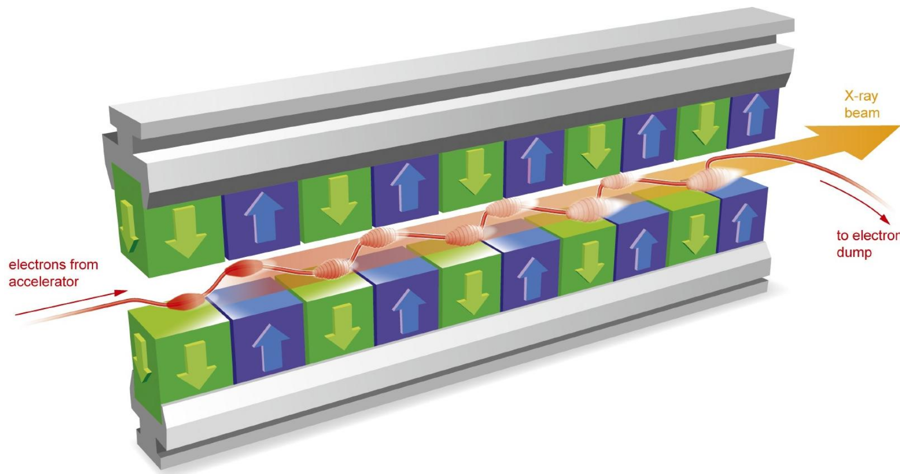

Figure 2.2: An undulator is an array of magnets of alternating polarity, forcing charged particles traversing it on an oscillating track and therefore to radiate photons.

The use of arrays of alternating magnets brought a major increase of brilliance for light sources compared to simple bending magnets. These devices are called undulators or wigglers and are specially designed for the generation of synchrotron radiation by forcing particles on a sinusoidal trajectory by the Lorentz force (figure 2.2).

The magnet arrays are mainly characterized by the undulator parameter K, defined as

$$K = \frac{\lambda_u e B_0}{2\pi m_e c^2} = 0.934\,\lambda_u[\text{cm}]B_0[\text{T}] \tag{2.4}$$

where λ_u is the magnet period and B_0 the magnetic field strength. Devices with $K > 1$ are called Wigglers. The strong magnetic field forces electrons on an oscillating path with a large amplitude. The emitted synchrotron radiation does not interfere, like in a series of bending magnets, resulting in a broad spectrum with an intensity proportional to the number of magnets ($I \propto N$). Undulators usually have a smaller magnetic field with $K \leq 1$, forcing the particles to oscillate with a smaller

amplitude. Constructive interference between the emitted photons on the beam axis results in a spectrum with sharp lines. However, the reachable photon energy is smaller, due to the weaker magnetic field. The radiation can increase with up to the second power of the number of magnetic periods ($I \propto N^2$).

The resonance condition for constructive interference in the undulator gives the photon wavelength of the first harmonics:

$$\lambda_{ph} = \frac{\lambda_u}{2\gamma^2} \left(1 + \frac{K^2}{2} + \gamma^2\theta^2\right) \tag{2.5}$$

where λ_u is the undulator period, K is the undulator parameter, and θ is the emission angle. The last part shows that the radiation wavelength is shortest along the beam axis and increases with the angle θ. As for the particle in the bending magnet, virtually all radiation is emitted in a narrow cone with an opening angle of $\theta = \pm\frac{1}{\gamma}$. Moreover, the equation shows that tuning of the wavelength of the emitted radiation can be achieved by changing the particle energy, and by modifying the undulator mechanics and magnetic field.

Today's state-of-the-art synchrotrons like PETRA 3 or ESRF typically have a brightness of about 10^{23} to 10^{24} $\frac{\text{photons}}{\text{s}\,\text{mm}^2\,\text{mrad}^2\,0.1\%\text{BW}}$ at an electron energy of a few GeV.

2.3 Free Electron Laser Light Sources - 4th generation

In spite of their scientific achievements, scientists called for an upgrade to the 3rd generation synchrotrons. A higher brilliance, but also shorter X-ray pulses were the main requests. The shortest X-ray pulses the synchrotrons can provide are several 10 ps long. The timescale of molecular processes, on the other hand, is in the picosecond range. Recording intermediate states of such reactions would require much shorter laser pulses, which can be realized by the free electron laser.

Laser is an acronym for Light Amplification by Stimulated Emission of Radiation. Historically, a laser is made up of three elements: a laser medium, an energy pump, and a resonator. The pump generates population inversion in the discrete energy states of the laser medium. By stimulation through a photon with the desired wavelength, an excited atom can emit a photon with identical wavelength and phase. Both photons travel in the same direction and will act as stimulation for further emissions. Because of the resonator, each photon repeatedly passes the laser medium, being amplified each time.

A free electron laser uses a completely different principle. Here, electrons generated by an electron gun are accelerated to energies up to several GeV. Subsequently, they are guided into undulators, thereby emitting radiation. In contrast to the undulators used in today's synchrotron facilities, the undulators of an FEL are much longer, allowing the radiation to interact with the electron beam. We will see in the following, that the FEL light output has similar properties to conventional lasers: it is almost monochromatic, polarized, coherent, collimated and has an extremely high brilliance. Moreover, its wavelength can be adjusted through several parameters, which is not possible in this magnitude for conventional lasers.

John Madey published the first work on the Free Electron Laser (FEL) in 1971 [8] with a quantum mechanical description of the stimulated emission of bremsstrahlung by relativistic electrons passing through a periodic magnetic field. The concept consisted of a linear accelerator, an undulator, and an electromagnetic wave as a stimulation input. The first FEL with a photon wavelength of 10.6 μm was built by Madey and his colleagues at Stanford University in the following years [9]. It

took many more years for the scientific community to realize the possibility of unprecedented light sources using FELs.

Two FEL variants have been developed (figure 2.3):

- A low-gain FEL, where the electrons are circulating in a storage ring and are going through a relatively short undulator many times. The radiation is captured, similar to conventional lasers, by optical mirrors. Each time the electrons pass through the undulator, the radiation intensity grows.
- No suitable mirror materials are available today for the X-ray and extreme ultraviolet regime. The amplification must thus be achieved in a single transit of the electrons through the undulator. The high-gain FEL, further described in this section, solves the problem by using very long undulators to build up the radiation intensity, requiring only a single pass of the electron bunch.

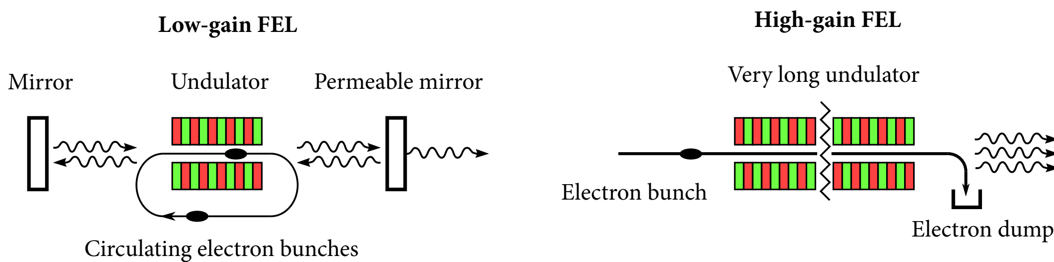

Figure 2.3: Left: Low-gain FEL using mirrors. Right: Single pass high-gain FEL.

In the following, certain aspects of the high-gain FEL theory are highlighted. First of all, as for 3rd generation synchrotrons, the resonance condition for undulators (2.5) holds true. The wavelength is thus depending on the Lorentz factor γ, and the properties included in the undulator parameter K, namely the magnetic field strength and the undulator period.

The intensity of the radiation grows quadratically with the number of coherently acting particles N. Ideally, all particles of a bunch would be concentrated into a region far smaller than the light wavelength, making them all radiate coherently. The problem is obviously to concentrate the $\approx 10^9$ electrons of a bunch into such a small volume. The solution to this technical problem is the process of *microbunching*, describing an interaction of the electromagnetic wave with electrons ahead in the undulator: Electrons that are losing energy to the light wave are forced on a larger sinusoidal trajectory through the magnet arrangement than those gaining energy from the wave. Both energy transfer between wave and electrons and the dispersion in the magnet field leads to concentration of the electrons into slices, where the electric field strength is zero, i.e. in distances of the wavelength.

At the beginning of the undulator, without microbunching, all N electrons in a bunch can be seen as individually radiating particles, with a radiation power $\propto N$. The radiation interacts with electrons further ahead in the undulator, arranging them in disks separated by the light wavelength through energy transfer. Over the length of the undulator, the radiation growth is making the electron arrangement forces stronger. With micro-bunching completed, all electrons radiate in phase, resulting in a radiation power $\propto N^2$, as shown in figure 2.4. Along the way through the undulator, the radiation power grows exponentially as given by

$$P(z) = A\,P_0\,e^{z/L_g} \tag{2.6}$$

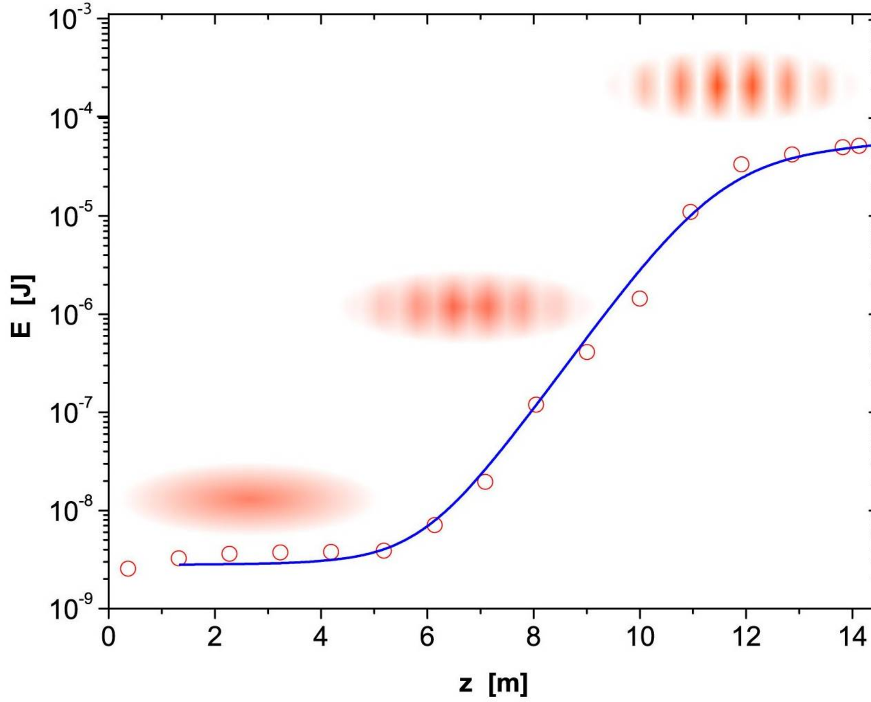

Figure 2.4: The growth of the radiated power as a function of the position in the undulator z, obtained at the TESLA Test Facility. The progression of the microbunching is sketched above the data. Saturation sets in for $z \leq 12$m. [10]

where P_0 is the input power, z is the distance along the undulator, L_g is the power gain length, and A is a coupling factor. For an ideal electron beam in one-dimensional FEL theory, A is equal to 1/9. The exponential growth is limited by complete bunching of the electrons resulting in saturation of the radiation power.

The power gain length used here describes the length after which the beam power has increased by a factor of 2.718 and can be derived as

$$L_g = \frac{\lambda_u}{4\sqrt{\pi}\rho_{FEL}} \tag{2.7}$$

where the important FEL parameter ρ_{FEL} has been used.

$$\rho_{FEL} = (\frac{K}{4}\frac{\Omega_p}{\omega_u})^{2/3} \tag{2.8}$$

where $\Omega_p = (4\pi n_e r_e c^2/\gamma^3)$ is the beam plasma frequency, n_e is the electron bunch density and $\omega_u = 2\pi c/\lambda_u$. It is evident that the FEL parameter can be increased (and the gain length reduced) by increasing the peak current and reducing the transverse extent of the electron beam.

Generally, a FEL will show a larger power gain length, since effects of space charge, energy spread, betatron oscillations and diffraction have been neglected here and tend to reduce the effective gain per unit length, thus increasing the gain length.

Using the FEL parameter, the saturation power can be written as

$$P_{sat} = \rho_{FEL} E I \tag{2.9}$$

with the electron beam energy E and its current I. The FEL parameter ρ_{FEL} apparently describes the ratio of the beam power transferred to the radiation and is typically on the order of 10^{-3}. Saturation is usually reached after the saturation length

$$L_{sat} \approx 20\, L_g \tag{2.10}$$

which can easily extend over more than 100 m for hard X-ray FELs. The bandwidth of the ideal high-gain FEL is given by

$$\frac{\Delta\lambda}{\lambda} = 2\frac{\Delta\gamma}{\gamma} = 2\rho_{FEL} \tag{2.11}$$

X-ray FELs impose high requirements on the quality of the electron beam. The importance of a high peak current for gain length reduction has been mentioned already. The longitudinal compression also reduces the timescale of the FEL radiation to the 10 fs regime. Reducing the transverse beam size in the long undulators helps to ensure the energy transfer between electron and photon beam. Finally, a low energy spread within the beam on the order of the FEL parameter is necessary to achieve laser saturation and to limit the spread of emitted wavelengths. All these requirements are so demanding that they are currently only realizable with linear accelerators.

The startup of the lasing processes typically needs seed radiation of the desired wavelength. For X-rays, no suitable radiation source is known - the use of higher harmonics of optical lasers has been evaluated. However, the *Self-Amplified Spontaneous Emission* (SASE) mechanism allows lasing start-up at any wavelength without requiring an external seed radiation. This mechanism makes use of the emission of spontaneous undulator radiation by electrons in the first section of a long undulator, which is then acting as seed radiation further on.

SASE FEL radiation can be seen as a chaotic process, since it relies on the noisy distribution of the electron beam, resulting in a variety of seed wavelengths. The energy spectrum therefore shows slight pulse-to-pulse variations, depending on the amplified wavelength. Moreover, the spectra from SASE undulator radiation typically show intense peaks on top of a white noise background.

The peak brilliances of third and fourth generation light sources are shown in figure 2.5. An increase of several orders of magnitude has been reached. The main physical reasons for the high peak radiation power are

- the coherent superposition of the radiation fields from the large number of particles in a microbunch (large power),
- and the coherent superposition of the radiation fields from the microbunches within a coherence length (small divergence and narrow bandwidth).

Table 2.1 summarizes the currently active FELs at LCLS in Stanford, USA, and SACLA in Japan. Several other FELs are planned or already under construction. The European XFEL, recently commissioned in Hamburg, Germany, will be explained in more detail in the next section. The LCLS-II upgrade will upgrade the accelerator with a new superconducting linac extending the electron energy range up to 18 keV, increase the repetition rate above 100 kHz, and will add new sets of undulators to increase the energy range of LCLS. In Europe, several other FELs are under construction: FERMI is a new seeded FEL under commissioning in Trieste, Italy, SwissFEL is currently built at

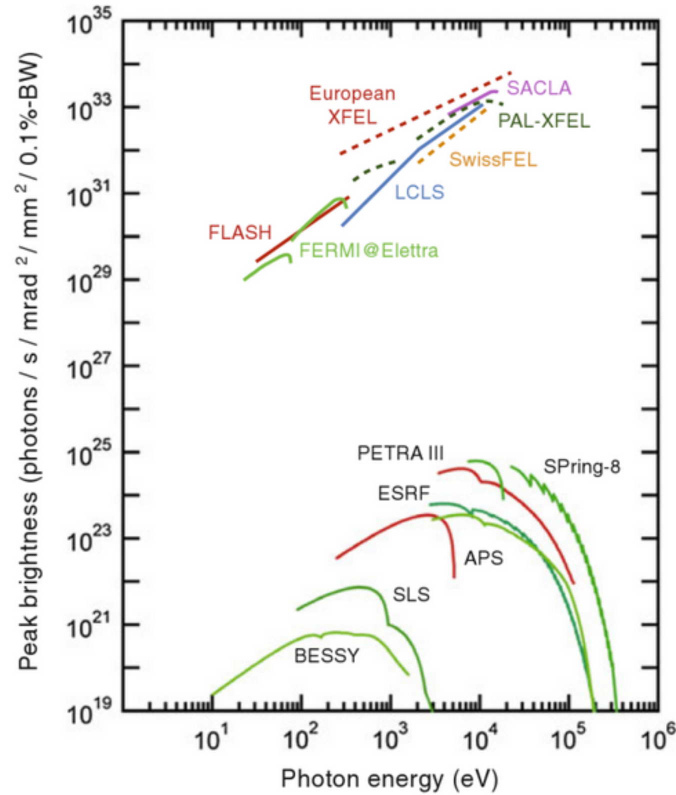

Figure 2.5: Peak brilliance of 3rd and 4th generation light sources. Free electron lasers bring a leap forward by many orders of magnitude in peak brilliance compared to synchrotron sources. [6]

the Paul-Scherrer-Institut, Switzerland, and will be a relatively compact, 740 m long FEL with wavelengths between 0.1 and 7 nm, comparable to SACLA.

2.4 The European XFEL

The main element of the European XFEL machine is the superconducting linear accelerator. The necessary technology has been developed in a previous project called *TeV-Energy Superconducting Linear Accelerator* (TESLA). TESLA was planned around the turn of the millennium as a 33 km long linear accelerator for high-energy physics and an integrated 4 km long X-ray free electron laser. The two subprojects have been split up later: The idea of a long linear accelerator for particle physics is now projected in the *International Linear Collider* (ILC) framework, while the X-ray free electron laser has been prototyped as *FLASH* (Freie-Elektronen-Laser in Hamburg) and is now realized in the *European XFEL* (EuXFEL) project.

An in-depth technical description of the EuXFEL machine can be found in [14] with more recent updates to be found in [15]. The key technical points of the machine are summarized here.

The journey of the electrons starts at the injector. The injector for the Linac is formed by an RF gun, an acceleration module and a diagnostic part. An electron bunch is emitted from a Cs_2Te

	Facility length	Max. electron energy [GeV]	Max. photon energy [keV]	Flashes per second
LCLS [11]	1.13 km	14.35	10	120
SACLA [12]	0.7 km	8.5	10	60
EuXFEL [13]	3.4 km	17.5	25	27000

Table 2.1: Comparison of today's constructed X-ray free electron lasers. The peak brilliance of all these facilities is on the order of $10^{33} \frac{\text{photons}}{\text{s}\,\text{mm}^2\,\text{mrad}^2\,0.1\%\text{BW}}$.

Figure 2.6: Superconducting cavity developed in the TESLA framework. The cavity is made out of Niobium, the pure metal with the highest critical temperature of 9.2 K and highest critical magnetic field. [13]

cathode illuminated by a UV laser pulse. The laser pulse is only 20 ps long, causing a 1 nC charge to be emitted. The cathode is located in a high accelerating field with a gradient of 60 MV/m on the cathode and 30 MV/m on average in the 0.25 m long gun cavity. A solenoid focuses the beam into the first accelerator module, located after a 3 m long drift segment. The first accelerator module accelerates to about 120 MeV. A diagnostics section at the end of the injector part supervises the beam emittance and energy spread. Measurements have shown a final normalised transverse emittance below 1 mrad mm, which can be tuned by reducing the initial laser spot size.

The linac itself consists of 672 superconducting cavities, one of them shown in figure 2.6. The

nine-cell standing wave structure of 1 m length has a fundamental TM mode frequency of 1300 MHz. The cavities are made out of solid Niobium, cooled by superfluid Helium at 2 K. The nominal acceleration gradient is 23.6 MV/m. The superconducting cavities have been chosen because of their extremely low surface resistance at 2 K with RF losses being five to six orders of magnitude lower than in conventional copper cavities. However, proper treatment of the surface is extremely challenging, as contaminations or mechanical defects on the surface decrease the quality factor and may even lead to thermal breakdown of the superconductor due to local overheating. Perfect cleaning of the inner cavity surface is of utmost importance, final cavity treatment and assembly is therefore done in clean rooms.

The cavities are assembled in 84 modules, each containing eight cavities and a package of superconducting magnets, consisting of a quadrupole and two dipole magnets for beam corrections in both horizontal and vertical planes. A beam position monitor is also included in the module. The quadrupoles in the accelerator modules are alternatingly focusing and defocusing. Focusing quadrupole magnets are focusing in horizontal direction and defocusing in vertical direction, while defocusing quadrupoles are horizontally defocusing and vertically focusing. This *FODO* structure results in a focusing effect in both dimensions. The FODO cells used here have 24 m length.

Since the longitudinal profile of the beam is limited by space charge effects in the electron gun, a high peak current needed for the SASE process can only be reached after accelerating them to relativistic energies. Bunch compressors, utilizing the energy dependence of the path length in a magnetic field, increase peak current of the beam to 5 kA before the main linac by sending the beam through a magnetic chicane.

After the main linac, a fast kicker is located. Unwanted bunches can be sent to beam dump at the full bunch frequency of 4.5 MHz, so specific pulse patterns can be produced by this kicker. Before the two beam lines (see below), a second, slower kicker is located with a typical pulse width of 290 μs, called *flat top kicker*. Using this kicker, the beam is distributed in the different undulator beamlines. During the kicker switching time of 20 μs, the upstream dump kicker will remove any bunches, until the flat top kicker field is stable.

An aerial map of the whole machine is shown in figure 2.7 with the planned beamline layout given in figure 2.8. The injector, the start of the 3.4 km long complex, is located on the DESY campus in Hamburg-Bahrenfeld. After passing the 2.1 km long linear accelerator, the electron bunches are distributed towards the individual beamlines is located in the Osdorfer born area, northwest of the injector complex. A first beam dump is placed here as well. The tunnel starts to fan out here, followed by the undulators and the experimental hall in Schenefeld.

Two different undulator types are foreseen, summarized in table 2.2: Hard X-rays with an energy between 3 and 25 keV can be generated at SASE1 and SASE2 with an undulator period λ_u of 40 mm. The photon energy can be tuned by changing the electron energy or by changing the magnetic gap of the undulators. SASE3 has a larger undulator period of 68 mm and is designed to provide soft X-rays with energies between 0.25 and 3 keV.

Undulator system	λ_u	Wavelengths	Photon energy	Magnetic length
SASE1 & SASE2	40mm	0.4 - 0.05 nm	3 - 25 keV	175m
SASE3	68mm	4.7 - 0.4 nm	0.25 - 3 keV	105m

Table 2.2: Undulators planned for the European XFEL [16].

Figure 2.7: Aerial map of the European XFEL machine [13]. The injector complex can be seen in the lower right part, the electrons are accelerated in a 2.1 km long Linac towards the undulators in the Schenefeld area in the upper left.

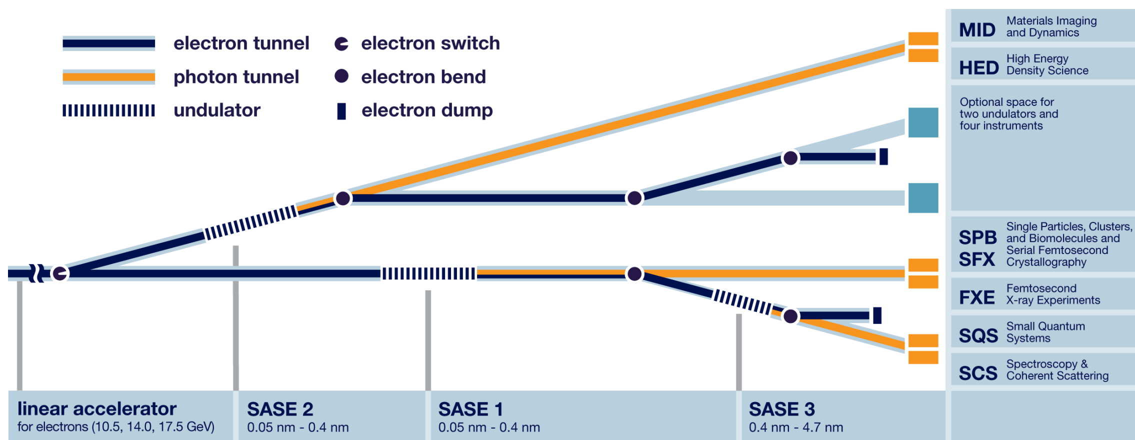

Figure 2.8: Planned layout of the beamlines at the European XFEL [14]. Several undulators are served by the linac to generate high brilliance pulses.

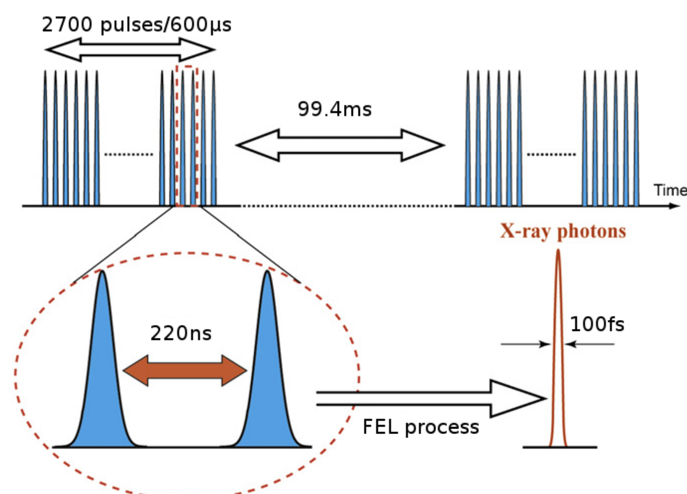

Figure 2.9: The EuXFEL features a unique X-ray bunch timing of 220 ns bunch spacing and 100 fs photon pulse length. A set of 2700 bunches is followed by a pause of 99.4 ms [14].

The X-ray pulses are generated by the European XFEL machine with an exceptional timing, depicted in figure 2.9. The machine generates *trains*, composed of up to 2700 X-ray pulses spaced by 220 ns (4.5 MHz bunch frequency). Each train thus has a length of 600 µs. Trains are repeated every 100 ms (10 Hz train frequency), leaving a long gap of 99.4 ms. As explained above, the FEL process in the undulator will generate X-ray pulses of only 100 fs length.

The 4.5 MHz bunch frequency originates from the injector RF gun, which is running at this frequency. The limitation of the number of pulses per second is related to the maximum load of 300 kW on each of the solid state beam dumps in the two initially installed beamlines. 300 kW relate to about 1700 bunches per train at a bunch charge of 1 nC and a train rate of 10 Hz.

One of the main wishes of scientists is, of course, to increase the number and intensity of flashes available for the experiments. Both repetition rate and beam energy can be varied to some degree, limited by the available power for the RF and the cryogenic systems. A strong increase of the machine duty cycle would however make improvements of these systems mandatory, also regarding the injector part. As a mitigation, the number of bunches per train could be reduced to compensate an increased repetition rate.

2.5 Experimental techniques

The European XFEL opens up new experimental possibilities. Typically, diffraction experiments will be conducted, sketched in figure 2.10. The photon beam generated in the undulator, usually being mostly undeflected, travels through a central hole in an imaging detector towards the beam dump. Targets can be brought into the photon beam, causing X-rays to be scattered and creating a diffraction pattern on the detector plane. The 2D detector records the diffraction images for offline analysis, allowing to calculate the atomic structure of the target.

While being a well-known technique widely in use at today's synchrotron facilities, FEL radiation establishes new use cases due to its supreme properties. Short pulse widths of 100 fs and fast frame rates up to 4.5 MHz allow the generation of movies of chemical reactions. Shorter wavelengths

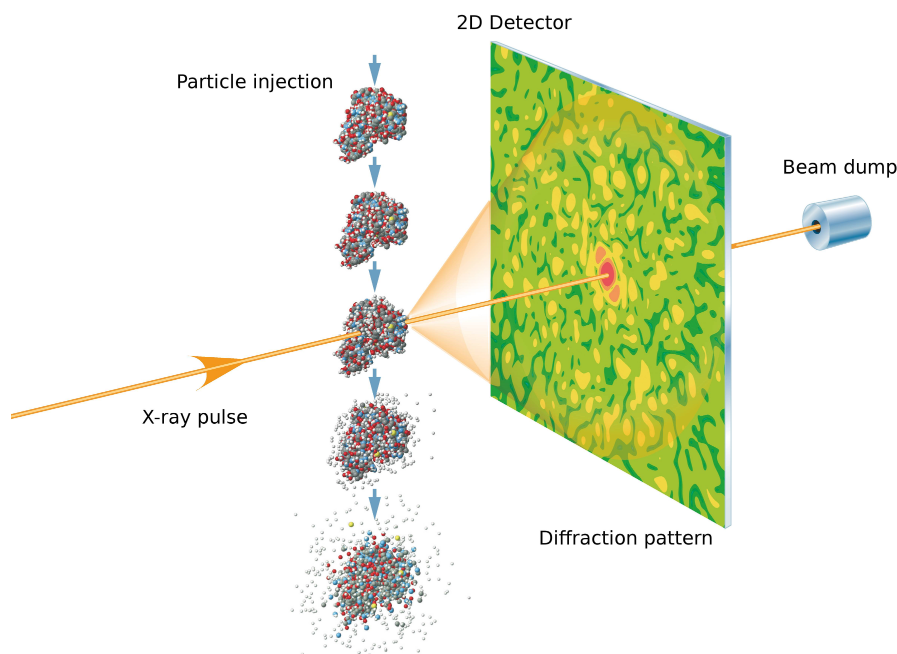

Figure 2.10: Typical X-ray scattering experiment [13]. The incident X-ray beam is scattered by the target particles, creating diffraction patterns on the 2D imaging detector plane. The sample molecule is destroyed by the intense beam.

allow smaller structures to be resolved, helping the progress of material sciences. Moreover, the enormous peak brilliance allows to study matter under extreme conditions.

The analysis of molecular structures by scattering experiments requires sufficient statistics of the diffraction patterns, either through long irradiation times or repeated measurements of similar samples. The irradiation with the tremendous brilliance given at the European XFEL will however degrade or destroy the target [17] already after one pulse, especially for biological samples. The ultra-short pulse duration allows to record a single diffraction pattern, since the timescale for molecular damages are typically longer [18]. Repeated measurements, on the other hand, requires crystallization of the samples, which is not possible for many molecules so far. Current research is targeted to mitigate the need for growing large crystals by using a liquid jet of nanocrystals to acquire snapshots of single nanocrystals [19].

The atomic-scale behaviour of molecules during chemical reactions will be the focus of research in pump-and-probe experiments. Here, the chemical reaction of a probe is started with an optical or infrared laser pulse before the probe X-ray pulse from the XFEL arrives. The reaction can then be recorded by changing the time interval between the pump and the probe pulse. This technique will allow for recording movies of molecular reactions with resolution on the atomic scale, allowing researchers to better understand the dynamics of chemical processes.

Several instruments are being prepared in close cooperation with the user community at the European XFEL, making use of the previously mentioned techniques. Hard X-rays from the SASE1 or SASE2 undulators will be used for:

SPB/SFX - Ultrafast Coherent Diffraction Imaging of Single Particles, Clusters, and Biomolecules,

Serial Femtosecond Crystallography, primary focus on biological targets like macromolecules, viruses and cells.

MID - Materials Imaging and Dynamics, analysis of structures and dynamics at nanolevel.

FXE - Femtosecond X-ray Experiments, designed for studies of the dynamics of chemical and biochemical reactions in liquids as well as solid state physics studies.

HED - High Energy Density Matter, matter under extreme pressure, temperature or electric field conditions will be under study here.

Soft X-rays from the SASE3 undulator will be used at these instruments:

SQS - Small Quantum Systems, this instrument will research processes in atoms, ions or small molecules under intense beams.

SCS - Spectroscopy and Soft x-ray Coherent Scattering, for the investigation of electronic and atomic structures and dynamics of soft matter, biological samples, and material samples.

2.6 Detector requirements at the European XFEL

The high frame rate, high brilliance and high photon energy of the XFEL calls for new detectors. Three detector development projects have been started: *AGIPD*, *DSSC* and *LPD*. The main requirements for these high speed X-ray cameras are summarized in [20]:

- Detection of photons with an energy range between 250 eV and 90 keV, not to be covered by a single detector.
- Single photon detection. This is related to the detection of higher orders of the scattering peaks, which allow a higher precision after reconstruction, but also for background detection, which can be caused by stray light caused by the experiment itself. Several tens of photons should be detected with single photon resolution.
- Dynamic range of up to 10^4 photons for scattering peak detection and differentiation. For higher numbers of photons, single photon detection is not necessary any more, since the photon generation and scattering processes underlie Poisson statistics. This poses an upper limit on the measurement accuracy.
- Single shot imaging. Due to the enormous peak brilliance, the sample under study will not survive a single shot, so each scattering image has to be treated on its own.
- Record as many images of the burst as possible. The high frame rate of single shots to be taken imposes temporary image data storage inside the readout pixel. Furthermore, full parallel readout of all pixels is necessary, as the detectors have to finish processing an image after 220 ns.
- A central hole is needed in the detector mechanics to let the unscattered part of the high intensity beam through.
- When detecting hard x-rays, radiation tolerance is mandatory. Although the sensor itself may shield the readout electronics to some extent, total absorption doses in the GGy regime can be expected.

All of these requirements must be met simultaneously. The DSSC detector will be explained in more detail in chapter 4, accompanied by a comparison with the AGIPD and LPD systems, after an introduction to the detection of photons in today's detectors in chapter 3. Some details about the AGIPD and LPD systems are given for a comparison in section 4.5.

3 Photon detection

The advances of synchrotron radiation sources in the last decades have been accompanied with technological developments in the field of photon detection.

This chapter intends to introduce the reader to the fundamentals of photon detection in modern detectors and the DSSC camera in particular. The physical effects exploited for the detection are presented as well as technological aspects of different detector technologies. In the last section of this chapter, an analytical view on noise sources in detectors will be presented, including theoretical aspects of signal processing in detectors.

This chapter has mainly been composed using the books by G. Knoll [21], H. Spieler [22], G. Lutz [23] and Rossi et al. [24], with more specific references given in the text.

3.1 Interaction of photons with matter

While a large number of interaction mechanisms are possible for photons in matter, only three types are dominant in current detectors: photoelectric absorption, Compton scattering and pair production. These mechanisms result in partial or complete energy transfer from the photon to electrons in the absorbing material.

The process in which an electron is removed from its shell in an atom and ejected as an energetic photoelectron is called photoelectric absorption. The energy of the photoelectron is given by the energy of the photon, reduced by the energy needed to remove it from its bound shell. The vacancy in the remaining ionized atom is quickly filled by a rearrangement of the other electrons or by capturing a free electron, leading to the emission of further characteristic X-rays. The photoelectric effect dominates at energies below 100 keV and its cross-section is strongly affected by the atomic number Z of the absorbing material ($\sigma_{photo} \propto Z^4$).

Compton scattering describes the inelastic scattering of a photon by a charged particle, i.e. in matter, an electron. A part of the photon energy is transferred to the electron, given by the scattering angle. The scattering probability increases linearly with the number of scattering targets available and thus with the atomic number Z of the absorbing matter. The differential cross-section is described by the Klein-Nishina formula. In the low energy case, the Klein-Nishina formula can be simplified to yield the classical Compton formula for the wavelength shift

$$\lambda' - \lambda = \frac{h}{m_e c}(1 - \cos \Theta) \tag{3.1}$$

peaking if the direction of the scattered photon is reversed with respect to the incident photon, i.e. $\Theta = 180°$. This maximum is recognized as the Compton edge when plotting the energy of the emitted photons.

Pair production occurs in the presence of a nucleus when the photon energy is sufficiently high to produce an electron-positron pair. 1.02 MeV, twice the rest-mass energy of the electron, are needed, all excess energy is converted to kinetic energy of the created pair. Roughly above 10 MeV, the cross-section of pair production exceeds Compton scattering.

The attenuation of a beam containing many photons can be described by an absorption probability per unit path length, the attenuation coefficient. The beam intensity after a given path length is then given by the exponential decrease described by the Lambert-Beer law

$$I(x) = I_0\, e^{-\mu x} = I_0\, e^{-\frac{\mu}{\rho}\rho x} \tag{3.2}$$

where I_0 is the intensity of the incident beam, μ is the attenuation coefficient, and x is the distance travelled in the medium. Often, the mass attenuation coefficient $\frac{\mu}{\rho}$ instead of the attenuation coefficient is used. The mass attenuation coefficient depends strongly on the photon energy, since the underlying absorption cross sections are affected by the photon energy. Figure 3.1 shows the attenuation coefficient in silicon for a wide range of energies, being of primary interest with respect to the DSSC camera. The plot shows that for photon energies well above 10 keV the efficiency of absorption rapidly drops to values where only a small fraction of the beam is absorbed in a typical thin detector.

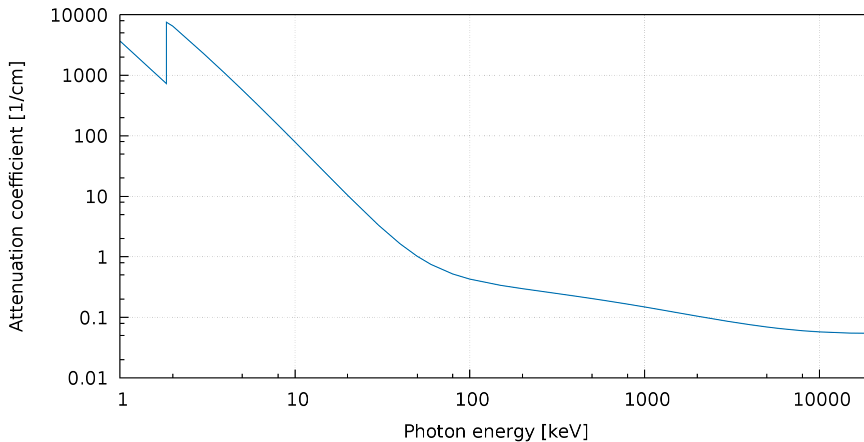

Figure 3.1: X-ray attenuation coefficient for silicon as a function of the energy [25]. The sharp edge at low energies is related to the K_α absorption edge.

3.2 Modern photon detectors

Photon detectors can be classified by the absorber material used to convert incident radiation to an electrical signal, or by their performance criteria. A few common criteria are discussed here.

The *quantum efficiency* describes the probability of an electron being released by an incident photon by one of the effects explained above. For a larger number of photons, this is given by the ratio of generated electrons and the number of photons. The quantum efficiency is typically a function of the photon energy.

In spectroscopy applications, the aim is to measure the energy distribution of the incident photons. Since the charge generated within the detector volume is composed of a discrete number of charge carriers, statistical fluctuations from event to event of absorption are introduced for the number of charge carriers. The *energy resolution* is conventionally defined as the ratio of full width at half maximum (FWHM) and the peak centroid energy:

$$R = \frac{FWHM}{E_0} \tag{3.3}$$

The smaller the energy resolution, the better the detector can distinguish between two radiation energies close together. Assuming a Poisson process for the generation of N charge carriers, a Gaussian distribution with a standard deviation of $\sqrt{N}$ is expected, whose FWHM is given by $FWHM = 2.35\sigma$. If we assume a linear detector response for the typically large number N of charges, we can calculate the expected resolution limit as

$$R_{Poisson} = \frac{FWHM}{E_0} = \frac{2.35K\sqrt{N}}{KN} = \frac{2.35}{\sqrt{N}} \tag{3.4}$$

with a proportionality factor of K for relating the charges to the energy. It is evident that the energy resolution is improved by increasing the number of charge carriers N generated per event.

Measurements have shown however that some types of actual detectors achieve a much smaller energy resolution than expected by the calculations above. The *Fano Factor* is used to relate the observed variance to the variance expected from Poisson statistics:

$$F = \frac{\text{Observed variance in N}}{\text{Poisson predicted variance (N)}} \tag{3.5}$$

Realistic models to describe the processes in semiconductors have been developed by Alig [26] and Fraser [27] in the 1980s, also allowing to calculate the Fano factor. The models are in good accordance with the measured values for silicon of about $F_{Si} = 0.1$ and also describe the radiation energy dependence of the electron-hole pair creation.

The *dead time* is used to describe the minimum time that has to pass between two events to allow the detector to register them as separate events. It can originate in the sensor element or in the readout electronics. High rate applications may need corrections for dead time losses in counting detectors.

3.2.1 Gaseous detectors

The most commonly used type of photon detectors are based on the ionization or excitation of a gas by incident photons or high energy particles. In an ionization process, an electron-ion-pair is created in the volume of the measurement chamber. While the first ionization energy for typical detector gases is somewhere between 10 und 25 eV, the energy needed to create an electron-ion-pair is higher at about 30 to 40 eV. This is due to other processes like excitation of electrons to higher bound states that contribute to photon energy loss, but do not create signal in the detector.

An electric field externally applied between the readout electrodes separates the electron-ion pairs and forces them to drift towards the electrodes. Constant acceleration due to the electric field and deceleration due to collisions with gas molecules result in a mean velocity, affected by the electric field, the gas pressure and the particle type. Electrons typically have a drift velocity on the order of a few cm/µs, 3 orders of magnitude higher than ions.

Gas detectors can be operated in several regimes, given by the electric field at the readout electrode. High electric field strengths result in a strong acceleration of ions or electrons resulting in secondary ionization processes. This can create avalanches of charges around the readout electrodes, providing a huge gain of the signal charge allowing single photon resolution in the readout electronics. Proportional counters are gas detectors with an output proportional to the energy deposited in the detector volume, while a higher acceleration voltage gives the same signal magnitude for each incident photon energy, making the device a photon counter.

A limiting factor for counting application is the significant dead time due to the quenching of the charge avalanche. A typical gas-filled detector with active quenching shows a dead time of several 100 ns, limiting the accurate count rate to some 10^5 counts per second.

In high energy physics, a large variety of gaseous detectors have been manufactured and operated. For each application, custom-tailored detectors can be made, with optimizations regarding electric field geometry and strength, gas mixture, readout electrode pitch and mechanical geometry. Multi-wire projection chambers are a common type for track reconstruction due to their 2-dimensional array of readout electrodes, for the development of which a nobel prize has been dedicated in 1992. Through the use of the signal's timing information, time projection chambers also yield 3-dimensional information about the particle track.

3.2.2 Scintillators

The molecules of a scintillating material emit visible light after being excited by radiation. Scintillators are grouped in organic and inorganic scintillators. Organic scintillators are usually made of plastic, although crystals and organic liquids are also in use. In general, fast response and decay times in the ns-range and high light output are advantages of organic scintillators, making them very useful for timing measurements or trigger devices. Plastic scintillators can typically be handled and shaped without difficulty.

Inorganic crystals like the very common NaI(Tl) are typically slightly slower than organic materials with response and decay times starting in the 10 ns-range, but have a higher density and thus a higher stopping power for high energy photons or particles. Crystals like the NaI(Tl) or the newer product LYSO can also be cut into arrays of small sections giving spatial information about incoming light. This is exploited nowadays in medical applications like gamma-ray detection in PET scanners or in security applications.

Visible photons emitted by the scintillators need to be amplified and converted to an electrical signal by a photomultiplier tube. Inside the PMTs, the photons hit a cathode ejecting photoelectrons. An electric field accelerates the photoelectrons to following electrodes called dynodes, where, again, a larger number of electrons is ejected. Through a series of dynodes with properly generated high voltages between them a huge amplification of up to 10^8 can be achieved.

3.2.3 Semiconductor detectors

The development of semiconductor detectors was made possible by the technological advances in the microelectronics industry. Starting with silicon strip detectors in high energy physics experiments in the 1970s, this detector type is nowadays found not only in scientific applications, but also in consumer products due to its low price and compact sizes.

Apart from the possible compact dimensions, superior energy resolution is possible. As mentioned before, the energy resolution is limited by the number of charge carriers generated by the

incident radiation. In semiconductors, incident photons liberate an electron from its bound state in one of the crystal atoms or bonds. The energy needed to do so is given by the gap between the energy bands for the electrons, established by the periodic lattice of the material. In the band model, liberating an electron from an atom means lifting the electron from the lower energy *valence band* to the higher energy *conduction band*. Electrons in the conduction band are free to move throughout the lattice and contribute to the electrical conductivity. Conversely, the hole as a positive charge carrier can move as well.

A semiconductor at 0 K has a full valence band and an empty conduction band, just like an insulator. The energy spread between the two bands, called *bandgap*, makes the difference: Semiconductors have a bandgap in the eV-range, resulting in thermal excitation being sufficient to populate the conduction band. Silicon as the most prominent example due to its relatively low cost and wide use in many applications has a bandgap of 1.12 eV.

However, the energy needed to create an electron-hole pair $w_{e,h}$ is somewhat higher than just the bandgap, as some energy is deposited in the crystal as lattice vibrations. In silicon, for example, an average energy of 3.6 eV is needed.

Semiconductor	Average Z	Density [g/cm^3]	Bandgap [eV]	$w_{e,h}$ [eV]
Silicon	14	2.3	1.12	3.6
Germanium	32	5.3	0.67	2.96
Gallium arsenide	32	5.4	1.43	4.35
Cadmium telluride	50	6.1	1.44	4.43
Cadmium zinc telluride	49.1	5.8	≈ 1.6[1]	4.6

Table 3.1: Properties of commonly used semiconductor materials. Other materials than silicon might be favourable for some applications, as materials with higher Z (increased absorption) or higher number of charge carriers per photon are available.

A selection of semiconductor materials often used in sensor applications has been summarized in table 3.1. Silicon has several properties that make it attractive for sensors: First, its relatively low density and low radiation length X_0[2] make it a viable tool for particle physics with its typical low material budget requirement. However, its low density and low atomic number is a disadvantage for X-ray detectors, since the cross-section for the photoelectric effect is rather low ($\sigma_{photo} \propto Z^4$). The technological advances for silicon have been impressive, large silicon crystals can be grown with low impurity density (detector grade silicon has a typical impurity concentration of 10^{12} cm^{-3}), resulting in large charge carrier lifetimes in the order of 100 µs. Last, doping of both donors and acceptors using atoms of the 3rd or 5th group is possible.

Different requirements can make other materials more attractive. Germanium and gallium arsenide have a smaller $w_{e,h}$ than silicon, resulting in a superior energy resolution. Ge must be cooled however to low temperatures to reduce thermally generated leakage curent. GaAs and CdTe/CdZnTe are attractive for X-ray detectors because of their high photoabsorption cross-section for energies below 50 keV.

In practice, the charge carriers generated by incident radiation are separated in an external electric field applied to the semiconductor. In the presence of an electric field **E**, charge carriers are

[1] The bandgap of CdZnTe is depending on the exact composition.

[2] The radiation length of a material is the mean length to reduce the energy of an electron by the factor 1/e.

accelerated in between random collisions with the lattice. The average drift velocity for electrons and holes can be expressed similarly as for gaseous detectors as

$$\mathbf{v}_n = -\frac{q\tau_c}{m_n}\mathbf{E} = -\mu_n\mathbf{E} \tag{3.6a}$$

$$\mathbf{v}_p = -\frac{q\tau_c}{m_p}\mathbf{E} = -\mu_p\mathbf{E} \tag{3.6b}$$

where the electron and hole mobility, μ_n and μ_p, has been defined. τ_c is the mean free time between collisions and m_{np} the effective electron or hole mass. At room temperature, silicon shows an electron mobility of $\mu_n = 1450\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ and a much lower mobility of holes of $\mu_p = 450\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$.

The electric field, and therefore the bias voltage, is in general chosen to be as high as possible to increase the drift velocity and thus minimize the time needed to reach the readout electronics. This reduces the probability of charges being trapped as well as the dimensions of the charge cloud due to diffusion. Increasing the bias current also increases the leakage current in the sensor material. Leakage current comes from free electrons in the valence band or in energy levels of impurities or defects, being thermally excited into the conduction band. The intrinsic, i.e. undoped and unbiased free charge carrier concentration is given by

$$n_i^2 = N_C N_V \exp(-\frac{E_C - E_V}{k_B T}) = N_C N_V \exp(-\frac{E_g}{k_B T}) \tag{3.7}$$

where N_C and N_V are the effective densities of states in the bands. Practically, the charge carrier concentration is expressed as the material resistivity

$$\rho = \frac{1}{e\mu n} \tag{3.8}$$

The doping technology has opened up new opportunities for detectors: While the geometrical layout possibilites of gaseous detectors, for example, are very limited, sophisticated field configurations in the sensor volume can be produced by doping the semiconductor appropriately. In addition, signal charge movement is not obstructed by the doping itself. Different doping profiles and detector sizes and widths allow for application-specific detector design, matching the need for specific compactness, radiation hardness or quantum efficiency, for example. A few common subtypes are presented.

Reverse-biased diode

The fundamental semiconductor sensor structure is a p-n-junction with a region depleted of mobile charges, depicted in figure 3.2 (left). Electron-hole pairs created in the depletion region will be separated by the electric field and can be detected as a current at the electrodes.

The depletion region can be shaped by the doping profile and the externally applied bias voltage. A reverse biasing of the diode will increase the depletion region and the field strength within, increasing the volume sensitive to photons and decreasing the drift time to the electrodes.

Sensor-internal amplification of the charge generated by the incident photons has been realized in the *Avalanche Photodiode* (APD) by a special doping profile (figure 3.2 right). After drifting through the depletion region, the electrons are accelerated in an area with high field strength. Here, the electrons receive enough energy to generate secondary electron-hole pairs and thus multiply the charge in the sensor. The typical doping profile of a Si-APD is p^+-i-p-n^+, where the last p-n^+-junction serves as the multiplication region, typically being operated at a reverse bias above 100 V.

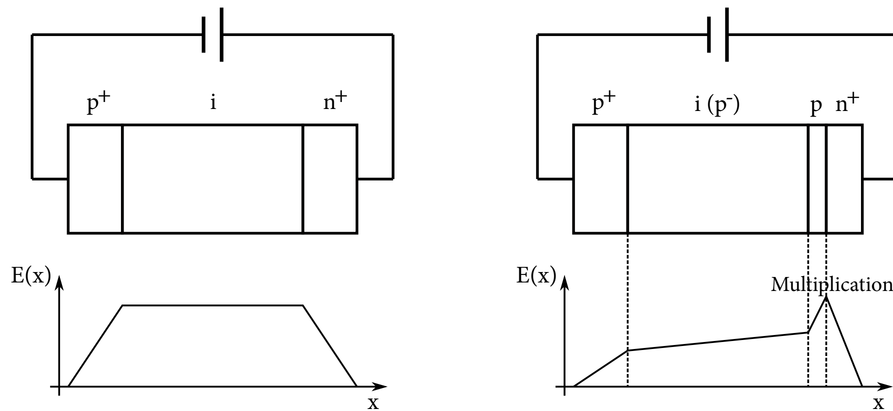

Figure 3.2: Cross-sections of a simple reverse-biased diode (left) and avalanche photodiode (right). Photons absorbed in the depleted region will generate an electron-hole pair that is separated by the electric field. In the APD case, the high electric field in the multiplication region (bottom part) results in secondary electrons.

Multiplication factors of several 100 have been realized with fast response times in the ps-regime, making APDs an excellent tool for timing measurements and photon counting purposes. Special care has to be taken, since these devices are operated close to breakdown voltage, making a stable cooling and biasing a necessity. APD arrays on a common silicon substrate have been developed and named *silicon photomultiplier* or SiPM, greatly expanding the photon counting rates on a very small area.

Position-sensitive semiconductor detectors

A large variety of position sensing semiconductor detector types have been developed based on VLSI technology mainly for applications in nuclear physics or particle physics tracking systems. Position information can be provided by segmenting the sensor electrodes. The signal magnitude per segment then depends on the position of the electrode relative to the location of the charge formation.

Starting from the fundamental diode structure, a strip detector can be obtained by dividing one of the contacts into thin parallel stripes. Each strip forms a pn-junction with the backplane. While photons generate a cloud of electron-hole pairs in a small volume of the sensor, charged high-energy particles generate charges along its track, which can be exploited: Angled tracks may introduce a signal on more than one segment, increasing the position information above the limit of the electrode pitch. However, as the division of the charge over several strips reduces the signal for each node, the signal to noise ratio must be considered. Typically, strip pitches of 25 to 100 μm are used in colliding-beam experiments, with strip lengths in the cm-regime up to 30 cm.

Two-dimensional information can be gathered by simply segmenting the backplane as well, obtaining double-sided strip detectors. These devices generate, for each hit, an x- and y-coordinate. This is problematic for high hit rates: n tracks generate n^2 hits, of which $n^2 - n$ are fake. The problem can be reduced by using a small angle between the strips rather than 90°: A hit in one strip can form fake combinations with all transversal strips overlapping it. A smaller angle between the strips reduces the number of overlapping strips.

True two dimensional information can be obtained by segmenting one of the electrodes in a matrix of electrodes or pixels with a common back contact. The straight-forward implementation of an electronic readout involves coupling a readout chip to the sensor through a matrix of solder bumps, connecting each sensor pixel to a readout channel. In this *hybrid detector* concept, additional area is needed for interconnection of the assembly to peripheral electronics, while the pixel area is typically limited by the area needed by the readout electronics.

Several approaches to monolithic pixel detectors have been implemented, integrating the sensing element and the readout electronics on the same substrate. A first approach to a large scale pixel array is the *Charge Coupled Device* (CCD), where each sensor pixel collects signal charge in a potential minimum below an electrode. In order to read the amount of charge in each pixel, the charges are transferred from bucket to bucket to the edge of the sensor by applying an appropriate sequence of voltages. At the edge, an amplifier reads the signal charges arriving from the matrix. The biggest drawback of this approach is the sequential reading which limits the detector speed.

The *Semiconductor Drift Chamber*, invented by Gatti and Rehak [28], removes the need for discrete readout steps. The potential in the device is shaped such that signal charge accumulates in the center and then drifts to the readout electrode. The position can be reconstructed from the time needed for the drift. More details will be given in the context of the DSSC camera in section 4.1.1.

The *active pixel Sensor* (APS) already contains a first amplifying stage and is usually fabricated using a standard IC process, but using a high-quality, high-resistivity epitaxial layer grown on a standard Czochralski substrate. Standard IC processes typically use much higher doping levels than used for sensor production. The doping levels for APS are still high and are limiting the depletion width of the pixel diode to a small layer of several μm. For visible light detection, the pixel is divided into a sensor part and an electronics part, where the light can not penetrate into the sensitive epitaxial layer. The electronics usually includes three transistors for resetting the cell, buffering and for selection for readout. The development for visible light applications has been driven mainly by consumer electronics in the past years with significant advances in terms of pixel size, fill factor and noise.

A special kind of active pixel sensor, the *DEPFET* (DEpleted P-channel Field-Effect Transistor), is based on a fully depleted silicon substrate with a field-effect transistor embedded on the surface. The depleted bulk forms the radiation-sensitive area. The electrons are forced by an electric field to drift towards an n-doped area below the FET channel called internal gate. There, they modulate the current flowing in the FET by inducing mirror charges in the channel. An in-depth description of the DEPFET is given in the DSSC context in section 4.1.2.

3.3 Noise sources in semiconductor detector systems

Several types of noise sources can be distinguished in a typical detector readout system.

Thermal noise is caused by the thermally excited vibration of charge carriers. In a semiconductor, the movement of the electrons in the conduction band is mainly influenced by electric fields and carrier density gradients. However, the random Brownian motion caused by their thermal energy is also present. For a resistor or a transistor at a V_{ds} of 0 V, this results in a power spectral density of the thermal current noise given by

$$\bar{i}_n^2 = \frac{4k_B T}{R} \tag{3.9}$$

which is not frequency-dependent (*white noise*).

For a transistor in saturation, the current noise is affected by the transconductance $g_m = \frac{\partial I_{ds}}{\partial U_{gs}}$:

$$\bar{i}_n^2 = 4k_B T \gamma g_m \tag{3.10}$$

where γ is a complex function of the transistor geometry and bias conditions. By referring it to the gate of the transistor, the power spectral density of the voltage source can be written as:

$$\bar{v}_n^2 = \frac{4k_B T \gamma}{g_m} \tag{3.11}$$

The given equations show that g_m should be maximized to reduce the noise for an amplifying transistor, while g_m should be reduced for a low-noise current source.

The physical theories for low-frequency noise or *1/f noise* are numerous. In transistors, this can be modeled as random trapping and detrapping of carriers in the channel and in the gate oxide (McWhorther's model) or as a fluctuation of the charge carrier mobility (Hooges' model). For MOSFETs, this is related to the interface between the channel and the SiO_2 gate dielectric, where the lattice structure abruptly changes. Here, unsaturated bonds of silicon atoms give rise to possible trapping of passing charge carriers in the transistor channel, resulting in variations of the channel conductivity. The trapped charge can be reemitted due to its thermal energy with a probability given by the temperature, the electric field condition, and the energy level of the trap. In summary, 1/f noise can be modeled as a voltage noise in series with the gate:

$$\bar{v}_n^2 = \frac{K}{C_{ox} W L} \frac{1}{f^\alpha} \tag{3.12}$$

where K is a characteristic process dependent constant, and the exponent α is usually ≈ 1. The transistor geometry affects the 1/f noise as well through the gate insulator capacitance C_{ox}.

Shot noise occurs whenever charge carriers are injected into a sensor volume independently of one another. Thermal generation of electron-hole pairs in the depleted sensor volume is an example, leading to a leakage current. Its spectral noise density is also white:

$$\bar{i}_n^2 = 2qI \tag{3.13}$$

where q is the carrier's charge and I is the average current. Shot noise mainly plays a role for large volume detectors or slow readout, where the average leakage current is high. Cooling of these detectors is often used to reduce the leakage current.

3.4 Signal processing

In order to reduce the noise of semiconductor detector systems, it is important to understand the basics of the noise sources in the readout electronics. In general, the sensor readout can be modeled as shown in figure 3.3. The charge generated in the sensor is modeled as a delta current pulse. The input capacitance C_{in}, on which the signal charge is integrated resulting in a voltage step, is comprised of the sensor capacitance itself, the input capacitance of the amplifier, and any other stray capacitance of the input node.

Noise sources are modeled as voltage sources for thermal and 1/f noise, or as a parallel current source, modeling the leakage current shot noise. Examples for physical sources have been given in the last section with spectral densities. Finally, the circuit contains a noiseless preamplifier and a shaping circuit (filter). The filter should be designed to suppress the noise bandwidth and to increase the signal over noise ratio.

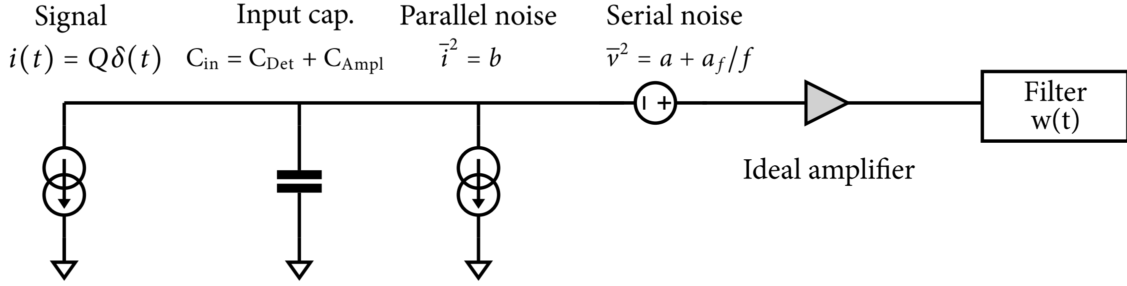

Figure 3.3: Equivalent circuit with noise sources for a typical detector front-end circuit.

While the model circuit comprises voltage or current sources, radiation detectors are actually used to measure charge. The noise level is therefore conveniently expressed as an equivalent noise charge, or ENC. The ENC is defined such that it is equal to the detector signal resulting in a signal-to-noise ratio of one. It is usually expressed as the corresponding number of electrons, or the equivalent deposited energy in eV.

In theory, one distinguishes two different types of shapers, time-invariant and time-variant ones. In a time-invariant shaper, the system response is independent of the arrival time of an input signal. It is conveniently expressed by its impulse response $h(t)$, which is also readily measurable, or its frequency domain equivalent, obtainable through Fourier transformation, $H(j\omega)$. A simple example of a time-invariant system that is often used for reference is the CR-RC-shaper.

On the other hand, the response of a time-variant shaper changes with respect to the signal arrival time, for example in a system that is only sensitive during a selected time interval, or gated system. These are typically modeled through their weighting function $w(t)$, weighting a signal in dependence of the arrival time, or in the frequency domain.

In general, the total noise depends on the bandwidth of the system. Consider a voltage amplifier with the frequency dependent gain $A(f)$, then the total noise is calculated by an integration over the noise power:

$$\bar{v}_n^2 = \int_0^\infty e_n^2 A^2(f)\,\mathrm{d}f \tag{3.14}$$

The noise for this model circuit can be calculated by the well known formula ([29], [30])

$$ENC^2 = \frac{a}{\tau} C_{in}^2 A_1 + 2\pi a_f C_{in}^2 A_2 + b\tau A_3 \tag{3.15}$$

where C_{in} is the detector capacitance, and A_1, A_2, A_3 are the so-called shaping coefficients weighting the white series noise, series 1/f noise and white parallel noise. τ is the characteristic time constant of the selected shaper. a, a_f and b are the power spectral densities modeling the series white, series 1/f and parallel white noise sources in the system.

For calculations in the frequency domain, instead of the impulse response $h(t)$, its Fourier transform, the transfer function $H(j\omega)$ is used. By setting $x = \omega\tau$, we can express the shaping coefficients

in the frequency domain as:

$$A_1 = \frac{1}{2\pi}\int_{-\infty}^{\infty} x^2 \frac{|H(x)|^2}{\tau^2}\,\mathrm{d}x \tag{3.16a}$$

$$A_2 = \frac{1}{2\pi}\int_{-\infty}^{\infty} |x| \frac{|H(x)|^2}{\tau^2}\,\mathrm{d}x \tag{3.16b}$$

$$A_3 = \frac{1}{2\pi}\int_{-\infty}^{\infty} \frac{|H(x)|^2}{\tau^2}\,\mathrm{d}x \tag{3.16c}$$

The analysis of 1/f noise in the time domain is mathematically challenging and not intuitive, but has been treated in the important and well known paper by Pullia [31]. We can finally express the shaping coefficients in the time domain as

$$A_1 = \int_{-\infty}^{\infty} (w'(y))^2 \mathrm{d}y \tag{3.17a}$$

$$A_2 = \int_{-\infty}^{\infty} (w^{\frac{1}{2}}(t))^2 \mathrm{d}t \tag{3.17b}$$

$$A_3 = \int_{-\infty}^{\infty} (w(y))^2 \mathrm{d}y \tag{3.17c}$$

where $w(t)$ is the shaper's weighting function and $y = t/\tau$ is the time normalized to the characteristic shaping time. $w^{\frac{1}{2}}$ is the derivative of order $\frac{1}{2}$.

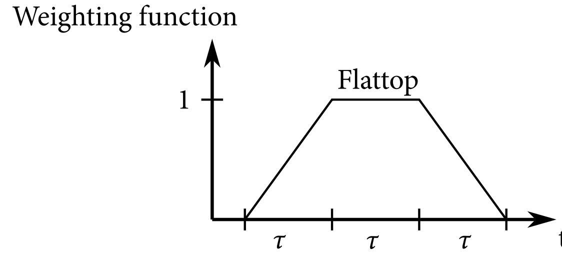

Figure 3.4: The trapezoidal weighting function expects the signal arrival during the flattop. The flattop increases the noise coefficients for 1/f and leakage noise, but is needed due to the finite rise time of the signal in the sensor.

At the foreseen readout speed of the DSSC instrument, the white noise is dominant. The optimum filter with the given time limitation is the trapezoidal shaper [30], whose weighting function is sketched in figure 3.4. The trapezoidal shaper is the optimum filter for 1/f noise in case of a limited time for shaping. Lower noise coefficients could in principle be achieved by removing the flattop yielding a triangular weighting function, at the expense of a reduced signal due to the finite signal arrival and settling time in the sensor.

For the trapezoidal filtering scheme, the dependence of the shaping coefficients on the flattop can be calculated to [32]

$$A_1 = 2 \tag{3.18a}$$

$$A_2 = \frac{1}{\pi}[(y+2)^2 \ln(y+2) + y^2 \ln y - 2(y+1)^2 \ln(y+1)] \tag{3.18b}$$

$$A_3 = y + \frac{2}{3} \tag{3.18c}$$

where y is the flattop length in units of τ. A_2, the shaping coefficient for the 1/f noise, is depicted in figure 3.5. Note that for the DSSC case at 4.5 MHz, a flattop of about $\approx 1\tau$ is foreseen, resulting in the following coefficients

$$A_1 = 2 \tag{3.19a}$$
$$A_2 = 1.38 \tag{3.19b}$$
$$A_3 = 1.67 \tag{3.19c}$$

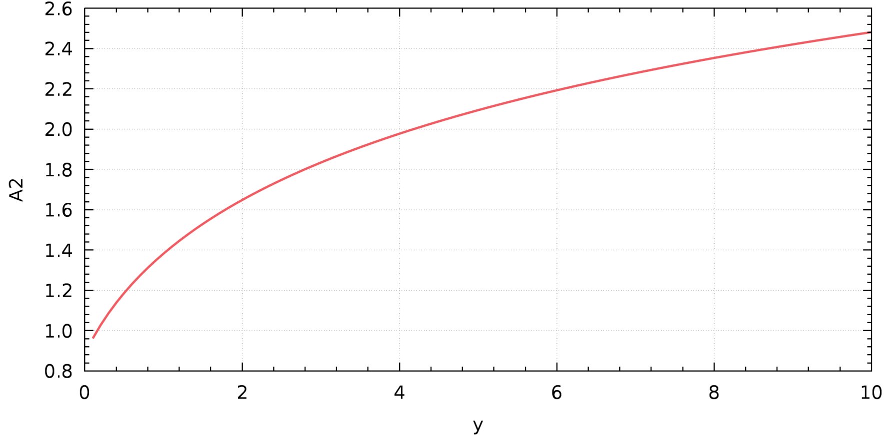

Figure 3.5: Plot of A_2 coefficient for the trapezoidal shaper as a function of the flattop, given in units of the shaper time constant τ.

The above expressions show that series white noise (3.17a) contribution can be minimized by increasing the shaper's time constant, which also reduces the derivative of the weighting function. However, parallel white noise (3.17c) can be optimized by reducing the integral of the weighting function, or, in other words, short shaping times. The 1/f noise (3.18b) is not affected by the shaping time, thus giving a constant contribution. 1/f noise has to be reduced by a proper choice of the shaper.

Theoretically, the optimum weighting function would be the triangle. However, the triangular shaping function expects the signal to be deposited during the infinitely small peaking. In practice, signal collection times in the sensor are finite, resulting in a loss of output signal amplitude for the triangular shaper. This problem is known as ballistic deficit, and has been studied for many shaper types. In general, a significant part of the signal amplitude is lost if the peaking time of the shaper is smaller than the charge collection time.

4
DSSC Detector

The DEPFET Sensor with Signal Compression, abbreviated DSSC, is one of three 2D detector development projects for use at the European XFEL. This chapter presents detailed aspects of the detector development, which have been published in [33], [34], [35] and [36].

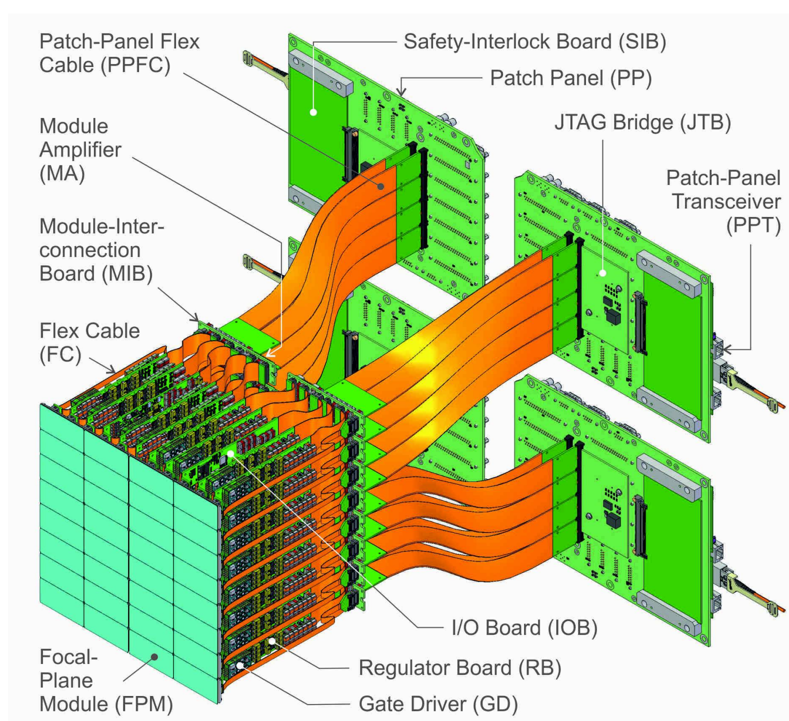

Figure 4.1: Overall design view of the detector electronics, which will cover an active area of 210 x 210 mm^2 [37].

The central requirements for the DSSC detector are single photon resolution for energies between 0.5 and 6 keV, a large dynamic range up to 10^4 photons and a maximum frame rate of 4.5 MHz. These simultaneous requirements go far beyond all existing instruments.

The central element of the DSSC system depicted in figure 4.1 is a hybrid pixel detector, based on the DEPFET active pixel sensor. Its low noise and amplification features allow for single photon resolution down to low photon energies. A novel type of DEPFET incorporates signal compression for large signals, allowing to increase the sensor's dynamic range. Each DEPFET pixel is bump-bonded to a channel in the readout ASIC, which allows for full parallel readout of the pixel matrix

to cope with the high frame rate. Each pixel in the readout ASIC incorporates an analog filter and an ADC for immediate digitization. The digitization in the focal plane allows for a large number of images to be stored in an in-pixel SRAM.

During the development of the project, the DEPFET production accumulated significant delays, triggering a search for a different sensor and accompanying readout circuits. This has led to a simpler and passive sensor type for the DSSC detector based on mini silicon drift detectors (MSDD). The MSDD however does not incorporate the low noise and signal compression features of the DEPFET.

The data stored in the in-pixel SRAM cells are sent out during the XFEL machine gaps. Digital control of the detector is achieved through a set of FPGAs on the I/O Boards and the Patch Panel Transceiver. The power for the readout ASICs is generated on the Regulator Boards.

The development of such a complex detector includes numerous complex work packages and research activities. These are spread between the current and former members of the consortium: DESY, European XFEL GmbH, Halbleiterlabor of the Max-Planck-Society, pnSensor GmbH, Politecnico di Milano and Universität Heidelberg.

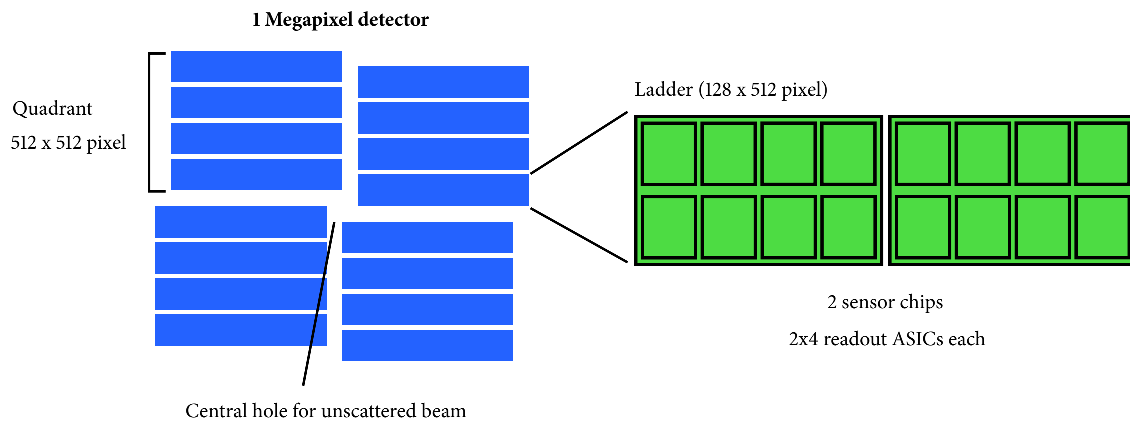

Figure 4.2: Hierarchy of the DSSC detector.

Figure 4.2 shows an overview of the individual detector units. The smallest usable unit is a ladder containing 128 x 512 sensor pixels. Each ladder contains the full focal plane electronics needed for operation. Each ladder is equipped with two large sensor chips (62 x 30 mm^2), each bump bonded to 8 readout ASICs. Using four ladders, a quadrant can be assembled. Four quadrants make up the complete 1024 x 1024 pixel detector. Note that the four quadrants can be moved with respect to each other to create a central hole with tunable size for the unscattered beam. The complete detector has an active area of approximately 210 x 210 mm^2.

The insensitive area of the present design will be about 15% [36] due to gaps between the individual sensor chips, the individual ladders and the four quadrants.

4.1 The sensor

To convert the incident photons to electrical signals, a fully depleted silicon sensor bulk will be used. The sensor thickness in the DSSC design is 450 μm, which is large enough to fully absorb photons

up to 6 keV. Only photons with a higher energy will not be absorbed with 100% probability and can thus reach the sensor backside or the readout ASIC. Radiation hardness is therefore given for photon energies lower than 6 keV.

The sensor is pixelated with a landing pad for a bump bond connection to the readout ASICs.

Two different variants of sensors have been developed and produced during the course of the project, which will be explained in the following sections.

The project was initially planned as a DEPFET-based system, utilizing the low noise properties of the DEPFET, expanded by an ingenious design change to vastly increase the dynamic range. However, the DEPFET fabrication has been delayed for various reasons. The DSSC consortium has therefore decided to pursue a second development in parallel, based on a passive mini Silicon Drift Detector (MSDD), with a shorter production time for the sensor. Both types of sensors are explained here in more detail.

4.1.1 Silicon Drift Detector

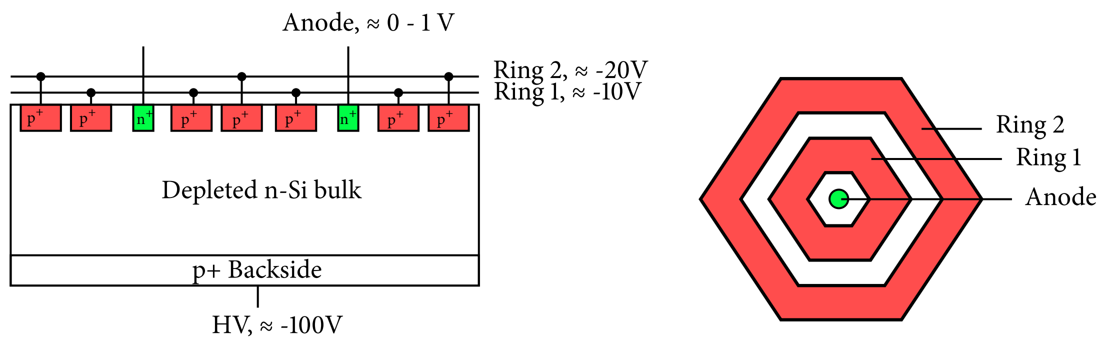

Figure 4.3: Cross-section (left) and top view (right) of the MSDD sensor. Signal electrons generated in the bulk of the sensor accumulate at the anodes.

During the project, an increased need for sensors with reduced production time became apparent. A simplified sensor has been produced based on the Silicon Drift Detector (SDD) concept [28].

The miniSDD sensors, sketched in figure 4.3, are based on a depleted n^- bulk with a passive collecting n^+ anode. The sensor volume is fully depleted by a sufficiently negative backside voltage.

A lateral field is added by p^+ ring implantations, biased at negative voltages with respect to the anode. Charge collection times well below 50 ns can be realized by a segmentation of the rings and adding a gradient between the outer and inner ring, directing the charges to the anodes. Sufficiently low ring voltages are capable of generating a large enough depletion zone to remove the high ohmic connection between individual pixels through the substrate. The depletion zone thus grows from the top side of the device, a mechanism called *sidewards depletion* [28]. Due to the lateral field which is generated by the ring voltages, the anodes can be very small with little capacitance. The ring regions further shield the pixels against each other, reducing the inter-pixel capacitance and thus pixel-to-pixel crosstalk.

As explained by equation 3.15, the input capacitance of the detector and front-end directly affects the noise performance of the system. Careful simulation of the anode pad and the bump connection lead to an expected C_{in} of 400 - 500 fF, mainly dominated by the interconnection. The bump

contribution could in principle be reduced by fabricating the ASIC with smaller bumps.

These entirely passive sensors result in a linear characteristic, i.e. the voltage step[1] on the pixel capacitance is proportional to the energy deposited in the sensor by photons. In order to reach a large dynamic range with this kind of sensor, a signal compression technique is needed in the read-out electronics. The benefit of these sensors is the fast production time, since only two implantation and two metallization steps are needed on the front side. These sensors allow to test our full system in advance and will be used at the first day of user operations at the EuXFEL - a large fraction of the foreseen experiments can be done with the reduced set of operation parameters.

4.1.2 DEPFET with non-linear amplification

The basic principle of a DEPleted Field Effect Transistor, abbreviated DEPFET, has been proposed in 1987 [38] and is illustrated in figure 4.4. The fully depleted high-resistivity n-type wafer is acting as the sensitive area. Depletion is achieved through sidewards depletion by reverse biasing the diode given by the p-doped back contact and the n-doped bulk.

On top of the substrate, a P-type field effect transistor (FET) is used as the first amplifier stage. A deep n^+ doping below the FET creates a potential minimum for electrons. Signal electrons created in the bulk drift towards the minimum and increase the conductivity in the channel by inducing mirror charges. Since the electrons in the minimum have an effect on the transistor current like the gate voltage on a typical FET, it is called *internal gate*.

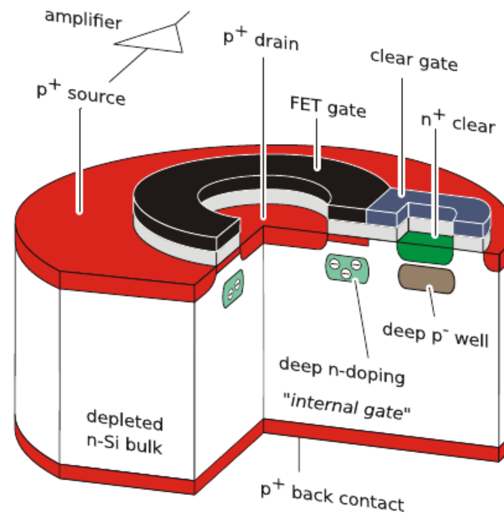

Figure 4.4: 3D illustration of a DEPFET. The deep n doping is a potential minimum for signal electrons. The second n-doped area, the clear contact, is shielded from the bulk by an additional p doping.

The change in current through the transistor dI_{ds} is related to the signal charge dQ_{sig} in the internal gate and defines the internal gate amplification g_q. According to the analytical model developed

[1]for an open loop electronics input

in [38], it can be calculated to

$$g_q = \frac{\mathrm{d}I_{ds}}{\mathrm{d}Q} = \sqrt{\frac{2\mu_p I_{ds}}{WL^3 C_{ox}}} \tag{4.1}$$

where μ_p is the mobility of the holes in the PMOS channel and W and L are the dimensions of the channel. It is evident that the internal amplification can be improved by increasing the drain current and, more strongly, by shrinking the gate length and width. Typical values for a DEPFET are on the order of 300 to 500 pA per electron.

The charge in the internal gate can be removed by applying a voltage pulse to the n^+ doped clear contact and a second MOS gate called clear gate. The clear contact is shielded from the sensitive area by a deep p implantation, in order to prevent signal electrons created in the bulk from drifting towards the clear contact rather than the internal gate. The internal gate, the clear and the clear gate form an n-channel transistor allowing the signal charges to be extracted from the internal gate.

For noise calculations, the capacitance of the internal gate is needed, however, direct measurement is not possible. The effective capacitance of the internal gate can be defined geometrically:

$$C_{eff} = \frac{WL}{\gamma} C_{ox} = \frac{C_G}{f} \tag{4.2}$$

where f is a parameter describing the influence of the internal gate relative to an influence of the gate itself. It approaches unity when the internal gate is very close to the channel and is smaller for larger distances. An indirect measurement of the effective capacitance becomes available when we refer the effect of a signal charge q_{sig} in the internal gate to a voltage ΔV_g applied to the external gate with the same effect. This results in the definition

$$C_{eff} = \frac{q_{sig}}{\Delta V_g} \tag{4.3}$$

and has been measured to 40 fF [39].

With this definition, the equivalent noise charge for a DEPFET can be calculated by

$$ENC^2 = a' A_1 \frac{1}{\tau} C_{eff}^2 + 2\pi a'_f A_2 C_{eff}^2 + b A_3 \tau \tag{4.4}$$

with the following constants for the individual noise spectral densities

$$a' = \frac{4}{3} \frac{k_B T}{g_m} \tag{4.5a}$$

$$a'_f = \frac{K_F}{WLC_{ox}^2 g_m} \tag{4.5b}$$

$$b = 2I_{leak} e \tag{4.5c}$$

for thermal noise, 1/f noise and shot noise, respectively. The coefficients A_1, A_2 and A_3 are defined by the shape of the filter's weighting function with the shaping time constant τ, which needs to be optimized according to the specific application case. It is evident that through the buried low-capacitance internal gate a low noise can be achieved.

The parameters a and a_f in equation 4.4 have been experimentally determined for DEPFETs in [39] with a drain current of 100 µA at 25 °C as $a = 1.53 \times 10^{-16}\,\mathrm{V^2\,Hz^{-1}}$ and $a_f = 4.5 \times 10^{-12}\,\mathrm{V^2}$. The capacitance of the internal gate has been estimated in [34] as $C_{in} = 60\,\mathrm{fF}$. The parameter b for the

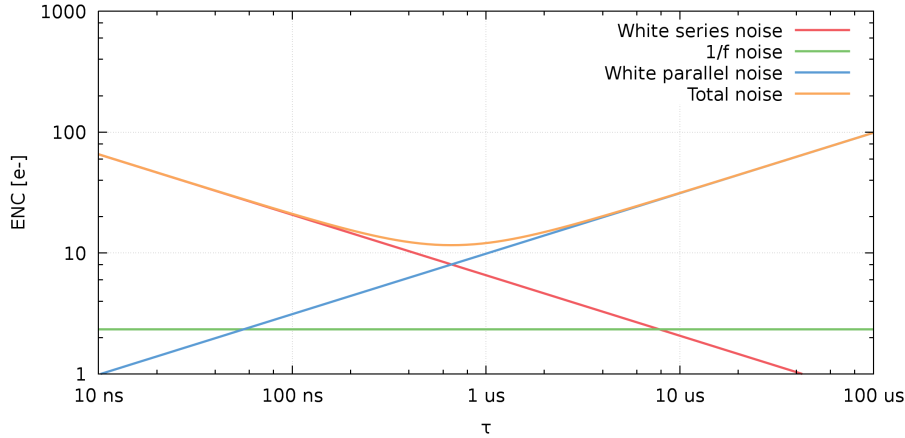

Figure 4.5: The equivalent noise charge for the DEPFET readout system (parameters given in the text) shows a minimum at a shaping time of about 800 ns for the chosen conditions.

parallel white noise can be estimated from the leakage current as $b = 2I_{leak}e$. The leakage current should be below 100 pA cm^{-2} at room temperature, resulting in $b \approx 1.5 \times 10^{-30}$ A^2 s for a DSSC-sized pixel.

The resulting ENC depending on the trapezoidal shaping time is plotted in figure 4.5. A minimum noise of about 10 e$^-$ is reachable with the DEPFET. Note that the noise numbers given here only include the DEPFET noise and no noise contributions from any readout circuit element. For shaping times larger than 800 ns, the leakage current contribution rises further and dominates. For the foreseen operation at 4.5 MHz, a DEPFET noise of 30 e$^-$ can be estimated. It should be noted that the plot is valid for room temperature only, as leakage is strongly depending on temperature as in $I_{leak} \propto T^{3/2}e^{-\frac{E_G}{k_B T}}$. With lower leakage devices and longer shaping times, lower noise values have been realized with DEPFETs.

It is worthwile to note that reading the DEPFET is non-destructive, i.e. the charge collected in the internal gate is not altered. Measurements can thus be repeated for lower noise or charge can be stored in the internal gate, limited only by leakage current in the sensor volume which can be reduced by lower temperature. Repetitive measurements require alternating measurements of the baseline current and the current with signal charge. This has been demonstrated in [40] by using two adjacent DEPFET structures, between which the signal charge can be moved back and forth.

The *DSSC-type DEPFET* [42] uses a slightly modified pixel structure, depicted in figure 4.6. Here, the internal gate is split in several regions underneath a large-area source. The potential minimum for electrons is still located directly below the FET channel. Small signal charges are still accumulated below the channel, while large charges are distributed between the regions below the channel and the source. Only the parts below the channel have an influence on the FET current.

The non-linear characteristic of the device (figure 4.6 right) shows a linear part up to 30 keV to 40 keV. Here, additional charges start to fill the first overflow region below the source. The other overflow regions are filled at 600 keV and 2.5 MeV, respectively. The typical g_q of a DSSC-type DEPFET is 500 pA/el to 600 pA/el for small signal charges.

The complete sensor matrix is composed of the individual pixels with hexagonal shape. The

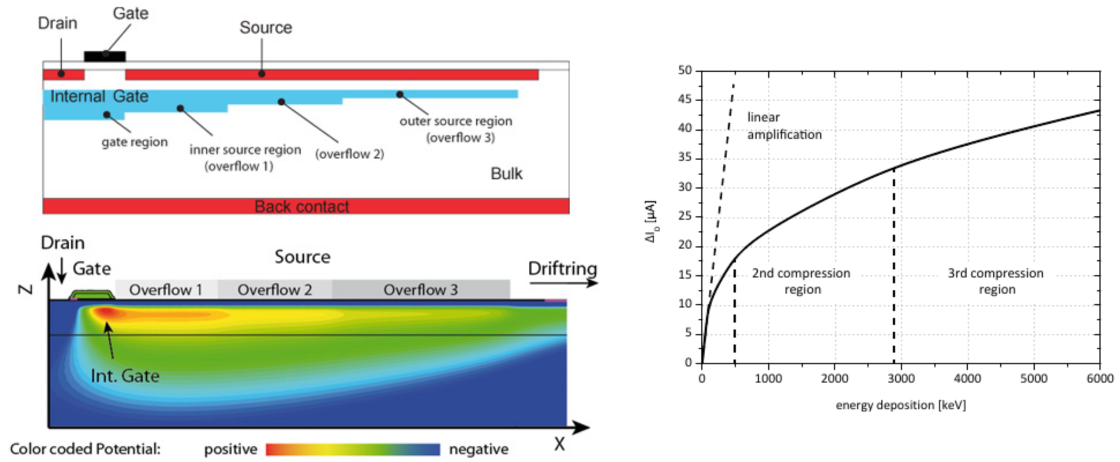

Figure 4.6: Left: Structure and potential in the non-linear DEPFET. Right: Simulated non-linear characteristic of the DSSC-type DEPFET [41].

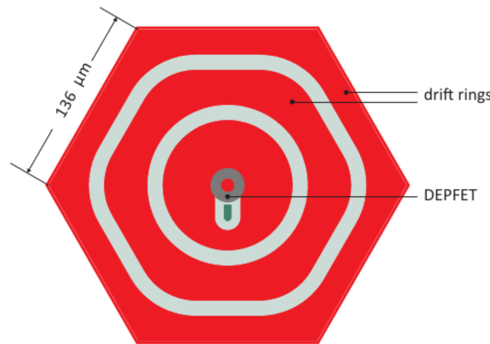

Figure 4.7: Simplified layout of a DEPFET pixel. The hexagonal structure creates a more homogeneous drift field compared to a rectangular pixel.

DEPFET itself is located in the center of the pixel (see figure 4.7). Charge electrons created in the sensor bulk are drifting to the pixel centers due to the static bias applied to the drift rings. The hexagonal pixel generates a more homogeneous drift area than square pixels, effectively reducing charge collection times. The DEPFET pixels have slightly larger pitch than the ASIC pixels, as the inevitable gaps between the ASICs are covered by sensor pixels as well. A redistribution layer from sensor pixels to ASIC bump bond landing pads is used on the sensor.

A sensor-internal charge injection possibility [43] has been studied in the scope of the DSSC project. Usually, the inner substrate contact, located between the two drift rings inside the pixel, is at a higher potential than the DEPFET source, effectively removing electrons generated at the device surface. By lowering the bias voltage electrons can be injected, which can spill over and reach the internal gate. This charge injection is planned to be used for system testing and calibration.

4.2 The Readout ASIC

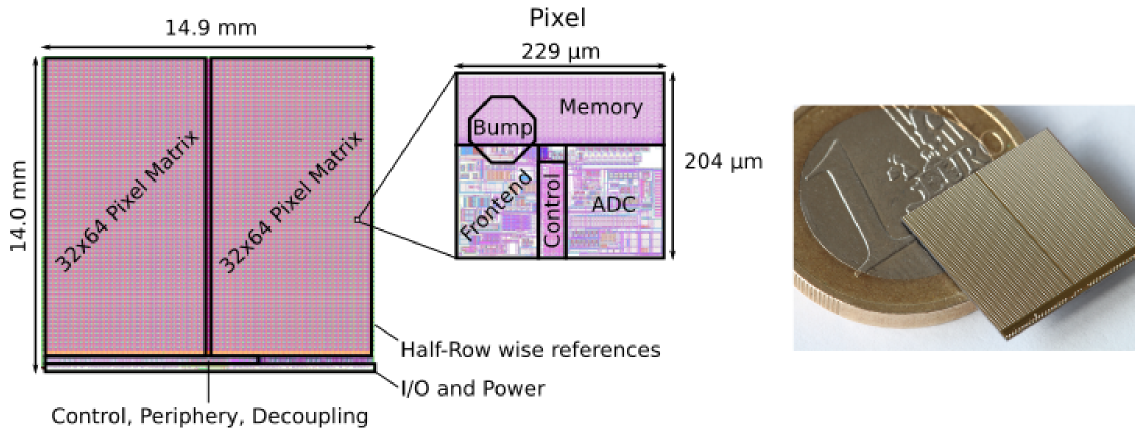

Figure 4.8: Left: The major part of the F1 readout ASIC floorplan is covered by the pixel matrix. Right: Photograph of an F1 readout ASIC, on a Euro coin for scale.

Extensive information about the ASIC design can be found in [44] and more detailed publications are linked in the following. In this section, the most relevant points are summarized, since the readout ASIC is the main tool used for this thesis. Furthermore, the author has been involved during the prototyping phase in simulation and characterization work on prototype pixel matrices, and during commissioning of the full format ASIC in characterization of the pixel matrix.

The F1 readout ASIC contains a 64 x 64 pixel matrix and periphery circuits necessary for the operation of the matrix. The total size of the chip is 14.9 x 14.0 mm^2, mostly occupied by the pixel matrix (14.670 x 13.056 mm^2). Each pixel has a size of 229 x 204 µm^2. The chip is manufactured in the IBM (now GlobalFoundries) 130 nm process, which offers C4 SnAgCu bumps for interconnection. Each pixel uses a bump for connection to a sensor pixel for full parallel readout, while power and control signals are delivered through bumps in the periphery. The IO and periphery circuits are completely located on one side of the ASIC in a 890 µm wide balcony, making the ASIC three-sides buttable. Figure 4.8 shows the F1 ASIC floorplan and photograph.

In order to reduce overall power consumption, a power-cycling scheme is employed for the readout ASIC. During the 99.4 ms long XFEL pause, power is shut off for all the analog parts and the ADCs, since they are only needed during the 600 µs burst period. The power for the digital configuration and control block and the in-pixel SRAM cells is constantly on.

A simplified schematic of the readout electronics for one pixel is shown in figure 4.9. Analog front-ends for both DEPFET and MSDD type sensors are included in each pixel, sharing the subsequent stages and selectable through switches. The signal current from the front-end is integrated on the feedback capacitor of the filter amplifier. A Wilkinson-type single slope ADC digitizes the filter output after the integration has finished by latching timestamps from a peripheral counter. In the ADC, the filter output voltage is stored on a sample and hold (S&H) capacitor and ramped up by a constant current source. A comparator sets the latch signal when the in-pixel reference voltage is reached. The delay of the latching is thus proportional to the magnitude of the input signal. The conversion result is then stored in the 800-cell in-pixel memory.

It is worthwile to note again that full parallel readout of the pixel matrix is used to achieve the

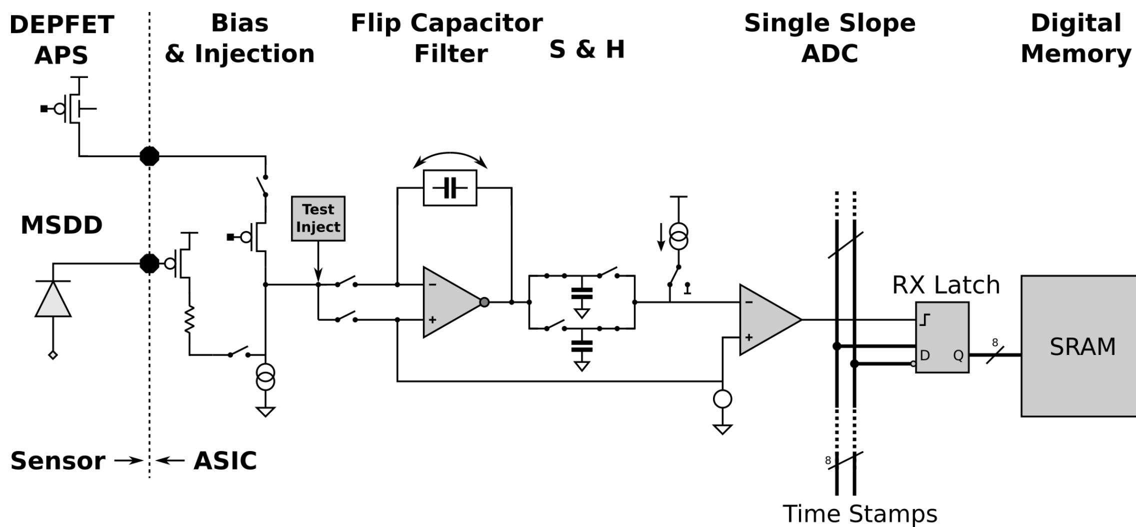

Figure 4.9: Simplified pixel schematic including the analog front-end for both sensor types, filtering stage, the pipelined ADC and the memory [44].

high frame rates of up to 4.5 MHz. Therefore, each ASIC pixel reads the sensor pixel simultaneously through the in-pixel front-end, pipelined ADC, and memory. The individual blocks in each pixel of the readout ASIC are described in more detail in the following sections.

4.2.1 Analog Front-End

Two sensors are supported by the analog front-end: A DEPFET-type sensor, where the ASIC input is connected to the DEPFET drain node sending a signal-dependent current, and an MSDD-type sensor, where the charge is collected at the input node. The pixel operation mode is controlled through switches programmable via slow-control.

DEPFET front-end and Flip Capacitor Filter

In the drain readout configuration employed here (figure 4.10), the source and gate voltages of the DEPFET are fixed by external circuitry. Any signal charge below the internal gate thus introduces a positive modulation of the current through the DEPFET. A cascode stage in the ASIC pixel is used to fix the DEPFET drain voltage. The cascode also ensures fast settling of the signal current by hiding any stray capacitance. The settling time of the system is then dominated by the charge collection time in the sensor volume.

The DEPFET bias current is sunk in a programmable current source, so the following analog filter only has to process the signal current from the DEPFET.

The Flip Capacitor Filter, published in [45] and [46], implements the trapezoidal weighting function, which minimizes the white series noise dominant at the foreseen frame rates of 4.5 MHz (section 3.4).

The circuit uses a new approach to implement correlated double sampling that uses only one operational amplifier to save space in the pixel. Figure 4.11 shows the needed dynamic control signal timings and a sample waveform of the filter output, which are generated by the on-chip digital

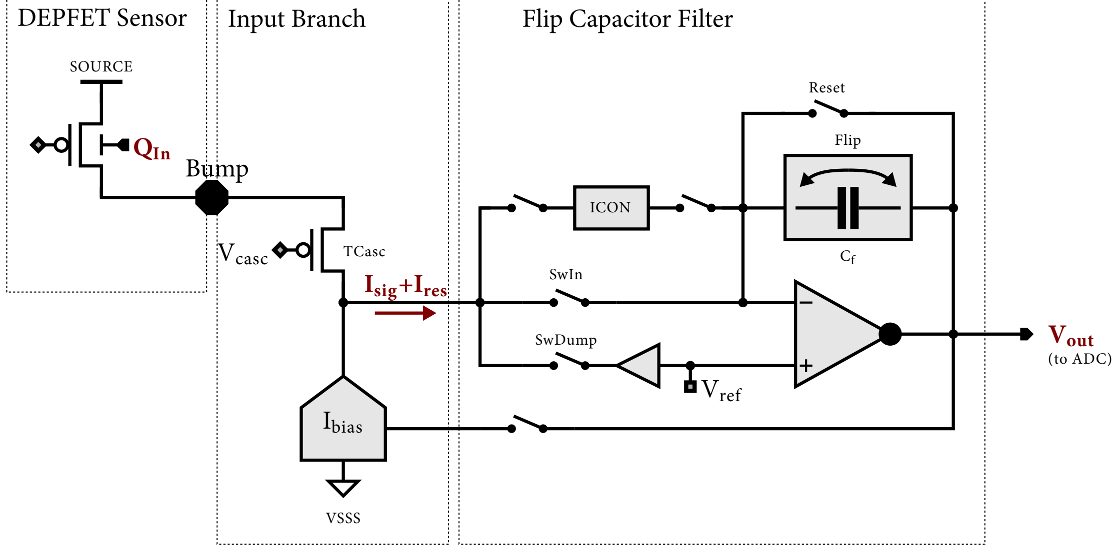

Figure 4.10: Simplified schematic of the DEPFET-type front-end and the flip capacitor filter. Through the bump, the DEPFET supplies a current composed of a bias part and a signal-dependent part. The bias current is subtracted by the current sink to VSSS [44].

control block. After resetting the filter initiated by the *DDYN_Reset* signal, the baseline measurement is conducted by integrating the input current on the feedback capacitor C_f, enabled through *DDYN_SwIn*. During the following flattop phase, the X-ray pulse is expected, depositing signal charge in the sensor pixel which is collected in the internal gate. The input current is sent to a dump node in this phase by *DDYN_SwDump*. Moreover, the feedback capacitor is flipped during the flattop by a set of switches controlled by *DDYN_Flip*. This inverts the polarity of the baseline measurement. In the last phase, both baseline and signal current are integrated on C_f. Since the first baseline measurement has been inverted, the baseline measurements cancel each other out, yielding only the signal current integration on C_f. After the second integration has ended, the ADC needs to start the conversion through *DDYN_Rmp*. Subsequently, the front-end is reset again in preparation of the next pulse, whereas the pipelined ADC digitizes the last pulse.

A critical point of this technique is the non-linearity of the filter. This has been studied in [47] and [48] for the linear amplification region of the DEPFET with a non-linearity error below 0.05 photons at 1 keV. Outside the sensor's linear region, the error increases, which is less critical and has to be evaluated in combination with the DSSC's non-linear response.

The resulting output voltage of the filter can be approximated by the equation

$$V_{out} = V_{ref} + \frac{1}{C_f} \int_0^{\tau_1} I \, \mathrm{d}t - \frac{1}{C_f} \int_{\tau_1 + t_{ft}}^{\tau_1 + t_{ft} + \tau_2} I \, \mathrm{d}t \qquad (4.6)$$

where V_{ref} is the reference voltage of the filter, τ_1 and τ_2 are the integration lengths, and t_{ft} is the flattop length. The offset current contribution will be cancelled if a trapezoidal weighting function is realized by setting $\tau_1 = \tau_2$.

Although the bias current compensation should result in a negligible residual current in the ideal case, it is worthwile to note the maximum residual bias current tolerable by the filter. The filter

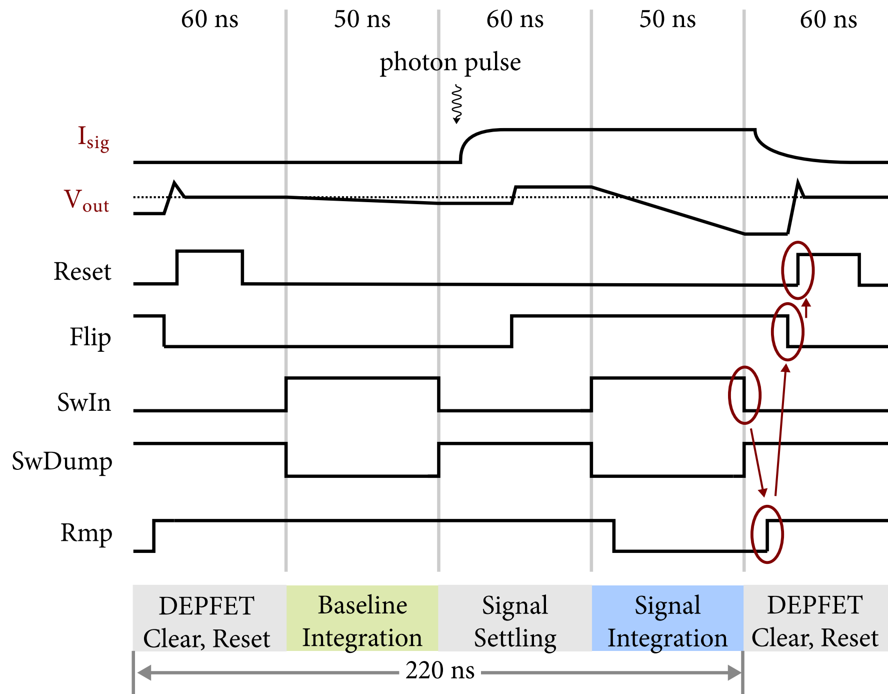

Figure 4.11: Timing of the dynamic control signals needed for the operation of the flip capacitor filter. Three control signals are necessary for the front-end (SwDump can be derived from SwIn by inverting), Rmp is the ADC control signal.

amplifier has an operating region of 0.2 - 1.0 V, leaving this region saturates the amplifier. The design value for the filter's reference voltage is 0.9 V, so a headroom of 100 mV above the reference is available. The bias current can deviate from the "ideal" value in both directions. Less bias current than expected can saturate the filter during the first integration, while an increase of the bias current leads to a smaller output voltage during the first integration, which can saturate the filter during the flip of the capacitor.

The maximum tolerable residual current, assumed as constant during the integration (ideal case) then calculates to

$$I_{bias,max} = \frac{\Delta U C_f}{t_{int}} \tag{4.7}$$

where ΔU is the headroom voltage, C_f is the feedback capacitance and t_{int} is the integration time. For 4.5 MHz operation with 50 ns integration time and 1.5 pF feedback capacitance (for the 1 keV photon energy case), this results in 3 µA tolerable current.

The ADC, introduced in the next section, is designed to digitize the full output range of the filter (0.2 - 1.0 V) with 8 bit resolution or 255 bins. The front-end gain has to be changed in order to fit the full response into the given voltage range. The front-end gain will be fixed by realizing the 1-to-1 relation between photons and ADC bins, resulting in a maximum signal current given by the resolution of N bits of the ADC:

$$I_{signal,max} = I_{LSB} 2^N \tag{4.8}$$

Table 4.1 summarizes the minimum and maximum signal currents for several photon energies expected at the European XFEL, as well as the feedback capacitance needed to attribute the first photon to the first ADC bin at nominal operation parameters. A variety of capacitors is needed due to the wide range of photon energies foreseen for the DSSC and has been realized in the F1 pixel. Fine-tuning of the operation parameters will be needed in order to adapt the system to deviations from the ideal values, which is realized in the ADC.

E_{ph} [keV]	min. signal [nA]	max. signal [μA]	C_f [pF]
0.5	69	18	0.89
1	139	36	1.78
3	417	107	5.3
6	833	213	10.67

Table 4.1: Parameters for the DEPFET front-end for a g_q of 500 pA/el, an integration time of 40 ns and an ADC bin size of 3.125 mV.

Table 4.1 states maximum signal current of 213 μA to be fed into the filter, which is almost the maximum design value of the filter (250 μA). Throughout the system development process, a need to increase the maximum input current became apparent, e.g. for use cases without the need for single photon resolution, but rather an increased dynamic range. This has been realized by an additional current boost in the filter's output branch, which increases the maximum signal to 330 μA. The branch can be enabled through the FCF_HDR slow-control bit.

A dedicated circuit to inject a variable test current has been published in [49] and implemented in each pixel. The circuit can also be used to create a charge pulse for the MSDD front-end, described in the next section.

A signal current is generated in the chip periphery by an 8 bit current DAC. Since supply and ground levels differ between periphery and each pixel, a voltage drop compensation has been implemented to mirror the current into the pixel. It is based on generating reference voltages for the current mirror that are distributed to the matrix without current load. In the pixel, an operation amplifier is needed to generate a low-impedance copy of one of the reference voltages.

The signal current can be pulsed through one of the dynamic control signals (*DDYN_Sw*), which sends the current either to a dump or to the filter input. In order to mimic a DEPFET signal current due to photons arriving in the flattop phase, the DDYN_Sw needs to be active during the second integration phase.

The current DAC and the mirrors can be operated in low gain mode, where the current from the periphery DAC is mirrored with a 10:1 ratio into the pixel yielding 0.01 - 2.55 μA. A high gain mode with mirror ratio 10:10 is available as well, thus yielding 0.1 - 25.5 μA of signal current. The circuit thus allows for a wide selection of a fraction of a 0.5 keV photon up to the equivalent of several hundred photons. A dispersion on the order of 4% has been reached, at INL and DNL levels well below 0.5%.

The circuit moreover allows to generate a static current, switchable by a control bit in the pixel, similar to the bias current from a DEPFET. Here, a voltage drop compensation is neither provided nor needed, since the accuracy of the current is of no importance. A 5 bit current DAC for bias currents between 14 and 150 μA has been implemented.

MSDD front-end

The circuit published in [50] offers a simple way to read out the charge collected by the MSDD while offering signal compression and sharing the subsequent processing chain in the pixel. The front-end design was introduced late in the project after it became clear that the DEPFET sensor fabrication would accumulate significant delays. It is therefore optimized for integration with the already developed rest of the signal processing chain.

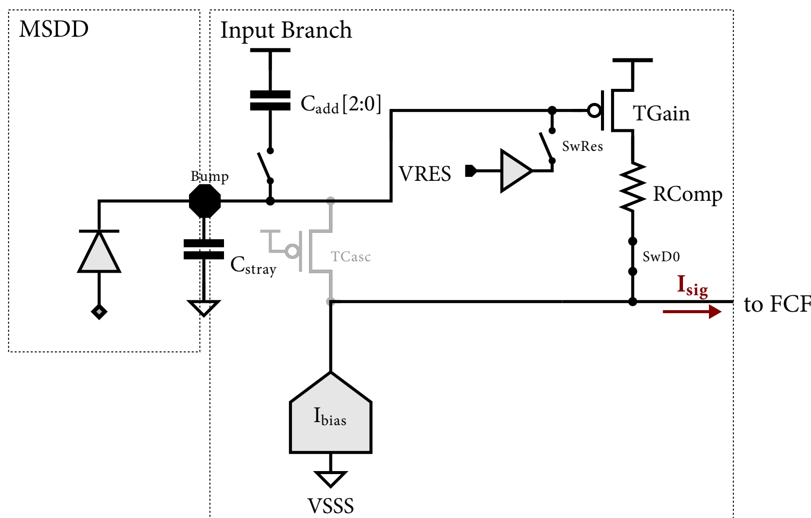

Figure 4.12: In charge readout mode, the input charge is converted to a current through transistor TGain. The gate is biased through a reset circuit and left floating otherwise, especially during charge collection [44].

It is based on the simple idea of converting the charge to a current using a single PMOS (TGain in figure 4.12). The charge is directly converted to a voltage on the total capacitance at the ASIC input. The PMOS delivers a current controlled by the detector output voltage at its gate, essentially replacing the DEPFET by a transistor in the ASIC. The current is fed into the filter's virtual ground node. The transistor is normally operated in saturation with a peak transconductance of 1 mS. To increase the dynamic range, the *triode compression* has been invented [50]. With increasing signal charge and thus increasing current, the drain-source voltage of the transistor is decreased by the voltage drop across the resistor RComp connected between the transistor drain and the filter. The decrease of V_{ds} and increase of V_{gs} move the transistor into the ohmic regime, where the transistor current still increases with V_{gs}, but with decreasing gain compared to the R = 0 case (red lines in figure 4.13).

The transistor has to be reset to the nominal bias point after each cycle, i.e. the gate voltage with maximum g_m. After the reset, the gate is left floating, waiting for signal charge to act on the input node.

The circuit implemented on F1 reaches a maximum g_m of 1 mS. Using the lower boundary design value of 300 fF, this calculates to a signal current of 148 nA for a photon of 1 keV energy, which is comparable to the DEPFET case.

As mentioned in the previous section, the current injection circuit can be used to generate a charge pulse at the input node. Here, the pulsed signal current is sent through a resistor, thus gen-

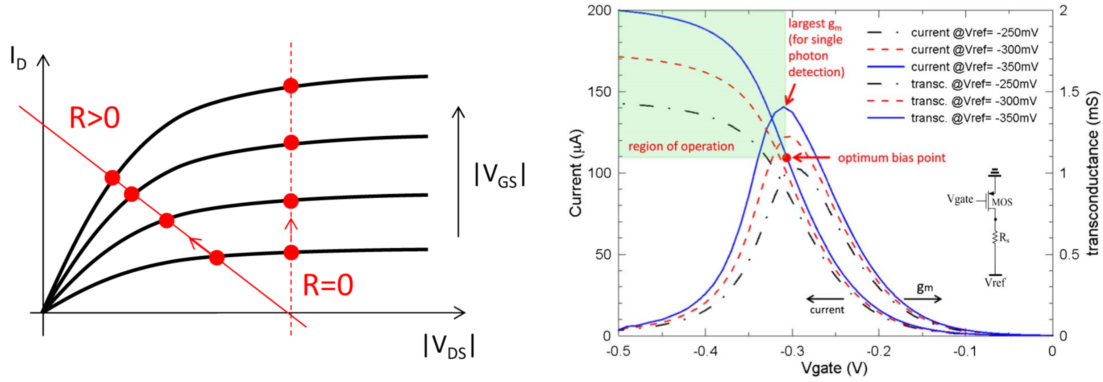

Figure 4.13: Triode compression mechanism [50]. The series resistor decreases the input transistor Vds for increasing signal current, thus decreasing the gain for high amounts of signal charge at the input.

erating a voltage pulse. Through capacitive coupling to the input node, charge is injected. The injected charge on the input node can be calculated by the equation for the capacitive divider, formed by the injection capacitance and the input capacitance:

$$Q_{inj} = \frac{C_{inj}C_{in}}{C_{inj} + C_{in}} R_{inj} I_{inj} \tag{4.9}$$

On the F1 ASIC, injection capacitors of 10 fF and 200 fF are available. Both signal current ranges of 0.01 - 2.55 μA (low gain) and 0.1 - 25.5 μA (high gain) are usable with the smaller capacitor, while the large injection capacitor is only usable with the higher capacitor, thus forming three ranges for signal charge injection.

Bias current subtraction

In both previously described front-end circuits, a bias current is flowing through the input transistor and eventually modulated by input charge. Sending the approx. 100 μA bias current to the filter would require huge capacitors, which are not realizable in this pixel architecture. The bias current is therefore subtracted by a current sink to a ground net.

The current sink architecture has been published in [45]. The implementation includes a coarse DAC configured through slow-control and a variable branch that is fine-tuned by an analog circuit to match the input bias current. Both coarse and fine branches are utilizing cascoded resistors. While the cascode gates in the coarse branches are fixed to VDD resp. VSS, the gate in the variable branch, called V_{Hold}, is used to fine-tune the subtracted bias current. V_{Hold} is programmed just before each XFEL burst in the IProg phase, lasting several 10 μs, and stored on a capacitor. In the IProg phase, a closed loop is formed using the filter amplifier. Any residual current flowing into the filter is integrated and thus increases the V_{Hold} voltage, resulting in a larger current subtraction of the variable branch. When the loop has settled only a small residual current flowing into the filter remains.

The resistors in the constant branches are binary scaled to provide a wide range of coarse settings with only four digital control bits (60 kΩ, 30 kΩ, 15 kΩ and 7.5 kΩ resistors are implemented).

This allows for a bias current between 0 µA and 240 µA to be subtracted. The coarse programming accounts for variations across the pixel matrix, and for tracking the variations of the bias current due to shifts in the threshold voltage, e.g. after irradiation damage in the DEPFET.

The programmable branch utilizes a 25 kΩ resistor, with storage of V_{Hold} on a 3.3 pF MIMcap. The MIMcap is necessary since leakage on this node would result in a changing offset current throughout the burst, up to a value that can saturate the filter. The variable branch yields roughly 38 µA or 2.5x coarse granularity.

The thermal noise is primarily caused by white noise of the resistors and given by

$$\bar{i}_n^2 = \frac{4 k_B T \Delta f}{R} \tag{4.10}$$

depending on the temperature and the bandwidth of the system. The thermal current noise has to be referred to the input for reference.

Earlier in the project, when the DEPFET gain was anticipated to be substantially lower, the noise contribution of the DAC was tried to be reduced by adding a negative supply voltage called *VSSS*. VSSS was supposed to be at a level of −3 V in order to increase the resistor sizes for lower noise.

4.2.2 ADC

Binning concept

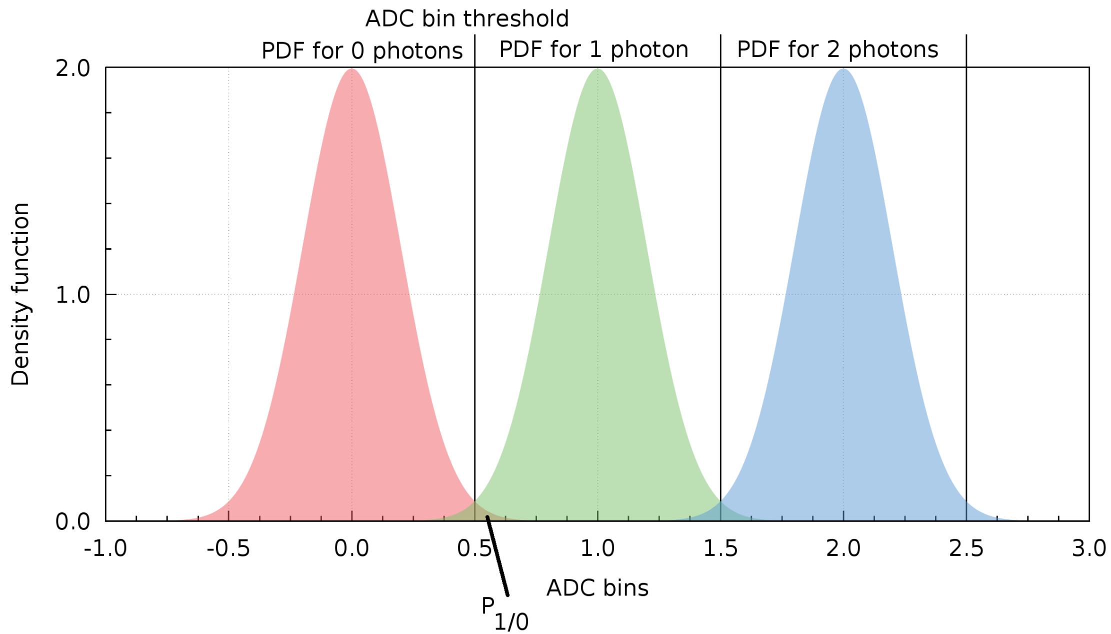

Figure 4.14: Binning philosophy for the first photons. The probability distribution function for each number of absorbed photons is centered in the ADC bin.

The ADC exploits the fact that incident photons are monochromatic. For the linear part of the sensor characteristic, i.e. for low numbers of absorbed photons, a 1:1 relation between photons and

bin number will be established, depicted in figure 4.14. The electronics noise is assumed Gaussian here, and the mean output for each photon centered in the ADC bin. $P_{1|0}$ describes the probability that a pixel erroneously identifies one photon although none has been absorbed, if the electronics noise is large enough as assumed here. $P_{1|0}$ can be computed as the integral of the density function for zero photons between 0.5 and 1.5 bins.

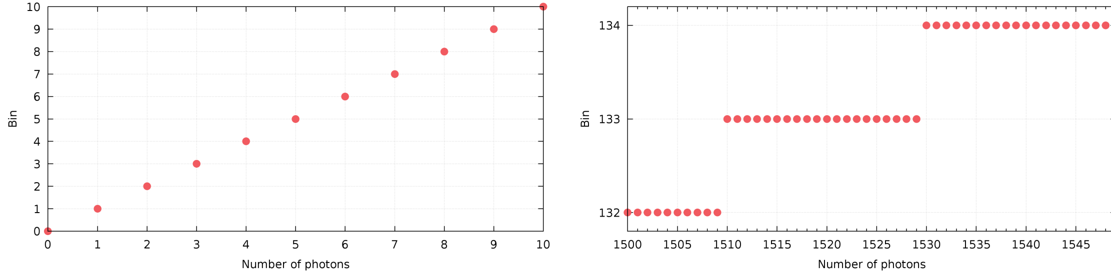

Figure 4.15: Assignment of photons to bins for linear (1:1 relation between photons and bins) and for compressed part.

Since the DEPFET or MSDD front-end characteristic is compressing the output signal for higher numbers of photons while the ADC response is linear, more and more photons will be assigned to each bin (figure 4.15). The noise of the system, for larger signals dominated by the quantization noise of the ADC, is expected to be smaller than the Poisson noise of the photon generation.

In order for the bin-wise photon counting to work, the front-end response and the ADC bin size have to match, so the filter output increase per photon has to be the same as the bin width. Therefore, precise control over the ADC bin size is mandatory. Moreover, pixel-to-pixel variations have to be equalized. Centering the first photon in the middle of the first ADC bin requires the offset to be adjusted precisely.

By increasing the number of bins attributed per photon to 2, for example, finer information about gain and offset dispersions become available, simplifying the pixel-wise calibration. In addition it would allow to detect split events, where signal charge is distributed among two pixels, while giving up a part of the dynamic range for a fixed number of ADC bins.

Implementation

The in-pixel ADC [51] uses a Wilkinson-type architecture, where the input voltage is translated into timing information using a capacitor and a constant current source. The constant current source charges the capacitor pre-loaded with the voltage to be measured, until a threshold voltage is reached. The time needed for the charging is measured by a counter (figure 4.16).

Two capacitors are implemented, in order to allow pipelining of front-end and ADC: While the filter is connected to one capacitor to store the result, the ADC is connected to the other one, converting the voltage to the timing information. In the next cycle, the connections are reversed. Matching between the two capacitors is essential to avoid different gains from cycle to cycle. The mismatch has been measured to be in the permil region and is thus negligible.

The current source can be fine-tuned by six control bits in order to equalize mismatch between the pixels and fine tune the bin size. The nominal ramp current of 4.5 μA with the design capacitance of 1.04 pF results in a maximum 184 ns conversion time for the dynamic range of the filter of

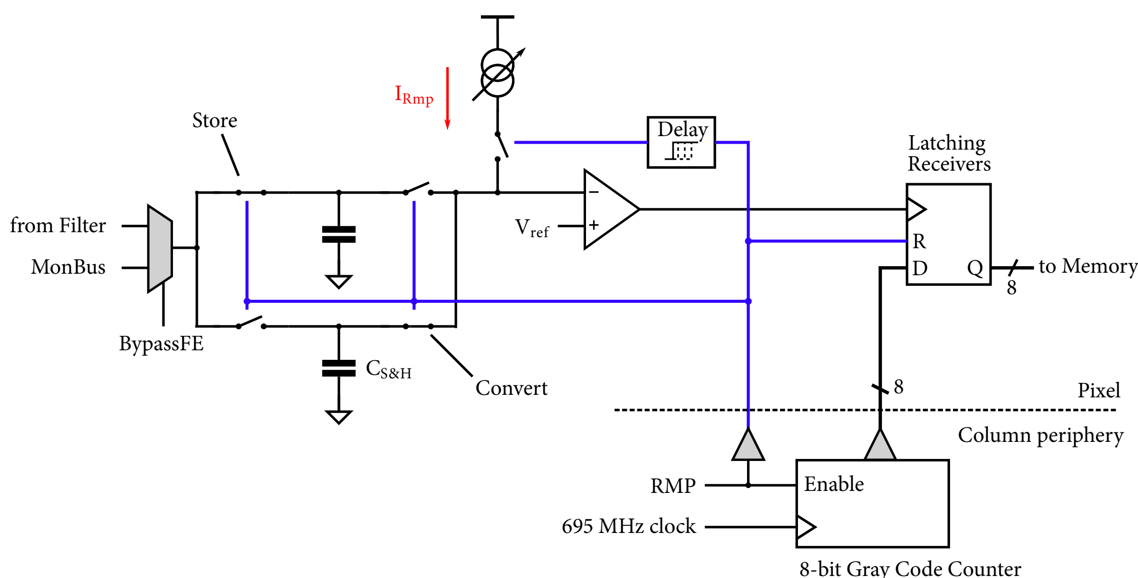

Figure 4.16: Simplified schematic of the pixel-internal ADC. The constant current source ramps up the input voltage stored on the capacitor until the threshold is reached, causing latching of the timestamp.

800 mV, well within the 220 ns limit of the XFEL pulse timing. With the clock speed of the counter of 1.4 GHz, 255 bins (8 bit resolution) are realized. The ramp current can be halved in order to provide a longer conversion time and thus up to 510 bins, if the system is not running at the full frame rate of 4.5 MHz. The last digital code, 511, is used as an error code, indicating that the comparator threshold was not reached in the given conversion time.

A delay line is used to move the pedestal within a bin to the center position. It features delay steps of 60 ps and a maximum delay of 1.5 bin widths delays the start of the conversion with respect to the counter.

A small digital part inside the pixel is used to derive the steering signals for the two Sample & Hold branches, the delay circuit, and the reset of the latches. A method to generate a ninth bit inside the pixel is included as well (not shown in the figure).

The time is measured by a Gray-code counter (GCC) in the column periphery of the chip. The timestamps are transmitted differentially from the periphery along each column on 14 mm long shielded coplanar waveguides. When the threshold is reached in the pixel, the GCC value is stored in latches in the pixel. Since the latching in the pixels is asynchronous to the counting clock, bit errors due to different transmission delays or component variances between the individual bits must be avoided. This is solved by using the Gray code, which has a Hamming distance of 1. Hence, in every transition only a single bit toggles. It also minimizes power consumption of the counting and transmission blocks and switching noise originating from them.

The GCC is clocked with both edges of the 695 MHz clock, resulting in a time conversion bin width of 720 ps. The duty cycle of the clock is extremely important, any deviations from the ideal 50% duty cycle results in alternating large and small bins. A dedicated circuit in the chip periphery allows duty cycle adjustment, one for each half.

4.2.3 Storage

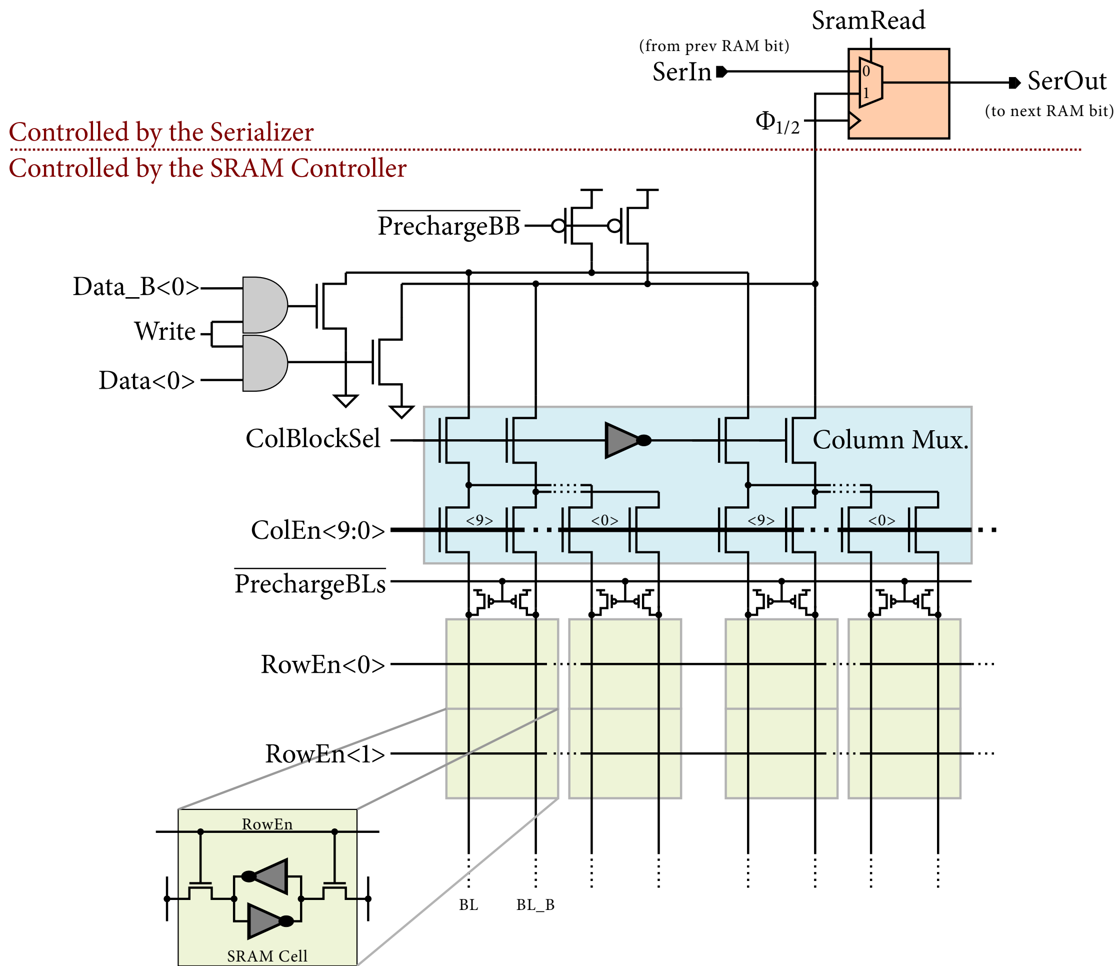

Figure 4.17: Schematic of a BitBlock including SRAM cells (green), column multiplexer (blue), read-out register (orange) and write circuit. 9-bit words can be stored by using the BitBlock 9 times [44].

The digitized values are stored locally in each pixel in a custom designed SRAM memory. IBM's dense SRAM cells are used with a custom periphery to reduce the control and address overhead. The SRAM size in F1 is 800 9-bit words per pixel with about 1/3 of the pixel filled by the memory. The memory architecture has been developed in the scope of another thesis [44], also published in [52], and are summarized here for further reference.

The SRAM is organized in 9 blocks for each bit to be stored (BitBlock), depicted in figure 4.17. Each block is again divided into a matrix of 40 x 20 cells, each consisting of a 6 transistor SRAM cell of 2.04 μm^2 size. Addressing a specific cell is possible by setting a RowEnable signal and switching the column multiplexer (NMOS switch) as desired. For read access, the bitline has to be precharged (PrechargeBLs) before connecting the memory cell by setting the address lines. Writing a value to the cell is achieved by precharging the bitlines, then pulling the positive or negative terminal to

ground, and subsequently connecting the memory cell to the bitlines, forcing the cross-coupled inverters to the desired state.

Since the address generation algorithm is implemented in the periphery, only a marginal periphery is needed inside a pixel, consisting mostly of the precharging and multiplexing transistors. Of the total space attributed to the memory, 88% is used for the memory cells and only 12% for periphery circuits. The address generation circuit includes a feature to overwrite memory cells during a burst after a veto command has been sent to the detector (see section 4.2.5.

For the readout of the pixel data during the XFEL pause, the memory cell addresses are selected in ascending order. The 9-bit value of each pixel is loaded in parallel into a serial shift register. The shift registers are connected along the columns, transporting the data to the chip periphery, where a fast serializer is driving a 350 MHz LVDS line.

4.2.4 13-bit Periphery DAC

Figure 4.18: Simplified schematic of the periphery DAC. The current from the PMOS sources is either directly sent to a resistor to ground (Low Range) or to a resistor to VDD via an NMOS current mirror (High Range). [44]

A high precision DAC is needed by the pixels for two purposes: In order to generate the MSDD front-end reset voltage, and to supply a test input signal for the ADCs. This has been realized on the F1 ASIC by a 13 bit Rail-to-Rail DAC driving the monitor bus, connected to a buffer in the front-end. The ADC input can either be connected directly to the monitor bus or via the filter amplifier as a buffer, in this case the monitor bus replaces the pixel-internal reference voltage.

Figure 4.18 shows a simplified version of the output stage of the DAC. The DAC itself consists of 8192 unit PMOS current sources which are activated through slow-control. Each unit current source yields a current of 60 nA, derived from an internally-generated reference current. The output stage converts the current from the array of parallel current sources to a voltage through a 1.65 kΩ resistor in two modes. In the Low Range Mode, the current is sent directly to ground, yielding a voltage between ground and 811 mV. A higher voltage can not be realized directly here due to the required headroom of the PMOS current sources. In the second mode, the High Range mode, the current is

mirrored first and then drawn through a resistor to the supply rail. In this case, the output voltage can reach VDD, again with a maximum swing of 811 mV.

4.2.5 Global control block

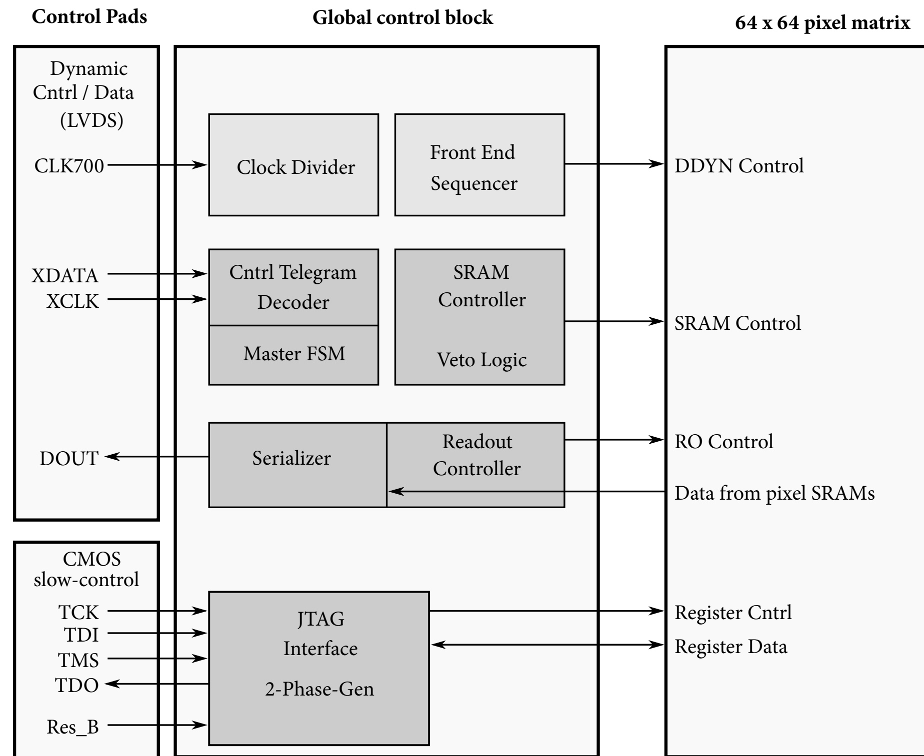

Figure 4.19: Overview of the global control block of the readout ASIC.

A digital synthesized block generates the signals needed to steer all the blocks on the chip. It is located in the periphery of the chip close to the IO bumps. The interface to the outside is minimalistic in order to minimize the bump count for the digital interface: Only a 4-pin JTAG interface for slow control and two LVDS lines for dynamic control of the chip are necessary. A reset signal, the fast clock for the ADCs and a single LVDS link for off-chip data transmission complete the digital interface. The differential LVDS standard minimizes switching noise and is available in standard FPGA IO cells, allowing easy interfacing without additional components.

Many functions of the global control block operation are configurable through registers. All slow-control registers on the chip are accessible through the JTAG TAP port. The TAP controller manages selection of registers, and shifting or loading selected registers. Four pins are necessary (TDI, TCK, TMS, TDO), while the reset of the TAP controller can be realized through a dedicated reset pin (TRST_B) or by clocking the TAP several times with TMS set low. The latter is used in the DSSC case to reduce the IO pin count. Chains of JTAG devices can be established by connecting the data output TDO and data input TDI of two devices. The pixel matrix is configured through several full custom shift register chains. The pixel registers can be programmed either as a chain or, individually selected through x-y-select registers, programmed directly.

The dynamic control signals for the in-pixel front-ends and ADCs (DDYN signals) are generated by a sequencer block with a granularity of a 695 MHz cycle. The sequencer module is based on shift registers that produce repeatable patterns.

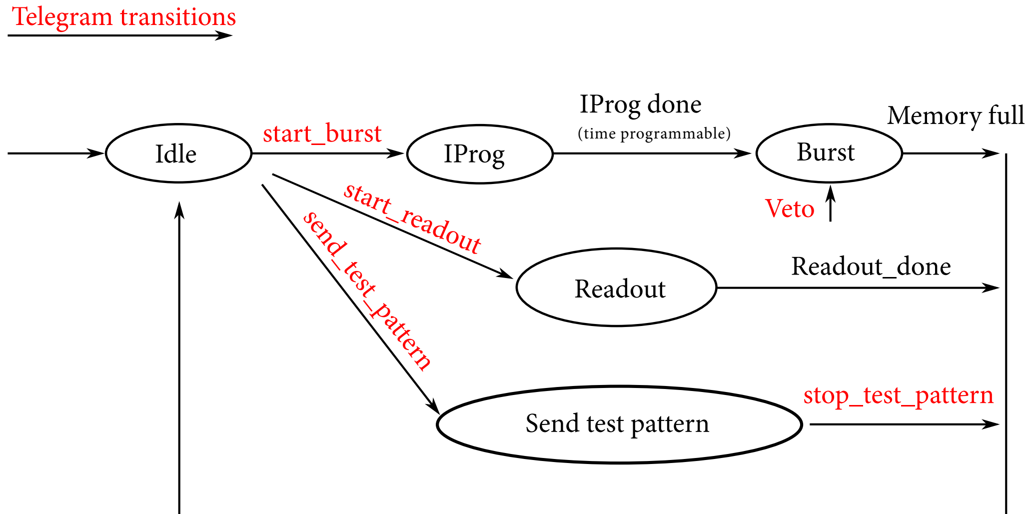

Figure 4.20: Master FSM state diagram. By sending command telegrams, data-taking can be triggered, as well as sending out the stored data.

A data line and a corresponding separate clock for sampling (*XDATA* and *XCLK*) are used to steer the dynamic behaviour of the ASIC. The master state machine is depicted in figure 4.20, where any transition from the idle state is triggered by a custom 5 bit command telegram.

After issuing a start_burst command, the ASIC directly enters the IProg state which fine-tunes the current subtraction in the pixel front-ends. The length is configurable. The detector electronics need to take care of sending the start_burst command at the appropriate time ahead of a train, and to enable the ASIC power supplies. The number of subsequent measurement cycles can be programmed as well. Individual events can be overwritten by a veto command, which triggers a reuse of the corresponding SRAM memory cell. The veto message has to be sent after a fixed, but programmable, delay.

The readout command triggers the SRAM controller and the serializer to send out the complete data from the in-pixel SRAMs through a 350 Mbit/s LVDS line. The readout speed is fixed through a 1:2 clock divider to the 695 MHz ADC clock. Total readout time is approx. 94 ms[2] and therefore close to the limit given by the XFEL pause of 99.4 ms. A test or synchronization sequence for the readout FPGA can be started through the send_test_pattern telegram, which continuously sends out a previously programmed pattern.

Synchronization between the readout system and the XFEL pulse frequency has to be realized through the length of a measurement cycle. It is configurable via slow-control in the range of 220 ns (maximum planned framerate) down to 1.28 µs. Even slower readout modes can be realized through the hold functionality of the sequencer.

[2]Readout time is $t_{RO} = \frac{n_{Px} n_{Cells} w_{word}}{f_{clk,RO}}$ with the word width $w_{word} = 10$ (9 data bits, 1 checksum bit)

4.2.6 Performance goals

The performance goals are listed in table 4.2 for a set of photon energies. The table shows that the noise of the MSDD system is ≈ 3 times higher than a DEPFET-based detector. A signal-to-noise ratio larger than 5σ for photon energies of and below 1 keV is only possible with DEPFETs.

E_{ph} [keV]	DEPFET		MSDD	
	ENC [el.]	Dynamic Range [ph.]	ENC [el.]	Dynamic Range [ph.]
0.25	NA	480	NA	294
0.5	18.4	1116	62.6	420
1	26	3270	71.6	2859
1.5	21.1	>4000	58.8	2022
2	24.4	>7000	71.6	1429
3	19.5	>10000	58.8	1011

Table 4.2: Performance goals for the DSSC detector system [53]. ENC and dynamic range values are given for 4.5 MHz frame rate (255 ADC bins).

4.3 The Camera Head

The DSSC detector will be split into ladder modules [54] of 128 x 512 pixels containing 2 monolithic sensors. Each monolithic sensor of 128 x 256 pixels is bump-bonded to 8 readout ASICs, glued to a Si-heat spreader and a mainboard PCB. Wirebonds between mainboard and sensor connect power and signals to the focal plane, where it is routed to the pixel matrix or to the readout ASIC on the sensor.

The mainboard carries the two sensor-readout chip stacks and connects to five rigid-flex PCBs and a single flex cable in orthogonal orientation, shown in figure 4.21. The mainboard is an 18-layer LTCC[3] PCB with cavities, u-vias and a bond pad pitch of only 150 µm. FR4 boards have been studied as the conventional solution, but the surface quality of the studied EPIG (electro-less palladium immersion gold) and immersion silver was unsatisfactory or not suited for wire bonding at all. The LTCC board's gold surface proved to be superior for wire bonding. However, the ceramics have proven to be fragile, and shrinking of the ceramics during the sintering process has to be taken into account for the following camera assembly steps.

Four regulator boards generate both the static supply voltage as well as the cycled supply voltages for four readout ASICs each. The supply voltages are digitally controlled by a chain of shift registers, with the parallel outputs of the shift registers controlling a single voltage regulator. The voltage regulators are provided with large capacitor banks to provide power during the 600 µs long trains. The Clear pulses needed for DEPFET operation are generated on the regulator boards as well by a dedicated circuit.

The four regulator boards are controlled by the central PCB, the I/O board. Initially developed in [55] and refined during the course of this thesis, the I/O board generates all the logic signals locally needed in the camera head. Its core element is a Xilinx Spartan-6 FPGA listening to telegrams from

[3] low temperature co-fired ceramics

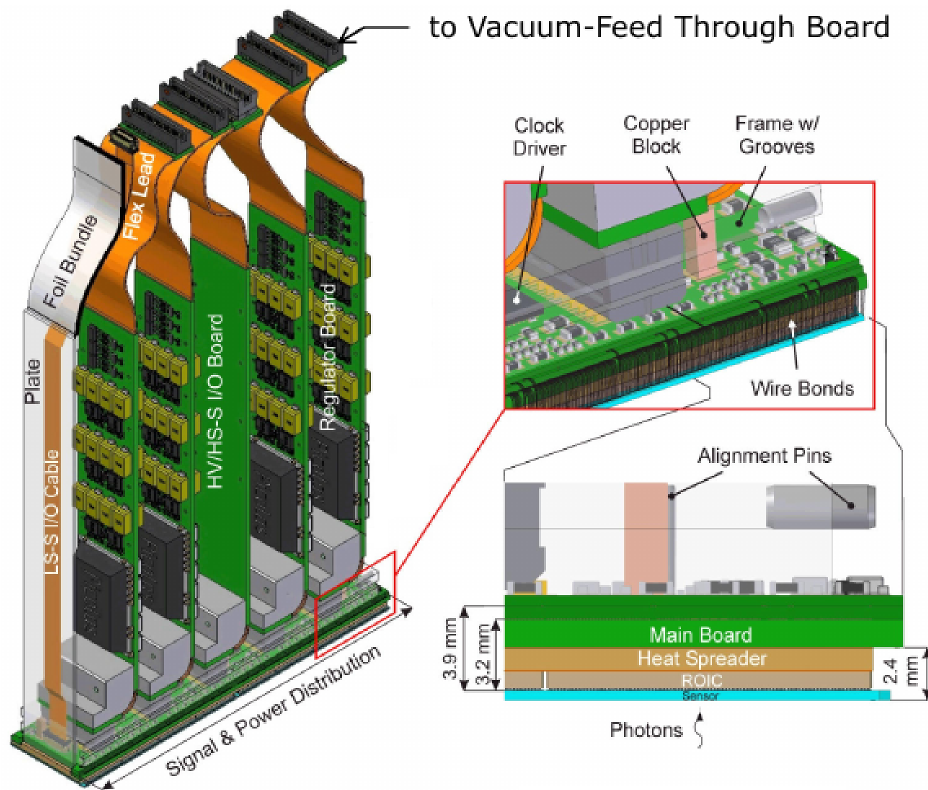

Figure 4.21: Components in the camera head. The sensor and ASIC assembly at the bottom is powered and controlled by the PCBs behind the focal plane [37].

the backend electronics indicating upcoming data-taking. With programmable timing, the supply voltages for the ASICs are turned on, sensor clear pulses are enabled, and the ASIC control signals are forwarded. The second main challenge of the I/O board is data aggregation from the readout ASICs. The FPGA receives on 16 LVDS data lines the data from each readout ASIC connected to the mainboard, each sending data at 350 Mbit/s during the readout phase. The data is merged into three data streams based on the Aurora protocol running at 3.125 Gbit/s.

The flex cable, visible on the left in figure 4.21, serves as a simple way of connecting static, low current DEPFET bias voltages and JTAG signals to the mainboard.

All regulator boards, the I/O board and the flex cable connect to the Module Interconnection Board (MIB). It hosts further decoupling capacitors for the source voltage and a Module Amplifier needed for the Clear pulse generation.

The whole ladder electronics up to the MIB will be placed inside a vacuum chamber below 10^{-5} mbar and will be cooled to a sensor temperature of −20 °C. Heat generated on the focal plane or on devices on the PCBs will be removed by an Al frame guiding the heat to the cooling blocks. The Patch-Panel Flex Cable connects the MIB to the interface outside the vacuum chamber.

4.4 The backend electronics

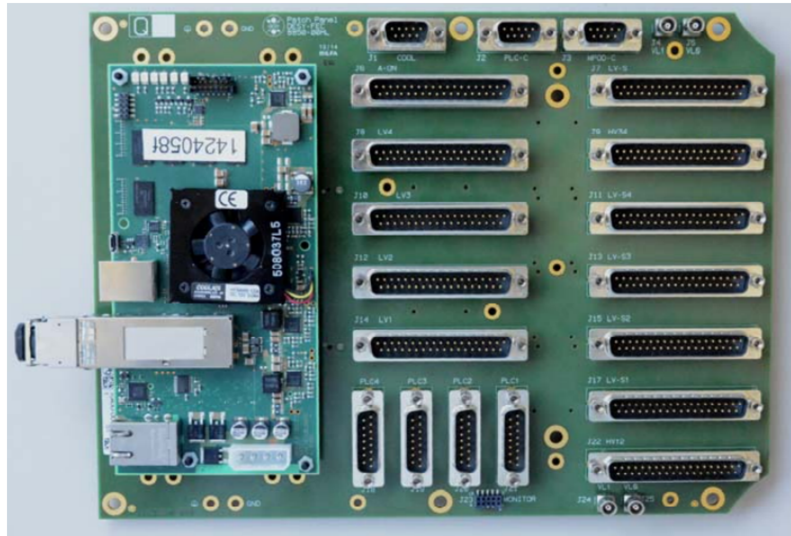

Figure 4.22: Patch Panel Transceiver (left) mounted on the Patch Panel [37]. The FPGA on the PPT is the main detector control and readout entity.

Outside the vacuum chamber, four Patch Panel Cables from four ladders connect to the Patch Panel, the main interface board for the power supplies and for the control signals going to and from the ladders. On the Patch Panel, two extra cards are plugged: The Safety Interlock Board (SIB) and the Patch Panel Transceiver (PPT).

The *SIB* [56] is designed to keep the detector system in a safe state. The SIB monitors 75 temperature sensors as well as two pressure sensors and a humidity sensor, all located in the vacuum chamber. A decision-matrix software reads the sensor states continuously and determines the current state of the system. In case of failure or eventually hazardous situations, the SIB can shut down power delivery to the detector and stop the liquid cooling system.

The *Patch Panel Transceiver* [57], seen on the left in figure 4.22 is a highly integrated, small form factor (only 80 x 160 mm^2) card to be plugged on the Patch Panel, where it acts as the main interface, control and readout device of a detector quadrant. It utilizes state-of-the-art FPGA technology to achieve the density needed for the small form factor. The board has been designed in the Heidelberg institute and mainly hosts the following circuits:

- Xilinx Kintex-7 XC7K325T FPGA providing 16 Multi-Gigabit Transceivers
- RJ-45 connector for slow-control ethernet
- RJ-45 connector using an LVDS-based custom protocol for synchronization with the XFEL machine
- QSFP connector for four 10 Gbit/s output links
- 800 MHz DDR3 memory for frame buffering (4 x 2 Gbit)
- 400 MHz DDR3 memory for the processor (2 Gbit)
- Non-volatile configuration flash memories
- Circuit to derive and distribute the system clocks from the XFEL clock, including the low-

jitter clock needed by the ADCs in the focal plane, also used for operation of the ASIC sequencer synchronous to the XFEL machine

Appendix A is presenting the microprocessor environment of the PPT designed by the author.

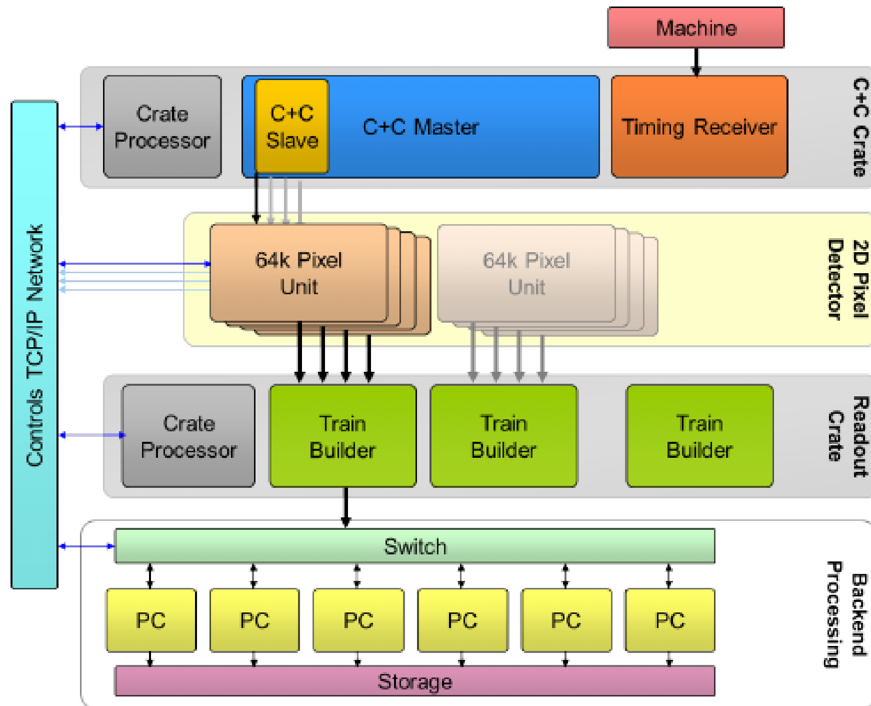

Figure 4.23: Block diagram of the XFEL C&C and DAQ system [58]. The C&C system generates timing information for the detectors, which send their data through the train builder system to a PC layer.

Figure 4.23 shows a schematic of the Clock & Control (C&C) and the Data Acquision (DAQ) system at the European XFEL. The timing information regarding the accelerator is distributed to the detectors via the C&C Crate, where fanout boards generate synchronous timing signals for several detector units. The detectors receive a 99 MHz clock for synchronization to the XFEL machine, derived from the 4.5 MHz bunch clock, and a start signal 15 ms ahead of an upcoming train. During a train, veto information for specific events can be distributed to the detectors using a custom and eventually detector-specific command protocol. Status information from the detectors can be sent directly to the C&C system on a status link. More details about the C&C system have been published in [58].

The Patch Panel Transceiver uses four 10 Gbit/s Ethernet links for data transmission amounting to a net data rate of 36 Gbit/s. The total amount of data output from the whole camera thus calculates to the tremendous amount of 144 Gbit/s. The FPGA-based Train Builder System [59] will be the device handling these large amounts of data, reassembling complete images from the different optical links the fragments are transmitted on. The reassembled images are subsequently sent to a PC farm for immediate visualization, data processing and long-term archiving.

4.5 Comparison with other Detectors for the European XFEL

While the DSSC detector is designed and best suited for low energy photons below 6 keV due to the low noise DEPFET device, two other detectors are under development for the beamlines with higher photon energies. A compact comparison is given in table 4.3.

The Adaptive Gain Integrating Pixel Detector (AGIPD), presented in [60] and [61], features a 500 µm thick silicon sensor with 200 x 200 µm^2 pixels providing a 90 % quantum efficiency at 12 keV. In the readout ASIC [62], a charge-sensitive amplifier featuring correlated double sampling (CDS) is used, while a discriminator adds additional feedback capacitors if the signal is large enough to cross a tunable threshold. This increases the dynamic range by reducing the gain by a factor of 16 or, subsequently, by 64, resulting in a dynamic range of 2×10^4 at 1 keV photons. The result is stored in an array of 352 analog memory cells, implemented by NMOS in N-well transistors. The analog memory has its caveats, requiring a large area (85 % of a pixel for 352 cells) and leakage, which is non-negligible for the maximum time until readout of 99 ms. Both the analog output value of the CDS stage plus the 3-level gain bit are stored for each event. The stored values are fed to an amplifier during the readout phase, buffering the stored value for digitization by discrete ADCs on the PCBs. The AGIPD detector is planned for an energy range of 3 to 13 keV and offers single photon sensitivity with an SNR of 10 at 12 keV in the high gain stage. As the AGIPD detector is planned for high energy beamlines, a radiation tolerance of up to 1 GGy over three years is needed. Measurements on prototypes have shown no functional deterioration of the chip, just a slight increase of noise, for doses up to 10 MGy.

The Large Pixel Detector (LPD) uses a 500 µm thick sensor with 500 x 500 µm^2 pixels. The signal charge generated in the sensor is fed to a preamplifier with a 50 pF feedback capacitor. This input branch gives a dynamic range of 10^5 12 keV photons per pixel per pulse. A low dynamic range, but also lower noise option with 5 pF feedback is also available. As in the AGIPD detector, analog memory cells are used, the larger pixels allow for 512 storage cells. During readout, 16 on chip ADCs convert the stored values and stream the data off on LVDS links. Mechanically, a silicon interposer with through vias for every pixel is used between ASIC and sensor, which puts some vertical space between the two. Moreover, the wire bonds for the ASIC connection are hidden behind the sensor, making the sensor and ASIC assembly 4-side buttable. Radiation hardness has been proven up to 5 MGy at 12 keV. The LPD detector is designed for an energy range of 1 to 24 keV, while offering single photon sensitivity at 5σ at 12 keV. More details on the LPD can be found in [63].

	AGIPD	LPD	DSSC
Sensor	500 µm p-in-n Si	500 µm Si	DEPFET, 450 µm thick
Energy Range	3 - 13 keV	1 - 24 keV	0.5 - 6 keV
Sensor pixel size	200 µm x 200 µm	500 µm x 500 µm	236 µm x 204 µm (hex.)
Noise	< 343e$^-$ (0.1 ph at 12 keV)	1000e$^-$ (0.3 ph at 12 keV)	< 30 e$^-$ (0.1 ph at 1 keV)
Gain concept	Adaptive gain switching	Multiple gain paths	Non-linear sensor
Data storage type	Analog storage on cap.	Analog storage on cap.	Digital SRAM cells
Storage cells	352	512	800

Table 4.3: Comparison of the main properties of the three 2D imagers for the European XFEL.

5 ASIC Test Environment

While the focal plane hardware developments described in the last chapter are an excellent tool for the final research applications, PCBs like the regulator and I/O board or the mainboard are no viable tool during the prototyping phase of individual components, although designed exactly for these components. First, these final system components are optimized to occupy the smallest space possible, while being able to connect to as many other devices as possible, leaving mostly no space for test points or spare connections. Second, the specialized geometries like the rigid-flex boards are expensive and not needed for the prototyping "on the table". Moreover, the high bandwidth communication standards needed by the final DAQ system are requiring specialized computer hardware to receive and save the data, as they are designed for transferring data streams from larger numbers of ASICs.

The goal of the test setup development in the scope of this thesis was a flexible, easy-to-use hardware to characterize ASICs and ASIC-sensor assemblies without the full module complexity, but in similar environment. Full module complexity includes the demand for final system parts like the Patch Panel, cooling, vacuum operation and tight space constraints as well as specialized hardware for high-speed data transfers like the 40 Gbit/s optical link on the PPT. For the test system, an accompanying software package for control, readout and visualization has been developed, which can be run on a standalone computer.

The only external hardware required is a power supply and a simple USB connection for control of the system and data transfer. Nevertheless, a lot of possibilities to attach external measurement or test injection equipment are provided, a feature which is not available in the very compact and integrated final system.

The result is a compact test hardware, suited for constricted space environments like beamlines or temperature controlled chambers. It is in use in several groups of the DSSC collaboration: the ASIC development groups at DESY and Politecnico di Milano, the module test group at University of Bergamo, and the calibration groups in Munich (EuXFEL GmbH) and Politecnico di Milano. In the following sections, the hardware, firmware and software developments are explained in detail.

5.1 Hardware

The core system depicted in figure 5.1 is composed of an FPGA board, a mainboard and a carrier board for the device under test (DUT). The device under test can be just an ASIC or an assembly of ASIC and sensor, where the voltages needed for sensor biasing can be easily fed to the assembly from the Bias board or from external equipment. In this topology, since the DUT carrier is an entirely passive board, larger numbers of carriers can be produced at reasonable prices, allowing various ASICs and assemblies to be tested by simply plugging in a different carrier. The connections to

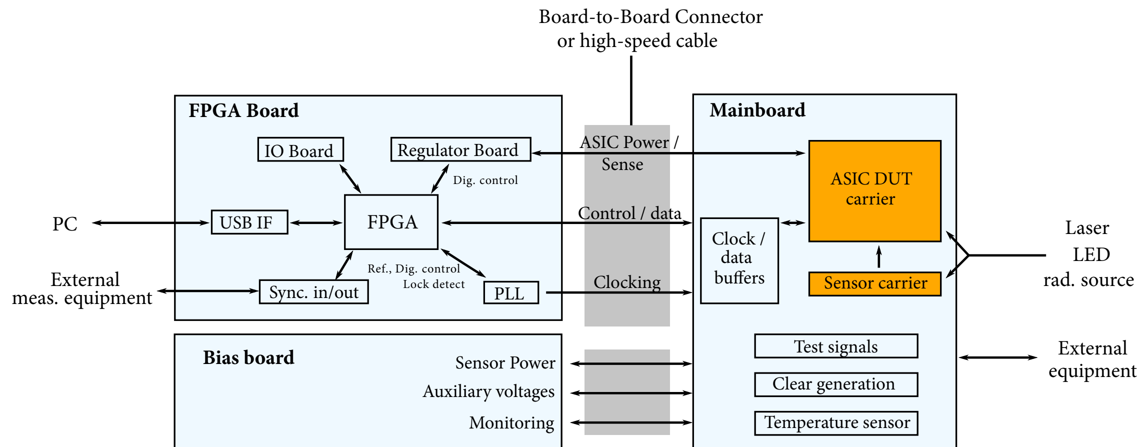

Figure 5.1: Block diagram of the lab test setup. The Mainboard holds the ASIC and sensor under test on special carriers and can be operated remotely, e.g. in a vacuum chamber.

the mainboard can be established either directly through board-to-board connectors or as remote connections via cables.

A voltage drop on the power lines over the cables or connectors is compensated by sensing the power and ground voltage at the load. If the sense lines for power and ground are properly connected, the supply voltage at the ASIC input can be held stable. Anyways, the ASIC supply lines are routed on dedicated power and ground planes in on the PCBs to minimize the resistance. Signal deterioration over the cable has been addressed by adding buffers for critical signals.

The modularity and the possible connections of the system allowed for a continously growing integration of several final system components into the test system. This includes the possibility, for example, to include and test final DAQ hardware (I/O Board, Patch Panel Transceiver), power generation hardware (Regulator Board) and final ASIC and sensor assemblies.

The individual boards are explained in more detail in the following.

5.1.1 FPGA Board

The FPGA board serves as the central control module and readout controller. The centerpiece of the general purpose board is a Xilinx Spartan-6 FPGA with multi-gigabit transceivers. An external USB 2.0 controller IC (FTDI FT2232H) connected through an 8-bit bidirectional FIFO bus establishes the connection to the control PC, allowing the transmission of both JTAG signals for FPGA programming as well as user data after programming through one common USB port. A programmable PLL IC (Analog Devices ADF4351) generates the low-jitter 695 MHz clock needed by the ASIC's ADCs. Through a series of clock multiplexers and dividers, the clock is fed to the DUT as well as the FPGA, allowing synchronous operation of both devices.

The ASIC's supply voltages are fed to the mainboard from connectors, offering the possibility to use a regulator board as in the final detector system or by plugging simpler replacement boards. The replacement boards used for the F1 ASIC tests feature three LT1764A regulators, each providing a peak current up to 3 A and an output voltage adjustable by the selection of a resistive divider. Digital control through five 3.3 V lines from the FPGA is available.

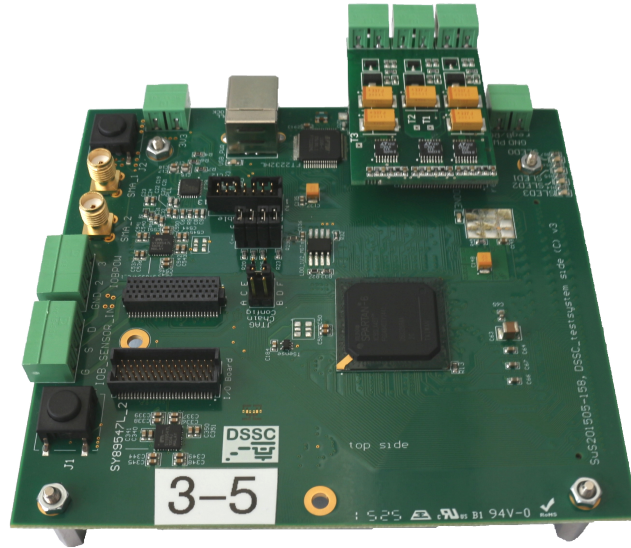

Figure 5.2: FPGA board with Regulator Replacement Board attached. The core element, a Spartan-6 FPGA, creates precise timing signals for the readout ASIC under test, generates slow-control programming signals and forwards the data from the readout ASIC to the control PC via USB. Not visible, on the bottom: A 200 pin connector to the mainboard.

In the same way, connectors are provided to plug an I/O board, allowing to feed an ASIC's data stream into the final readout hardware. An MGT link between the I/O board and the readout system FPGA board can be established as well, which allowed to test the I/O Board's MGT capabilities before the PPT was available.

A large number of power and signal lines with various I/O standards are going to the mainboard, making the FPGA board a flexible tool for the readout system. For instance, 77 single-ended and 20 differential lines including dedicated clock lines are routed from the FPGA to the connector. These are used, for example, for distributing the differential *XCLK* and *XDATA* signals for fast control of the ASIC, and for the JTAG slow-control signals.

The FPGA board was initially developed at the chair in 2010. Modifications by the author were necessary during the course of the thesis, fixing power supply problems and expanding the connection possibilities to external devices through additional connectors. External devices can since be run synchronously to the device under test, or the system can be triggered by other devices, e.g. in a test beam environment. The board is also very compact with a size of 110 x 117.5 mm^2.

The latest design change by the author included a complete rework of the board, mainly to incorporate a USB 3.0 connection to the host PC in order to overcome a bandwidth bottleneck. More details about the data bandwidth can be found in section 5.2.

5.1.2 Mainboard

The mainboard serves as the central board for interconnection to the ASIC and sensor bias distribution PCB in the setup. Several iterations of this board were necessary to support changes in ASIC

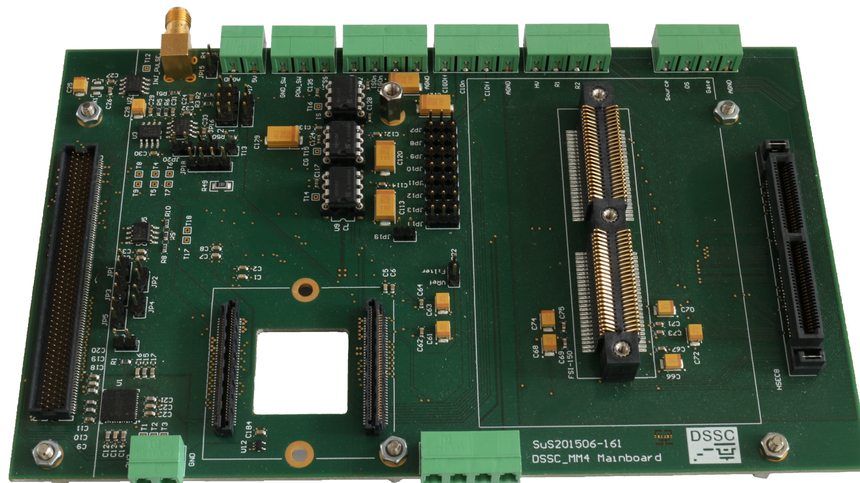

Figure 5.3: Last generation of the DSSC test system mainboard. Left: Connector to the FPGA Board. Bottom left: Connectors to ASIC/Sensor under test with hole for sensor irradiation. Right: Connectors for sensor ceramics and sensor biasing cable.

development or to meet the demands for improved measurements. The latest version of the board is shown in figure 5.3 with a size of 110 x 180 mm^2.

On the left side, a large connector (200 pins) for the FPGA board can be found, delivering clock, control, and power signals. The ASIC carrier can be plugged next to it. Two connectors are used for the ASIC carrier to provide mechanical support, and to separate the sensitive analog supply and bias nodes from the digital lines. The large hole between the ASIC connectors allows for an unobstructed irradiation from the bottom, if needed.

A clock buffer and distributor IC (LMK01000) buffers the fast ADC clock and distributes two copies to the ASIC connector, allowing to use up to two ASICs in parallel. The IC features very low jitter (30 fs) and allows to delay the output clocks with respect to the input. The clock delay is used in the testsystem to shift the ASIC's output data with respect to the sampling clock in the FPGA, that is generated from the non-delayed version of the clock.

A separate connector for stand-alone DEPFET sensors mounted to dedicated ceramics is visible on the right. All sensor bias voltages are routed to both the ASIC connector and the stand-alone sensor connector, with several lines between the two for the connection of sensor pixels to readout pixels.

While the ASIC supply voltages are delivered through the FPGA board connector, the bias voltages needed for sensor operation can be fed in flexibly via single cables as well as, more compact, by a 64 pin Samtec EEDP cable. The EEDP cable solution in principle also offers the possibility for digitally controlled bias voltages, as digital control lines are routed from the FPGA board to the connector. Supply and bias voltage decoupling has been implemented on the mainboard, offering the possibility to check different decoupling and ground connection schemes.

Circuits to generate the Clear, Clear gate and Inner Substrate pulses needed for DEPFET operation and sensor-internal charge injection have been implemented using analog high-voltage multiplexers. The circuitry is controlled by the FPGA and runs synchronously to the readout ASIC.

The board also holds a temperature measurement circuit, consisting of an IC with a single pin PWM output whose duty cycle depends on the temperature. The output is digitized by the FPGA and is available for monitoring or temperature regulation in the user software. The sensor IC is placed close to the ASIC connectors in order to measure the temperature as close to the ASIC as (easily) possible.

5.1.3 Chip carriers

Being the most delicate part of the setup, the chip carrier boards hold the device under test and are essentially fanout boards. Control and readout signals are usually routed on the external layers, while the power to the ASIC and sensor assemblies are put on split power and ground planes in the inner layers to provide low impedance paths. When using bump-bonded sensor-ASIC assemblies, a hole in the PCB is provided for wirebonding the high voltage needed for depletion from the backside. Through the hole, the sensor to be tested can be irradiated.

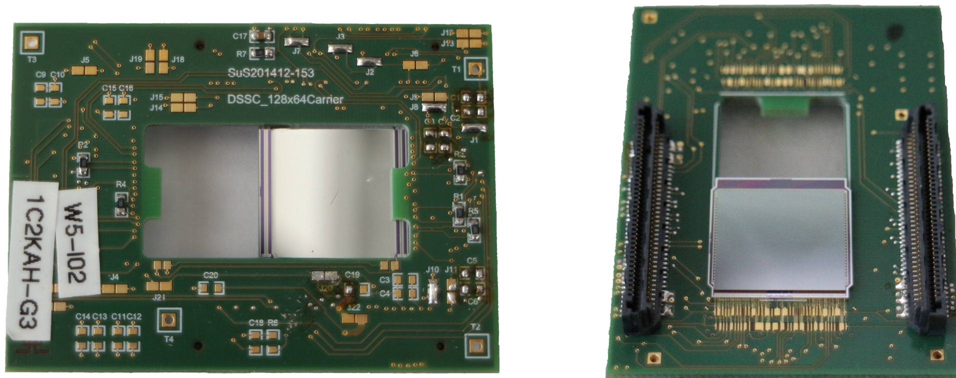

Figure 5.4: Left: Top view on a 64 x 64 MSDD and F1 assembly with the reflective entrance window visible. Right: Bottom view on the dense wirebonding area between carrier PCB and assembly, and the connectors.

The most complex carrier designed during the course of this thesis is a PCB designed to carry the large test structures containing a sensor and one or two bump-bonded F1 ASIC, depicted in figure 5.4. This can be a MSDD assembly, where only 64x64 pixel versions for one readout ASIC are available, or a DEPFET assembly, where a 128x64 version has been designed for two readout ASICs. In the latter case, in total 184 wirebonds on two opposite sides of the assembly are needed on a 150 µm pitch for the connection of the assembly. The 6-layer PCB delivers the power to the assembly on dedicated power and ground layers. All differential pairs, including the most sensitive ADC clock pair due to its influence on the bin size matching, is routed closely together with length matching, shielded from switching lines like the DEPFET clear.

5.1.4 Probecard

Prior to mounting ASICs to sensors or interposers, testing the ASICs electrically is necessary. This is done on a probestation, where individual chips or whole wafers can be connected by probe needles.

Figure 5.5: Probecard (left) and needle ring (right). The needle ring, inserted into the probecard, establishes the contact to the 88 periphery bumps on the F1 ASIC.

In order to test the full scale chip, all 88 bumps in the periphery need to be connected in order to supply control and power signals to the ASIC while being able to read the data.

Therefore, alternatively to the mainboard, a probecard (figure 5.5) can be attached to the FPGA board. Due to the restricted space around the probestation, a cable is used to connect them. A dedicated high-speed cable ensures proper transmission for the high-speed clock and data lines.

The probecard is fixed in the probestation by a metal frame. The position of the probecard can be tuned with micrometer screws, while the alignment of the wafer relative to the fixed probecard is done by an XYZ-movable chuck. The wafer is fixed to the chuck by vacuum.

The electrical connection to the ASIC under test is realized by a touching the bump bonds with probe needles. The needle ring is manufactured by htt GmbH according to the specification of the bump position, where the needle tips are supposed to be. The needles are glued into an Epoxy ring pointing to the center. The tips are bent in order to contact the bumps below the ring. Different needle tip geometries are in use to contact different types of material or pad types. In the F1 case, the 80 µm diameter bumps are touched with tungsten needles with a tip diameter of 1.3 mil (33 µm). The Epoxy ring is positioned on a round PCB with metal pins, serving as a connector to the probecard PCB.

On the probecard PCB, several injection methods have been added in order to provide a stimulus to the ASIC. This includes a 16-bit voltage DAC for ADC characterization and connectors for external devices for high precision measurements of the monitor bus or current injections during the burst phase, similar to a sensor.

The needle positions are optimized in order to have the LVDS pairs closely together, both on PCB level and on needle level. This is only possible by using needles with an additional bend right before the tip (see figure 5.6). The needle type has been selected due to bad experience with flat needles at the chair. Since no protection environment for the bumps is available, oxidation will take place inevitably. Flat needles could not properly remove the oxidation layer, resulting in a bad electrical connection to the bump. In order to contact the F1 chip, a sharp needle with a tip diameter of 33 µm were used, which could establish a reasonable contact.

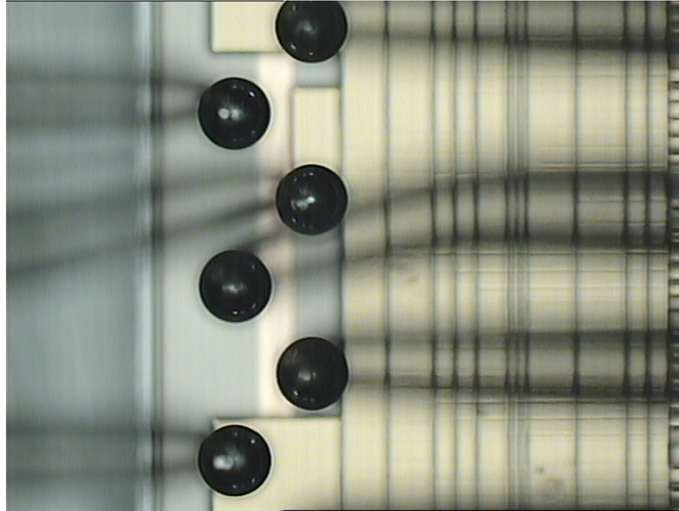

Figure 5.6: View through the microscope on the needles and the F1 ASIC below. The two needles on the lower right carry the 695 MHz clock to the chip under test. For better signal quality, the needles are grouped together.

5.2 Firmware

The firmware code for the DSSC prototype system has been written in plain Verilog 2001, allowing it to be synthesized to several hardware platforms, with the exception of low-level blocks for access to clocking resources, input/output buffers and FIFO memory structures. These are generated using Xilinx primitives for the used Spartan-6 FPGA [64].

The FPGA firmware in the DSSC test environment is divided in three major parts and clock domains. These are the ASIC operation block, the USB interface block and a third part independent of the others. The firmware structure is shown in figure 5.7. The main idea behind the used architecture is to make the firmware flexible for different variants of ASICs or mainboards. This has been achieved by making the firmware blocks configurable through control registers, for example, and by making it easy to add further modules to the USB interface to implement new tasks.

The USB block has been previously developed at the chair [65] and encapsulates the data transfer between the external USB microcontroller (FTDI FT2232H) and the FPGA. The low-level bidirectional synchronous FIFO procotol for interaction with the microcontroller is implemented with FIFO memory blocks for incoming and outgoing data. A state machine generates the control signals in order to transfer data from the FTDI chip to the FPGA ('Write access') or from the FPGA to the FTDI ('Read access'). The FIFOs are implemented with two independent clock domains for data buffering and easy clock domain crossing e.g. from the ASIC clock domain to the USB interface domain. A lightweight packet-based protocol is implemented on top, with just a header being added to each set of data containing command, address and data length information, allowing flexible and high data rate transfers to and from the FPGA with a check for data integrity.

The FTDI chip also acts as a clock source, generating a 60 MHz clock signal driving a Clock Management Tile (CMT) primitive inside the FPGA. While this clock is used in the USB communication blocks in the FPGA, it is also fed out as a reference clock for the PLL generating the fast

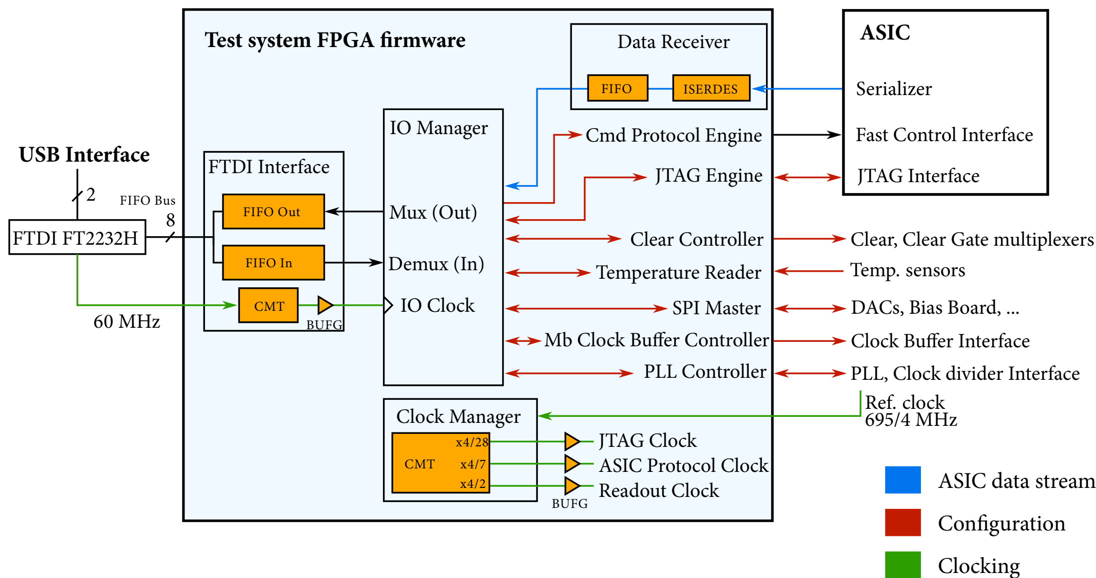

Figure 5.7: Structure of the DSSC prototype setup firmware. The central IO Manager device features a light-weight packet-based interface to other firmware modules. Xilinx IP primitives are marked orange.

695 MHz clock for the ASIC. The PLL needs to be configured and enabled through a custom serial interface, implemented in the FPGA fabric. In order to allow synchronous operation of logic in the FPGA and in the ASIC, a copy of the fast clock is divided (1:4) and fed back into the FPGA, driving another CMT primitive. Division of the fast clock is necessary due to the FPGA's performance constraints.

The *JTAG engine*, also previously developed at the chair, implements the JTAG master for the slow-control communication with one or several daisy-chained ASICs. The JTAG clock speed has been fixed for the prototype systems to 6.25 MHz, resulting in a total configuration time of 31 ms per ASIC (writing all registers). The full reconfiguration of the pixel matrix between two XFEL bursts is desirable for the final system, requiring an increased TCK frequency of 31 MHz due to the JTAG chain comprising 16 ASICs. Future studies in the final ladder systems will show the feasibility of full reconfiguration between two bursts.

The *Command Protocol Engine* serves as the central state machine for the ASIC fast control. It can be manually controlled through the user software to move the ASIC to the burst, readout or test pattern modes, or, the standard way, to do a burst, directly followed by a readout. The FPGA logic generates the necessary command telegrams on the *XDATA* line. The corresponding clock line *XCLK* is running at 100 MHz. The Command Protocol Engine also delivers status information for other blocks about the current operation mode of the ASIC. Finally, the engine is capable of continuously repeating the burst and readout commands at a 10 Hz burst rate, similar to the final application at the EuXFEL. Tests have shown that the continuous operation stabilizes the temperature of the ASIC, improving the stability of the ASIC measurements compared to 'random' events triggered by the host PC.

The cycled sensor voltage control signals are generated by the *Switched Signals Controller*. A

counter clocked with *XCLK* provides timing information within the ASIC measurement cycle, yielding a granularity of 10 ns. The Clear, Clear Gate and Inner Substrate signals are pulsed at user-defined positions in the measurement cycle.

Temperature sensors are located on the FPGA board and the mainboard, close to the ASIC location. These ICs are connected by just one line to the FPGA, on which they continuously send the temperature information encoded as the duty-cycle of a fixed-frequency signal. This information is converted to a digital value by the FPGA and is available for the user software to read. An implementation for continuous monitoring of the temperature can be realized straightforward by adding the digitized temperature to the ASIC data stream, resulting in a 10 Hz frequency of temperature readings.

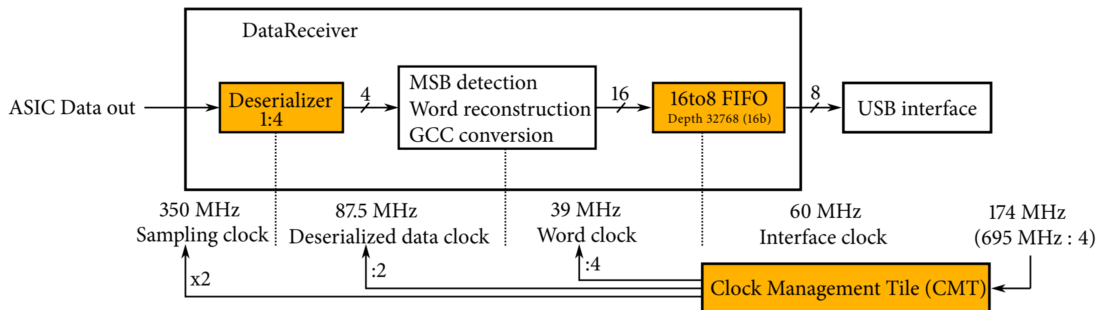

Figure 5.8: Architecture of the Data Receiver logic in the FPGA. The firmware module deserializes the input stream from the readout ASIC and repacks it into 16 bit words. Used Xilinx IP cores are marked orange.

Data Receiver (Figure 5.8) In order to reach the goal of receiving the tested ASIC's data stream at 350 MHz, the incoming data is fed into deserializer blocks (ISERDES) to repack the serial data stream into the 8-bit wide USB interface. A single ISERDES primitive with 1:4 deserialization can be conveniently used at the given clock speeds, resulting in a 87.5 MHz output rate. The Data Receiver logic includes a detection of the leading 1 of the ASIC data stream in order to align the data. For the pixel memory data, conversion from Gray code to binary is already done in the FPGA, so no further computation on the data is needed on PC level. Each word sent by the ASIC contains 9 bits, which are repacked into two bytes, allowing for convenient sorting on the computer but inflating the data stream.

At this point, the bandwidth of the USB connection should be addressed. USB 2.0 HighSpeed mode uses a gross bit rate of 480 Mbit/s, with net data rates up to 300 Mbit/s. This is not sufficient for the transmission of the complete data stream from a single readout ASIC to the host PC. Moreover, the FTDI chip operates in bulk transfer mode, a low priority USB transfer mode with no guaranteed bandwidth, with a packet size of 512 bytes. Since the data stream from the ASIC can neither be halted nor stored completely in the FPGA or the FTDI chip, any delays in the USB connection lead to data piling up in the FIFOs. As soon as a FIFO runs full, data has to be discarded. Since the USB interface speed is slightly slower than the ASIC's data rate, there will be no time for the FIFOs to be emptied. The FIFO depth available in the Spartan-6 FPGA for data buffering is 32768 16-bit words. Hence, it takes the ASIC data stream only 840 μs to fill the FIFO completely, which is definitely reached due to the USB delays. Full F1 data reception and forwarding is therefore not feasible.

In order to overcome the USB 2.0 data rate limiting the direct forwarding the full 350 Mbit/s data stream from an F1 ASIC to the PC, different data selection algorithms have been developed: single pixel readout, full F readout, and an intermediate window mode are available. The single pixel mode is straightforward, only the memory entries of one channel are sent through the USB connection, the rest is discarded by the FPGA, resulting in only 1/4096 of the data rate.

Full F readout mode implements the opposite, sending all the data from the ASIC. The challenge here was to reduce the data rate while maintaining data integrity. This has been achieved by utilizing the non-destructive readout of the SRAM cells in the F1 ASIC and properly selecting the data words to be sent over the USB connection. The FPGA triggers eight readout cycles of the chip, each time, it sends the whole memory content of each pixel. The FPGA forwards every eighth word, with an offset incremented in each readout cycle. Thus, in the first run, words 0, 8, 16 etc. are sent, then words 1, 9, 17, and so on, until, after eight runs, each word has been sent to the PC, which has to correctly assemble the full data set. Using this mode, the full SRAM content of one burst can be acquired in the PC.

The intermediate "window" mode can be used if a subset of pixels is sufficient. In the current implementation, the data from a 10 x 10 pixel window is sent through USB, effectively reducing the data rate to 8.5 Mbit/s. In principle, an unrestricted set of up to 512 pixels (1/8) could be selected for sending out - the implementation of a 2D area of pixels has been a suggestion from the calibration groups, which was also straightforward to implement, as row and column indices were already available for selection. Thus, a 'small 2D sensor' running at full speed has been realized.

An effort to finally overcome the limitation of the USB 2.0 data rate has been made after interface chips for the new USB 3.0 standard have been available. A new FPGA board with the FTDI FT601 and a new generation FPGA generation (Xilinx Artix-7) has been designed by the author, allowing to exploit the 5 Gbit/s bandwidth of the new connection standard. At the time of writing of this thesis, the new board has been used successfully during tests of the new F2 ASIC.

5.3 Software

Since the testing of the first small matrix chip started in 2010, a custom C++ software project has been started. Continuous contributions mainly by the Heidelberg group members have vastly expanded the software package to be a versatile and effective environment for chip testing and measurements.

The software interacts on a low level with the test system connected to the USB port of the computer it is running on. The application uses the libftdi[66] library for communication over the USB bus. The FPGA firmware is uploaded through the same USB connection, not requiring any additional Xilinx programming software. A graphical user interface is provided using the Qt[67] environment shown in figure 5.9, offering custom-made interfaces and inter-widget communication using the signal-slot mechanism. Communication with the test system is only initiated after the user interacts with the interface, constant status polling is neither needed nor implemented. For efficient data archiving and visualization, our software uses the ROOT framework[68]. A dedicated data analysis package has been developed in the scope of a different PhD thesis [69] in our group. Additional laboratory equipment like digital multimeters or oscilloscopes can be steered and read out by the application by accessing the GPIB bus or the ethernet interface, allowing automated sweeps involving the ASIC.

The software features easy access to the configuration of the DSSC chip. The software can even

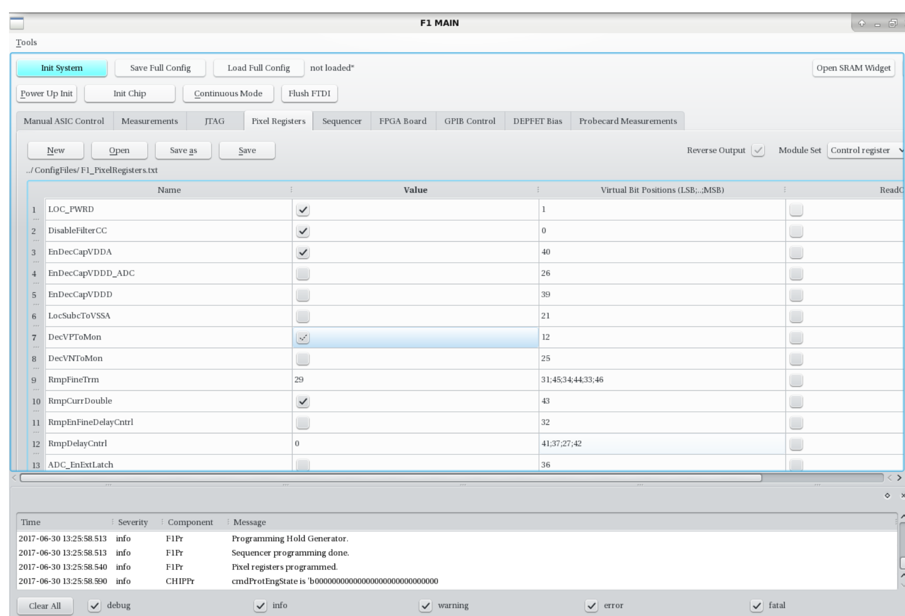

Figure 5.9: Software interface on the host PC connected to the test system interfacing the DSSC readout ASIC. Left: Screen for pixel register configuration. Right: visualization of the pixel register contents as a map.

be easily modified to support several chips, as in the ladder systems, where 16 readout chips are connected in one JTAG chain. After an initial mapping of configuration bit positions to logical configuration registers which can be different in each chip, the software encapsulates the programming details and allows the user to operate on those logical registers. The challenge for the configuration GUI and software is the large amount of channels, in each F1 chip, each of the 4096 pixels has a configuration register of 47 bits length, which are grouped to 31 logical registers, with additional registers in the periphery controlling the global chip operation. The GUI allows the user an easy access to the registers of single pixels, or larger sets of pixels, while automated access through get/set value functions are available as well.

A first implementation as XML structure by the author proved to be useful for small matrix chips, but not scaleable enough for the large pixel matrices of the F1 chip. Manfred Kirchgessner reimplemented the register structure without the overhead of XML, with the full register structure in the memory and simple text file storage.

The software has been structured such that it can be easily reused in different readout systems. This has been driven by the need of a control software for the first ladder prototypes using the final readout hardware (PPT and I/O Board) in a beamline environment. The software is structured in GUI classes for user interaction and underlying classes for data handling and configuration storage as well as classes for the actual implementation of the USB communication (the test system presented here) or the TCP/IP communication in case of the Patch Panel Transceiver.

The data reading from the ASIC test system through the USB channel is included in the software as well. Immediate data plotting is available with several modes. Histograms for individual pixels can be created and the development of data during a burst can be shown. The data of a matrix

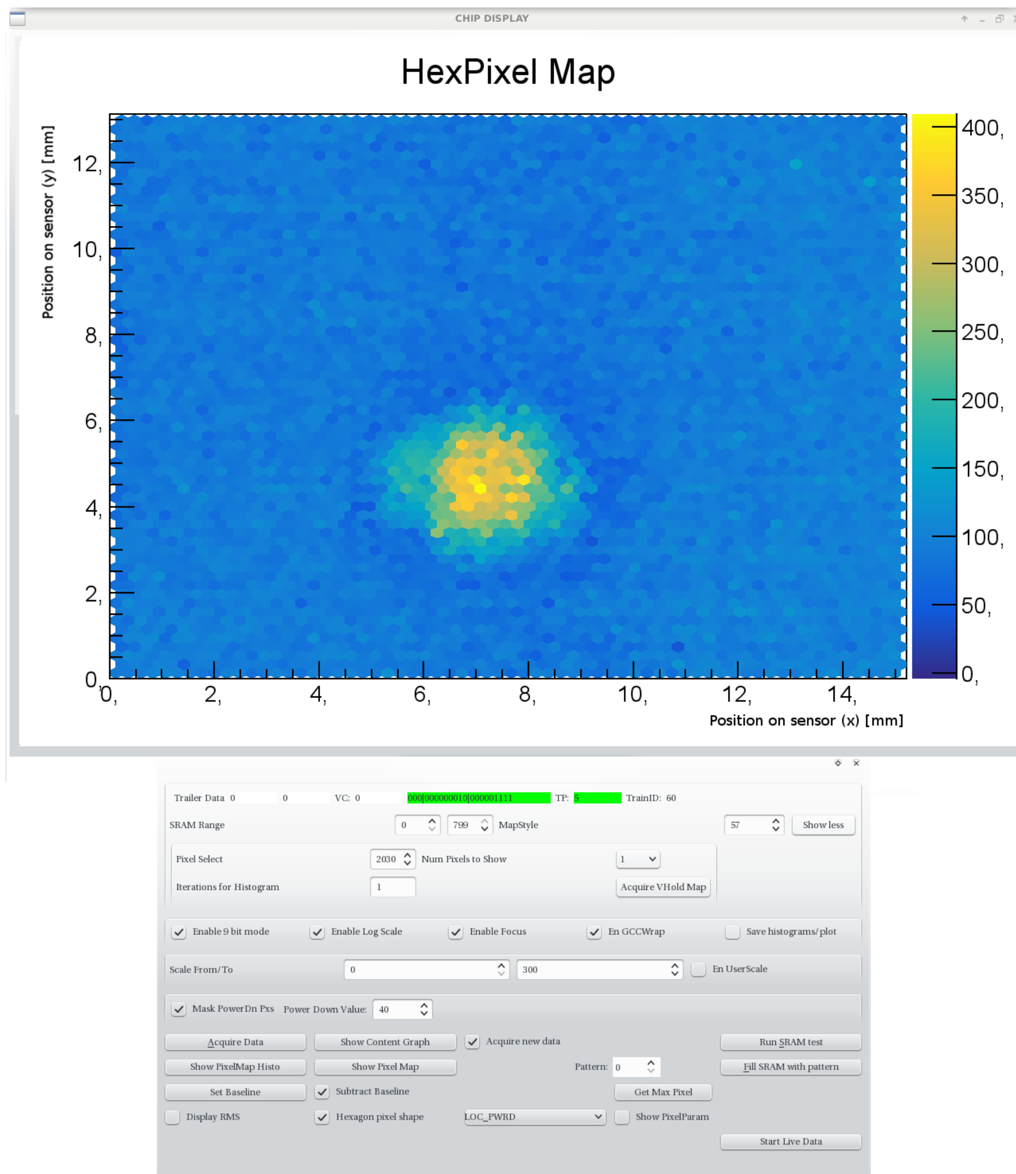

Figure 5.10: Sample illustration in the software. An unfocused laser beam has been directed on an MSDD sensor read out by an F1 ASIC. Hexagonal sensor pixel layout can be selected in the software.

of pixels can be plotted as 2-dimensional maps, featuring either simple rectangular pixels as in the ASIC layout, or hexagonal sensor pixels (figure 5.10). Both memory content and the value ASIC parameters can be shown. More data evaluation algorithms specifically targeted for the DSSC system are available in another data analysis package.

6 ASIC characterization and simulation results

This chapter presents methods and results of the verification process of the electronics design. Specific aspects of the detector readout architecture are highlighted and performance assessments of individual building blocks are shown, with feedbacks given to the ASIC developers pointed out.

6.1 Full format ASIC F1

After a long R&D phase concerning an SDD readout circuit triggered by the unavailability of DEPFET sensors, the large F1 matrix chip has been submitted in 2014. The first full sized matrix chip has been extensively characterized, both standalone and mated with sensors in order to gain information for future improvements. Moreover, a procedure for final module assembly has been developed including known good die selection as a part of this thesis.

6.1.1 Commissioning

In order to bring the ASIC into operation, the global control block needs to be initialized properly through the asynchronous reset and the programming of all registers. Some forbidden combinations of register settings can lead to problems: The SRAM control bits can be set through JTAG and possibly create a short circuit between power and ground. This is the case if the active PrechargeBitBus signal pulls the positive and negative bitline to VDD, while the Write_B signal pulls one of the bitlines to ground (see schematic in figure 4.17). Since the registers are not reset to initial values, but rather come up with random values after power-up, this case can occur but can be resolved by power-cycling. Power-cycling of single ASICs is possible on the final detector modules through the I/O board interface. Moreover, the activation of both the periphery DAC's high range and low range modes creates a current path from analog supply to ground and should be avoided, also rendering the DAC useless.

The differential pads for the clocks, the protocol line and the data link have to be configured properly. The TX common mode voltage can be adjusted in four settings between 490 mV and 750 mV and must fit to the needs of the receiver side, in this case the FPGA, if the data link is DC-coupled. The LVDS standard specifies a common mode voltage of about 1.25 V, but most receivers are tolerant as long as the differential voltage is large enough. The TX bias current, generating the differential voltage at the termination resistor, is adjustable between 1.6 mA and 3 mA, which is a bit lower than the standard value of 3.5 mA. This needs be kept in mind in case of driving high capacitive loads like long cables.

Simple checks for data integrity have been implemented. The test pattern, sent at the beginning of the data stream, is programmed and checked by the software. After the pixel data has been received,

the trailer words containing an XOR bit for each slow-control register as well as the number of vetos received by the ASIC are checked by the software. In case of bit errors while receiving the test pattern or the register XORs, which are compared to the contents programmed by the software, the received data is discarded.

Finally, the sequencer needs proper programming in order to generate the dynamic control signals for the pixels. The cycle length of the sequencer must fit to the master FSM cycle length. The burst length setting controls the number of frames taken. Static values for the IProg phase must be taken into account for proper reset of the filter and the feedback capacitors. For the individual tracks of the sequencer, explained in section 4.2.5, different modes have been developed selectable from the user software. These include debugging modes like ADC-only operation (static front-end signals), buffering of the filter's reference voltage, and the standard operating mode with a reset, two integration phases, and the flipping of the feedback capacitor between the integrations. A mode with only a single integration is available as well, which can be used for analysis of residual currents flowing into the filter.

6.1.2 Power consumption

The F1 ASIC is powered by three nets: The always-on digital net *VDDD_GL* supplying the control logic and SRAM cells, the *VDDD_ADC* for the digital part of the ADCs and *VDDA* for the analog parts of the front-ends and ADCs. The latter ones are power-cycled and only active during the nominally 600 µs long datataking (burst) phase at a 10 Hz frequency.

The static digital net supplying the control logic has a very low current consumption with about 30 mA in idle after programming. During a burst, an extra current for SRAM writing is drawn, which is dependent on the frequency of writing, i.e. the cycle repetition rate. This amounts to about 100 mA at 4.5 MHz and 50 mA in 2.25 MHz mode, being the most notable cases for the final application. After a burst, the data is read from the SRAM cells and sent out on the serial link. The readout architecture is designed such that every pixel reads a word from the SRAM into a register. The registers are connected between the pixels to form a long shift register chain for each column. This way, the readout frequency for the SRAM is reduced to 8.5 kHz. The SRAM reading and shifting the data through the register chains increase the current consumption by only 12 mA.

For the switched nets, the power consumption can be measured by taking the mean current consumption and taking into account the duty cycle, or by measuring the discharge of the capacitors on the regulator board, illustrated in figure 6.1. The regulator board uses two 330 µF capacitors per ASIC supply net which are charged during the 99.4 ms XFEL pause to a maximum of 7 V. During the burst phase, the linear regulator discharges the capacitors with the constant supply current drawn by the ASIC (and the negligible regulator supply current of about 1 mA), resulting in a linear decrease of the voltage across the capacitors. In order to reduce power dissipation, the start voltage should be minimized to a value sufficient to the desired burst length.

The total current consumption has been measured to 2.9 A on the analog supply net and 1.3 A on the ADC supply net at a chip input supply voltage of 1.3 V. The simulated distribution of power consumption with respect to the individual pixel building blocks has been summarized in table 6.1. For the dominating analog supply, the main contributors are the analog filter and the analog parts of the ADC (current source and comparator), which make up 85 % of the current drawn.

The usable number of frames in one train is limited by the 660 µF capacitors on the regulator board supplying *VDDA*. These are charged up to 7 V, the ASIC discharges them to about 2.5 V with

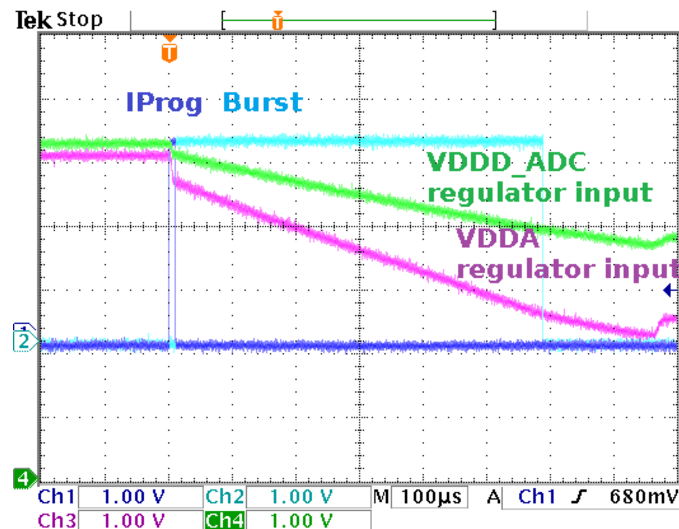

Figure 6.1: The ASIC power consumption can be measured through the discharge of the regulator capacitor bank. Here, during the current request, the 660 µF capacity for *VDDA* is discharged from 5 V to 2.5 V in about 710 µs.

approx. 2.9 A. This gives a maximum on-time of

$$t = \frac{CU}{I} = 1.02\,\text{ms}. \tag{6.1}$$

The time needed for the current programming (around 100 µs) must be subtracted. At 4.5 MHz framerate, a maximum number of 4000 frames can be taken. Another notable case is 10 µs long cycles including a long flattop for signal injection methods e.g. for calibration, resulting in only 90 usable frames. For the prototype development systems, additional capacitors can easily be soldered in order to increase the number of frames usable for the user.

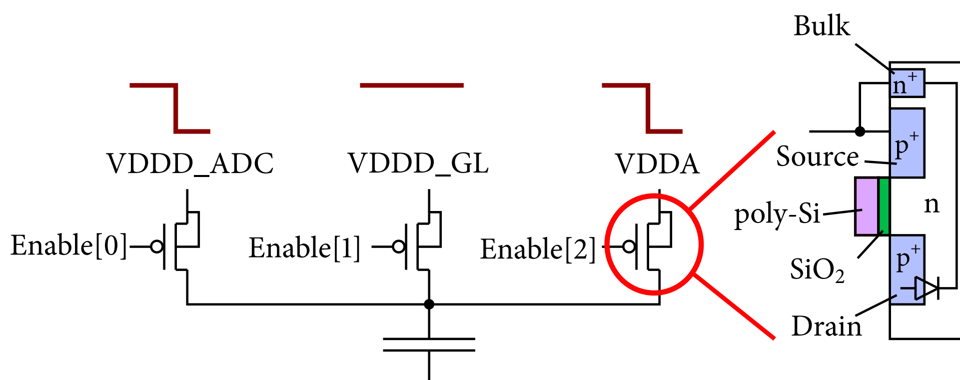

Figure 6.2: The in-pixel decoupling capacitor can be switched to either supply net. The drain diode in the switches for the cycled nets causes an increased current flow, if the *VDDD_GL* switch is active.

Supply (1.3 V)	Building blocks		Total (4k px.)	
	I_{sup} [mA]	Power [mW]	I_{sup} [A]	Power [W]
VDDA (analog cycled)			3.27	4.25
per pixel	0.799	1.039		
Filter	0.388	0.504		
ADC	0.303	0.394		
MSDD_FE	0.100	0.130		
Reference, per half row	0.008	0.010		
VDDD_ADC (dig. cycled)			1.13	1.46
per pixel	0.275	0.358		
GCC & TX, per column	1.152	1.5		

Table 6.1: Distribution of power consumption of the pixel building blocks and periphery circuits for the power-cycled nets (values from simulation) [44].

After power-up, a troubling amount of current is flowing on the constantly-on *VDDD_GL* net. This is caused by an error in the design of the decoupling cap switches (figure 6.2). The positive side of capacitors connected to the always-on *VDDD_GL* supply are shorted to the other supplies through the diode between the drain and the bulk contact. After initial power-up, the control registers are undefined, and some capacitors are connected to *VDDD_GL*, causing a large current flow from *VDDD_GL* to the other supplies. A solution for the F1 chip has been found by programming the pixel registers to a safe state while shortly powering up *VDDA* and *VDDD_ADC*, whereas in future ASIC revisions the bulk contacts of switches to the cycled supply nets will be connected to the always-on net.

6.1.3 Power grid

Being the first large matrix chip submitted in this topology for the DSSC design, the feasibility of supplying the large current requests while maintaining a sufficient pixel supply voltage over the full matrix was studied on F1. As shown in figure 6.3, three requirements make it a necessity to distribute the power in a comb-like structure, with a 'tooth' in each of the 64 pixel columns, spanning over a total length of 1.3 mm:

- Power to the pixel matrix has to be delivered through the periphery bumps located along one side of the chip only.
- Three power and ground nets have to be delivered to the pixel matrix.
- Narrow edges next to the pixel matrix do not allow further low-resistivity metal connections on the sides.

The drop along one column of N pixels can be estimated by treating each pixel as a constant current source with a resistance to each neighbor. At the first pixel, the current for N pixels flows through the resistor ($\Delta V = NIR$). The next one carries a current of $(N-1)I$, and so on. This results

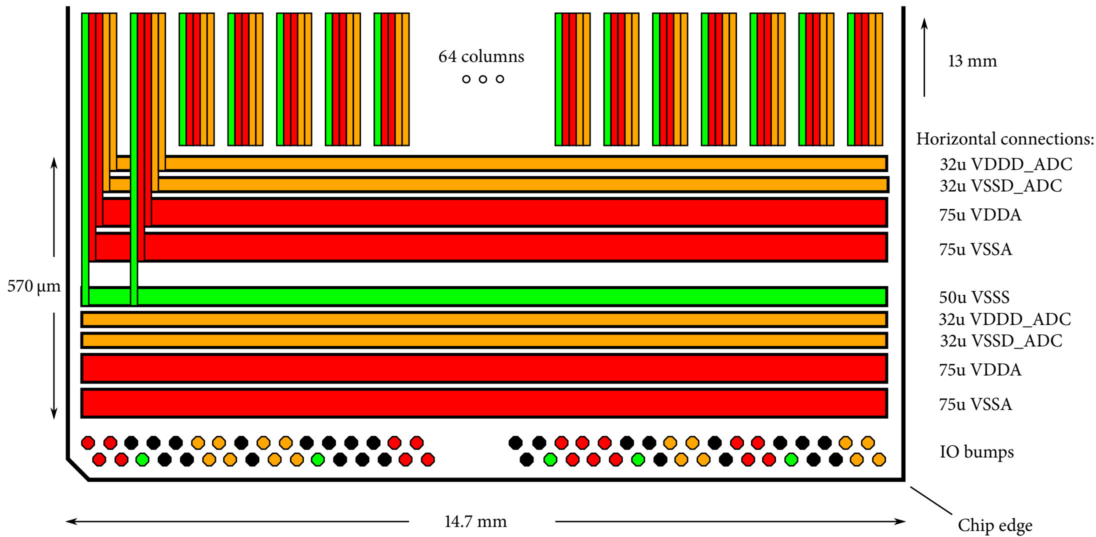

Figure 6.3: Simplified sketch of the comb structure for distribution of the power from the peripheral bumps to the pixel columns. Vertical interconnections are realized on a second low-resistivity layer and are partly omitted for clarity. The space for horizontal connections is mostly filled.

in a total drop along a column of N pixels:

$$\Delta V_{col} = \sum_{i=1}^{N} iIR = \frac{N(N+1)}{2} IR \tag{6.2}$$

For the *VDDA* case with a per-pixel current of 680 µA and 30 mΩ resistance, this results in a drop of 84 mV along a column, combined for the power and ground lines. The width of the *VDDD_ADC* supply line, drawing less current, has been designed to result in a similar drop.

In order to study the distribution in more detail, the local supply and ground voltage in each pixel has been measured. Both positive and negative terminal of the decoupling capacitor in the pixel can be connected to the monitor bus, where each of the three supplies can be switched to the capacitor. The resulting mean voltage on the monitor bus during the burst has been read using a digital oscilloscope.

The results of the measurements are shown in figure 6.4 as a map of the supply voltage in each of the 4k pixels on the chip. The left plot shows the analog supply, being sensed in the lower left edge of the chip. Here, a maximum difference between pixels of 110 mV has been measured, with a large horizontal component. The pixels on the right edge of the matrix have a significantly (about 40 mV) lower supply voltage compared to the row's maximum. The drop along the columns is slightly smaller than the expected value at 60 mV.

Figure 6.4 (right) shows the ADC's switched digital net across the chip with a more severe condition. The lowest supply voltage at the top center of the chip is only at 1.1 V. The maximum drop is 180 mV to the pixel closest to the sense point at the lower right edge of the chip. Again, the drop along the columns is as expected around 50 mV.

A careful simulation taking into account the bump positions and the horizontal and vertical interconnection resistances has been set up to confirm the measured supply distribution in theory.

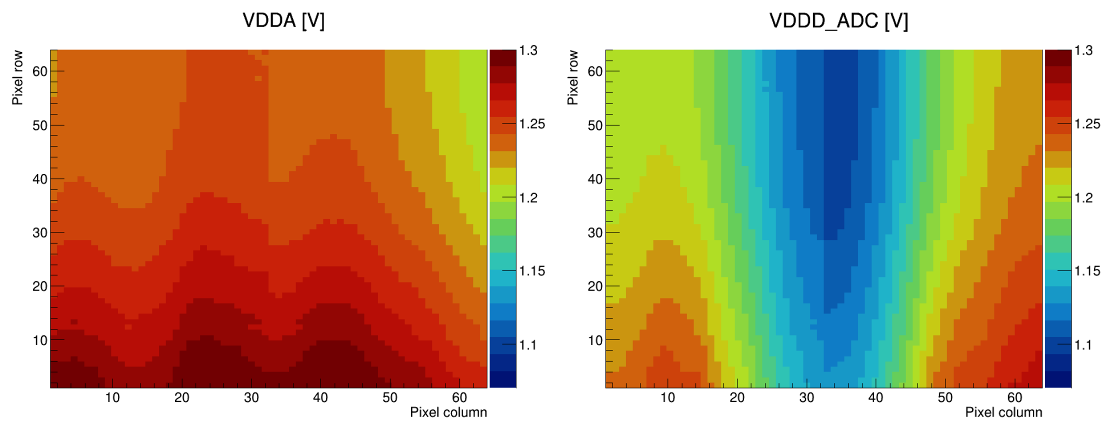

Figure 6.4: *VDDA* resp. *VDDD_ADC* measured on the chip, ground raise included.

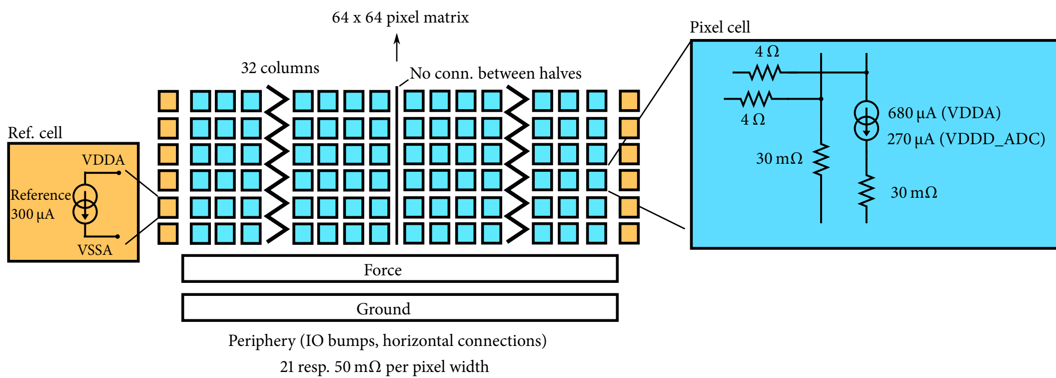

Figure 6.5: Simulation model for the power distribution simulation. The IO bumps are modeled as voltage sources supplying the 1.3 V input at their design positions.

A simulation including the layout would be extremely time-consuming for such a large matrix of components and complex metal layout. A simpler simulation model has been developed, sketched in figure 6.5. Each pixel is interpreted as a constant current source drawing 680 µA with vertical and horizontal resistances for power and ground lines. The horizontal wiring between the pixels is routed 5 µm wide on Metal 6 with a high sheet resistance of $R_s = 0.089 \pm 0.014\ \Omega$/square, resulting in a 4 Ω resistance between two pixels. Along the column, both Metal 7 (E1) and 8 (MA) are used with lower resistivities. While the layout for E1 is not an ideal rectangular shape[1], a mean width of 22.5 µm can be assumed, resulting in 30 mΩ per pixel length.

On the left and right side of the pixel matrix, a reference circuit for each row is drawing current from the *VDDA* net of the pixel next to it. These circuits are modeled as current sources as well, drawing 300 µA per row.

In the periphery, MA is used for the horizontal connection. The metal for *VDDD_ADC* has a total width of 32 µm (50 mΩ per pixel width), while *VDDA* is using 75 µm traces (21 mΩ per pixel

[1] caused by MIMcap connections

width), which have been scaled with the expected current per pixel. For every column, a GCC counter and 12 drivers for the transmission lines (eight timestamp bits and four dynamic control signals) in the periphery creates the timestamps for the ADCs, modeled as a 3 mA current source.

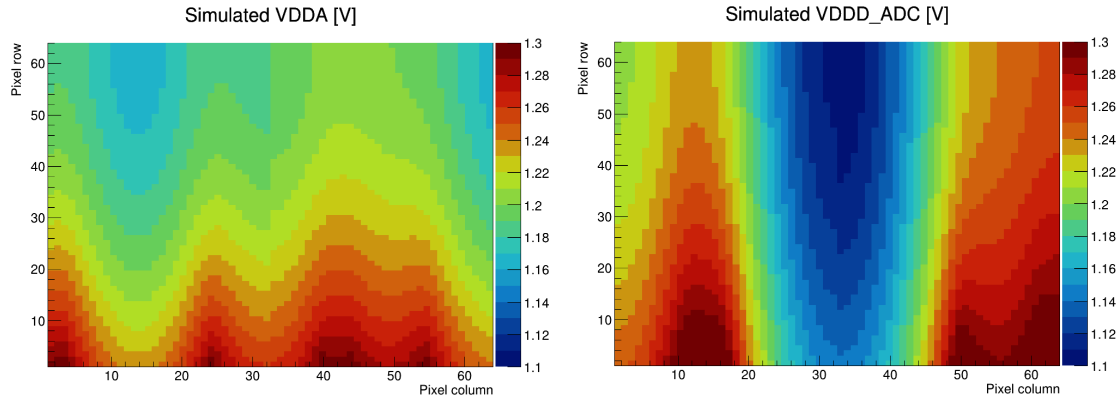

Figure 6.6: Simulated distribution of *VDDA* (left) and *VDDD_ADC* (right), ground raise included.

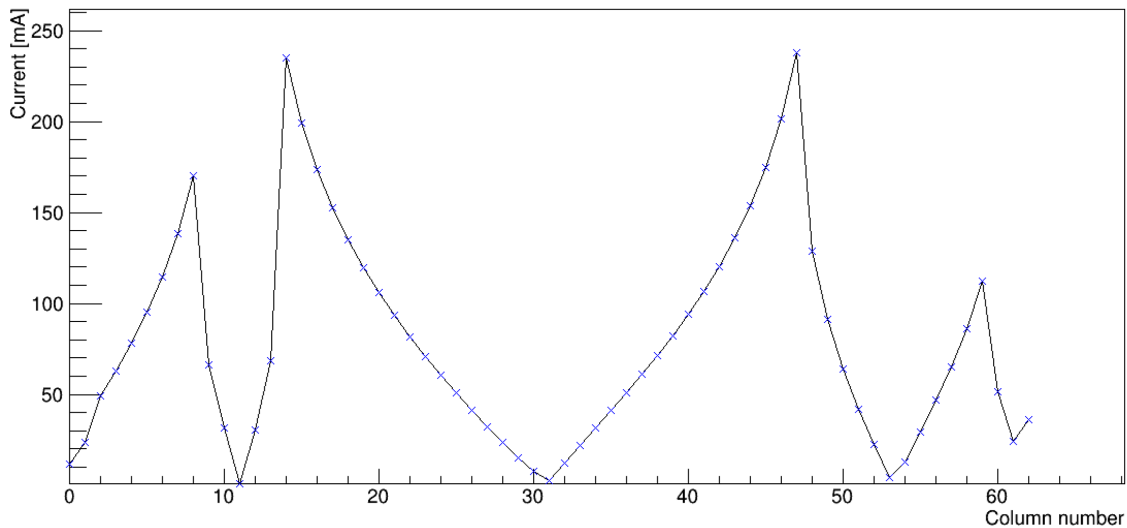

Figure 6.7: Simulated supply currents flowing in the periphery for the *VDDD_ADC* case. The bumps located at columns 14 and 47 serve all columns in between, resulting in up to 240 mA flowing locally at the bump position.

The resulting supply voltage distributions are shown in figure 6.6 for the analog and the ADC supply. Similar shapes and voltage drops could be reproduced in simulation with local differences between simulated and measured values up to 100 mV, explainable by the assumptions made in this very simple model. In any case, the supply currents flowing through the horizontal periphery, depicted in figure 6.7, reveal the real, unexpected problem of supply voltage distribution in the given topology: the supply current for several long columns has to pass through narrow busses in

the periphery. Consider the *VDDD_ADC* case in figure 6.3 with 32 columns in the center of the chip between two power supply bumps. The supplies are not connected between the left and right half in the pixel matrix. We can therefore assume that the supply current for 16 columns thus has to pass through the periphery, causing the voltage drop along the way.

Decreasing the resistance in the horizontal connections is not possible, since all the available space in the periphery is already filled on MA, while E1, the second layer with low resistivity, is used for vertical connection to the bumps. All bumps not needed for control or readout are already assigned to power or ground nets, so only a redistribution of the net assignments is possible and has been realized on the recently produced successor ASIC. Since the module development is very well advanced, every change on ASIC level also requires expensive changes on the mainboard and the test equipment.

A little extra space for horizontal connections could be gained by increasing the die size in the next chip generation by 130 μm, allowed by a margin in the module design. The increased die size will however mainly be used to double critical bumps in order to increase reliability of the module assembly process.

6.1.4 Global Voltage DAC

The F1 chip features a high precision 13-bit DAC, explained in section 4.2.4, for the purpose of ADC characterization, and for setting the reset voltage for the MSDD front-end. The performance of the DAC has been checked with an external voltmeter with main focus on the overall linearity. The LSB current cells have been switched on in a common centroid way to reduce mismatch effects.

The low range mode, achieved by sending the current from the PMOS sources to a resistor to ground, is shown in figure 6.8 (top). The residual voltage of ≈ 10 mV at the lower end of the scale is caused by leakage currents from the pixel matrix flowing through the resistor, resulting in an offset voltage. For voltages above 0.7 V, the current sources are losing overdrive voltage, causing a non-linearity up to 330 LSB.

The high range mode on the other hand is realized by mirroring the current in an NMOS current mirror and converting to a voltage by a resistor to the positive supply rail. In this case, the simple current mirror goes out of saturation for decreasing output voltages, resulting in a large INL error below 0.8 V.

The average step per DAC setting is 110 μV in both modes, resulting in about 28 settings per ADC bin at the nominal bin size of 3.125 mV. The DNL is in both modes below ± 4 LSB for ≈ 80 % of the steps.

The overall INL for a rail-to-rail operation can be improved by switching the DAC modes at a suitable value. Switching at an output voltage of 0.6 V provides a rail-to-rail response with an INL of ± 20 LSB over the complete ADC input range of 0.2 to 1 V, with a very good INL of ± 2 LSB around the ADC reference.

A crucial point for high-precision measurements with the DAC is the temperature dependence of the output voltage. The resistors in the output branch (see figure 4.18) are the main contributor with a temperature coefficient on the order of 10^{-3} per 10 °C. This is primarily a concern for the test setups for ASIC prototypes, while the final detector will be cooled to a static temperature.

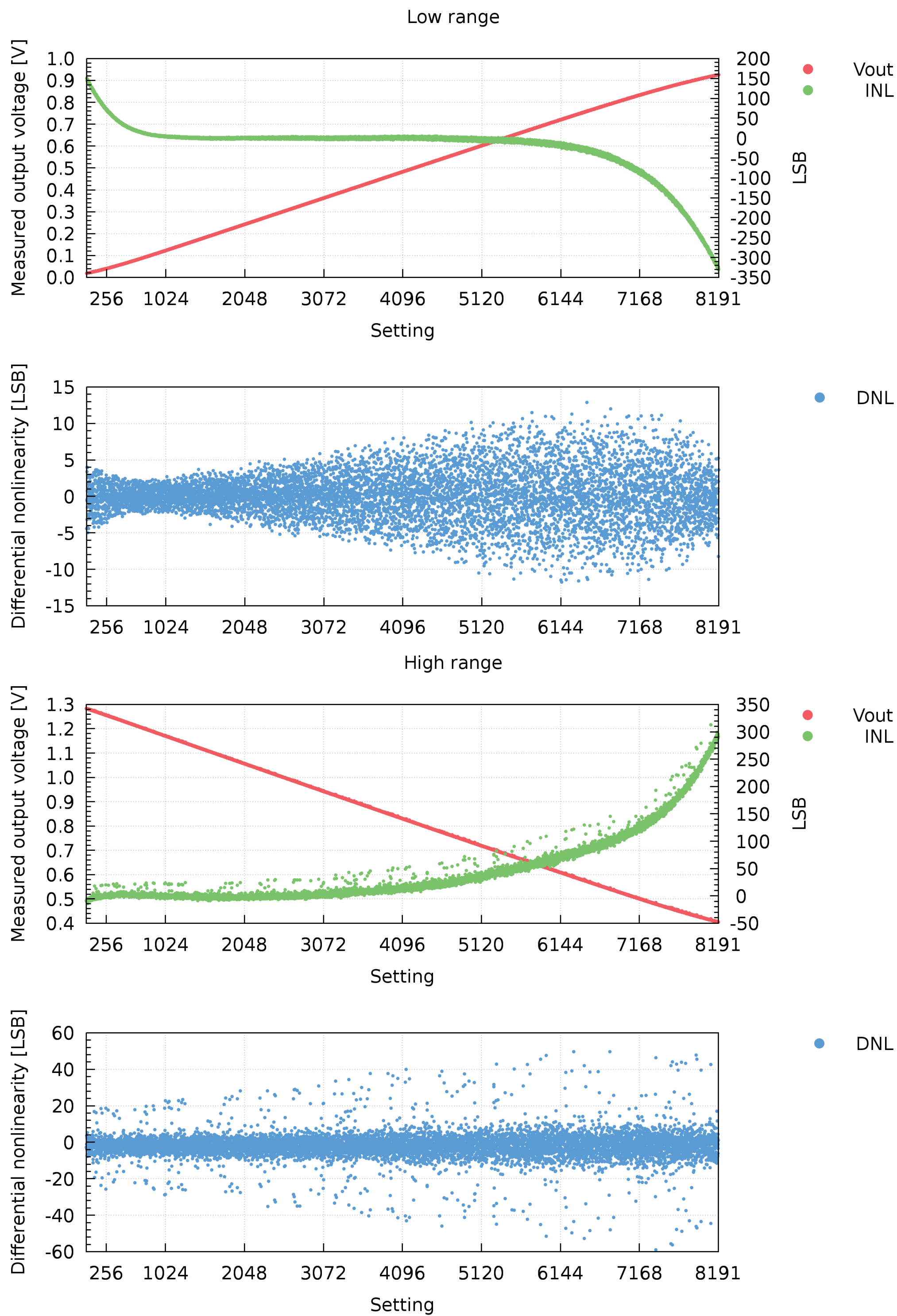

Figure 6.8: DAC output and linearity figures in low (top) and high (bottom) range mode. The low range mode linearity is limited by the PMOS current sources going out of saturation for high voltages, while the current mirror used for the high range mode loses overdrive voltage for low output voltages.

6.1.5 ADC

In the highly integrated matrix chip, analysis of the front-ends is mainly done through the in-pixel ADCs. A proper understanding of the ADC behaviour is therefore needed for any attempt to characterize the front-ends. ADC characterization and trimming work has been a joint effort of the DESY and Heidelberg groups and has been published in [70].

Analog domain and GCC counter architecture

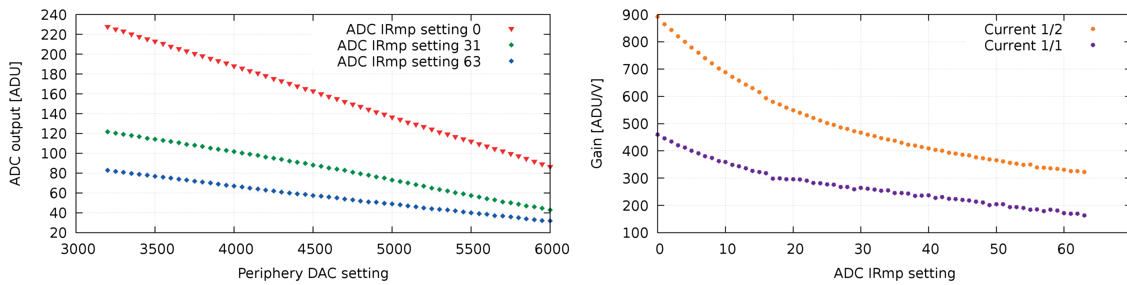

Figure 6.9: Left: Scan of the ADC output by applying input voltages from the periphery DAC. A fit of the data results in the ADC gain for each setting, plotted on the right. Both ranges of the gain are overlapping.

The ADC's gain can be changed through the adjustable current source for the ramping current (figure 4.16). By applying known voltages from the periphery DAC to the ADC input, the gain can be measured for each ramp current setting. The low-range mode of the DAC is especially suited for this purpose, with a wide linear regime with an INL well below 16 LSB between codes 2000 and 6000. The result is shown in figure 6.9. The switchable current sources are binary scaled, so the ramp current is proportional to the digital setting number. The gain is inversely proportional to the ramp current, visible in the $\frac{1}{n}$ curve shape. From the formula for the capacitor discharge, the time needed for the conversion can be calculated to $t = \frac{C}{I_{Rmp}} U$, showing that the ADC gain both depends on the capacitor size and the ramp current. Only both of them can be measured together.

An automated trimming procedure for the ADC gain has been implemented by the DESY and Heidelberg groups. Again, the Global DAC is used to generate input signals for the ADCs. This can be done fully parallel, although the high ohmic DAC output stage can not charge 4096 ADCs directly - each pixel has to buffer the monitor bus using the filter amplifier in buffer mode. This can be realized (compare section 4.2.1) by activating the filter reset (DDYN_Reset active) while keeping the filter flip signal constant and deactivating the integration signal (DDYN_SwIn low). This effectively shortens the filter output to the negative terminal, realizing a non-inverting amplifier. Several voltages are digitized at 4.5 MHz speed, the results written into the in-pixel SRAM and read by the PC. The resulting gains are compared to the target value for each pixel. The current sources are readjusted according to the comparison.

Figure 6.10 shows the result for an F1 before and after the trimming procedure. The left distribution before any trimming shows 20 % deviations from the nominal gain with a strong horizontal dependency and a step between the halves. This is caused by horizontal voltage drops between the references at the left and right sides of the matrix and the pixels.

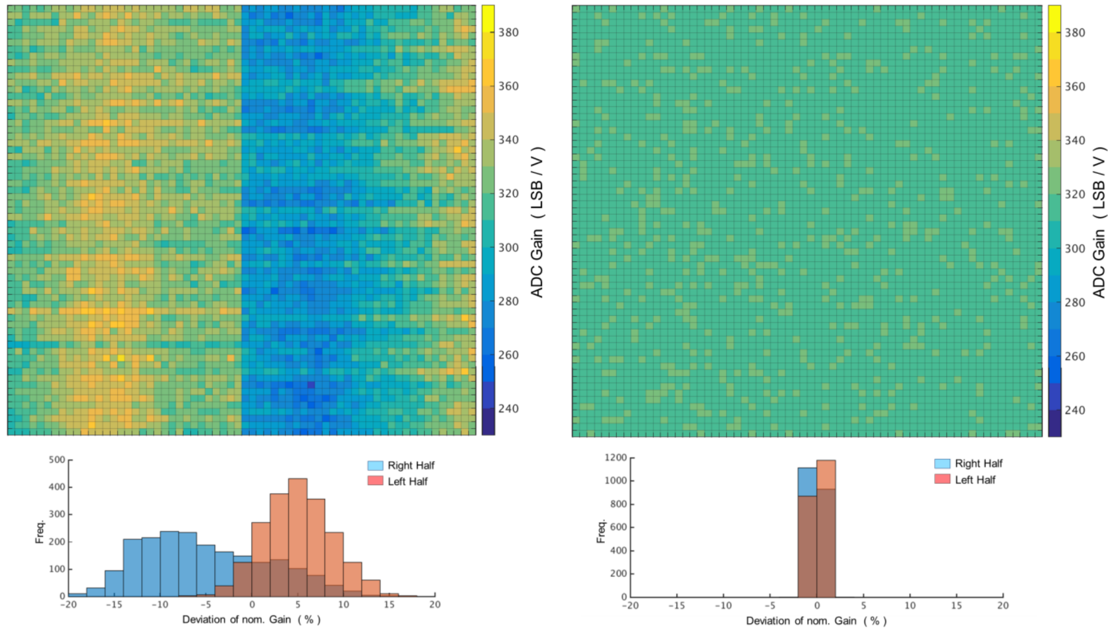

Figure 6.10: ADC matrix trimming results. Left: ADC gain before trimming, where the nominal setting has been programmed in each pixel. Right: Situation after trimming the I_{Rmp} current source individually for each channel.

In the right half, the bias voltage from the reference is lower due to the voltage drop in the right-most column, where the reference circuit's power supply is connected. In the pixel, a PMOS generates the ramp current with the reference voltage at its gate and the (locally higher) *VDDA* at the source, thus the local I_{Rmp} is higher in the pixel, leading to a faster latching and thus a smaller ADC gain. Conversely, in the left center of the matrix, a higher gain is obtained. Here, *VDDA* in the pixel is lower than on the left edge, where the reference for the left half is located, resulting in a smaller I_{Rmp}.

The per-pixel gain trimming results in a standard deviation of the slopes below 1 %. Maximum deviations across the matrix are below 2 %, in accordance with the designed gain resolution of 2 %.

In order to properly assign single photons to specific ADC bins in the sensor's linear range (section 4.2.2), a high sensitivity for these first ADC bins is most important. Any bin width deviation in this range causes bad bin assignments. The differential nonlinearity has been evaluated for the first 25 ADC bins by digitizing the output of the global voltage DAC in high range mode, where the nonlinearity of the DAC is below 5 % of an ADC bin. For each pixel, the DNL is evaluated and shown in figure 6.11 (left). While the mean DNL over all pixels is approx. 0.3 LSB, the worst pixel shows a DNL of 0.8 LSB. Generally, the DNL increases from the chip bottom, the location of the gray code counters and transmitters, to the top, far away from the transmitters. Detrimental effects of the supply voltage distribution can be excluded, as the large drop of *VDDD_ADC* in the chip center does not affect the DNL. It is assumed that the transmission lines for the Gray code bits suffer from mismatch along the columns.

The integral nonlinearity (INL) is expected to be very low, being mainly affected by the clock

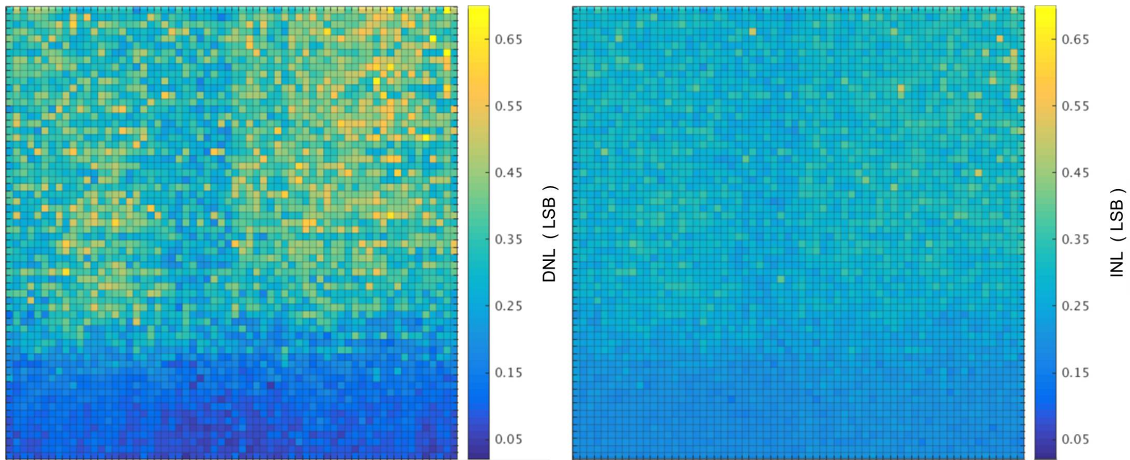

Figure 6.11: Differential and integral nonlinearity of the F1 pixel ADCs in the first 25 bins. An increase of the DNL towards the top of the chip is visible. The INL is well below the quantization limit of 0.5 LSB for 99 % of the pixels.

stability (jitter below 0.5 % of a clock period), the voltage coefficient of the S&H capacitor (on the order of 10^{-5}), and the stability of the current source. The result of the INL measurement on the full matrix, shown in figure 6.11 (right), is homogenous across the pixel matrix with 99 % of the ADCs within the quantization limit of ± 0.5 LSB within the first 25 LSB.

Noise and binning

The ADC noise has been determined using the pixel-internal reference voltage as the ADC input signal. With the filter in buffer mode, a very low-noise voltage can be realized in each pixel. The digitization of the reference voltage is equivalent to a dark image (0 photons) when including the front-end.

By sweeping the pixel-delay offset steps, the output value is moved through the first 1.5 ADC bins with a resolution of ≈60 ps. By moving the distribution across a bin edge, the noise can be determined as a function of pixel-delay steps. By including the measured pixel-delay step width, the input-referred noise voltage can be calculated. A mean value of 250 µV or 8 % of the bin size has been determined across the matrix.

In-pixel counter type

A different approach to the ADC counter has been tested on a small scale test chip L1, comprising a 8 x 64 pixel matrix and thus full columns as on the F1. As explained in the last section, the quality of the DNL across the matrix depends on the equality of the individual bitlines. Mismatches between transmitters, receivers and between the long waveguides introduce switching deviations between individual bits and therefore bin width deviations. In the new approach studied on L1, only the 695 MHz clock is distributed along the columns, with a counter embedded in each pixel. By synchronizing the comparator output with the clock, a Gray counter can be avoided in favor of a smaller-space ripple counter. The DNL of the counter then only depends on the quality of the clock signal received in the pixel.

Studies in [69] and by the author have shown that a mean DNL of less than 0.2 LSB on the full matrix can be reached, if the clock is received properly in the pixel. To study this in more detail, the ADC supply voltage for an L1 chip was lowered until a fraction of the pixels showed counting errors. For this situation, the supply voltage has been measured, showing that a minimum supply of ≈ 1.17 V was required to receive the clock properly.

This requirement is especially important in view of power consumption and distribution. As shown in 6.1.3, there is already a large drop on *VDDD_ADC* across the matrix. Changing to an in-pixel counter would increase the current drawn in the pixel from 270 μA to roughly 450 μA and thus drastically aggravate voltage drop problems in the given architecture.

6.1.6 DEPFET Front-end and Filter

Operation, Gain settings

Thanks to the thorough characterization of the in-pixel ADCs, a well understood digitization circuit is available in each pixel. The ADC gain can be easily trimmed across the pixels to characterize the front-end circuits alone. The ADC is not only suited to characterize the output of the filtering cycles, but can be used for diagnostic purposes, e.g. regarding the bias current cancellation.

The bias compensation DAC serves to subtract any bias current in the front-end, either from the DEPFET or a standing current in the MSDD front-end. The variable branch, with the potential to subtract up to 38 μA, is set before the datataking by setting the gate voltage V_{hold} of an NMOS cascode transistor according to the residual bias current flowing into the filter. This is referred to as the IProg phase. A higher V_{hold} relates to a higher amount of current to be sunk by the bias compensation DAC. The coarse setting however must be set beforehand. An iterative solution for proper setting without required knowledge about the current in the front-end branch has been developed.

After the current programming phase, the V_{hold} capacitor is disconnected and left floating. Since the filter directly charges V_{hold}, the voltage is also available at the ADC input and can be digitized. To do so, the ADC start signal is programmed such that a conversion is started right after the programming phase, in the same moment when the V_{hold} capacitor is disconnected. The information about bias current fine-tuning allows conclusions about currents that are not canceled by the DAC, i.e. if V_{hold} is saturated at the positive or negative rail. The digitized V_{hold} is used for off-line analysis and automated proper setting of the coarse DAC code.

In order to set the appropriate filter gain, the feedback capacitance has to be chosen taking into account the photon energy E_γ, the DEPFET's current amplification g_q, the integration time t_{int}, the ADC bin size V_{LSB} and the number of photons assigned to each bin $N_{\gamma,bin}$:

$$C_f = \frac{E_\gamma}{w_{e,h}} \frac{g_q t_{int} N_{\gamma,bin}}{V_{LSB}} \tag{6.3}$$

$N_{\gamma,bin}$ is expected to be usually set to 1, but could be increased for a higher dynamic range or decreased for higher resolution. Figure 6.12 shows a plot of the needed values for C_f as a color scale and the capacitors realized on F1 (and their combinations) as black lines for default values of $g_q = 500$ pA/el., $N_{\gamma,bin} = 1$ and $V_{LSB} = 3.125$ mV. Notable cases for the XFEL application are integration times of 50 ns for 4.5 MHz operation, whereas higher integration times up to 500 ns for 0.9 MHz operation are possible, too. For long integration times and high photon energies, the needed capacitance becomes excessively large. The pixel size on F1 allowed for a maximum capac-

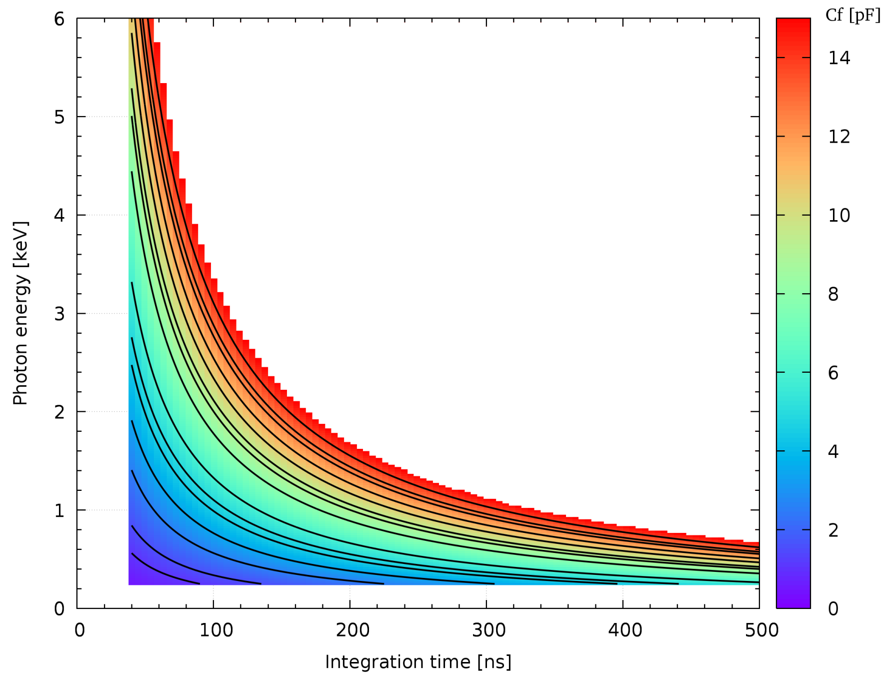

Figure 6.12: Contour plot of the needed feedback capacitance as a function of the integration time and photon energy for default operating conditions (1 bin per photon, g_q of 500 pA/el.). The contour lines are the capacitor values implemented on F1 and their combinations.

itance of 13.8 pF after layout improvements.

As visible in the contour plot and illustrated in figure 6.13, the current implementation of binary scaled feedback capacitors connected in parallel only gives very few settings for high gain operation, while most settings lead to tightly spaced low-gain settings. A different approach of connecting the capacitors serially gives a larger set of operation conditions with higher gains compared to the previous implementation, at the expense of available low-gain settings, which are mainly needed for high photon energies and long integration times.

ADC bin size determination

Another method of measuring the ADC bin sizes has been developed involving the front-end. By increasing the integration time with a signal current injected into the filter, an increase of the signal voltage at the filter output can be generated. The magnitude of the signal increase is adjustable by the signal current, while the method's linearity is given automatically through the digital setting of the integration time. The starting point on the y-axis can be moved by changing the GCC counter's start value. An impression of such a bin size measurement is given in figure 6.14. By using a very low signal current, the ADC bin size can be measured by several 10 points per bin.

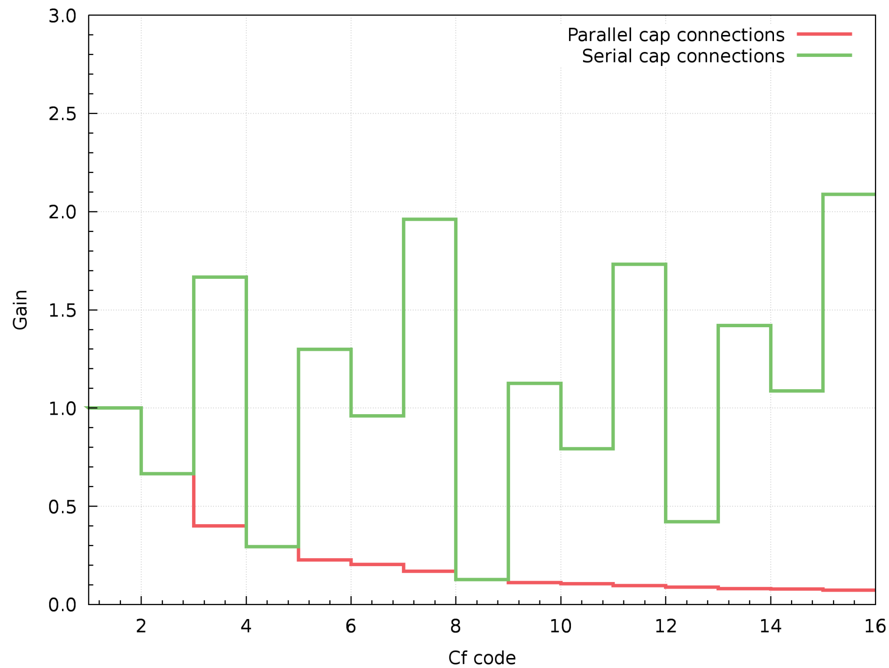

Figure 6.13: Comparison of the realizable gains for parallel and serial capacitor connection schemes. On F1, parallel connections are realized.

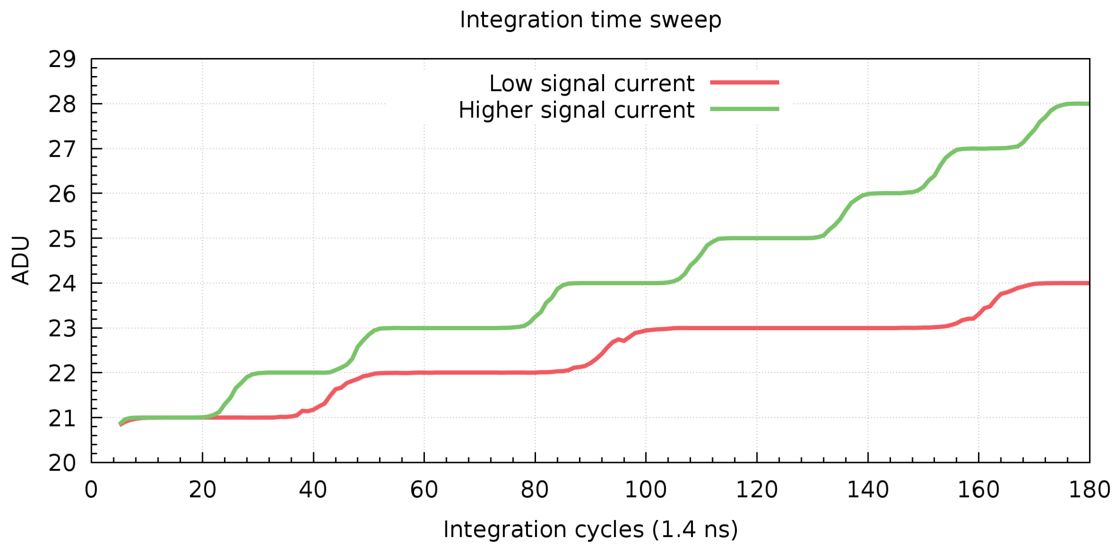

Figure 6.14: Measurement of the ADC bin sizes by changing the integration time. The magnitude of the signal (y axis) can be changed in a wide range through the injection circuit, while the offset can be changed through the GCC counter start value.

6.1.7 MSDD Front-end

The charge readout front-end for MSDD sensors, presented in more detail in section 4.2.1, uses a PMOS input stage with a resistor at the drain node for signal compression. The input node connected to the MOS gate is left floating after reset. The input capacitance is especially important for the circuit, as the signal magnitude is given by the charge generated in the sensor volume creating a voltage step on the input capacitance.

The input capacitance of the F1 front-end has been determined by using the MIM capacitors, which can be connected to the input node, as a reference. By measuring the gain reduction after connecting a capacitor of known design value, the original capacitance can be calculated [44]. On the naked F1 measured on the probestation, the input capacitance of the 4k pixels has been measured to 896 ± 70 fF. After bump-bonding to an MSDD sensor, only a slight increase of 70 fF is expected due to the small contribution of the anode, in agreement with data from smaller test chips. The expected value from front-end design is much smaller at 400 - 500 fF. The additional capacitance is related to the DEPFET cascode PMOS which is also connected to the input node, with the n-well also being unnecesarily connected to the input node.

On a smaller test chip MM6, where the pixel only includes a MSDD front-end and no DEPFET cascode, a smaller input capacitance of 250 fF has been measured. Moreover, the bump landing pad size has been reduced here to reduce the capacitance. The given data will be used in a future full size chip to improve the input capacitance.

Measurements on single pixels

By means of the internal charge injection readily available in each pixel, the proper behaviour and operating conditions of a single channel have been evaluated before going to a larger set of pixels. A check of performance boundaries regarding gain and the achievable dynamic range will be shown here. The magnitude of the front-end's response to a change on the gate node is the main point of interest here.

The bias point, in this case the voltage at the input node at the start of each cycle and thus the current in the input branch, is set by the periphery DAC. Its output voltage is distributed to every pixel through the Monitor Bus and is buffered by a source follower. By changing the periphery DAC setting, the start of the characteristic can be moved. Through the in-pixel injection circuit, a charge can be injected at the input node. This is shown in figure 6.15 for a set of periphery DAC settings, while the extracted gain in the first part is shown on the right. Here, the optimum reset voltage is 750 mV - small signal charges are amplified with maximum gain. The gain decreases for higher amounts of charge, in other words, compresses larger numbers of photons.

Using the design values for all involved components, the g_m at the point of maximum gain can be estimated:

$$g_{m,max} = \frac{\Delta I_{ds}}{\Delta V_g} = \frac{n_{bins} V_{bin} C_f t_{int}}{V_g} \tag{6.4}$$

The estimated value of ≈ 1.3 mS is slightly larger than values from simulations. Deviations apart from component values might be caused from the uncalibrated magnitude of charge injected by the internal injection circuit.

A first glance at the maximum signal detectable by the front-end shows that after 150 injection steps (corresponding to ≈ 2300 keV) the front-end saturates when starting at the maximum gain point. However, this dynamic range is only reachable for settings with relatively low gain at the

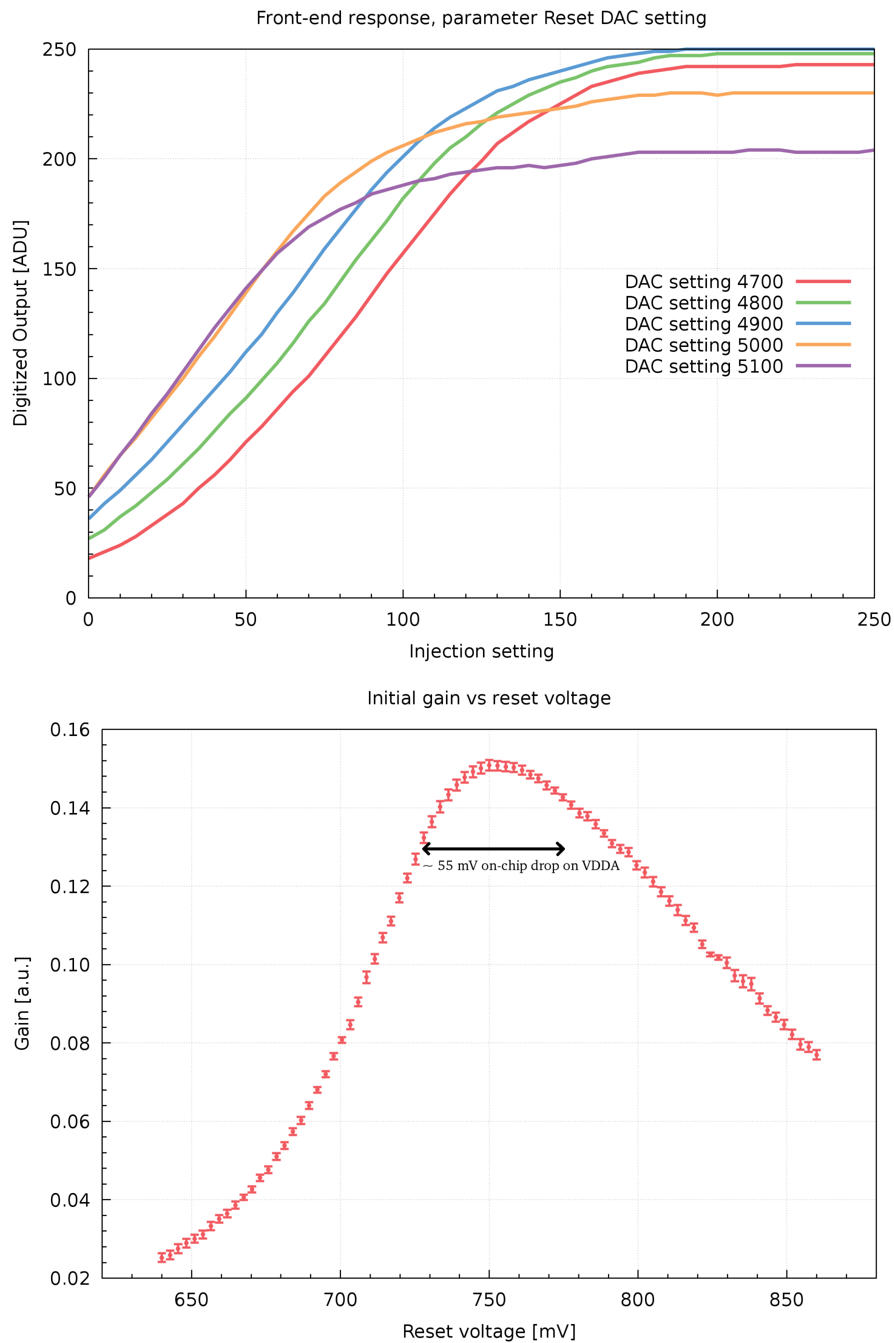

Figure 6.15: Single pixel measurement of the MSDD front-end response. Top: Pixel output as a function of the injected charge at the input, given as the digital value for the injection DAC (parameter: reset voltage). Bottom: The gain in the first part is a function of the reset voltage and the in-pixel *VDDA*.

beginning of the characteristic. The compression sets in very late, in this case, the first 70 injection steps (1000 keV) are basically uncompressed, filling 130 ADC bins. The following 1300 keV are compressed into the next 30 ADC bins. Of course, the front-end gain and ADC settings are in this case not optimized to use the full range of 256 bins, but the measurement already shows that the compression region is very small. More cases will be discussed in the next chapter.

The mean input capacitance has been measured to 0.9 pF. Additionally, extra capacitors (0.2 pF, 0.5 pF and 1.0 pF) can be added to the input, which reduces the voltage step on the input for a given input charge and thus increases the dynamic range of the circuit. The three capacitors result in seven possible combinations with a gain reduction between 22 % and 189 %.

The noise and further parameters of the circuit have been estimated with sensors and is given in chapter section 7.1.

Full matrix measurements

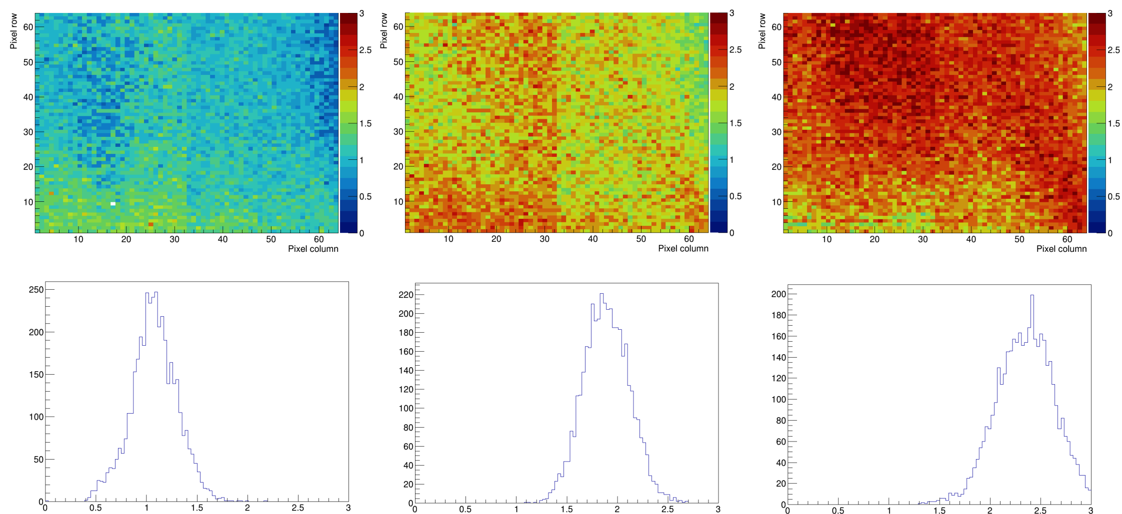

Figure 6.16: Gain of the first part of the characteristic, measured with all pixels running, for decreasing bias voltages. The maximum gain is reached first in the lower left, where the analog supply is highest. By further decreasing the bias, the maximum gain shifts to the upper right part with lower *VDDA*.

The simple design of the MSDD input stage with the transistor's source connected to *VDDA* performs well on single-pixel level, but more serious problems arise on matrix level. Since *VDDA* is not homogenous throughout the pixel matrix, the important front-end gain for the first photons is depending on the local *VDDA* inside the pixel, and therefore on parameters like the pixel position and number of active pixels. Figure 6.16 illustrates this by a map of the front-end gains of the first part while all pixels are active, with histograms attached, for a set of bias settings. For each pixel, the gain has been determined by means of the internal charge injection. In order to minimize crosstalk effects while keeping the measurement time at a reasonable level, sets of 128 pixels have been measured in parallel. From left to right, the bias voltage has been decreased. The ADC gains have been trimmed for this measurement to only see front-end variations in this measurement.

In the left plot at a reset voltage of 783 mV, the gain is well below the maximum, with a distribution similar to that of *VDDA*, with minima in the upper left and upper right parts (section 6.1.3). With decreasing bias voltage, the gain of all pixels increase, with a maximum at the lower left (center plot, reset voltage 728 mV) - the pixels here have the highest *VDDA*, the maximum gain is reached here first. Consequently, the gain in the lower left drops for further decreasing bias voltage, and the pixels across the center of the matrix reach the maximum gain (right, 673 mV). The mean gain across the matrix increases from 1.08 ± 0.23 ADU/Injection step (left plot) to 2.34 ± 0.28 ADU/Injection step (right plot). Tests have validated that the remaining gain deviations can be compensated by changing the filter's feedback capacitor and I_{Rmp} current pixel-wise.

6.1.8 SRAM

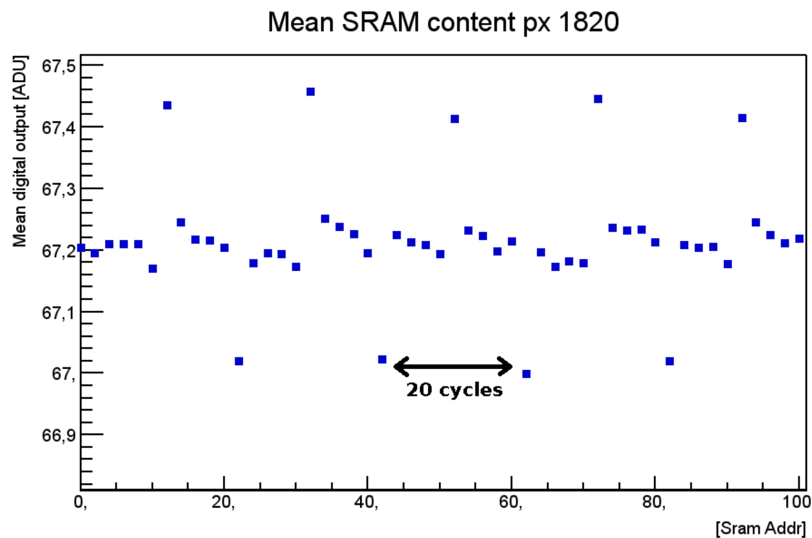

Figure 6.17: Effect of SRAM control lines coupling into analog pixel parts. The repetition rate, in this case, is 20 measurement cycles.

An influence of SRAM write access on other parts of the pixels has been detected by thorough investigations of the DSSC calibration groups. For each individual SRAM cell, a mean value has been calculated as exemplarily shown in figure 6.17. Regular deviations in the sub-ADU range have been spotted. Repetition with frequencies of 20 or 160 cycles have been observed, depending on the pixel position, which can be explained by the SRAM address lines being shared between four pixels. This is visible in both charge and current readout mode. It is assumed that a capacitive coupling of address line enables into sensitive part of FE, probably the filter or the reference, is the cause.

While the exact origin of the effect is difficult to find, it is clear that the routing of digital CMOS-level control signals close to sensitive analog blocks like the front-end is the problem. As a simple mitigation, shielding of the control lines has been added for the next chip revision. More sophisticated approaches like differential low-voltage signaling typically use more space, which is not easy at hand in the dense pixel layout.

6.2 Prototype matrix chips measured before F1

The path to the first large matrix chip has been continuously accompanied with assessment of the performance of the individual building blocks and their interaction. Three small matrix chips called MM1, MM2 and MM3 (figure 6.18) have been submitted and thoroughly tested in the years prior to F1. The individual advances and drawbacks found in these chips are summarized in this section.

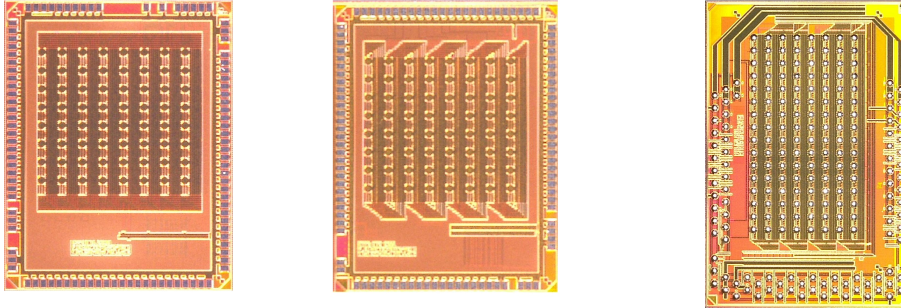

Figure 6.18: Die photographs of the mini matrix precursor chips MM1, MM2 and MM3. MM3 was the first chip bump-bonded to DEPFET mini matrices, demonstrating the low noise readout architecture.

The first mini matrix chip MM1 has been fabricated in 2010. It contained, for the first time, the full DSSC signal processing chain with fully functional integration of all pixel building blocks in the final pixel size. The noise of the wire-bonded 8x8 pixel matrix has been assessed with linear DEPFETs. On-chip decoupling of bias nets has been found to be necessary to reach the noise goals. A suboptimal performance of the ADCs regarding DNL was measured, caused by the ADC transmission lines being wound up in a snake pattern.

The MM2 chip, submitted in 2011, mainly contained improvements in the filter to reduce the filter bandwidth during current programming, and the ADCs, improving the timestamp receivers and returning an error code if the comparator has not latched. The power busses have been routed in a snake pattern along the 8x8 pixel matrix to simulate the voltage drop along a full column of the full size chip. The voltage drops along the snake were found to be compatible to the developed model. Power-cycling of the pixel matrix has been tested without problems. Dips in the ADC transfer characteristic have been found, caused by a timing problem in the interface between the Gray code counter and the differential transmitters. Moreover, the first test of the ASIC with non-linear DEPFET prototypes has been conducted, verifying the increased dynamic range.

Finally, the MM3 chip produced in 2012 was designed to test the bump bond interconnection to a sensor and all periphery blocks of the final chip. The main change was the on-chip digital control block with the minimalistic external interface. The 8x16 pixel matrix included ADC versions with an in-pixel counter and clock distribution on one half, and a conservative GCC approach in the other half. A very good and homogenous noise performance (20 e^- at 370 ns integration time) with bump-bonded non-linear DEPFETs has been measured with this chip. For the fine-tuning of the bias current subtraction, ncaps for the V_{hold} have been tested on this chip, which however showed non-negligible leakage. The subtracted current changed throughout the burst, measurable for long hold times. The internal charge injection of DEPFETs has been tested successfully on this chip for calibration purposes.

7 Commissioning of ASIC and sensor assemblies

The prototype system has been used to evaluate the performance of the F1 readout electronics mated with DSSC-type sensors. Due to the unavailability of DEPFET matrices for a long time, major efforts have been put into MSDD sensors instead. Results obtained with both sensor types will be presented in this chapter. Photons from radioactive decay or from visible light sources have been used to test the performance. In collaboration with the calibration groups from Politecnico di Milano and Munich, an X-ray generator and a proton beamline has been used for detailed characterizations and calibration tests. Selected results from these measurements are presented, a subset of which have been published in a conference record [71].

7.1 MSDD Sensors

7.1.1 Preparation

The ASICs are equipped with SnAgCu solder balls by the fab and have been bump-bonded to sensor prototypes in a reflow process by an external company. Smaller prototypes (mini matrix chips) have been bump-bonded in our institute. The surface quality of the sensors typically defines the quality of the bonding result, with proper cleaning of the pads being mandatory.

After the reflow step, the assemblies are cleaned in an ultrasonic bath and glued along the sides to the narrow edge of the PCB. This way, short and easy to establish wirebond traces can be reached for the readout electronics side of the assembly, at the cost of covering a small part of the pixel matrix at the edge. The wirebond connection for the backside depletion voltage is established in a further step through the hole in the PCB. Different variants can be implemented, such as glueing the ASIC backside to a holder or cooling block. No further mechanics is then needed around the entrance window, allowing to use the full matrix.

In order to test the electrical functionality of a sensor assembly, several tests are conducted. The diode between the n^- bulk and the p^+ sensor backside is checked in an IV measurement. The sensor breakdown voltage, which should be stayed clear of due to the associated avalanche processes, has been measured to be well above 200 V for several samples. The typical depletion voltage has been measured to 100-120 V with a leakage current of about 100 nA. For full size sensors, the backside current is typically in the low nA region at 130 V backside voltage. The increased leakage current is assumed to originate from the handling of the sensors during flipping, movement to storage containers, and finally glueing to PCB and wirebonding. Especially the positioning of the sensor on the PCB and the glueing, which involves mechanical stress on the sensitive backside, probably increases the leakage current.

Moreover, the isolation between the drift rings, separated by the n^- bulk, has been checked. The two drift rings surrounding every pixel shape the electric field on the top of the device in order to accelerate drifting of the charges towards the center anode. In order for this to work, a suitable potential difference must be established between drift rings. Isolation has been tested up to 10 - 15 V. On the sensors tested in the scope of this work, there is a contact called Inner Substrate to the n-doped area between the p^+ drift rings which should not be biased, as this could activate a parasitic p-n-p transistor.

The isolation of the anodes has been checked by measuring the current flowing through the bulk contact, biased at 0 V. As expected, the current vanishes after ramping up the ring voltages and thereby depleting the bulk between the pixels, and between the pixel matrix and the substrate contact. Finally, the diode between the p^+ drift ring contacts and the substrate contact is checked in reverse bias. A typical current of some 10 nA can be expected with breakdown well above 40 V.

7.1.2 X-Ray measurements, noise determination

The total noise of the detector system is usually evaluated by referring the fluctuation of the output to the input charge. The gain of the system therefore needs to be determined using a precise source. Radioactive sources with its emission lines with known energy can be used, for example. ^{55}Fe is particularly suited for the DSSC system case, as the K_α and K_β lines at 5.9 keV and 6.5 keV are in the linear range of the system. Moreover, the readout ASIC is shielded from the radiation of the source by the 300 μm thick sensor, the photons are completely absorbed by the sensor bulk, therefore allowing the use high flux sources without risk to damage the readout electronics.

X-ray fluorescence provides another means of generating photons up to a fixed energy. It describes the emission of characteristic secondary X-rays from a material after illuminating it with a primary X-ray beam of sufficient energy. Concretely, an Yttrium target has been used, with characteristic emission energies at 14.96 keV (K_α) and 16.74 keV (K_β). A sample spectrum using an Y target is depicted in figure 7.1, showing the noise peak, the two lines, which can not be resolved due to noise, and the trough in between. The trough contains events split between pixels, and out-of-time events. Since the photons arrive asynchronously to the ASIC, each photon is weighted according to the trapezoidal weighting function. Only events arriving during the flattop phase are weighted fully.

For the performance evaluation of the F1 MSDD front-end, two different measurement settings have been used:

- In order to check the front-end on its own and retrieve the best case noise, single pixels or up to a window of 100 pixels are activated. Both power and reset voltage are statically applied from a low-ripple power supply. The readout cycle is slowed down to 0.9 MHz with an integration time of 50 ns, with a hold in the flattop of typically 500 ns to increase the probability to acquire photons. The front-end gain is also increased by reducing the feedback capacitance. The ADC gain is maximized by minimizing the ramp current by the current DAC and by setting the CurrentDouble bit to 0, in order to expand the spectrum for a higher resolution for fitting.
- Operation of all pixels is achieved by using the power-cycling operation with a regulator board. An operation resembling the 4.5 MHz operation is set with an integration time of only 50 ns, again with a long flattop of 500 ns, and a large feedback capacitance of 4.4 pF. A higher front-end gain resulted in saturated filter due to large offset currents (see section 7.1.4). Again, the ADC gain is maximized.

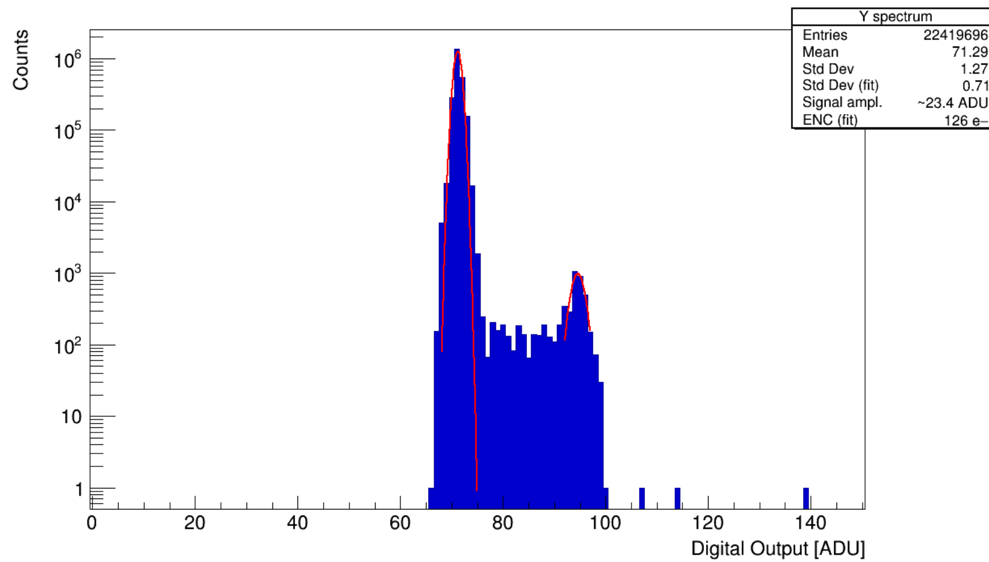

Figure 7.1: Typical spectrum for an Y XRF measurement acquired in window mode. The MSDD front-end resolution is not high enough to distinguish the K_α and K_β lines.

ASIC (pixels)	Measured Noise	Measured C_{in}	ASIC Front-End
MM4 (8 × 16)	130 e^-	≈ 0.9 pF	DEPFET + MSDD
(single pixel)	101 e^-		
F1 (64 × 64)	470 ± 205 e^-	≈ 0.9 pF	DEPFET + MSDD
(single pixel)	157 ± 30 e^-		
MM5 (8 × 16)	52 e^-	≈ 0.28 pF	only MSDD

Table 7.1: Measured noise figures for the MSDD readout with various ASIC variants. Shaping time is 50 ns for all measurements corresponding to 4.5 MHz operating speed. In single-pixel mode, only one pixel in the matrix is powered.

Table 7.1 summarizes the noise measured on several chips. MM4 is a smaller version of F1 comprising only an 8x16 pixel matrix, but sharing the same pixel circuitry. Already in single pixel mode, F1 shows a higher noise of 153 e^- compared to the MM4 with 101 e^-. The assumed reasons are the larger power supply ripple and more switching noise on F1, even if only one pixel is powered. This is caused, for example, by all periphery blocks being powered regardless of the number of active pixels, and by the switching activity of the larger number of digital circuits on F1.

A noise level of 470 e^- has been measured for the full F1 chip using X-ray fluorescence, which is clearly much higher than expected and simulated. The challenging evaluation of the data acquired in this mode has been shared with the DSSC calibration group, which included developing multithreaded fitting algorithms, greatly reducing the calculation time for the 4096 histograms. The resulting noise map and histogram are shown in figure 7.2. The peak of the gain is in this case lo-

cated in the upper right part of the matrix, while in the lower left, a lower gain and thus a higher ENC has been measured, caused by the *VDDA* distribution on the matrix.

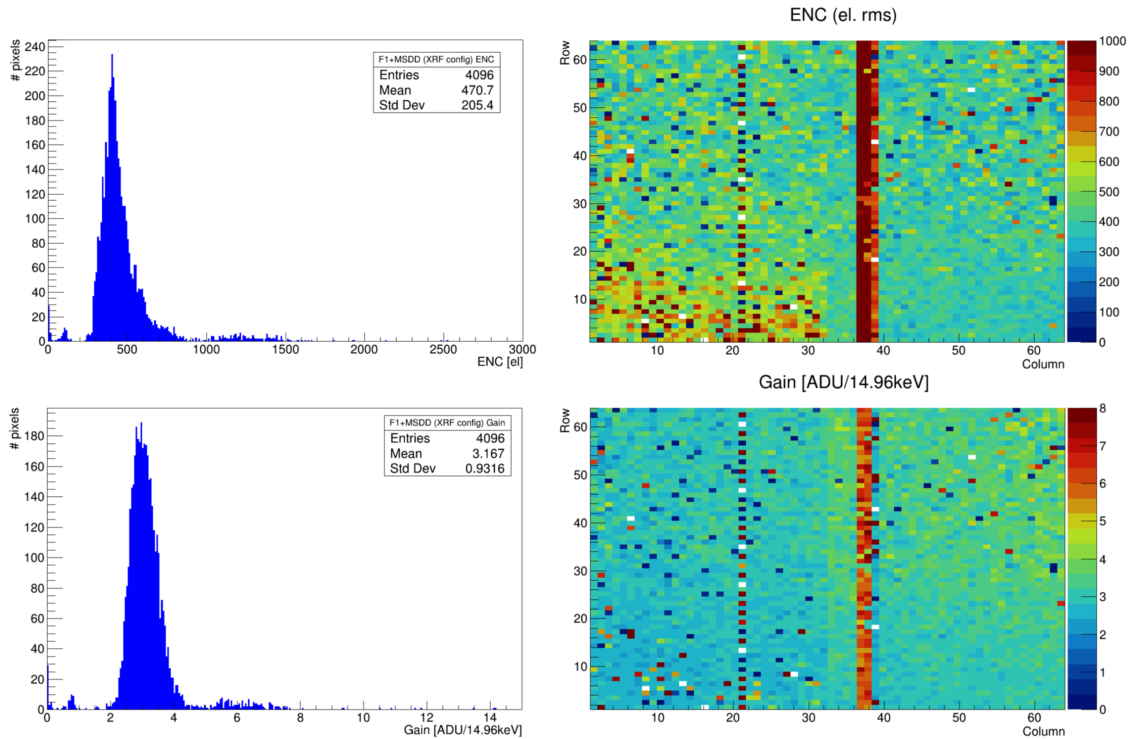

Figure 7.2: Measured ENC and gain of F1 and MSDD assembly illuminated by XRF radiation from an Y sample. Broad peaks at 470 e^- noise and 3.2 ADU / 14.96 keV have been measured on the pixel matrix. The unconnected column (see section 7.1.7) and three not properly working columns are standing out.

In parallel to the full format ASIC development, optimized ASICs dedicated for MSDD readout have been designed. One of these is the MM5 ASIC, which also uses a PMOS input transistor, but with a different signal compression technique and without a DEPFET cascode connection. A noise of 52 e^- has been measured on MM5. The measured noise is significantly lower as expected by the smaller input capacitance C_{in} and the missing leakage from the DEPFET cascode, but the noise associated with power supply ripple does not scale with C_{in}.

7.1.3 Dynamic range

The usage of high-gain settings on F1 proves useful for gain and noise evaluation, but only a very small dynamic range can be reached, since the compression sets in very late, after the maximum number of ADC bins at 4.5 MHz frame rate of 256 has been reached (figure 7.3). By lowering the gain of the system, the triode compression region can be reached, strongly increasing the dynamic range. The main tools used for gain reduction are the doubling of the ADC ramp current and an additional capacitor switched to the input. The following measurement configurations, both using 4.5 MHz frame rate, have been used:

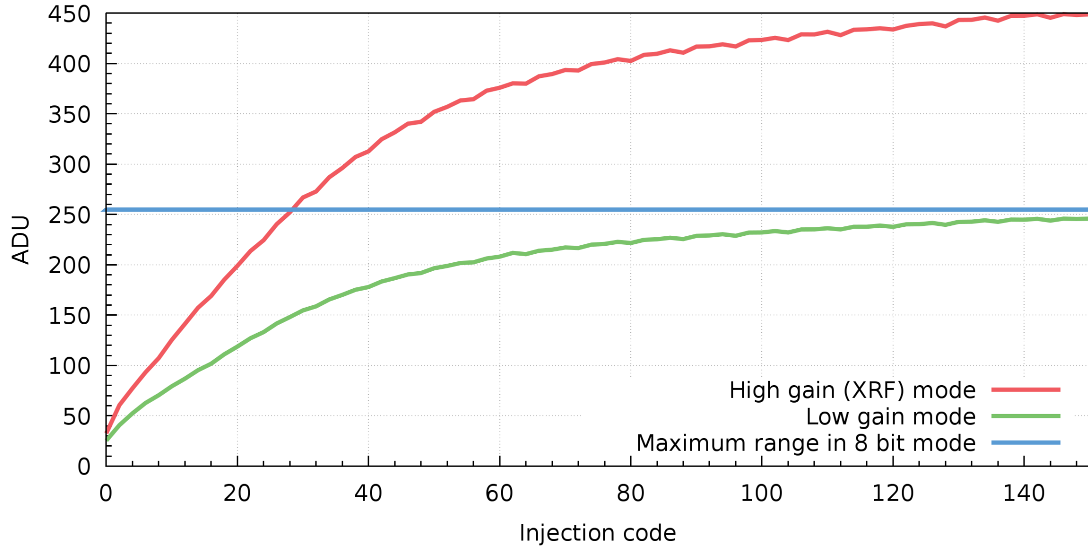

Figure 7.3: Response to high-gain injection for XRF mode (red) and low gain mode (green). Only 256 bins are usable at 4.5 MHz frame rate, cutting off the compression region for XRF mode. Non-linearities are caused by the injection circuit.

- XRF (high gain) configuration: No additional input MIMcap, 35 ns integration time, C_f 4.4 pF, I_{Rmp} trimmed, I_{Rmp} Current Double 0, Flattop hold 500ns
- High dynamic range (low gain, proton) configuration: Input MIMcap 0.2 pF, 35 ns integration time, C_f 4.4 pF, I_{Rmp} trimmed, I_{Rmp} Current Double 1, Flattop hold 500ns

The XRF configuration gives a mainly linear relation between injected charge and front-end output at a gain of 3.8 ± 0.9 keV per bin, resulting in a dynamic range of typically 400 to 600 keV. This mode has been used to measure the absolute gain of the system by detecting the 14.96 keV Y line. The gain in high dynamic range configuration is reduced to 9.37 ± 1.84 keV / ADU. Conversion factors for the gain of each pixel in the two configurations have been extracted from electrically pulsing the backside, which injects charge into every sensor pixel and allows an easy and ASIC parameter independent estimation of the small signal gain.

From the set of measurements above, the maximum dynamic range of the input circuit in units of input energy can be extracted for the low gain mode. Using the internal charge injection in high gain mode, the dynamic range in terms of injection steps can be found ($DR[\text{Inj_code}]$). Using the data from XRF measurements, the energy of one injection step can be calculated ($\frac{g_{Inj}[\text{ADU/Inj_code}]}{g_{XRF}[\text{ADU/keV}]}$). In order to convert this to low gain mode, the conversion factor ($\frac{n_{XRF_mode}}{n_{LowGainMode}}$) has to be applied. The final expression for the dynamic range is:

$$DR[\text{keV}] = DR[\text{Inj_code}] * \frac{g_{Inj}[\text{ADU/Inj_code}]}{g_{XRF}[\text{ADU/keV}]} \frac{n_{XRF_mode}}{n_{LowGainMode}} \tag{7.1}$$

For each pixel, the intersection between the quantization noise and Poisson noise (assuming 1 keV photons) has been extracted. The result for the pixel matrix is shown in figure 7.4. As expected, the distribution is very broad (1986 ± 810 keV). Pixels in the upper right of the matrix with a start of the

response well below the maximum gain point tend to have a very high dynamic range and run into the nonlinear part of the injection circuit. In case nonlinearities have been detected in the data of a pixel during the evaluation, it has been excluded from further evaluation, indicated by the white color.

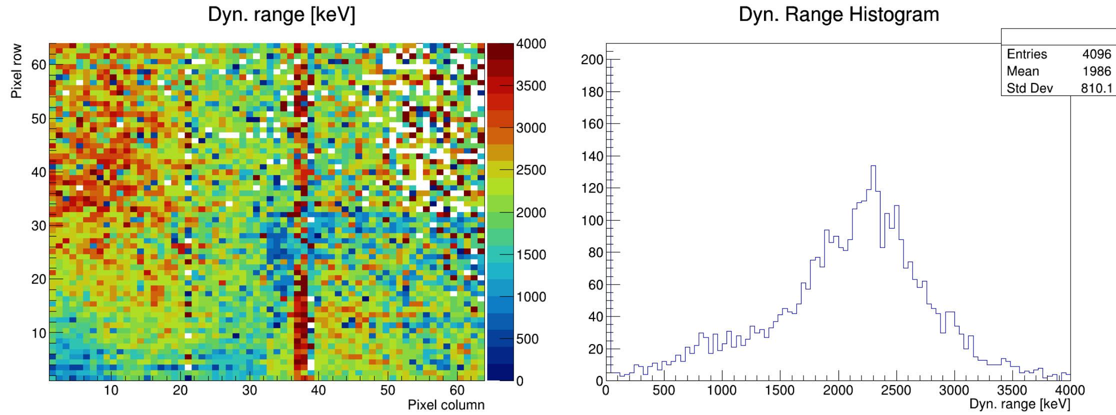

Figure 7.4: Map and histogram of reachable dynamic range with MSDD sensors and F1. The limit of the dynamic range for each pixel is given by the quantization noise reaching the Poisson limit.

7.1.4 Challenges of matrix operation on F1

Further increases of the MSDD front-end gain by an increased integration time or reduced feedback capacitance are not possible on F1. This is caused by a residual current flowing into the filter and saturating it for high gain settings. Variations on the *VDDA* supply current request throughout a cycle, and, more severe, variations between the current programming and the burst phases, change the current flowing in the input branch, while the current set in the bias subtraction DAC is fixed. The changing current consumption of the filter, illustrated in figure 7.5, is caused by a dependency of the current consumption of the filter output stage on the output voltage.

Through the finite resistance on the supply lines, the changing current request causes changes in the pixels' local *VDDA*, which leads to a change of the bias currents and therefore a wrong fine-tuning of the subtracted currents, in other words, a large residual current. The residual current saturates the filter in case a high filter gain is selected, either by small feedback capacitances or long integration times. Saturating the filter during the integration leads to increased noise and imperfect residual current cancellation.

In the simulation, the bias current changes from the IProg phase to the first integration phase by 25 µA. Due to the power line resistance along the column, this will cause an additional worst-case voltage drop of 1.6 mV, causing the operating point of the input branch to shift and also causing an uncancelled offset current (1.6 µA at 1 mS) flowing into the filter. Additional drops arise from the horizontal resistances in the periphery of the chip.

Moreover, the stability of the system with respect to certain operating parameters related to the readout sequence has been checked. Some of these parameters, like the position of the front-end readout with respect to the ADC conversion or the timing of the capacitor flip during the flattop,

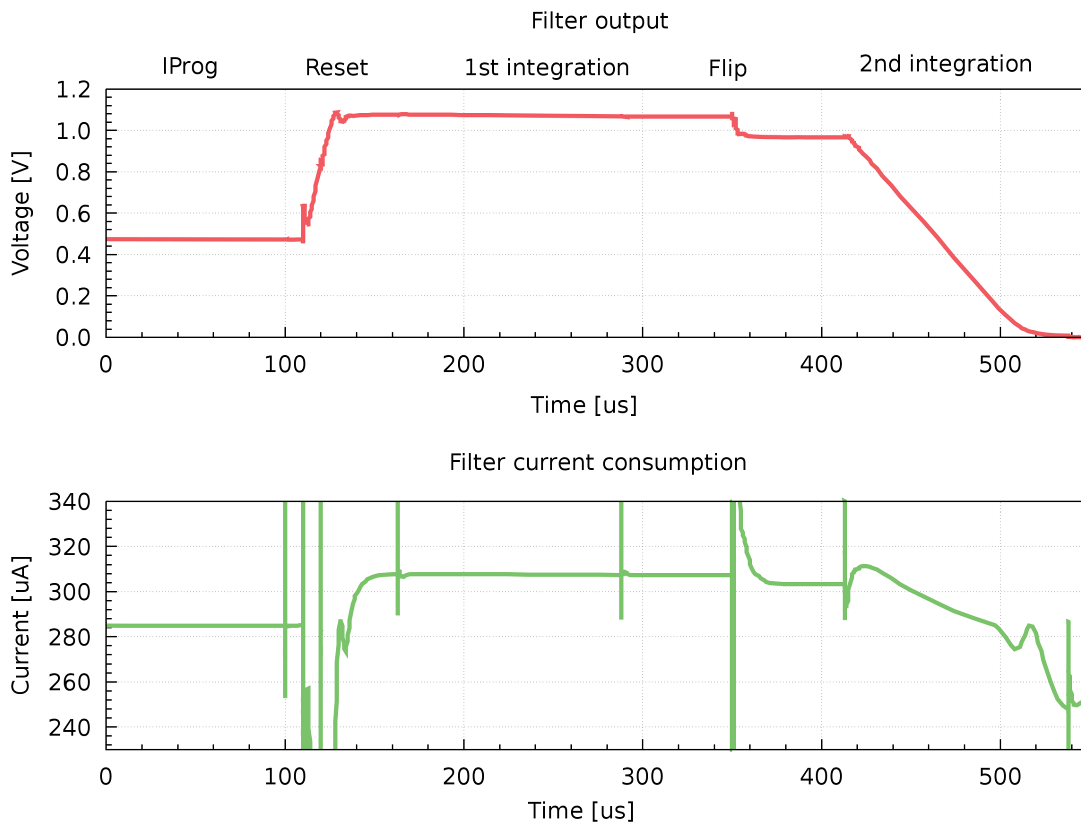

Figure 7.5: Top: Simulated 2.25 MHz filter cycle with a signal current of 20 µA during the second integration at 2.5 pF feedback capacitance. Bottom: The static current consumption of the filter changes between IProg and Burst phase, and even during an integration, depending on its output voltage.

should not change the pedestal position (given by its operating point, defining the residual current flowing into the filter) or width, which is given by the noise. However, peculiar effects have been found, which are not describable by the theory of the pixel circuit. These are caused by fluctuations of the analog power supply on the chip related to the large number of pixels on the chip, which can not be compensated by the relatively slow regulator connected via long traces. These power supply instabilities directly couple into the input branch.

Furthermore, leakage on the input node on the order of a few nA has been measured on assemblies without sensor, with a probable source being the large cascode transistor for the DEPFET mode. The leakage current is negligible when reducing the temperature below 0 °C, but for room temperature operation, it also changes the pedestal and therefore the operating point with varying flattop length. Any calibration attempt with long flattop, important for radioactive sources or optical injection, is not directly applicable to the same system configuration without flattop hold.

While working well on single-pixel level, the poor matrix performance of the MSDD front-end on F1 in terms of gain, noise, dynamic range, and the dependency of operation results on a large set of parameters make calibration very challenging. For user operation, a well calibrated and stable

detector is mandatory, which has caused the design groups to search for alternative front-ends.

Better solutions for an increased robustness of the input branch have been studied and partially published in [44] and [72]. The proposed solutions typically include cascoding FETs for the main input transistor to stabilize the supply for the input branch and thus improve the PSRR. In order to reduce the spread throughout the matrix, a circuit for controlling the threshold voltage of the input transistor via the bulk contact has been developed. However, a different circuit for the input has been implemented on the successor ASIC F2, which is a charge sensitive amplifier. An outlook on the successor ASIC design and preliminary performance results is presented in section 7.1.9.

7.1.5 Crosstalk

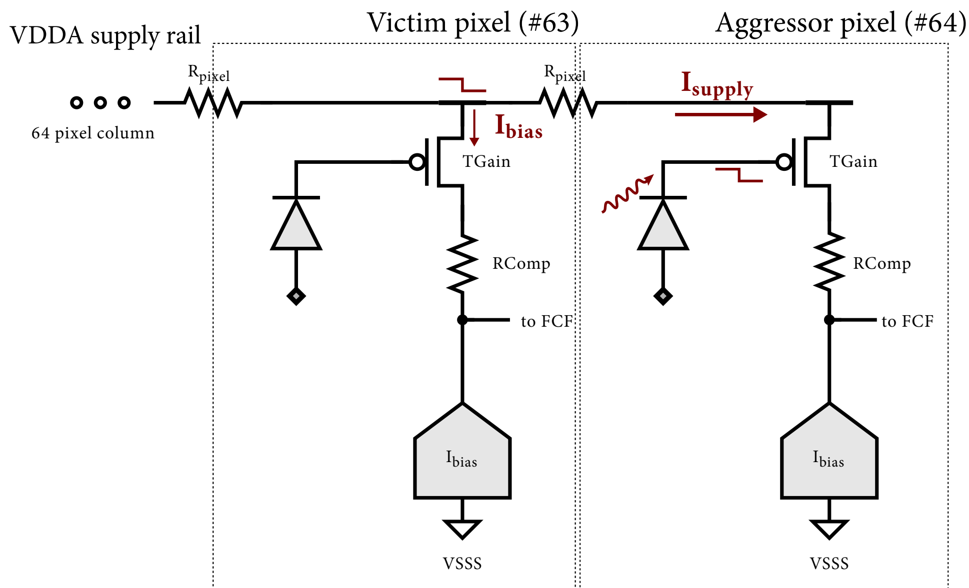

Figure 7.6: Illustration of the supply sensitivity of the MSDD readout front-end. The additional current drawn by the aggressor pixel after signal deposition results in a reduced supply voltage in other pixels.

It is evident from the schematic that the MSDD front-end has the same gain on its input node as on the power supply node. Consider a simple case (figure 7.6) of the last two pixels in a column of the ASIC. The last pixel receives a signal of 100 photons of 1 keV energy, leading to a ΔV_{in} at its input capacitance of 1 pF of 4.4 mV. At the maximum g_m of 1 mS, this yields an additional current request of 4.4 µA on the analog supply rail.

The additional current drawn by pixel no. 64 is resulting in a voltage drop on the *VDDA* rail, caused by the per-pixel resistance R_{pixel}. The additional current is flowing from the periphery of the chip, with a total column resistance of approx. 2 Ω. This results in a *VDDA* drop of 8.8 µV in pixel no. 63, effectively reducing the gate-source voltage in this pixel. The calculated difference of 8.8 µV corresponds to 0.2 % of the stimulus or 20 % of a 1 keV photon.

While the relatively small effect calculated above is not easy to detect on the F1 chip, an even worse situation can be easily realized. Since there is a large number of pixels unconnected on the prototype sensors measured in the scope of this thesis (see section 7.1.7), these can be used as victim

pixels guaranteed to receive no signal from the sensor, while signal is injected in all other pixels of the matrix through electrically pulsing the backside, which capacitively injects signal into the pixels. In the measurement, a signal of ≈ 50 keV has been injected into each pixel, causing a voltage step at the input of 1.9 mV per pixel and an additional current request up to 1.9 µA per pixel (at an input transistor g_m of 1 mS). The gain of the unconnected pixels have been measured with ≈ -40 % of the mean gain of the other pixels ('negative signal'), caused by the dropping analog supply due to the current load in all other pixels.

The model developed for the analysis of the voltage drops on the pixel matrix has been used to verify the magnitude of the effect in simulation. A large voltage drop in the given column is caused by the resistance of the horizontal connections in the periphery, allowing to estimate a similar effect from the simulation. Other patterns of illumination of the matrix would cause different voltage drops across the matrix and thus different effects of crosstalk, making the system no viable tool for user applications. As stated in the last section, the successor chip will provide a much more robust MSDD front-end.

7.1.6 Calibration studies

In a joint activity with the DSSC calibration groups in Munich and Milan, experimental calibration techniques for the DSSC detector were to be developed and tested. Also, equipment and software needed for the small module calibration were to be developed. Concerning the software, an interface was needed between chip development and characterization infrastructure mainly developed by the Heidelberg group and the calibration software.

The system response to several injection methods has been tested and cross-checked:

- X-ray fluorescence (XRF): Emission of characteristic secondary X-rays, by exciting a target material with X-rays, e.g. from a conventional X-ray tube. A wide set of target materials with energies in the linear range of the DSSC detector of 2 - 20 keV are available. For the F1 tests, an Yttrium target with X-ray lines at 14.96 keV (K_α) and 16.74 keV (K_β) has been used. Depending on the tube angle and the distance, a large set of pixels can be illuminated.
- Pulsed optical laser: Must be calibrated in energy, but linear over large range. Depending on the focussing optics, a single pixel or up to several ten pixels can be hit with a high flux. As described in section 7.1.8, each position must be calibrated carefully when focussing on one pixel.
- Backside injection: Capacitive coupling of backside to anodes. Injection to all pixels in parallel. Must be calibrated in energy, since the injected charge depends on the coupling capacitance and the pixel capacitance.
- In-pixel injection circuit, which directly injects charge at the input node. Low and high gain modes are available, with significant non-linearities in the high gain mode. Needs to be calibrated in energy.
- Proton beam from accelerator

The possibility of using a pulsed monoenergetic proton beam in air has been studied in [74] at the DEFEL beam line at the LABEC[1] accelerator in Sesto Fiorentino, Italy. The tandem accelerator allows a final proton energy range from 1 MeV up to 6 MeV. Due to the very short range of protons in air, the energy loss and influence of the exit window material have been studied in detail. Using

[1]LAboratorio di tecniche nucleari per i Beni Culturali, INFN, Sezione di Firenze

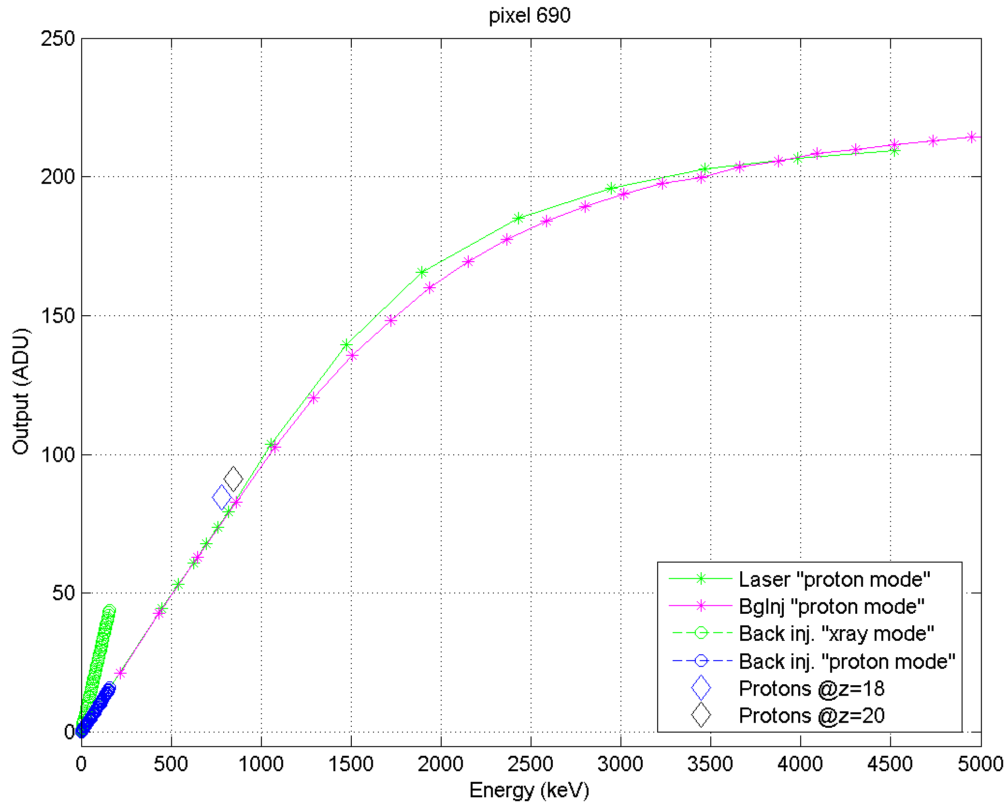

Figure 7.7: Overlay of results from the various, individually calibrated, injection techniques including protons for a single pixel of the F1 matrix. The fitted proton peaks are systematically higher than expected. [73]

a 7.5 µm thick polyimide film, the proton beam was extracted from the vacuum chamber with an energy loss of about 27 % for 1 MeV protons. Additional energy loss of ≈ 30 keV/mm is added due to window-detector travel distance in air. A calibration of the proton energy has been realized with a reference diode, positioned in the same distance from the window as the DSSC prototype.

For the energy calibration of laser, backside pulsing and the in-pixel charge injection, the Y XRF peak has been used. While the laser pulsing may scan the entire dynamic range up to several 1000 keV, the backside pulsing is limited to about 300 keV, but allows for very fine scanning of the low-energy (linear) regime. The in-pixel injection on the other hand can inject charge up to an equivalent of ≈ 3900 keV, but shows high non-linearities especially for large amounts of injected charge.

While the overlay of all injection techniques show good conformity in the low-energy regime, the picture is different for high-energy depositions, depicted for one of the probed pixels in figure 7.7. Here, all used injection techniques have been calibrated individually, with the pixel response plotted against the energy. Internal charge injection and the laser response already differ by up to 200 keV, which can be explained by non-linearities and crosstalk effects of pulsing in a larger number of pixels (128). Moreover, the response generated by protons of two different energies differ by about the same amount from the laser curve.

Sources of the deviations of the proton lines are

- fitting of X-ray spectra, which may lead to errors due to the very few bins available for fitting,
- the distance of the DSSC detector to the proton window, which might differ from the reference detector position by few millimeters,
- the metallization of the entrance window of the DSSC, which causes an additional energy loss of the protons.

7.1.7 LED injection

LEDs offer the possibility of injecting a large amount of light over a relatively large area through their opening angle of typically 50-120°. The green LED used here has a wavelength of 530 nm and is driven by an external pulser, synchronized to the detector system through the FPGA such that the LED is activated during the flattop phase. The flattop has been set to a duration of 1 µs. The long flattop is needed due to optical blocking filter on the backside, which reflects most of the light. Integration and reset times correspond to 4.5 MHz operation.

In the following, the baseline value for each pixel has been determined with the LED turned off. The net value for each pixel has been calculated by subtracting the baseline value from the measurement with LED turned on. Each pixel value is a mean value of all usable frames of a burst. Due to crosstalk effects, the magnitude of the individual pixel responses are of no interest here, however, the feasibility of imaging using large-area injection has been tested.

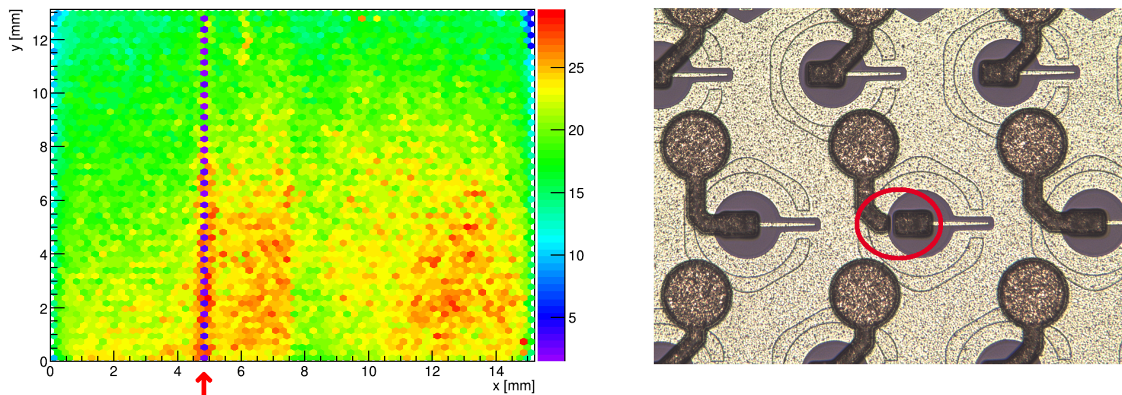

Figure 7.8: Left: LED illumination of the whole assembly. Right: Missing connection between anode and bump landing pad (image courtesy of S. Aschauer, PNSensor)

A design error has been identified while trying to illuminate the full 64 x 64 pixel matrix. Figure 7.8 (left) shows the result of such an illumination, where almost all pixels see a positive net signal. Note that no trimming has been applied here, and the LED was positioned close to the sensor, resulting in inhomogeneous flux over the pixel matrix. Along the left and right edges, low to vanishing flux is visible. This is expected due to overlap of the PCB and glue used to mount the sensor prototype on the PCB over the pixels along the edge, covering it from the incident light. This is only valid for the prototype test systems, there will be no obstruction on the final modules.

In the center, 32 pixels stick out with zero signal, which can not be attributed to any mechanical influence nor is this related to the ASIC - there's no structure on the ASIC that repeats only every

second pixel along a column. Careful inspection of unmounted sensor prototypes has unvealed a design fault in the metal redistribution layer on the sensor. For these pixels, a small gap between the collecting anode and the bump landing pad (figure 7.8 right) prohibits processing of the signal electrons in the ASIC. Due to the sensor covering also the gaps between neighboring ASICs, the length of the connection between anode and bump pad is not the same for every pixel. In this precursor production, the length of the metal interconnection for this column has not been set properly, which has been fixed for future productions.

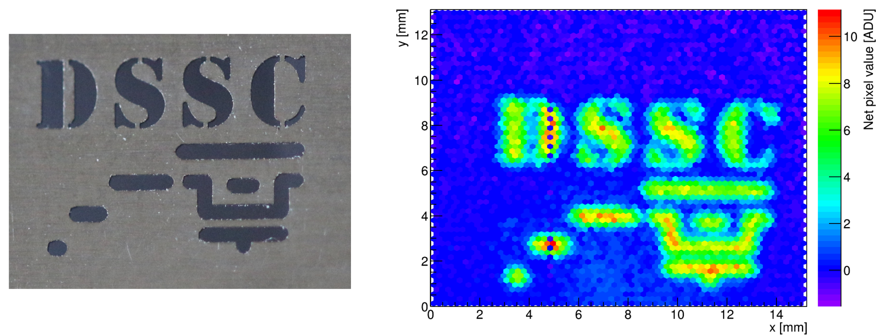

Figure 7.9: Left: Metal mask used for first imaging test of a DSSC assembly. Right: Net pixel value shown as a color value for each pixel of the 64 x 64 assembly.

The imaging capability has been verified using metal masks of 100 µm thickness. In order to reduce multiple reflections of light between the sensor back metallization and the mask, a light-absorbing cover has been applied to the mask. Figure 7.9 shows an example of a mask and the net sensor response, averaged over the 800 storage cells of a single burst.

7.1.8 Laser injection

A laser setup with computer-controlled movement stages available at the chair has been used for detailed testing of the pixel response with regard to the position of the charge generation. Since the sensor has an Al-coated backside, a reasonable light-tightness is sufficient. The box is constructed of black Plexiglass with rubber sealing along the edges and shielded cable feedthrough. Inside the box, the optical setup and motor stages prepared for mounting of a sensor chip are installed on an optical table.

For the following measurements, a red laser diode with a wavelength of 655 nm has been used. Since the output flux of a laser diode is strongly dependent on temperature for a fixed driver current, a driver circuit for output stabilization has been implemented. In the laser package, a photo diode allows monitoring the laser light flux. An IC provided by iC-Haus adjusts the laser drive current appropriately to keep the monitor current constant. During the off-phase of the detector, this laser light calibration takes place, and the proper operating current is stored. During the on-phase of the detector, a pulsing frequency of max. 155 MHz is supported. The laser is enabled by the FPGA through an SMA connection to the driver board, synchronized to the readout ASIC.

Figure 7.10 shows the test setup with a F1 and MSDD assembly, mounted in the laser box. An XYZ stage allows for moving the sensor assembly relative to the laser spot. The laser output is fed in by an optical fiber (lower right edge) and goes through an adjustable pinhole mask, a mirror

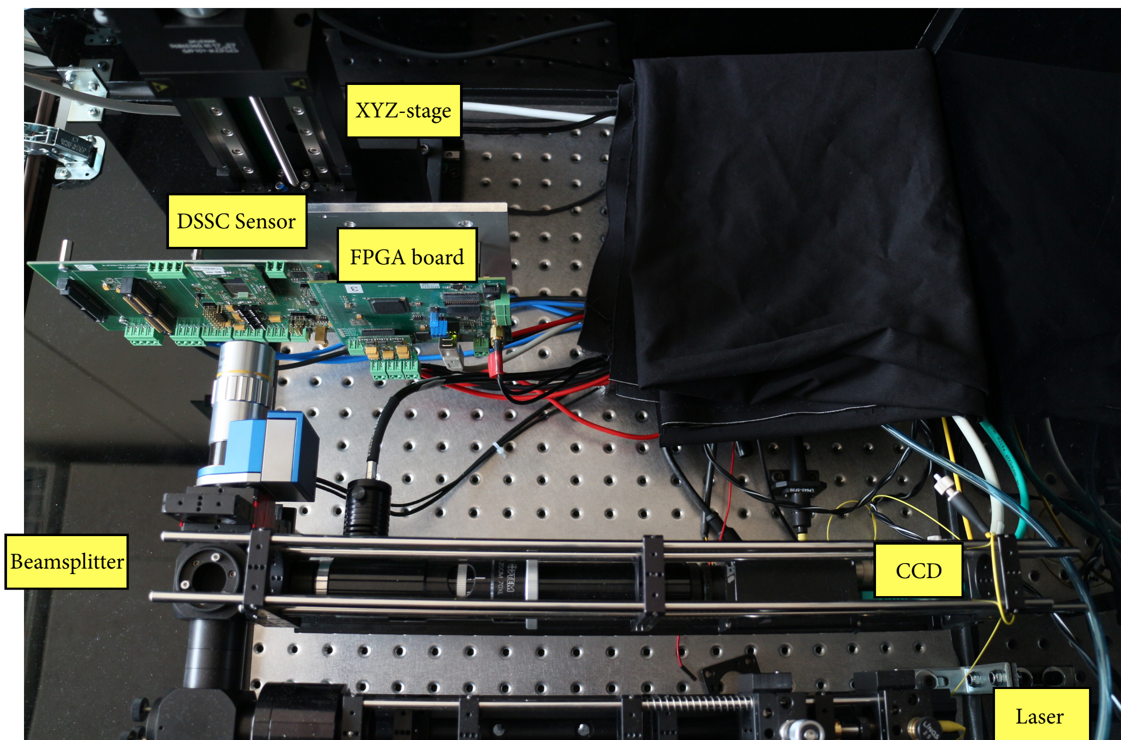

Figure 7.10: Test setup mounted in the laser box. The synchronized laser beam is focused onto the sensor with a μm sized spot. The XYZ-stage allows PC-controlled movement of the sensor.

and a lense focussing the beam onto the target. A beamsplitter allows for optical inspection of the alignment using a CCD.

The scan of a single pixel is shown in figure 7.11. A large variation of the signal amplitude between 15 and 40 ADU can be seen in the central region of the pixel, not affected by charge sharing with neighboring pixels. In order to rule out variations caused by the laser, a cross-check at a fixed position has been done, resulting in variations in the low % regime. The variations across a pixel must therefore be caused by variations in the generated signal charges.

The most likely cause is the aluminum backside, which is sputtered on the entrance window. Sputtering is a technique widely applied for large area deposition of material, where particles are ejected from a solid target by energetic particles. After ejecting, the neutral atoms travel in a straight line until hitting the sputtering target and coating its surface, resulting in a not totally flat surface.

Figure 7.12 shows the summed net values of three neighboring pixels for two different injection amplitudes. On the left, the signal amplitude is (as before) in the linear regime of the front-end. In the charge sharing regions, each pixel value corresponds to 1/2 resp. 1/3 of the total value, no signal is lost here.

Increasing the signal amplitude into the compressed regime (right) highlights the pixel borders through a simple mechanism: If the charge is divided, the response of each pixel will be in the linear regime, thus increasing the summed amplitude. This is most pronounced at the point where three hexagonal pixels meet.

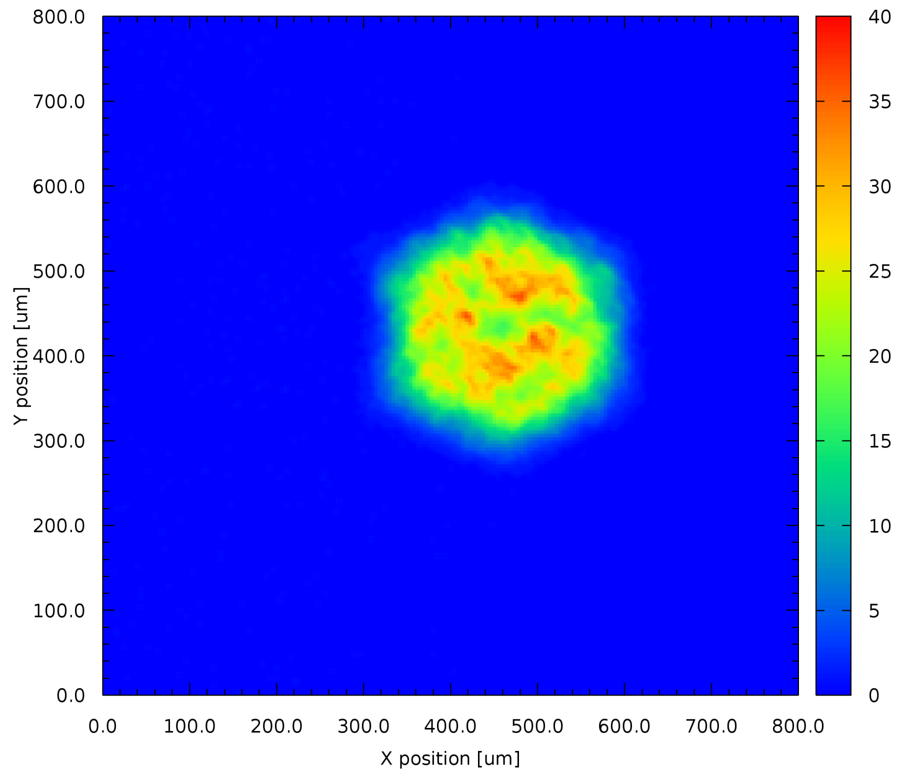

Figure 7.11: XY laser scan of one pixel. Signal magnitude deviations of 50 % across the area of a single pixel are measurable.

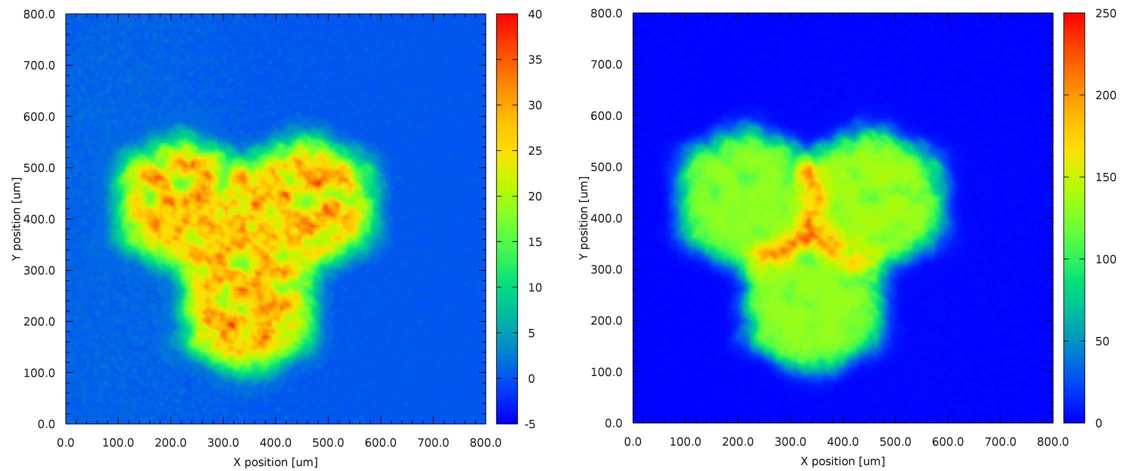

Figure 7.12: XY scan of three pixels. Left: Signal amplitude in linear regime, Right: Signal amplitude in nonlinear regime.

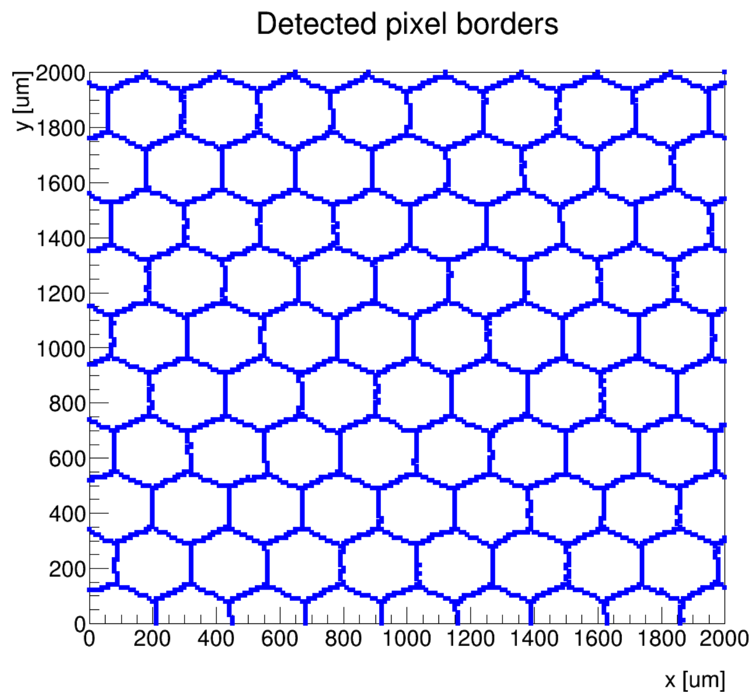

Figure 7.13: An XY scan of a larger area shows the very homogeneous distribution of pixel borders detected by the control software.

While the very precise scanning of pixel borders shown in figure 7.12 takes a large amount of time - for the above scan of a 800x800 μm^2 with 4 µm step size and complete readout of the pixel matrix 11 hours are needed - a larger part of the pixel matrix of 2 x 2 mm^2 has been scanned with a larger step width of 10 µm in both directions. In order to detect the pixel borders, a simpler algorithm has been implemented:

- For each injection coordinate, calculate the pixel with the highest net value (px_{max})
- If the px_{max} changes between two coordinates, mark this coordinate as a border of two pixels

The result of this scan is shown in figure 7.13. Very uniformly sized pixels have been detected[2], as expected from the implantation technology used for sensor production, with a standard deviation of the pixel size of 2 %. The visible deviations from perfectly straight lines can be explained by the relatively coarse stepping of the injection and plotting and by a slight tilt of the matrix with respect to the coordinate system defined by the table and motors.

Solely based on measurement of the pixel matrix response, an algorithm for automated movement across the pixel matrix has been implemented, since optical inspection is not possible (uniform backside). The algorithm is based on finding the pixel centers of three pixels by scanning with a laser in x and y direction until pixel borders are detected and attributing the pixel center in between. By finding only three pixel centers, a conversion matrix for pixel positions to step motor settings can be calculated, allowing direct movement to all pixels on the matrix.

[2] Pixels along the edges of the scan have been neglected, resulting in 68 evaluated pixels.

7.1.9 Outlook on F2

The successor ASIC F2 has been designed to overcome the severe performance limitations of the MSDD front-end on F1. The new ASIC, fabricated in 2017, is out of scope of this thesis, but its most relevant design changes and first results are presented here. The simple PMOS input stage has been replaced by a charge sensitive amplifier (CSA) [75] with an offset-cancelled voltage-to-current converter included. This way, the CSA is compatible with rest of the pixel circuit, i.e. the filter and ADC. A simplified schematic of the front-end is depicted in figure 7.14. Both linear and compressing circuits have been studied, whereas the linear version has been used on F2, as it has been prototyped and tested for robustness on small matrix level. For the given circuit, the linearity error has been measured to less than 0.25 %.

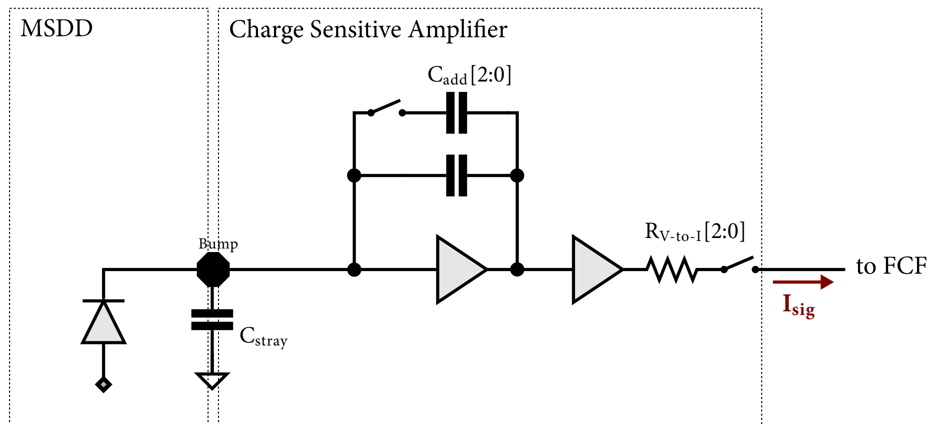

Figure 7.14: Simplified schematic of the charge sensitive amplifier implemented on the successor ASIC F2. The input branch is a low noise and robust readout circuit for MSDD sensors.

An improved DEPFET front-end has been included in the pixel, but it is disconnected on a single metal layer. In order to fabricate a DEPFET readout version of the chip, only the wiring layer has to be changed, greatly reducing the cost of a new production. The improvements include decoupling of the input cascode voltage to the DEPFET source, such that it droops along the burst together with the source, and a higher output resistance for the bias compensation circuit.

Through a relocation of the power supply bumps, a more homogeneous supply distribution has been reached, reducing the large horizontal spread measured on F1. Moreover, the reference circuit has been simplified and moved into the pixel, in order to improve the robustness against remaining horizontal voltage drops.

The ADC trimming results, illustrated in figure 7.15 by the response of all pixels to a sweep of the input voltage before and after trimming, are comparable to F1 with a standard deviation of the ADC gains of 1 % and maximum deviations of less than 2 %. No severe drawbacks concerning the in-pixel references have been detected so far. A slight gradient across the matrix of the ramp trim settings has been detected, illustrated in figure 7.16, indicating a gradient of the related analog supply voltage, which will be studied further. Moreover, all trim settings are well below the default value of 27, which will probably reduce the available trim settings for front-end gain variations.

The first noise measurement incorporating the full pixel matrix of F2 using the low-energy ^{55}Fe source is depicted in figure 7.17. A noise of 77 ± 12 e$^-$ has been measured at an integration time

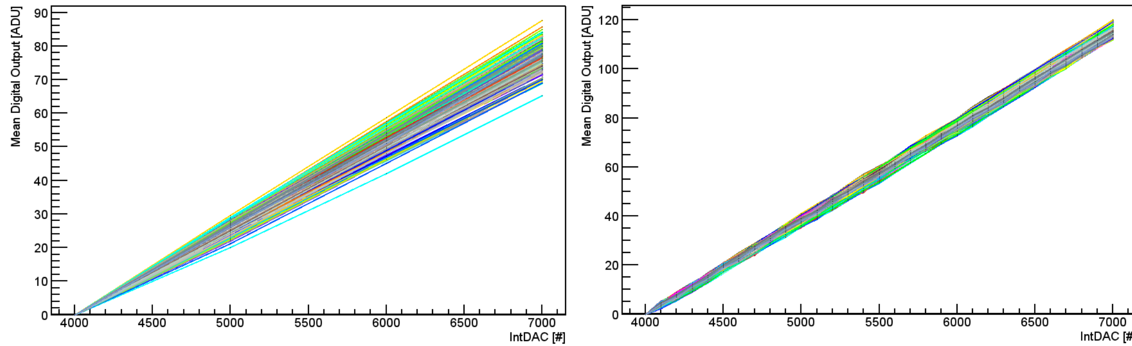

Figure 7.15: Response of 4k pixel ADCs on the F2 ASIC to a sweep of the input voltage using the on-chip DAC. Left: Before trimming, default settings. Right: The maximum slope deviations after per-pixel trimming of the ramp current are below 2 %.

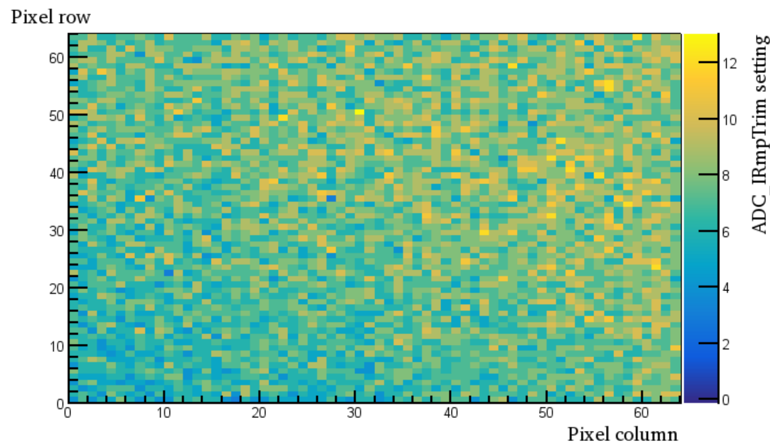

Figure 7.16: Resulting distribution of ramp current DAC settings on the matrix. A slight gradient from the lower left, where the analog supply voltage is sensed, to the upper right part of the chip is visible.

of 101 ns and a flattop length of 360 ns, which is worse than expected (60 e^- at an integration time of 50 ns). The reason for this is currently under study. However, the first noise measurements already show the vast improvement in robustness compared to F1. The white pixels in the map did not see any signal, most likely due to a missing connection between ASIC and sensor caused by a suboptimal flip-chip process.

The gain across the matrix (see figure 7.18) is quite homogeneous with a standard deviation of only 4 %, well in the trimming range of the ADC. The absolute gain of the system is 0.61 ± 0.03 keV/ADU. The CSA and filter gain settings have been fully exploited in this measurement, a higher gain will only be possible through increasing the integration time or by increasing the ADC gain.

Checks of further properties of the readout ASIC will be conducted in the near future, involving studies of crosstalk between pixels, system stability, and linearity.

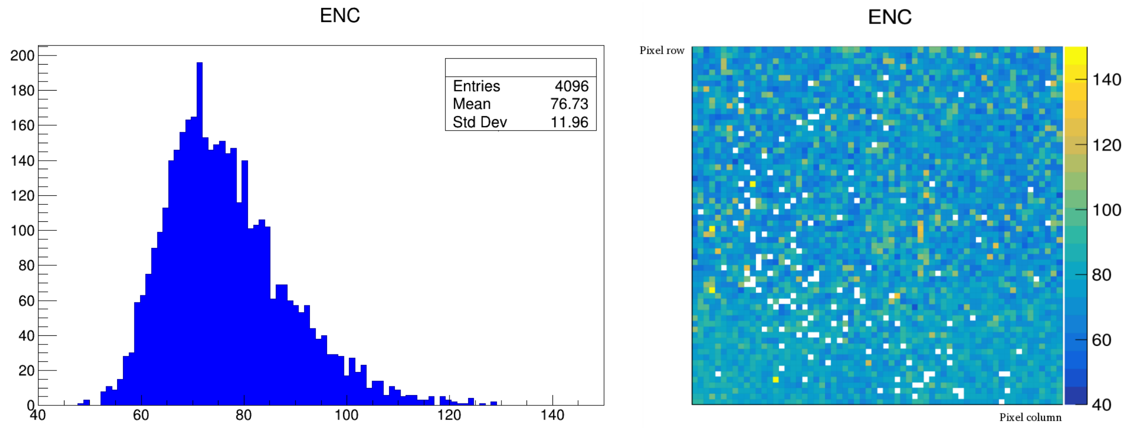

Figure 7.17: Histogram and map of the measured noise across the F2 pixel matrix using a ^{55}Fe source. Mean ENC is 77 e$^-$ at 101 ns integration time.

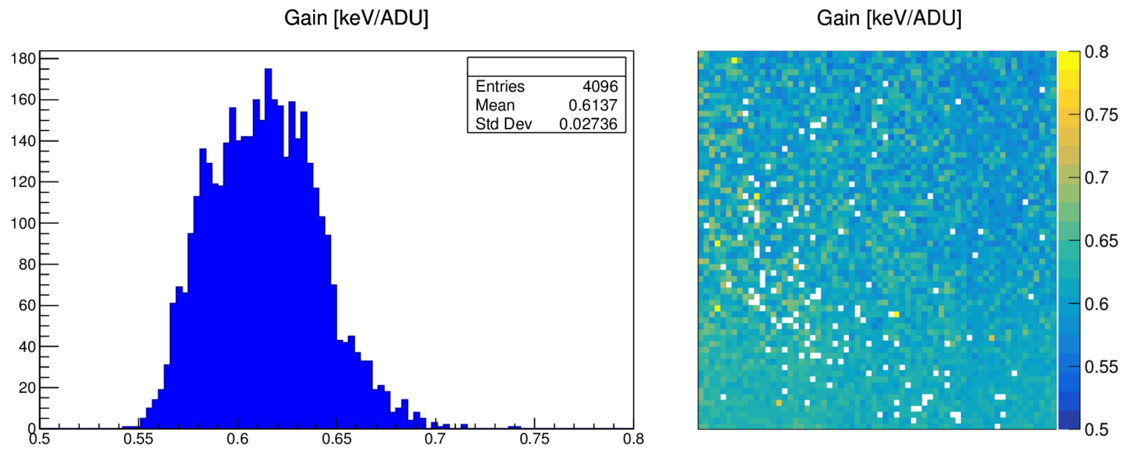

Figure 7.18: Histogram and map of the measured front-end gain of the 4k pixels on the F2 chip.

7.2 DEPFET Sensors

7.2.1 Preparation

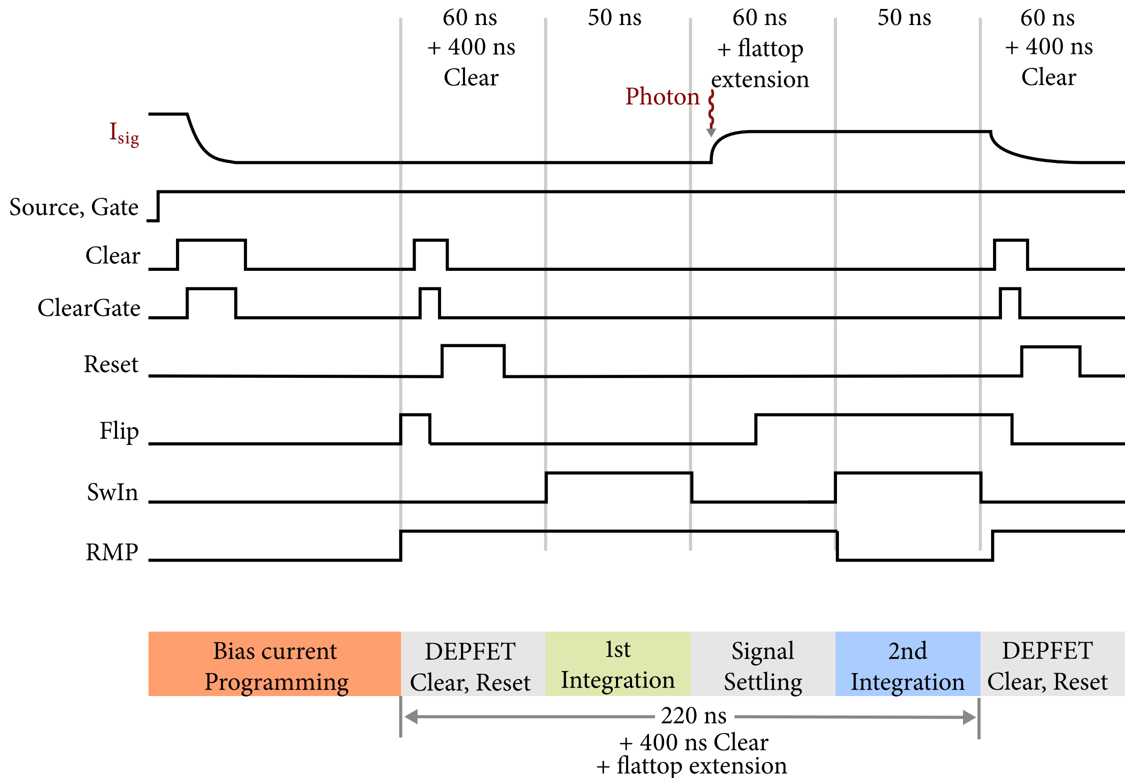

Figure 7.19: Operation principle of DEPFET assemblies in the test setup. The gate and source voltages (not shown here) are switched off between the bursts to save power. Clear and Cleargate are switched on at the start of the IProg phase and each cycle to remove any signal charges from the internal gate for the baseline measurements.

The operation of DEPFET sensors requires several additional, partly switched, bias voltages and a different timing scheme, shown in figure 7.19. In the DSSC system, the gate and source voltages will be switched off during the XFEL pause to reduce the power consumption. This has been implemented for the prototype test system as well by similar switching circuitry as on the I/O Board [55], while the clear and cleargate voltages are generated by analog multiplexers rated for these high voltages. At the start of the IProg phase, the gate and source driver circuits are activated, taking 120 ns to ramp up the bias for the matrix. IProg times as short as 50 µs are sufficient to prepare for datataking. The clear and cleargate voltages are needed to remove any charge from the internal gate before a measurement. Since the F1 ASIC performs a bias current programming before the actual measurement, a clear cycle has been added at the start of the IProg phase to remove any charge that may have accumulated in the internal gate during the XFEL pause due to thermal generation of charge in the bulk at room temperature or during the last measurement cycle of the previous train. The 400 ns clear pulse envelops the 380 ns cleargate pulse to prevent charge injection from the channel into the sensor.

Health checks of the devices after glueing and wirebonding to a PCB include a backside I-V measurement and a check of the ring isolation, similar to MSDD sensors. A measurement of the operation current of the matrix as a function of V_{gate} (transfer characteristic) allows for a basic check of the FETs and allows to estimate the expected coarse compensation DAC code in the pixels for a given set of source and gate voltages.

The applied sensor bias voltages are summarized in Table 7.2.

Bias contact	Applied Voltage
Source	4 V
Gate	2.5 V
Outer Substrate	4 V
Inner Substrate	4 V
Ring 1	−15 V
Ring 2	−20 V
Backside	−100 V
Clear	7.8 (low) - 16 V (high)
Clear Gate	1.4 (low) - 9.8 V (high)

Table 7.2: Applied bias voltages to the DEPFET devices, if not stated otherwise in the following.

7.2.2 Radioactive source measurements

Using small 8x8 mini matrices, which have been available earlier and in larger numbers than full-size sensors, bump-bonded to a prototype ASIC (MM4) similar to the final F1 readout chip, the noise of the front-end has been evaluated in detail. The processing chain in the pixel of the MM4 ASIC is fully identical to the F1 pixel.

In order to exclude digitization noise for the front-end noise analysis, the front-end gain has been increased up to values of 20 bins per keV. In the sample spectrum depicted in figure 7.20 showing the spectroscopic performance of the system, a slow readout cycle of 0.9 MHz has been used with 316 ns integration time at a feedback capacitance of 2.5 pF. The flattop has been extended by a hold in the sequencer of 500 ns. Low noise values of 18 ± 5 e^- have been measured on the 64 pixel matrix on MM4.

The measured noise figures for long integration times are summarized for several test chips in table 7.3. The large 64x64 pixel F1 matrix shows a slightly higher noise than the mini matrix test chips, most likely caused by a larger ripple on the ASIC power supply lines coupling into sensitive nodes like the cascode reference voltage.

The trough between the noise and the signal peak is caused by two physical effects:

- charge sharing between two pixels,
- photons arriving out of the flattop, causing them not to be weighted fully.

The trough hinders fitting of the peaks and therefore the determination of the peak positions, especially for spectra taken with low gain. While special methods are under development in the scope of the DSSC calibration workpackage [76], the contribution of the trough to the total number of events are verified in the following.

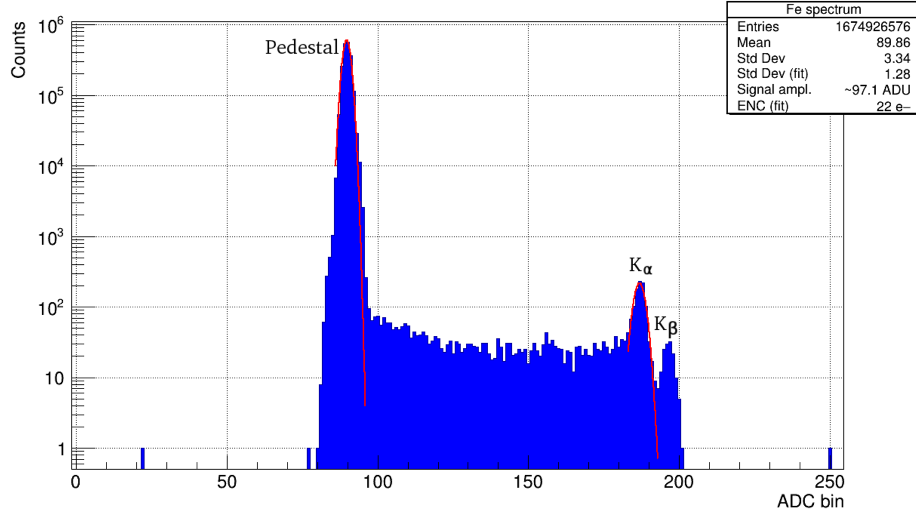

Figure 7.20: High gain spectrum of a ^{55}Fe source taken with a smaller matrix chip (MM4) at a frame rate of 0.9 MHz, with flattop extended to 500 ns.

ASIC (pixels)	Measured Noise	ASIC Front-End
MM3 (8 × 16)	20 ± 5 e$^-$	DEPFET
MM4 (8 × 16)	18 ± 5 e$^-$	DEPFET + MSDD
F1 (64 × 64)	32 ± 4 e$^-$	DEPFET + MSDD

Table 7.3: Measured minimum noise figures for the DEPFET readout with various ASIC variants. Shaping time is 370 ns for all measurements corresponding to 0.9 MHz operating speed.

According to [77], the diffusion width of a charge cloud generated from an X-ray absorption event can be approximated to

$$\sigma = \sqrt{\frac{2Dt^2}{\mu V_b}} \tag{7.2}$$

where $D = \frac{kT}{q}\mu$ is the diffusion constant of either electrons or holes, t is the thickness of the bulk, and V_b is the bias voltage. With typical values in silicon for the diffusion constant ($D = 12\,\mathrm{cm^2\,s^{-1}}$), mobility ($\mu = 450\,\mathrm{cm^2\,s^{-1}\,V^{-1}}$), thickness ($t = 450\,\mu\mathrm{m}$) and bias voltage ($V_b \approx 120\,\mathrm{V}$) for the DSSC sensor used here, a diffusion width of $\sigma \approx 10\,\mu\mathrm{m}$ can be calculated.

The geometry of the hexagonal sensor pixel is shown in figure 7.21. A full hit is an event where an incident photon creates a charge cloud that completely drifts to one pixel center only. The full hit area for one pixel is given by the total size of the pixel reduced by the border, where a hit would cause a split event with one or two neighbor pixels by lateral diffusion of the charge cloud:

$$A_{full} = (a - d)(b - d + c) \tag{7.3}$$

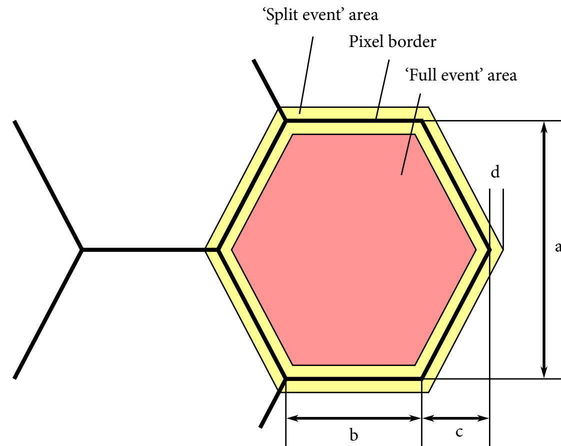

Figure 7.21: Geometry of a hexagonal DSSC sensor pixel (not to scale). Photons hitting the sensor close to the pixel border in the yellow area cause a split event.

The total area for any events detectable in the pixel caused by any kind of event, i.e. both full events and split events can be calculated by

$$A_{total} = (a + d)(b + d + c). \tag{7.4}$$

For the DSSC pixel geometry (a = 236 µm, b = 136 µm, c = 68 µm) and the assumed diffusion width, one obtains a ratio of 83 % full events and only 16 % split events for a homogeneous illumination of the sensor area. Out of these full hits of a pixel, not all photons arrive during the flattop phase of the weighting function. Out-of-time events contribute to the trough, as they are not weighted completely. For the spectrum above, a flattop of 500 ns was used at an integration time of 316 ns, yielding a 44 % ratio of full weighting time to partial weighting time[3]. Multiplying the geometric and temporal 'full event' ratios, a total ratio for full events of 36 % can be calculated.

The spectrum shown above (figure 7.20) is typical for pixels in the inner part of the sensor matrix, with ≈ 30 % full events (K_α and K_β summed) and 70 % of the events in the trough part, close to the values calculated above. Pixels along the edges of the matrix measure a larger fraction of split events, likely due to deformed drift fields close to the chip edges.

In the following, measurements of the influence of several parameters on the system noise will be shown, illustrating the performance boundaries of the system.

Several spectra with various integration times, all other parameters constant, have been measured at a flattop length of 5 µs, with its ENC being evaluated and plotted in figure 7.22. The yellow curve is a fitted function $\propto t_{int}^{-1}$, showing that the system behaves just as expected from theory, compare to (3.15). The minimum noise reachable for the used settings, especially the prolonged flattop, is 20 e^-, which is already close to the minimum calculated in section 4.1.2.

In a similar fashion, the noise has been evaluated for a variety of flattop lengths (figure 7.23) at an integration time of 300 ns. A fit of the expected function shape, given in eq. 3.18b, has been added. As expected, the 1/f noise contribution increases the total ENC from 17 e^- at a 1 µs flattop to about 27 e^- at 30 µs.

[3] The effect of signal collection time in the sensor has been neglected here, which slightly reduces the time available for a full event.

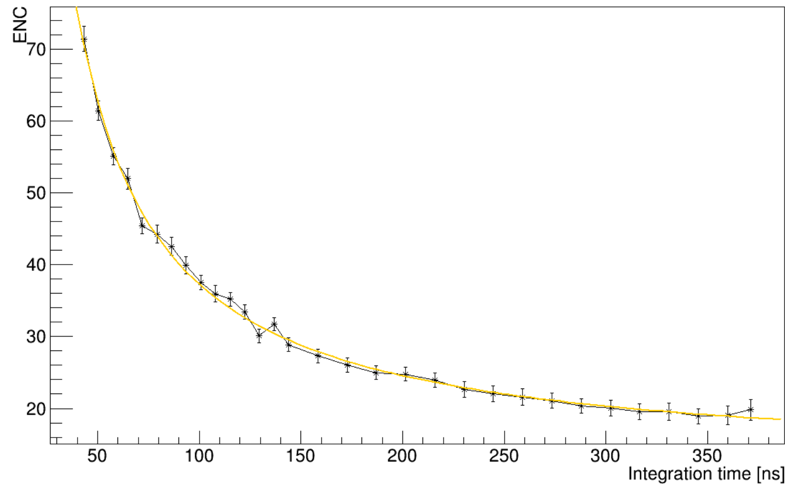

Figure 7.22: Measured noise of DEPFET readout as function of the integration time, measured on small matrix chip (MM4).

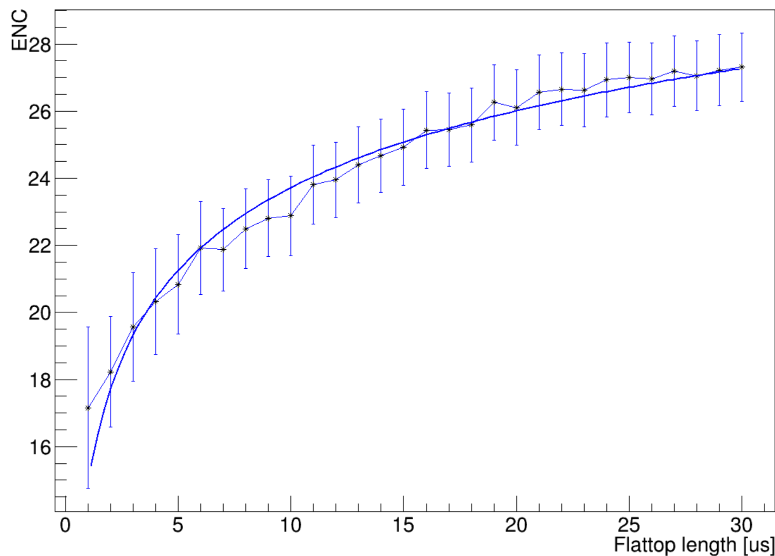

Figure 7.23: Measured noise of DEPFET readout as function of the flattop length, measured on small matrix chip (MM4), at an integration time of 300 ns.

Figure 7.24 shows a sample spectrum including the effects of a prolonged flattop of 50 µs and a smaller integration time of 154 ns. The noise is increased to 47 e^- smearing the K_α and K_β peaks, but increasing the probability to absorb a second photon during the flattop phase. The pile-up is visible as a secondary spectrum on the right. The distances between the peaks are 54 ADU and 55 ADU, almost equidistant. Small deviations might be due to ADC binning effects which have not been checked in this case. Pile-up measurements can be used for calibration of the linear regime of the system, generating two or even more equidistant peaks using just one source.

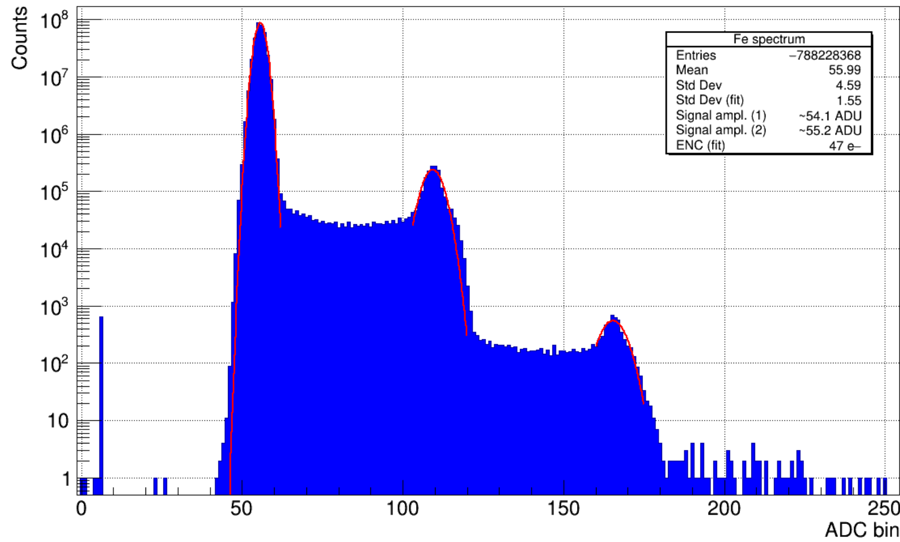

Figure 7.24: Typical spectrum of a ^{55}Fe source obtained with a smaller matrix chip with a flattop extended to 50 µs by a hold of the sequencer, increasing the probability to catch one or even more photons, visible as pile-up.

Clear efficiency

The goal of the DEPFET clear mechanism is the removal of all charges from the internal gate. Since the deep p implantation below the clear contact creates a potential barrier between clear and internal gate, a voltage pulse on the cleargate contact located in between is needed to create a conducting channel, while a sufficiently high voltage on the n^+ clear contact removes the signal electrons from the internal gate. A measure of the efficiency of the charge removal is the remaining pedestal current after the clear, which has been evaluated with respect to the clear and clear gate voltages applied.

In order to measure the remaining pedestal current after clearing, a test signal has been injected by an LED pulse before the clear, giving rise to a mean current per pixel of 8 µA. After clearing, the ASIC pixels perform a single integration, yielding a measure of the pedestal current, digitized by the ADCs. A certain offset even for complete clearing is expected due to a high ADC gain setting.

The result of a scan of 10000 combinations of clear and clear gate voltages is shown in figure 7.25. For the given clear timings of the test system of 400 ns clearing with a 380 ns embedded clear gate pulse (rise and fall time 30 ns) at a source voltage of 4 V, complete clearing of the device can already be reached with a clear voltage of 10 V if clear gate is sufficiently high at ≥ 6 V. Lower clear gate voltages can be used, at the drawback of increased clear voltages, e.g. clear gate at source level and clear above 16 V. The clear voltage must in this case be large enough to punch trough the p-well barrier. Note that the low off voltages for the clear and clear gate pulses have been chosen sufficiently low to close the clear channel.

A conclusion can be drawn that full clearing can be achieved with a relaxed set of clear and clear gate voltages with the long clearing times in the test system. In the final system with much shorter timescales for clearing of ≈ 60 ns, different clear voltage generation circuits and larger sensor matrices, this has to be studied again.

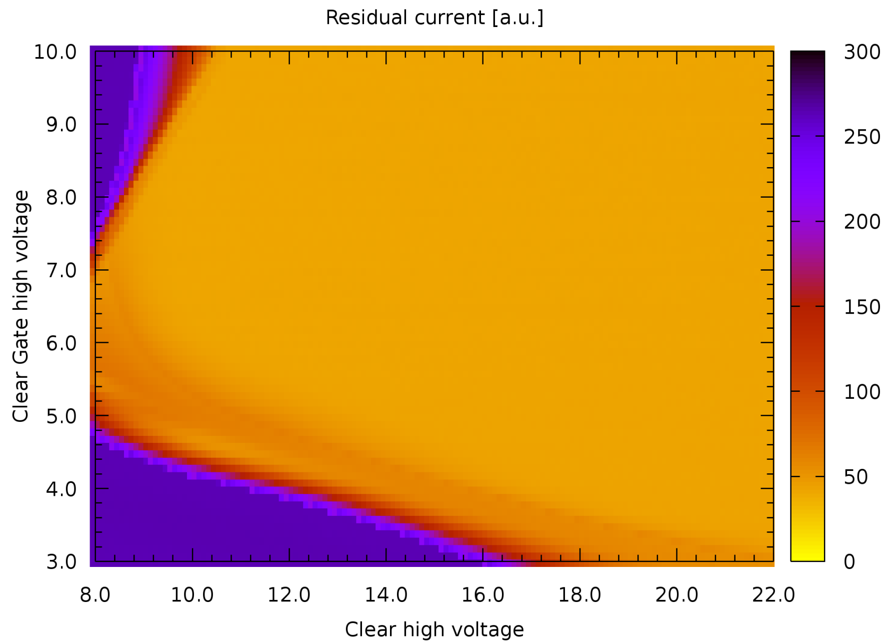

Figure 7.25: The residual current after clearing is shown as color scale for a matrix of clear and clear gate voltages. Complete clearing is visible as the homogeneous orange area.

7.2.3 Full matrix measurements

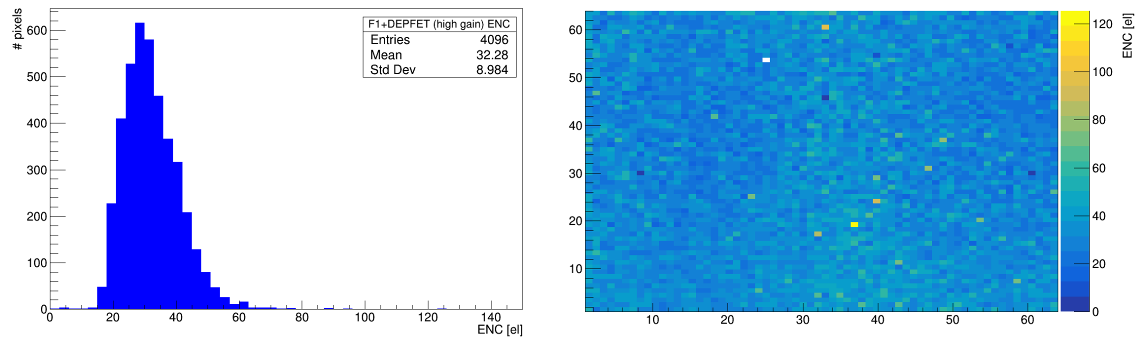

Figure 7.26: Noise histogram and map of 4k F1 pixels reading DEPFETs in high gain configuration.

The result of the fitting of ^{55}Fe spectra in all pixels of the 64x64 matrix is depicted in figure 7.26. The data of 734 bursts has been acquired in about 10 minutes using full F readout mode, with a high gain configuration set in the pixels. For each individual pixel, the pedestal has been moved to the bin center by an automated routine sweeping the pixel delay settings. A mean noise value of 32 ± 9 e^- has been measured, yielding a signal to noise ratio for 1 keV photons of ≈ 9. 90 % of the pixels show a noise below 60 e^-. The flattop has been kept short at 1 μs to stay as close as possible to the

final application case and to minimize the 1/f and leakage current noise contribution.

The amplitude of the pixel response to the 5.9 keV photon is 31.4 ± 4 ADU. Using the design values for the feedback capacitors and the ramp current at the given integration time of 196 ns, a mean g_q of 531 ± 69 pA/e$^-$ can be estimated, in good accordance with the design values for the DSSC-type DEPFET structure.

For a more realistic scenario of a gain of 1 keV/bin at the envisaged 4.5 MHz frame rate, the integration time has been reduced to the design value of 50 ns. A similar calculation using fitting of Gaussians results in a noise of 132 ± 42 e$^-$ on the matrix. However, many fit results showed either overestimation of the pedestal peak width since just 2-3 bins are available for fitting, or a bad estimation of the signal peak position. Better fitting algorithms are needed for this case and are under development in the DSSC calibration work package.

By adding a laser fibre to the setup, simultaneous injection of laser light and ^{55}Fe photons is possible. This allows for calibration of the energy injected by laser pulses in order to probe the pixels' dynamic range. The previous 1 keV/bin configuration has been used to probe a realistic estimation of the dynamic range and the parameters of the compression in the sensor.

The diode laser with a wavelength of 655 nm is enabled with a trigger signal from the test system FPGA during the flattop phase of the readout chip. The laser pulse length can be adjusted from software, while the intensity can be adjusted on the laser driver PCB. A series of laser pulses of the same length and intensity is used to inject charge into the sensor proportional to the number of pulses applied. Using the laser in an unfocused way allows to scan the response of several pixels in parallel, while not being too depending on the exact position of the laser, at the cost of a reduced flux per pixel.

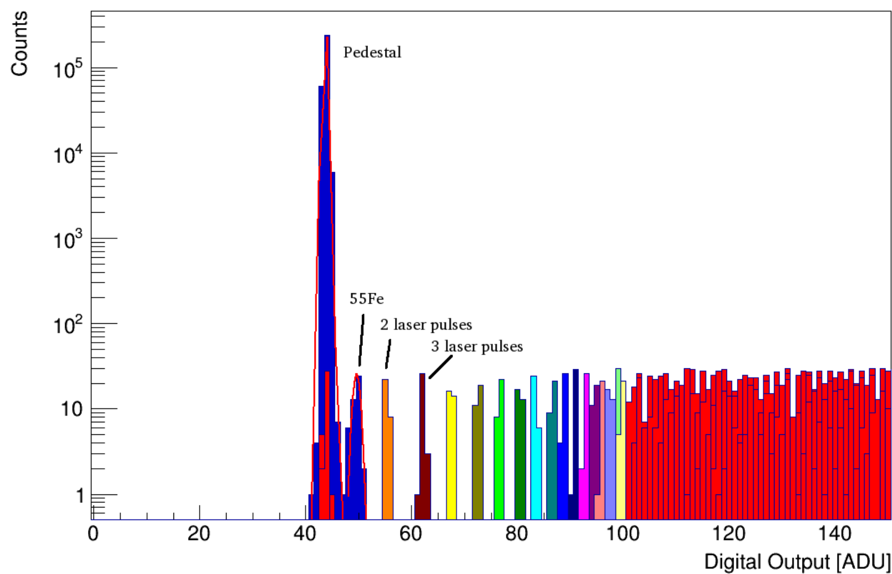

Figure 7.27: The laser pulses shown in red are calibrated in energy by the ^{55}Fe spectrum (blue). The peak for one laser pulse has been omitted due to the overlay with the K_α peak. The signals for different pulse numbers are color-coded up to the onset of compression, visible as shrinking distance between the peaks.

The flattop length of 15.1 µs is held constant for all laser pulse settings, in order to keep the conditions similar for each measurement, especially keeping the leakage current constant. The laser pulses have a duration of 30 ns at 60 ns repetition rate, allowing up to 250 laser pulses during the flattop to scan the non-linear pixel response. Two sets of laser scans have been conducted, one for a fine scanning of the linear and first compression region, and a second one to scan the high-energy region of the following compression region. The lower energy laser pulses have been calibrated using the ^{55}Fe source as depicted in figure 7.27, and per-pixel conversion factors have been extracted to allow the high-energy injection to be energy-calibrated as well.

The energy calibration is hindered by the spectrum filling less than ten ADC bins, introducing large errors in the gain determination. The addition of other calibration sources at higher energies to the setup would improve the calibration result.

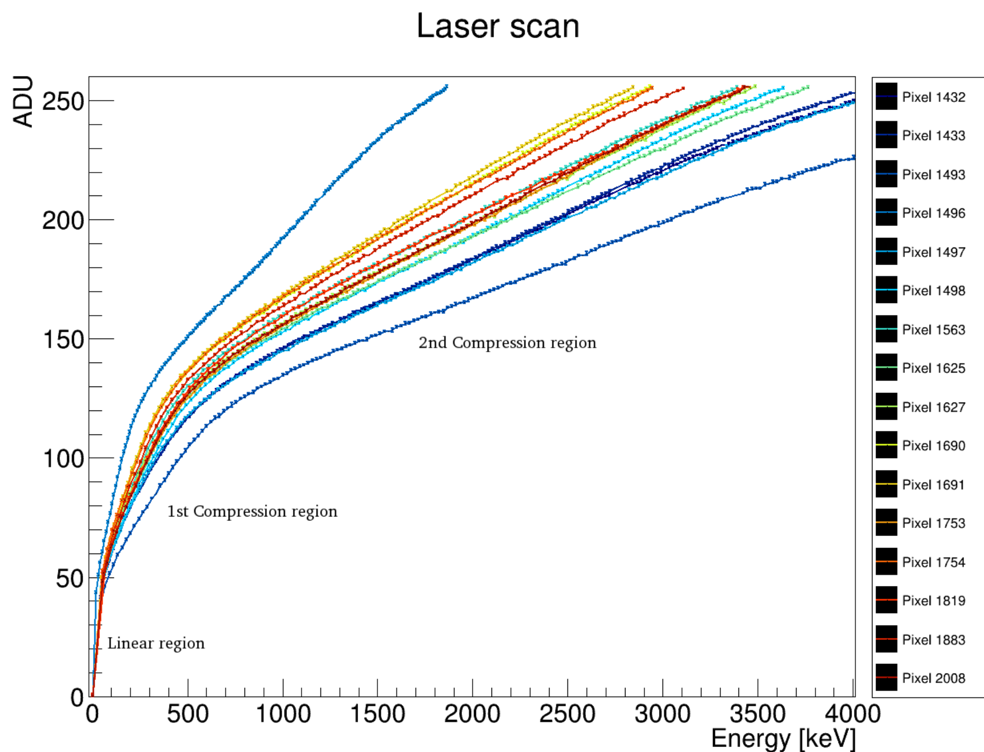

Figure 7.28: Scan of the F1 + DEPFET pixel response (offset corrected), calibrated by the ^{55}Fe line, for a set of pixels, showing the vast dynamic range of the system.

The resulting characteristics have been analyzed for a subset of the illuminated pixels, showing that the dynamic range target of 3270 photons at 1 keV is within reach. In the measurement shown in figure 7.28, the mean measured gain is slightly higher than anticipated at ≈ 1.2 keV/bin, therefore cutting off the characteristic before 3270 photons. This can be fixed easily by the ASIC configuration. Apart from ASIC gain settings, the reachable dynamic range is mainly DEPFET parameter-dependent, since the gain of the ASIC will typically be set to 1 keV/bin in the linear region. In this measurement, the third compression region of the device has not even been reached. A vast increase of dynamic range up to 10^4 photons at 1 keV is possible by

- removing the need for single photon resolution, thus decreasing the gain at the beginning at the characteristic in order to reach higher signal currents before running into the filter and ADC limits,
- running at a slower frame rate, thus enabling the use of the 9th ADC bit.
- For photon energies higher than 1 keV, the dynamic range is increased intrinsically, as the overflow regions are reached for lower numbers of photons.

The compression factor, defined as [41]

$$C_{comp} = \frac{g_q^{linear}}{g_q^{compressed}} \tag{7.5}$$

describes the amount of reduction of signal amplitude by larger amounts of signal charge. These can be estimated from the geometric design of the electrostatic potential of the internal gate regions. If we assume a homogeneous electrostatic potential within each overflow region and an abrupt potential step in between the regions, the compression region can be estimated as

$$C_{comp}^{i} = \frac{A_{center} + \sum_{k=1}^{i} A_{of,k}}{A_{center}} \tag{7.6}$$

with the area of the region below the channel A_{center} and the k-th overflow region $A_{of,k}$.

From the measurement data, the compression factors of each pixel has been determined by fitting a linear slope independently in each region of compression. The compression factors and the kink energies, here estimated by the intersection point of the two fits of the linear regions, are summarized with their design values in table 7.4. The measured kink energies are systematically lower than expected from sensor design. The fluctuations of the pixel responses can be explained mainly by the difficult gain determination caused by the fitting, sensor production fluctuations are expected to be lower.

Region	Measured kink energy [keV]	Design kink energy [keV]	Measured C_{comp}	Design C_{comp}
Linear region	57 ± 10	80	1	1
1st compression region	426 ± 52	470	9.0 ± 0.5	7
2nd compression region	-	2880	33.5 ± 3.3	20

Table 7.4: Comparison of measured and design values of the non-linear DEPFET compression regions. 3rd compression region of the device with design $C_{comp} \approx 55$ has been omitted.

Imaging

Due to the higher amplification and lower noise figures of the DEPFET compared to the MSDD circuitry, imaging with a lower energy source is possible. This has been tested by taking spectra of the 5.9 keV and 6.5 keV lines of ^{55}Fe with the F1 and DEPFET assembly.

A typical spectrum acquired by an F1 pixel reading out the DEPFET, with the gain set to about 0.5 keV per bin, is depicted in figure 7.29. The noise peak is fitted by a simple Gaussian fit centered at the bin of maximum height. Split events in the trough as well as full events are counted by an automated routine running over the data of each pixel, counting all events to the right of the fitted

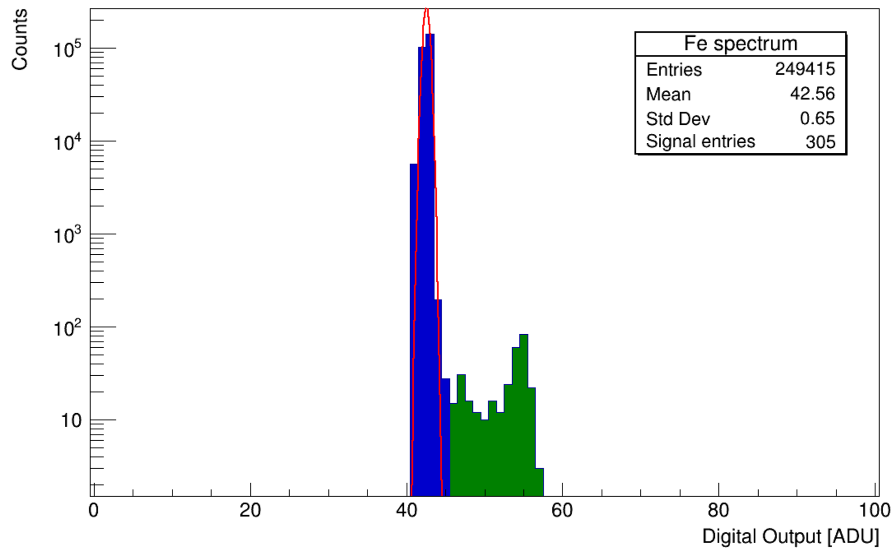

Figure 7.29: Sample histogram for the ^{55}Fe imaging examples. Counted signal events are marked green.

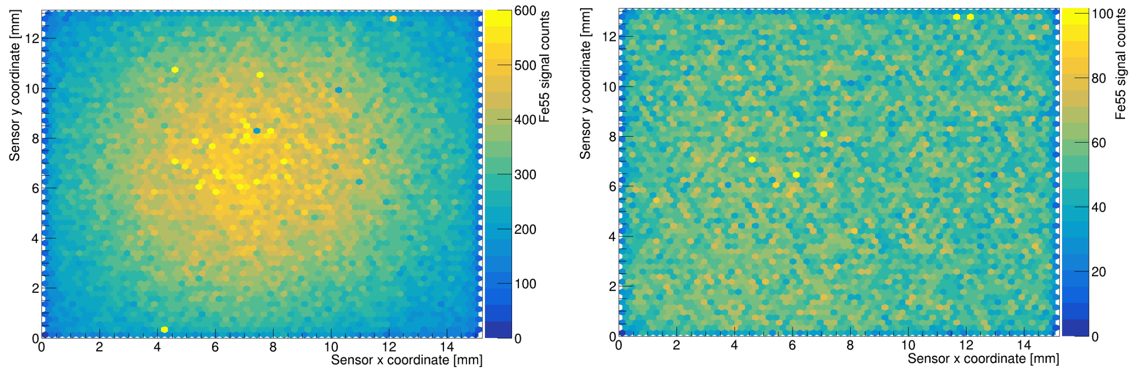

Figure 7.30: Map of the signal counts of the ^{55}Fe source, centered close to (left) and further away (right) from the sensor.

pedestal Gaussian with a distance of more than $2\sigma_{noise}$ to the mean of the pedestal. These signal events are counted by an automated routine running over the data of all 4096 pixels in order to measure the intensity of the source. Split events are usually counted twice, but could be ruled out by checking these events in the neighboring pixels. Out-of-time events in one pixel are counted once.

Figure 7.30 shows the color-coded number of events of the ^{55}Fe source, a small capsule with a round active area having a diameter of about 4 mm, taken in different distances from the sensor (1 cm and 7 cm). For the case of the source being further away, the source can be approximated as point-like.

From the calibration data of the source, an activity on the day of the measurement of 282 MBq can be calculated. At 7 cm distance from the source, one pixel on the sensor was thus irradiated by 62 cps of K_α and K_β photons (summed). In the measurement, 1000 bursts have been acquired with 600 entries each being evaluated. The last 200 entries were discarded from each burst as the regulator board circuitry ran out of power due to the prolonged flattop. The flattop of 92 ns, the hold time during flattop of 1.007 µs and the two integration cycles form the 'sensitive' period of 1.491 µs during each cycle. By summing up the sensitive periods, a total number of 55 events can be expected per pixel, neglecting split events.

From the measurement data, a mean value of 53.2 events per pixel can be extracted. The measured rate includes split events caused by out-of-time events, which do not distort the true event rate, and events split between pixels, which causes events to be counted up to two or three times, depending on the impact location. From the geometrical calculations given in section 7.2.2, a homogeneous illumination of the sensor will result in 16 % of the events being split between pixels. By correcting the event rate measured by the sensor for the split events

$$n_{X-ray} = \frac{n_{sensor}}{x_{full} + y x_{split}} \tag{7.7}$$

where n_{X-ray} is the true event rate and n_{sensor} is the rate measured by the sensor, and x_{full} and x_{split} are the ratios for full and split events. y describes how often a split event is counted and can be approximated to 2 for geometrical reasons. This results in a measured X-ray event rate of 46 cps, slightly lower than the expectation value, but showing no obvious signs of event loss on a large scale in the detector.

8

Wafer-level testing

8.1 Introduction

In the last two chapters, the in-detail characterization of single ASICs, bump-bonded to interposers or sensors, has been described. While the characterization of single pieces is an important part of the electronics development process, a large number of tested chips are needed for the assembly of larger modules, i.e. the megapixel camera.

During the assembly of the focal plane module, eight readout chips are bump-bonded to a large sensor chip. Since the production of these sensor chips is expensive and can take years in case of the DEPFET, the availability of sensors is typically very limited. Therefore it is mandatory to use only readout chips known as functional, as removing a defect chip and then resoldering another one adds risks to the whole process. Furthermore, the JTAG modules of the readout chips are daisy-chained in a ladder, so a chip with a defect JTAG block renders the rest of the chain unusable - that is, in the worst case, the whole ladder. In the DSSC project, the chips are tested and selected on the wafer before cutting. This section describes the wafer-level tests for known-good die selection and selected results from the F1 wafer tests.

The number of chips to be tested for a full camera is fairly high: Per ladder 16 chips are assembled, for a full camera this amounts to 256 chips. DSSC will deliver a full camera plus a spare quadrant, thus 320 known good dies are needed. Since the testing has been foreseen for the existing probestation available at the chair, and with limited manpower, the sheer number of chips dictates how much time can be devoted to each chip on the probestation.

The F1 dies are produced on an eight inch (200 mm) wafer with a fiducial diameter of 194 mm, containing 74 full reticles with one F1 die each (figure 8.1). Each reticle has been assigned a unique identifier throughout the process of die selection, cutting, and assembly on modules. A time of 20 minutes per chip will result in roughly 24 hours of work or three full work days. Additional time is needed for setting up, (re)alignment of the probe card and the wafer on the probestation, and, sometimes, the search for the cause of problems. A realistic assumption was about one week per wafer.

An impression of the probestation setup is shown in figure 8.2. Necessary hardware developments have been explained in the scope of the test system development in section 5.1.4. The wafers are placed on a computer-controlled chuck below the probecard with the needlering attached. All power, control signals, and data output are transferred through a high-speed cable (Samtec EEDP) to and from the FPGA board. The PC running the test software controls the FPGA board and reads the data through the USB interface. Some external equipment like oscilloscope, digital multimeter, and a high precision pulser are connected directly to the probecard or the FPGA board, being controlled and read via GPIB or Ethernet.

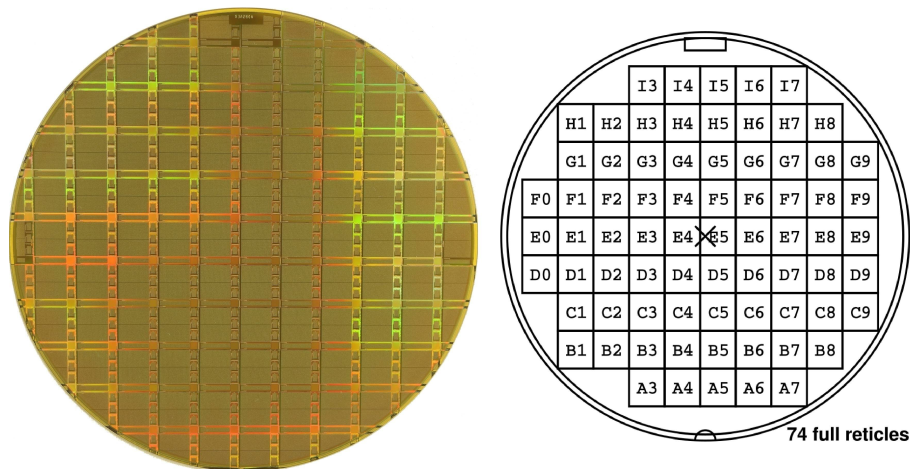

Figure 8.1: Photo and numbering scheme of an F1 wafer holding 74 full reticles.

Given the incredibly complex chip with its 4096 channels to be tested, 20 minutes is a very short time. It is clear that no perfect characterization can be done in this time, only a test whether the main blocks are working as expected and in an initially to-be-defined performance boundary. If possible, any test regarding the pixels should be parallelized as much as possible.

This chapter describes the tests performed on each ASIC as well as illustrates the process of Known Good Die (KGD) selection for module assembly. The F1 chips selected in the scope of this thesis have been used for development of the processes including KGD testing, dicing, flip-chipping to sensors and subsequent testing and shipping of modules. Prototypes of sensors with F1 chips have been produced in different formats (64 x 64 MSDD, 128 x 64 DEPFET, and large format structures for first ladders) and tested in different setups, with results given in section 7. As the characterization results have shown, F1 shows a poor performance regarding MSDD readout - the full scale production for a megapixel camera will therefore be done with the successor chip F2.

The tests are grouped in evaluations of the digital control block (DIG), the ASIC's power consumption (PW), periphery circuits (P), the in-pixel ADCs (ADC) and front-ends (FE). The individual tests are summarized in table 8.1. Moreover, in the following sections, each test will be described in more detail, with specific results attached. An overview of the Known Good Die selection outcome will be given in section 8.6.

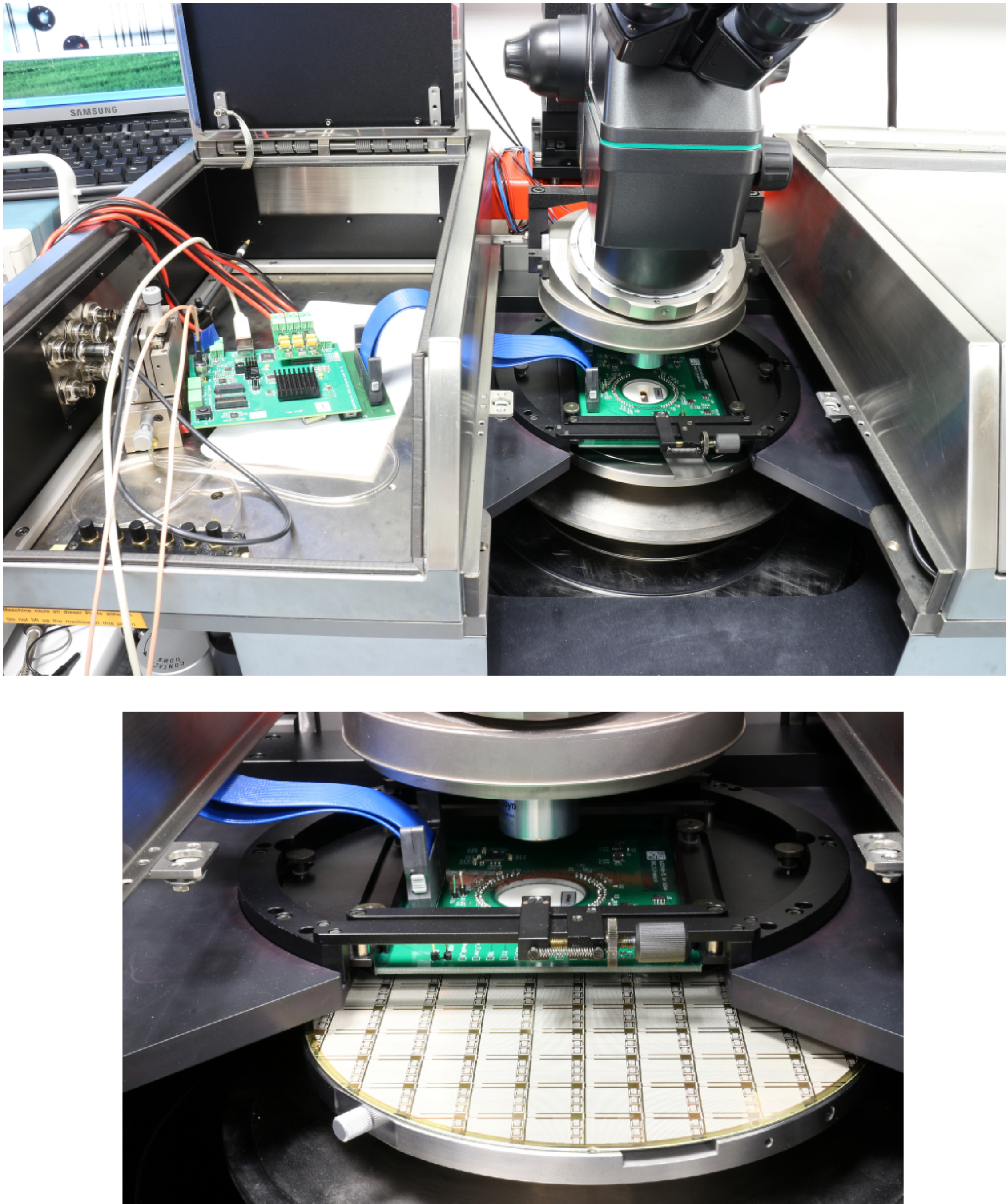

Figure 8.2: Top: Overview of the probestation setup including control PC, FPGA board and probecard. Not shown: External equipment like power supplies, function generator, digital multimeter and oscilloscope. Bottom: Detail view on the probecard connecting to an ASIC on the wafer. Power and data connections are realized through the blue high-speed cable on the left.

Test	Function	Details
DIG1A/B/C	JTAG	All registers are written and read back with different patterns.
DIG2A/B/C	Pixel register	Both pixel register chains are written and read back with different patterns.
DIG3A/B	SEU chain	Toggle XOR input to each register chain, read XOR output from JTAG register.
DIG4A/B	Output link & state machine	Send command to ASIC and read test pattern from data output.
DIG5A/B	Matrix SRAM	Write 0101/1010 pattern into each cell and read through serializer.
DIG6	Sequencer hold	Check latching of two timestamps with and without hold functionality for the latch signal.
PW1	Supply current reset	Measure digital supply current while ASIC is in reset. Decoupling caps must first be programmed to harmless states.
PW2	Supply current idle state	Measure digital supply current with clocks active, but all pixels off.
PW3	Supply current operation	Measure all supply currents with all pixels on, 1 % duty cycle.
PW4	Decoupling caps	Use decoupling cap self test feature
P1	Periphery DAC	Check functionality with external multimeter. Static analog power, pixels turned off.
ADC1	GCC start values	The GCC start value is latched directly after start of the ramp in the pixel through the external latch functionality.
ADC2	ExtLatch scan	Use Extlatch via XDATA to latch every timestamp in one burst.
ADC3	Pixel delay	Measure ADC shift by each delay bit for all pixels.
ADC4	ADC ramp current	Measure ADC value at 2-4 fixed periphery DAC values for all currents, all pixels.
FE1	Bias compensation DAC	Check correct bias current compensation with all DAC bits, digitize VHOLD with pixel ADC.
FE2	DEPFET front-end	Check linear response to internal signal current injection for each bit.
FE3	FE Gain settings	Check gain with all four filter feedback caps.
FE4	MSDD front-end	Bias with periphery DAC and check proper response to internal charge injection.

Table 8.1: Tests performed on the F1 dies on wafer level.

8.2 Digital tests

The tests DIG1-4 and DIG6 can be summarized as tests evaluating the operation of the digital control block and the slow-control registers on the chip. If these tests are successful, a chip is considered *programmable*. Any not programmable chip will not be used for module assembly, further tests on these chips have been skipped to save measurement time.

DIG1 and DIG2 are checking every slow-control bit on the chip by writing different patterns to the registers and subsequently reading the stored value. The used patterns are series of 1s, 0s, and alternating patterns, so the possibility to set the bits to both values is checked, and registers that are stuck at one value are detected. The JTAG interface is used to access the registers.

The SEU[1] detection chain consisting of an XOR chain of each bit of a certain register is checked in DIG3, where a bit flip is emulated by toggling the input signal for the XOR chain which is normally set to a fixed value. The output of the chain is simply expected to flip as well. The proper reception of dynamic control signals *XCLK*, *XDATA* and the 695 MHz ADC clock, the main FSM and the output serializer are all checked in DIG4. In this test, the *Send test pattern* command is sent on the *XDATA* line, moving the FSM into the equivalent state and the configurable test pattern word consisting of alternating bits is continuously sent out on the output link. The other states of the state machine (IProg, Burst, Readout) are checked during the ADC and FE tests.

The test of the in-pixel SRAM cells (DIG5) is treated on its own in section 8.3.

The sequencer hold test (DIG6) aims to check that the sequencer can be stopped through the hold functionality, as described in section 4.2.5. This is done by latching the timestamp through the DDYN signal generated in the sequencer at a given time, resulting in a certain output value. The sequencer is then reconfigured with an additional hold after the start of the counter and before the latch, with the hold being two 99 MHz cycles long. Due to the counter being clocked with both edges of the 7 times faster 695 MHz clock, the output value is expected to increase by 28. It is assumed that the other sequencer tracks are stopped as well if this test succeeds, since the Hold generation circuit is common for all sequencer tracks.

The tests have shown that about 20 % of the chips are not programmable. However, this can be due to fabrication defects, but also due to connection problems in the setup. For instance, if only one of the needles for the JTAG pins or the reset pin is not properly touching the ball, the JTAG programming will not work. These pins can be considered *single points of failure*. In some cases, retouching the balls resolved the problem. For the next iteration of the readout chip, these critical bumps will be duplicated. This has been possible due to generous spacing in the periphery region, and the fact that sensor production was still ongoing, since extra landing pads on the sensor are needed for the new solder balls.

8.3 SRAM test

The SRAM test intends to find any bit errors in the memory cells for the image data in the pixels. These amount to 29.491.200 bits (4k pixels, 800 cells per pixel, 9 bits per cell) in 3.276.800 cells. Corrupt words can't be skipped pixel-wise during writing of the cells in a train, since the SRAM addresses are set globally for a chip. However, defect cells can be marked as invalid in the readout chain after data taking. This is important for final user applications, in order not to insert erronous values into the data reconstruction algorithms.

[1]Single Event Upset

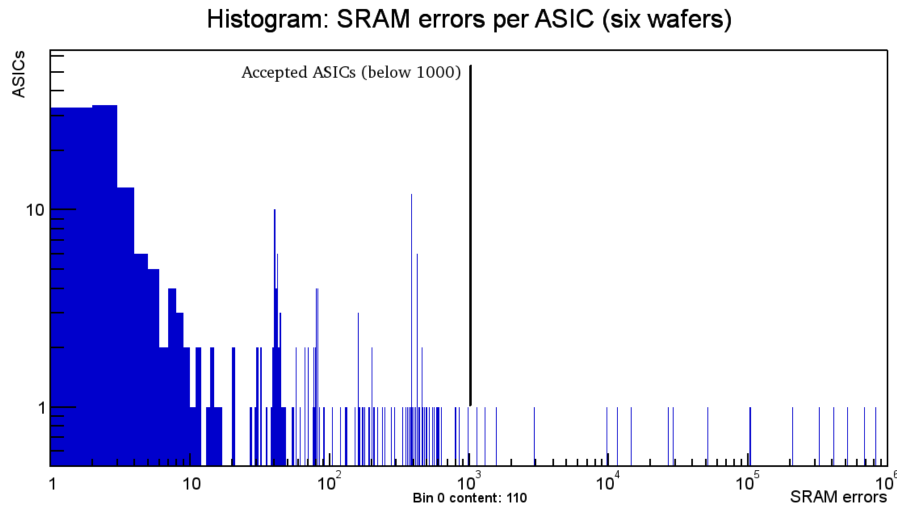

Figure 8.3: Histogram of defect SRAM words per chip. The threshold for good F1 dies has been set to 1000 defect cells.

A threshold of 1000 erronous cells or 0.03 % has been set for known good dies. This number is a compromise between having perfect readout chips and production yield, allowing for a large number of chips to pass the test while excluding the ones with excessive numbers of errors. 4 % of the tested ASICs have been discarded with an increased SRAM error count. Of course, stricter boundaries may be used, at the expense of test yield, e.g. only 110 out of the 444 tested ASICs can be classified as programmable and zero SRAM errors.

A closer look at the affected memory cells reveals both random and structured errors. Random errors are characterized by a single bit being constantly read as a logic low or high, while its neighboring bits are functioning properly. In contrast, structured errors have been identified, where a complete bit column comprising 40 bit cells is stuck at either 0 or 1 (compare bitblock structure shown in section 4.2.3). If one of the small bitline precharge transistors (W/L 280 nm/120 nm) is defect, the bitline for a whole column of SRAM bits (40 cells) can not be pulled to VDD. The memory cells connected to that bitline can then not be written with a logic 1, in case the positive Bitline pin is affected, or with a logic 0, if the inverted Bitline_B is affected. This relates to the peak at 40 errors in figure 8.3, where one column is defect on an ASIC.

However, the numerous precharge transistors (two for each of the 20 columns in each of the 9 bit blocks) are in a very dense area of the pixel. Duplicating or increasing might reduce the risk of losing whole bit columns, but would reduce the amount of realizable memory cells due to space constraints.

The distribution of errors per bit and per pixel have been checked and are inconspicuous, as expected by the strict hierarchical and therefore identical design of the bitblocks and pixels. Concerning the number of errors per reticle, summed up for all six tested wafers, show a higher amount of errors on the edges of the wafers (bottom, top left, and top right). Moreover, the 'E' ASICs lined up horizontally on the wafers typically show an increased number of errors, which can not be explained by any edge effect.

8.4 Periphery, ADC and front-end tests

The global voltage DAC is checked in P1 - the DAC is used further on to generate the stimulus for the ADC in the ADC4 test and to generate the reset voltage for the MSDD front-end checked in FE4. Since the DAC is binary scaled (with the exception of the LSB current sources), it is sufficient to measure only a few points of the characteristic in order to check every branch. Using a GPIB-controlled multimeter, the measurement could be fully automated. In the evaluation of the data, the overall offset and slope of the output characteristic are checked as well as the monotonicity, where the DNL of ± 4 LSB has to be considered. No programmable ASIC has failed this test.

ADC1 is a simple check of the possiblity to set the start values for the gray code counters. Here, the timestamps are latched directly after the start of the ramp phase through the external latch functionality. Every single bit is checked by two patterns (0b10101010 and 0b01010101). No problems have been found here.

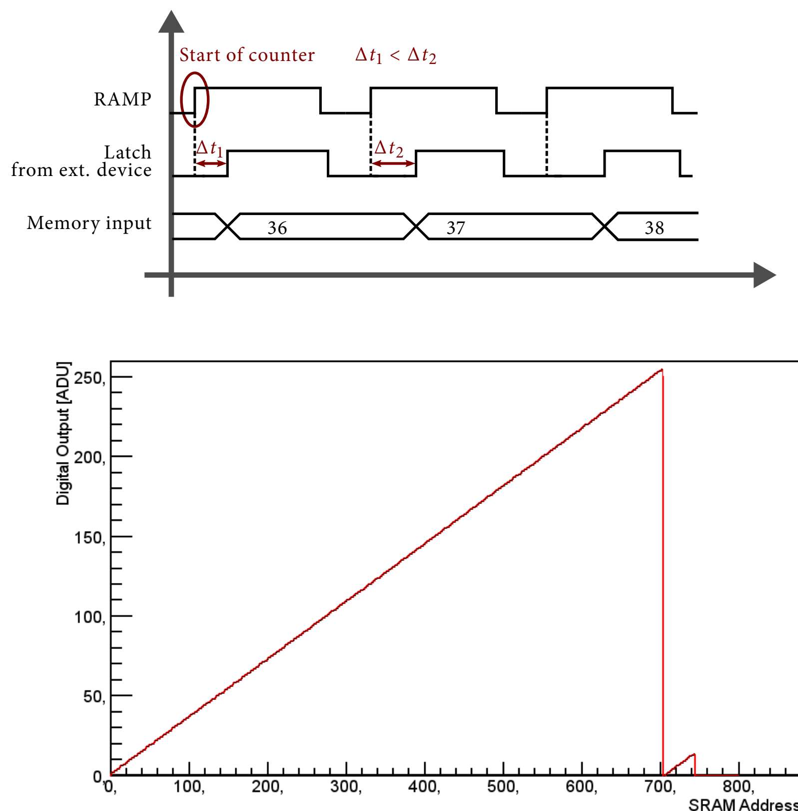

Figure 8.4: In the ADC2 test, an external latch signal is applied to all pixel ADCs with a frequency slightly slower than the repetition rate of the RAMP signal (top), thus increasing the latched value over time (bottom).

The digital domain of the ADCs is assessed by trying to latch every timestamp transmitted differentially from the counters and received in every pixel. An external high-accuracy Arbitrary Function Generator (Tektronix AFG3252) synchronized with the test system is used to generate the precise latch signals supplied to the ASIC. In order to minimize the time needed for this test, every

value should be latched in just one burst. The 800 storage cells in each pixel offer the possiblity of storing every one of the 256 bins three times. The latch signals are therefore generated with a slightly lower frequency than the ASIC cycle frequency of 4.5 MHz corresponding to a cycle length of 221.54 ns, so the latch signal is delayed from cycle to cycle by one third of the counter clock period of 719 ps with respect to the start of the counter. An illustration of the timing of the control signals and a sample measurement without missing codes is shown in figure 8.4. This measurement allows an easy and very fast assessment of the digital part of all 4096 pixel ADCs in parallel in just one burst.

While the tests on wafer level show a peak at a relatively large number of errors (figure 8.5), the same test run on ASICs flipped to sensors or interposers shows several orders of magnitudes lower error counts. Again, the test on wafer level is not suited for a characterization of the ADCs, but can be used to sort out ASICs with extensive problems of timestamp distribution. A limit slightly higher than the peak distribution at 50000 errors has been set.

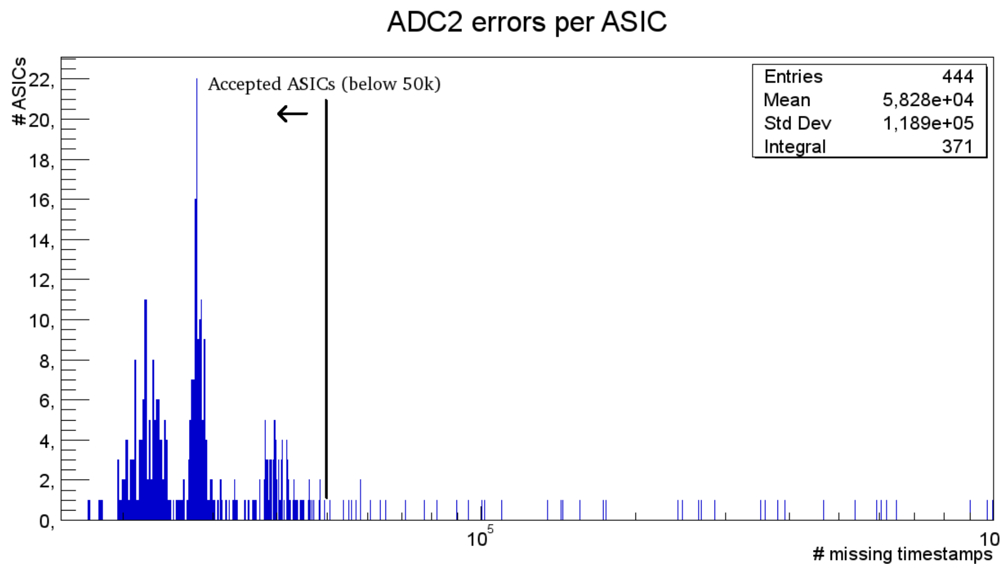

Figure 8.5: The histogram of the missing timestamps per ASIC shows a peak at ≈ 30000. These are typically randomly distributed throughout the pixel matrix.

The analog part of the ADC is tested in the ADC3 (Pixel Delay) and ADC4 (I_{Ramp}) tests. The sensor readout front-ends are tested in the FE1-4 tests. All these tests have been susceptible with regard to the quality of the needle connection to the balls. The main concern is the connection of the power supply needles and their corresponding sense needles. Two detrimental situations may appear while contacting with needles: High series resistance on the force or ground nets, and high resistivity or even open connection on the sense nets.

Series resistances are compensated by sensing the ASIC supply voltage at the ASIC level. In case of a high resistance over the needle-bump connection, the regulator increases its output voltage to generate the desired voltage at the sense point. This requires, however, a reasonable contact on the (single) sense needle. If both force and sense pins are poorly connected, the ASIC will suffer from a reduced supply voltage.

Moreover, simulations have shown that the used LDOs may cause a high voltage, up to the regulator input voltage, on the force lines in case of an open force sense connection. This has been resolved by adding 10 Ω between force and sense (and between ground and the respective sense) on the probecard, which ensures that no excess voltage is present at the ASIC input at any time. The fail-safe resistors do not prohibit sensing the supply voltage at ASIC level, which works well if a low-resistivity contact through the needle is established.

ADC3 tests the 70 ps delay steps of the ADC conversion, setting high requirements on the stability of the system. However, this measurement provided mostly inconsistent and not reproducible results. It is assumed to be strongly depending on contact quality, but also on temperature stability of the ASIC under test, which could not be realized easily in the given environment. ADC3 has therefore been excluded from further evaluation.

In the last ADC test, several voltages are applied to the ADCs from the previously tested voltage DAC in the periphery. The voltages are buffered by the in-pixel filter amplifier, allowing to test all ADCs in parallel without loading the monitor bus, and digitized for several ramp currents. The ramp current DAC is binary scaled, so the test only checks that every branch of the DAC is properly working. The control bit for current halving for 9 bit ADC operation is also tested. Reticles with more than 5 errors (0.1 % of the pixels) in this test have been sorted out, with only very few ASICs having failed this test.

Finally, the front-end tests aim to check the functionality of all building blocks for sensor readout. These are the current DAC for the sensor bias current subtraction, the flip capacitor filter, the pixel injection and the MSDD front-end branch. A threshold for KGD selection has been set individually for each test based on the results of the evaluation, such that ASICs with increased numbers of erroneous pixels are excluded, while providing enough ASICs for the precursor productions.

The bias subtraction DAC is checked by applying all available bias currents from the in-pixel injection circuit. For each setting, the DAC is sweeped while recording the V_{hold} voltage for the current fine-tuning branch. Non-working branches of the DAC can be found by analyzing the behaviour of V_{hold}, as the variable branch accounts for 2.5 coarse DAC settings. Most ASICs proved to be working, so a threshold of 5 errors per ASIC has been set for KGDs.

The filter and the pixel injection, simulating a signal current from the DEPFET, are checked in FE2. A linear system response within the design parameters is expected here, checked by the offset (below 100 ADU) and slope (2 ± 0.5 ADU/injection code) of a linear fit for each pixel. Any irregularity is registered as an error here, with up to 100 errors (2.5 % of pixels) allowed. Optimizations of this test are possible by also checking the linearity figures (DNL, INL) of the resulting characteristic.

Similarly, the filter gain settings, i.e. the four binary scaled feedback capacitors, are checked by applying a signal current from the on-chip circuit. In principle, recording only one measurement per capacitor would be sufficient. However, to increase statistics mainly for the smallest capacitors which tend to be sensitive to operate on the probestation, all combinations are recorded as well. A decreasing gain proportional to the feedback capacitance is expected. This test has produced very stable results with pixels being mostly working, resulting in only 10 erroneous pixels allowed per ASIC.

In the MSDD front-end test, the input transistor and the compression resistor are checked by setting a bias voltage through the periphery DAC and injecting charges into the input node by the internal charge injection. The DAC setting is chosen such that is typically well below the point of highest gain, so a large part of the s-type response can be scanned by the high gain injection. In the evaluation of the data, the slope in the maximum gain region is checked, although a wide range of gains are accepted (3.5 ± 1.5 ADU/injection step). Up to 100 errors (2.5 % of pixels), as for the

FE2 test, have been allowed here. Due to the strong susceptibility of the input branch on the analog supply, this test has produced a lot of failures, where over 10 % of ASICs had to be discarded.

Using the probestation setup, the input capacitance has been determined for the configuration with floating input balls. The results have been described in section 6.1.7.

It should be noted that the errors from the individual tests may add up to 6 % faulty pixels. In order to exclude the adding up and to get a more precise number of working pixels on each ASIC, the test evaluation software will be upgraded for the successor ASIC, where a bookkeeping table for each pixel will be created.

8.5 Power

The power consumption is measured for the constantly on digital power by reading the digitally controlled power supply value for three cases: Reset, idle and while 10 Hz cycles are active. Before measuring the power consumption, the chip has to be programmed to set the in-pixel decoupling caps to a harmless state (see section 6.1.2). Therefore, the test is only executed if the chip can be programmed correctly, i.e. if the digital tests do not fail. For PW1 and PW2, the cycled supplies *VDDA* and *VDDD_ADC* are switched off, for PW3, they are switched on for the nominal 10 Hz repetition rate at 600 µs on-time.

While the ASIC is in reset, the current drawn by the ASICs classified as KGDs is 28.7 ± 4.1 mA, with minimum/maximum values at 25 mA/50 mA. In this test, the complete digital control part is in reset, also disabling the clock dividers deriving the three clocks for the internal logic from the 695 MHz clock. The current drawn by non-KGDs can be much higher up to the current limitation of the *VDDD_GL* regulator set to 150 mA. Taking the ASIC out of the reset state adds about 8 mA to the current request. The resulting 36.7 ± 3.5 mA mean supply current for KGDs on the always-on net corresponds well with design values [44], where only very few outliers with a maximum value of 58 mA have been measured. In this state, the ASIC is ready for data-taking and listening on the *XDATA* control line. Again, non-KGDs may exhibit an increased supply current. By switching on the data-taking and therefore adding write (during burst) and read (in between bursts) cycles for the SRAM memory, a realistic operation mode can be achieved. Writing the SRAM cells at a 4.5 MHz frequency adds 100 mA of current on *VDDD_GL*, but at a duty cycle of below 1 %. The reading and sending of data on the LVDS output link has a higher impact of 12 mA at a duty cycle of 99 %. The digital supply current during operation has been measured to 46.5 mA, well within the expectation from simulation and well within the power and thermal budget in the system.

As explained in section 6.1.2, the current consumption on the cycled power supplies *VDDA* and *VDDD_ADC* is measured through the discharge along the burst measured by a digital oscilloscope. It is both read and evaluated automatically by the control PC connected via ethernet.

Both KGD and (programmable) non-KGDs have a similar current consumption of 2.9 ± 0.3 A (*VDDA*) and 1.3 ± 0.2 A (*VDDD_ADC*) during the burst. No strong outliers have been detected. The current consumption during operation is unfortunately no indicator for the ASIC quality.

The last power test PW4 aims to check the large 35 pF Mimcap for power decoupling, located above the SRAM. These caps occupy a large area, increasing the risk for fabrication faults, i.e. shorted capacitors, and a shorted capacitor could make the entire chip inoperative. The caps are connected to each of the three supplies and grounds by a switch transistor, one for the P side, and one for the N side. While the P transistor is switched directly from the control register, the N switch includes a logic to detect a faulty capacitor, explained in more detail in [44]. The main idea is to try

to discharge the N side of the capacitor to ground through a weak transistor while enabling the P switch. In case the capacitor is shorted, the N side is pulled to VP. The state of the capacitor, i.e. the voltage on the N side after enabling the P switch, can be read through slow control.

This test did not reveal any defect capacitors if the digital tests succeeded, being the prerequisite to proper reading of the capacitor states. Unfortunately, no test structures were available to simulate a faulty capacitor, allowing to test the fault detection circuit.

8.6 Overview

In total, 444 ASICs on 6 wafers have been tested. Table 8.2 summarizes the pass/fail results of each test.

Test name	Discarded ASICs	Fraction of tested ASICs
DIG1-4,DIG6	81	18 %
DIG5 (SRAM)	19	4 %
P1 (DAC)	0	0
ADC tests	54	12 %
FE tests	73	16 %
Sum	227	51 %

Table 8.2: Overview of failed ASICs per test. Tests are evaluated from top to bottom. If an ASIC fails a test, it is not considered in the following ones.

The major contributors are the digital tests with 18 % failed chips and the MSDD front-end test with 11 % failed chips. The chips failed during the digital test also include those with failed electrical connection between needle ring and bump bonds. The share of the digital tests is expected to drop for the next ASIC generation with doubled critical control bumps. The MSDD front-end test has been improved after the first wafers after gaining more and more knowledge from more detailed ASIC characterization, mainly regarding dependence on *VDDA*, reset voltage, and the number of active pixels, which has been reduced to 1024 (1/4th of the matrix). This has led to a reduced number of ASICs failing this test.

Subsequently to the probestation testing, the wafers are thinned from 750 µm to 250 µm and cut with a margin below 20 µm, well below the gap between two chips on the sensor modules foreseen with 200 µm. Diced chips are delivered to the consortium for bump bonding to the sensors. The assemblies are then tested again to ensure only working assemblies are glued and bonded to the expensive main boards for final ladder assembly.

9 Conclusion and Outlook

This thesis covered characterization and large scale testing of the sensor readout ASIC for the DSSC camera. In order to verify the properties of the ASIC, a hardware test system and adequate control firmware and software had to be written.

The test system is a flexible tool for verification of the electronics developed by the ASIC designers. Various ASIC and sensor variants, generations and samples can be plugged into the system, also allowing easy connection of external test equipment. A recently developed board also allow for full data rate operation of a DSSC-type ASIC, exploiting the bandwidth offered by a USB 3.0 port. The interconnection experience available at the chair [78] allowed for rapid prototyping of sensor and ASIC structures. Large pixel matrix assemblies have been characterized on the prototype test system, which has proven to be viable in various environments including beamlines.

While the MSDD readout circuitry proved to be well performing on single-pixel level at noise levels of 101 e^-, matrix operation emerged as a challenge. The missing power supply ripple rejection of the MSDD readout branch and unanticipated horizontal voltage drops across the large matrix chip were the main reasons for poor performance. Low-energy ^{55}Fe photons could be detected by the large readout ASIC running a subset of the pixel matrix, but the noise and dynamic range goals for the full matrix could not be reached. Using higher energy photons from an XRF measurement, a noise of 470 ± 205 e^- has been measured on the F1 matrix. Promising results have been obtained already with the recently fabricated successor ASIC F2, incorporating a more robust CSA front-end.

However, the readout ASIC architecture was initially planned for connection to a DEPFET matrix, which has been tested in the scope of this thesis as well. The low noise features of the full matrix down to 20 e^- could be measured for a frame rate of 0.9 MHz, while offering a vast dynamic range by the non-linear characteristic of the sensor. First tests of the dynamic range on matrix level have been conducted, reproducing the expected shape of the non-linear response of the DSSC-type DEPFETs.

Wafer-level testing procedures have been implemented with no false positive chips known to be mounted on the precious large format sensor chips. The main challenge has been the allowable time per ASIC while having to test several building blocks in a large 4k pixel matrix. This has been resolved by parallelizing measurements as far as possible and, for example, by assessing the ADC performance in just one burst. For future tests, a different type of needle will be evaluated in order to resolve the problems with high resistivity contacts to the device under test. Moreover, the imprint of the sharp needles made a reflow of the solder balls necessary.

First tests of a MSDD ladder in a lab environment have been published in [79]. For these tests, the chips previously tested on wafer level have been bump-bonded to large format sensors and assembled in the final module geometry. Measurements at a synchrotron beamline at PETRA III have been successfully completed, showing the expected characteristic front-end response curves. The synchronization of the Patch Panel Transceiver to the synchrotron running at a speed of 2.6 MHz

has been accomplished. The stability of the control and readout circuitry involving the PPT and the I/O Boards have been demonstrated in several days of beamtime.

There are busy times ahead for the DSSC consortium with the production of the successor ASIC F2 and the assembly of the full megapixel detector. Individual modules have to be produced, tested, and finally installed at the beamline and calibrated for user operation. The very first preliminary measurements on F2 assemblies show a noise of 77 ± 12 e^- on the 4k pixel matrix at an integration time of 101 ns, already showing a significant improvement with respect to the F1 circuitry.

The development of a new DEPFET fabrication methodology in a commercial process has been investigated in the past years [80]. One of the main issues for low noise applications in this production is bulk leakage current. The leakage has proven to be sufficiently small, typically below $1\,\mathrm{nA\,cm^{-2}}$. The first production run already gave promising results on the spectroscopic performance of these devices with a larger g_q on the order of 1 nA per electron and an ENC comparable to previous productions. The production times have been reduced to only half a year per batch. These new devices are expected to be a great tool for single photon detection at low energies at the European XFEL.

Concerning the technological side of hybrid pixel detectors, new developments have emerged in recent years. By the use of Through-Silicon Vias (TSV), readout ASIC pads can be made accessible from the backside, eliminating the need for wirebonding by a BGA-style fanout on the ASIC backside [81]. The assemblies are thus fully 4-side buttable and reduce the dead sensor area. As an alternative, the TSV technology may be used to integrate a second ASIC in the stack, which can be dedicated to storage of image data, which either allows to vastly increase the available memory space, or to shrink the pixel size for a higher pixel density.

9.1 Summary of own contributions

The contributions of the author to the DSSC project are summarized here:

- A complete test setup environment has been designed and manufactured for ASIC testing and studies on calibration of ASIC parameters. The setups have been distributed to other members of the consortium, consortium members have been trained in using the test systems for hardware testing, and continuous support for hardware, firmware and software has been given.
- Characterization of various analog and digital ASIC building blocks through measurements including the in-pixel front-end, filter, ADC, and SRAM, up to the operation of the full readout chain in the large pixel matrix chips. Feedback to the ASIC developers for improvements of circuits has been reported.
- Careful simulations have been carried out for the main in-pixel circuits for comparison with measurement results.
- Tests of the imaging capabilities using different light sources and different sensor types has been conducted, including the verification of the expected sensor properties. An automated xy-scanning of sensor pixels using a focused laser beam has been implemented.
- The noise and dynamic range of DSSC sensors and associated front-ends has been measured and analyzed, including MSDD and DEPFET sensors.

- Wafer-level testing of a large number of chips has been implemented and carried out. The test protocol involves testing of the digital periphery circuits as well as the front-end, ADC and memory in each of the 4k pixels. Software for automated data analysis for known good die selection has been written and selection of several hundred chips has been done.
- Design of DAQ chain testing environment to allow full data rate testing of the I/O Boards and Patch Panel Transceiver.
- Mass production of highly integrated rigid-flex IO Boards has been carried out and boards have been tested before shipping them for final detector module assembly.
- First implementation of detector slow-control firmware and software including design and implementation of server/client communication.
- Design of a laser driver circuit with optical power stabilization and fast pulsing, used for calibration of the non-linear response of the DEPFET system.
- Design and implementation of a super-speed USB interface upgrade for an FPGA board has been carried out including implementation of associated firmware and low-level interface software.

A

MicroBlaze control system for the PPT

The Patch Panel Transceiver (PPT) serves at the boundary of the DSSC detector as the main control unit. From the XFEL Clock & Control system, it receives the system clock and data telegrams indicating upcoming trains as well as events to be vetoed. Based on these telegrams, precise timing signals have to be generated for proper operation of the detector. The data received from the I/O Boards has to be sent via optical links to the TrainBuilder subsystem. These tasks are implemented in dedicated hardware in the FPGA fabric, interfacing with external components like the 10 GbE Phy IC.

Slow control of the system, however, has to be implemented on the PPT as well. The task of the slow control part is to set and monitor the operation parameters of the digital blocks in the PPT, the I/O boards and the readout ASICs. This has to be done in cooperation with a control software running on a PC, where a user operates the detector and thus modifies the operation parameters. The hardware interface between the PC and the PPT is realized by a gigabit ethernet connection.

Naturally, the network interface task would be well suited for a dedicated microcontroller IC. Since this application does not call for high processing power or high transmission bandwidths, a microprocessor implemented in the FPGA fabric is also feasible. This can be realized in the Xilinx framework as a MicroBlaze soft-core processor, entirely implemented in general-purpose memory and logic cells. Access to the custom single-task, high-speed hardware in the FPGA fabric is possible via bus protocols or by individual pins. A standard linux kernel can be used as an operating system, since it is customizable for small memories. While being flexible by loadable drivers (kernel modules), it offers built-in multi-processing and networking features. As a bonus, hardware developers are typically familiar with linux architectures and software.

A.1 Architecture

This section quickly summarizes the architecture of the MicroBlaze processor as explained in [82]. A block diagram of the processor is shown in figure A.1.

The MicroBlaze is a reduced instruction set computer (RISC) optimized for the use in Xilinx FPGAs. It uses a 32-bit architecture with configurable endianness. The processor is configurable by a lot of parameters, allowing to customize it both for saving space on smaller FPGA types or for higher performance at the cost of logic slices.

The instructions executed on the processor are pipelined in either three or five stages, configurable at synthesis. Each stage takes one clock cycle to complete for most instructions. The pipeline is stalled for those instructions taking more than one clock cycle to complete.

Instruction and data address space are separated, thus implementing a Harvard architecture. However, the memory ranges can be overlapping by mapping them both to the same physical mem-

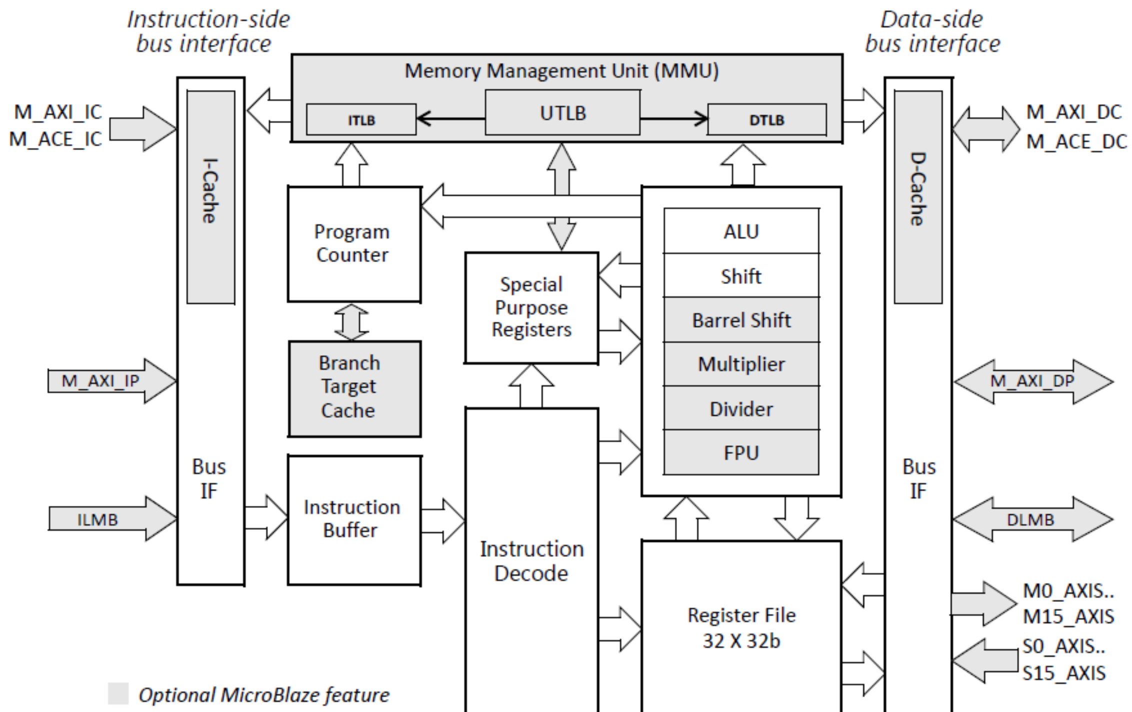

Figure A.1: Block diagram of the MicroBlaze processor. The processor is highly configurable. Optional blocks are depicted in gray. [82]

ory. Both memory interfaces are 32 bits wide and have configurable endianness. Prefetching of instructions is supported.

An implementation of a memory management unit (MMU) is available optionally. While the processor can use the address space to directly access physical memory, it can also use the MMU to translate addresses into physical addresses. System software can thus move currently unnecessary programs and data out of the physical memory of the processor to free space for the currently running software.

FPGA-internal memory like the Block RAM cells in Xilinx FPGAs can be used for the instruction and data caches. Block RAMs are connected through the Local Memory Bus (LMB) protocol. External memory can be connected through the now-standard Advanced eXtensible Interface 4 (AXI4).

A basic floating-point unit (FPU) can be implemented. Only single precision floating point format is supported with the basic mathematic operations and conversions. Although an FPU is available, code should be optimized to avoid the latencies associated with floating point operations.

In order to ease embedded software development, several features are offered for debugging. The JTAG interface of the FPGA is used by the debugging software called Xilinx Microprocessor Debug (XMD). The processor can be started, stopped, reset, and executed step-by-step, and its registers can be read and programmed. Breakpoints and watchpoints can be used for software analysis. Multiple processors can be accessed on the same FPGA and, by building a JTAG chain, on several FPGAs.

A.2 PPT Processor design

The processor for the DSSC camera use case is designed to include an MMU to access the external memory, no FPU, and cache sizes of 4096 bytes for instructions and data. Controller logic for the external DDR3 memory chip is included in the processor design running at 400 MHz with a 16 bit wide interface.

The Mixed-Mode Clock Manager module (MMCM) on the FPGA fabric is used to generate all necessary clocks for the processor and its periphery modules. In total, 6 different clocks are needed: 100 MHz for the processor and the AXI bus structure, 25, 200 and 400 MHz for the DDR3 controller, and a 125 MHz for the ethernet interface. These are all derived in an FPGA-internal PLL from an oscillator delivering 200 MHz to the FPGA input pins.

Further modules attached to the processor include

- a debug module for accessing the processor registers through the JTAG programming interface,
- UART interfaces to the linux kernel brought out via USB interface and a serial interface to be used with external programmable power supplies through the Patch Panel,
- an ethernet core with DMA access to the DRAM,
- access to FPGA fabric pins realized by a general purpose I/O module (GPIO),
- two SPI modules for read and write operations to flash memory chips on the PCB
- and a controller for external devices with a 32 bit wide address and data bus (External Peripheral Controller - EPC).

The main task of the GPIO module is to control and read the JTAG lines towards the four ladder IO Boards and the JTAG chain comprising the 16 ASICs of each ladder.

Attached to the EPC, user devices and registers are attached in the PPT firmware. Using the EPC, other logic in the FPGA fabric can be configured. Response to commands from XFEL is enabled through the EPC, for example.

The total number of registers and LUTs occupied by the processor and its interface to peripheral components is 20075 (registers) / 21554 (LUTs) or 5% (registers) / 3.5% (LUTs) of the available slices. The processor runs at 100 MHz. The ethernet connection speed has been measured between 2000 and 3000 kByte/s for receiving, and about 1000 kByte/s for sending.

While being sufficient for the DSSC application, the low speed of the MicroBlaze architecture has been addressed by Xilinx by integrating an ARM-based processor core on the FPGA die [83]. Suitable devices based on the Kintex-7 FPGA with sufficient numbers of gigabit transceivers are now available in the Zynq family during the writing of this thesis.

A.3 Software

The MicroBlaze processor runs a standard linux kernel, cross-compiled for the MicroBlaze architecture. While this is a standard procedure, some aspects must be considered. First, during the build of the linux kernel, a description of the hardware architecture must be provided. Mainly the memory addresses of the peripheral blocks must be known for the processor to properly address control and data registers. Second, a root file system can be prepared and included in the kernel binary. The root file system will be mounted during the boot procedure and may contain a basic set of user software. In the case of the PPT, the BusyBox software package is used to provide common

linux utilities in a small footprint [84]. More DSSC-specific software for access to the board serial number, board and detector configuration, and even a lightweight webserver to view the system status are provided.

The kernel sources itself had to be changed due to flaws in the implementation of the SPI device driver. Only a default bus number is assigned to each SPI devices, even if several devices are available in the processor design. More serious, the use of the STARTUPE2 primitive in the SPI device for the FPGA bitstream flash memory was necessary. The STARTUPE2 primitive allows to control the configuration pins from user logic after the FPGA has been programmed. This is used in the PPT implementation to allow reprogramming of the flash memory with files received over the ethernet connection. However, the STARTUPE2 primitive ignores the first three clock cycles from user logic. During the boot process, the kernel tries to identify the flash memories connected via SPI, but fails to correctly to do so due to the missing clock cycles. The kernel is therefore patched to simply run the identification procedure twice.

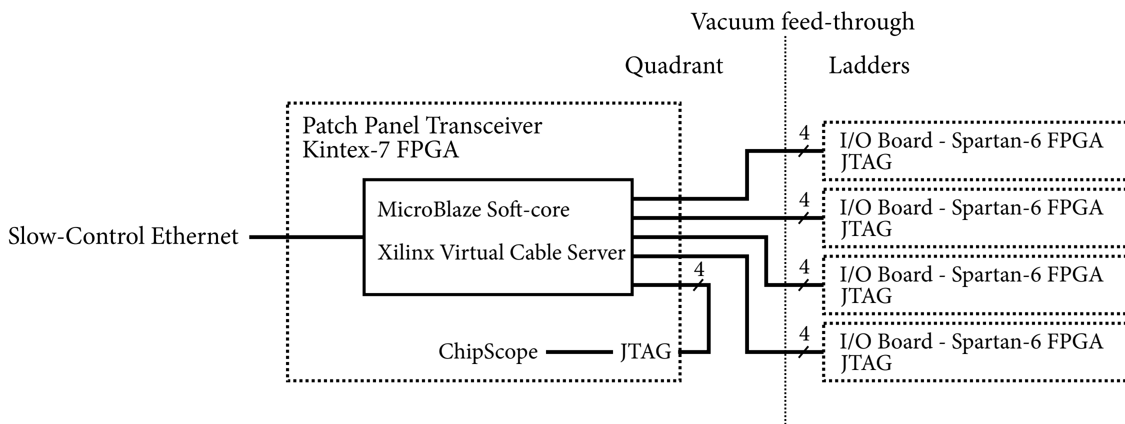

Figure A.2: Connection scheme of the FPGA JTAG signals in the DSSC system. The I/O board FPGAs are programmed by the MicroBlaze. The Xilinx Virtual Cable Server allows access to the ChipScope debugging cores in each FPGA in the DSSC system through the PPT ethernet connection.

The I/O Boards of four ladders are connected to the PPT (figure A.2). The FPGAs on the IOBs are programmed via JTAG pins accessed by the MicroBlaze. A software running on the processor decodes the JTAG commands in the programming files and sets the programming pins accordingly, monitoring the proper output from the I/O Board FPGA.

An important debugging tool for Xilinx FPGAs is provided in the ChipScope tool. The ChipScope cores for FPGAs allow analysis of logic signals in the FPGA fabric without putting them on output pins. Instead, the signals to be analysed are sampled and stored in FPGA-internal memory by extra logic inserted in the user design. Such cores have been implemented in both the I/O Board and the PPT design. The ChipScope cores are accessed through the FPGA JTAG pins. A dedicated software on the MicroBlaze accesses the JTAG pins of the I/O Boards and the PPT FPGA itself to make the ChipScope cores available via ethernet. This feature allows debugging of the digital reprogrammable parts of the detector without any extra cables like the dedicated Xilinx programming cable connection usually needed.

The complete detector control is realized by a server process running on the PPT, the SlowCon-

trolServer. The lightweight server process opens a socket on the unreserved port 2384, allowing one connection from a control PC running the DSSC control software. The server interprets the command messages received via ethernet and reacts accordingly by accessing the external peripheral controller (EPC) by direct memory access, or by starting other processes. Complex operations have been implemented in this server in the meantime, e.g. allowing the full initialization of a detector ladder through a single command.

A.4 Bootloader

The start-up phase of the hard- and software on the Patch Panel Transceiver is completely automated and comprises several stages.

First, the FPGA configuration bitstream of about 11 MB size is loaded by the FPGA via SPI, the processor is contained in the bitstream with a first bootloader program included in the instruction and data registers. The bootloader software copies the binary image of the Linux (32 MB size) from another flash memory to the DDR3 memory, the external memory used by the processor. Subsequently, the bootloader executes a jump to the first address of the Linux image, thereby starting the boot of the operating system.

The boot sequence is started without interaction needed after power-up of the board or after a reset, which is triggerable by the MicroBlaze through a Xilinx primitive[1] and thus accessible from the user interface. The time needed from power-up or reset until start-up has finished and the PPT is ready for user interaction is about 4 minutes. The speed of the copy process between SPI flash and FPGA resp. DDR3 is the main limiting factor, which could be optimized in the present design by changing to a Quad-SPI interface for the flash chip. Moreover, flash chips with dedicated 'fast read' commands with a higher frequency for reading larger amounts of data are available. These vendor-specific commands are usually not implemented by off-the-shelf IP cores, requiring the development of custom logic for the interface. For the given application, a faster start-up time was not necessary and has not been pursued.

Since both flash memory chips are accessible to the processor and the operating system, the memory chips can be written through the slow-control ethernet connection. Updates can be therefore be transferred to the control system without the need for another physical connection or further dedicated hardware, e.g. a Xilinx programming cable.

The previously mentioned control, updating and debugging tools have proven themselves viable during several months of prototype usage in lab environments as well as in testbeams at synchrotron beamlines.

[1] Internal Configuration Access Port (ICAPE2) primitive

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