Assessment of Rear-Surface Processing Strategies for III–V on Si Multijunction Solar Cells Based on Numerical Simulations

Diego Martín-Martín, Elisa García-Tabarés, and Ignacio Rey-Stolle

***Abstract*— The manufacturing of high-efficiency III–V on Si multijunction solar cells needs the development of hybrid, i.e., adapted to both families of materials, solar cell processing techniques, able to extract the full photovoltaic potential of both the subcells. This fact especially impacts the processing of the silicon rear surface of the tandem, which cannot receive treatments commonly used in the single-junction Si solar cell industry [Al-back surface field (BSF), thermal SiO_2, and so on], since these would result in an excessive thermal load that would deteriorate the III–V upper layers (top cell, tunnel junction, and buffer layer). However, the Si bottom cell requires an advanced design with good rear passivation, a good ohmic contact, and good carrier selectivity, so that its contribution to the efficiency of the tandem is maximized. Accordingly, in this paper, several low-temperature compatible rear-surface passivation techniques for the Si bottom subcell in a monolithic III–V/Si tandem solar cell are explored. In particular, aluminum BSFs, passivated emitter and rear cell (PERC)-like architecture, passivated emitter and rear locally diffused (PERL)-like architecture formed with low thermal loads, and heterojunction with intrinsic thin layer (HIT)-like processes are assessed using numerical simulations, and a comparison of the Si bottom cell performance for the mentioned alternatives in a GaAsP/Si dual-junction solar cell is presented.**

***Index Terms*— III–V on Si, multijunction solar cell, rear-surface passivation, Si processing.**

I. Introduction

THE INTEGRATION of III–V semiconductors on Si substrates has received a lot of attention over the last years. As a result of this impulse, good quality metamorphic III–V materials and the first complete tandem devices have been reported, demonstrating great promise toward the achievement of highly efficient III–V/Si solar cells [1], [2]. The vast majority of the efforts in this direction have been focused on the optimization of the heteroepitaxial growth of the III–V compounds on Si [1]–[4], with the primary goal of the minimization of crystal defects. Nonetheless, little to no work has focused on optimizing the device configuration and its processing [following the conventional III–V jargon, by *processing* we mean the technological steps that take place after epitaxy to complete the manufacturing of the solar cell, namely, surface passivation, contact formation, and antireflection coating (ARC) deposition]. Typically, the few implementations of III–V/Si devices reported so far have used the processing strategies of III–V solar cells for both the front and back contacts [i.e., evaporated front grid and full rear-side metallization, as shown in Fig. 1 (left)] [1], [2]. While for the top side of the structure (i.e., the front side of the III–V top subcell), this provides a standard and excellent solution it is not so for the rear side (back surface of the Si bottom subcell). A full metal coverage of the rear side [Fig. 1 (left)] leads to intolerably high recombination losses. Accordingly, several works have highlighted the importance of rear-surface passivation in the Si bottom cell in GaAs/Si [5] or GaAsP/Si dual-junction solar cells (DJSCs) [6]. Therefore, in order to fully exploit the efficiency potential of the tandem III–V/Si solar cell, the Si bottom subcell needs a more advanced processing—closer to what is done in conventional single-junction silicon photovoltaic (PV) technology—that provides good rear passivation in addition to a good ohmic contact and good carrier selectivity [6]. In order to determine the best technological solution for this problem, in this paper, we review the restrictions of III–V/Si structures regarding rear-side passivation (as compared with the conventional single-junction Si solar cell technology) and analyze using numerical simulations the performance of a Si subcell in GaAsP/Si metamorphic structure with an ideal back surface field (BSF) and several adapted rear processing alternatives, namely, aluminum BSFs, passivated emitter and rear cell (PERC)-like architecture, passivated emitter and rear locally diffused (PERL)-like architecture formed with low thermal loads, and heterojunction with intrinsic thin layer (HIT)-like backside processing, to produce highly efficient bottom subcells for III–V/Si tandems.

II. Potential of an Ideal Back Surface Field

One of the most direct approaches for the rear-side processing in p-type Si solar cells is the incorporation of a p^+

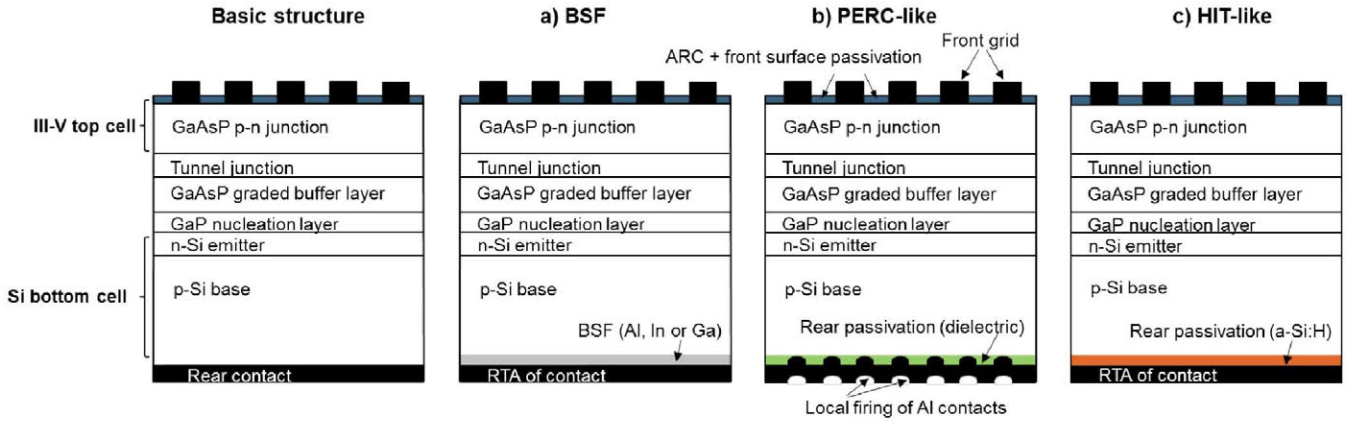

Fig. 1. Schematic of the suggested GaAsP/Si DJSC structures. Left: basic structure. Right: reviewed alternatives. (a) BSF structure. (b) PERC-like structure, with local rear contacts. (c) HIT-like passivating scheme.

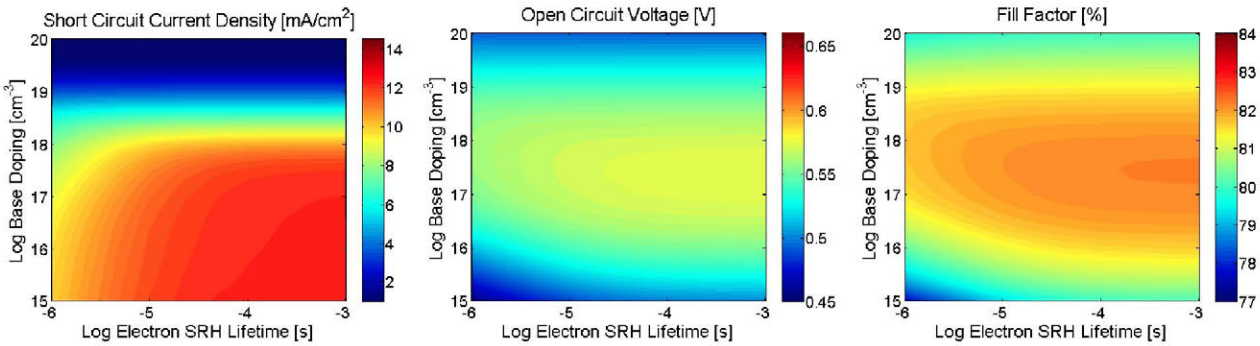

Fig. 2. Performance of the n/p Si bottom cell *basic structure*, in a GaAsP/Si DJSC structure under 1-sun AM1.5G, as a function of base doping and minority carrier (electron) lifetime and with a GaP/Si IRV of 10^6 cm/s (without ARC). Left: J_{SC}. Center: V_{OC}. Right: FF.

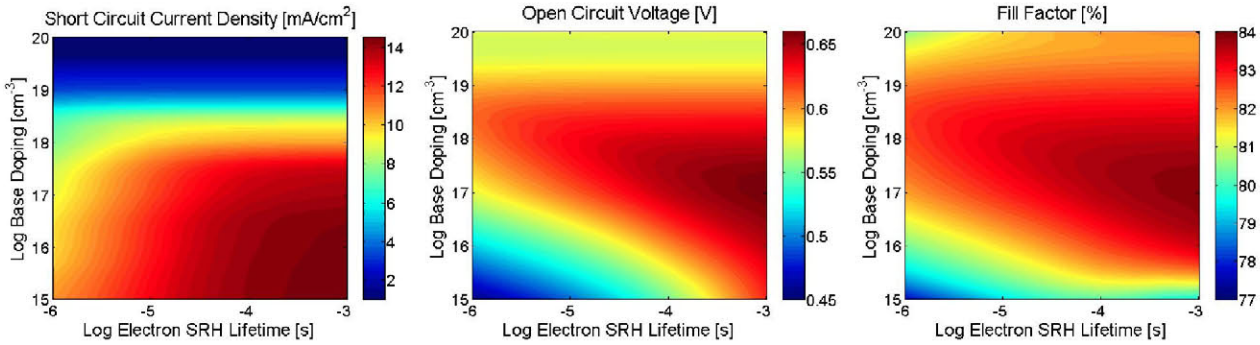

Fig. 3. Performance of a n/p Si bottom cell with an ideal BSF, in a GaAsP/Si DJSC structure under 1-sun AM1.5G, as a function of base doping and minority carrier (electron) lifetime and a GaP/Si IRV of 10^4 cm/s (without ARC). Left: J_{SC}. Center: V_{OC}. Right: FF.

layer to create a BSF [7]. The p^+-doped region improves the quality of the semiconductor–metal contact and keeps the minority carriers away from the highly recombining rear interface. To quantify its influence when Si forms the bottom active subcell in a GaAsP/Si DJSC, J_{SC}, V_{OC}, and Fill Factor (FF) under 1-sun AM1.5G illumination have been calculated for a n/p Si bottom cell, with no rear passivation [basic structure in Fig. 1 (left)] and with an ideal 1-μm thick, 10^{20} cm^{-3} uniformly doped BSF [Fig. 1(a)], as a function of the Si bulk (electron) Shockley–Read–Hall (SRH) lifetime and substrate doping. The results are shown in Figs. 2 and 3, respectively. Figs. 2 and 3 show how the presence of the BSF not only yields the expected improvement of the 1-sun performance (maximum J_{SC} goes from 12.6 to 14.4 mA/cm^2 and maximum V_{OC} from 570 to 660 mV) but also makes that both J_{SC} and V_{OC} cease being limited by surface recombination, to become dominated by bulk phenomena. Consequently, any increase in the minority carrier lifetime in the Si subcell would produce a corresponding increase in its PV performance.

However, creating ideal BSF layers in III–V/Si structures is far from being easy. In particular, the key limitation of the

process stems from the fact that it is not possible to treat the samples at high temperatures for long times once the epitaxial growth of the III–V materials has taken place. If this was done, III–V buffer layers and tunnel junctions would be noticeably degraded as a result of the high-thermal load. This fact hampers the use of conventional well-established processes of the Si PV industry once the III–V layers have been epitaxially grown on the substrate. Therefore, the development of a hybrid postprocessing technology to preserve the high-quality III–V/Si structure that is compatible with both the materials (i.e., Si and III–V semiconductors) needs to be addressed.

III. Alternatives for Low-Temperature Rear-Side Processing of the Si Bottom Subcell

This section reviews the suitability of three strategies (schematically depicted in Fig. 1) for III–V/Si solar cell processing to obtain a high-quality passivation of the rear Si surface without exposing the III–V part to high-thermal loads, which also would help maintain high bulk carrier lifetimes in the Si subcell through the processing. The performance for each strategy is analyzed and compared using the numerical simulations done with Silvaco ATLAS [8]. The simulated Si subcell structure includes the upper layers in a complete GaAsP/Si metamorphic DJSC. It consists of a 90-nm, 2×10^{18} cm^{-3} n-type epitaxial Si emitter on a 300-μm 2×10^{15} cm^{-3} p-Si base. Regarding the III–V part, it includes a 250-nm n-GaP nucleation layer followed by a ten-step compositionally graded 2.5 μm thick n-GaAsP buffer ($0.07 \leq y \leq 0.70$). The buffer is caped with a thick 2-μm n-$GaAs_{0.7}P_{0.3}$ layer ($E_G = 1.78$ eV), which simulates the absorption of the top cell. A moderate concentration of crystallographic defects is assumed at the GaP/Si interface, and thus its interface recombination velocity taken in all simulations is 10^4 cm/s. No surface charge is considered at the GaP/Si interface. All the simulations have been done without ARCs. More details of the simulated structure can be found in [6].

In the quest for these strategies, we have only focused on the alternatives that would be performed after the epitaxial growth. It could be argued that some other alternatives for rear passivation could be implemented before the epitaxial step. In this way, the growth of the III–V layers would neither be degraded nor influenced by the subsequent high-thermal loads. Being this true, we believe that the epitaxial growth is probably the process with a higher impact on the production yield, and thus should be performed first (i.e., only wafers with a high-quality epitaxy should undergo subsequent processing).

A. Low-Temperature BSF

Today, full-area aluminum screen printed and alloyed rear contact is the most common approach for manufacturing the industrial p-type Si conventional solar cells, due to its simplicity and low manufacturing costs [9]. Al is typically fired in belt furnaces at ~750 °C–900 °C, leading to Al peak concentrations in the range of 10^{18}–10^{19} cm^{-3} [10].

As discussed in the Section II, due to the high-thermal load required, such conventional Al-BSF is not compatible with the III–V/Si structures. Any attempt to form a BSF must keep the thermal budget as low as possible. The alternative would be the use of very fast firing processes at medium-to-low temperatures (<700 °C) based on rapid thermal annealing (RTA). Candidate materials for this low-temperature BSF (LT-BSF) include not only Al but also Ga and In. In all the cases, shallow- and medium-doped rear diffusion profiles are expected. Rear-side processing would be completed by forming the back contact using Al evaporation or sputtering, followed by a second low-temperature annealing or RTA. A schematic representation of such a structure is depicted in Fig. 1(a).

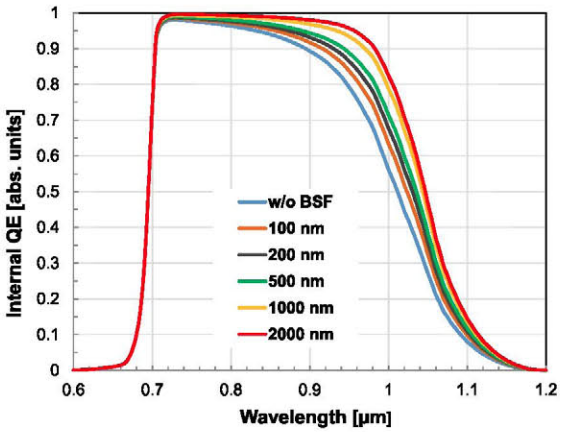

Fig. 4. IQE comparison for the Si bottom cell with ERFC-type LT-BSF as a function of the BSF depth ($N_{peak} = 10^{19}$ cm^{-3}).

Fig. 4 shows the simulated internal quantum efficiency (IQE) for the Si bottom subcell, assuming LT-BSF complementary error function (ERFC)-type shallow doping profiles, with a fixed peak doping concentration of 10^{19} cm^{-3} and a variable depth. Realistic electron SRH lifetimes of 500 μs in the p-type base have been chosen in all the cases [11]. Fig. 4 shows how the top $GaAs_{0.7}P_{0.3}$ layers (top cell + buffer) absorb all the radiation for the wavelengths up to 690 nm, according to its 1.78-eV direct gap. Regarding the performance of the LT-BSF, it is clearly seen how the improvement in the cell photoresponse is not very significant when working with shallow BSF layers (<500 nm). In these cases, the built-in electric field created by moderately doped shallow profiles is not strong enough to counterbalance the high recombination of the rear full-area contact.

To have a more complete picture of the LT-BSF impact on the overall Si bottom cell performance, the variation in J_{SC} (without ARC) and V_{OC} at 1-sun AM1.5G has been studied in a wider range of peak doping concentrations and depths. These results, summarized in Fig. 5, show that for peak dopings lower than 10^{19} cm^{-3}, obtaining a J_{SC} higher than 14 mA/cm^2 is only feasible for BSF depths larger than 1 μm. Shallower BSFs will only work relatively well if a peak concentration well within the 10^{19} cm^{-3} range could be eventually reached. As it is well established, the rear passivation has an even greater impact on V_{OC}. Without any rear passivation, the high saturation current density caused by the full-area rear contact decreases V_{OC} down to 524 mV; the value is in good

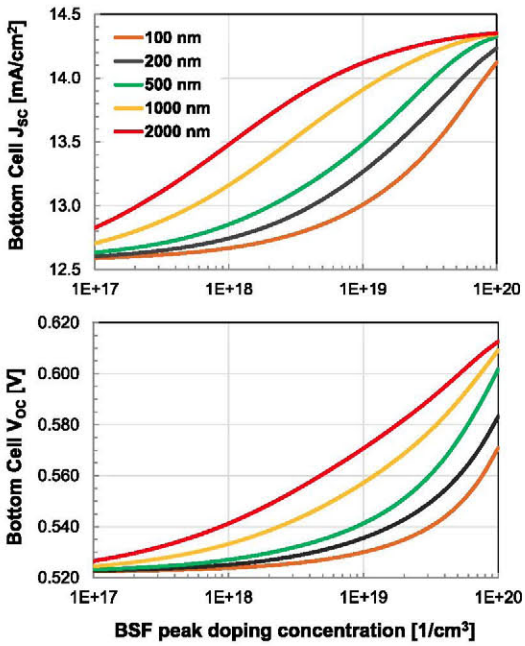

Fig. 5. J_{SC} (top) and V_{OC} (bottom) at 1-sun AM1.5G for the bottom Si cell with ERFC-type LT-BSF as a function of the LT-BSF peak doping concentration and depth.

agreement with the first published experimental data [12]. The LT-BSF approach provides little improvement on this baseline result. Getting some extra 50 mV is only feasible for $N_{peak} \geq 5 \times 10^{19}$ cm^{-3} and thickness $\geq$200 nm. V_{OC} exceeding 600 mV would only be possible for N_{peak} as high as 10^{20} cm^{-3} and thickness $>$500 nm, values that could be hard to get considering the low thermal load restriction of this approach.

B. PERC- and PERL-Like Rear Passivation

A second alternative for rear passivation would be to reproduce the also well-known PERC developed by Blakers *et al.* [13] in 1989. In this case, rear-surface passivation is obtained by depositing dielectric layers and using point metal contacts. In fact, this approach was developed to avoid the standard high-temperature surface passivation schemes in Si (as thermal oxidation). Typical candidates for p-Si are SiN_x [14], Al_2O_3 [15], or stacks of these layers and SiO_x [16] deposited by deposited by plasma-enhanced chemical vapor deposition (PECVD) or atomic layer deposition (ALD), at temperatures below 350 °C. Despite of being greatly dependent on the quality and composition of the dielectric layer and/or the presence of fixed charge, rear effective surface recombination velocities (SRVs) around or lower than 100 cm/s are regularly obtained with this approach [17]. In addition, backside processing would be completed using Al evaporation—or sputtering—followed by a laser process to form locally fired point contacts [Fig. 1(b)] [18]. The laser-fired contact (LFC) technique allows forming ohmic contacts between the Al layer and Si without the need for a photolithographic step. As the laser power, pulse duration and interval between pulses can be adjusted;

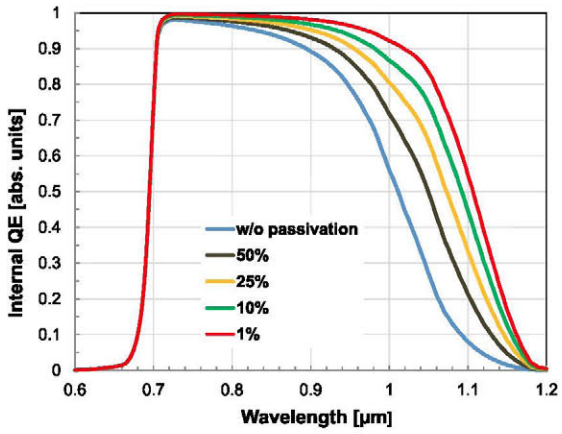

Fig. 6. IQE for the bottom Si cell including a 300-nm SiN_x + 1-μm Al rear layers, as a function of the rear contact coverage area (in percentage) for a 1 × 1 mm^2 GaAsP/Si simulation domain.

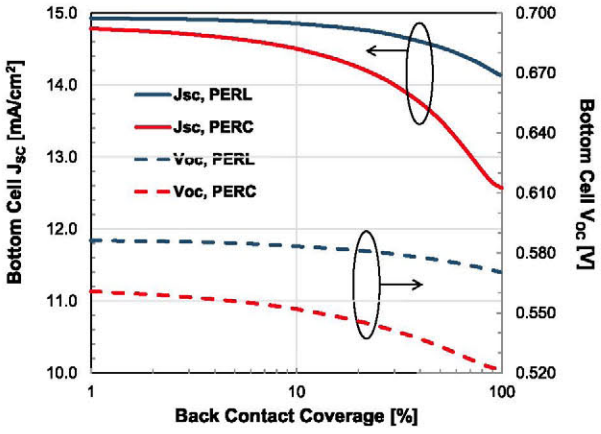

Fig. 7. J_{SC} and V_{OC} at 1-sun AM1.5G for the bottom Si cell including a 300-nm SiN_x + 1-μm Al rear layers as a function of the rear contact coverage area (in percentage) for a 1 × 1 mm^2 GaAsP/Si simulation domain. Red lines: PERC approach. Blue lines: local BSF under the contacts (PERL).

it is expected that the thermal budget for the top III–V layers could be kept within reasonable limits.

Fig. 6 shows the simulated IQE for the Si bottom cell of a device as the one depicted in Fig. 1(b) that includes a 300-nm SiN_x + 1-μm Al rear layers, as a function of the rear contact coverage area (in percentage) for an SRH electron lifetime of 500 μs. The rear passivation under the dielectric is modeled by setting an effective back SRV of 100 cm/s (no dielectric fixed charge at the interface is used). Fig. 6 clearly shows that the lower the rear metal-contacted area, the greater the photoresponse in the infrared region. This result is not only due to the reduced recombination in the contact area but also due to the greater quality of the rear Al mirror, which has been greatly improved by the insertion of the dielectric layer. In the end, this mirror reflects the nonabsorbed part of the incoming spectrum, enhancing the infrared response of the solar cell. With this approach, values for J_{SC} (without ARC) at 1-sun AM1.5G as high as 14.8 mA/cm^2 are expected for a rear contact coverage area of 1% (see the red solid line in Fig. 7).

Interestingly, LFC processes under certain firing conditions allow to create p^{++}-doped regions under the contacts, which

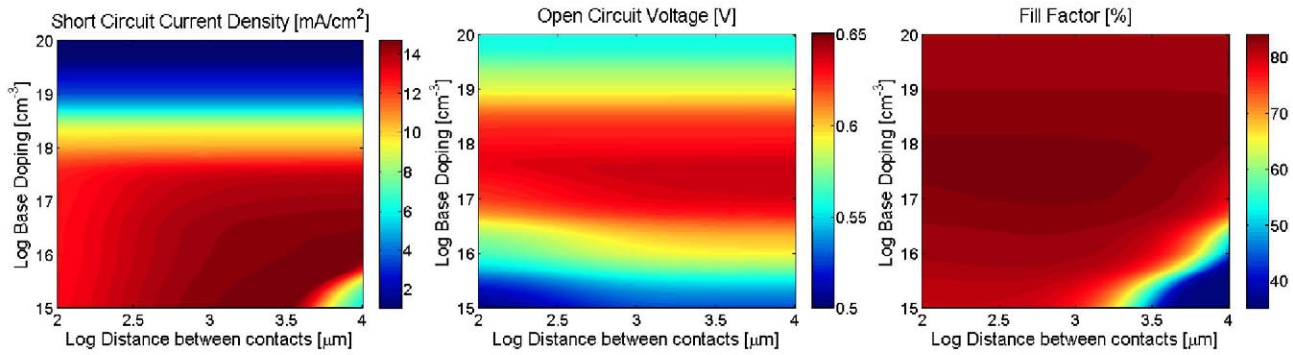

Fig. 8. Si bottom cell performance under 1-sun AM1.5G for a PERC-like structure with a typical laser-fired rear point contact of 100 μm in diameter, as a function of base doping and distance between the contacts (without ARC). Left: J_{SC}. Center: V_{OC}. Right: FF.

are beneficial not only to the achievement of low specific contact resistances in low-resistivity Si substrates but also to the formation of local BSFs that minimize recombination. This rear-surface passivation approach matches the well-known PERL cell structure, developed by Wang *et al.* [19] in 1990, with which 25.0% efficient Si cells were manufactured in 1999 [20]. Consequently, if a 2-μm-thick ERFC-type local BSF with a peak doping of 10^{19} cm^{-3} is assumed under the contacts, J_{SC} becomes almost independent of the contact coverage in the 1%–10% range, keeping the J_{SC} value as high as 14.9 mA/cm^2 (Fig. 7). The impact of adding the local BSF under the contacts is most marked in V_{OC}, obtaining at least 30 mV more than PERC-like Si cells while the contacted rear area lies within the 1%–10% range. The decrease in both J_{SC} and V_{OC} observed for the coverages from 10% to 100% is due to the progressive substitution of the dielectric-enhanced reflector by the fired Al layer, whose reflectivity and surface passivation properties are poorer.

In practice, the laser used to fire the rear contacts usually has a certain beam diameter, which results in a circular contact with a fixed area [18]. The rear point-contacted cell structure is then optimized by modifying the distance between the fired contacts. In this sense, we have studied the influence of the distance between the contacts together with the base doping on the Si bottom cell performance for a PERC-like structure. Fig. 8 (left) shows how the highest J_{SC} is obtained for a base doping of 10^{16} cm^{-3} and the distance between the contacts as high as 10^4 μm. However, FF is greatly decreased by the combination of a low-doped base and a distance between the contacts greater than 1–2 mm [Fig. 8 (right)], due to an increased series resistance in the base of the Si subcell. The highest V_{OC} [Fig. 8 (center)] of ~630 mV is reached for a doping concentration in the low 10^{17} cm^{-3} range (a fixed SRH lifetime of 100 μs is assumed for all doping concentrations). In summary, the Si bottom cell would maximize its performance for a substrate doping of 1–2 $\times$ 10^{17} cm^{-3} and a distance between the contacts in the 2–4-mm range.

C. HIT-Like Rear Passivation

The third and last approach considered in this paper to passivate the rear surface of the Si bottom subcell at low temperature is based on using hydrogenated amorphous Si.

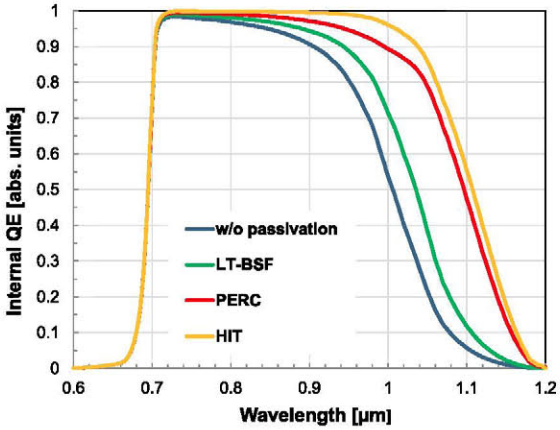

Fig. 9. IQE comparison for the Si bottom cell in a GaAsP/Si structure, under 1-sun AM1.5G illumination for standard (without passivation), LT-BSF (10^{19} cm^{-3} and 0.5 μm), PERC-like (1% contact coverage and effective rear SRV of 100 cm/s), and HIT (10 nm and effective rear SRV of 10 cm/s).

It consists of a thin (~10 nm) intrinsic a-Si:H layer deposited on the p-type c-Si followed by a p-type a-Si:H layer. This passivation scheme was used in the HIT Si solar cell developed by SANYO in 1990 [21]. Record efficiencies as high as 24.7% [22] and 25.6% (with interdigitated back contacts) by SANYO (now Panasonic) [23] have been confirmed in 2014 for HIT Si solar cells.

The use of a high-quality intrinsic a-Si:H layer is the key to achieving a very good rear-surface passivation, due to the effective reduction of the surface dangling bonds by hydrogenation, together with the BSF created by the c-Si/a-Si heterojunction. Rear effective SRV lower than 10 cm/s is easily reached with this approach, allowing V_{OC} as high as 750 mV in HIT solar cells at 1-sun illumination [22]. More interestingly, high-quality a-Si:H layers can be deposited by PECVD at very low temperatures (~200 °C), which makes this alternative an excellent candidate to keep the thermal budget of the III–V/Si structure to a minimum. The rear stack would be completed by evaporating a metal (i.e., Al) layer to enhance back reflection [Fig. 1(c)]. When passivating only the rear contact, a transparent ITO layer between the a-Si:H layers and the rear contact metal is not compulsory [24], though its presence improves the electrical contact and increases the internal reflectance at the rear surface [25].

TABLE I

TYPICAL CALCULATED VALUES FOR THE PERFORMANCE OF A Si BOTTOM CELL IN A GaAsP/Si STRUCTURE, UNDER 1-SUN AM1.5G FOR STANDARD (WITHOUT PASSIVATION), LT-BSF, PERC-LIKE, PERL-LIKE, AND HIT-LIKE

Alternative	Performance at 1-sun AM 1.5G			
	J_{SC} (mA/cm^2)	V_{OC} (mV)	FF (%)	Eff. (%)
Standard	12.6	524	80.8	5.33
LT-BSF	13.5	543	81.3	5.96
PERC-like	14.8	561	79.0	6.56
PERL-like	14.9	586	79.2	6.92
HIT-like	15.0	628	79.6	7.50

Fig. 9 shows IQE, simulated for a HIT-like passivated Si bottom subcell with 10-nm a-Si intrinsic/p-type layers, an Al 1-μm-thick back reflector, and assuming an effective back SRV of 10 cm/s at the c-Si/a-Si interface. The a-Si input parameters for the simulations are taken from [26]. IQE for the standard (without rear passivation), LT-BSF, and PERC-like alternatives are also included for comparison. More details are given in the caption of Fig. 9. Both the LT-PERC and HIT-like schemes are much more efficient in terms of enhancing collection and photon reflection for longer wavelengths, as compared with the low-doped shallow BSF present at the LT-BSF. However, the HIT-like scheme shows a higher IQE in the 900–1050-nm wavelength range as a result of its better rear-passivation properties.

To conclude the comparison between the reviewed alternatives, Table I shows the simulated Si bottom cell performance under 1-sun AM1.5G for each configuration. Compared with the nonpassivated cell, the LT-BSF, PERC-like, PERL-like, and HIT-like schemes lead to an increment in J_{SC} of 0.9, 2.2, 2.3, and 2.4 mA/cm^2, respectively (without ARC). Regarding V_{OC}, the calculated increments are 19, 37, 62, and 104 mV. Though the FF for the HIT-like is slightly lower (due to the higher series resistance of the intrinsic a-Si:H layer), it is by far the approach with which a larger improvement is expected, as a result of its excellent passivating properties, together with being the option that keeps the thermal budget of the III–V/Si structure to a minimum. Though the practical implementation of complete GaAsP/Si DJSC is still in an early stage [2], [3], future experimental efforts should be focused on validating these conclusions.

IV. CONCLUSION

There are remarkable differences between a conventional standalone Si solar cell and the Si subcell integrated into a III–V/Si solar cell stack. In the latter one, only the higher wavelengths reach the Si subcell, so they are in average absorbed farther from the front Si subcell surface, this front surface is passivated by the nucleation layer heterostructure, and there is no lateral conduction in the Si subcell emitter, which is typically manufactured by epitaxy and uniformly doped. In addition, once the III–V stack has been grown over the Si substrate, there is a huge limitation in the thermal load that the structure can handle without degrading the quality of the III–V upper layers. Then, to achieve highly efficient III–V/Si solar cells, the configuration of the Si bottom subcell has to be compatible with maximizing the device performance and maintaining the physical integrity of the tandem structure.

In that quest, this paper has reviewed using numerical simulations the adequacy of three well-known rear-surface passivation schemes to maximize the Si bottom cell performance in a GaAsP/Si DJSC while keeping the thermal budget as low as possible. First, an LT-BSF strategy is discussed. It is seen that the improvement in the cell performance is moderate, being basically driven by the peak doping concentration and depth attainable with an LT-BSF approach. A PERC- or PERL-like rear-surface approach combined with LFCs is much more effective. Finally, it is discussed how the most promising approach, combining the lowest processing temperatures and the highest Si bottom cell performance improvements, is based in using a HIT-like (rear intrinsic/p-doped a-Si:H) passivation strategy.

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