# Overview, equivalences and design guidelines of $v^1$ concept: a voltage mode control that behaves as a current-mode with near time-optimal response

Jorge Cortés, Vladimir Šviković, Pedro Alou, Jesús A. Oliver and José A. Cobos

***Abstract*—This paper summarizes the proposed $v^1$ concept, that explains how by only measuring the output voltage, designers have information about almost every signal of the power stage. Following the $v^1$ concept, the implementation of some ripple-based controls as a conventional voltage mode control or current mode control is studied. Based on these, it is explained how to design a traditional type-III voltage mode control to behave like a current mode control with near time-optimal response under load transients. The work is validated in simulations and experimentally on a 300kHz Buck converter.**

## I. Introduction

Applications with highly demanding load steps and dynamic voltage scaling (DVS) such as Point-of-Load converters and Voltage Regulator Modules (VRMs) need very fast controls in order to comply with the dynamic requirement and still maintain an output capacitor as small as possible.

Ripple-based controls are one popular solution to achieve a fast dynamic response. They are composed by a fast feedback (FFB) path and a slow feedback (SFB) path. The fast feedback path is a rippled signal with information about the power stage and it is responsible of the modulation of the duty cycle and the dynamic behavior of the control. The slow feedback path is an integrator designed to have a very low bandwidth and it is responsible to regulate the output voltage in steady state.

The $v^2$ control [1, 2] only uses the output voltage, but it behaves properly only with high ESR output capacitors [3]. In [4, 5], the inductor current is added to the $v^2$ control to stabilize it. On the other hand, [6], proposed in 2011, instead, to add the capacitor current information using only the output voltage, which allows the control to behave almost optimally under load transients [7, 8]. This control is named $v^2i_c$ (or "current-mode control of the output capacitor current" in a previous version from 2010 [9]). Using the capacitor current to improve the dynamic response is not a new concept since it dates back at least to 1986 [10], but [6] improves the idea by using a simple lossless sensor of the capacitor that only measures the output voltage and that takes into account the ESL of the output capacitor. In 2013, [11] proposed the same concept with a different implementation of the sensor of the current. Later in 2014, Google™ filed a patent including the same concept as in [9] but with a different sensor of the capacitor current [12].

Recently, [13] proved that some ripple-based controls can be implemented as a conventional voltage mode control with only one feedback path and measuring only the output voltage. Specifically, it was proven that the $v^2$ control can be implemented as a type-II voltage mode control achieving the exact same dynamic response. Also, the $v^2i_c$ control ($v^2$ with capacitor current compensation) can be implemented as a type-III voltage mode control under some conditions.
Based on this, [13] introduced the $v^1$ concept that explains how, in Buck-type converters, by only measuring the output voltage, designers have information about almost every signal of the power stage. By exploiting this feature, it was shown how the measurement of the output voltage is all that is needed to react almost optimally under load transients and that a voltage mode control can exhibit a kind of feedforward of the output current if designed as was proposed in [13].

This paper summarizes the findings in [13] in section II, highlighting the key points. Additionally, section III extends the work by providing design guidelines of the proposed design of voltage mode control. Section IV shows the experimental validation of the proposed design of voltage mode control and section V summarizes the contributions of the paper. The simulation results of the paper are obtained from the program Simplis.

## II. Summary of proposed $v^1$ concept and equivalences between different control techniques

Some ripple-based controls such as $v^2$ [1, 2] and $v^2i_c$ [6, 11] only sense the output voltage but they are in nature current-mode controls. This is because the output voltage has inherently information of the capacitor current (from the ESR of the capacitor or by using a trans-impedance amplifier). Also,

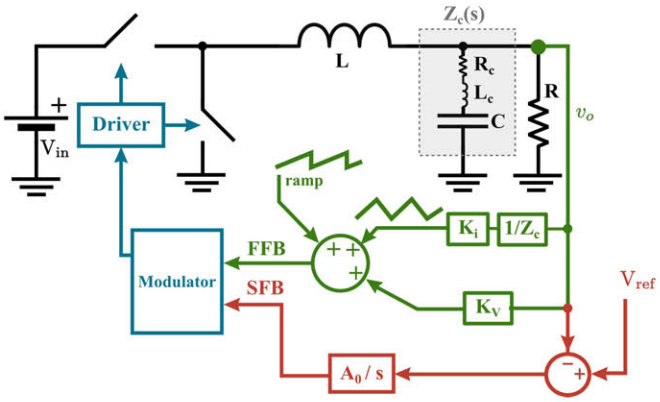



Figure 1: Scheme of $v^2 i_c$ sensing the capacitor current using only the output voltage. This sensor of the capacitor current is explained in [14].

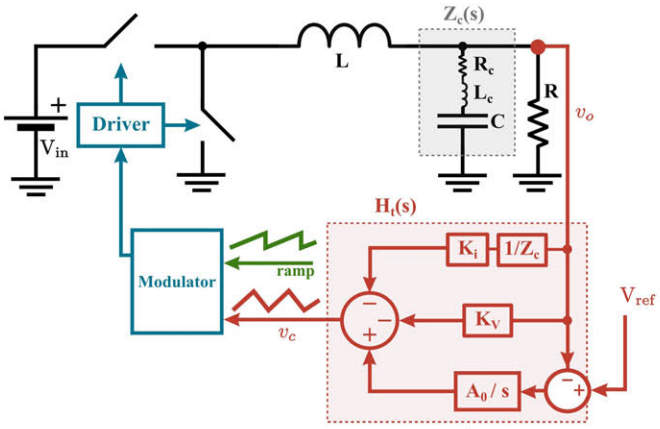



Figure 2: Alternative representation of $v^2 i_c$ control.

the capacitor current itself has combined information of the inductor current and the output current. This information about the output current is very important because it is what allows the $v^2$ and $v^2 i_c$ controls to behave almost time-optimally under a load transient. Additionally, the inductor current has information of the input voltage during the on-time. This concept of only sensing once the output voltage and using its inherent information about the power stage is what we call $v^1$.

Following the $v^1$ concept, the question then arises whether a traditional voltage mode control can be designed in a way so that this intrinsic information is exploited and, consequently, it behaves like a current-mode control with a very fast dynamic response. This voltage mode control could be modulated, as ripple-based and current-mode controls, with constant frequency (peak or valley), constant on-time, constant off-time or hysteretic modulations.

Figure 1 shows the structure of the $v^2 i_c$ control where the capacitor current is sensed with a trans-impedance amplifier with an impedance proportional to the impedance of the output capacitor. The $v^2 i_c$ control is implemented with two paths: the slow feedback path (SFB), that regulates the output voltage with an integrator, and the fast feedback path (FFB), composed by the output voltage, the sensed capacitor current and an optional external ramp.

Now, as an alternative equivalent representation, both the sensing of the capacitor current and the output voltage of the fast feedback path can be deducted to the output of the integrator (fig.2).

The equivalent regulator, $H_t(s)$, is then:

$$H_t(s) = \frac{A_0}{s} + K_v + K_i \frac{1}{Z_c(s)} \tag{1}$$

where

$$Z_c(s) = \frac{L_c C s^2 + R_c C s + 1}{Cs}. \tag{2}$$

Figure 3 shows the Bode diagram of the controller of equation (1). This regulator has an integral action, $A_0/s$,

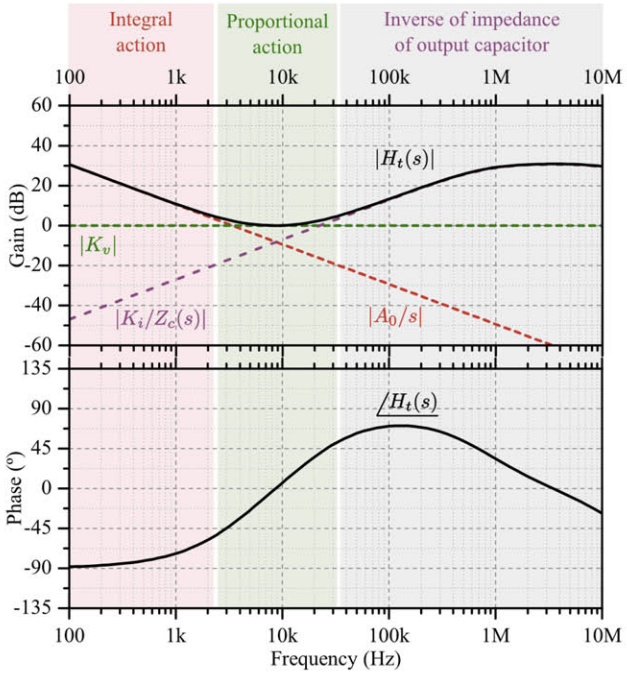



Figure 3: Decomposition of the frequency response of the equivalent regulator of $v^2 i_c$, $H_t(s)$.

which regulates tightly the output voltage, a proportional action $K_v$, that provides a zero to the regulator, boosting the phase, and a weighted estimator of the capacitor current, $K_i/Z_c(s)$ that converts voltage information into current information. This current sensor is crucial because it provides the control a feedforward of the output current, needed to obtain a near time-optimal response under load transients.

Equation (1) and figure 3 are very important because they synthesize the objective of the $v^1$ concept: in order to effectively use the current information hidden in the output voltage, the regulator needs to mirror the impedance of the output capacitor at high frequencies. In this way, the voltage mode control behaves as a current-mode control exhibiting a feedforward of the output current and it can be modulated with different modulation techniques. Of course, it is important to comment that a perfect matching of the

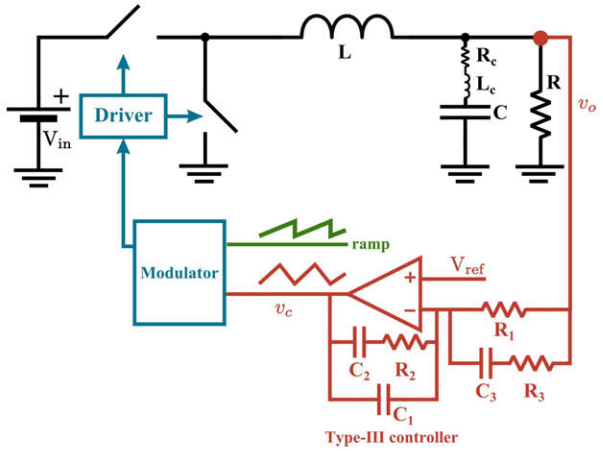



Figure 4: Scheme of a type-III voltage mode control.

impedance of the output capacitor is not possible in an actual product and, consequently, tolerances of the output capacitor due to aging, temperature and dc bias will have to be considered when designing the controller. Its effect on the stability can be studied and the control can be optimized by means of the procedure proposed in [15] and [16], respectively.

Using eq.(1) and fig.3, which reorders different feedback paths into a single regulator, it is found out that different ripple-based controls can be in fact implemented as a voltage mode control or as a current mode control. This equivalence between different control techniques can give designers important insights on how to design controls with a simple and cheap conventional implementation that behaves very fast under load transients.

The following subsections analyze the voltage mode implementation of the $v^2 i_c$ control (subsec.II-A) and the $v^2$ control (subsec.II-B) and the current mode implementation of the $v^2$ control compensated with inductor current (subsec.II-C)

### *A. $v^2$ compensated with capacitor current ($v^2 i_c$) $\leftrightarrow$ type-III voltage mode*

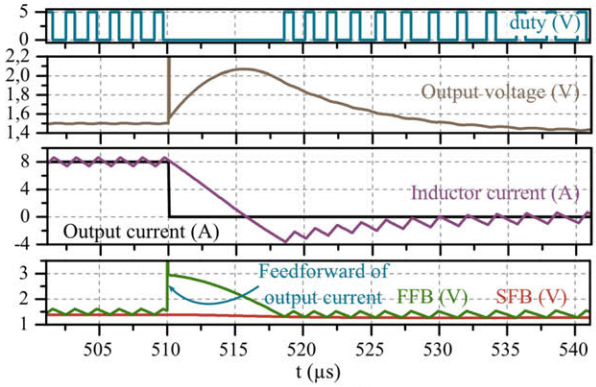
Eq.(1) can be solved for different impedances of the output capacitor. [13] shows that for low-Q capacitors ($Q < 0.5$), the $v^2 i_c$ control is equivalent to a type-III voltage mode control (fig.4) with regulator:

$$H_t(s) = A_0 \frac{\left(1+\frac{s}{z_1}\right)\left(1+\frac{s}{z_2}\right)}{s\left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_2}\right)} \tag{3}$$

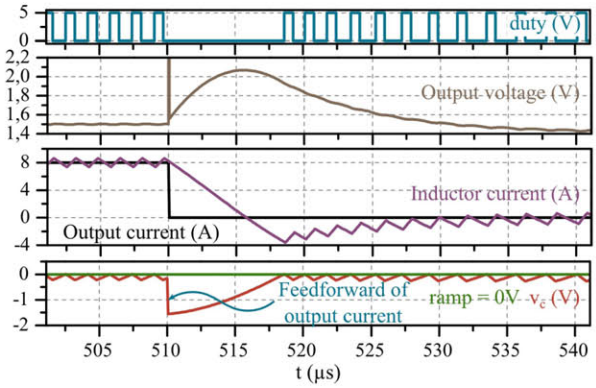
where

$$z_1 = \frac{A_0}{K_v}, \quad , z_2 = \frac{K_v}{K_i C}, \quad p_1 = \frac{1}{C R_c}, \quad , p_2 = \frac{R_c}{L_c}. \tag{4}$$

To validate this equivalence, simulations of the dynamic response of both controls are performed. The power stage has the following parameters: $V_{in} = 5V$, $v_o = 1.5V$, $L = 1.5\mu H$, $C = 42\mu F$, $R_c = 5m\Omega$, $L_c = 50pH$, $T_{on} \approx 660ns$. The control parameters are: $K_v = 1$, $K_i = 0.17$, $A_0 = 21.28k$.




(a) Implementation as a $v^2 i_c$ control




(b) Implementation as a type-III voltage mode control

Figure 5: Load transient response $8A \rightarrow 0A$ of $v^2 i_c$ control with constant on-time modulation and its equivalent implementation as a type-III voltage mode control for a low-Q output capacitor.

Also, no compensating ramp is added. The resulting exact passive elements of the type-III controller are (fig.4): $R_1 = 1k\Omega$, $R_2 = 193.44\Omega$, $R_3 = 5.27\Omega$, $C_1 = 54.48pF$, $C_2 = 46.95nF$, $C_3 = 37.93nF$. Of course, in a real implementation of the controller, the values of the passives would be rounded to the nearest standard value.

Figure 5 shows the response under a load step $8A \rightarrow 0A$ of the $v^2 i_c$ control (fig.5a) and its equivalent implementation as a type-III voltage mode (fig.5b). Notice that both designs achieve exactly the same dynamic response which is near time-optimal and exhibits a feedforward of the output current, seen in the instantaneous saturation to zero of the duty cycle. Notice that including an external ramp is not mandatory for this proposed design of voltage mode control because the ramp does not modulate but serves as a compensation to improve the stability of the converter.

On the other hand, for high-Q capacitors ($Q > 0.5$), the capacitance and the ESL of the output capacitor resonate and create two conjugate complex poles. The equivalent regulator, $H_t(s)$, is found to be [13]:

$$H_t(s) = A_0 \frac{\left(1+\frac{s}{z_1}\right)\left(1+\frac{s}{z_2}\right)}{s\left(1+\frac{1}{Q w_c}s+\frac{1}{w_c^2}s^2\right)} \tag{5}$$

where

$$z_1 = \frac{A_0}{K_v}, \quad z_2 = \frac{K_v}{K_i C}, \quad Q = \frac{\sqrt{L_c/C}}{R_c}, \quad w_c = \frac{1}{\sqrt{L_c C}} \tag{6}$$

As the regulator has complex poles, the exact equation (5) can be implemented only as a $v^2 i_c$ control. This is a very important feature of $v^2 i_c$ control because the phase variation of the complex poles has a larger slope compared to real poles. This means that the complex poles have less effect at frequencies below the resonant frequency compared to real poles which start decreasing the phase from approximately one decade below of the pole frequency. Consequently, a large phase margin can be achieved more easily.

However, an approximated version of the regulator can be implemented as a type-III voltage mode by placing the real poles at the same frequency as the complex poles:

$$H_t(s) \approx A_0 \frac{\left(1 + \frac{s}{z_1}\right)\left(1 + \frac{s}{z_2}\right)}{s\left(1 + \frac{s}{w_c}\right)^2} \tag{7}$$

This approximation is only valid if the bandwidth of the control is at least one decade lower than the resonance frequency of the output capacitor, $w_c$.

The section IV shows the experimental verification of the implementation of the $v^2 i_c$ control as a type-III voltage mode control for a high-Q output capacitor. Moreover, [13] shows additional validation by means of simulation results.

### B. $v^2$ control ↔ type-II voltage mode

Similarly as with the $v^2 i_c$ control, the feedback paths of the $v^2$ control can be reordered to derive an equivalent regulator. In the case of the $v^2$ control the fast feedback path is a proportional action and the slow feedback path is an integral path. If both actions are composed together in a single regulator, the resulting transfer function is the same as a type-II controller or PI controller (fig.6):

$$H_t(s) = A_0 \frac{1 + \frac{s}{z_1}}{s} \tag{8}$$

where

$$z_1 = \frac{A_0}{K_v}. \tag{9}$$

[13] shows the validation with simulation results of the implementation of the $v^2$ control as a type-II voltage mode control.

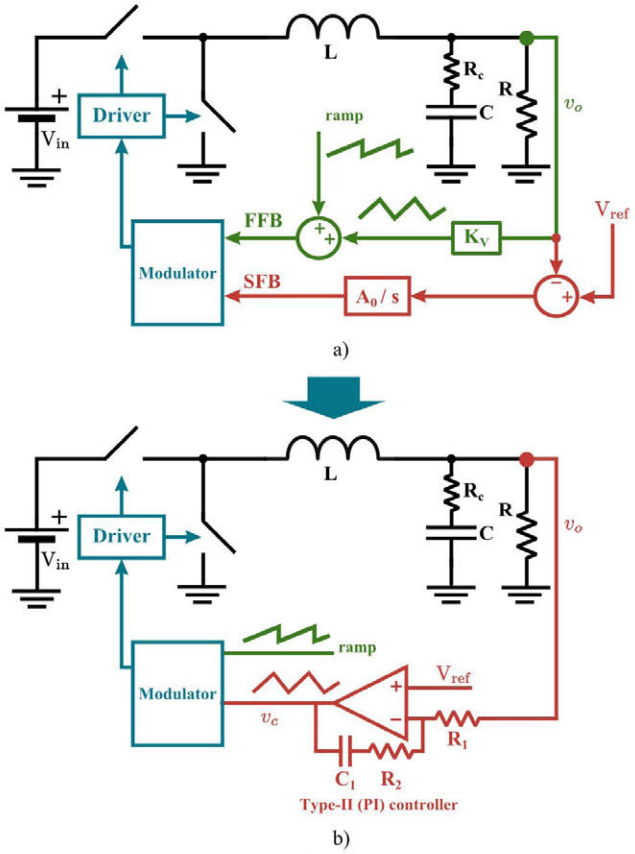



Figure 6: Implementation of a $v^2$ control as a conventional type-II voltage mode control.

### C. $v^2$ compensated with inductor current ↔ type-II current mode

In the $v^2$ control compensated with inductor current (fig.7a) [4, 5], the inductor current is added to the fast feedback path to avoid sub-harmonic oscillations and to improve the dynamic response for low-ESR output capacitors. As seen in the previous subsection, the $v^2$ control is equivalent to a type-II voltage mode control. Consequently, the feedback voltage paths of the $v^2$ control compensated with inductor current can be implemented as a single type-II controller. This way, the control is composed by a feedback path composed by the inductor current and an optional compensating ramp and a feedback path composed by a type-II controller regulating the output voltage (fig.7b). This is a conventional type-II current-mode control.

For the simulation results, the power stage has the following parameters: $V_{in} = 5V$, $v_o = 1.5V$, $L = 1.5\mu H$, $C = 42\mu F$, $R_c = 5m\Omega$, $L_c = 50pH$, $f_{sw} = 300kHz$. The control parameters are: $K_v = 1$, $K_i = 0.05$, $A_0 = 21.28k$ and the amplitude of the ramp is $0.8V$ (fig.7a). The resulting exact passive elements of the type-II current mode control are (fig.7b) are: $R_1 = 1k\Omega$, $R_2 = 1k\Omega$, $C_1 = 47nF$. Of course, in a real implementation of the controller, the values of the passives would be rounded to the nearest standard value.

Figure 8 shows the response under a load step $8A \rightarrow 0A$

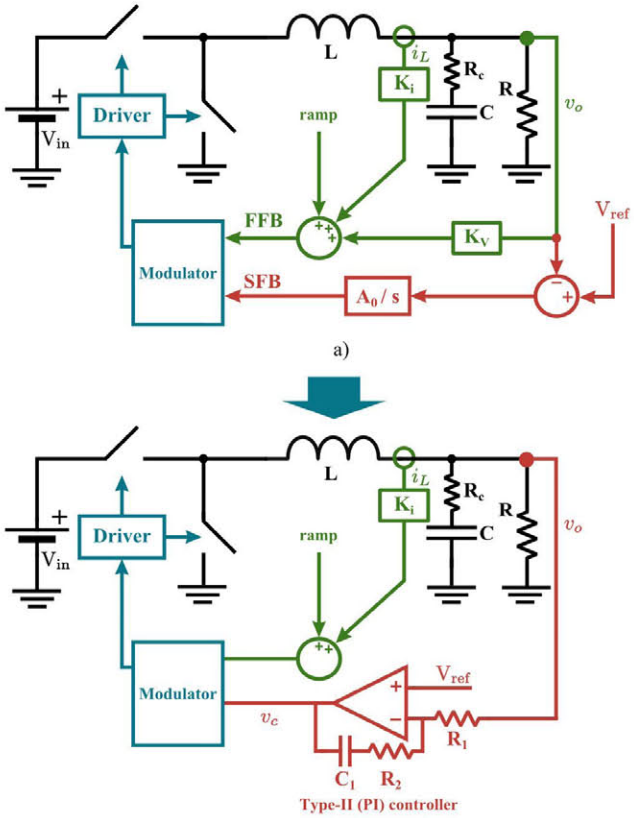
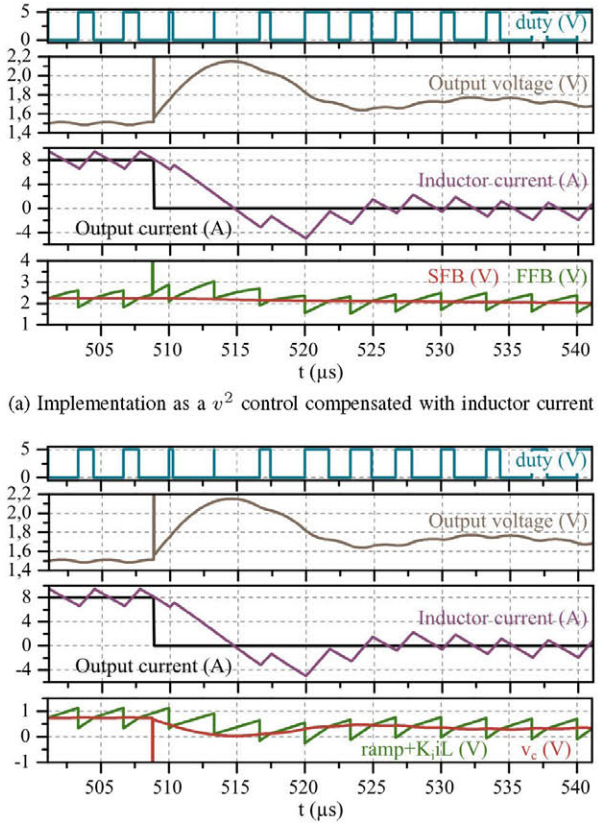



Figure 7: Implementation of a $v^2$ control compensated with inductor current as a conventional type-II current mode control.




(a) Implementation as a $v^2$ control compensated with inductor current

(b) Implementation as a type-II current-mode

Figure 8: Load transient response $8A \rightarrow 0A$ of $v^2$ control compensated with inductor current with constant frequency modulation and its equivalent implementation as a current mode control.

of the $v^2$ control compensating with inductor current and modulated with constant frequency modulation (fig.8a) and its equivalent implementation as a current mode control (fig.8b). Notice that both designs achieve exactly the same dynamic response.

## III. Design Guidelines of Proposed Voltage Mode Control Based on the $v^1$ Concept

As stated, the controls based on the $v^1$ concept behave like a current-mode control. Of course, this does not mean that they can be used to ensure current sharing in parallel converters, but that these controls use the current information of the output voltage. As opposed to traditional designs of voltage mode controls, the regulator of these controls does not act as a low-pass filter since high frequency information is allowed to go through. By doing this, a very fast transient response can be obtained. The downside is that the control is prone to sub-harmonic oscillations because side-band frequencies are not attenuated by the controller and are fed back to the modulation stage. Furthermore, the designs require the poles of the controller to match the zeros of the impedance of the output capacitor so deviations from the exact values might move the control closer to instability. Consequently, a careful design of the control is needed.

In order to design the voltage mode control based on the $v^1$ concept, the effect of the poles and the zeros of the equivalent controller needs to be analyzed. Recall also that the poles and the zeros are related to the gains of the feedback paths of their corresponding ripple-based control. The design guidelines for the equivalent regulator are as follows:

– The poles need to be placed at the same frequency of the zeros of the impedance in order to use the current information hidden in the output voltage, which is the key for the design and it is what we call the $v^1$ concept. If the output capacitor is a high-Q cap, the poles will be at the resonant frequency of the output capacitor. If the output capacitor has the ESR-zero well below the switching frequency, then no poles (besides the pole in the origin) are included in the controller and the regulator is implemented as a type-II controller.

– The zero placed at the higher frequency, $z_2$, of the regulator determines for this design the recovery time and sets the phase margin of the control. In general, if the control does not saturate the duty cycle, the zero placed at the higher frequency of the controller determines the settling time under a load transient [17]. As the proposed design of this voltage mode control typically saturates the duty cycle until the deviation of the output voltage is minimized, it can be assumed that the second zero $z_2$ approximately determines the recovery time of the control, $t_r$, which is the time from the maximum deviation of the output voltage to the settling of the

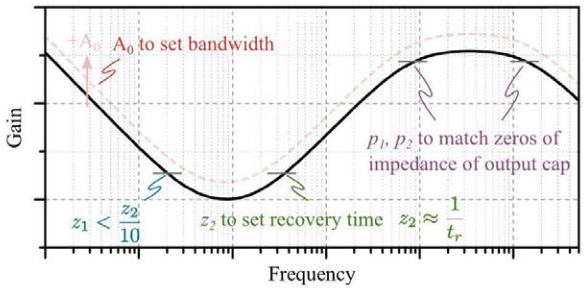



Figure 9: General design guidelines based on the $v^1$ concept of the equivalent regulator of a $v^2 i_c$ control and its implementation as a type-III voltage mode control.

output voltage. This can be seen for example in fig.5, where the second zero of the regulator is $z_2 = 143.5krad/s$ and the predicted recovery time is therefore $t_r \approx 7\mu s$, which agrees well with the simulation results. Consequently, from (6), $z_2 = K_v/(K_i C) \approx 1/t_r$. This is the same design guideline obtained in [11] from the Describing Function modeling. Additionally, $z_2$ needs to be placed so that the phase margin is at least larger than $60^o$ to avoid a peaking in the output impedance [17].

– The first zero $z_1$ is placed at least one decade below the second zero $z_2$ to decouple their effects on the dynamic behavior in the same way as a ripple-based control where there is a fast feedback path and a slow feedback path.

– The gain $A_0$ is set so that the required bandwidth is achieved. In order to achieve a fast dynamic response, a bandwidth of one fifth of the switching frequency $\triangle B = f_{sw}/5$ is recommended.

Figure 9 shows visually the proposed design guidelines of the $v^2 i_c$ control and its implementation as a type-III voltage mode control.

Besides these design guidelines, the modeling and equivalent circuits based on the Describing Function [18, 19] can be used to provide physical insight of the converter. After arriving to a first initial design, a more accurate analysis is needed to account for tolerances of the parameters and mismatches of the current sensor. In [15], a methodology that takes into account all the above is proposed to evaluate the stability of converters based on discrete modeling and Floquet theory. With these tools, an optimization algorithm can be created that designs the controls to behave very fast while assuring robustness under the whole operation region, accounting for tolerances of parameters and sensing networks [16]. Additionally, a commercial simulation program that can work with switched-mode power supplies and frequency responses is a good supplementary tool to design the voltage mode control based on the $v^1$ concept.

## IV. Experimental validation

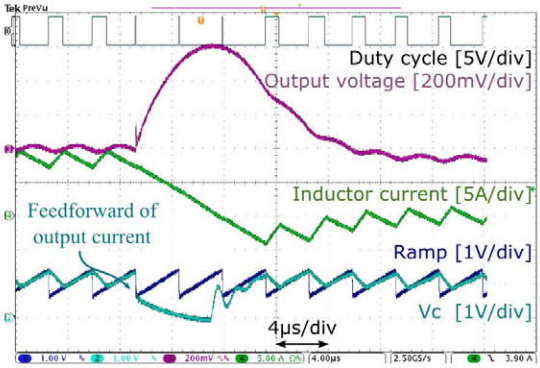
This section validates the proposed design of the type-III voltage mode control for the case of high-Q output capacitor, where its impedance has a resonance produced by the C and the ESL, and compares to its implementation as a $v^2 i_c$ control. This case is chosen to validate the proposed design methodology because it is the worst-case, since an approximation is required and an experimental validation is therefore needed. Remember that, for the case of a high-Q output capacitor, a type-III voltage mode control can be designed with the same response as $v^2 i_c$ only if the bandwidth of the loop gain is at least one decade below the resonance frequency of the output capacitor.

The power stage has the following parameters: $V_{in} = 5V$, $v_o = 1.5V$, $L = 1.5\mu H$, $C = 42\mu F$, $R_c = 5m\Omega$, $L_c = 1.2nH$, $f_{sw} = 300kHz$. The controls are modulated with constant frequency and the parameters of $v^2 i_c$ are (fig.2): $K_v = 1$, $K_i = 0.17$, $A_0 = 21.28k$. The amplitude of the compensating ramp is $0.8V$. The resulting passive elements of the type-III controller are (fig.4): $R_1 = 10k\Omega$, $R_2 = 2k\Omega$, $R_3 = 60\Omega$, $C_1 = 117pF$, $C_2 = 4.6nF$, $C_3 = 3.8nF$. Both controls are perturbed with a load step from 8A to 0A. The load step is placed at the beginning of the on-time on purpose because, in order to react optimally, an extremely fast reaction is needed to command an on-time as small as possible. Figure 10a shows the dynamic response of the $v^2 i_c$ control reordered as in fig.2 whereas fig.10b shows the dynamic response of the proposed design of type-III voltage mode control. Notice that both controls have the same dynamic response and exhibit a feedforward of the output current. This behavior that mirrors the output current in the output voltage is because the control is designed according to (1) and fig.3 and it is what allows a very fast reaction just after the load transient. Consequently, it has been shown in an experimental prototype that both $v^2 i_c$ and a type-III voltage mode control can achieve the same transient response.

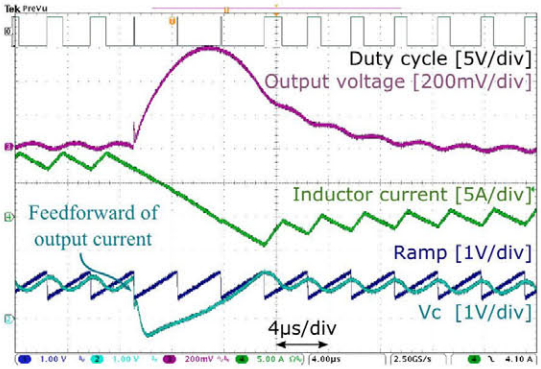
Figure 11 shows the comparison of the measured regulators, $H_t(s)$, and loop gains, $L(s)$, of $v^2 i_c$ and a type-III voltage mode control. The Bode 100 Analyzer is used to perform the measurements. Notice that the equivalent regulator of $v^2 i_c$ exhibits complex poles, as predicted. The position of the second zero and the real poles of the type-III voltage mode control does not match exactly the equivalent regulator of $v^2 i_c$ control because, in the implementation, it is needed to modify slightly the resistances and capacitances of the linear controller to use commercial values. Specifically, in the prototype the actual values are: $R_1 = 7.87k\Omega$, $R_2 = 1.6k\Omega$, $R_3 = 47\Omega$, $C_1 = 150pF$, $C_2 = 5.6nF$, $C_3 = 4.7nF$. However, the transient responses of both controls are almost exactly the same, so there is no need for a perfect matching of the poles and zeros.

## V. Summary and conclusions

This paper has proven both in simulation and in an experimental prototype that sensing the output voltage is all that is needed to react almost optimally under a load transient. This is because, in a Buck converter, the output voltage has information about almost all the signals of the power stage. This property is what we call the $v^1$ concept. By exploiting this feature, a traditional voltage mode can be designed to behave as a current-mode control and to achieve a near time-optimal load transient response. This does not mean that the control can be used for current sharing but that the current




(a) Load transient response $8A \rightarrow 0A$ of $v^2 i_c$ control




(b) Load transient response $8A \rightarrow 0A$ of proposed design of type-III voltage mode control

Figure 10: Experimental validation of the equivalence between the $v^2 i_c$ control and a type-III voltage mode control for a high-Q output capacitor.

information hidden in the output voltage is effectively used to react very fast. The basic idea to achieve this is that, at high frequencies, the regulator needs to behave as the inverse of the impedance of the output capacitor. This way, the voltage information is converted to current information and then, the voltage loop has information about the capacitor current and, consequently, about the output current. This provides the control a kind of a feedforward of the output current by only sensing the output voltage. Furthermore, an interesting property of the proposed design of voltage mode is that an external ramp is not mandatory because the ramp does not modulate in this design but serves as a compensation to improve the stability of the converter, like in a current-mode control.

Additionally, based on reordering the feedback paths into a single regulator, the paper has come to the conclusion that some ripple-based controls can be implemented with the same dynamic response as a conventional voltage mode control and current mode control. Specifically, it is concluded that:

- The $v^2$ control can be implemented as a type-II voltage mode control (or PI controller).
- The $v^2$ control compensated with inductor current can be implemented as a type-II current mode control.
- The $v^2$ control compensated with capacitor current ($v^2 i_c$ control) can be implemented as a type-III voltage mode control if low-Q output capacitors are used or if high-Q output capacitors are used and the resonance of the impedance of the capacitor is at least one decade below the bandwidth of the control.

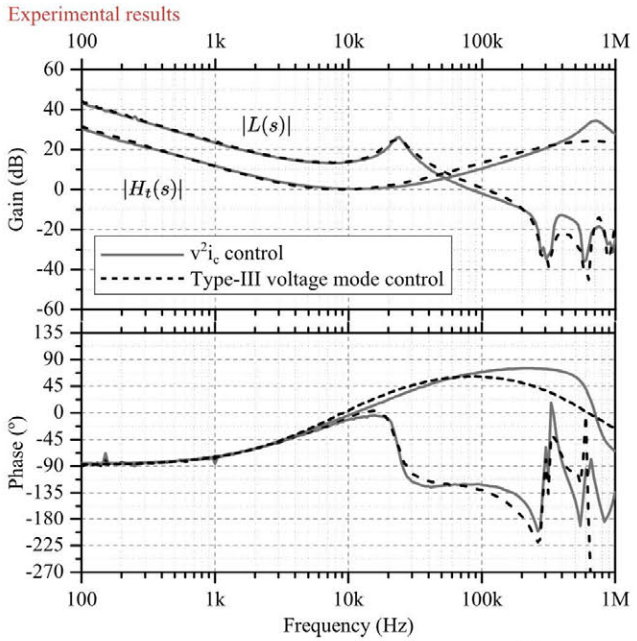



Figure 11: Comparison of the measured regulators, $H_t(s)$, and loop gains, $L(s)$, of $v^2 i_c$ and proposed design of type-III voltage mode control.

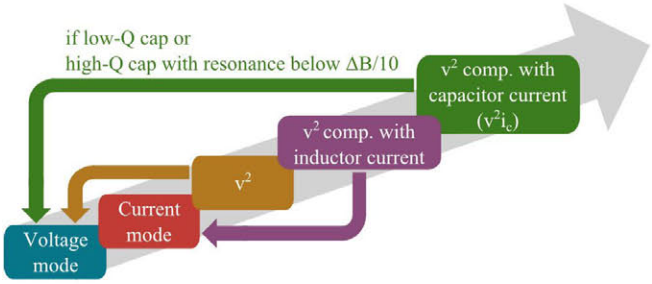



Figure 12: Equivalence between different ripple-based control techniques and a conventional voltage mode and current mode control.

Figure 12 summarizes this contribution. The paper also shows the relationship between the gains of the feedback paths of the ripple-based controls and the corresponding gain, zeros and poles of the regulator of the equivalent implementation as a voltage mode or current mode control.

Lastly, based on the $v^1$ concept and the equivalences between different control techniques, design guidelines are proposed to design voltage mode controls that behaves as a current mode with near time-optimal response. These can be applied either to a type-III voltage mode control or to a $v^2 i_c$ control by converting the gain and the zeros to the corresponding gains of the feedback paths. The design guidelines are summarized as follows:

1) Place the poles $p_1$ and $p_2$ at the same frequency of the zeros of the impedance of the output capacitor

to use the current information hidden in the output voltage.

2) Place the second zero $z_2$ based on the required settling time and to obtain at least $60^o$ of phase margin.
3) Place the first zero $z_1$ at least one decade below the second zero $z_2$.
4) Design the gain $A_0$ to achieve the desired bandwidth of the control.

With all this information, low-cost very fast controllers that only sense the output voltage can be designed and manufactured.

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