

# Optimizing diffusion, morphology and minority carrier lifetime in Silicon for GaAsP/Si dual-junction solar cells

Elisa García-Tabarés, Ignacio Rey-Stolle

Diego Martín

**Abstract**— Dual-junction solar cells formed by a GaAsP cell on a silicon bottom cell seem to be attractive candidates to materialize the long sought-for integration of III-V materials on Si for photovoltaic applications. In this study, we analyze several factors for the optimization of the bottom cell, namely, 1) the emitter formation as a result of phosphorus diffusion; 2) the growth of a high quality GaP nucleation layer; and 3) the process impact on the bottom subcell PV properties.

**Keywords**—III-V on Si, MJSCs, MOVPE, bottom cell.

## I. INTRODUCTION

The combination of III-V compounds and silicon (Si) in multijunction solar cells (MJSC) represents a long sought for device that would link the already demonstrated efficiency potential of III-V semiconductor MJSCs with the low cost and unconstrained availability of Si substrates. Among the different existing alternatives for their integration [1], currently the most developed technique is based on the direct epitaxial growth of III-V nucleation layers on Si- substrates. This approach consists on the growth of a GaP nucleation layer onto a Si substrate to obtain a III-V template free of nucleation-related defects [2-5] for growing subsequent III-V epitaxial layers. The grading of the lattice constant is achieved by a transparent step-graded GaAs<sub>y</sub>P<sub>1-y</sub> buffer to shift the lattice constant to the target top cell composition (Figure 1).

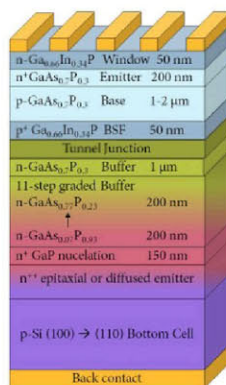


Figure 1. Metamorphic III-V on Si multijunction solar cell.

Several research groups have been working in the development of this structure. Most efforts have been directed

towards the optimization of key steps in the epitaxial growth of III-V compounds on Si [3, 6, 7]. However, it is frequently overlooked that all these efforts have to be compatible with the simultaneous formation of a high quality Si subcell, which is crucial for obtaining a highly efficient III-V-on-Si MJSC. The formation and optimization of the bottom cell implies not only the formation of an emitter, while preserving the silicon surface for subsequent heteroepitaxy; but also to develop an adequate growth routine for the III-V nucleation layer, which will act passivating the emitter. These points have to be achieved maintaining good photovoltaic (PV) properties in its base. This paper review each of these topics related to bottom cell optimization.

## II. EMITTER FORMATION

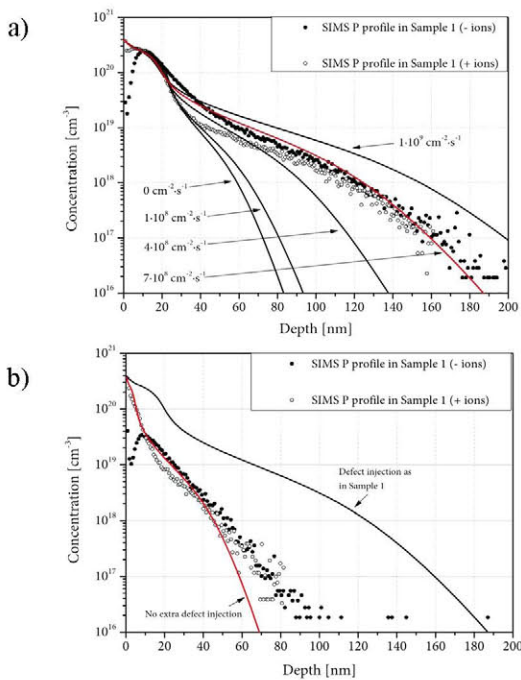
In our approach, the emitter of the bottom cell is formed as a result of the phosphorus (P) diffusion that takes place during the initial stages of the Metal-Organic Vapor Phase Epitaxy (MOVPE); being a complex process somewhat dissimilar to the traditional diffusion step in conventional PV technology, a well-known phenomenon which has been thoroughly studied in the past 40 years [8]. In a MOVPE reactor, the emitter is formed by the diffusion of P atoms resulting from the pyrolysis of a gaseous source, namely PH<sub>3</sub>, which will occur as a result of the high thermal load of the process.

A side effect of the formation of the emitter by P diffusion is the roughening of the Si surface. Although the exposure of substrates (before growth) to a short PH<sub>3</sub> flush has been proven to be beneficial for obtaining a high quality GaP morphology [9-11]; we have demonstrated [12] that the effect of long PH<sub>3</sub> exposures at temperatures ranging from 800-875 °C (required for obtaining a deep enough emitter) will lead to an important degradation of the surface due to Si hydridation and subsequent dimmer displacement [13, 14]. Therefore, in our quest for obtaining an optimized bottom subcell for a hybrid III-V-on-Si DJSC, we have assessed whether or not it is possible to form the emitter by P diffusion, while maintaining a high quality surface morphology on the silicon wafer.

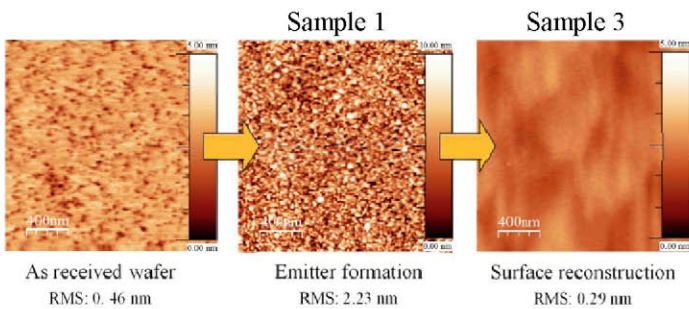
With the aim of analyzing the reported effect of the surface roughening on the emitter formation, the diffusion profiles for



several samples have been measured and theoretically simulated (Figure 2). These samples have followed the same thermal process (60 min. at 830 °C) but with different phosphine partial pressures (32.1 mbar and 0.7 mbar, respectively) and consequently, with different surface roughness (Figure 3). In this respect, when large amounts of PH<sub>3</sub> are present in the reactor during annealing (Sample 1), the surface morphology of the sample degrades; accordingly, an extra injection of point defects (i.e. silicon vacancies and self-interstitials) at the surface has to be assumed to simulate such deep profiles (Figure 2.a). The origin of this phenomenon has been postulated to be the hydration of Si surface atoms by PH<sub>3</sub>. On the contrary, when low partial pressures of PH<sub>3</sub> are used (Sample 3), not causing noticeable surface morphology degradation, the P diffusion profiles measured can be simulated without any extra addition of point defects (Figure 2.b) [15].



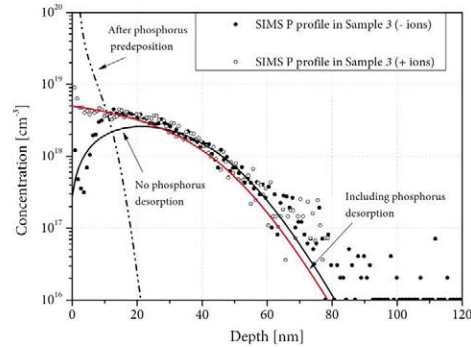
**Figure 2.** Comparison of the measured phosphorus SIMS profiles and the simulation (thin solid lines) for: (a) Sample 1 for a fixed vacancy injection of  $7 \cdot 10^{10} \text{ cm}^{-2} \text{ s}^{-1}$  and as a function of the Si self-interstitial injection; (b) Sample 2 for different defect injection levels.



**Figure 3.** Evolution of the RMS roughness (measured by AFM) during the emitter formation and subsequent surface reconstruction (by means of H<sub>2</sub> anneal).

In agreement to the previously mentioned morphology deterioration, PH<sub>3</sub> exposure must be minimized for obtaining a smooth Si surface, avoiding excessive Si surface roughness (Figure 3). However, according to our simulations, the use of weak PH<sub>3</sub> anneals leads to thin emitter, probably prone to show low shunt resistance [15]. Therefore, with the goal of achieving optimal emitter depths, while preserving the surface morphology, an alternative process was proposed. In this case, the formation of the emitter by exposing wafers to a high PH<sub>3</sub> partial pressure (Step 1) was followed by a H<sub>2</sub> annealing (Step 2) intended to recover the damaged surface morphology.

In order to understand the effect of the combined treatment on the P diffusion process, a comparison between experimental and simulated profiles has been carried out (Figure 4). A sample which has followed the two-step process (Sample 3) has been selected for establishing this comparison. This sample was exposed to our higher PH<sub>3</sub> partial pressure conditions (32.1 mbar) for only 10 min. at 830 °C, followed by a drive-in at 875 °C in a H<sub>2</sub> atmosphere for 90 min. Little surface degradation is expected (Figure 3) due to the short exposure time to PH<sub>3</sub> and thus no increase in the surface injection rates for vacancies and self-interstitials was assumed.



**Figure 4.** Comparison of the phosphorus SIMS profiles measured for Sample 3 and the profiles calculated with and without phosphorus desorption (solid lines). The calculated profile after P deposition has been also calculated for comparison (dashed line)

The black solid line in Figure 4 presents the simulated P profile for the two-step thermal treatment of Sample 3 using the nominal times and temperatures and a constant surface P concentration during the predeposition step. The fit between simulated and measured profiles is fairly reasonable in the tail region. However, at the first nanometers, the simulation predicts lower phosphorus concentrations after such a prolonged dopant drive-in. In fact, the simulation follows well the SIMS profile taken with negative ions which is known to produce an underestimation of the real surface concentration. The SIMS profile obtained with positive ions shows a nearly constant dopant concentration in the first 25 nm. According to our simulations, this is only possible if a certain amount of P is made available at the surface during the drive-in step when no PH<sub>3</sub> was injected. This unintentional extra supply of P can be associated to memory effects (i.e. P desorption from the MOVPE reactor walls and crucible). In summary, it has been

observed that when the exposure to  $\text{PH}_3$  is short enough and is followed by an annealing under hydrogen, the degradation in morphology is minimum (Figure 3) and the diffusion profiles associated to the redistribution of P can be calculated without considering extra injection of point defects but taking into consideration memory effects.

A comparison between the junction depths estimated from ECV profiles with the depths calculated from simulated P profiles is shown in Table 1. Moreover, this table includes RMS values for each sample, for quantifying the surface degradation. As shown by this table, the agreement between both values is fairly good, offering an indirect proof of the robustness of the simulation model developed.

**Table 1.** Description of MOVPE process followed by Sample 1 and Sample 2 (annealed under  $\text{PH}_3$ ); and Sample 3 (which was then annealed under pure hydrogen). A comparison between simulated and experimentally measured emitter depths was established for assessing the accuracy of the diffusion model developed.

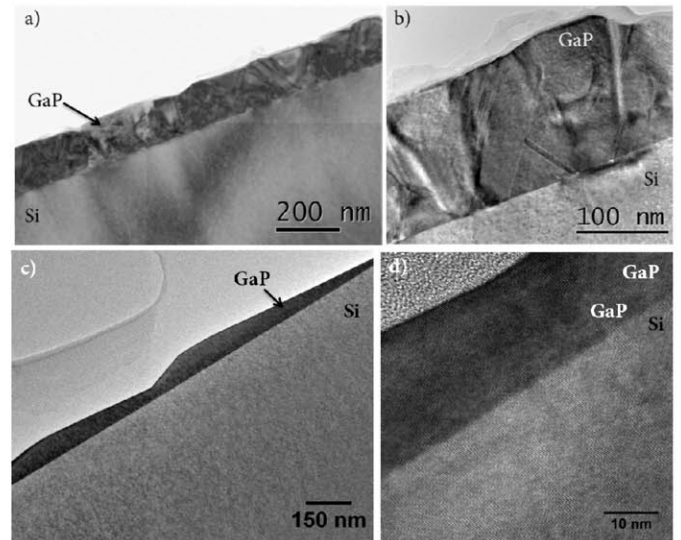
		Sample 1	Sample 2	Sample 3
Step 1	Temp (°C)	830	830	830
	Time (min)	60	60	10
	$\text{PH}_3$ (mbar)	32.1	0.7	32.1
Step 2	Temp (°C)	-	-	875
	Time (min)	-	-	90
	$\text{PH}_3$ (mbar)	-	-	0
<b>RMS (nm)</b>		2.23	0.37	0.29
Emitter depth	Simulated (nm)	95-100	22-23	84-90
	Extrapolated (nm)	97-100	75-80	110-121

### III. III-V/Si NUCLEATION

Once the emitter is formed and the surface is prepared for subsequent heteroepitaxial growth, a high quality III-V layer, intended to passivate the bottom cell emitter and to serve as a III-V template for subsequent growth, has to be grown. In this respect, different routines -framed within the continuous growth-mode approach- have been tested. In this approach, both precursors (i.e. TMGa and  $\text{PH}_3$ ) are introduced simultaneously on the reactor for GaP nucleation. Nevertheless, to enhance the wetting of GaP to Si, Si surfaces are initially exposed to a short flux of one of the precursors. In this respect, both possibilities (i.e. group-V and group-III pre-exposure) have been considered in literature; however, the group-V exposure is usually preferred for favouring a 2D growth [2, 4, 10, 11]. While  $\text{PH}_3$  has been generally used for the group-V exposure; it has been also reported the beneficial effects of  $\text{AsH}_3$  on preparing the surface for a high quality

nucleation [16]. After the initial pre-exposition to group-V precursors, the GaP nucleation took place.

With the aim of defining a practical parameter space for obtaining a high quality GaP on Si nucleation, high- and low-temperature approaches were considered. Moreover, different GaP thicknesses, growth rates or V/III ratios were used. From these studies, it was concluded that when the described substrate preparation is carried out, the exposure of samples to  $\text{PH}_3$ , followed by a low temperature nucleation results in a 3D growth, with total island coalescence. In this sense, the resulting surface is a continuous layer, with a good morphology but with a crystallographic quality which needs to be improved for minimizing the dislocation density (Figure 5.a and Figure 5.b). On the contrary, the use of high temperatures for the nucleation results in a heterogeneous 3D island-type growth, where islands are irregularly distributed along the Si surface. On the other hand, the exposure of wafers to  $\text{AsH}_3$  prior to the nucleation has been found to be a promising approach for a 2D nucleation. Although the morphology still needs to be improved for obtaining a smooth GaP layer, interesting results have been reported at high temperatures, observing a flat step-flow growth, parallel to the step edges, with a high structural quality, where no crystallographic defects were revealed within the GaP layer (Figure 5.c and Figure 5.d).



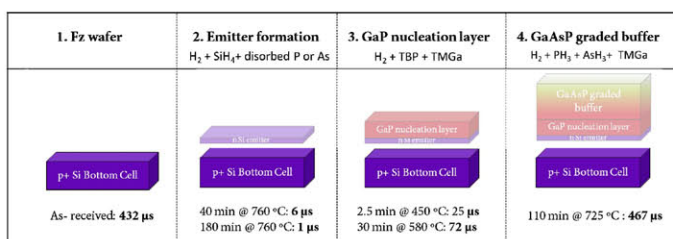
**Figure 5.** TEM images of a GaP layer grown on silicon which has been pre-exposed to  $\text{PH}_3$  (a and b) or  $\text{AsH}_3$  (c and d).

### IV. MINORITY CARRIER LIFETIME EVOLUTION

In conventional Si PV technology, it is well established that the minority carrier lifetime ( $\tau$ ) is not a constant material property but strongly depends on the thermal history and processing environment where the solar cell is manufactured [17]. Moreover, the Si minority carrier parameters will not only govern the PV performance of the Si bottom subcell, but in turn, will also impact the entire MJSC [18]. Therefore, it is important to fully characterize and understand the evolution of



the bulk Si minority carrier lifetime during the fabrication process used for the III-V/Si MJSC structure depicted in Figure 1. With the purpose of studying the effect of these environments on the PV performance of the solar cell, a scientific collaboration was established with the Ohio State University (OSU), which developed the III-V/Si structures, carrying out the optimization of the epitaxial routines and their structural characterization. These structures were used afterwards to study the effect of the III-V growth routines on the minority carrier lifetime. To visualize the evolution of minority carrier lifetime in the Si wafer throughout the growth process, a wide set of samples were grown, with interruptions at one of four different points in the process (1) the formation of the emitter by Si homoepitaxial growth - the alternative for the emitter formation selected by the OSU group-; (2) GaP heteroepitaxial nucleation; (3) bulk GaP film growth; and (4) thick GaAs<sub>y</sub>P<sub>1-y</sub> compositionally-graded metamorphic buffer growth. Figure 6 shows the evolution of this parameter during each of the above mentioned steps.



**Figure 6.** Evolution of average Si bulk minority carrier lifetime during the production sequence of a GaAsP/Si DJSC.

Initially, during the emitter formation by Si homoepitaxy, an approximately two order of magnitude reduction in the minority carrier lifetime was observed. This degradation is related to the formation of thermally-generated crystal defects and/or defect-impurity complexes (e.g. point defects, swirls, precipitates, etc.) which act as recombination centers. Following the GaP nucleation and thicker film growths the lifetime was found to increase by about an order of magnitude. The thick GaAs<sub>y</sub>P<sub>1-y</sub> graded buffer was then found to provide further recovery back to around the initial starting value. Lifetime recovery is attributed to the passivation of these recombination centers by fast-diffusing atomic hydrogen coming from precursor pyrolysis, especially the group-V hydrides (PH<sub>3</sub>, AsH<sub>3</sub>), during the III-V growth. These results indicate that the MOCVD growth methodology used to create these target III-V/Si solar cell structures has a substantial and dynamic impact on the bottom cell minority carrier lifetime.

#### Acknowledments

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