

Post-CMOS compatible high-throughput fabrication of AlN-based piezoelectric microcantilevers

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Abstract

A post-complementary metal oxide semiconductor (CMOS) compatible microfabrication process of piezoelectric cantilevers has been developed. The fabrication process is suitable for standard silicon technology and provides low-cost and high-throughput manufacturing. This work reports design, fabrication and characterization of piezoelectric cantilevers based on aluminum nitride (AlN) thin films synthesized at room temperature. The proposed microcantilever system is a sandwich structure composed of chromium (Cr) electrodes and a sputtered AlN film. The key issue for cantilever fabrication is the growth at room temperature of the AlN layer by reactive sputtering, making possible the innovative compatibility of piezoelectric MEMS devices with CMOS circuits already processed. AlN and Cr have been etched by inductively coupled plasma (ICP) dry etching using a $\text{BCl}_3\text{-Cl}_2\text{-Ar}$ plasma chemistry. As part of the novelty of the post-CMOS micromachining process presented here, a silicon Si (100) wafer has been used as substrate as well as the sacrificial layer used to release the microcantilevers. In order to achieve this, the Si surface underneath the structure has been wet etched using an HNA (hydrofluoric acid + nitric acid + acetic acid) based solution. X-ray diffraction (XRD) characterization indicated the high crystalline quality of the AlN film. An atomic force microscope (AFM) has been used to determine the Cr electrode surface roughness. The morphology of the fabricated devices has been studied by scanning electron microscope (SEM). The cantilevers have been piezoelectrically actuated and their out-of-plane vibration modes were detected by vibrometry.

Keywords: microcantilevers, aluminum nitride, piezoelectric

1. Introduction

Over the last decades, CMOS technology has become by far the predominant fabrication technology for integrated circuits (ICs). Nowadays, the power of CMOS technology is not only exploited for ICs but also for a variety of microsensors and MEMS benefiting from well-established fabrication

technologies and the availability of on-chip circuitry [1, 2]. The main advantage of the CMOS MEMS integration is related to mass production making microsystems more powerful and less expensive.

The aim of this work is to develop low-temperature manufacturing recipes which will facilitate the integration of MEMS devices such as piezoelectric microcantilevers with

CMOS technology. Low-temperature processing means not just compatibility with CMOS standard procedures; it also translates into higher throughput and, as a consequence, lower manufacturing costs. The use of AlN by reactive sputtering at room temperature is a critical step towards the integration of piezoelectric devices into CMOS technology. Although several studies have shown the integration of MEMS structures into CMOS circuitry [3, 4], the integration of piezoelectric MEMS is still a challenge.

A standard polycrystalline silicon (poly-Si)-based MEMS process typically employs deposition temperatures near 600°C and annealing temperature of above 900°C in order to achieve low-resistivity, low-tensile-stress structural films. These temperatures are too high to be compatible with conventional IC metallization and doping schemes, which convert heat generation in one of today's major yield killers [5]. On the other hand, in the search for an all-electrical scheme, a piezoelectric material is needed, and the usual synthesis temperatures of most commonly used piezoelectric materials (bismuth titanate: 300°C [6], quartz: 900°C, lithium niobate: 700°C [7], lithium tantalite around 1000°C [8]) are too high to allow their integration into CMOS technology [9].

AlN properties such as piezoelectricity, high acoustic velocity, biocompatibility and chemical stability at high temperatures make this material an attractive option for MEMS devices. The use of AlN instead of other piezoelectric material is particularly advantageous for the fabrication of post-CMOS compatible microcantilevers [10, 11]

On the other hand, MEMS are undergoing a huge development, achieving in 2013 sales of around 12 billion US dollars with applications in very diverse fields such as biological research and medical instruments, RF and optical communication, environmental monitoring and protection of energy sources [12].

The technological impact of the integration of MEMS within standard Si manufacture is becoming increasingly evident [13]. To mention one example, the effective identification and quantification of biomolecules is critical for the detection and diagnosis of several illnesses, including cancer [14]. In these studies, the cancerous cells are detected when they are absorbed at the surface of a microcantilever coated with a special receptor that reacts with the biomolecules. The deflection of the cantilever is proportional to the concentration of the absorbed biomolecules [15, 16]. Besides its many advantages as a piezoelectric material, the material used in the present study, AlN, is also biocompatible, which makes it the perfect candidate for such kinds of applications. Among many others applications of these MEMS, the fabricated microstructures are of potential interest in the field of biodetection due to the biocompatibility of the AlN thin film. Many methods for growing AlN thin films have been discussed in the literature [17–19] such as chemical vapor deposition (CVD), physical vapor deposition (PVD), reactive evaporation or molecular beam epitaxy (MBE). In this work, the synthesis of the (0002)-oriented AlN thin films has been done in a reactive pulsed-dc magnetron sputtering at room temperature, which makes it compatible with post-CMOS technology.

The piezoelectric microcantilever fabrication process involves the use of ICP dry etching techniques, reactive sputtering techniques as well as wet etching processes. The structural characteristics of the cantilevers are described in detail. Finally, the piezoelectric properties of the device are studied by laser Doppler vibrometry (LDV) [20].

2. Experimental

Each cantilever beam in the present study consists of a thin film of AlN sandwiched between two metal (chromium) electrodes. Two different thicknesses of the Cr bottom electrode have been studied, namely 50 and 200 nm. This bottom electrode is covered with a thin AlN piezoelectric film synthesized in a reactive sputtering process at room temperature. The thickness of the AlN thin film has been varied from 300 to 600 nm. This AlN thickness range is enough to develop piezoelectric microcantilevers that can be successfully actuated [22, 23]. As the top electrode, a 300 nm thin Cr layer has been used. In order to determine the implementation of the proposed manufacturing process, an array of microcantilever dimensions ranging from 20 to 50 μm in width and 30–625 μm in length has been investigated. The microstructures have been fabricated on Si (100) *p*-doped substrates. As part of its novelty, the proposed fabrication process involves the use of the silicon substrate not only to support the microcantilevers, but also as a sacrificial layer. To facilitate understanding, the process flow, shown in figure 1, has been divided into four steps.

2.1. Step 1: Cr bottom electrode

The Cr bottom electrode formation includes the optical lithography step, metal deposition and subsequent lift-off. After an initial clean-up with acetone at 60°C for 5 min and an ultrasonic bath in isopropanol (IPA), the lithography exposure step is done (Karl Suss MJB3 model). In this first lithography step to pattern the Cr bottom electrode, a positive photoresist (microchemicals AZ5214E) is used. The photoresist is spun at 5000 rpm for 45 s and baked at 110°C for 60 s, obtaining a resist thickness of 1.4 μm . After resist exposure for 3.5 s (using a mercury lamp working at 350 W with a wavelength of 350–450 nm), it is developed using AZ400 for 40 s. These parameters are common for all other optical lithography steps shown in this work.

Poor adhesion to the Si substrate causes the Cr layer (bottom contact) to peel off during lift-off. Thus, after resist development, a BHF (hydrofluoric acid 10%) cleaning of the Si surface is done to improve the metal adhesion. Thereafter, the Cr thin film is deposited by thermal evaporation in a high-vacuum Joule-effect evaporator system (Balzers BAE 250).

Finally, a lift-off process is used to pattern the Cr bottom electrode. A warm (60°C) acetone bath is used to expand and dissolve the resist underneath the Cr layer. This creates cracks in the metal layer on top of the AZ5214E positive resist and starts the lift-off.

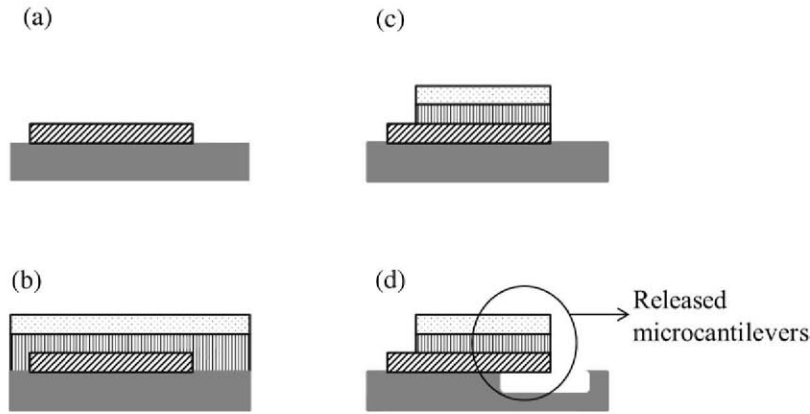


Figure 1. Schematic illustration of the microcantilevers fabrication process: Cr bottom electrode lithography, deposition and lift off (step 1), deposition of AlN and Cr top electrode (step 2), second lithography and ICP etch of the Cr top electrode and AlN (step 3) and etching of the Si substrate (step 4).

2.2. Step 2: AlN and Cr top electrode deposition

The thin AlN film is deposited in a home-built balanced magnetron-pulsed dc reactive sputtering deposition system at RT (room temperature). As mentioned before, this low thermal budget step is one of the key factors of our manufacturing process which allows for high throughput and makes it compatible with post-CMOS technology.

In order to determine the influence of the discharge power on the degree of *c*-axis orientation of the AlN thin films, it has been varied in the 500–700 W range. If not otherwise specified, the parameters used for the AlN synthesis on each experiment are as shown in table 1.

After deposition of the AlN layer, the Cr top electrode is deposited in the same high-vacuum Joule-effect evaporator system (Balzers BAE 250) used for the Cr bottom electrode.

2.3. Step 3: AlN and Cr top electrode patterning

In this step, the AlN thin film and the Cr top electrode are patterned by optical lithography and then etched. For the optical lithography, an AZ5214E positive photoresist is used following the same procedure as described in step 1. AlN is chemically stable and insoluble in most common etchants at room temperature. Furthermore, wet chemical etching of polycrystalline AlN produces isotropic etch profiles and slow etch rates, especially undesirable when high throughput is considered. Thus, in this case, ICP dry etching techniques are an attractive alternative. ICP technology has the potential to control the etch rate, the degree of etching anisotropy, material selectivity and hence the ability to find an etch stop layer. Both the Cr top electrode and the AlN layer are patterned by the same ICP equipment (PlasmaPro NGP 80, Oxford Instruments) and process, using a $\text{BCl}_3\text{-Cl}_2\text{-Ar}$ chemistry.

In order to optimize the etching, the Ar flow was varied between 1 and 10 sccm keeping the remaining parameters constant. If not otherwise specified, the parameters summarized in table 2 are used in all ICP etch steps. A dc bias voltage of 120 V was monitored.

After the AlN and Cr top electrode formation, the photoresist is stripped with N-Methyl-2-pyrrolidone at 60 °C for

Table 1. Parameters used during the deposition of the AlN thin layer.

Parameter	Value
Power (W)	500
Base pressure (mbar)	$<5 \times 10^{-8}$
Gas composition Ar/N ₂ (sccm)	3/9
Process pressure (mTorr)	3
Substrate temperature (°C)	25
Target substrate distance (mm)	45
Target diameter (mm)	101.6
Target thickness (mm)	6.35
Deposition rate (nm/min)	46

Table 2. ICP dry etch process parameters.

Parameter	Value
RF power (W)	30
HDP0 power (W)	200
Base pressure (mbar)	5×10^{-5}
Gas composition Ar/Cl ₂ /BCl ₃ (sccm)	3/25/15
Process pressure (mTorr)	10
Substrate temperature (°C)	25

5 min. In cases when the photoresist is hardened during the ICP step, an oxygen plasma (Plasma Etch Unitronics) is necessary. For this O₂ plasma, the processing pressure was 270 mTorr, whereas the oxygen flow and the discharge power were fixed at 15 sccm and 50 W, respectively. The plasma exposure time to ensure the removal of the entire photoresist layer was 5 min.

2.4. Step 4: cantilever release

Finally, a smooth and isotropic wet etching step of the silicon underneath the structure is performed in order to release the Cr–AlN–Cr microstructure, thus forming free cantilevers.

For this wet etching step of the Si surface acting as a sacrificial layer, two different chemistries have been studied: (a) HNA, a mixture of hydrofluoric⁴, nitric⁵ and acetic⁶ acids,

⁴ HF 36%. VLSI Selectipur BASF.

⁵ HNO₃ 65%. VLSI Selectipur BASF.

⁶ HAc 99.8%. Sygma Aldrich.

HF:HNO₃:CH₃COOH, in a 5:10:16 proportion, and (b) potassium hydroxide KOH. Both chemicals have been studied at different concentrations. HNA-related experiments were performed at room temperature. Due to its exothermic nature, the reaction temperature in the KOH etching steps varied for each chemical concentration.

ICP etch rates have been determined *in situ* by an end-point detector using optical reflectivity from a 670 nm laser (Global Laser Technology Solutions, Intellevation LEP 400), normal to the nitride surface.

To verify that the microcantilevers have been completely released from the Si surface and determine structural and morphological properties, a scanning electron microscope (SEM) has been used (Oxford FEI Inspect FSO), applying a voltage of 5 kV.

The degree of *c*-axis orientation of the polycrystalline AlN layer has been determined by high resolution x-ray diffraction (HR-XRD) using the Cu K α radiation of 1.54 Å. This assessment is critical to the piezoelectric behavior of the fabricated cantilevers. $\theta/2\theta$ scans and rocking curve measurements have been done using a Philips X-Pert Pro MRD diffractometer. The $\theta/2\theta$ scans from 20–80° have been done using a step size of 0.02° and a step time of 0.5 s. In the rocking curve analysis, the FWHM of the 0002 AlN peak has been measured from 3 to 25°, with a step size of 0.009° and a step time of 0.7 s.

The layer thickness has been measured on each sample using a KLA-Tencor Alpha Step IQ profilometer.

To study the influence of the substrate surface roughness on the AlN orientation, the roughness of the Cr bottom electrode has been measured with an atomic force microscope, AFM (Digital Instruments MultiMode Scanning Probe Microscope, model MMAFM-2) in tapping mode.

Finally, a laser Doppler vibrometer (MSV 400 Polytec) has been used to characterize the performance of the manufactured piezoelectric microcantilevers under applied electric field. The performance of the cantilevers has been determined by applying a chirp signal (5 mV frequency domain amplitude) to the electrodes in a frequency range from 1 kHz to 1 MHz.

3. Results and discussion

3.1. Etching of active and sacrificial layers

3.1.1. Dry etching steps (ICP). Different ICP recipes have been studied with the aim of finding an equilibrium between a high AlN etch rate and an etch rate of the photoresist mask sufficiently low to prevent burning effects as well as a complete consumption of the resist masking layer.

It has been shown in the literature that the chemical breaking of the AlN III-nitrogen bond is dependent on the chlorine concentration (BCl₃-Cl₂) [24, 25]. The Ar content dominates the physical contribution of the ICP etch process, including the photoresist mask etch. As a consequence, the parameter varied in this study was the Ar flow. Emphasis is focused on verifying that the AlN etch rate is enhanced while the photoresist is not completely etched or burned.

Thus, we have varied the Ar flow between 1 and 10 sccm while keeping the chlorine flow constant. The results can

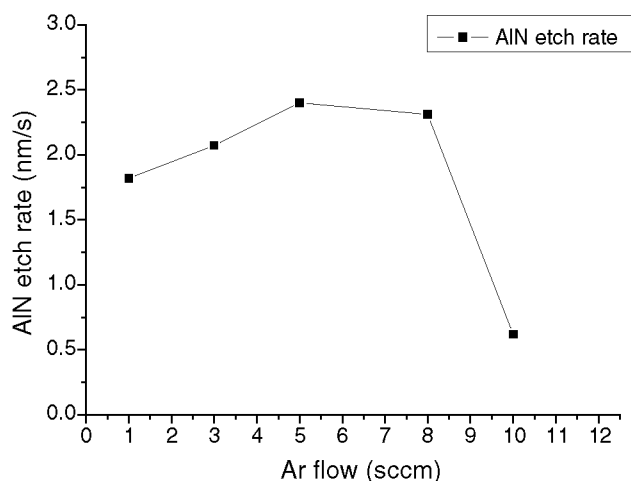


Figure 2. Ar flow influence on the AlN etch rate.

be visualized in figure 2 which shows the etch rates measured by the etch-point detector [26] observed on the nitride film as a function of the Ar flow. It is seen that for Ar flows below 8 sccm, reducing this parameter does not imply a significant effect on the AlN etch rate, which confirms that the etch mechanism in that range is predominantly chemical.

A noticeable decrease in the AlN etch rate was found for an Ar flow of 10 sccm which, since the total process pressure is not varied, can be explained by the corresponding proportional decrease of the chlorine contribution.

For an ICP dry etch step using the parameters shown in table 2 (Ar flow 3 sccm), the AlN, Cr and AZ4214E resist etch rates are 2.1, 4.3 and 3.9 nm s⁻¹, respectively. This recipe can be used to pattern a structure of 300 nm of Cr (top electrode) and a maximum of 600 nm of AlN before the photoresist mask is completely etched away. As shown in figure 2, for 1 sccm of Ar, the AlN rate is not much slower than for 3 sccm of Ar. However, the Cr etch rate at 1 sccm of Ar is reduced to the point of limiting the maximum thickness that can be etched before the photoresist mask is consumed, and hence also the Cr top electrode thickness.

In addition, by reducing the Ar flow, burning of the photoresist mask is avoided. Using gas flows higher than 3 sccm of Ar, the photoresist mask starts to burn and it can only be removed in an oxygen plasma. Using lower Ar flows, the photoresist is easily removed in a N-methyl-2-pyrrolidone bath.

After several tests, the etch recipe that etches the whole microcantilever structure before the photoresist mask is completely etched or burned, is that containing an Ar flow of 3 sccm. Cl₂/BCl₃ were kept constant at values shown in table 2. This is the recipe used for all dry ICP etching steps in this work.

3.1.2. Si wet etch. In order to release the microcantilevers using the manufacturing recipe proposed here, the silicon surface sacrificial layer is wet etched from the top, instead of from the back as in conventional back micromachining processes, which would render the process incompatible with CMOS technology [10, 27].

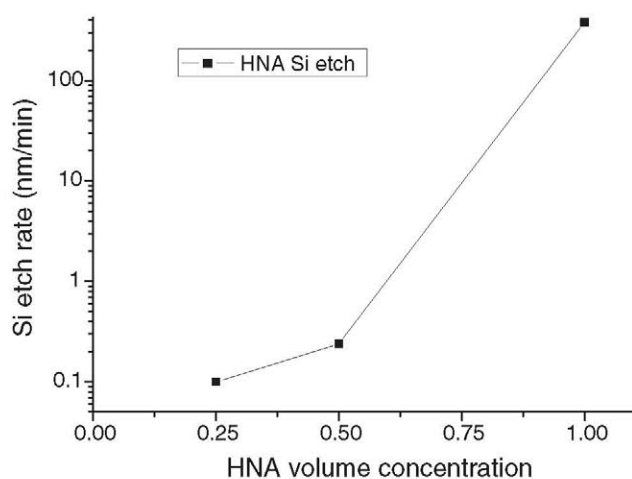


Figure 3. HNA volume concentration influence on the Si wet etch rates.

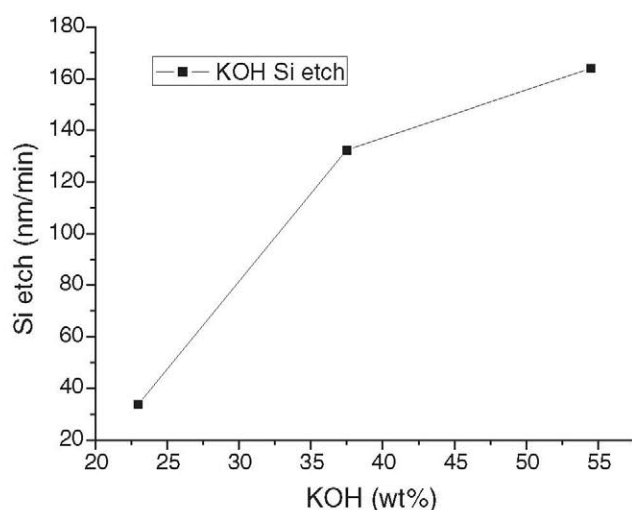


Figure 4. Si wet etch evolution with KOH concentration.

For this Si etching step, we have investigated two different wet chemical recipes: the mixture of hydrofluoric, nitric and acetic acids (5:10:16), HNA, and a potassium hydroxide (KOH)-based solution. These are among the most common wet etch recipes for Si found in the literature. Moreover, the Cr layer shows a very high selectivity to both etchants.

As will be explained in section 4, Si wet etch steps would be carried out in wafer areas where no circuits had been processed. In this way, sensor performance previously developed by CMOS technology can be composed of materials attackable by the Si etch recipes without suffering any damage.

Due to the isotropic nature of the HNA etch, the width underneath the cantilevers is etched in the vertical and lateral directions simultaneously. Hence, cantilevers of the same width are all released uniformly.

The KOH is an anisotropic etch in which the etch rates are dependent on the direction. The anisotropy degree is extremely dependent on many factors such as temperature, etchant concentration or doping concentration of the Si, and the etching performance is hard to predict [28–30].

Different concentrations of HNA and KOH have been studied to compare the Si etch rate and the isotropy degree in order to find the faster and more effective recipe to release the microcantilevers.

The study has been based on the maximum possible concentration for both recipes. According to this principle, for HNA the volume concentration is represented with 1 being the maximum concentration (i.e. not diluted with water), 0.5 for a HNA:H₂O solution in the relation 1:1, and 0.25 for a HNA:H₂O 1:3 solution. Figure 3 shows the logarithmic evolution of the Si etch rate with these concentration values for the HNA case.

For the KOH case, the graph in figure 4 represents the Si etch rate dependence with the KOH weight fraction percent. The rates represented correspond to the (100) plane (vertical direction). The rates on the (110) and (111) directions that allow the cantilevers release are lower. The maximum weight fraction (the maximum quantity of KOH that can be solved in water, also referred to as solubility [31]) of the KOH is 54.5%. For comparison with the maximum weight fraction, the Si etch rates for KOH solutions of 37.5 and 23% weight fractions have been also studied.

All HNA-based experiments were done at room temperature. The KOH recipes have been studied at their exothermic reaction temperatures, depending on molar concentration (64, 58 and 45 °C for 54.5, 37.5 and 23% weight fractions) [32, 33].

Both HNA- and KOH-based solutions showed a strong influence of their respective concentration on the Si etch rate, achieving the fastest rate for the highest concentration. For KOH the evolution was softer and linearly approached as seen in figure 4. Nevertheless, for the HNA mixture, the Si etch rate differences became especially noticeable for concentrated solutions.

For the highest concentration in both chemicals, the rate of the HNA-based mixture (382 nm min⁻¹) is twice that of the KOH (164 nm min⁻¹) solution. In addition, KOH etch rate values of this study are related to the (100) direction and the rates for the lateral directions are lower. Consequently, HNA releases the microcantilevers faster than KOH.

Moreover, unlike the KOH etch, the HNA etch rate is easily controlled and very reproducible. Using this recipe, the microcantilevers are released uniformly and the Si surface remains clean and smooth. This result cannot be achieved with the KOH etch, which is more irregular in etch rates and leaves the Si surface rougher.

Consequently, all the microcantilevers processed for further characterization have been etched in an HNA non-diluted solution.

This step makes possible the high throughput required for the process. The wet etching technique permits the simultaneous release of cantilevers with batches of the same wafer width. At the same time, it is a clean, fast process and easy to implement in the industry for a wide range of microcantilever dimensions. Figure 5 left image shows different dimensions of cantilever beams fabricated and released in the same process step.

During the microcantilever releasing step, the whole Si surface is wet etched. As shown in figure 5 (right image), the

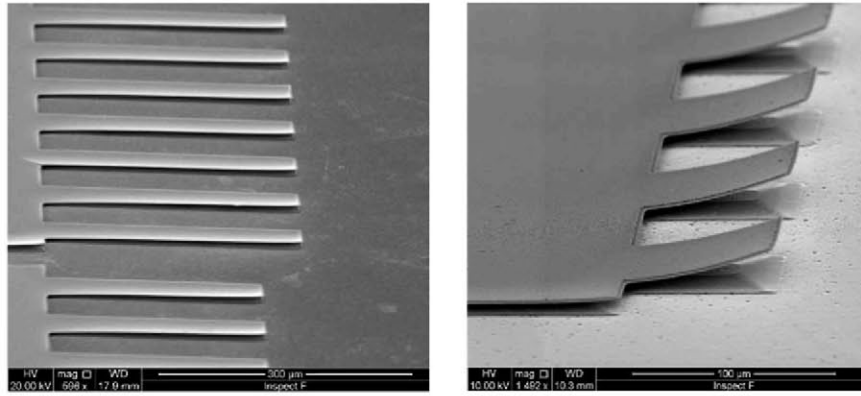


Figure 5. (a) SEM micrographs of microcantilevers arrays of different lengths; (300 and 375 μm) and 50 μm width (left). (b) Right image shows an array of cantilevers after release.

height gradient under the microcantilevers caused by the wet etching of the Si substrate surface is shown in detail. The last area etched before the cantilever is completely detached from the Si surface is the space under the middle of the microcantilever, causing a height gradient. The height gradient of the Si substrate surface under the released cantilever is of a few tens of microns. Since the Si etch is isotropic, the exact height of this gradient corresponds to the released microcantilever width. Its rounded shape can be clearly differentiated right under the released microcantilevers. The image shows a free space under the cantilevers and a slight tensile stress. This effect is not common to all the fabricated microcantilevers, but the image has been selected for illustrative purposes since the bending of the cantilever facilitates the visualization of the Si etch profile underneath the microcantilever.

3.2. Structural characterization

3.2.1. Scanning electron microscopy (SEM). This technique has been used to check the morphological characteristics of the microcantilevers.

Figure 6 shows the fabricated Cr/AlN/Cr microcantilevers and a free space under them obtained after the Si surface wet etch step. The precise thickness of the beam layers is also determined by SEM. The typical columnar texture of the *c*-axis oriented AlN film is easily distinguished in the image. Our SEM study of several samples supports the reproducibility of the process, showing cantilevers etched uniformly, a clean Si surface and a reproducible and well-defined device pattern.

3.2.2. X-ray diffraction measurements. For these microcantilevers to be used as piezoelectric MEMS, it is critical to control the crystallographic orientation of the AlN thin film. First, a scan $\theta/2\theta$ x-ray diffraction analysis was done to verify that the sample orientation is in the *c*-axis direction. The second step is a rocking curve analysis. In a rocking curve measurement, the sample is rotated (rocked) through an angular range around the (0002) peak orientation obtained in the scan $\theta/2\theta$, bringing the plane in and out of the Bragg condition. The width of the measured peak, normally measured in terms of the full width at half maximum (FWHM) value, contains information

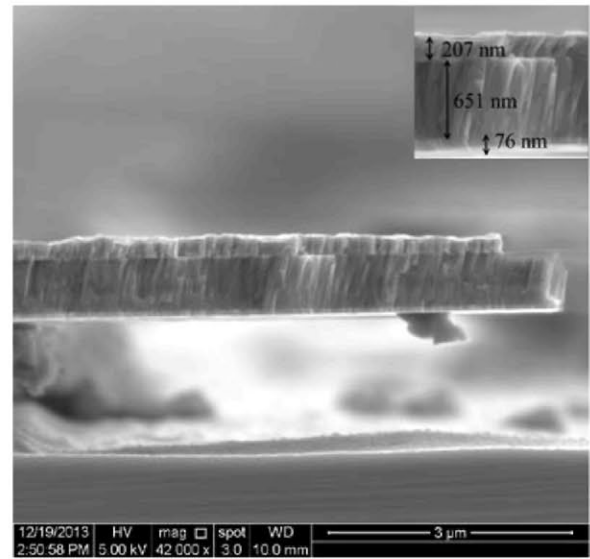


Figure 6. Cross sectional SEM view of the cantilever showing the Cr-AlN-Cr sandwich structure i.

regarding the amount by which the measured plane is off the surface normal, sometimes referred to as the ‘degree of orientation’ of the specimen. This value has an inverse relationship with the sample quality. Figure 7 shows a rocking curve measurement of a 700 nm AlN layer grown on 200 nm of Cr presenting a FWHM of 2.65° .

Some researchers have discussed the influence of deposition parameters on the orientation of the AlN films in an attempt to find a general guideline promoting a well *c*-axis oriented thin film [34, 35]. One of the most influenceable parameters is the target power, whose tendency is not completely clear since it is affected by the other parameters available in the process.

Since the film orientation also depends on its thickness, for proper comparison only films of 700 nm of AlN over 100 nm of Cr have been evaluated in terms of target power influence.

Figure 8 shows the rocking curve FWHM values of the (0002) peak of AlN thin films deposited at discharge powers varying from 400 to 700 W. It is seen that the AlN thin films grown at low discharge power (i.e. below 500 W in this work) do not exhibit a well-defined orientation in the *c*-axis. This

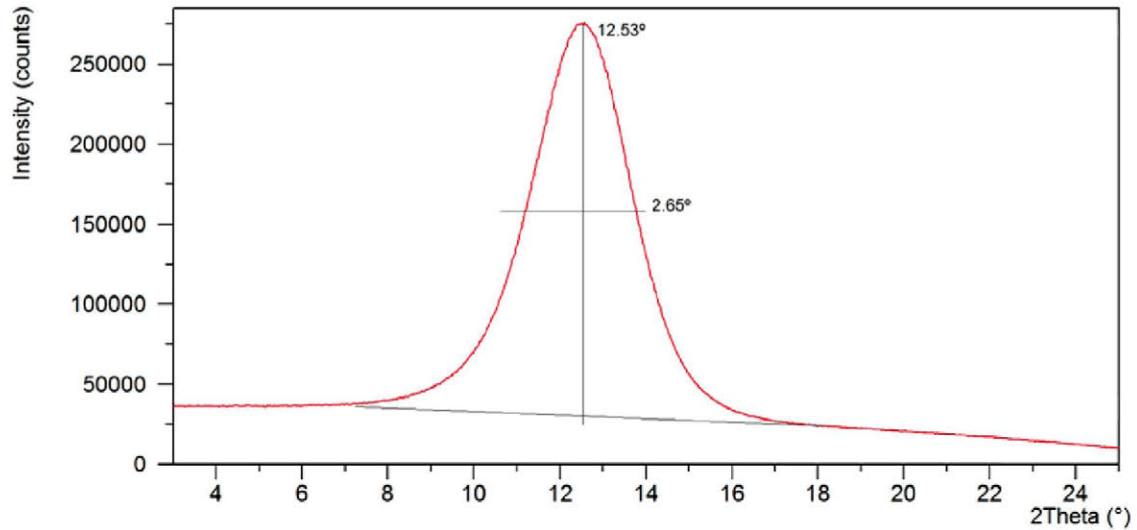


Figure 7. Rocking curve of *c*-axis oriented AlN thin films deposited at 500W on 200 nm of Cr.

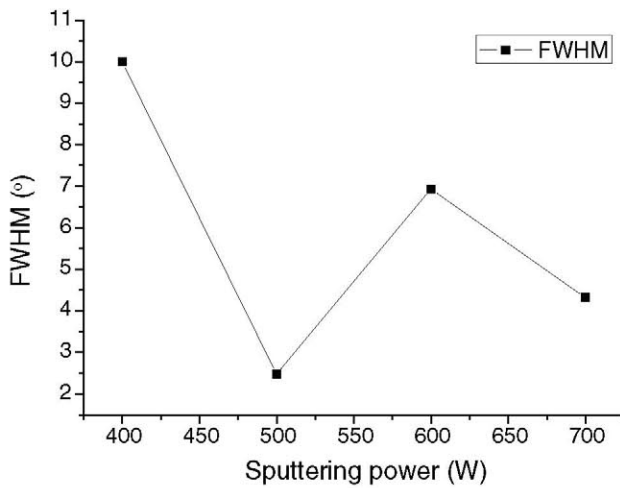


Figure 8. Rocking curve FWHM values of *c*-axes oriented AlN films synthesized over Cr using different target power values.

may be due to the fact that the atoms sputtered towards the substrate do not possess (as a collective) the required energy to form the well-oriented structure because the power is too low. In other words, the process is outside the desired energy window to promote crystal growth [36]. As is clearly shown in figure 8, the AlN thin film grows with a much better degree of *c*-axis orientation using discharge powers at 500 W.

3.2.3. Atomic force microscopy analysis of the chromium surface (bottom electrode). Several researchers have studied the influence of the substrate (in this case the Cr bottom electrode) on the quality of the AlN layer. These studies found in the literature reveal how a smooth substrate surface roughness favors the synthesis of highly *c*-axis oriented AlN thin films.

Three Cr samples from different metallization processes and thicknesses have been analyzed obtaining analogous

results. Areas of 2, 4 and 5 μm^2 have been scanned in at least three different positions in each Cr sample in order to make sure that the images taken in the AFM are representative of the film surface.

Figure 9 shows a 3D and height AFM micrograph (4 μm^2 area) of chromium, showing a root-mean-square (RMS) of 8.9 nm. With this substrate roughness value, the growth in the *c*-axis direction can be expected to be diminished. However, as shown previously in the x-ray section, a good AlN thin film orientation was achieved. Thus, we have seen that when using the optimized parameters shown in table 1 for the synthesis of AlN thin films, the use of a very smooth substrate to promote the growth in the (0002) direction is not strictly necessary.

3.3. Optical characterization

3.3.1. Vibrometry. A first approach for the characterization of the out-of-plane vibrating modes has been done. The actuation of the cantilevers is done by applying a chirp signal between the top and the bottom metal electrode. A chirp signal is a superposition of sinusoidal signals designed to keep constant the amplitude in the frequency domain and hence allow for a uniform excitation. In our case, the frequency of the chirp signal varied between 0 and 1 MHz. The vibrometer provides a laser spot which can scan a grid of points on the top cantilever surface to measure the out-of-plane component of either velocity or displacement of each point.

Figure 10 shows the measured frequency response of a 50 × 250 μm^2 cantilever. The sandwich structure of these cantilevers is made out of a 100 nm Cr bottom electrode/ 250 nm AlN/ 200 nm Cr top electrode. Three different modes of vibration were detected: the first bending mode, the first torsional mode and a second-order torsional mode. For each mode, an inset is included that shows the measured velocity distribution on the cantilever surface (red for positive values, green for negative values), which allows for a proper

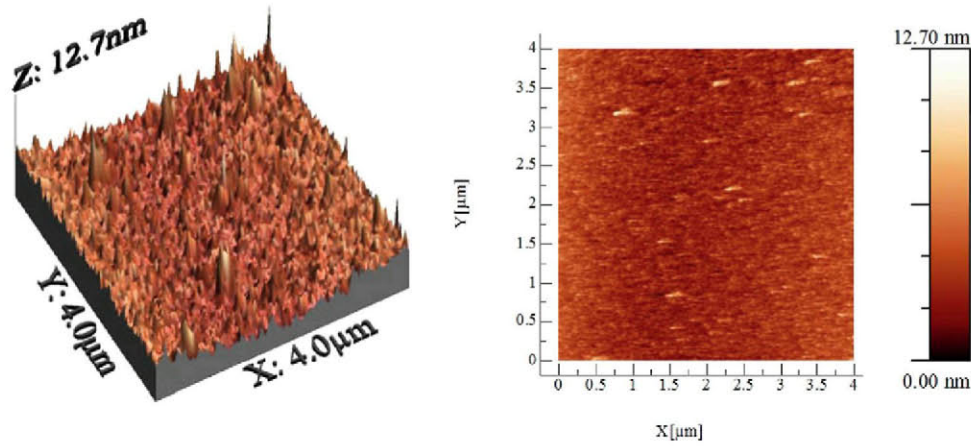


Figure 9. 3D and height AFM micrograph ($4\mu\text{m}$ area, data scale of 12.7nm) of a 300nm thin Cr surface.

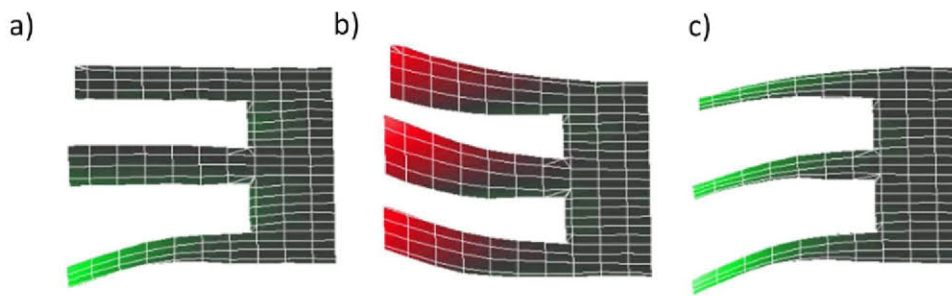


Figure 10. Laser Doppler vibrometry measurements for $50 \times 250\mu\text{m}^2$ cantilevers at around (a) 0.2MHz , (b) 0.5MHz and (c) 1MHz .

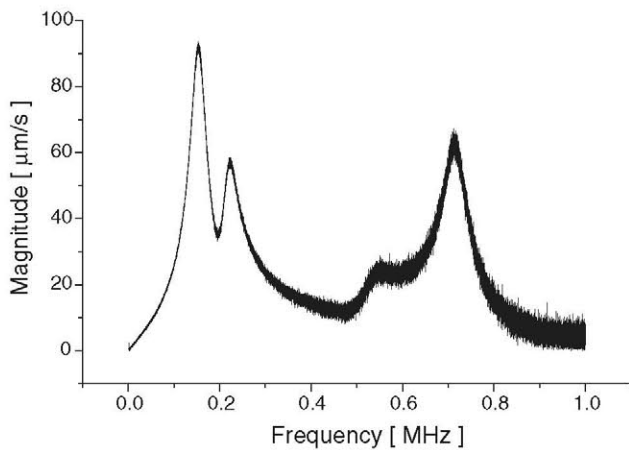


Figure 11. Velocity spectrum versus resonance frequency of the microcantilevers using laser vibrometry.

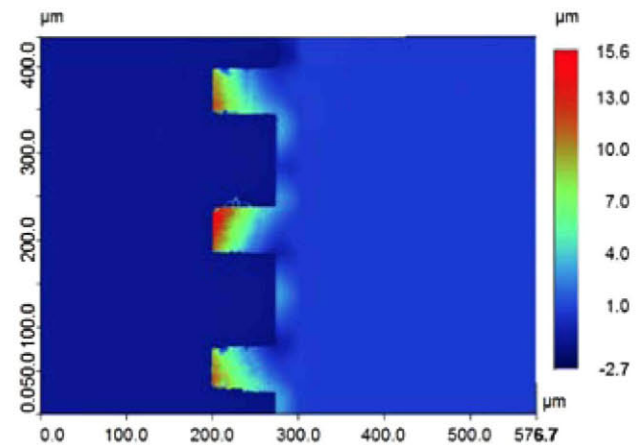


Figure 12. White light interferometry image of the $50 \times 250\mu\text{m}^2$ microcantilevers measured.

identification of the mode under study. Figure 11 is the velocity spectrum that causes the microcantilevers behavior represented in figure 10 using the laser vibrometry with an excitation source of 5mV . The purpose of these studies is to reveal the existence of a peak response due to the piezoelectricity of the AlN layer, and confirm that the device can move in different modes.

Figure 12 shows the average displacement of the resonances detected by white light interferometry for the microcantilevers measured in figures 10 and 11.

4. Proposed CMOS integration process

We have shown a successful manufacturing process of piezoelectric MEMS devices (microcantilevers) at RT. In this section, we propose the possibilities for integration of our process into state-of-the-art CMOS technology.

The fabrication method we propose could be implemented after the BEOL (Back End of Line) of a standard CMOS process, depositing a layer of amorphous silicon (a-Si) on top of the passivation layer. The microcantilevers

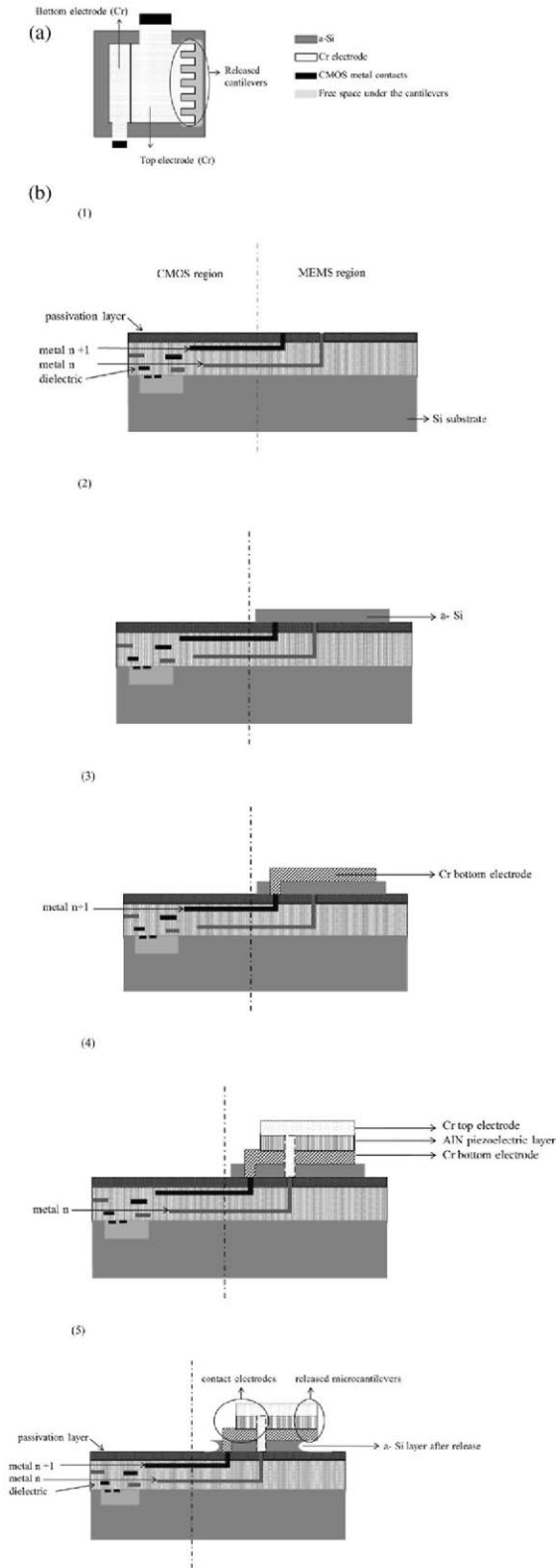


Figure 13. (a) Schematic top view of microcantilevers arrays processed post-CMOS. (b) CMOS standard processing leaving two metal vias exposed (step 1). PECVD deposition and patterning of amorphous silicon (a-Si) (step 2). Deposition and patterning of the Cr bottom electrode, contacting the vias at metal ' $n+1$ ' level (step 3). Subsequent synthesis of the piezoelectric AlN layer (at RT), the Cr top electrode and patterning of both layers by ICP (step 4). Si etch by HNA wet etch releasing the microcantilevers structure (step 5).

are released by attacking the a-Si underneath with HNA. Thus, a-Si is used as sacrificial layer. To make contact between CMOS and MEMS circuits, the CMOS vias are exposed through an opening in the passivation layer. The microcantilever electrodes are deposited on top of the CMOS vias, making contact between both technologies (see figure 13(a)). The proposed fabrication process can be used to fabricate piezoelectric AlN-based microcantilevers on top of the passivation layer (post-CMOS). The standard passivation layer material in a CMOS process, Si_3N_4 , shows a high resistance to the HNA etching recipe, which overcomes issues related to HNA attacking other layers of the CMOS circuit such as AlCu, W, SiO_2 , SiN_x , Ti, TiN and so on.

Figure 13(a) is a schematic illustration of the fabricated device viewed from the top. In this image, both top and bottom electrodes are connected with the BEOL metal levels (' n ' and ' $n+1$ ') in the CMOS circuit.

Figure 13(b) shows the flow steps of the integration process. The CMOS circuit is fabricated following state-of-the-art CMOS technology procedures. Using Cu single or dual damascene processes, BEOL metal level n and/or metal level $n+1$ vias can be fabricated reaching the wafer surface before passivation. BEOL metal level n and metal level $n+1$ correspond to two BEOL metal levels in the CMOS circuit. These can be left exposed through an opening in the passivation layer (commonly Si_3N_4) and if needed in the IMD layer, represented in figure 13 step 1. These metals named ' n ' and ' $n+1$ ' can be used to contact the microcantilever electrodes allowing the activation of the piezoelectric device. An important advantage of this integration process is that, by using dual damascene processes, these metal levels can come from any BEOL metal level of the CMOS circuit (not necessarily the last two).

Step 2 in figure 13 shows the PECVD deposition of an amorphous silicon layer over the entire wafer surface after patterning (by RIE), to determine the area where the microcantilevers will be processed [21]. Using standard low temperature PECVD-based a-Si deposition, the a-Si layer surface roughness will not interfere with the subsequent c -axis oriented AlN growth.

The microcantilever can be fabricated on top of the a-Si layer. The Cr bottom electrode can be deposited and patterned by lift-off, contacting with the vias of metal ' $n+1$ ' (figure 13 step 3). The next step is the growth at room temperature (by reactive sputtering) of the piezoelectric layer AlN and the deposition over it of the Cr top electrode. Both layers can be simultaneously patterned by ICP (figure 13 step 4). The Cr top electrode contacts can be patterned to make contact with the vias of the BEOL metal ' n ' level. The last step is the release of the microstructures by wet etching the a-Si underneath using an HNA solution (figure 13 step 5). Both Si_3N_4 and Cr show a high resistance to this HNA solution, and consequently the Si_3N_4 passivation layer protects the CMOS circuit from the etchant. At the same time, the Cr pads and electrodes will remain unaffected by the HNA releasing step.

5. Conclusions

A successful fabrication process of suspended piezoelectric AlN microcantilevers is presented. The compatibility of the process accomplished at room temperature with post-CMOS processes has been demonstrated.

The microcantilevers are fabricated using optical lithography, thermal evaporation, sputtering techniques and a combination of wet and dry etch processes. The process parameters and steps have been selected considering post-CMOS compatibility and high throughput, searching in each step for the faster recipe and the best results. In this respect, the choice of device materials is a key factor and has been described in detail.

Although the Cr substrate surface measured by AFM showed a rough profile, good *c*-axis orientation of the AlN over it could be achieved, as shown by x-ray diffraction analysis. SEM reveals a high reproducibility of the process, in addition to well-defined and completely released microcantilevers from the Si surface. Vibrometry measurements show that the cantilevers can be actuated electrically and consequently prove their viability as sensing and actuation devices.

Due to the biocompatibility of the materials used in this process, there are many potential applications of these AlN microcantilevers for biodetection purposes. Apart from many other applications, the compatibility with post-CMOS processes as well as the high throughput of the MEMS fabrication process presented here makes it an attractive alternative method towards faster and more reliable massive bio-related data analysis systems.

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