Multiphase Current-Controlled Buck Converter With Energy Recycling Output Impedance Correction Circuit (OICC)

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***Abstract*—This study is related to the improvement of the output impedance of a multiphase buck converter with peak current mode control (PCMC) by means of introducing an additional power path, which virtually increases the output capacitance during transients. Various solutions that can be employed to improve the dynamic behavior of the converter system exist, but nearly all solutions are developed for a single-phase buck converter with voltage mode control, while in the voltage regulation module applications, due to the high currents and dynamic specifications, the system is usually implemented as a multiphase buck converter with current mode control to ensure current sharing. The proposed circuit, output impedance correction circuit (OICC), is used to inject or extract a current $n - 1$ times larger than the output capacitor current, thus virtually increasing n times the value of the output capacitance during the transients. Furthermore, the OICC concept is extended to a multiphase buck converter system and the proposed solution is compared with the system that has n times bigger output capacitor in terms of dynamic behavior and static and dynamic efficiency. The OICC is implemented as a synchronous buck converter with PCMC, thus reducing its penalty on the system efficiency.**

***Index Terms*—DC-DC converter control, multiphase DC-DC converters, output impedance correction circuit (OICC).**

I. Introduction

In voltage regulation module (VRM) applications, it is well known that the main driver in designing the output filter stage is the output impedance of the system due to the strict specifications imposed by the load. Therefore, the ongoing research trend is directed to improve the dynamic response of the VRM while reducing the size of the output capacitor by means of either improving the controller [1]–[5] or by introducing an additional energy path (AEP) to compensate the charge perturbation in the output capacitor [6]–[26]. The output capacitor reduction leads to a smaller cost and longer lifetime of the system since the big bulk capacitors, usually implemented with OSCON capacitors, may not be needed to achieve the desired dynamic behavior. An additional advantage is that, by reducing the output capacitance, dynamic voltage scaling can be performed faster and with smaller stress on the power stage, since the needed amount of charge to change the output voltage is smaller.

The dynamic behavior of the system with a linear control (voltage mode control, VMC, peak current mode control, PCMC, etc.) is limited by the converter switching frequency and filter size. The reduction of the output capacitor can be achieved by increasing the switching frequency of the converter, thus increasing the bandwidth of the system, and/or by applying advanced nonlinear controls [1]–[5]. Applying nonlinear control, the system variables get saturated in order to reach the new steady state in a minimum time; thus, the output filter, more specifically the output inductor current slew-rate, determines the output voltage response. Therefore, by reducing the output inductor value, the inductor current reaches faster the new steady state, so a smaller amount of charge is taken from the output capacitor during the transient. The drawback of this approach is that the system efficiency is penalized due to increased switching losses and RMS currents. In order to achieve both the output capacitor reduction and high system efficiency, while satisfying strict dynamic specifications, a multiphase converter system is adopted as a standard for VRM applications [27]. In order to ensure the current sharing among the phases, the multiphase converter is usually implemented with current mode control (CMC).

The second possibility to reduce the output capacitor of the converter is to introduce an AEP to compensate the charge unbalance of the output capacitor [6]–[26], consequently reducing the transient time and output voltage deviation. Doing so, during the steady-state operation, the system has high efficiency because the main low-bandwidth converter is designed to operate at moderate switching frequency, to meet the static requirements, whereas the dynamic behavior during the transients is determined by the high-bandwidth auxiliary energy path. The auxiliary energy path can be implemented as a resistive path [16], [17], as a linear regulator (LR) [7]–[11], [24], [25], or as a switching converter [12]–[15], [18]–[23], [28]. The first two implementations provide faster response, at the expense of increasing losses during the transient. On the other hand, the switching converter implementation presents lower bandwidth, limited by the auxiliary converter switching frequency, though it produces smaller losses compared to the two previous implementations. Depending on the application, the implementation, and the control strategy of the system, there is a variety of proposed solution in the state of the art (SoA), having different features where one Solution offers some advantages over the

others, but also some disadvantages. In general, an ideal AEP system should have the following features:

1) *The impact on the system losses should be minimal:* During its operation, the AEP generates additional losses; thus, ideally, the AEP should operate for a short period of time, only when the transient is occurring as employed in [9], [11]–[26]; the other option is to have the AEP constantly on, as used in [7], [8], and [10], but due to the inductor current ripple compensation at the output, unnecessary losses are generated.
2) *The AEP should be activated nearly instantaneously to prevent bigger output voltage deviation:* To achieve near instantaneous activation, the converter system can be informed by the load prior to the load step [14]–[16] or the system can observe the output capacitor current, which is the first system-state variable that reacts on the load current perturbation [13], [20], [24]–[26]. In this manner, the AEP is turned on with near zero output voltage error, providing smaller output voltage deviation.
3) *The AEP should be deactivated once the new steady state is reached to avoid additional settling transients:* Most of the SoA solutions estimate duration of the transient [17]–[20], [22], [23], which may cause additional transient if the estimation is not performed correctly (e.g., if the main converter inductor current has higher or lower value than needed, the slow regulator of the main converter needs to compensate the difference after the AEP is deactivated). Other SoA solutions are observing state variables, ensuring that the system reaches the new steady state [9], [11]–[13], [21], [24]–[26] or they are informed by the load [14]–[16].
4) *During the transient, at least one subsystem, either the main converter or the AEP, should be in closed loop:* Implementing a closed-loop system, preferably the AEP subsystem, due its higher bandwidth, increases the robustness under system tolerances and circuit parasitic [7]–[13], [24]–[26]. In addition, the AEP can operate with any type of load. The solutions that operate in open loop [14]–[23] usually perform minimal time charge balance control, thus reducing the transient length and minimizing the impact on the losses; however, they are very sensitive to tolerances and parasitics.
5) *The AEP should inject a current at the output in a controlled manner,* thus reducing the risk of high and potentially damaging currents and increasing robustness on the input voltage deviation as implemented in solutions [12], [13], [18]–[20], [24]–[26]. This issue is mainly related to the systems where AEP is implemented as auxiliary converter. The auxiliary converter is designed for small power and, as such, the MOSFETs are rated for small power/currents. If the current is not controlled, due to the some unpredicted spike in input voltage caused by some other part of the system (e.g., different converter), it may lead to a current spike in auxiliary current which will cause the perturbation of the output voltage and even failure of the switching components of the auxiliary converter. In the case when the current is controlled, using peak CMC or hysteretic window CMC, the auxiliary converter has inherent feed-forwarding of the input voltage in current control and the current is defined and limited. Furthermore, if the solution employs charge balance control, the system may perform poorly if the input voltage has different value than the nominal, causing that AEP injects/extracts more/less charge than needed.
6) *Scalability of the system to multiphase converters:* As commented previously, in VRM applications, due to the high load currents, the main converters are implemented as multiphase to redistribute losses among the modules, lowering temperature stress of the components. To ensure the current sharing, usually a CMC is employed. The SoA solutions that are implemented with VMC [10]–[21] are limited to a single-stage implementation, while solutions [22]–[26] can be easily extended to multiphase converter systems.

The output impedance correction circuit (OICC) concept, employed in this study, has been presented in [24] and analyzed in detail in [25]. The proposed solution has all the features commented earlier: the OICC is activated only during the transients; it is activated with output capacitor current and deactivated by observing both the output voltage error and output capacitor current; during the transients, both the main converter and the OICC operate in closed loop; the OICC operates as a controlled current source (CCS), having high immunity on input voltage perturbation and inherent overcurrent protection; the main stage is implemented with CMC, allowing easy extension to a multiphase solution [26].

The OICC operates during the transients as a current-controlled source, so that the auxiliary current, injected/extracted through the AEP, is controlled to have $n - 1$ times higher value than the output capacitor current with appropriate directions. Doing so, the OICC creates an equivalent n times bigger virtual capacitor at the output, thus reducing the output impedance. In order to measure the output capacitor current, a noninvasive current estimator from [28] is used.

With respect to [25], this study provides detailed analysis of the multiphase solution with demonstration of the robustness of the system under repetitive load steps during the transient routine, as well as the robustness under output capacitor variation due to the tolerances and aging effect. In addition, the proposed solution is compared with a reference design which has n times bigger capacitor in terms of dynamic performance and the impact on the dynamic efficiency of the system has been measured. Furthermore, two additional advantages are obtained from the reduction of the output capacitance produced by the OICC concept: a footprint reduction and an increase of the reliability of the system, since only ceramic capacitor may be employed instead of big bulk capacitors, which are usually implemented with OSCON capacitors.

The OICC has been implemented as a synchronous buck converter with PCMC, thus improving the efficiency of the system compared to the solutions with LR [7]–[11], [24], [25]. The auxiliary current peak-to-average (Pk_Avg) offset compensation block has been employed in the OICC subsystem to ensure that the average auxiliary current is equal to the auxiliary current

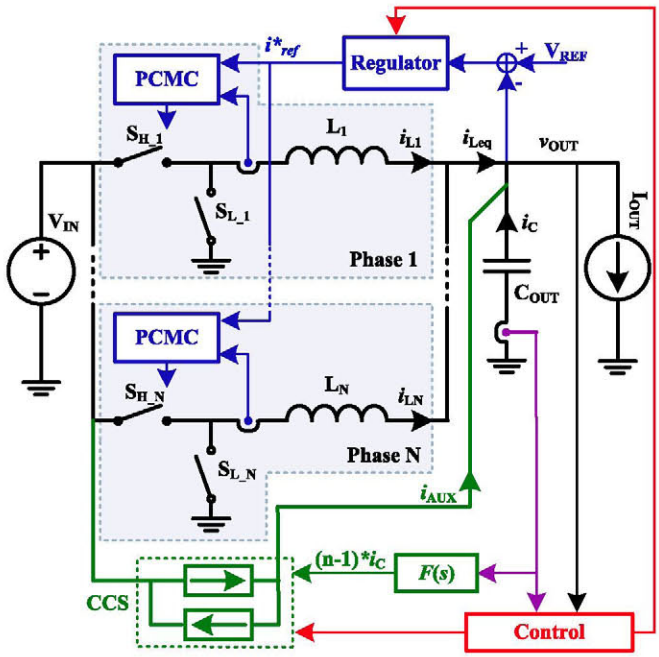

Fig. 1. Multiphase buck converter with the OICC—buck converter (black), the current measurement, driving signal generation, and the regulator (blue), noninvasive current estimator (purple), the OICC (green), and system control (red).

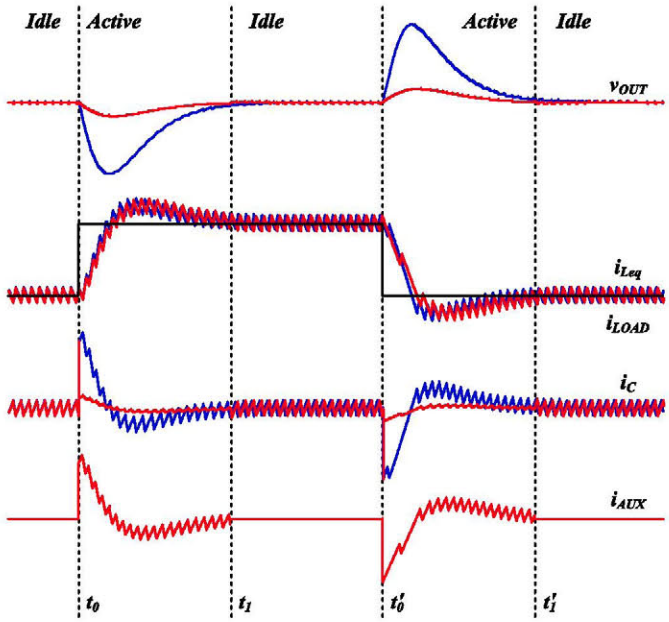

Fig. 2. Ideal system waveforms—basic operation: load step transitions with (red) and without (blue) the OICC.

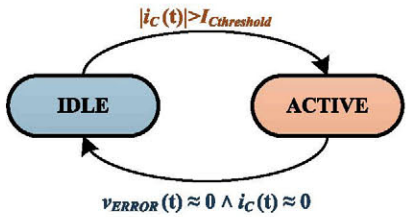

Fig. 3. State machine of the control system.

reference. This way, the OICC subsystem behaves as an equivalent capacitor (average current equal to zero).

II. OICC—Ideal Operation

A multiphase buck converter with PCMC and with the OICC is shown in Fig. 1. As explained in [24] and [25], the system utilizes the OICC in a manner that the OICC injects/extracts a current in the output node that is n–1 times bigger than the output capacitor current with their corresponding directions. This behavior of the OICC virtually increases the output capacitance n times during the transients, thus reducing the output impedance by the same factor. The system is composed of the multiphase buck converter (black) with a slow regulator (blue) which can be dynamically modified, the OICC (green—power stage, purple—current measurement) behaving like a CCS and the system control (red). The control block allows the OICC to inject/extract the current only in certain states of the transient routine. At the same time, in order to maintain the stability of the system, the control modifies the main converter regulator.

During the steady state, the OICC is inactive; all the energy is transferred through the multiphase buck converter and it is behaving like a voltage source, while the system control is sensing the output capacitor current in order to initialize the transient routine when a load step occurs. In this manner, by sensing the output capacitor current, the system reacts nearly instantaneously to any load perturbation, since the output capacitor current is the fastest variable in the system that detects this perturbation. In Fig. 2, the ideal transition routine behavior is presented. The waveforms of the system variables with OICC are presented as a red line and without the OICC are presented as a blue line. In the steady-state operation, the OICC is turned off and the small load variations are regulated by the low bandwidth regulator. When the load step occurs with an amplitude bigger than the critical, defined as the biggest amplitude which the main converter can handle without the OICC, the OICC is activated and the output impedance correction starts. The system controller, implemented as a state machine in Fig. 3, is triggered by the output capacitor current in the time instant t_0 and the system goes to the *Active* state. In this state, the OICC is providing $n-1$ times more current than the output capacitor, thus reducing the amount of the charge extracted/injected from/to the output capacitor. As a result, the voltage perturbation is smaller.

In the case that the critical amplitude is smaller than the output capacitor steady-state peak-to-peak ripple, the detection of the transient can be performed using the derivative of the capacitor current as presented in [29]. In the initial approach, in order to start the transient routine, the measured capacitor current is compared with the two references which are equal to the critical amplitude of the load step. When it is detected that the capacitor current is bigger than the positive reference or smaller than the negative reference, the load step is detected and the transient routine is launched. However, in the case when the critical amplitude is smaller than the output capacitor current

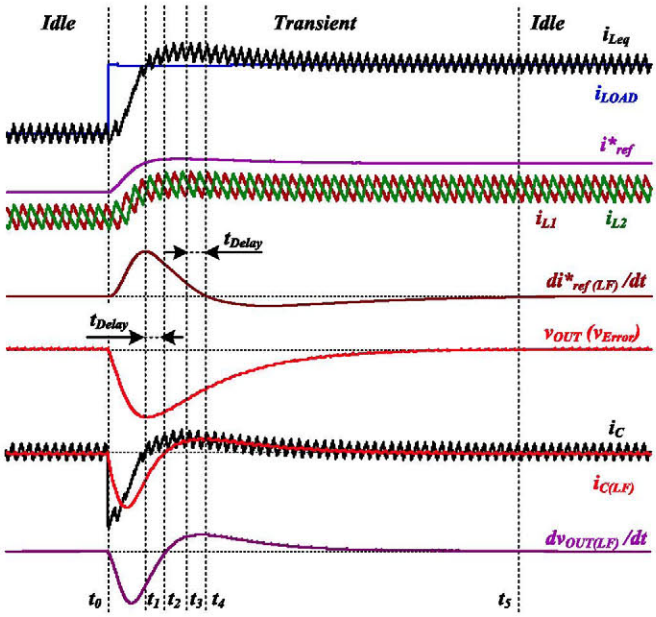

Fig. 4. Ideal system waveforms—EoT detection.

peak-to-peak ripple, the system controller would detect the transient each switching cycle, provoking undesired behavior of the system. In order to avoid this situation, the derivative of the capacitor current can be used to detect the load steps with smaller amplitude, as presented in [29]. In this case, the thresholds for triggering the transient routine should be designed to be bigger/smaller than the values obtained for positive/negative derivative of the steady-state capacitor current.

In order to finish the *Active* state, the system controller senses the output voltage error signal and the low frequency component of the capacitor current. Since the dynamic response is determined by the main converter bandwidth frequency, BW_{main}, these signals are filtered using the first order low-pass filter (LPF) with the pole at the main converter bandwidth frequency; thus, the analysis presented below is applicable up to the bandwidth frequency. The filter is used to remove the ripple from the state variables and to be able to observe just their averaged values. Observing these two signals, the system controller has information about the first derivative of the averaged values of the state variables of the system (the inductor currents i_{L1}, $i_{L2}, \ldots, i_{LN}$ and the output voltage v_{OUT}) and it can detect the end-of-transient (EoT) when the system enters in a new steady state. In order to illustrate the mechanism of the EoT detection, the waveforms of the state variables and its filtered derivatives are presented in Fig. 4 for a general multiphase system. By definition, neglecting the switching ripple, the steady state is defined by

$$\frac{d}{dt}v_{\text{OUT}} = 0 \quad \wedge \quad \frac{d}{dt}i_{Li} = 0, \quad i \in [1,\, N]\,. \tag{1}$$

The first condition can be detected by sensing the filtered capacitor current $i_{C(LF)}$ (red in Fig. 4), since it is, by definition, the first derivative of the output voltage (the capacitive effect is dominant at the considered frequencies). As it can be seen in Fig. 4, the filtered capacitor current $i_{\text{C(LF)}}$ has a delayed response with respect to the actual capacitor current i_C (black in Fig. 4) due to the filtering action. The actual capacitor current i_C crosses zero and it enters in a regeneration phase of the output voltage at time instant t_1, while the filtered value $i_{\text{C(LF)}}$ crosses zero at time instant t_2. Although the delay exists in the initial part of the transient, when the system reaches new steady state in t_5, both the actual capacitor current i_C and its filtered value $i_{\text{C(LF)}}$ have the same response; thus, zero value can be detected correctly. Furthermore, in Fig. 4, it can be seen that both the filtered value of the capacitor current $i_{\text{C(LF)}}$ and the derivative of the filtered value of the output voltage $dv_{\text{OUT(LF)}}/dt$ has the same behavior.

The second condition is indirectly monitored through the output voltage error v_{Error}, assuming that inductor currents are following the inductor current reference i^*_{ref} and that the currents are equal, as shown in Fig. 4. The condition can be modified as

$$\frac{d}{dt}i_{Li} = \frac{1}{N}\frac{d}{dt}i^*_{\text{ref}} = 0. \tag{2}$$

Since the inductor current reference i^*_{ref} is determined by the slow regulator transfer function and the output voltage error v_{Error}, it can be seen that, when the output voltage error is equal to zero apart from t_5, the inductor current reference i^*_{ref} (pink in Fig. 4) stops changing its value or, in other words, the derivative of the inductor current reference is equal to zero. Once again, the derivative of the filtered inductor current reference $di^*_{\text{ref(LF)}}/dt$ has a delay with respect to the actual reference response due to the filtering action: when the inductor current reference i^*_{ref} reaches its maximum value in t_3 and starts to decrease (negative derivative), the derivative of the filtered inductor current reference $di^*_{\text{ref(LF)}}/dt$ still has a positive value and it reaches zero in t_4. Finally, when both the output voltage error v_{Error} and the filtered capacitor current $i_{C_{(LF)}}$ are equal or close to zero in t_5, the system is in a new steady state.

This approach is implemented in the OICC system control, so that the detection of the steady-state condition event in t_1 (see Fig. 2) triggers the system controller, which returns the system back to the *Idle* state, and deactivates the OICC. If a low frequency low amplitude load current perturbation is present in the system during the transient, as it is usually the case, the detection of the EoT is still performed correctly due to the implementation of the EoT detection system: the low frequency component causes the regulator to modify the inductor current reference i^*_{ref} to compensate the disturbance, but, since the amplitude and the frequency of the perturbation are low and due to the low impedance and tight regulation at these frequencies, the output voltage error and the output capacitor current have near zero value, which will trigger the EoT detection. In this way, by observing these two variables, the detection is performed correctly which would not be the case if the inductor current reference derivative $di^*_{\text{ref(LF)}}/dt$ is used. Furthermore, the main system should be designed to compensate low frequency perturbations independently, without the help of the OICC; therefore, when the EoT is detected and the system returns to *Idle* state, the output voltage error and the output capacitor current have near zero value; thus, a new transient routine is not initiated.

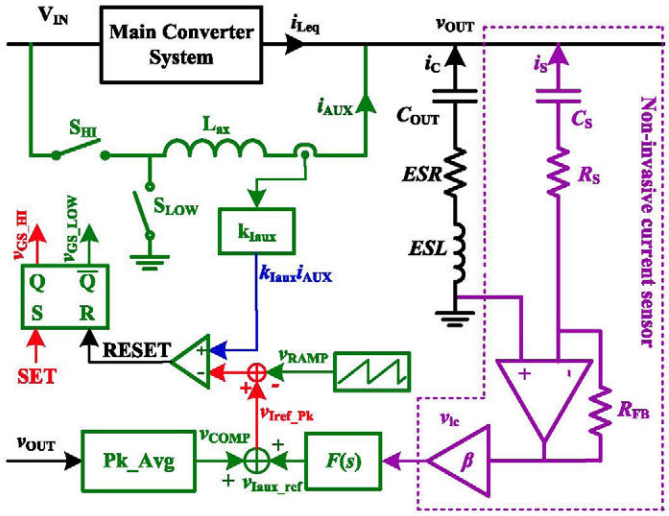

Fig. 5. Implementation of the OICC—synchronous buck converter with PCMC, auxiliary reference generator, and current ripple compensation (green), noninvasive current estimator (purple), and the main power stage (black).

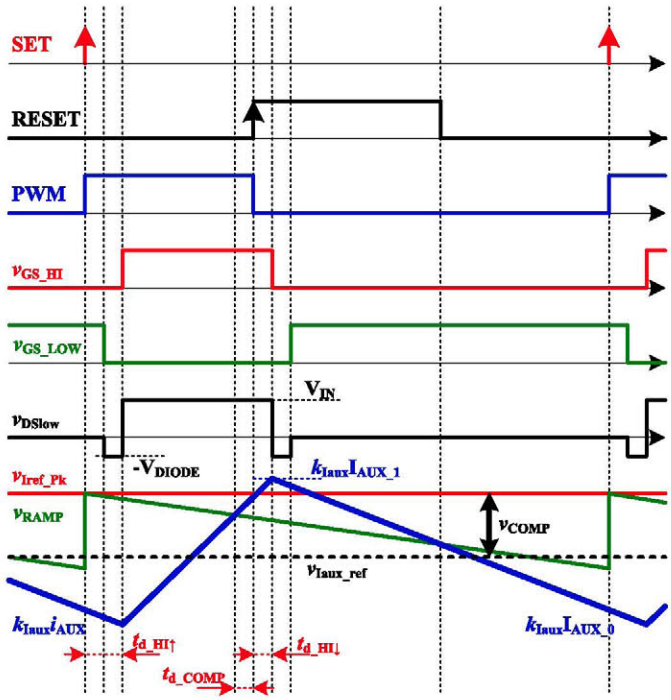

Fig. 6. PCMC waveforms with delays.

During the Idle state, the output capacitance is the actual physical capacitance, $C_{\rm OUT}$, but during the *Active* state, the equivalent capacitance in the ideal case is $n{\cdot}C_{\rm OUT}$. This affects the PCMC multiphase buck converter averaged model and, therefore, the stability requirements related to the regulator modification addressed in [25] need to be satisfied.

III. Synchronous PCMC Buck OICC Implementation

The OICC implementation is presented in Fig. 5. The OICC subsystem is composed of noninvasive current estimator (purple) designed by applying the impedance matching procedure presented in [28], the auxiliary current reference generator, the Pk_Avg offset compensation block, and a high-switching frequency synchronous buck converter with PCMC that operates as a CCS, shown in Fig. 1. The capacitor current estimator can be adjusted with the amplifier β and in the following analysis it is assumed that the total gain of the estimator is 1 V/A. When the OICC is active, the CCS is injecting an auxiliary current, $i_{\rm AUX}$, at the output node composed of the mean value given by the auxiliary current reference generator $v_{I\rm aux\_ref}$ and the ripple component generated by the auxiliary buck converter. Since the buck converter is PCMC controlled, assuming unity gain of the inductor current sensor, $k_{I\rm aux}$, an offset between the peak current reference $v_{I\rm ref\_Pk}$ and the mean value of the auxiliary current $i_{\rm AUX}$ exists due to: 1) the current ripple; 2) the compensation ramp; and 3) the turn on/off delays of the PCMC modulator. Therefore, the Pk_Avg offset compensation block is employed to compensate the difference by adding $v_{\rm COMP}$ to the auxiliary current reference voltage $v_{I\rm aux\_ref}$, thus ensuring that the mean value of the auxiliary current $i_{\rm AUX}$ equals to the auxiliary current reference voltage $v_{I\rm aux\_ref}$.

A. Pk_Av Compensation Block

Fig. 6 shows PCMC waveforms where it can be seen that, due to the type of the modulation, the mean value of the auxiliary current $i_{\rm AUX}$ is not equal to the peak current reference $v_{I\rm ref\_Pk}$. Depending on the slope of the compensation ramp m_C, turn-on and turn-off delay ($t_{d\_HI\uparrow}$ and $t_{d\_HI\downarrow}$) as well as on the comparator delay $t_{d\_\rm COMP}$, the difference between the peak current reference $v_{I\rm ref\_Pk}$ and the mean value of the auxiliary current $i_{\rm AUX}$, which needs to be compensated by the Pk_Avg compensation block $v_{\rm COMP}$, can be derived and it is defined by (3).

$$\begin{aligned} v_{\rm COMP} &= v_{I\rm ref\_Pk} - k_{I\rm aux} I_{\rm AUX} = \frac{k_{I\rm aux} v_{\rm OUT}}{2Lf_{\rm SW}} - \frac{k_{I\rm aux} v_{\rm OUT}^2}{2Lf_{\rm SW} v_{\rm IN}} \\ &+ \frac{m_C}{f_{\rm SW}} \frac{v_{\rm OUT}}{v_{\rm IN}} + m_C \left(t_{d\_\rm HI\uparrow} - t_{d\_\rm HI\downarrow} - t_{d\_\rm COMP}\right) \\ &- \frac{k_{I\rm aux} \left(v_{\rm IN} - v_{\rm OUT}\right) \left(t_{d\_\rm HI\downarrow} + t_{d\_\rm COMP}\right)}{L} \end{aligned} \tag{3}$$

Linearizing (3) in the operating point defined by $V_{\rm IN}$ and $V_{\rm OUT}$, a linear dependence of the compensating voltage $v_{\rm COMP}$ on input variables $v_{\rm IN}$ and $v_{\rm OUT}$ is obtained and given by

$$v_{\rm COMP} = V_{\rm COMP} + k_1 \left(v_{\rm OUT} - V_{\rm OUT}\right) + k_2 \left(v_{\rm IN} - V_{\rm IN}\right) \tag{4}$$

where $V_{\rm COMP}$ is the dc value of $v_{\rm COMP}$, obtained by calculating (3) in the operating point ($v_{\rm IN} = V_{\rm IN}$ and $v_{\rm OUT} = V_{\rm OUT}$), and k_1 and k_2 are the slopes of the plane defined by (4) and given by

$$\begin{aligned} k_1 &= \frac{k_{I\rm aux}}{2Lf_{\rm SW}} - \frac{k_{I\rm aux} V_{\rm OUT}}{Lf_{\rm SW} V_{\rm IN}} + \frac{m_C}{f_{\rm SW} V_{\rm IN}} \\ &+ \frac{k_{I\rm aux} \left(t_{d\_\rm HI\downarrow} + t_{d\_\rm COMP}\right)}{L} \\ k_2 &= \frac{k_{I\rm aux} V_{\rm OUT}^2}{2Lf_{\rm SW} V_{\rm IN}^2} - \frac{m_C}{f_{\rm SW}} \frac{V_{\rm OUT}}{V_{\rm IN}^2} - \frac{k_{I\rm aux} \left(t_{d\_\rm HI\downarrow} + t_{d\_\rm COMP}\right)}{L}. \end{aligned} \tag{5}$$

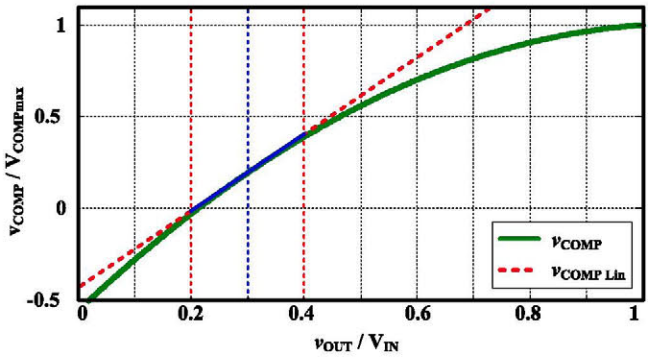

Fig. 7. Normalized compensation voltage: dependence on the normalized output voltage (green), linearization at the operating point (red-dotted), and part of the linearized function in the region of interest (blue).

Additionally, an assumption that the input voltage v_{IN} is constant leads to further simplification of (4) which leads to

$$v_{\mathrm{COMP}} = V_{\mathrm{COMP}} + k_1 \left(v_{\mathrm{OUT}} - V_{\mathrm{OUT}} \right). \tag{6}$$

The limitation of the bandwidth of v_{OUT} needs to be included in order to minimize the influence of the switching ripple of both the main system and the OICC. The Pk_Avg compensation block, defined by (6), has been implemented as a linear amplifier with LPF. The LPF bandwidth is the same as the closed-loop bandwidth of the main converter system, BW_{main}, in order to follow the dynamic of the output voltage. Implementing lower LPF bandwidth than BW_{main}, the Pk_Avg block attenuates better the ripple components, but it increases the delay caused by the filtering and the Pk_Avg block does not modifies v_{COMP} correctly at initial part of the transient, causing that the auxiliary current does not have desired value. If LPF bandwidth is higher than BW_{main}, the Pk_Avg block follows better the changes in the output voltage, but the ripple components are attenuated with smaller amplitude; thus, the compensation signal v_{COMP} might introduce them in the PCMC modulator block, affecting the stability.

Normalized compensation voltage v_{COMP} is shown in Fig. 7. For the presented case, the delays are selected to be realistic for high-frequency application with discrete implementation ($t_{HI\uparrow}$ is $8\%T_{\mathrm{SW}}$, $t_{HI\downarrow}$ is $10\%T_{\mathrm{SW}}$, and t_{COMP} is $7\%T_{\mathrm{SW}}$). It can be seen from Fig. 7 that a relatively good overlapping of the simplification (red) defined by (6) and the real dependence (green) defined by (3) can be obtained.

B. Stability Considerations

In order to ensure the small signal stability of the OICC subsystem, the high-frequency component of the auxiliary current, which exists in the capacitor current measurement (v_{ic}), needs to be filtered by the auxiliary current reference generator. The auxiliary current reference generator transfer function is given by

$$F(s) = \frac{v_{Iaux\_ref}(s)}{v_{ic}(s)} = \frac{n-1}{1 + \frac{s}{2\pi f_{\mathrm{OICC_c}}}} \tag{7}$$

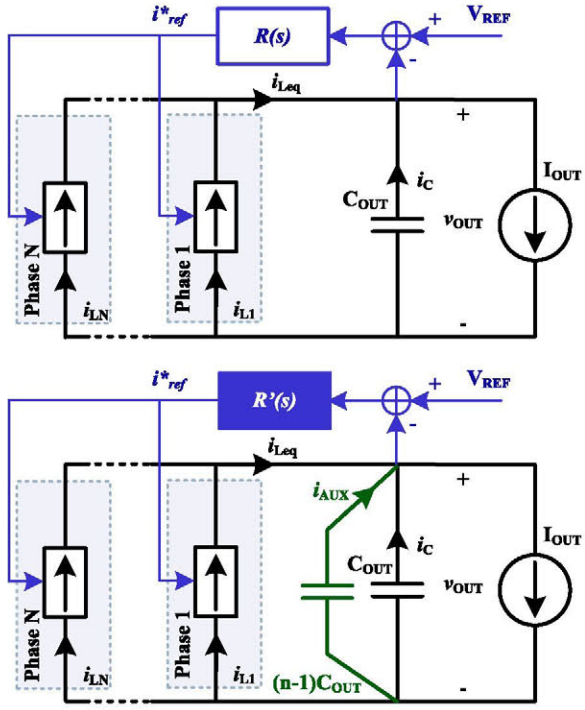

Fig. 8. Averaged models of the system during: (a) *Idle* state and (b) *Active* state.

where n is the output capacitor multiplication factor and $f_{\mathrm{OICC_c}}$ is the OICC corner frequency, which is a frequency up to which the OICC has constant gain $n-1$. By implementing (7), the OICC system corrects the output impedance up to $f_{\mathrm{OICC\_c}}$, which needs to be at least 2.5 times higher than the closed-loop bandwidth of the main converter system, BW_{main}, in order to minimize the influence of the pole in (7) on the main converter open-loop gain. In that case, the OICC is behaving as $n-1$ times bigger capacitor in the low frequency part of the spectrum; thus, the linearized model of the whole system can be simplified, as it is presented in Fig. 8.

Assuming that CCS is ideal, the impedance seen at the output node when the OICC is active is

$$Z_{Cout}^{\mathrm{EQ}} = \frac{Z_{C\mathrm{out}}}{1 + F(s)} \xrightarrow{f < f_{\mathrm{OICC_c}}} Z_{Cout}^{\mathrm{EQ}} = \frac{Z_{C\mathrm{out}}}{n} \tag{8}$$

where Z_{Cout} is the impedance of the output capacitor and the open-loop impedance of the system during the *Idle* state.

Since the main converter output voltage loop has to be stable in both *Ideal* and *Active* states, according to [25], the regulator needs to be modified in order to maintain the same closed-loop gain characteristics by applying

$$R'(s) = nR(s) \tag{9}$$

where $R(s)$ and $R'(s)$ are the regulator transfer functions for the system operating in *Idle* and *Active* states, respectively.

The closed-loop impedance of the system during the *Idle* state is given by

$$Z_{\mathrm{OUT}}(s) = \frac{Z_{C\mathrm{out}}}{1 + L(s)} \tag{10}$$

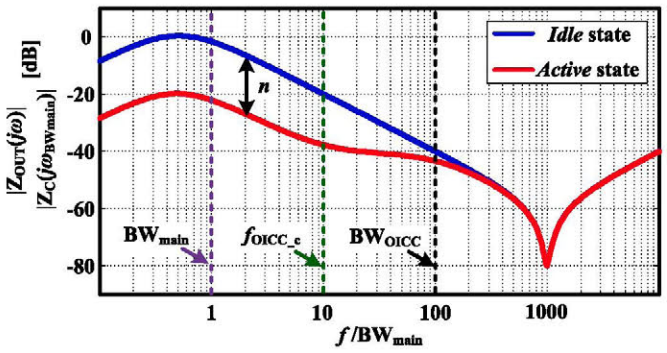

Fig. 9. Output impedance of the system in *Idle* (blue) and *Active* (red) states.

TABLE I
CONVERTER SPECIFICATION

	Low_C_{OUT} prototype	High_C_{OUT} prototype
Main Conv. (two-phase PCMC)		
V_{IN}	5 V	5 V
V_{OUT}	1.5 V	1.5 V
f_{SW} **per Phase**	150 kHz	150 kHz
BW_{main}	20 kHz	20 kHz
L per Phase	2 μH	2 μH
C_{OUT}	**Ceramic: 3** $\times$ **47** μ**F** (ESL = $\sim$4 nH, ESR = $\sim$7 mΩ);	**OSCON: 2**$\times$ **560** μ**F** (ESL = $\sim$9 nH, ESR = $\sim$18 mΩ); **Ceramic: 8**$\times$ **100** μ**F** (ESL = $\sim$2 nH, ESR = $\sim$5 mΩ); **Ceramic: 2**$\times$ **47** μ**F** (ESL = $\sim$1 nH, ESR = $\sim$5 mΩ)
MOSFETs	SI4866BDY	SI4866BDY
Driver	ISL6605	ISL6605
Auxiliary Conv.		
f_{SW_OICC}	5 MHz	–
L_{OICC}	100 nH	–
n	15	–
f_{OICC_c}	50 kHz	–
BW_{OICC}	700 kHz	–
MOSFETs	FDMS7620S	–
Driver	ISL6605	–

where $L(s)$ is the open-loop gain in *Idle* state. The output impedance with OICC is

$$Z'_{OUT}(s) = \frac{Z_{Cout}^{EQ}}{1 + L'(s)} \xrightarrow{f<f_{OICC_c}} Z'_{OUT}(s) = \frac{Z_{OUT}(s)}{n}. \quad (11)$$

The output impedance of the system in both *Idle* and *Active* state is plotted in Fig. 9. The reduction of the output impedance of the system in *Active* state by a factor n is achieved up to the OICC corner frequency f_{OICC_c}.

IV. SIMULATIONS AND EXPERIMENTAL VALIDATION

In order to demonstrate and compare the simulated with the real dynamic behavior, two prototypes, Low_C_{OUT} and High_C_{OUT}, have been designed and built for the specifications presented in Table I. The first prototype, Low_C_{OUT}, has the output capacitor of 140 μF and it utilizes the OICC in order to improve the dynamic behavior. The OICC has been implemented as a synchronous buck converter with PCMC which has multiplication factor of 15 and the OICC corner frequency f_{OICC_c} at 50 kHz and the bandwidth BW_{OICC} of 700 kHz. On the other hand, High_C_{OUT} prototype has been designed to have the same power stage as Low_C_{OUT} prototype with the difference that, instead of using the OICC, it has 15 times bigger output capacitor (2.1 mF), which is implemented with two OSCON capacitor of 570 μF, eight ceramic capacitors of 100 μF and two ceramic capacitors of 47 μF. The estimated area for the output capacitor for High_C_{OUT} prototype, obtained by summing footprints areas of the capacitors, is 200.6 mm^2, while in the case of Low_C_{OUT} prototype, the estimated area is 92.8 mm^2, considering the footprints of output capacitors and the auxiliary OICC power stage (inductor, MOSFETs, and driver). As it is presented, the used area for the output capacitor and the OICC in a discrete implementation is only 46% of the area used for High_C_{OUT} prototype. Higher area reduction would be expected by integrating the OICC subsystem. In addition, the reliability of the system has been improved since Low_C_{OUT} prototype is using only ceramic capacitors, which have significantly bigger lifetime and reliability compared to the OSCON capacitors employed in High_C_{OUT} prototype.

In following sections, the experimental results of both prototypes are presented. All the experiments are performed using on-board resistive dummy load, which produces load steps of $\pm$8.2 A (SR+ = 11 A/μs and SR– = $-$270 A/μs). In Section IV-A, the basic operation is presented comparing Low_C_{OUT} prototype with and without the OICC and the High_C_{OUT} prototype. In Section IV-B, an experiment with repetitive load steps is performed demonstrating the robustness of the system. Section IV-C presents the results for a variation of the output capacitor, causing mismatching of the output capacitor current estimator, which was identified as the most critical part of the system in [25]. In Section IV-D, a comparison of the static and dynamic efficiency is presented. Finally, in Section IV-E, the design guidelines are provided.

A. Basic Operation

In this section, the basic operation of the system is validated both in simulation and experimentally. The system simulations under the resistive load step of $\pm$8.2 A (slew rate: SR+ = 11 A/μs and SR– = $-$270 A/μs) are performed for Low_C_{OUT} prototype system both with and without the OICC and on the High_C_{OUT} prototype system. The simulations have been done including all the parasitics of both components and the board. The corresponding waveforms for the load stepup are presented in Figs. 10, 11, and 12, respectively. It can be seen that Low_C_{OUT} prototype with the OICC (see Fig. 10) has similar behavior as High_C_{OUT} prototype (see Fig. 12), having the undershoot of $\sim$30 mV and the transient of $\sim$200 μs, with the difference that the high frequency ripple at the output voltage exists due to the switching of the auxiliary buck and big parasitic inductance (equivalent series inductance ESL) of the output capacitor, as demonstrated experimentally in Fig. 13. The biggest part of the ESL is originated from the vias that connect the negative terminal of the output capacitor to the ground

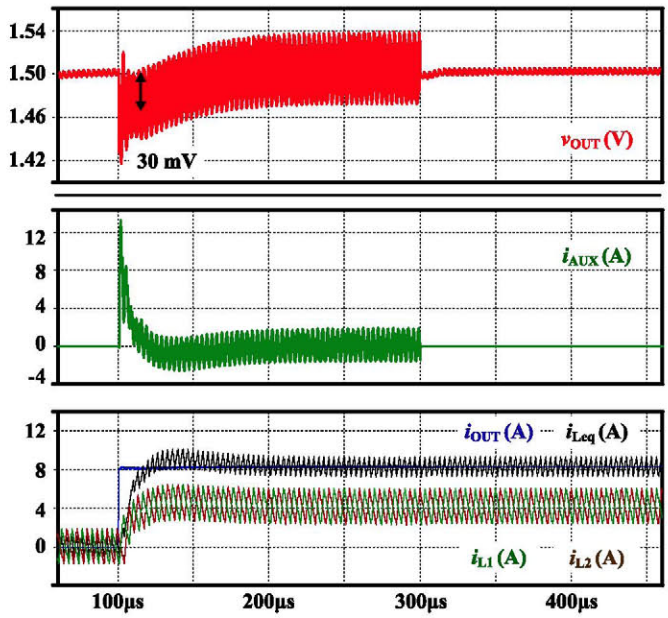

Fig. 10. Simulation results—load step-up in the Low_C_{OUT} prototype with the OICC: C_{OUT} 140 μF.

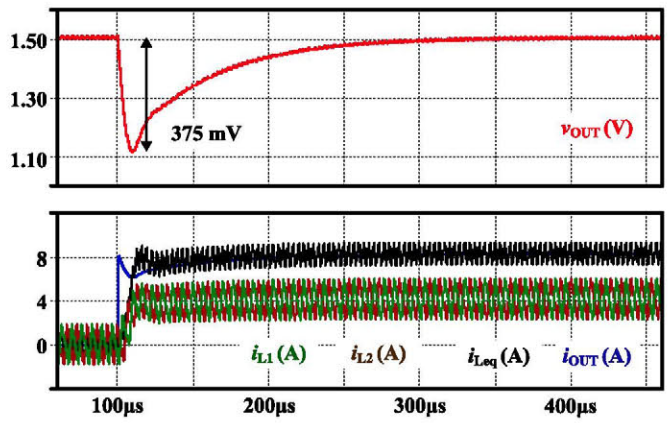

Fig. 11. Simulation results—load step-up in the Low_C_{OUT} prototype without the $OICC$: C_{OUT} 140 μF.

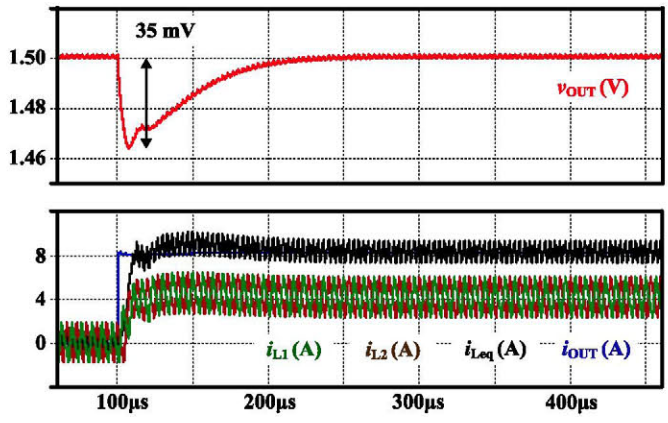

Fig. 12. Simulation results—load step-up in the High_C_{OUT} prototype: C_{OUT} 2.1 mF.

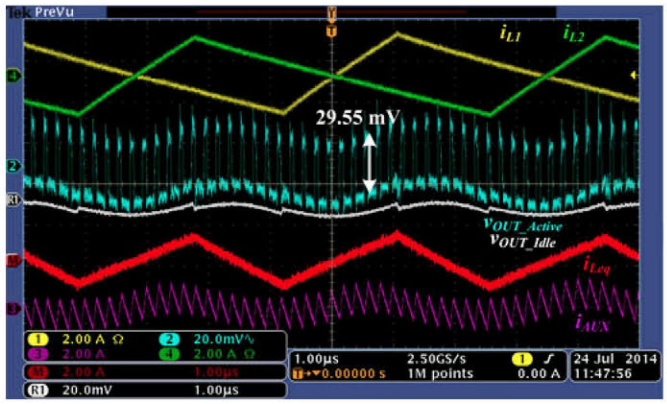

Fig. 13. Experimental results—the Low_C_{OUT} prototype steady-state switching ripple with and without the OICC: the first phase current i_{L1} (yellow 2 A/div), the second phase current i_{L2} (green 2 A/div), sum of the first and second phase current i_{Leq} (red 2 A/div), the output voltage with OICC active v_{OUT_Active} (blue 20 mV/div), the output voltage with OICC inactive v_{OUT_Idle} (white 20 mV/div), the auxiliary current i_{AUX} (pink 2 A/div) and time 1 μs/div.

plane. It can be seen in Fig. 13 that the high-frequency peak-to-peak output voltage ripple when the OICC is active is 29 mV (v_{OUT_Active}, blue) and it occurs at the time instances where the auxiliary current changes its slopes. Furthermore, the output voltage during the *Idle* state, v_{OUT_Idle} (white), is presented together with both phase currents i_{L1} (yellow), i_{L2} (green) and the sum phase currents i_{Leq} (red). Since the phase interleaving is used, the sum of the phase currents has a 300 kHz ripple which can be seen in the output voltage in the both states, v_{OUT_Active} and v_{OUT_Idle}. Since the ripple frequency is inside the OICC bandwidth (700 kHz), the auxiliary current i_{AUX} (pink) is trying to compensate it, as it can be seen in Fig. 13. Measured total equivalent inductance is 1.2 nH, while the vias total inductance is 680 pH (56% of total equivalent inductance). The ESL and consequently the output voltage ripple can be reduced by employing better PCB technology.

As it can be seen in Fig. 10, the Low_C_{OUT} prototype with the OICC does not enter in an additional settling transient which existed in [25], due to the end of transient detection improvement and implementation of Pk_Avg compensation block. Furthermore, the Low_C_{OUT} prototype with the OICC has 12 times smaller deviation compared to the case when the OICC is inactive (375 mV), which is presented in Fig. 11.

In order to verify the assumptions made in the simulations, the same experiment has been performed for both prototypes under the same conditions and the waveforms are presented in Figs. 14 and 15, for Low_C_{OUT} prototype with the OICC and in Fig. 16 without the OICC, while the results for High_C_{OUT} prototype are presented in Fig. 17. It can be observed that the results are in good agreement with the simulations for both prototypes (see Figs. 10–12). It is very important to highlight that the current sharing between the two phases of the main converter is perfectly balanced during both the steady state and the transients.

Furthermore, Figs. 14 and 15 show how auxiliary current is injected at the output node only during the transient and how

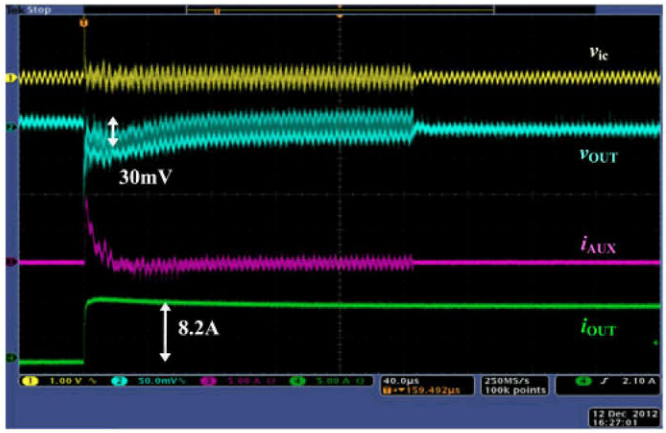

Fig. 14. Experimental results—load step-up in the Low_C_{OUT} prototype with active OICC: the load current i_{OUT} (green 5 A/div), the auxiliary current i_{AUX} (pink 5 A/div), the output voltage v_{OUT} (blue 50 mV/div), estimated capacitor current v_{Ic} (yellow 1 V/div) and time 40 μs/div.

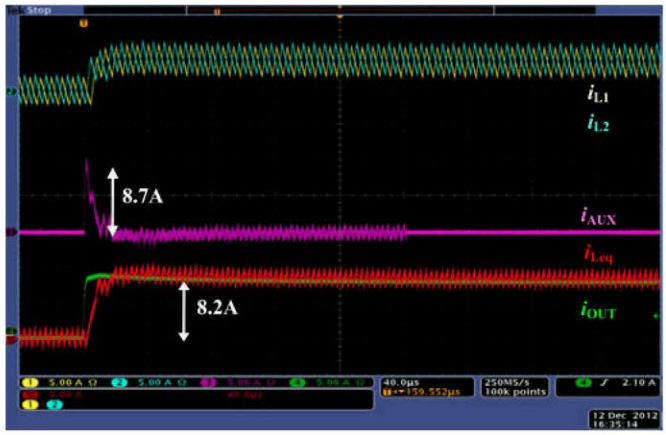

Fig. 15. Experimental results—load step-up in the Low_C_{OUT} prototype with active OICC: the load current i_{OUT} (green 5 A/div), the auxiliary current i_{AUX} (pink 5 A/div), the first phase current i_{L1} (yellow 5 A/div), the second phase current i_{L2} (blue 5 A/div), sum of the first and second phase current i_{Leq} (red 5 A/div) and time 40 μs/div.

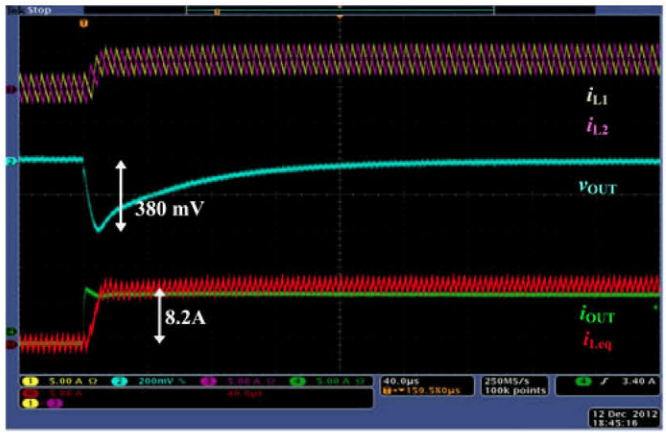

Fig. 16. Experimental results—load step-up in the Low_C_{OUT} prototype with inactive OICC: the load current i_{OUT} (green 5 A/div), the first phase current i_{L1} (yellow 5 A/div), the second phase current i_{L2} (pink 5 A/div), the output voltage v_{OUT} (blue 200 mV/div), sum of the first and second phase current i_{Leq} (red 5 A/div) and time 40 μs/div.

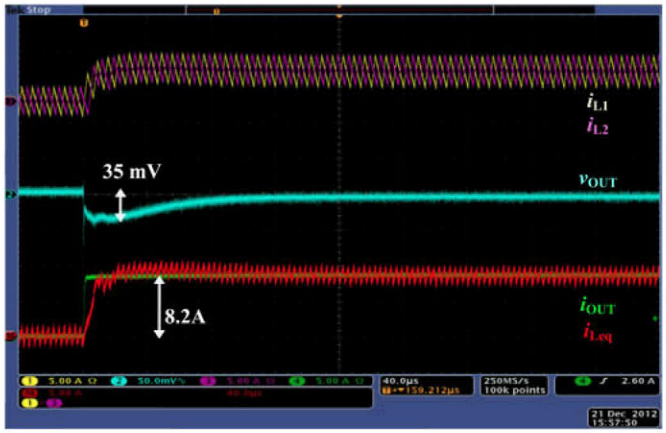

Fig. 17. Experimental results—load step-up in the High_C_{OUT} prototype: the load current i_{OUT} (green 5 A/div), the output voltage v_{OUT} (blue 50 mV/div), the first phase current i_{L1} (yellow 5 A/div), the second phase current i_{L2} (pink 5 A/div), sum of the first and second phase current i_{Leq} (red 5 A/div) and time 40 μs/div.

TABLE II
OUTPUT VOLTAGE DEVIATION

		Low_C_{OUT} prototype (inactive OICC)	Low_C_{OUT} prototype (active OICC)	High_C_{OUT} prototype
Load	*simulation*	−375 mV	−30 mV	−35 mV
step-up	*experiment*	−380 mV	−30 mV	−35 mV
Load	*simulation*	500 mV	45 mV	40 mV
step-down	*experiment*	520 mV	45 mV	45 mV
Repetitive	*simulation*	585 mV_{P-P}	70 mV_{P-P}	45 mV_{P-P}
load-steps	*experiment*	600 mV_{P-P}	70 mV_{P-P}	50 mV_{P-P}

the high frequency ripple is degrading the output voltage, which can be improved, as said previously, by utilizing better PCB-layout technology to reduce the parasitic inductance of the vias. Fig. 15 presents all the currents in Low_C_{OUT} prototype system. It can be seen how the auxiliary current (pink) is compensating the difference between the load current (green) and the sum of the phase currents (phase currents: yellow and blue; sum: red). Fig. 16 presents the results of Low_C_{OUT} prototype without the OICC where it can be seen that the output voltage deviation is 380 mV, compared to the 30 mV when the OICC is active, as presented in Fig. 14. Fig. 17 shows all the system variables of High_C_{OUT} prototype. Comparing the waveforms of Low_C_{OUT} prototype with corresponding ones of High_C_{OUT} prototype, it can be seen that both the output voltage v_{OUT} (see blue in Fig. 14 and blue in Fig. 17) and the sum of the phase currents $i_{L_{eq}}$ (see red in Fig. 15 and red in Fig. 17) have the same dynamic behavior in both systems. The summary of the results for all three cases are presented in Table II where it can be seen that the experimental results are in a good agreement with the simulations for both load step-up and load step-down.

B. *System Robustness on Repetitive Load Steps*

As commented earlier, for most of the SoA solutions, the behavior of the system under repetitive load steps is unknown. Even more, for systems which are employing charge balance

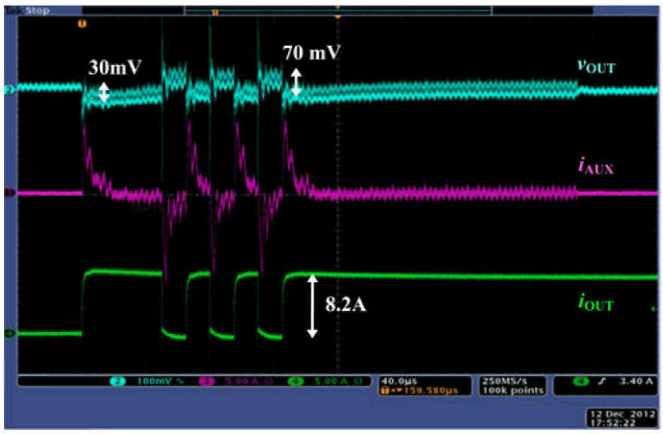

Fig. 18. Experimental results—repetitive load steps—Low_C_{OUT} prototype with active OICC: the load current i_{OUT} (green 5 A/div), the auxiliary current i_{AUX} (pink 5 A/div), the output voltage v_{OUT} (blue 50 mV/div) and time 40 μs/div.

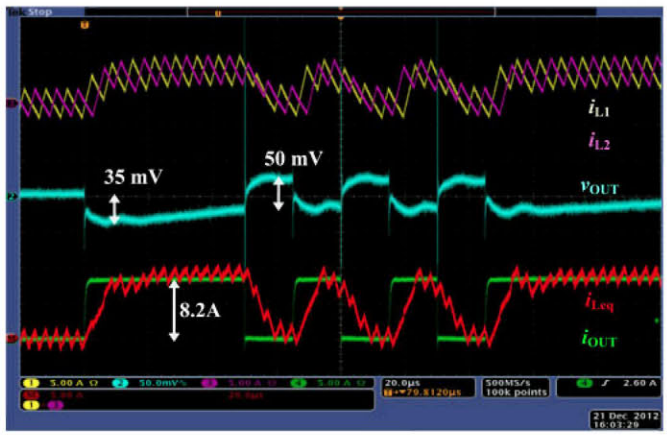

Fig. 19. Experimental results—repetitive load steps—High_C_{OUT} prototype: the load current i_{OUT} (green 5 A/div), the output voltage v_{OUT} (blue 50 mV/div), the first phase current i_{L1} (yellow 5 A/div), the second phase current i_{L2} (pink 5 A/div), sum of the first and second phase current i_{Leq} (red 5 A/div) and time 20 μs/div.

technique, repetitive load-steps may create big settling transient at the end of the transient routine due to the fact that the system is in open loop and it is unaware of additional load steps. Since the OICC concept is always operating in closed loop, the system is inherently robust on repetitive load steps as demonstrated in simulation in [25]. In this section, that statement is demonstrated experimentally. The waveforms of the Low_C_{OUT} prototype state variables are presented in Fig. 18. After the initial load step, the system has changed its state to *Active* state and the OICC improves the response. After 50 μs, while the system is still in the transient routine, the repetitive load current starts to switch with 30 μs ON/OFF period, as it can be seen in the load current (green, Fig. 18). Since the OICC is already active, it compensates the perturbation immediately (see auxiliary current in Fig. 18, pink) while the main converter is reacting as well. As a result, 70 mV peak-to-peak output voltage deviation occurs, which is in a good agreement with the simulation, as shown in Table II. On the other hand, when the OICC is inactive, for the same load current pattern, measured peak-to-peak deviation is 600 mV, very close to the simulated value (585 mV). Additionally, comparing the response of Fig. 18 with Fig. 14, it can be seen that total transient routine is prolonged in the case of the repetitive load steps, lasting in total 320 μs, compared to 200 μs of a single load step transient routine.

Furthermore, Fig. 19 shows state variables of the High_C_{OUT} prototype under the same pulsating load current pattern. It can be seen how the sum of inductor currents compensates the pulsating perturbation, achieving a total output voltage peak-to-peak deviation of 50 mV (45 mV in simulation). The result is comparable to the one obtained in Low_C_{OUT} prototype with the OICC.

C. Effect on the Robustness of the Output Capacitor Current Estimator Mismatch and the Output Capacitor Variation

The output capacitor current estimator is identified as the most critical and sensitive subsystem of the proposed concept. Due to the variation of the parasitics, the current estimator behavior can be drastically affected, leading to a deteriorated estimation of the capacitor current. Although the estimator exhibits high sensitivity, the overall system is stable under variations of the current estimator input impedance, as demonstrated in [25]. In this section, the robustness of the system under the mismatching of the current estimator due to the output capacitors parameters variation is analyzed and experimentally validated. In the following analysis, the output capacitor value variation is represented as a scaled value with a parameter α, assuming that the equivalent series resistance ESR has an opposite trend of variation with respect to the capacitance and that the ESL is constant, since its value is determined by vias parasitic inductance, which connect the negative terminal of the capacitor to the ground plane. The capacitor impedance is defined by

$$\begin{aligned} Z_{\mathrm{Cout}}(s) &= \frac{1}{s\alpha C_{\mathrm{OUT}}} + \frac{ESR}{\alpha} + sESL \\ &= \frac{1 + sC_{\mathrm{OUT}}ESR + s^2 ESL\alpha C_{\mathrm{OUT}}}{s\alpha C_{\mathrm{OUT}}}. \end{aligned} \quad (12)$$

On the other hand, the output capacitor current estimator is designed for the nominal case, in that manner that the estimator input impedance is k_S times bigger than the nominal output capacitor impedance

$$\begin{aligned} Z_S(s) &= \frac{k_S}{sC_{\mathrm{OUT}}} + k_S ESR + sk_S ESL \\ &= k_S \frac{1 + sC_{\mathrm{OUT}}ESR + s^2 ESLC_{\mathrm{OUT}}}{sC_{\mathrm{OUT}}}. \end{aligned} \quad (13)$$

The capacitor current measurement transfer function, based on the model presented in Fig. 5, can be defined as

$$\begin{aligned} G_{Ic}(s) &= \frac{v_{Ic}}{i_C} = \beta R_{FB}\frac{Z_{\mathrm{Cout}}}{Z_s} \\ &= \frac{\beta R_{FB}}{k_s \alpha}\frac{1 + sC_{\mathrm{OUT}}ESR + s^2\alpha ESLC_{\mathrm{OUT}}}{1 + sC_{\mathrm{OUT}}ESR + s^2 ESLC_{\mathrm{OUT}}}. \end{aligned} \quad (14)$$

The voltage amplifier β is used to define a unity gain of the current estimator in the nominal case; thus, its gain is k_S/R_{FB}, which modifies (14) to

$$G_{Ic}(s) = \frac{1}{\alpha}\frac{1 + sC_{OUT}ESR + s^2\alpha ESLC_{OUT}}{1 + sC_{OUT}ESR + s^2 ESLC_{OUT}}. \quad (15)$$

When the system is in *Active* State, the output capacitor impedance is modified with OICC subsystem open-loop gain L_{OICC}, which is equal to $F(s)$ in the initial case, and defining the equivalent output capacitor impedance with (8). If the current estimator mismatch is taken into account, the OICC subsystem open-loop gain L_{OICC} is modified and defined by

$$\begin{aligned} L_{OICC}(s) &= G_{Ic}(s)F(s)G_{Iaux}(s),\ G_{Iaux}(s) \\ &= \frac{i_{AUX}}{v_{Iaux\_ref}} \end{aligned} \quad (16)$$

where $G_{I_{aux}}$ is the auxiliary current reference to auxiliary current transfer function and $F(s)$ is defined by (7).

Finally, the impedance of the equivalent output capacitor is

$$\begin{aligned} Z^{EQ}_{Cout}(s) &= \frac{Z_{Cout}}{1 + L_{OICC}} \\ &= \frac{1 + sC_{OUT}ESR + s^2\alpha ESLC_{OUT}}{\alpha sC_{OUT}\left(1 + G_{Ic}(s)F(s)G_{Iaux}(s)\right)} \end{aligned} \quad (17)$$

$$Z^{EQ}_{Cout}(s) = \frac{1}{sC_{OUT}(n + \alpha - 1)},\ f < f_{OICCc}. \quad (19)$$

If the capacitor multiplier n is significantly bigger than $(\alpha - 1)$, which is usually the case, (19) can be further simplified to

$$Z^{EQ}_{Cout}(s) = \frac{1}{snC_{OUT}} = \frac{Z^{nom}_C}{n},\ \ (f < f_{OICCc}) \wedge (n > \alpha - 1). \quad (20)$$

Equation (20) shows that in the low frequency range the mismatching effect is annulated due to the OICC subsystem loop-gain transfer function L_{OICC} and that the equivalent output capacitor impedance remains the same, as shown in Fig. 20 (nominal case: red, dotted; Case A ($\alpha = 0.7$): blue, solid; and Case B ($\alpha = 1.3$): black, solid). From the analysis earlier, it can be concluded that, since the equivalent capacitor impedance is the same as in the nominal case, the main system converter has the same loop-gain characteristics during *Active* state and that the closed-loop impedance of the system remains as in (11). Finally, this yields to the conclusion that the low-frequency response of the system (averaged signals) on the load perturbation will be the same in terms of the transient length and the deviation of the output voltage.

On the other hand, the OICC subsystem loop-gain is affected by variations of the output capacitance. In the analysis presented

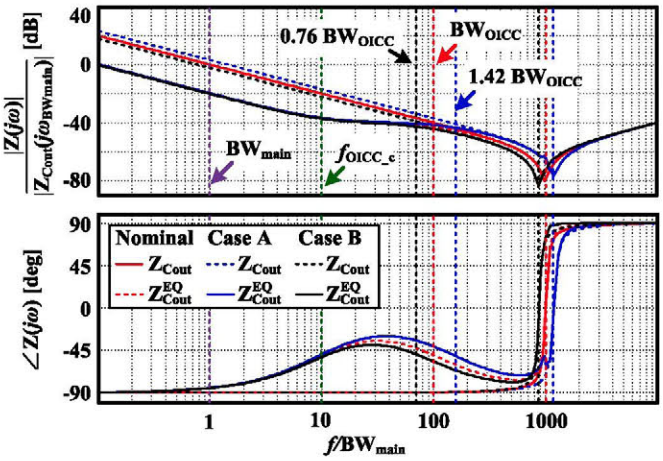

Fig. 20. Magnitude and phase transfer functions of the impedance at the output node in nominal case: *Idle* (red, solid) and *Active* (red, dotted) state; in Case A: *Idle* (blue, dotted) and *Active* (blue, solid) state; and in Case B: *Idle* (black, dotted) and *Active* (black, solid) state.

earlier, the CCS is assumed ideal in all the frequency range. Due to the PCMC buck converter implementation, the CCS has a limited bandwidth defined by its switching frequency $f_{OICC-SW}$. Since $f_{OICC-SW}$ is a higher frequency than f_{OICC_c}, the performed analysis is valid. In order to ensure the stability of the OICC subsystem loop-gain, $f_{OICC-SW}$ should be at least five times higher than the OICC subsystem bandwidth BW_{OICC}. On the other hand, the switching frequency should be as low as possible, to reduce the switching losses of the auxiliary converter; thus, mentioned criteria ($f_{OICC-SW} = 5\ BW_{OICC}$) are a good tradeoff between stability and efficiency. According to [30], the PCMC buck converter current reference to inductor current small signal transfer function has a double conjugate pole at half of the converter switching frequency; thus, the OICC auxiliary current reference to auxiliary current transfer function G_{IAUX} can be modeled as

$$G_{Iaux}(s) = \frac{1}{\left(1 + s\frac{2}{Q\omega_{OICC-SW}} + s^2\frac{4}{\omega^2_{OICC-SW}}\right)} \quad (21)$$

where Q is a quality factor of the double-pole and it depends on the auxiliary inductor current slopes and the compensating ramp. Again, according to [30], a good tradeoff between linearity of the amplitude characteristics and the deviation of the phase characteristics of G_{IAUX} can be achieved if Q is designed to have unity value. Implementing (21) into (16) and assuming that the output capacitor resonance is at much higher frequencies than the OICC subsystem bandwidth BW_{OICC}, the OICC subsystem

$$Z^{EQ}_{Cout}(s) = \frac{1 + sC_{OUT}ESR + s^2\alpha ESLC_{OUT}}{\alpha sC_{OUT}\left(1 + G_{Iaux}(s)\frac{n-1}{\alpha}(1 + sC_{OUT}ESR + s^2\alpha ESLC_{OUT})\Big/\left(1 + \frac{s}{p_{OICC\_c}}\right)(1 + sC_{OUT}ESR + s^2 ESLC_{OUT})\right)} \quad (18)$$

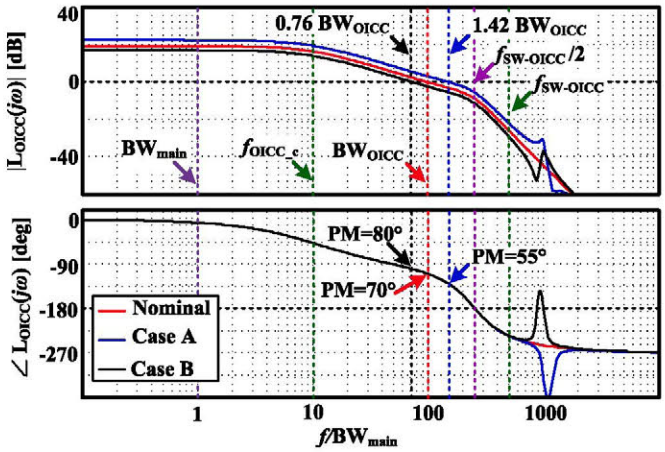

Fig. 21. OICC open-loop amplitude and phase transfer functions in nominal case (red), Case A (blue) and Case B (black).

loop-gain transfer function can be defined as

$$L_{\mathrm{OICC}}(s)=\frac{n-1}{\alpha\left(1+\frac{s}{p_{\mathrm{OICC\_c}}}\right)\left(1+\frac{2s}{Q\omega_{\mathrm{OICC-SW}}}+\frac{4s^2}{\omega^2_{\mathrm{OICC-SW}}}\right)}. \tag{22}$$

From (22), it can be concluded that the mismatching of the current estimator affects the dc gain, while the singularities remain on the same frequencies. Modification of the dc gain further modifies the bandwidth of the OICC which is defined as

$$\mathrm{BW}_{\mathrm{OICC}}=\frac{(n-1)\,p_{\mathrm{OICC\_c}}}{\alpha}. \tag{23}$$

Finally, the modification of the BW_{OICC} affects the stability of the loop, since the phase margin (PM) is defined by the double pole at half of the OICC switching frequency. In Fig. 21, loop-gain characteristics, including the resonances mismatch of the current estimator, are presented for all three cases (nominal: red, Case A ($\alpha=0.7$): blue and Case B ($\alpha=1.3$): red). It can be seen that, in the nominal case, the PM is 70° providing maximally flat amplitude characteristic of the auxiliary current, since it is defined as

$$i_{\mathrm{AUX}}(s)=\frac{L_{\mathrm{OICC}}(s)}{1+L_{\mathrm{OICC}}(s)}i^{\mathrm{EQ}}_{\mathrm{Cout}}(s). \tag{24}$$

When the output capacitor capacitance is reduced (Case A), the gain and, respectively, the bandwidth are increased 1.42 times. As a result, PM is reduced to 55°; thus, it is expected that auxiliary current has increased oscillatory behavior. On the other hand, when the output capacitor capacitance is increased (Case B), the gain and the bandwidth are decreased 0.76 times. The PM is increased to 80°, so the auxiliary current will have more dumped response.

Both Cases A and B are experimentally validated and the waveforms of the auxiliary current (pink), the output voltage (blue), and the output capacitor current measurement (yellow) are presented in Figs. 22 and 23, respectively. As expected, the output voltage low-frequency deviation in both cases is nearly the same with respect to the nominal case, presented in Fig. 14. Comparing the responses of the auxiliary current, in Case A scenario (see Fig. 22), the waveform has more oscillatory response with respect to the nominal case (see Fig. 14, pink) due to the increased bandwidth and decreased PM, while in Case B scenario (see Fig. 23), the waveform has more dumped response.

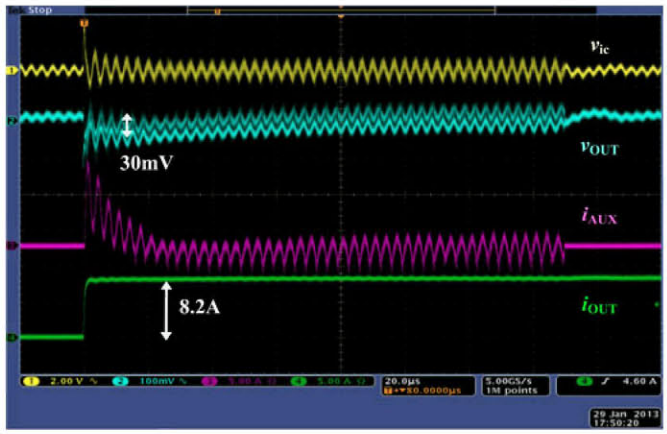

Fig. 22. Experimental results. The output capacitor variation: $C'_{\mathrm{OUT}}=0.7\,C_{\mathrm{OUT}}$—the load step-up—Low_$C_{\mathrm{OUT}}$ prototype: the load current i_{OUT} (green 5 A/div), the auxiliary current i_{AX} (pink 5 A/div), the output voltage v_{OUT} (blue 50 mV/div), estimated capacitor current v_{Ic} (yellow 2 V/div) and time 20 μs/div.

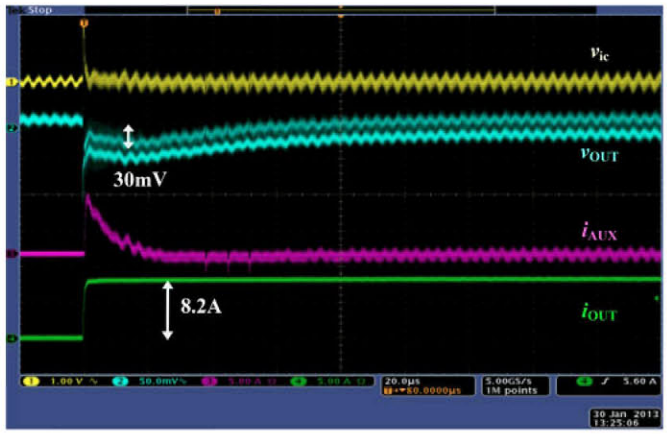

Fig. 23. Experimental results. The output capacitor variation: $C'_{\mathrm{OUT}}=1.3\,C_{\mathrm{OUT}}$—the load step-up—Low_$C_{\mathrm{OUT}}$ prototype: the load current i_{OUT} (green 5 A/div), the auxiliary current i_{AX} (pink 5 A/div), the output voltage v_{OUT} (blue 50 mV/div), estimated capacitor current v_{Ic} (yellow 1 V/div) and time 20 μs/div.

As presented, the overall system remains stable under variation of the output capacitor capacitance by $\pm30\%$. Although the capacitor current estimator measurement is affected, the output voltage has nearly the same response as in the nominal case, while the auxiliary current response is affected. With this in mind, a variation of the output capacitor, due both to the tolerances and aging effects, needs to be taken into account in order to ensure the stability of the OICC subsystem and consequently the overall system.

D. Static and Dynamic System Efficiency Comparison

As demonstrated so far, the OICC concept improves dynamic response of the initial system achieving a dynamic behavior

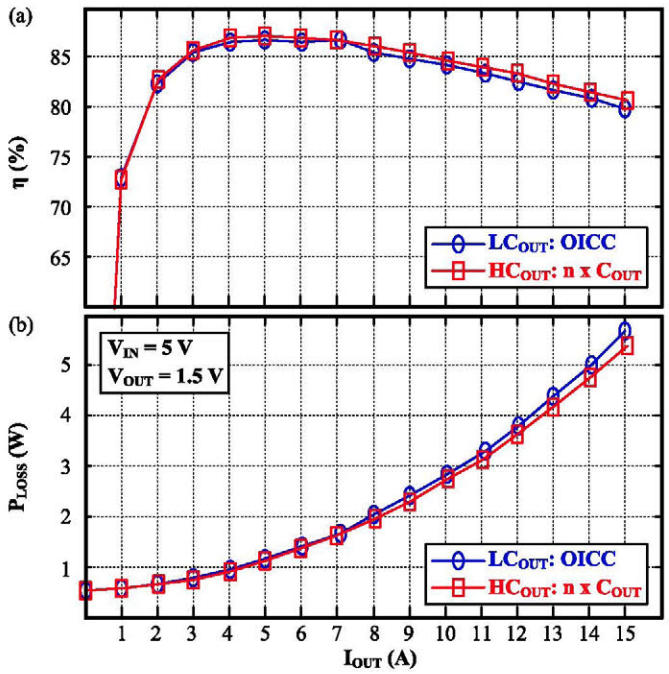

Fig. 24. Static characteristics comparison—Low_C_{OUT} prototype (blue; circles) and High_C_{OUT} prototype (red; squares): (a) efficiency comparison and (b) power losses comparison.

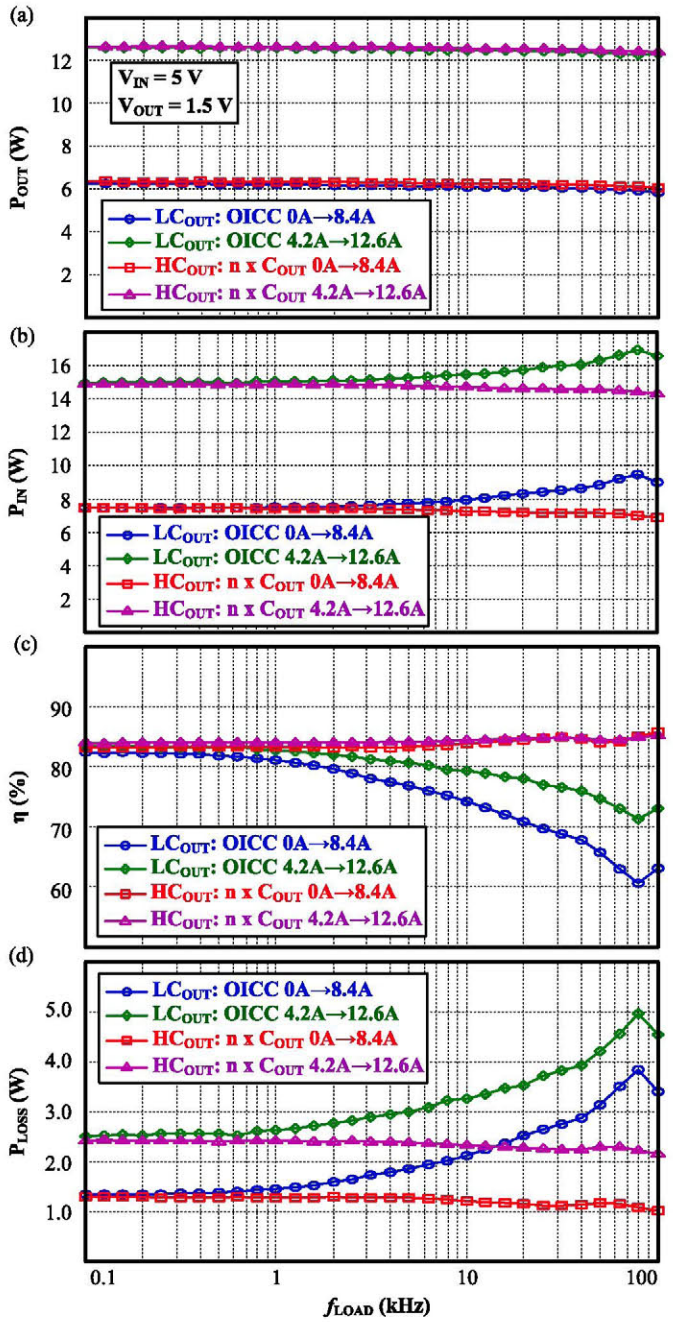

Fig. 25. Dynamic characteristics comparison—Low_C_{OUT} prototype with load steps from 0 to 8.4 A (blue; circles); Low_C_{OUT} prototype with load steps from 4.2 to 12.6 A (green; diamonds); High_C_{OUT} prototype with load steps from 0 to 8.4 A (red; squares); High_C_{OUT} prototype with load steps from 4.2 to 12.6 A (pink; triangles): (a) the average output power, (b) average input power, (c) efficiency, and (d) power losses comparison.

equivalent to system with 15 times bigger output capacitor, while using smaller footprint area. The biggest drawback of all concepts based on an AEP is an increase of the system power losses during the transient, since the auxiliary energy path has worse efficiency than the main converter. In this section, the impact on the power losses of the OICC concept is presented. Since Low_C_{OUT} and High_C_{OUT} prototypes have the same main converter and the same dynamic behavior, it can be assumed that, during the transients, both main converters are generating similar losses, while the added losses to the Low_C_{OUT} prototype are originated from the OICC. In Fig. 24, the static characteristics are presented, showing that both main converters have nearly the same efficiency [see Fig. 24 (a)] and power losses [see Fig. 24(b)], since the OICC is inactive during the steady-state operation. The efficiency measurements are performed with 5 V input voltage and 1.5 V output voltage. As it can be seen from Fig. 24, the efficiency curves are relatively low, due to the high conduction losses, generated on 20 mΩ shunt resistances, which are used to measure phase currents. The efficiency can be improved by using noninvasive sensors (*RC* impedance matching or current transformers). Due to the shunt resistances, at full load, additional 2.25 W of losses is generated, reducing the efficiency by 7%. Since the focus of this part of the study is the impact of the OICC circuit on the losses, the shunt resistance losses are not excluded from the efficiency calculation.

Further, the dynamic characteristics have been measured and presented in Fig. 25. The systems are tested with a pulsating load current with 50% duty cycle, while the sweep is performed changing the frequency of the load steps. Two sets of experiments have been performed on both prototypes: in the first one, the load current is switching from 0 to 8.4 A, while in the second the current is switching between 4.2 and 12.6 A with 5 V input voltage and 1.5 V output voltage. Due to the fact that the duty cycle is 50%, the averaged output power is relatively constant for each load current frequency; the output power is 6.3 W, for the first experiment, and 12.6 W, for the second one as presented in Fig. 25(a). The total average input power has been measured as well and presented in Fig. 25(b). Furthermore,

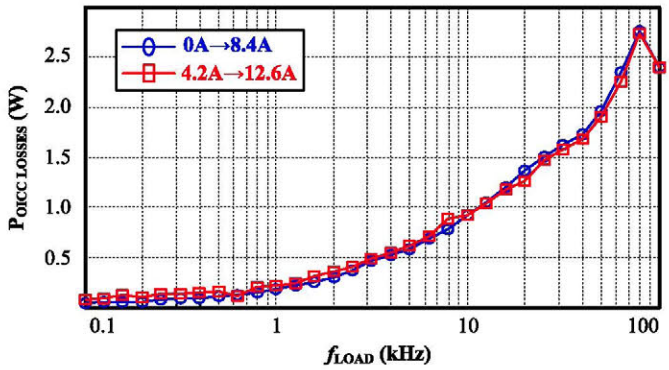

Fig. 26. OICC average dynamic power losses dependence on the load steps frequency—load steps from 0 to 8.4 A (blue; circles); load steps from 4.2 to 12.6 A (red; squares).

in Fig. 25(c) and (d), dynamic efficiency, defined as the ratio between averaged output and input powers, and total average power losses are presented. As it can be seen, when the systems are operating with low load current frequency, the input power, the efficiency and the power losses are nearly the same comparing Low_C_{OUT} and High_C_{OUT}prototypes for corresponding cases: Low_C_{OUT} prototype with 0 to 8.4 A load jump (blue; circles) with High_C_{OUT} prototype with 0 to 8.4 A load jump (red; squares) and Low_C_{OUT} prototype with 4.2 to 12.6 A load jump (green; diamonds) with High_C_{OUT} prototype with 4.2 to 12.6 A load jump (pink; triangles). This is due to the fact that the time interval when the OICC is active is smaller compared to the load current period; thus, the losses are defined by the static behavior of both prototypes. As the load current frequency increases, the OICC operation time interval becomes more relevant, causing an increase of the power losses of the Low_C_{OUT} prototype (4.2–12.6 A load steps (blue; circles) and 4.2–12.6 A load steps (green; diamonds)) and consequently the drop in the efficiency. The maximum is achieved at 80 kHz load current frequency when the auxiliary current starts to reduce its amplitude due to the limited bandwidth of the OICC subsystem and implemented auxiliary current reference generator transfer function defined by (7). Finally, the OICC power losses dependence is provided in Fig. 26, where the comparison between the two experiments is presented. The losses are obtained by subtracting the power losses of the Low_C_{OUT} and High_C_{OUT} prototypes. It can be concluded that the OICC losses do not depend on the total output power, rather than the amplitude of the load step. Once again, the maximum is at 80 kHz, while the expected tendency of the losses value is that the OICC losses reduce to no-load losses above OICC subsystem bandwidth, BW_{OICC}, since the OICC stops to inject the current and all the perturbation is compensated by the output capacitor. With this in mind, it can be expected that the biggest impact on the system losses is in the frequency range from around one tenth of the main converter bandwidth (2 kHz) up to the OICC subsystem bandwidth (700 kHz). If the behavior of the load is known, it is possible to determine average power which the OICC needs to handle and further optimize the system to improve efficiency.

E. Design Guidelines

As demonstrated so far, the OICC system has the same behavior as the referent system with $n-1$ times bigger capacitance; thus, in order to design the OICC system, the first step is to design the High_C_{OUT} prototype. The focus of the optimization of the High_C_{OUT} prototype is to achieve as higher efficiency of the system as possible, while satisfying dynamic specification. After the optimization has been performed, the main converter of the Low_C_{OUT} prototype is obtained.

The second step is the design of the OICC subsystem. In order to design the OICC subsystem, multivariable optimization needs to be employed, where the inputs are the bandwidth of the main converter BW_{main}, the value of the output capacitance C_{OUT}, the deviation of the output voltage Δv_{OUT} and load behavior statistics: probability of the load steps and the amplitude of the load steps ΔI_{OUT}. The outputs of the optimization are the multiplication factor n, the OICC corner frequency $f_{\mathrm{OICC\_c}}$, the OICC switching frequency $f_{\mathrm{SW-OICC}}$, the inductor L_{OICC}, and the power losses estimation. From the bandwidth of the main converter, a minimal OICC corner frequency $f_{\mathrm{OICC_c}}$ is defined as twice the BW_{main}. This ensures that the deviation of the output voltage will be the same in both designs since the impedance is improved at the bandwidth of the main converter system. The corner frequency can be increased to improve the dynamic behavior penalizing the efficiency of the system as explained in previous section and shown in Fig. 26. Next step is to perform a tradeoff between n and losses of the system. As n is increased, the instantaneous auxiliary current is also increased. Furthermore, the bandwidth of the OICC subsystem BW_{OICC} is determined as $(n-1)f_{\mathrm{OICC_c}}$, which is defining the OICC switching frequency as five times bigger to ensure that auxiliary converter is behaving as a CCS. In other words, the OICC switching frequency is

$$\begin{aligned} f_{\mathrm{SW-OICC}} &= 5\mathrm{BW}_{\mathrm{OICC}} = 5(n-1)f_{\mathrm{OICC\_c}} \\ &= 10(n-1)\mathrm{BW}_{\mathrm{main}}. \end{aligned} \tag{25}$$

Both n and $f_{\mathrm{SW-OICC}}$ increase the losses in the OICC subsystem. Finally, the OICC inductance is designed based on the maximal slew-rate of auxiliary current reference $v_{\mathrm{Iaux\_ref}}$. The goal of optimization is to achieve reduction in size and area of the output capacitor while minimally influencing the losses of the system.

Regarding the system controller, its implementation can be done using singe D-Latch gate to define both states of the system, while detections of the start and end of the transient are performed using comparators; thus, AD conversion is not needed.

V. Conclusion

In this study, the OICC concept is extended to the multiphase current controlled buck converter with PCMC. Since the OICC concept is developed for CMC, current sharing is ensured among the phases and the extension to multiphase solution has been performed without significant modifications of the initial system presented in [25].

Furthermore, the OICC subsystem is implemented as a synchronous buck converter with PCMC providing better efficiency than those solutions based on LRs. In this study, the Pk_Avg offset compensation block has been employed and implemented in a simple manner, in order to ensure that the auxiliary current, injected at the output node, has the same value given by the auxiliary current reference voltage.

Regarding the dynamic behavior, a two-phase PCMC buck converter with the OICC ($C_{\mathrm{OUT}} = 140$ μF, $n = 15$) has been designed and compared with a converter which has the same power stage and n times bigger output capacitor ($C_{\mathrm{OUT}} =$ 2.1 mF). They are compared in terms of dynamic behavior under single resistive load step, repetitive load steps, and dynamic efficiency. Both systems exhibit the same dynamic behavior under single resistive load steps of 8.2 A at both simulation and experimental levels, thus implying that the reduction of the output capacitor by a factor 15 can be applied (from 2.1 mF down to 140 μF): the OICC prototype has -30 mV output voltage deviation under positive load step (-380 mV when the OICC is inactive); the second prototype with n times higher capacitance has -35 mV output voltage deviation. Similar results are obtained for the down load step. In addition, the state variables of both systems have the same dynamic behavior. Furthermore, the robustness of the system under repetitive load steps and capacitor current estimator mismatch is experimentally validated. The output voltage peak-to-peak deviation under repetitive load steps is 70 mV for the OICC system (600 mV when the OICC is inactive) and 50 mV for the converter with 15 times higher capacitance. Regarding the capacitor current mismatching, the system has been analyzed and tested for $\pm 30\%$ output capacitor variation. Although the capacitor current measurement deteriorates, the system is robust and the output voltage deviation is nearly the same with respect to the nominal case. Another contribution of this study is that the system efficiency under a pulsating load has been presented and it has been demonstrated that the OICC power losses are dependent on the load step amplitude instead of the absolute averaged output power, which can be used to further optimize the OICC subsystem.

Furthermore, the output capacitor area is reduced. Total output capacitor area of the prototype with the OICC is 92.8 mm^2, including the footprints of the output capacitors and the OICC power stage (inductor, MOSFETs, and driver), while in the case of the converter with n times bigger output capacitor, the area is 200.6 mm^2, considering the footprint of output capacitors. Using discrete technology, a reduction to 46% of the second prototype total area is obtained. Further reduction is expected if the OICC subsystem is integrated. In addition, the reliability of the system is increased, since the prototype with the OICC uses only ceramic capacitors, which have significantly larger lifetime and reliability compared to the OSCON capacitors employed in the prototype with n times bigger capacitor.

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