Impact of the control on the size of the output capacitor in the integration of Buck converters

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***Abstract*—One of the main challenges in PowerSoC converters is the integration of the output capacitor. In some applications, the minimum value of the capacitance is constrained not by the maximum allowed voltage ripple but by dynamic requirements. This paper investigates for a 10 MHz Buck converter if the design of very fast controls can reduce the required output capacitor and which controls are more suitable. It is also analyzed the effect that the moment in which the load transient can occur has on the reduction of the size of the output capacitor.**

***Index Terms*—Optimization, Control of DC/DC converters, Voltage mode, Peak current mode, V2, V2Ic.**

I. Introduction

The size of the output capacitor of Buck converters in point-of-load applications is determined by the static requirements, given by the minimum allowed ripple of the output voltage, and the dynamic requirements, given by the minimum variation of the output voltage during the worst-case load transient.

The control is a crucial part of the design of the converter as a very fast control strategy can reduce the required output capacitor by taking most of the effort of the load transient response. Also, if the load is a microprocessor, dynamic voltage scaling might be required where the converter needs to change the output voltage according to the operation of the microprocessor. In this case, a small output capacitor could lead to an underdamped response of the control, causing the converter to go out of the dynamic specifications.
Consequently, the control plays a major role in the design of the output capacitor.

This paper compares for a $10MHz$ Buck converter different control strategies to study which is the minimum output capacitance that can be reached for each of them that allows the converter to stay within dynamic requirements during the transients.
The studied controls are the Voltage mode, the Peak current mode, V^2 [1] and V^2I_c [2] controls. In order to design the controls that achieve an optimal dynamic behavior and, consequently, to greatly reduce the size of the output capacitor, this paper proposes an optimization algorithm which is based on a large-signal discrete model of the converter and the Floquet theory to assess stability in different cases.

II. Theoretical limits of different modulation strategies

Even an ideal instantaneous control cannot prevent a certain drop of the output voltage [3] which is given by the equation (1) for the loading case and (2) for the unloading case without considering the ESR and the ESL of the output capacitor.

$$\triangle v_{o_{min,loading}} = \frac{1}{C} \cdot \frac{\triangle i_o^2}{2(V_{in} - v_o)} L \tag{1}$$

$$\triangle v_{o_{min,unloading}} = \frac{1}{C} \cdot \frac{\triangle i_o^2}{2v_o} L \tag{2}$$

In (1) and (2), the parameters are the minimum voltage variation during the loading and unloading transient, $\triangle v_{o_{min,loading}}$ and $\triangle v_{o_{min,unloading}}$, the load current transient variation, $\triangle i_o$, the input voltage, V_{in}, the output voltage, $\triangle v_o$, the inductance of the inductor of the filter, L, and the output capacitor C.

Equations (1) and (2) set the minimum required output capacitor for the case of a control that can immediately saturate the duty cycle. However, if constant on-time, constant off-time or constant switching frequency modulations are used, then, the worst-case transient presents a delay where the control is unable to react, greatly increasing the required output capacitor. Hysteretic controls does not present this problem.

In the case of fixed-frequency controls, the worst case is the situation where a positive load step occurs when the off-state begins, as the control is not able to react until the end of the period. Figure 1 shows that, when the converter is perturbed with a positive load step at the beginning of the off-state, the voltage starts to drop with the control unable to react until the beginning of the next period. Consequently, because of the off-state delay, even for an optimal control, a minimum output capacitor is required that is dependent on the power

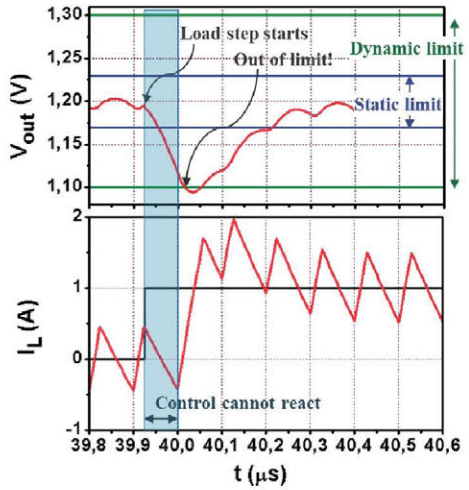


Fig. 1: Dynamic response under worst-case load step of a fixed-frequency control.

stage, the switching frequency and the off-state delay. If the control is fast enough, the dynamic response can be within the required dynamic limit with this minimum output capacitor but, for slower controls, the size of the output capacitor would need to be increased so that the converter meets the dynamic requirements.

In the case of constant T_{on} controls, the worst-case transient is the situation where a negative load step occurs when the on-state begins, as the control is not able to react until the end of the constant on-time. In the case of constant T_{off} controls, the worst-case transient is the situation where a positive load step occurs when the off-state begins, as the control is not able to react until the end of the constant off-time.

For a fixed-frequency control and without considering the ESR and the ESL of the output capacitor, the additional drop of the output voltage due to a time delay because of a positive load step is:

$$\triangle U_{delay} = \frac{1}{C} \triangle i_o t_d \tag{3}$$

where t_d is the time delay and, in the worst case, it is equal to the off-time, $t_{off} = (1 - D)T$, where D is the duty cycle and T is the switching period.

The minimum capacitance required taking into account the time delay is then:

$$C_{min,loading} = \frac{1}{\triangle v_o} \cdot \left(\triangle i_o t_d + \frac{\triangle i_o^2}{2(V_{in} - v_o)} L \right) \tag{4}$$

This equation is only an approximation that does not take into account the ESR and the ESL of the output capacitor but it shows that the delay in the response of the control greatly increases the minimum required size of the output capacitor.

The question arises whether the control is sufficiently fast so that the absolute minimum capacitance is enough to stay within dynamic requirements. If the control is not fast, the size of the output capacitor would need to be increased accordingly. Also, in applications with voltage reference tracking, the control has to respond fast also under voltage reference steps to make sure that the required minimum output capacitor set by the load transient is enough.

III. Comparison of different control strategies

The section compares the Voltage mode (fig.2a), Peak current mode (fig.2b), V^2 [1] (fig.2c) and $V^2 I_c$ [2] (fig.2d) controls with fixed-frequency modulation for an very high-frequency integrated Buck converter. The section is divided in four subsections:

- The subsection A briefly explains how the controls are optimized for a very fast dynamic response with a proposed algorithm. These optimized designs are used in the comparison in order to assure that the controls achieve their optimal response.
- The subsection B compares the optimized dynamic responses of the controls with the minimum output capacitors that meet dynamic requirements in the worst-case transient which, for the fixed-frequency modulation, is when the load transient occurs at the beginning of the off-state.
- The subsection C compares the optimized dynamic responses of the controls with the minimum output capacitors supposing that, because of a synchronization between the load and the power supply, the load transient cannot occur during the off-state and, consequently, the transient response presents no delay.
- The subsection D discusses about the results of the comparison.

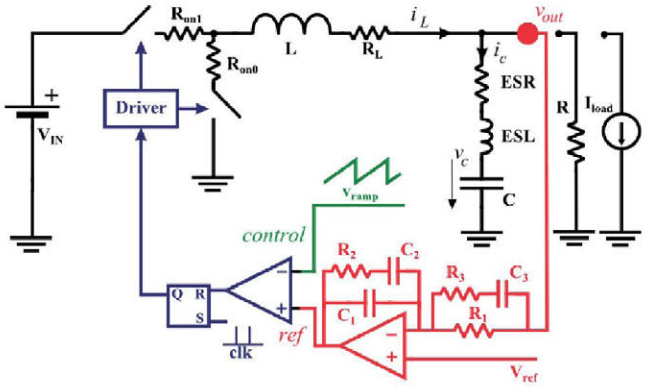
The specifications of the converter are: $F_{sw} = 10MHz$, $V_{in} = 5V$, $v_{out} = 1.2V \div 2.2V$, $I_{out} = 0A \div 1A$, $L = 100nH$. The power stage also includes the on-resistances of the switches (high-side MOSFET: $290m\Omega$, low-side MOSFET: $80m\Omega$) and the ESR of the inductor ($110m\Omega$). The time constant of the capacitor is $C \cdot ESR = 3.5ns$ and the ESL is considered negligible. The static limits and the dynamic limits that the power supply has to comply with are $\pm 5\% V_{out}$ and $\pm 11\% V_{out}$, respectively.

The V^2 control is not shown under voltage reference step because it is significantly slower than the other controls (fig.3).

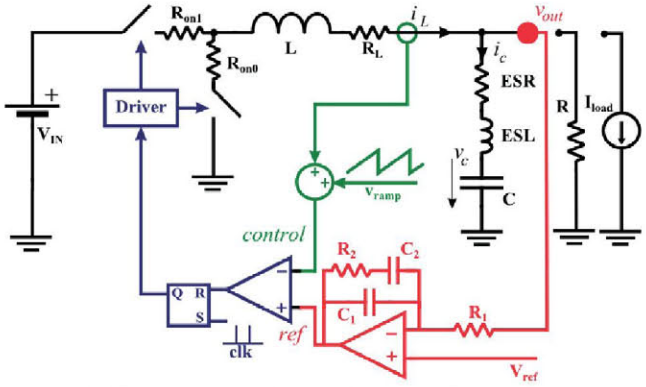
A. Modeling and optimization

The dynamic behavior of power converters can be accurately modeled by means of discrete modeling together with Floquet theory [4]. Not only a discrete model of the form of $x_{k+1} = f(x_k)$ can be derived but the whole time-domain waveform can be reconstructed. The stability of the power converter can be analyzed by means of the Floquet theory which is able to predict the appearances of sub-harmonic oscillations, which are a concern in Peak current mode, V^2 and $V^2 I_c$ control. The major advantages of these techniques are the accuracy, the simplicity of including parasitic elements and the extension of the methodology to other controls.

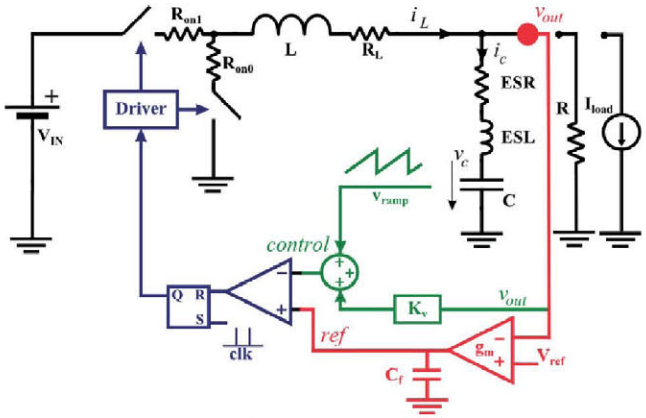
The proposed optimization algorithm uses the computed dynamic behavior of the discrete model and designs the



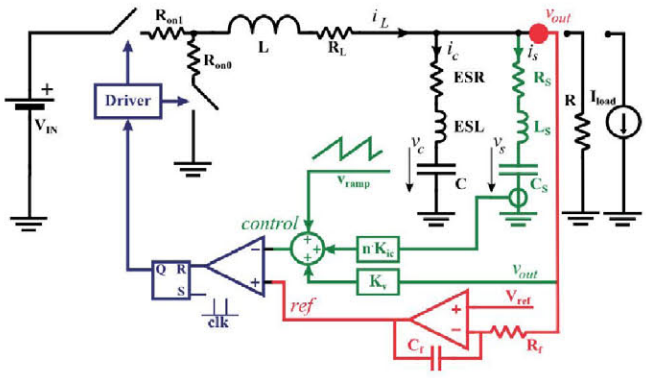
(a) Voltage mode control with type-III controller.



(b) Peak current mode control with type-II controller.



(c) V^2 with type-I controller.



(d) $V^2 I_c$ with type-I controller.

Fig. 2: Schemes of compared controls.

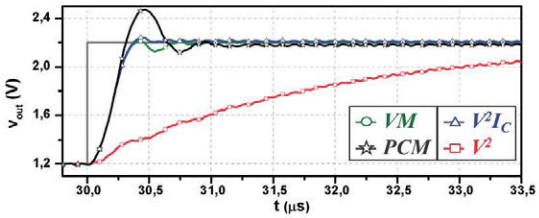


Fig. 3: V^2 control is much slower than the other controls under a voltage reference step.

parameters of the control in order to find out the optimal transient response which is fast and robust.

In order to design robust controls of power converter, not only the dynamic behavior at nominal operation needs to be optimized but the system needs to be stable and within dynamic requirements over all the desired region of operation and under changes in the value of parameters of the power stage due to tolerances. This means that the stability needs to be assessed at different conditions. Also, the values of the passive elements need to be implementable in practice. The optimization process takes into account all these and reject the solutions that do not comply with the requirements.

Each control is designed for the optimal dynamic response using the proposed algorithm. In the comparisons, the optimization algorithm is set to assure stability at a maximum output voltage of $3V$ and to only allow capacitance values greater than $10pF$ in the linear controllers so that the design is implementable analogically in practice.

B. *Worst-case transient*

Figure 4 shows the comparison of the dynamic response under voltage reference step and load step of the Voltage mode, Peak current mode, V^2 and $V^2 I_c$ control for the worst-case transient. In all controls, the minimum size of the output capacitor to comply with the dynamic requirements is the same and has a value of $1.1\mu F$. Note that, in the worst-case transient, the delay time is equal to the off-time, where none of the controls can respond to the load transient until the end of the period. Then, during the next on-state, although the controls try to saturate the duty cycle, they cannot prevent the drop of the output voltage that reaches the dynamic limit. This is why the minimum output capacitance of all controls in this case is $1.1\mu F$, independently of the control.

C. *"No delay" transient*

Figure 5 shows the comparison of the dynamic response under voltage reference step and load step of the Voltage mode, Peak current mode, V^2 and $V^2 I_c$ control supposing that the load transient cannot occur during the off-state due to a synchronization between the load and the power supply and, consequently, there is no time delay. In this case, the minimum size of the output capacitor to stay within dynamic requirements changes. For the case of Voltage mode control, the minimum output capacitor is $700nF$, for the case of Peak current mode is $700nF$, for the case of V^2 is $600nF$ and for the case of $V^2 I_c$ is $320nF$.

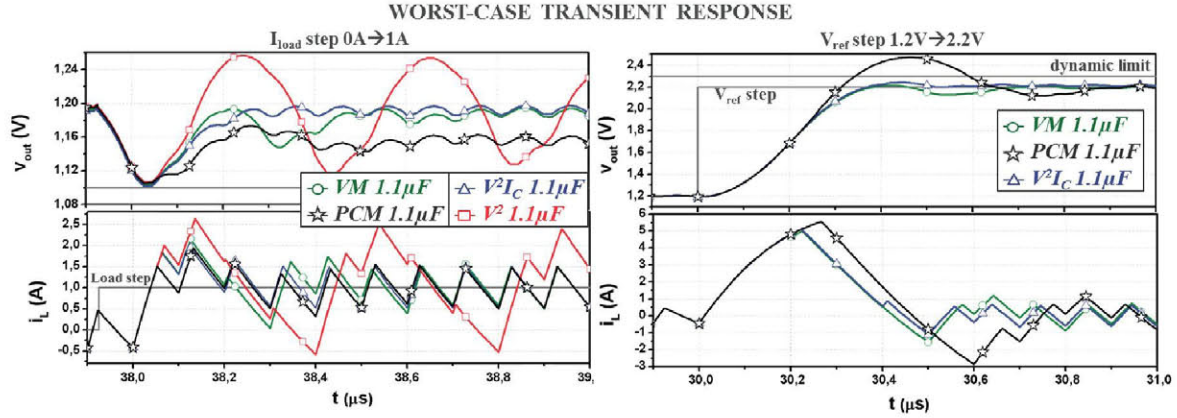


Fig. 4: Dynamic response for the worst-case transient of Voltage mode (VM), Peak current mode (PM), V^2 and $V^2 I_c$ control under a load step $0A \rightarrow 1A$ (left) and voltage reference step $1.2V \rightarrow 2.2V$ (right).

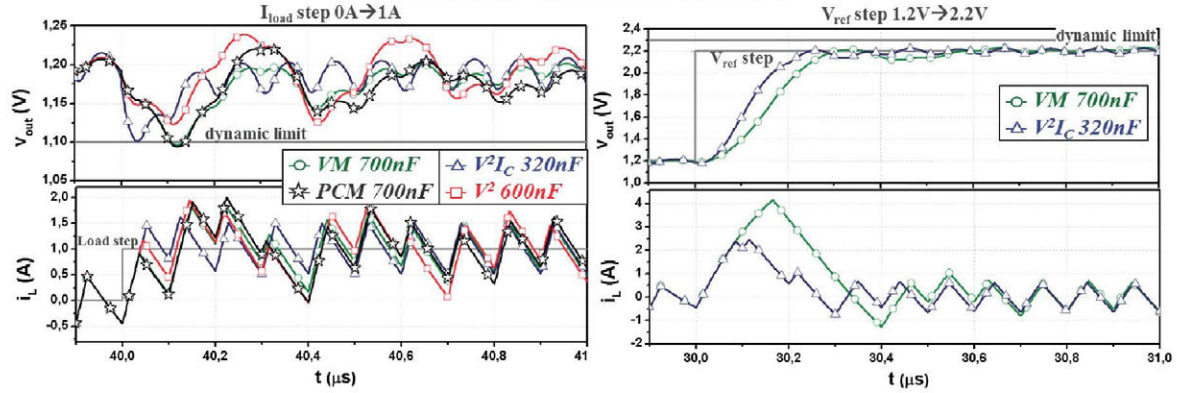


Fig. 5: Dynamic response for the "no delay" transient of Voltage mode (VM), Peak current mode (PM), V^2 and $V^2 I_c$ control under a load step $0A \rightarrow 1A$ (left) and voltage reference step $1.2V \rightarrow 2.2V$ (right).

D. Discussion

First, note in the voltage reference step of the Voltage mode control of figures 4 and 5 that the control, which was designed with the proposed optimization algorithm, fully saturates the duty cycle to on-state and then to off-state to reach the steady state without overshooting. This transient response is very similar to the Minimum Time control transient which is implemented digitally and achieves the fastest settling time possible for the power stage [5, 6]. This shows that the controls of the comparisons are truly optimized for a very fast dynamic response.

The evaluation of the comparison is as follows:

- Voltage mode control achieves very good results for the case of the worst-case transient, reaching the steady-state under voltage reference step in three cycles without overshooting and quickly recovering from the drop of the output voltage under the load step. For the case of the "no delay" transient, the minimum required output capacitor is $700nF$, and the performance under the voltage reference step is very good but under load step, the output voltage oscillates before the steady-state is reached.
- Peak current mode achieves in the worst-case transient a fast dynamic performance under voltage reference step but there is an overshoot of the output voltage of around 13%, which is out of the dynamic limit. The output voltage drops a lot under the load step and, furthermore, the converter converges very slowly to the steady-state. The needed output capacitance for the "no delay" transient is $700nF$, the dynamic response for this case under load step presents some oscillations that attenuate over time. The dynamic response for the voltage reference step is not shown for this case because it is very oscillatory.
- V^2 is not appropriate for voltage reference tracking (fig.3). Under load step, for the worst-case transient, the control reacts fast but quickly enters an oscillating state that attenuates very slowly. For the case of the "no delay" transient, the minimum output capacitor is $600nF$. Although, the figure 5 shows that the output voltage has not yet reached the dynamic limit for the loading transient, actually, it reaches it in the unloading transient, although this is not shown. The response under load step with $600nF$ is oscillatory and attenuates more slowly than other controls.

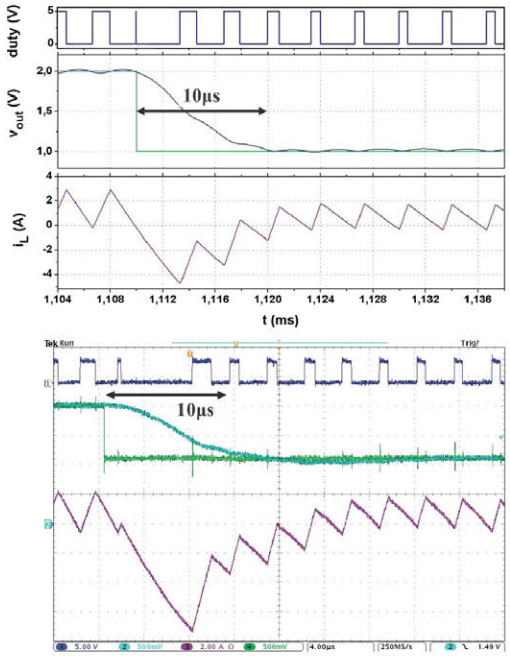


Fig. 6: Comparison between simulation results (upper figure) and experimental results (lower figure). Experimental transient response under voltage reference step $2V \rightarrow 1V$ of a 300kHz Buck converter with Voltage mode control. Experimental results: output voltage in light blue ($500mV/div$), reference voltage in green ($500mV/div$), inductor current in purple ($2A/div$) and duty cycle in dark blue ($5V/div$) with $500\mu s/div$ time scale.

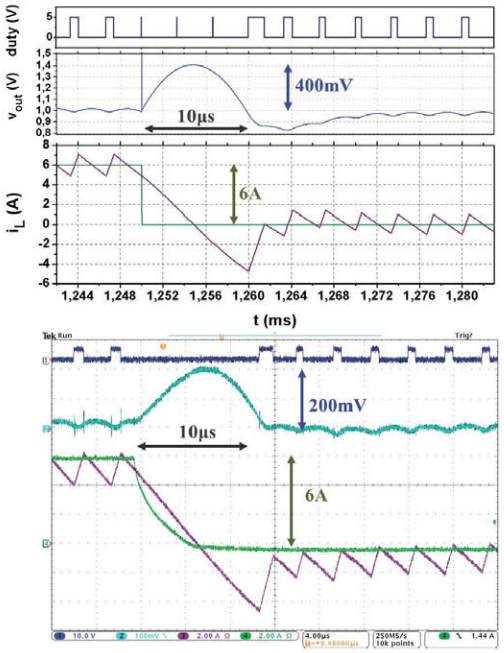


Fig. 7: Comparison between simulation results (upper figure) and experimental results (lower figure). Experimental transient response under load step $6A \rightarrow 0A$ of a 300kHz Buck converter with Voltage mode control. Experimental results: output voltage in light blue ($100mV/div$ (AC)), reference voltage in green ($500mV/div$), inductor current in purple ($2A/div$) and duty cycle in dark blue ($10V/div$) with $500\mu s/div$ time scale.

As seen, a good transient response cannot be reached with V^2 control with a low ESR capacitor. In order to improve the dynamic response, current information has to be added to the fast loop. The current information can be the inductor current, what is known as V^2 with hybrid ramp compensation [7], or the current through the output capacitor, what is then known as $V^2 I_c$ control.

- $V^2 I_c$ achieves a very good response for the worst-case transient. The dynamic under voltage reference step is the same as the Voltage mode control. Under load step, $V^2 I_c$ is the fastest in reach the steady-state and does not oscillates. For the case of the "no delay" transient, the minimum output capacitor is $320nF$ which is a reduction of approximately a 50% of the size when compared with the other controls. Moreover, the output voltage reaches steady state under voltage reference steps in two clock cycles and the dynamic behavior under load steps is the fastest even-though the size of the output capacitor is lower.

IV. Experimental Results

This section validates the optimized designs of a Voltage mode and $V^2 I_c$ of a $300kHz$ Buck converter to demonstrate that the designs of the proposed optimization algorithm that is used in the comparisons are feasible. The Buck converter has the following specifications: $F_{sw} = 300kHz$, $V_{in} = 5V$, $v_{out} = 1V \div 2V$, $I_{out} = 0A \div 8A$, $C = 30\mu F$, $L = 1.3\mu H$. The power stage also includes the ESR ($4m\Omega$) and ESL

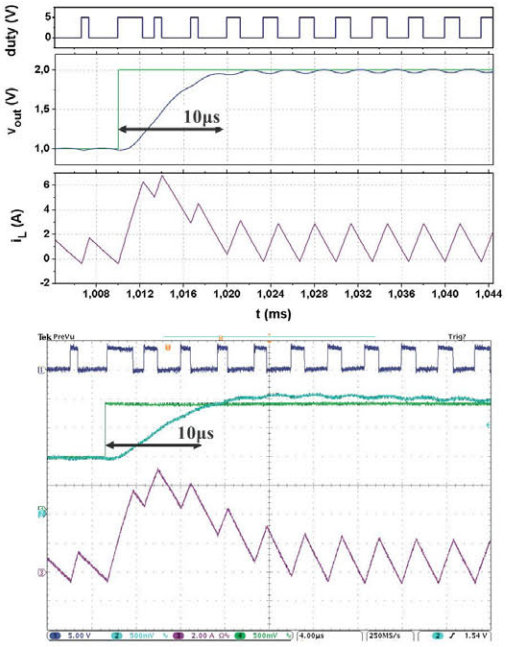


Fig. 8: Comparison between simulation results (upper figure) and experimental results (lower figure). Experimental transient response under voltage reference step $1V \rightarrow 2V$ of a 300kHz Buck converter with $V^2 I_c$ control. Experimental results: output voltage in light blue ($500mV/div$), reference voltage in green ($500mV/div$), inductor current in purple ($2A/div$) and duty cycle in dark blue ($5V/div$) with $500\mu s/div$ time scale.

TABLE I: Summary of the comparison for the $10MHz$ Buck converter.

	WORST-CASE TRANSIENT			NO DELAY TRANSIENT		
CONTROL	**Minimum C_{out}**	**Voltage reference tracking**	**Load step**	**Minimum C_{out}**	**Voltage reference tracking**	**Load step step**
VM	$1.1\mu F$	excellent	good	$700nF$	excellent	medium
PCM	$1.1\mu F$	fast but overshoots	medium	$700nF$	very bad	medium
V^2	$1.1\mu F$	very bad	bad	$600nF$	very bad	medium
V^2I_c	$1.1\mu F$	excellent	excellent	$320nF$	excellent	excellent

($600pH$) of the output capacitor, the on-resistances of the switches ($30m\Omega$ for the high-side MOSFET and $14.2m\Omega$ for the low-side MOSFET) and the ESR of the inductor ($15m\Omega$). Each control is designed for the best dynamic response possible using the proposed optimization algorithm. The optimization algorithm is set to assure stability at a maximum of $4V$ of output voltage, under output current range from $0A$ up to $10A$ and under 100% variations of the nominal ESL and limiting the capacitance value of the linear controller so it must be higher than $10pF$ to guarantee that the design is implementable in practice.

Figure 6 and 7 show the experimental validation of the Voltage mode control. The figure shows the transient response under a negative voltage reference step from $2V$ to $1V$ and a negative load step from $6A$ to $0A$. The converter is able to react within three clock cycles both in simulation results and in the experimental prototype, validating that the Voltage mode control designed with the proposed optimization methodology can be implemented in practice and achieves very fast transient responses.

Figure 8 shows the experimental validation of the Voltage mode control. The figure shows the transient response under a positive voltage reference step from $1V$ to $2V$. The converter is able to react within three clock cycles both in simulation results and in the experimental prototype, validating the V^2I_c design that the optimization algorithm yields.

V. Conclusions

The design of a very fast control can reduce the required output capacitor to improve the dynamic response under load transients. An optimization algorithm is proposed in order to design fast and robust controls to achieve the greatest reduction of the output capacitor. The tested prototypes with a Voltage mode and V^2I_c control manage to reach steady state under voltage reference steps and load steps in three clock cycles without overshooting, validating experimentally that the optimized designs are very fast and feasible.

The optimization algorithm is used to study and compare the reduction of the output capacitor that can be reached with the control techniques Voltage mode, Peak current mode, V^2 and V^2I_c. The results (table I) yield that, when the response of the control presents no delay, V^2I_c manages a reduction of a 50% more of the size of the output capacitor when compared with the other controls, while still performing excellent in the transient responses. Voltage mode, Peak current mode and V^2 manage a similar reduction in the size of the output capacitor but Voltage mode performs better in the transient responses. If the worst-case load transient is allowed, then the minimum required size of the output capacitor is the same for all the controls as they are unable to respond during the off-time if the worst-case load transient occurs. For this case, Voltage mode control and V^2I_c perform better.

The results also yield that, when optimized, both Voltage mode and V^2I_c can be used in voltage reference tracking applications achieving an excellent performance.

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