Material requirements for the adoption of unconventional silicon crystal and wafer growth techniques for high-efficiency solar cells

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Abstract:

Silicon wafers comprise approximately 40% of crystalline silicon module cost, and represent an area of great technological innovation potential. Paradoxically, unconventional wafer-growth techniques have thus far failed to displace multicrystalline and Czochralski silicon, despite four decades of innovation. One of the shortcomings of most unconventional materials has been a persistent carrier lifetime deficit in comparison to established wafer technologies, which limits the device efficiency potential. In this perspective article, we review a defect-management framework that has proven successful in enabling millisecond lifetimes in kerfless and cast materials. Control of dislocations and slowly diffusing metal point defects during growth, coupled to effective control of fast-diffusing species during cell processing, is critical to enable high cell efficiencies. To accelerate the pace of novel wafer development, we discuss approaches to rapidly evaluate the device efficiency potential of unconventional wafers from injection-dependent lifetime measurements.

Keywords: silicon; lifetime; silicon solar cell; crystal and wafer growth techniques; defects

I. Introduction:

To sustainably reduce the cost of crystalline silicon (c-Si) photovoltaics (PV) through technological innovation, two often-contradictory goals must be achieved: Reduce wafer substrate cost, and increase material performance. The latter goal is achieved by improving "quality", *i.e.*, bulk minority-carrier lifetime. The former is achieved primarily by improving "rate", *i.e.*, increasing throughput, reducing cost of tool ownership, reducing the amount of Si feedstock per wafer by reducing wafer thickness and/or kerf losses. Achieving both simultaneously, in a potentially disruptive crystal growth process, has proven challenging. During the last fifteen years, no new c-Si crystal growth technology achieved a lasting foothold in the PV market to supplant ever-improving Czochralski monocrystalline silicon (Cz-Si) and cast multicrystalline silicon (mc-

Si). But the economic motivation to explore alternative growth methods remains, as wafer production costs comprise approximately 40% of module manufacturing costs [1][2], and reducing absorber cost is essential to ensuring the long-term competitiveness of c-Si in the face of steadily increasing thin-film module efficiencies [3].

Herein, we describe a path to improve the material performance of unconventional c-Si crystal growth technologies. We first roughly outline the defect mitigation strategy that has enabled homogeneous millisecond lifetimes in two promising growth techniques: kerfless epitaxial (epi) silicon and ingot non-contact crucible silicon (NOC-Si). At the example of the epi-Si technology, we then present an approach to use injection-dependent bulk lifetime measurements to estimate a wafer's efficiency entitlement in a given device architecture. We describe this approach for three different levels of complexity, first assuming injection-independent lifetimes, secondly, assuming injection-dependent lifetimes, and thirdly, assuming a different injection dependence of lifetime for different point defects with varying capture cross-sections and energy levels.

II. Overview of unconventional crystal growth techniques

Several unconventional wafer fabrication methods, which are reviewed in the next paragraphs, have been proposed as alternatives to Cz-Si and mc-Si. These include unconventional ingot, vertical ribbon, horizontal ribbon, and chemical vapor growth methods [4].

II.A. Taxonomy of unconventional wafer fabrication methods

Unconventional ingot growth methods are typically variants of directional ingot solidification, targeting improved throughput and material quality. For example, electromagnetic cold crucible (EMC, [5]) and non-contact crucible (NOC-Si, [6]) methods aim to limit impurity concentrations in the ingot by reducing contact with the crucible during growth. The former employs a continuous recharge, which is also present in continuous Czochralski (CCZ, [7][8][9]. Seeded casting methods, *e.g.*, by thick Cz wafers [10] or self-forming dendrites [11], aim to control grain size and orientation, thus reducing recombination-active grain boundaries and facilitating texturization. It was inspired by these innovations that high-performance multi was developed [12] by seeding with crushed Siemens-grade poly-Si, reducing grain size and intragranular dislocation density.

Non-ingot growth technologies aim to avoid wire-sawing losses and reduce processing steps by growing ribbons or discrete wafers from melt or gas phase. Examples of vertical ribbon growth include dendritic web (DDW), edge-defined film-fed growth (EFG), string ribbon (SR), ribbon-to-ribbon (RTR), and ribbon-against-drop (RAD) [4]. Horizontal ribbon growth aimed to decouple the crystal growth and solidification vectors, targeting accelerated throughputs; examples include low-angle silicon sheet (LASS), Wacker interface-controlled crystallization (ICC), ribbon growth on substrate (RGS), and AstroPower SiliconFilm [4][13]. Chemical vapor deposition methods grow wafers directly from gaseous silicon, typically epitaxially on partially recrystallized porous

silicon layers [14], with the benefit of avoiding the costly Siemens process and energy-intensive silicon melting.

II.B. Adoption requirements for unconventional wafer fabrication methods

Several unconventional wafer approaches were piloted or commercialized in industry, but none has yet sustained widespread market adoption. A combination of multidisciplinary technical and economic trade-offs is likely responsible. Unconventional methods that focus on reducing kerf loss without other obvious benefits have limited appeal during periods of declining silicon feedstock prices. Methods that focus on increasing throughput (and thereby reducing $\$/m^2$) are prone to sacrificing quality, with lower bulk lifetimes caused by increased structural defect densities resulting from large thermal gradients during growth. The reduction in material quality impacts cell efficiency, which is kept lower than that achieved by industry-standard Cz-Si and mc-Si; ribbon c-Si solar cell efficiencies, for example, have plateaued at ~18% with sophisticated laboratory-scale processing [15] [16], while staying in the 13–16% range at the industrial level [17][18][19][20][21][22][23]. Thus, the throughput-efficiency trade-off of these alternative methods has turned out unfavorable so far because the efficiency cost penalty is severe [3], resulting in higher \$/W.

The establishment of the material requirements that unconventional wafers must fulfill to compete with the incumbent technologies necessitates approaches to manage defect densities, from growth to processing, a clear vision for bulk lifetime targets as a function of device architecture, and a sufficient understanding of the device impacts of bulk defects, aspects that are addressed in the following sections.

III: Millisecond lifetimes in unconventional wafers enabled by defect management

III.A. The emergence of unconventional wafer technologies with millisecond lifetime

Two types of unconventional growth techniques have demonstrated recently to result in wafers that meet the high material-quality targets and are therefore well-suited for high-efficiency cell concepts: epitaxial silicon (epi-Si) wafers and wafers from an ingot grown by a non-contact crucible (NOC-Si) casting method.

Effective lifetimes >300 µs were demonstrated in *p*-type epi-Si wafers with 1.79 Ω-cm resistivity after standard P diffusion gettering (PDG) with a bulk lifetime estimate of >1 ms [24]. Even higher effective lifetimes >2 ms were measured in the latest generation of *n*-type epi-Si wafers [25]. These epi-Si wafers are single crystalline and upon defect Sopori etching [26], a low average density of structural defects $<10^4$ cm^{-2} is revealed. Pairs or quadruples of perpendicularly arranged stacking faults, some of which are surrounded by a high density of dislocations (locally $>10^6$ cm^{-2}) are the dominant performance-limiting defect complex in a density on the order of ~1 cm^{-2}. The high

material quality recently achieved by these epi-Si wafers has resulted in a solar cell conversion efficiency of 22.3% for heterojunction type devices made from 150 μm thick *n*-type epi-Si wafers [25]. A major advantage of epi-Si wafers over wafers that are sawn from an ingot is that there is no lower thickness limit and thus very thin wafers can be grown, bearing a potential for higher efficiencies in certain device architectures. A practical demonstration is the achievement of an efficiency of 21.2% in devices made from 35 μm thick epi-Si wafers [27].

In *n*-type wafers sawn from a NOC-Si ingot, effective lifetimes of around 150 μs have been measured in the as-grown state, and effective lifetimes of 750 μs and 1.5 ms have been demonstrated after standard and after extended PDG, respectively [28]. The dominant defect type in the material is a swirl-defect, also observed in Cz ingots and likely caused by thermal gradients during crystal growth. Apart from the swirl defect, a low overall dislocation density $<10^3$ cm^{-2} has been observed in NOC material, leaving potential to achieve high efficiency devices [29].

III.B: Defect management approach enabling millisecond lifetimes

The high demonstrated minority carrier lifetimes that enable high conversion efficiencies in both epi- and NOC-Si materials have been achieved through a systematic defect monitoring and management approach. A simplified version of this approach is outlined in *Figure 1*.

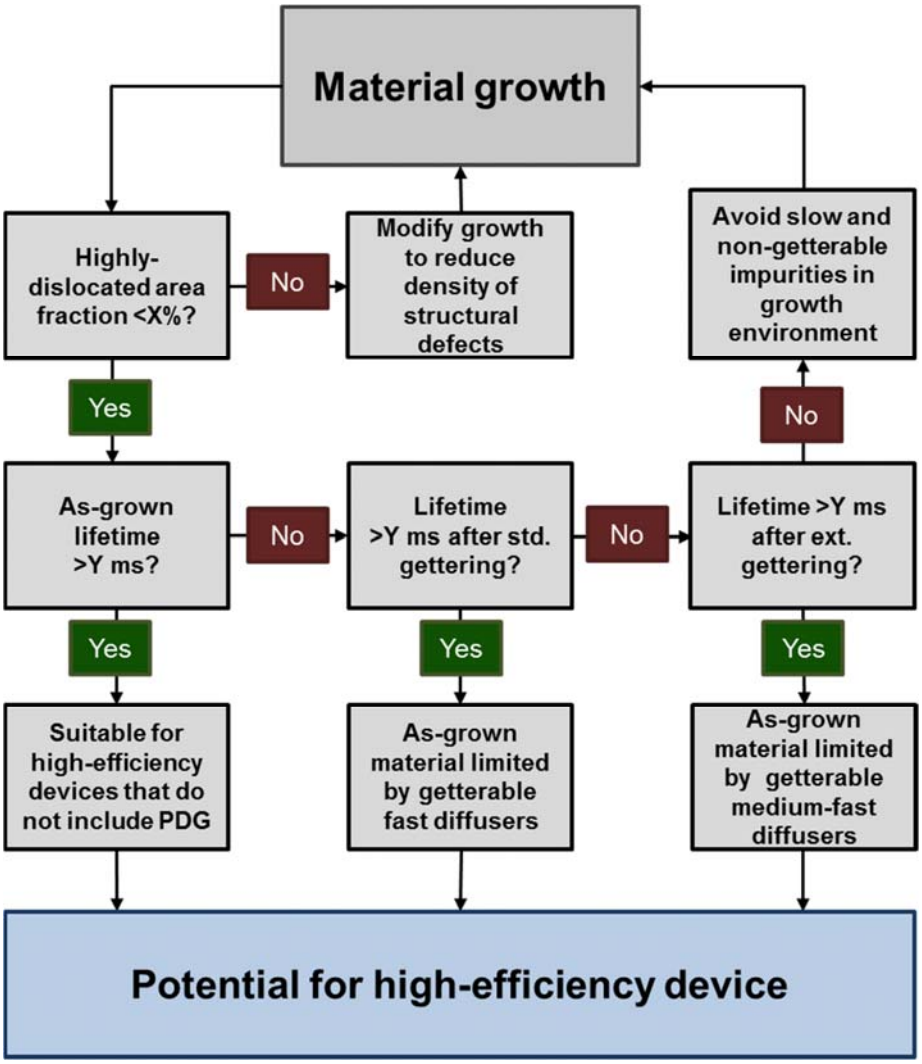

Figure 1: Simplified systematic approach to determine and manage performance-limiting defects in silicon materials from unconventional growth technologies. X and Y are variables whose value will depend on the performance target that is set for a particular material, following the guidelines of section IV.

The density of structural defects present in the as-grown material is one of the most important metrics to be tested early on. It can hardly be modified during the subsequent solar cell process and may therefore set an upper limit on the minority carrier lifetime and corresponding device efficiency. Areas of high dislocation density have been demonstrated to limit performance in standard mc-Si and in ribbon Si [30][31]. If the area fraction containing a high density of recombination-active structural defects is above a certain threshold "*X*", it may inhibit achieving the average bulk minority carrier lifetime necessary to support the aspired solar cell efficiency, and ways of reducing the structural defect density during growth will need to be investigated. For

example, calculations using Donolato's model [32] indicate that dislocation densities $<10^4$ cm^{-2} are required to support minority carrier lifetimes > 1 ms.

The bulk minority carrier lifetime in the as-grown silicon wafer is another important metric to be measured, benchmarking with a threshold value of "*Y*" ms. If the as-grown bulk lifetime is already above that threshold, the as-grown material is suitable to support the highest efficiencies in device architectures that do not include a PDG step (e.g. heterojunction devices). In fact, it may be advisable to avoid high-temperature steps during subsequent solar cell processing since the in-diffusion of fast-diffusing impurities may otherwise lead to material degradation. The formation of thermal donors that can occur in a medium temperature range of 450 – 600ºC may have to be taken into consideration as well [33].

If the as-grown bulk lifetime is too low to support high-efficiency devices, a standard PDG step can potentially improve material performance. A standard PDG step is defined as the typical emitter formation step that is applied in industry nowadays. It usually consists of a 10 – 30 min high-temperature step between 800 and 900°C, during which a phospho-silicate glass (PSG) layer forms from which P diffuses into the silicon wafer. Subsequently, wafers are removed from the furnace at relatively high temperatures >700°C. Gettering efficacy strongly depends on the chosen time-temperature profile, and usually increases with decreasing sheet resistance [34].

Bulk lifetime after standard PDG is the next metric to consider. If lifetime increases importantly during standard PDG, lifetime in the as-grown wafer is likely dominated by getterable medium- and fast-diffusing metal impurities (*e.g.* Cu, Ni, Co, Fe, Cr, Mn) at concentrations that are low enough to be effectively removed during the chosen process conditions. In a recent contribution we have shown that in conventional ingot-based mc-Si, a 25 min standard PDG at 845°C followed by pull-out at 845°C effectively decreases the concentration of detrimental iron interstitials, Fe_i, if the total iron concentration is $<10^{14}$ cm^{-3} in a 160 μm thick as-grown wafers [35]. Note that the gettering efficacy decreases with increasing wafer thickness [36].

In the case of mc-Si materials in which recombination at grain boundaries dominates, a hydrogenation step may have to be applied after PDG to effectively passivate these defects. [37][38][39]. If the bulk lifetime after standard gettering remains too low to support high device performance, an extended PDG step can be applied that may consist of the standard high-temperature P diffusion plateau followed by either a slow cool down (< 5°C/min), or a low-temperature anneal (LTA). The annealing time and temperature need to be adapted for the effective gettering of the metal point defect that is likely to dominate the post-gettering material performance [40].

Bulk lifetime after extended PDG has been demonstrated to improve significantly over lifetime after standard PDG if large concentrations of medium- and fast-diffusing metal impurities are present in the material, e.g., in form of precipitates [41][42][43][44]. Metal precipitates dissolve during the high-temperature step, resulting in high point defect concentrations of these impurities

after standard gettering, which can be removed during the extended thermal annealing. In contrast to medium- and fast-diffusing metal impurities, the diffusivity of phosphorus is significantly lower at temperatures <800°C so that a slow cool-down or even a low temperature annealing step below 800°C hardly alters the desired sheet resistance.

In the case that neither standard nor extended PDG lead to sufficiently high bulk lifetimes, and the density of structural defects is low, the material performance is likely limited by either non-getterable impurities, impurity complexes (*e.g.* B-O), or by slowly-diffusing metal impurities (*e.g.*, Ti, V, Zn, Pt, Au). The lifetime-limiting defect may then have to be determined through advanced defect-characterization techniques suitable for the detection of low defect concentrations on the order of ppb (*e.g.*, lifetime spectroscopy [45] or deep level transient spectroscopy (DLTS) [46]) so that growth conditions can be adjusted to avoid or reduce its introduction into the material.

It has to be noted that the analysis should incorporate the impact of subsequent high temperature processes, in particular that of the contact firing when part of the solar cell process. A thorough review of the influence of thermal steps during solar cell processing, at the example of iron and for different structural defect scenarios in the material, can be found in [47].

IV. Lifetime requirements for high-efficiency solar cells

IV.A. Simplified efficiency-lifetime relationship

To test the implications of bulk material quality on device efficiency, we simulate different solar cell architectures for varying Shockley-Read-Hall (SRH) lifetimes in the Si bulk material, assuming equal lifetimes for electrons and holes. SRH lifetime is varied from 1 μs to 5 ms and the resulting device efficiency is extracted as output parameter.

Four different cell architectures are simulated. First, we consider a "standard BSF" cell with a full-area Al back surface field (BSF) and a phosphorus emitter diffused from a PSG source. Second, a "Passivated Emitter and Rear Cell" or "PERC" with local BSF and improved phosphorus-diffused front emitter is simulated. Assumptions about emitter and BSF properties are described in [48][49]. The profile for the local BSF is taken from [50], the surface recombination velocity under the rear contacts is 10^7 cm/s, and the one at the silicon–dielectric interface is assumed to be 10 cm/s, a value which has been experimentally realized with Al_2O_3, see for example [51].

Third, a "GaP/Si" cell is simulated with the same rear side as the PERC, and with an *n*-type hetero-emitter at the front side which is made of gallium phosphide [49]. This hetero-emitter allows electrons from the Si bulk material to enter the front contact but it blocks the holes (minority carrier in *n*-type GaP) due to a high valence band offset. Even if practical high efficiency devices with this structure have not yet been demonstrated, we present it as an advanced cell architecture that can be industrially viable in the near future, representing at the same time a realistic scenario, that builds on the experience of rear passivation in PERC structures and carrier selective contacts in hetero-junction designs.

The three cell architectures are simulated for 180 µm thick Si wafers. The fourth structure is again the "GaP/Si" cell but assuming an 80 µm thick Si absorber. All cell architectures are simulated assuming a 1.79 Ω-cm boron doped *p*-type substrate.

The solar cell devices are simulated at 1 sun and 300 K, using the software Sentaurus Device [52]. Further details of the simulation input parameters and used models are given in references [49][53][54][55]. The optical generation is calculated with the software Opal Version 2.6 [56] assuming random upright pyramids. For the GaP/Si cell, a 10 nm thin GaP layer on top of the textured silicon is assumed. The resulting *I-V* curves are corrected for metal shading and resistive losses in the metallization (which include three busbars), as typically experienced in 15.6 × 15.6 cm^2 solar cells.

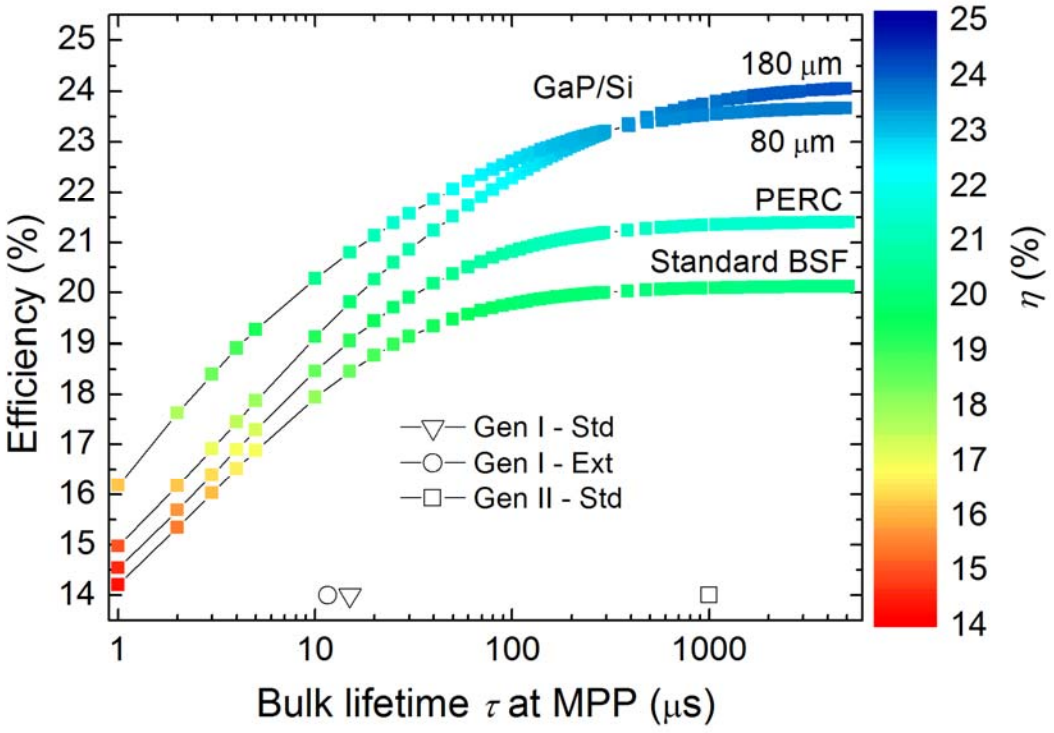

Figure 2: Efficiency as a function of the bulk lifetime at the maximum power point (MPP) during solar cell operation for four different device architectures. Color coding is added corresponding to the y-axis for easier comparison with simulations in Figure 3. Black open symbols are bulk lifetime values at an injection level of 2×10^{15} cm^{-3} measured in two different generations of epi-Si wafers after standard and after extended P diffusion gettering.

The simulated efficiency as a function of the bulk lifetime at MPP for the four device architectures is shown in Figure 2. Two regions can be distinguished: in the low lifetime range efficiency is very sensitive to lifetime and steeply increases with increasing lifetime, an indication that bulk material quality is limiting cell performance; above a certain threshold lifetime value, which is different for

each cell architecture, cell efficiency saturates and bulk material quality is no longer the limiting factor. The threshold lifetime is highest in the case of the GaP/Si cells, and lowest in the case of the standard BSF cells. A more detailed discussion can be found in [55].

To take advantage of the full potential of the different device architectures, bulk lifetimes in the high range in Figure 2 are required. However, the efficiency goal and the corresponding lifetime target need to be evaluated in a profitability study, individually for each material and device architecture, and accounting for the areal cost of the material produced. Hence, *X* and *Y* variables from Figure 1 depend on such specific evaluations.

Also plotted in Figure 2 are the bulk lifetime values on two generations of *p*-type epi-Si wafers, Gen I and Gen II, with resistivities of 0.5 and 1.79 Ω-cm, respectively. Bulk lifetime is estimated from effective lifetime measured on AlO_x-passivated samples with Quasi Steady-State Photoconductance (QSSPC) [57] (details on the measurements can be found in [24]), and reported in the figure for an injection level of 2×10^{15} cm^{-3}. As mentioned in section III.A, low structural defect densities have been demonstrated in these epi-Si wafers that should be able to support highest conversion efficiencies. However, low as-grown bulk lifetimes below 1 μs (not shown in the figure) have been measured in both generations of the material, which are therefore likely limited by impurities. After standard PDG, the bulk lifetime in Gen I material increases up to 15 μs (open triangle), indicating that getterable fast- and medium-diffusing impurities are contributing to low as-grown lifetimes, and that these can be at least partly removed during standard PDG. An extended PDG optimized for the removal of iron interstitials does not further improve the lifetime on Gen I material (open circle) as compared to the standard PDG.

As mentioned in section III.B, the insufficient gettering response in Gen I material to both standard and extended PDG indicates the presence of non-getterable or slowly-diffusing impurities or impurity complexes in Gen I material. Therefore, the growth environment of the epi-Si wafers was carefully examined and potential sources of these possible contaminants were reduced or removed.

Epi-Si wafers grown in the modified growth environment (Gen II) still exhibit equally low lifetimes in the as-grown state, but a bulk lifetime up to 1 ms is measured after standard PDG (open square in Figure 2). Similar to Gen I material, an extended PDG does not improve the gettering response any further (not shown in this case because it overlaps with the lifetime value after standard PDG), indicating again that un-getterable or slowly-diffusing impurities are still limiting the lifetime in Gen II material after gettering, but apparently at lower concentrations.

Nevertheless the achievement of bulk carrier lifetimes of up to 1 ms have been demonstrated in epi-Si wafers, mainly due to the reduction of potential impurity sources from the growth environment, and low average structural density upon growth. It has to be noted that the lifetime curves have been measured with the Sinton tool, with the measurement coil roughly covering an area of 1-2 inches in diameter, and we have checked that the material is fairly homogeneous over the wafer area.

IV.B. Efficiency-lifetime relationship considering injection-dependent lifetimes

Bulk lifetime values are often reported at a specific and somewhat arbitrarily-chosen injection level. That is the case, for instance, of the epi-Si lifetimes given in Figure 2, for which an injection level of 2×10^{15} $cm^{-3}$was selected. The injection level that is reached at MPP during solar cell operation, however, may be very different and is usually much lower. Therefore, to calculate the expected efficiency for a given material, the lifetime value at the correct injection level has to be assumed [58]. To elucidate this point, we plot in Figure 3 the same data as in Figure 2, but with a different representation to include the corresponding excess carrier density Δn (i.e., the injection level). The bulk lifetime at the MPP is plotted as a function of the excess carrier density at the MPP for the four different cell architectures. The color coding corresponds to the efficiency achieved for the given lifetime-injection level pair at the MPP for the respective device architecture (same color coding than in Figure 2). In a device structure with standard BSF, average excess carrier densities at the MPP increase from 4×10^{12} to 3×10^{13} cm^{-3} with increasing bulk lifetime, and a maximum efficiency of 20.1% is simulated for 5 ms bulk lifetime. In a PERC-type device, slightly higher average excess carrier densities between 4×10^{12} and 5×10^{13} cm^{-3} are simulated at the MPP, and a maximum efficiency of 21.4% is calculated. For a GaP/Si heterojunction device with 180 μm thick Si absorber, a steeper increase of average excess carrier densities from 4×10^{12} to 3×10^{14} cm^{-3} is obtained with increasing bulk lifetime, and the maximum efficiency is 24.1%. With a thinner Si absorber of 80 μm thickness, average excess carrier densities and device efficiencies are higher than in the case of the 180 μm thick device for bulk lifetimes up to ~300 μs. Above this lifetime threshold, slightly lower efficiencies are reached due to the decreased light absorption in the thinner substrate. The effect of the substrate thickness on the excess carrier density and on the different device parameters is discussed in detail in [59].

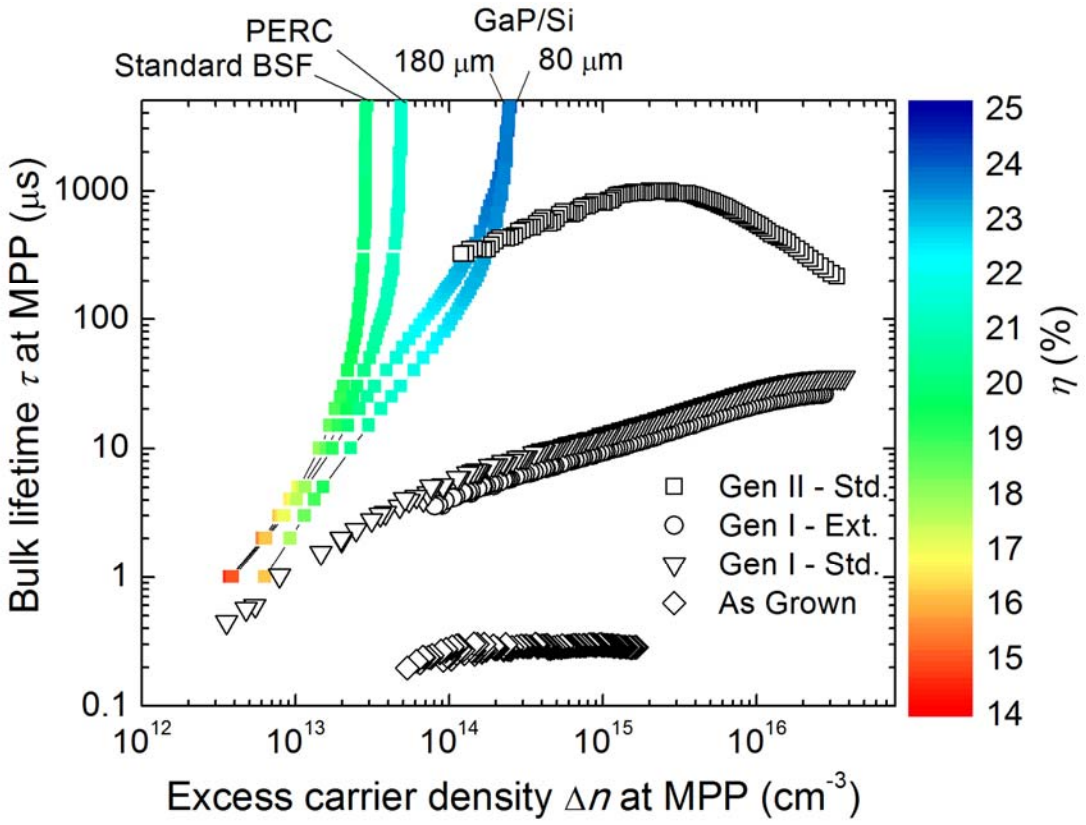

Figure 3: Colored curves show simulated bulk lifetime at the maximum power point (MPP) as a function of the excess carrier density at the MPP for four different device architectures. The color code indicates device efficiency. Black open symbols are measured bulk lifetime curve as a function of excess carrier density in two different generations of epi-Si wafers in the as-grown state, after standard, and after extended P diffusion gettering.

Plotted in Figure 3 are also the injection-dependent bulk lifetime curves measured on Gen I and Gen II *p*-type epi-Si wafers. From the cross-over point between the simulated curves at the MPP and the measured injection-dependent lifetime curves, the efficiency potential of the respective material can be read. For example, lifetimes measured in gettered Gen I material would result in device efficiencies below 16% for all the cell architectures. Note that these calculated efficiencies for Gen I material extracted from Figure 3 are lower than those deduced from Figure 2, as the injection level at the MPP is much lower than the value of 2×10^{15} cm^{-3} for which the lifetimes in Figure 2 were reported.

On the other hand, it can be seen that efficiencies ≥23% can be supported in GaP/Si heterojunction devices made from gettered Gen II *p*-type epi-Si wafers. An extension of the measured lifetime curves into the lower-injection regime (not shown) suggests that the highest possible efficiencies in standard BSF and PERC type devices can also be supported with gettered Gen II *p*-type epi-Si wafers.

IV.C. Efficiency-lifetime relationship considering different injection dependence for different point defects

The use of the injection-dependent lifetime curves as predictors for cell efficiency, as shown in Figure 3, has certain limitations. The assumptions behind the device simulations are elucidated in this section, in particular those related to the type of defects limiting the SRH lifetime.

The first assumption in Figure 3 is that the excess carrier density Δn is spatially invariant. Because Δn is known to vary throughout the device cross section, we make the following approximation: An average Δn is computed by *Sentaurus Device* at MPP spanning the entire thickness of the cell, but excluding the 5 µm nearest the front and rear surfaces (where varying net dopant concentrations and current crowding often cause large local spatial variations in Δn). In Figure 4 we show the spatial variation of Δn at the maximum power point for the different device architectures considered. We observe that Δn varies approximately by only a factor of 2 throughout the bulk of each device, justifying our assumption of spatially invariant excess carrier density.

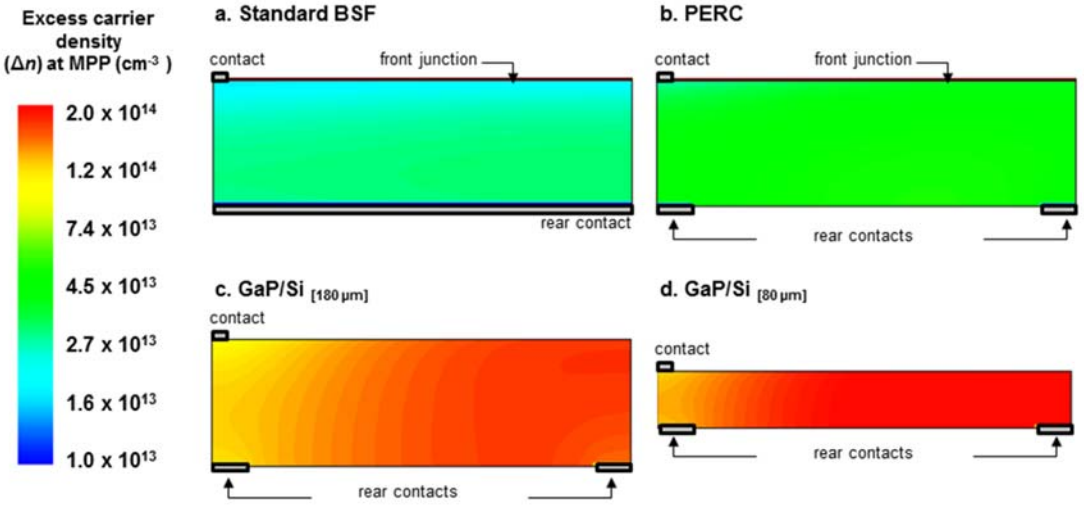

Figure 4: Cross sections of the four device architectures, (a) standard BSF, (b) PERC, (c) GaP/Si, (d) thin GaP/Si cell, showing the injection level Δn at the MPP on the color-coded scale. Bulk lifetime is set to 500 µs. Width of the devices are 600 µm, thickness are 180 µm for (a–c), and 80 µm for (d).

The second assumption in Figure 3 concerns the type and concentration of the lifetime-limiting defect center, which we assume to be a midgap trap with equal lifetimes for electrons and holes. In reality, the precise injection dependence of the SRH lifetime is governed by the defect concentration N_t, the trap energy level E_t, and the ratio of capture cross sections for electrons and holes $k = \sigma_{t,e}/\sigma_{t,h}$. Although the approximations used for Figure 3 can still provide valid results for certain defects in a low injection regime, it has to be generalized to account for the wide variety of

defects that can be present in the wafer, and for the device architectures that are driven to higher injection levels at the MPP.

To illustrate these points and broaden the applicability of Figure 3 to other defects, we plot in Figure 5 the effect of a hypothetical defect level at E_t = 0.38 eV (same as for interstitial iron, Fe_i) with four different *k*-values (k = 1, 10, 100, and 1000), which result from maintaining a constant hole capture cross section of $\sigma_h = 7 \times 10^{-17}$ (same as for Fe_i) and varying the electron capture cross section. The excess carrier density and electron lifetime at MPP for these hypothetical defects are simulated for two different cell architectures, PERC and thick GaP/Si. As expected from the discussion hitherto, for the PERC device, which operates in low injection at the MPP, variations in Sentaurus Device simulation traces are small for $k \leq 100$, while in the GaP/Si device the effect of asymmetric capture cross sections is more relevant, as it works at higher injection at the MPP.

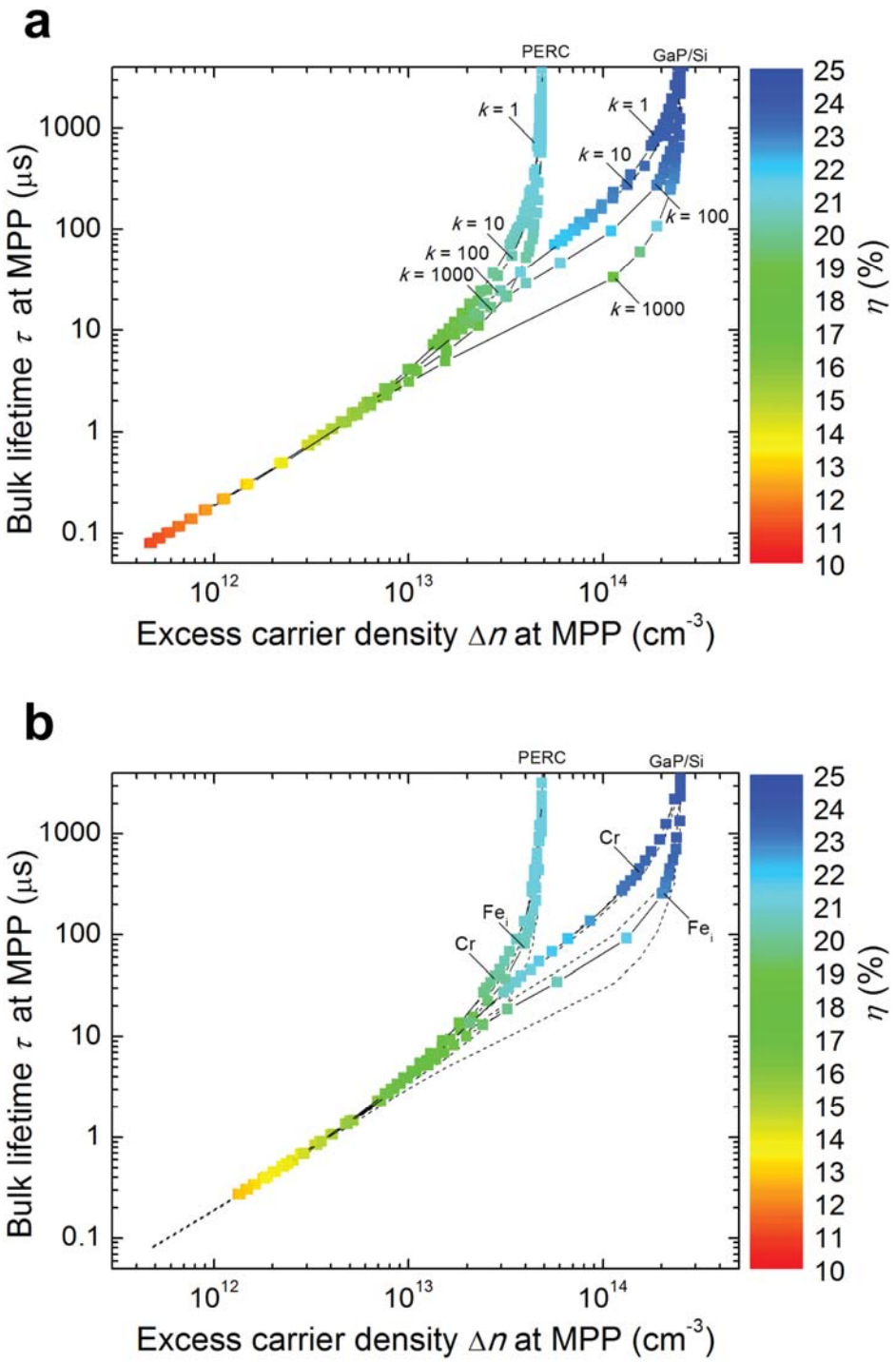

Figure 5: Reproduction of Figure 3 for two device architectures (PERC, GaP/Si [180 µm]) and different lifetime-limiting defects. (a) For a hypothetical defect with variable capture cross section ratio k=1, 10, 100, 1000. (b) For Fe (in the form of interstitial Fe_i) and Cr (forming Cr_i-B_s pairs).

Figure 5 also shows simulations for two of the most detrimental defects in *p*-type silicon, iron in interstitial form, Fe_i, and Cr_i-B_s pairs. The Fe_i point defect has a capture cross section ratio of k =186, and exhibits a large injection dependence [60][61], whereas Cr_i-B_s with k =2 exhibits a much smaller injection dependence [62][63]. In the PERC device, at low Δn, the curves for Fe_i and Cr_i-B_s defects fall on a similar line despite having different k At high Δn some divergence between the Fe_i and Cr_i-B_s curves is observed in the GaP/Si device architecture due to a strong injection-dependence of lifetime at the MPP is strong.

In conclusion, while Figure 3 is useful and elegant, we have established Figure 5 as a more broadly applicable version of this figure, which more accurately takes into account the injection dependence of bulk lifetime. We also note that if the background doping level changes, the transition between low- and high-injection regimes will also change, and Figure 5 will change subtly.

In the Appendix, we show how the presented method is applied to estimate the impact of different metal point defects on the achievable solar cell efficiency for the three cell architectures.

VII. Conclusions

In this perspective, we review bulk material requirements to achieve high cell efficiencies with unconventional wafer substrates. We show that some unconventional crystal growth techniques that traditionally were limited by material quality have recently reached millisecond-range bulk lifetimes, making them compatible with high-efficiency device architectures. We review the defect-management approach used to achieve large bulk lifetimes, including suppression of structural defects and slowly diffusing impurities during crystallization, and the gettering of medium- and fast-diffusing impurities during solar cell processing. Lastly, we review a methodology to predict a wafer's efficiency entitlement in a specific cell architecture, by superimposing the injection-dependent bulk lifetime data of the wafer on the Sentaurus Device simulations. We exemplify this in epi-Si, for which efficiencies over 20% for standard BSF and 21% for PERC device architectures are within reach now. This Si material also shows high efficiency potential for advanced architectures, such as a PERC device with a GaP n-type hetero-emitter.

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Appendix: Solar cell efficiencies as a function of metal impurity concentration

The methodology presented in section IV.C can be applied to calculate solar cell efficiency as a function of defect concentration for different cell architectures. The energy level E_t, and capture cross section ratio k of several relevant metal impurities in p-type silicon are presented in Figure A1, showing that defect properties vary widely.

It has to be noted that the accurate calculation of defect properties requires a sophisticated characterization methodology. It has been shown that the most exact ones can be determined by combining lifetime spectroscopy (in particular, Temperature- and Injection-Dependent Lifetime Spectroscopy (TIDLS) [64]) with Deep Level Transient Spectroscopy measurements (DLTS). The values represented in Figure A1 are taken from those used by the QsCell device model [65], in which the most reliable data coming from literature has been compiled and referenced.

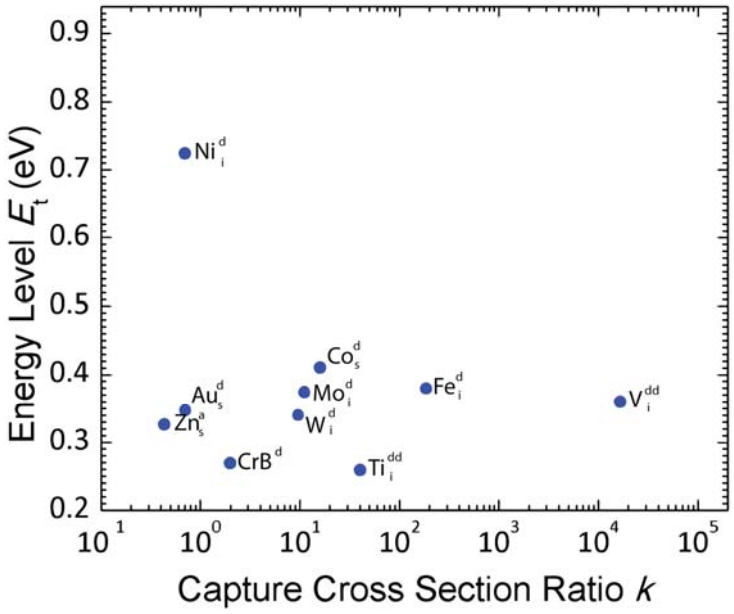

Figure A1: Defect capture cross sections and energy levels for common extrinsic defects in p-type silicon [65]***. Note the wide variation in values (x-axis in log scale).***

Using these defect parameters and SRH statistics, we calculate the bulk lifetime as a function of excess carrier density for a range of point defect concentration: from 10^9 to 10^{13} cm^{-3} (Figure A2). For device architectures that operate in the low injection regime (BSF, PERC), we use simulated efficiency curves shown in Figure 3 to superimpose the calculated lifetime curves and extract the expected device efficiency for each defect concentration. For the GaP/Si device architecture, we use Figure 5a, superimposing the calculated lifetime curves with the simulated efficiency curve for one of the capture cross section ratios k=1, 10, 100 or 1000, whichever is closest to the k value of the respective defect.

A similar approach had been chosen in reference [66] for a smaller set of defects, where a plot for a PERC structure similar to that shown in Figure A2.b was presented. The results match nicely for the impurities which are in both studies, Cr, Co, Fe and Ni. Our study expands the analysis to a wider set of impurities, and allows to compare the different sensitivity of the three cell architectures to their concentration.

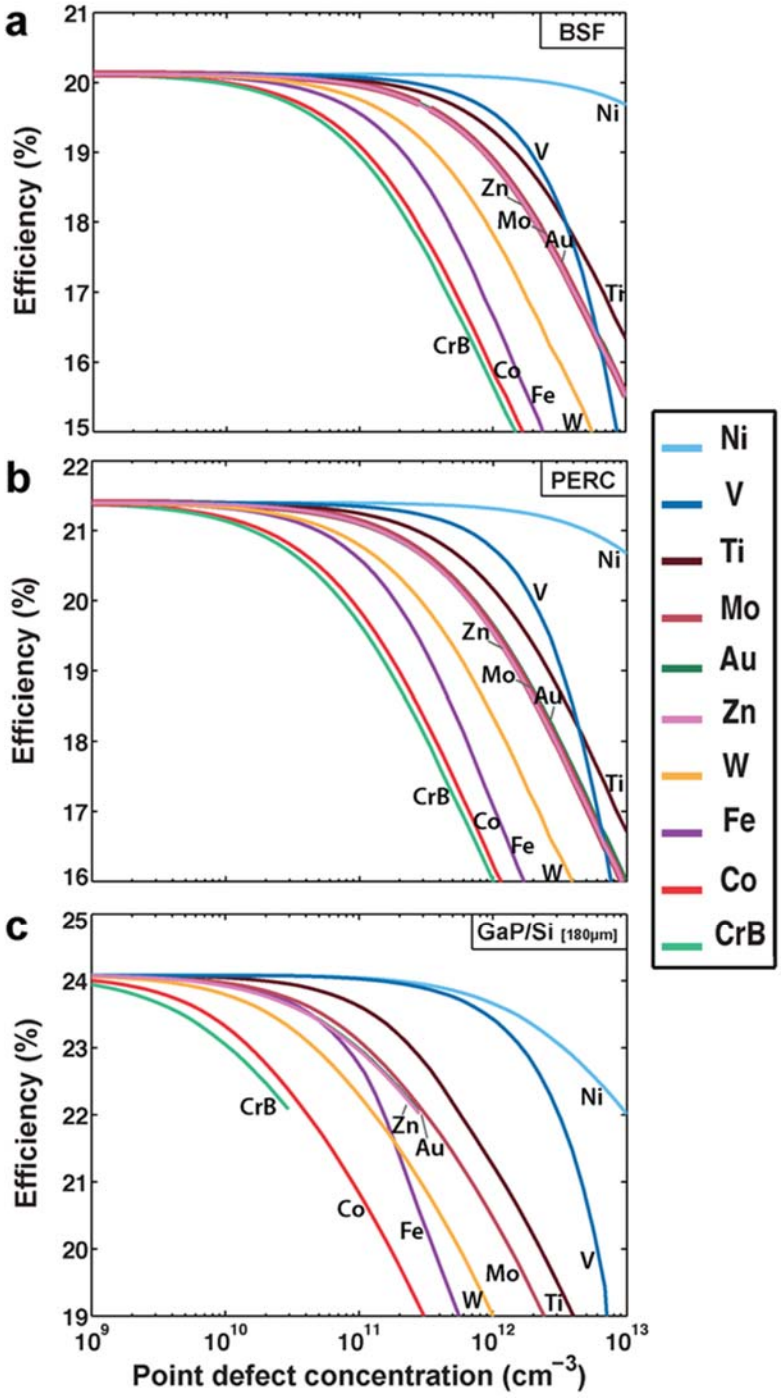

Figure A2: Simulated solar cell efficiency as a function of metal point defect concentration in a (a) BSF device; (b) PERC device; (c) GaP/Si 180 μm thick device. Efficiency values have been extracted from the intersection between simulated curves shown in Figure 3 (for BSF and PERC) and Figure 5a (for GaP/Si), and calculated bulk lifetime as a function of excess carrier density for varying defect concentration.

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