Impact of Metal-Organic Vapor Phase Epitaxy Environment on Silicon Bulk lifetime for III-V-on-Si Multijunction Solar Cells

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ABSTRACT

With the final goal of integrating III-V materials on silicon substrates for tandem solar cells, the influence of the Metal-Organic Vapor Phase Epitaxy (MOVPE) environment on the minority carrier properties of silicon wafers has been evaluated. These properties will essentially determine the photovoltaic performance of the bottom cell in a III-V-on-Si tandem solar cell. A comparison of the base minority carrier lifetimes obtained for different thermal processes carried out in a MOVPE reactor on Czochralski silicon wafers has been carried out. An important degradation of minority carrier lifetime during the surface preparation (i.e. H_2 anneal) has been observed. Three different mechanisms have been proposed for explaining this behavior: 1) the introduction of extrinsic impurities coming from the reactor; 2) the activation of intrinsic lifetime killing impurities coming from the wafer itself; and finally, 3) the formation of crystal defects, which eventually become recombination centers. The effect of the emitter formation by phosphorus diffusion has also been evaluated. In this sense, it has been reported that lifetime can be recovered during the emitter formation either by the effect of the P on extracting impurities, or by the role of the atomic hydrogen on passivating the defects.

Keywords: **III-V on Silicon, minority carrier lifetime, MOVPE, heteroepitaxy, MJSC, bottom subcell.**

1. INTRODUCTION

Multijunction solar cells (MJSCs) are one of the most successful device architectures to implement ultra high efficiency photovoltaic devices. More specifically, the combination of III-V compounds and silicon (Si) in hybrid MJSCs represents a long sought for device that would link the already demonstrated efficiency potential of III-V semiconductor MJSCs with the low cost and unconstrained availability of silicon substrates. The ultimate goal is to produce high-efficiency photovoltaic devices, while reducing the cost of solar electricity down to levels competitive with conventional sources.

Among the many alternatives followed for III-V on silicon integration [1], one of the most successful approaches so far investigated consists on the metamorphic integration of III-V semiconductors (GaAsP or GaInP) on a Si bottom cell, through the use of a GaP nucleation layer. This layer acts as a defect-free III-V template on Si [2-6], onto which a GaAsP graded buffer, which aims to confine the propagation of structural defects (i.e. threading dislocations), can be integrated. In this virtual substrate, GaAsP or GaInP top cells can be eventually integrated, thus forming a GaAsP/Si [7-11] or a GaInP/Si [12] MJSC. The vast majority of the efforts of the different groups trying to materialize this strategy have been directed towards the optimization of key steps in the epitaxial growth of III-V compounds on Si, such as the nucleation layer (GaP), the graded buffer (GaAsP) and the top subcell (GaAsP/GaInP) [6,9,11]. The main target has been the minimization and confinement of crystal defects in the structure. In this sense, high structural-quality graded buffers have been reported, achieving promising results in the reduction of the dislocation density and in the annihilation of antiphase domains [7, 9]. However, no work has been done aimed to understand the consequences of such processes on the photovoltaic performance (i.e. minority carrier lifetime) of the Si substrate, which eventually will act as the bottom subcell of the MJSC. Needless to say, the formation of a high quality bottom cell will be crucial for obtaining a highly efficient multijunction solar cell structure. This optimization requires several items, such as: (a) the preparation of the substrate for subsequent III-V growth, (b) the formation of an emitter with an adequate depth and doping concentration in the silicon bottom subcell, and (c) the attainment of a sufficiently high minority carrier lifetime in the base of the silicon bottom subcell. The latter is a key feature since the bottom cell base minority

carrier parameters will determine the PV performance of the bottom sub-cell in the tandem stack [13]. It is well established that the minority carrier lifetime in conventional PV silicon processing is not a constant material property but depends strongly on the thermal history and the environment where the sample was processed [14]. Analogously, a strong influence of the metal-organic vapor phase epitaxy (MOVPE) environment on this parameter has been reported by us elsewhere [15].

In this paper we will present results about minority carrier lifetime evolution in the MOVPE processing of silicon substrates for III/V-on-Si photovoltaics. Essentially two alternatives have been proposed in the literature for this processing or, more in particular, for the formation of the silicon subcell emitter. The first one is based on the homoepitaxial growth of silicon on the Si substrate [3,6]. This implies either the need for a special MOVPE reactor able to grow both group IV and III-V compounds (i.e. specially designed to minimize cross-contamination and carry over effects), or to grow the structure in a two-step process (i.e. taking the samples out of the reactor after Si growth, cleaning the reactor, and loading again for III-V growth). The use of homoepitaxial growth of Si has demonstrated to be a beneficial factor in the production of high quality GaP-on-Si layers [3,6], though, as discussed, introduces an additional degree of complexity in the epitaxial process. A simpler alternative would be to mimic what is done in conventional MJSC technology on germanium substrates, where the bottom subcell emitter is formed by diffusion of phosphorous (P), resulting from the pyrolysis of phosphine (PH_3). In this respect, it should be noted that several groups have also reported high quality GaP layers without homoepitaxial silicon buffers [2, 9]. Accordingly, in this work we will focus on this strategy and consider the formation of the emitter from diffusion as is the case in conventional III-V triple-junction solar cells based on germanium.

In summary, in this paper we will study the evolution of the minority carrier lifetime in the silicon substrate during the formation of the bottom subcell of a III-V/Si MJSC. In particular, in the diffused emitter approach, this process consists of three steps: 1) In the initial stage of the MOVPE process, wafers are typically subjected to a high-temperature annealing under hydrogen (H_2) atmosphere to prepare the surface for a high-quality III-V semiconductor epitaxy (oxide pyrolysis, double-step formation, …) [16, 17]; 2) in order to form the emitter, wafers are exposed to high-temperature bakes

under phosphine (PH_3) to enable the diffusion of phosphorus (P) into the silicon substrate [18]; and 3) finally, as a result of the surface degradation caused by the PH_3 exposure during the formation of the emitter, substrates need to be submitted to an additional treatment, aimed to recover the surface morphology for subsequent epitaxial growth [19]. In this sense, the formation of the emitter by exposing wafers to a high PH_3 concentration is followed by a H_2 annealing intended to recover the damaged surface morphology. Therefore, the impact on the base minority carrier lifetime of these three processes and environments will be assessed in this paper.

2. EXPERIMENTAL

The substrates used for this work were p-type boron-doped Czochralski (Cz) Si wafers oriented (100) with a miscut of 2º and 6º towards the nearest (110) plane (both misorientations were investigated). Unless otherwise is specified, the resistivity of the wafers is 5-10 Ω·cm. This kind of wafer is the mainstream product for microelectronic and single-crystal PV industries and thus offers the maximum potential for implementing low-cost III-V-on-Si technology. Before loading wafers into the reactor, they were chemically etched, as detailed in section 3.1, for removing the native silicon oxide and possible external contaminants. The experiments were carried out in a horizontal, research-scale MOVPE reactor, equipped with an IR-lamp heater. All the quartz and graphite components in the reactor chamber were installed clean and heated at 850 ºC before the experiments. The carrier gas was Pd-purified H_2, and the P precursor used was high purity PH_3. During the experiments, the phosphine partial pressure was varied from 0 to 32 mbar and the temperature range explored was from 800 ºC to 830 ºC. In order to crosscheck the results, some experiments were repeated in a different reactor: a close coupled showerhead (CCS) MOVPE reactor, located at the Ohio State University (OSU). Before performing minority carrier lifetime measurements, wafer surfaces were passivated in order to reduce the surface recombination and enable an accurate bulk material minority carrier lifetime measurement. For wafers processed only under H_2 (no P diffusion and thus, no emitter), samples were dipped in HF and then passivated using a 0,05M quinhydrone-methanol solution as the passivating agent [20]. For samples treated under phosphine, surface layers were removed with an acidic etch consisting in a HNO_3:H_2O:HF solution (to eliminate the P-diffused

layer) and then were passivated using the above mentioned wet method. Minority carrier lifetime was measured on the wafers using the well-known Photoconductance Decay (PCD) technique.

3. RESULTS

3.1 Impact of surface preparation

The effect of the surface preparation (i.e. high temperature annealing under H_2) on the minority carrier lifetime was studied elsewhere [15]. Results are summarized in fig. 1.

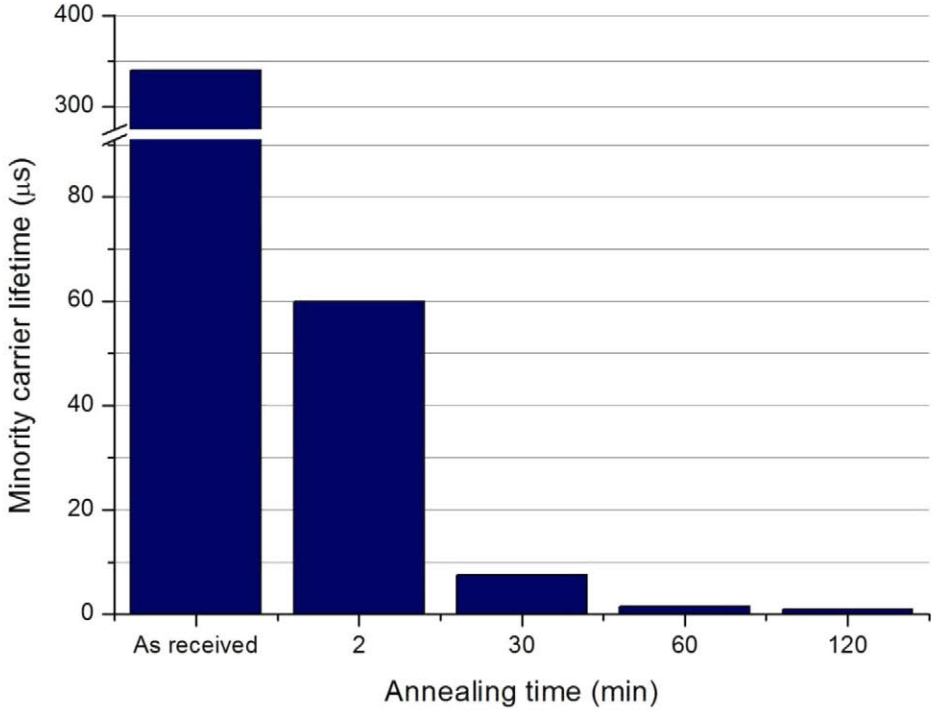


Fig. 1. Minority carrier lifetime for wafers annealed at 830°C and 900 mbar of H_2 for different times. An *as-received* wafer was included for comparison. Lifetime values were calculated for an injection level of 10^{14} cm^{-3} (except for the *as received* wafer, which was measured for 10^{15} cm^{-3}).

As shown in fig. 1, an important degradation of this parameter was observed after exposing wafers to a high temperature H_2 annealing. However, the origin of this degradation has not been fully understood. Several possibilities were considered initially for explaining this behavior: a) light induced degradation as a result of the activation of B-O pairs; b) external contamination present at the

wafer surface, which diffuses into the bulk at high temperatures (either present in the *as-received* wafer and not removed in the cleaning or introduced by the MOVPE environment); c) the activation (i.e. unpassivation) of lifetime killing centers in the Si bulk (initially non-active in the bulk); and finally d) the formation of crystal defects which eventually become recombination centers. The light induced degradation, enhanced by the activation of B-O pairs, was eventually discarded, since the same results were observed when working with gallium-doped silicon wafers, were Boron is not present [15]. The other possibilities have been studied in this work.

First of all, in order to fully rule out this degradation is a particular effect, caused by certain contamination present in our horizontal reactor; some of the experiments were repeated in a different reactor (CCS MOVPE). Results are presented in table 1.

Table 1. Minority carrier lifetime for wafers annealed in hydrogen for 30 min. at 100 mbar in two different reactors.

H_2 anneal	Reactor	Δn (cm^{-3})	τ (µs)
As received	-	10^{15}	340
30 min. 800 °C H_2	Horizontal	10^{14}	6.5
30 min. 800 °C H_2	CCS	10^{14}	4.8

As it is shown in table 1, the same results were obtained after the H_2 anneal, regardless of the reactor used for the thermal treatment. These results prove that the lifetime degradation observed after the surface preparation at MOVPE is neither the effect of a particular reactor condition nor configuration. On the contrary, lifetime degradation seems inherent to the MOVPE environment used for III-As/P growth.

It is well know that any metal contaminants initially present on a wafer surface will diffuse into the wafer's bulk during a high temperature annealing, as a result of the thermal load. In this sense, the importance of a thorough wafer cleaning before subsequent thermal processing has been repeatedly reported in the literature [21]. In order to discard external contamination as the origin of this

behavior, the impact of the cleaning method on the minority carrier lifetime has been assessed (Table 2). With this aim, wafers were cleaned using different methods and afterwards, they were annealed following the same MOVPE routine (i.e. 30 min. hydrogen annealing at 830 ºC). Three different cleaning methods were tested: 1) Method A: diluted fluorhydric acid; 2) Method B: diluted fluorhydric acid followed by a de-ionized water rinse; 3) Method C: the standard RCA cleaning (NH_4OH:H_2O_2:H_2O 1:1:5 + HF:H_2O 1:50 + HCl:H_2O_2:H_2O 1:1:6 + HF:H_2O 1:50). Furthermore, a non-cleaned wafer was included for comparison.

Table 2. Minority carrier lifetime of wafers cleaned following different routines. They were annealed in hydrogen afterwards for 30 min at 100 mbar.

Cleaning	H_2 anneal	Δn (cm^{-3})	τ(μs)
None	*As-received*	10^{15}	340
None	30 min. 830 °C	10^{14}	8.9
Method A	30 min. 830 °C	10^{14}	7.5
Method B	30 min. 830 °C	10^{14}	5.9
Method C	30 min. 830 °C	10^{14}	5.4

As table 2 evidences, no significant difference was observed on minority carrier lifetime despite the fact that different cleaning methods were used.

Another possibility which was considered to be responsible for this degradation was the activation of lifetime killing impurities. These impurities could be either initially present in the wafer (though passivated) and be then activated (i.e. lose their passivation) during the MOVPE process, or they could come from the reactor atmosphere. With the aim of ascertaining whether the activation of internal impurities is responsible for such degradation, different Cz wafer suppliers were tested in past works and the same degradation was observed after annealing in hydrogen (see details in [15]). Moreover, some of the experiments were repeated using float zone (Fz) Si wafers, which have a significantly lower impurity concentration. A minority carrier lifetime comparison between Cz and

Fz wafers is reported in table 3. Roughly the same degradation was measured after the H_2 annealing regardless the wafer growth method (table 3).

Table 3. Minority carrier lifetime comparison for Cz and Fz wafers annealed in H_2 for 30 min.

Wafer nature	H_2 anneal	Δn (cm^{-3})	τ(μs)
Cz	*As-received*	10^{15}	340
Cz	30 min. 830ºC	10^{14}	4.1
Fz	*As-received*	10^{15}	445
Fz	30 min. 830ºC	10^{14}	5.0

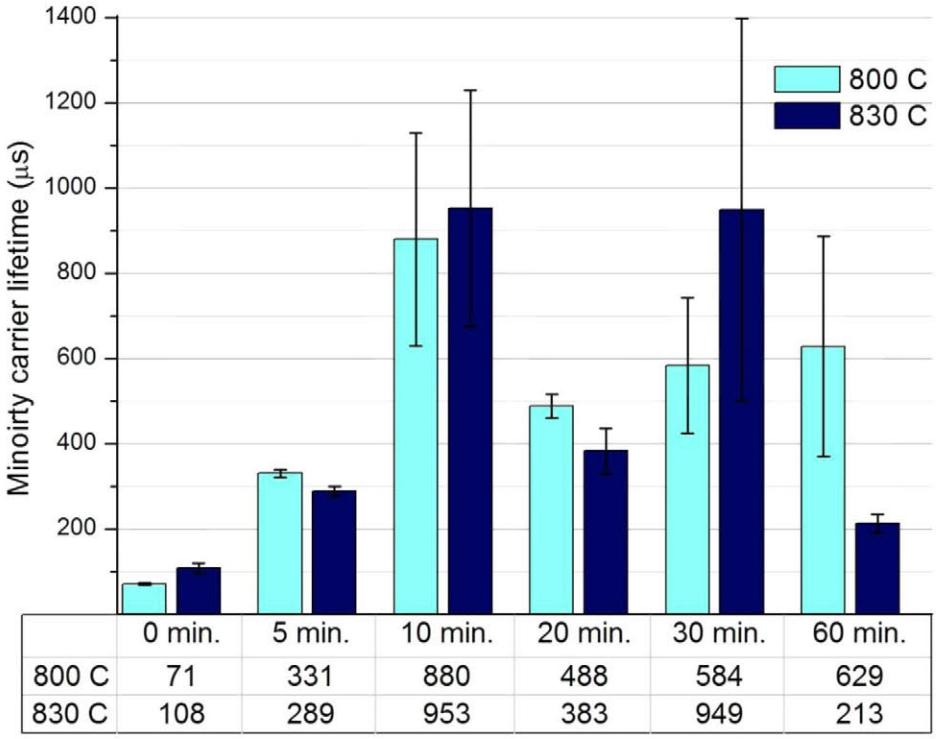
Finally, it has been assessed whether the lifetime degradation is caused by the activation of impurities coming from the reactor atmosphere. For conventional silicon PV technology, it has been reported, that the presence of H_2 in p-type crystalline Si wafers is not desirable because of the introduction of lifetime killing centers by the formation of H-O related complexes [14, 22]. The behavior of Fz wafers, were O is not present and which exhibited a lifetime degradation virtually identical to that of Cz-silicon, made us rule out this possibility. However, in order to fully discard this option we conducted an experiment aimed to confirm the effect of the carrier gas influence on to the lifetime degradation. In this case, nitrogen was used as the carrier gas and therefore samples were thermally treated in the absence of H_2. Results of this experiment are summarized in Table 4. As it is shown in Table 4, loosely the same values were measured after the annealing disregarding of the carrier gas, suggesting that H_2 carrier gas does not have a determinant role in the degradation of electron lifetime in the p-silicon wafer. However, in a MOVPE environment Si wafers are treated in a chamber where several group-III and group-V species coexist in the presence of organic radicals, hydrogen carrier gas and high temperatures. Therefore, other species (apart from hydrogen) could be involved in this reported lifetime degradation.

Table 4. Minority carrier lifetime of wafers annealed for 30 min. at 900 mbar in different atmospheres. In this case, wafers have a lower resistivity (1-5 ohm·cm)

MOVPE treatment	Δn (cm^{-3})	τ (μs)
As-received	10^{15}	107
30 min. 800 °C H_2 anneal	10^{15}	14.5
30 min. 800 °C N_2 anneal	10^{15}	17.2

3.2 Impact of the emitter formation

As it was described before, wafers are exposed to high-temperature annealing under phosphine to enable phosphorus (P) diffusion into the silicon substrate for the formation of the emitter. As it was reported previously [15], the minority carrier lifetime will be deeply affected by the phosphine partial pressure in the MOVPE reactor during this process. In this work, the effect on bulk lifetime of temperature and PH_3 annealing duration is assessed. With this aim, samples were annealed in phosphine at different temperatures (800 °C and 830 °C) for different times (5 min., 10 min., 20 min., 30 min. and 60 min.). In all cases, phosphine partial pressure remained constant and equal to 32.1 mbar as suggested in [15]. Wafers were cleaned (according to above mentioned method B) before being loaded into the MOVPE reactor. They were heated up in H_2 to the defined set point and, once the desired temperature was reached and stabilized, the PH_3 source was opened. In order to assess the impact of the initial H_2 heating ramp (prior to the phosphine exposure) on minority carrier lifetime, a sample which was just heated up to the annealing temperature (in H_2) and cooled down afterwards, was also included for each temperature. In order to check the significance of these results, each wafer was passivated and measured several times.



	0 min.	5 min.	10 min.	20 min.	30 min.	60 min.
800 C	71	331	880	488	584	629
830 C	108	289	953	383	949	213

Fig. 2. Average minority carrier lifetime for Si wafers annealed under 32.1 mbar of PH_3 at 800 °C and 830 °C for different times. Lifetimes were calculated for an injection level of 10^{15} cm^{-3}.

The average lifetime has been plotted in Fig. 2, which shows the lifetime evolution as a function of the PH_3 annealing conditions. The error bars represent the maximum and minimum values measured for each sample. The high variability of the results will be discussed in section 4.

3.3 Impact of anneals to recover surface morphology

Although the formation of the emitter by P diffusion can produce excellent minority carrier lifetimes in the base and optimum emitter properties in the Si subcell [18]; we have demonstrated that the effect of long PH_3 exposures at temperatures ranging from 800-875 °C (required for obtaining a deep enough emitter) will lead to an important degradation of the surface morphology [19]. Of course, a degraded surface morphology will cause deleterious effects on the quality of the subsequent epitaxial growth of III-V layers. In this sense, we have also proven that using a combined treatment consisting

on PH_3 exposure (P diffusion) followed by a H_2 annealing, lead us to obtain an optimum emitter (shallow and highly doped) while recovering surface morphology to acceptably low RMS roughness values [19].

The impact of this combined treatment on the minority carrier lifetime has been assessed. With this aim, a lifetime comparison between wafers annealed in PH_3 (samples 1, 3 and 7) and wafers submitted to the combined treatment (as described in table 5) is presented in fig. 3.

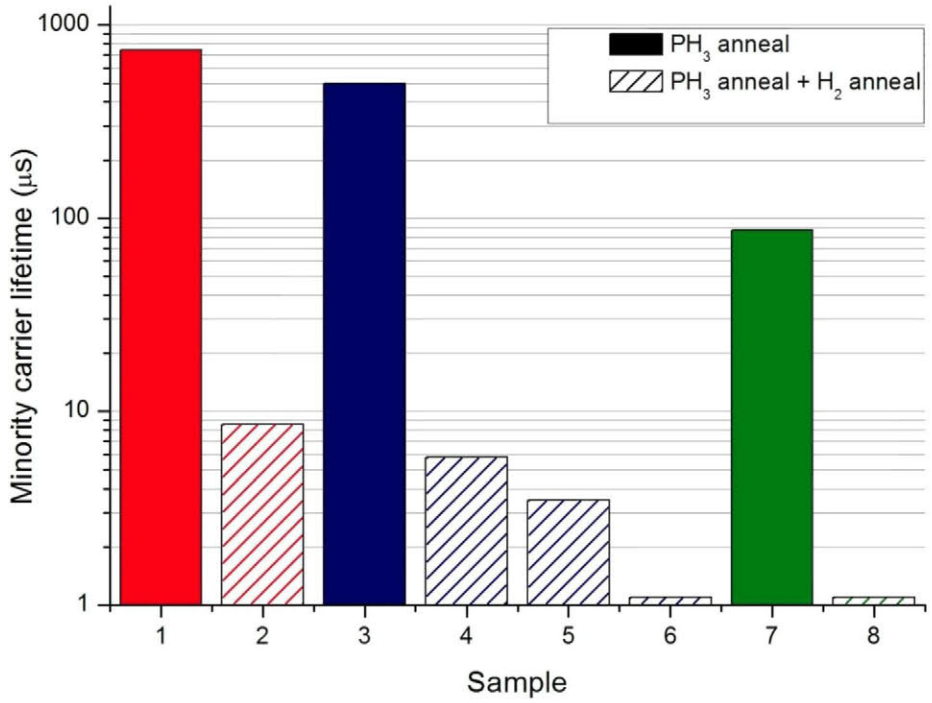


Fig. 3. Minority carrier lifetime for samples summarized in table 5. Solid bars correspond to samples annealed under PH_3 (lifetimes correspond to an injection level of 10^{15} cm^{-3}). Samples submitted to the combined treatment were represented as dashed bars (injection level of 10^{14} cm^{-3}).

Table 5. Description of the third batch of experiments where wafers were first annealed under hydrogen mixed with 32.1 mbar of PH_3 and then annealed under pure H_2.

Sample	PH_3 anneal (32.1 mbar)	H_2 anneal conditions
1	30 min. 800 ºC	-
2		20 min. 830 ºC
3	30 min. 830 ºC	-
4		20 min. 830 ºC
5		60 min. 830 ºC
6		60 min. 875 ºC
7	10 min. 875 ºC	-
8		60 min. 875 ºC

4. DISCUSSION

The evolution of the minority carrier lifetime of Si wafers during different treatments aiming the optimization of the Si bottom subcell has been analyzed. First of all, we have studied the effect of the surface preparation (H_2 anneal at 830 ºC) on the minority carrier lifetime. We have reported an unquestionable degradation in minority carrier lifetime as a result of the thermal treatment. It has been observed a rapid lifetime drop in the first minutes of the annealing and, afterwards, its progressive decrease until the lower detection limit of our PCD equipment is reached (~1 μs). In order to confirm the reproducibility of these results, some of the experiments were repeated in a different MOVPE reactor and the same effects were observed. Obviously, such low minority carrier lifetimes in the base of the silicon bottom subcell would make it impossible to manufacture even a modest-performing solar cell.

Some possible causes behind this effect can excluded in the light of the experiments of section 3. First of all, we have considered the introduction of external contamination, coming from the wafer surface, as the origin of lifetime degradation. In this sense, different chemical methods used in

conventional silicon PV technology have been used for cleaning the wafers. The same results were obtained in all cases, regardless of the cleaning method, indicating that the wafer cleaning procedure is not the main factor impacting lifetime.

Another possibility which was considered for explaining this behavior is the activation of lifetime killing impurities during the MOVPE treatment, which might be present initially in the bulk in an inactive state. If this assumption is correct, using Fz wafers (which have a significantly lower impurity concentration, as compared to the Cz wafers), should show a higher immunity to lifetime degradation. On the contrary, the same behavior was observed regardless the wafer growth method and supplier. Hence, it seems unlikely that this phenomenon is responsible for the lifetime degradation, although we can't fully discard this hypothesis.

One of the distinctive features of the MOVPE process is that it is developed under H_2 carrier gas, which is a significant difference as compared to processing environments in conventional PV technology. According to the literature, the use of hydrogen at high temperatures might have a determining effect on reducing the lifetime by the introduction of deep-level defects associated to H-O pairs [14, 22]. In order to confirm this possibility, we have repeated some of the experiments using N_2 as carrier gas but the same effects were observed. Hence, lifetime degradation cannot be attributed to H_2 either. Furthermore, in a prior work [15] we also ruled out that the formation of B-O pairs –we use CZ-grown B-doped silicon wafers– was behind this degradation since Ga-doped silicon wafers exhibited the same lifetime degradation.

In summary, the reason for the lifetime degradation is still unknown and different experiments are undergoing to clarify it. However, this effect has been found to be linked to a MOVPE environment but unrelated to the use of H_2 as the carrier gas, independent of the wafer nature, the cleaning procedure prior to loading the wafers in the reactor, and not caused by the formation of B-O pairs.

In a second set of experiments, we have reported the effect of the emitter formation (by P diffusion) on the minority carrier lifetime (fig. 2). After heating up the wafer to the annealing temperature (in the absence of phosphine), the initial lifetime (340 μs) is roughly reduced by a factor of 3 (see leftmost bars of both temperatures in fig. 2); corroborating the effect shown in fig. 1. Nevertheless,

despite the initial degradation during the heating up of the wafer, lifetime can be recovered during the emitter formation, as it is shown in fig. 3. The impact on annealing duration and temperature are difficult to assess. In the worst cases, lifetime was recovered to the initial value of the *as-received* wafer; while in the best cases, values larger than 1ms were measured.

The wide range of variation of the minority carrier lifetimes measured in the experiments is believed to be related to the surface passivation quality. According to [23], the effective lifetime (τ_{eff}) is related with the bulk lifetime (τ_b) and the effective surface recombination velocity (S_{eff}) as follows:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_b} + \left[\frac{W}{2S_{eff}} + \frac{1}{D}\left(\frac{W}{\pi}\right)^2\right]^{-1} \quad (1)$$

Being D the diffusion coefficient for silicon (30 cm^2/s) and W de wafer thickness (275 μm). This equation is valid for surface recombination velocity (S_{eff}) lower than 10^7 cm/s.

According to eq. 1, the effective lifetime will be limited by the surface recombination velocity for samples with a very high bulk lifetime. On the contrary, it will be determined by the bulk lifetime for samples with an excellent passivation quality (i.e very low S_{eff}). Fig. 4 shows the contribution of τ_b and S_{eff} to the effective lifetime. It shows the importance of having a low surface recombination velocity for measuring high effective lifetimes.

Moreover, fig. 4 points out that wafers with high bulk lifetimes require an extremely good passivation (S_{eff} < 5 cm/s), to ensure that the effective lifetime measured corresponds to the bulk lifetime and it is not being limited by S_{eff}. The fact that such low surface recombination velocity is needed for measuring the real bulk lifetime can explain the high variability of measurements shown in fig. 2. According to literature, a wide range of SRV can be obtained depending on the passivating agent and the wafer specifications. For instance, S_{eff} values in the 20-50 cm/s range are usually reported for Si_3N_4 passivated surfaces; however, a record low S_{eff} of 4 cm/s were reported for a low-resistivity p-type Si wafer [24], reducing roughly in a factor of 10 the recombination velocity reported for SiO_2 passivated surfaces. Typically values of S_{eff} for iodine/ethanol passivated surfaces

are in the 10-50 cm/s range [25]. Finally, typical values of about 10 cm/s were usually measured for quinhydrone/methanol passivated Si surfaces (the strategy used in this paper); being the lowest S_{eff} reported 4.2 cm/s for a Fz Si wafer [20]. Accordingly, it cannot be assumed a constant S_{eff} for all the samples, since it will be deeply modulated by the surface preparation and the wafer properties; however it seems reasonable to expect a S_{eff} in the range of 1-20 cm/s for our quinhydrone/methanol passivated surfaces (shown as a gray stripe in fig. 4).

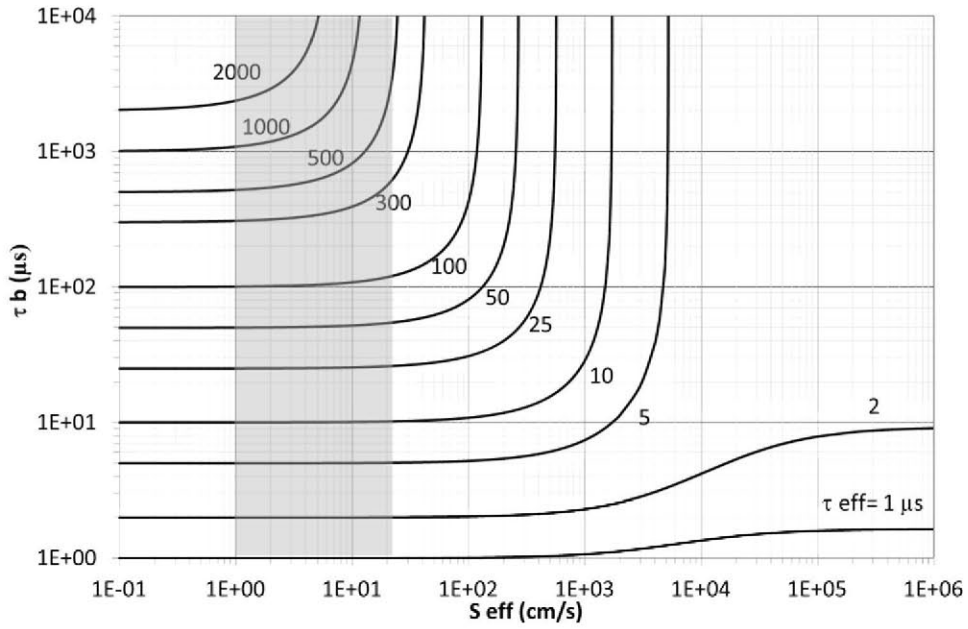


Fig. 4. Effective lifetime for a 275 µm thick Si wafer as a function of bulk lifetime and surface recombination velocity. A gray stripe, which corresponds to the expected range of Seff using quinhydrone:methanol solution as the passivating agent, has been also included.

With the aim of assessing the real impact of S_{eff} on the effective lifetime, we have compared the bulk lifetime, corresponding to each average effective lifetime shown in fig. 2, for two different values of S_{eff} (within the expected range) according to eq. 1. Results are summarized in fig. 5. Despite the surface recombination velocity is low in both cases (< 20 cm/s); a big discrepancy between τ_{eff} and τ_b is observed. In this way, only when having an extremely good passivation (S_{eff}= 1 cm/s), the effective lifetime will correspond to the bulk lifetime. Otherwise (when having slightly higher, but still low,

S_{eff}) the surface recombination limits the effective lifetime, and hence, the gap between τ_b and τ_{eff} increases, measuring much lower τ_{eff}. This fact can thereby explain the big variability in measurements depicted in fig. 2. In this sense, for a wafer with a certain τ_b, only when a perfectly cleaned surface is obtained, an excellent passivation quality is achieved and thus, a τ_{eff} close to the τ_b is measured (highest level of the error bars included in fig. 2). On the contrary, when surfaces are not perfectly passivated (because of a poorer cleaning or non-uniform passivation) the S_{eff} begins to limit the effective lifetime, measuring lower τ_{eff} (lowest level of the error bars in fig. 2) for the same τ_b.

With such wide variation ranges (which are the result of small changes in the processing of the samples) we have concluded that we cannot accurately and repeatedly determine lifetimes above 350 μs. In other words, for measured lifetimes below 350 μs, we can be sure that they are close to the real bulk lifetime. For measured lifetimes above the 350 μs limit, we are limited by surface recombination velocity and the effective lifetime is just a lower limit for the bulk lifetime.

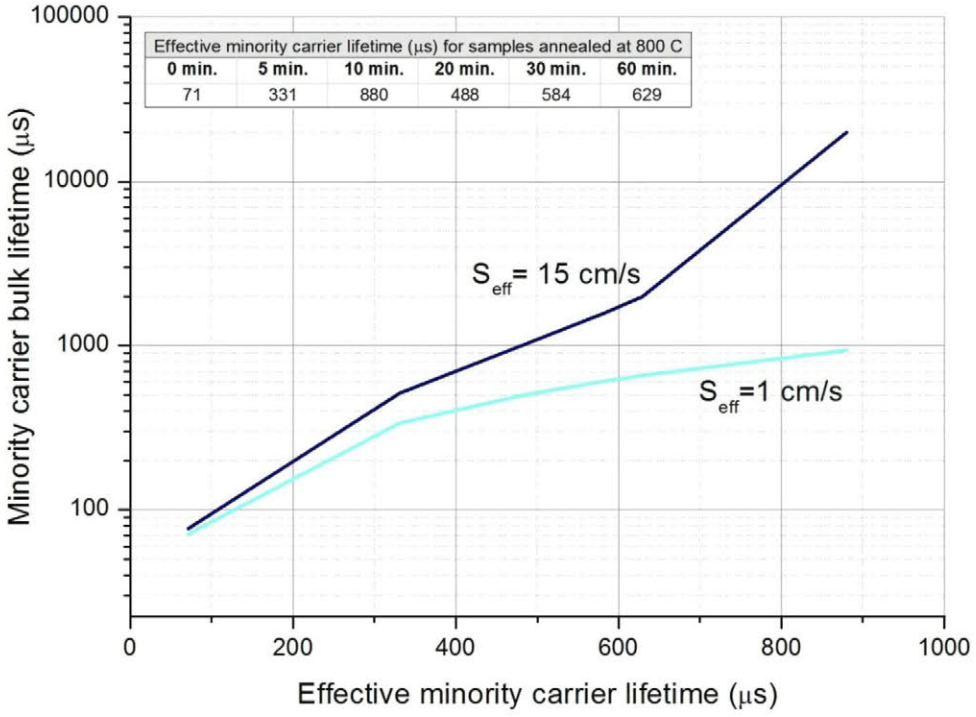


Fig. 5. Compassion of bulk lifetime, calculated from average effective lifetimes reported in fig. 2 for 800 °C, for two different surface recombination velocities.

In summary, the effect of the PH_3 annealing on recovering lifetime has been demonstrated. However, it is complicated to quantify this improvement, since results will be deeply affected by small (i.e. highly uncontrollable) changes in the surface passivation quality that will limit our precision to assess the real bulk lifetime.

Finally, we have reported the effect on the lifetime of a second annealing in pure H_2 (intended to recover surface morphology) after P diffusion (see fig. 3). Although bulk lifetime reaches high values after PH_3 exposure (solid bars in fig. 3), it gradually degrades after the second step in H_2 (dashed bars). This degradation is deeply modulated by the H_2 annealing conditions; becoming more important as the temperature and duration increase, as shown in fig. 3. In this case, the degradation of lifetime is unequivocal since the effective values measured are too low to be affected by surface passivation. This phenomenon limits the use of H_2 anneals to recover the morphology of the silicon surface and underlines the importance of gaining more insight into the processes behind minority carrier lifetime degradation.

What this result suggests is that the role of PH_3 in recovering lifetime is not related to a classic phosphorus diffusion gettering process as occurs in conventional silicon PV technology. In other words, the preferential segregation of the lifetime killing impurity/defect that is responsible for minority carrier lifetime degradation to the highly P-doped region seems unlikely. This is because the highly P-doped region is still there during the second H_2 anneal, the high temperatures (to promote fast diffusion of impurities) are still there too, but the minority carrier lifetime degrades indicating that the lifetime killing impurity (or level) is re-introduced (or re-activated) in the bulk. We do not fully understand this process yet. However, we are investigating several possible mechanisms that would explain our experiments.

Mechanism 1: The treatment under H_2 at high temperatures introduces an extrinsic lifetime-killing impurity coming from the reactor. During the PH_3 anneal, this impurity is either extracted with the help of the P surface coverage or passivated somehow with atomic H. The first process (extraction) seems unlikely since fig. 2 indicates that this process is extremely fast (in 5 minutes the lifetime seems to be recovered). More in agreement with such high speed would be a passivation process based on the diffusion of atomic H into the silicon lattice. Once PH_3 flow is interrupted whilst high

temperatures are still maintained, this passivation is gradually lost or new amounts of the impurity are introduced in the wafer.

A possible lifetime killing impurity that would be compatible with this behavior would be zinc. Zinc is a typical p-type dopant in III-V semiconductors (i.e. traces would be present in many MOVPE environments) and it is a lifetime killing impurity in silicon [26]. Levels of this impurity in the range of 10^{12} cm^{-3} (i.e. below SIMS detection) would ruin minority carrier lifetime. This mechanism would be independent of the wafer nature, affecting both FZ and CZ wafers.

Mechanism 2: The treatment under H_2 at high temperatures leads to the formation of crystal defects, which eventually become recombination centers. During the PH_3 anneal, these recombination centers are either recombined with the help of the P diffusion process or passivated with atomic H. As in the previous case, due to the speed of this process, the passivation process based on the diffusion of atomic H into the silicon lattice is the most realistic option. Once PH_3 flow is interrupted, this passivation is lost and hence, new recombination centers are formed in the wafer, degrading again the lifetime. This last mechanism would be also independent of the MOVPE environment and would affect both FZ and CZ wafers.

Mechanism 3: The treatment under H_2 at high temperatures releases (activates) an intrinsic lifetime-killing impurity coming from the wafer itself, which was initially inactive. During the PH_3 anneal, this impurity is neutralized with atomic H and it is re-activated by treatment under H_2 (i.e. once PH_3 flow is interrupted). This second mechanism would be independent of the MOVPE environment and would probably, show up with different intensities in FZ and CZ wafers.

Further experiments are ongoing to clarify which mechanism is governing the process and to determine whether the P or the atomic hydrogen is controlling the lifetime recovery. On the one hand, the role of the phosphorous will be assessed by replacing the PH_3 for AsH_3 and comparing the results. On the other hand, the role of the atomic hydrogen will be assessed by using tertiarybutylphosphine (TBP), a P precursor which produces far less H as a sub-product of its pyrolysis.

5. CONCLUSIONS

In this paper we have analyzed the impact of the MOVPE environment on the minority carrier lifetime during the optimization of the Si bottom subcell, for its eventual integration on a III-V/Si MJSC. First, we have studied the effect on the minority carrier lifetimes of the H_2 anneals at high temperature used for surface preparation. An important degradation of minority carrier lifetime during the thermal treatment has been observed. The reproducibility of these results has been proven by repeating the most relevant experiments in two different MOVPE reactors. The exact cause behind this phenomenon remains unclear. However, on the one hand, it has been demonstrated that this degradation is not produced by a defective cleaning process prior to loading the samples in the MOVPE reactor. Three standard cleaning methods, regularly applied in silicon PV technology, have been tested with essentially the same degradation results in minority carrier lifetime. This fact makes us rule out the introduction of an external contaminant (coming from a poorly cleaned wafer surface) as the possible cause behind lifetime degradation. On the other hand, we have discarded the sole effect of the hydrogen carrier gas on activating lifetime killing centers (as occurs in conventional Si technology with O-H pairs), since the same degradation was observed when N_2 was used as the carrier gas.

It has been also reported that the degraded minority carrier lifetime can be recovered during the exposure to a PH_3 atmosphere for the emitter formation. The extent of this recovery is difficult to assess since the impact of low (but not negligible) surface recombination velocities impedes an accurate determination of high bulk minority carrier lifetimes. Although the mechanisms governing this phenomenon have not been fully understood yet, it seems that phosphorus diffusion gettering cannot be the mechanism behind lifetime recovery.

Finally, we have assessed the impact on the minority carrier lifetime of an additional H_2 annealing after PH_3 exposure for emitter formation. The goal of this new annealing is to recover surface morphology (degraded during PH_3 exposure) and ensure a smooth surface for subsequent III-V growth. This experiment reveals that, once the phosphine supply was interrupted, the degradation of minority carrier lifetime starts again just as occurred in the initial H_2 anneal. Further work, aimed to

clarify the physical phenomena behind this lifetime degradation and to study the effect of growing III-V layers on the silicon substrate layers on lifetime is ongoing.

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