# A Built-in CMOS Total Ionization Dose Smart Sensor

Javier Agustin, Carlos Gil Soriano, Marisa Lopez Vallejo and Pablo Ituero

***Abstract*—Total Ionization Dose (TID) is traditionally measured by radiation sensitive FETs (RADFETs) that require a radiation hardened Analog-to-Digital Converter (ADC) stage. This work introduces a TID sensor based on a delay path whose propagation time is sensitive to the absorbed radiation. It presents the following advantages: it is a digital sensor able to be integrated in CMOS circuits and programmable systems such as FPGAs; it has a configurable sensitivity that allows to use this device for radiation doses ranging from very low to relatively high levels; its interface helps to integrate this sensor in a multidisciplinary sensor network; it is self-timed, hence it does not need a clock signal that can degrade its accuracy. The sensor has been prototyped in a 0.35$\mu m$ technology, has an area of 0.047mm2, of which 22% is dedicated to measuring radiation, and an energy per conversion of 463pJ. Experimental irradiation tests have validated the correct response of the proposed TID sensor.**

## I. Introduction

Accumulative radiation effects are a main concern in electronic design, especially in hostile environments such as space. Long term ionizing damage can cause devices to suffer threshold shifts, increased leakage and noise, timing changes, etc. In this scenario, monitoring the degradation suffered by devices becomes a must. Based on reliable measured data electronic systems can be aware of their health state and if necessary take actions. For instance, techniques based on annealing allow a partial recovery from the damage caused by ionizing radiation.

The most common way to measure ionization dose in electronic systems is by means of RADFETs [1]. These transistors present a predictable variation in the threshold voltage ($V_T$) as a function of the radiation dose. A stack-connected [2] structure improves their sensitivity that otherwise is scarce for low radiation doses. A main drawback is that they need a radiation hardened ADC if they are integrated in a digital system, which supposes an important area overhead. Furthermore, the area of the system dedicated to measuring the radiation is a small percentage of the total.

To overcome these disadvantages, we propose in this work a TID sensor based on measuring variations in a delay path. Our system is fully digital and can be implemented in many forms, from a built-in sensor in a standard cell application-specific integrated circuit (ASIC) to programmable devices such as FPGAs. Its small size and its lack of an analog part makes it attractive for electronic systems that require TID monitoring during their lifetime.

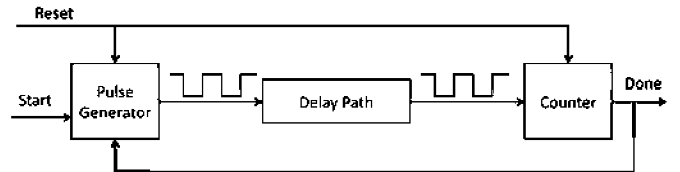


Fig. 1. Self-timed sensor scheme.

Additionally, its size allows to embed the sensor into complex systems taking locally accurate measurements for each part of the design instead of the global radiation sensing that RADFETs provide. Additionally this sensor has a time to digital interface able to be integrated in a on-chip monitoring network such in [4].

Our study has been corroborated with the design, fabrication, radiation and characterization of the proposed TID sensor. We have also analyzed how annealing takes place in circuits to recover from radiation effects.

The paper is organized as follows. First, we present the basis of the sensor and the manufactured prototype. Then, we show the radiation tests carried out in the devices under test (DUTs). After that, we analyze the results achieved during the test procedure. And finally, we conclude the work with our main contributions.

## II. Sensor Design

The proposed TID sensor is based on the multi-purpose sensor published in [3] whose basic scheme is shown in Figure 1. That sensor is implemented on an FPGA for temperature and process variations monitoring. We have modified it to sense the total ionization dose following a full-custom design.

The sensor is composed of three different blocks. The pulse generator provides a self-timed signal that acts as a self-generated internal clock creating the signal whose delay is going to be measured. The delay path is the most important block and it defines the purpose of the sensor and its accuracy.

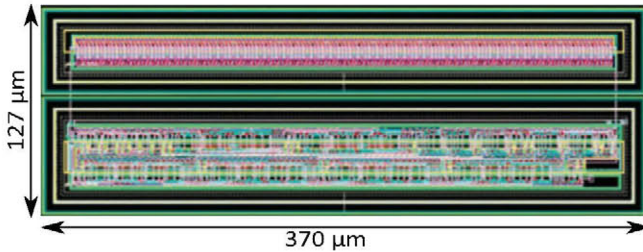


Fig. 2. Layout of the TID proposed sensor. Top (delay path). Bottom (pulse generator and counter).

And the third block is the counter which confers the sensor the skill to have a configurable sensitivity by changing the number of pulses that this part of the sensor counts.

The sensor works as follows. The external control system resets the sensor registers (pulse generator and counter), the control excites the $Start$ signal when it wants to monitor the TID level that the sensor has detected and it waits until the $Done$ output is triggered. The measured magnitude is determined by the lapsed time between $Start$ and $Done$. So a time-to-digital converter is necessary to digitize the sensing value to be used in other blocks.

Our goal is to design a delay path sensitive to radiation ionization making the rest of the blocks radiation-hardened. To achieve this target we have implemented the design of Figure 2. This sensor has been manufactured applying a $0{,}35\mu m$ technology from ON-SEMI. In this layout, two main parts can be seen. The top of the layout is composed of a delay path formed by a 256-inverter chain and the bottom block confines the pulse generator and the counter.

The delay chain utilizes common inverters of minimum channel length because it is well-known that CMOS transistors are altered by charge accumulation produced by radiation [5]. This alteration is mainly a threshold voltage (Vt) shift in p- and n-transistors. Therefore the variation of Vt will cause a change in the delay path propagation which ultimately allows to sense the accumulated ionization. Furthermore, the use of minimum transistors improves the integration and maximization of the area that is sensitive to radiation.

With regard to the bottom layout section, we have implemented various radiation hardened by design (RHBD) techniques. First, we have used enclosed layout transistors (ELT) [6] as the one in Figure 3. This type of transistors has evidenced better radiation performance for technologies bigger than hundreds of nanometers. Second n-transistors are electrically isolated from p-transistors by a guard ring. The guard ring catches close charges avoiding easy paths for ions through semiconductor interfaces where TID effects are more accused. And finally, the sensing part is also electrically isolated from the pulse generator and the counter. The sum of all these techniques provides our sensor with the radiation characteristics we were looking for: a radiation sensitive delay path and radiation tolerant logic blocks.

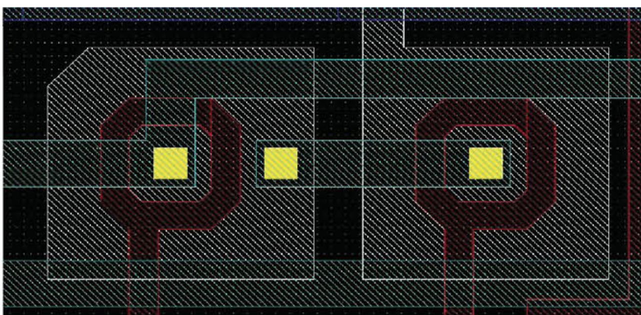

Fig. 3. ELT layout for radiation tolerant transistors.

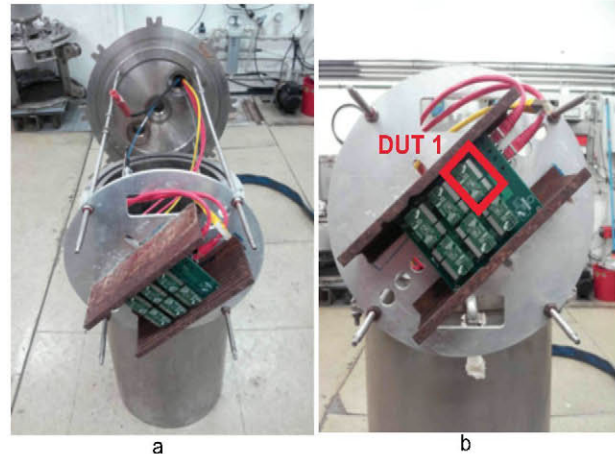


Fig. 4. Test set up for $^{60}Co$ radiation test at CIEMAT.

We have been unable to use the configurable sensitivity feature of the sensor because it was embedded within a more complex chip with scarce I/O pads. Therefore, we had to fix the value of the counter constant to the maximum 4-bit pulse-count.

TABLE I
SENSOR FEATURES.

| | Area | Percentage | Energy/conversion |
|---|---|---|---|
| Sensing | $10400\mu m^2$ | 22% of sensor | 300pJ |
| Logic | $18910\mu m^2$ | 40% of sensor | 163pJ |
| Electrical Isolation | $17680\mu m^2$ | 38% of sensor | |
| Total Sensor | $46990\mu m^2$ | 1.2% of ASIC | 463pJ |
| Total ASIC | $4mm^2$ | 100% | |

Table I summarizes the manufactured prototype. In a small chip of 2mmx2mm the sensor only requires the 1% of the total area. Another remarkable figure is the low energy per conversion.

## III. Test Setup

Radiation tests were carried out at the NAYADE facility of CIEMAT in Madrid. This water-pool station is ready to make radiation tests with $^{60}Co$ at different dose rates, depending on the distance between DUTs and the radiation sources.

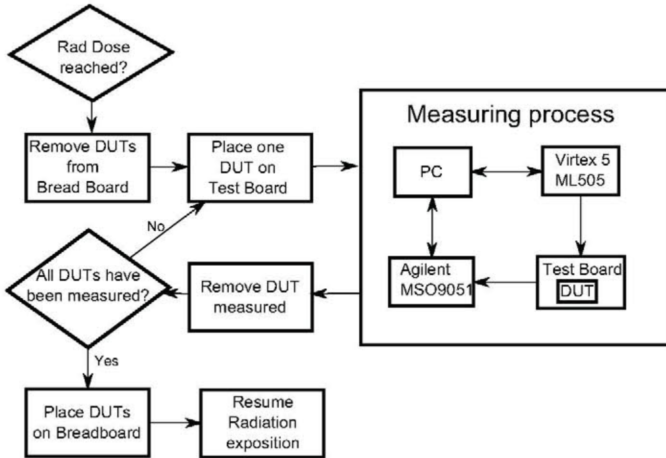


Fig. 5. Diagram of measurement process.

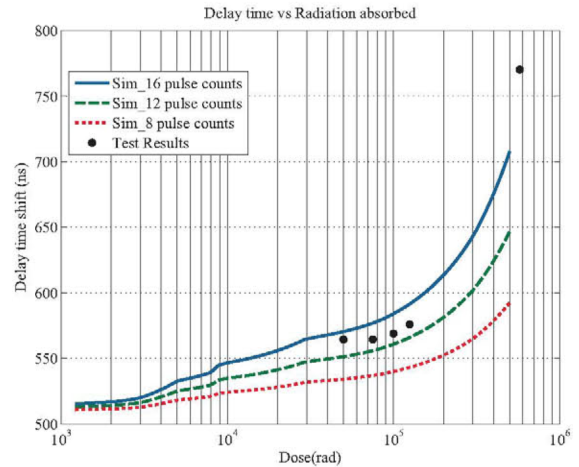


Fig. 7. Radiation Sensor Sensitive curve.

Seven DUTs were fabricated and six of them were inserted in a home-made breadboard and irradiated. The other DUT (DUT7) was treated as a golden copy to compare radiation effects versus normal configuration. Out of the six irradiated chips, half of them were biased (DUT2, DUT3 and DUT6) and the other half were unbiased (DUT1, DUT4 and DUT5). This choice was made to visualize if biasing had any effect on radiation absorption, we were expecting that unbiased chips were less altered by radiation effects [7].

Figure 4 (a) shows the board setup for the irradiation test. A water-sealed cylinder was introduced into a radiation controlled environment where it was disposed for the period needed to absorb the target radiation. Our test plan consisted of 6 different steps with a dose rate of 26.51krad/h. The first step was at minute 113 from the beginning, next four steps were separated 56 minutes and the final step last 16 hours. For the final step all DUTs were removed except DUT2 and DUT5 (first biased and second unbiased). So the absorbed radiation in these steps was 50 krad, 75 krad, 100 krad, 125 krad, 150 krad and 575 krad.

Figure 4 (b) provides a closer look to the DUTs disposition. The DUTs were biased at 3.3V with a current limit of 150mA, by an Ethernet cable though an RJ45 interface. All experiments were carried out at constant temperature (24°C in the pool and 28°C at room). The setup does not allow to execute on-line measurements, hence, to perform the measure at each step, the breadboard has to be extracted from the cylinder.

The measurement is accomplished following the scheme of Figure 5. Each DUT is measured independently using a Xilinx FPGA board (Virtex5 ML505), an Agilent MSO9051 oscilloscope, a developed test board and a PC. The FPGA board acts as the external control that excites the inputs of the sensor, the oscilloscope captures the input $Start$ and the output $Done$ and measures its delay, the test board routes all signals to the DUT and produces the oscilloscope inputs and the computer is used for device configuration and data acquisition.

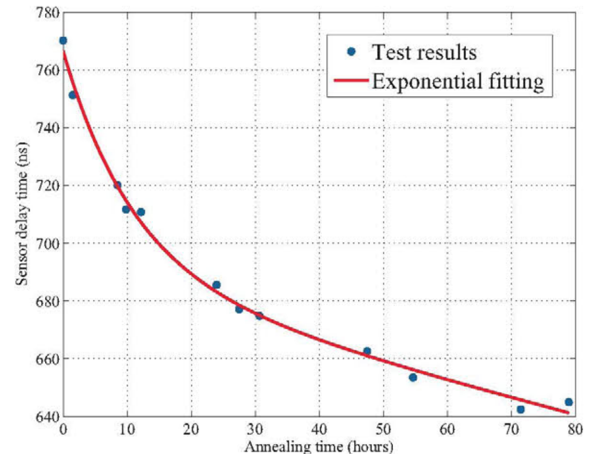


Fig. 8. Anneling along time in DUT2.

## IV. Experimental Results

Figure 6 summarizes the whole bunch of tests we carried out. In this figure green lines represent the sensor's $Start$ signal. And the rest of colored lines are the $Done$ signal at the different steps of the radiation test. $Start$ signal is delayed 500 ns from its real value to get more accuracy in the oscilloscope setup. The main conclusion at first sight is that DUTs 1,4 and 5 have been almost unaffected by radiation effects because they stayed unbiased along the test. DUT2 is widely the most affected DUT because it is the only biased one that remained in the $^{60}Co$ chamber during the last step. The differences in delay between the first measurements of each chip are due to process variations.

Next results are refered just to DUT2, considering this DUT as the only sensor with representative radiation results because it was exposed for a long enough period of time. Figure 7 plots the characteristic points of the sensor during the irradiation. This figure also compares theoretical curves of

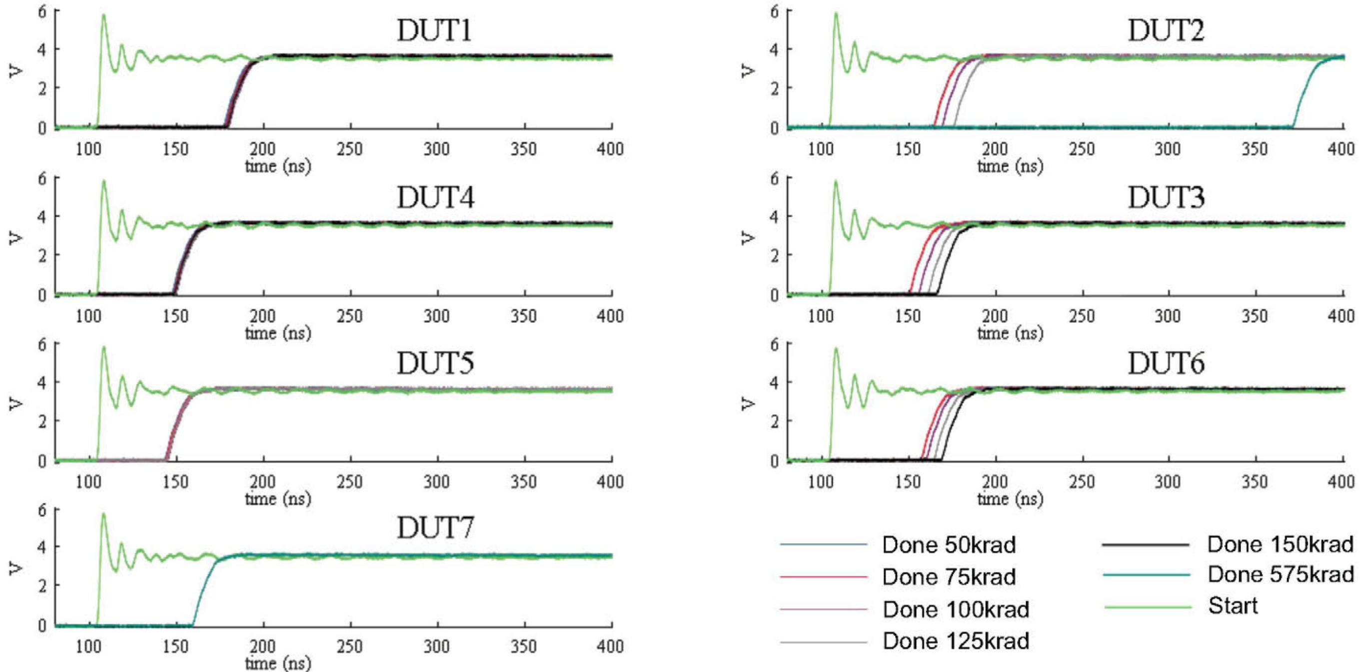


Fig. 6. Radiation results for every DUT at different radiation dose. *Start* signal is delayed 500ns.

the sensor with the results achieved after the test for different counter configurations. The theoretical curve is the result of the analysis of Vt variations impact on delay path with the Vt shift produced by radiation. Beyond its accuracy, the form of the curve fits substantially. We should recall that our sensor implements a sixteen cycle counter.

Figure 8 is the result of periodic measurements of the delay of DUT2 once radiation test is over. As can be seen, the annealing takes place because of charge redistribution. The exponential curve is a good approximation for how this effect behaves in our sensor.

## V. Conclusion

In this work a total ionization dose sensor has been designed, manufactured, irradiated and characterized. It is a digital CMOS sensor based on the relationship between accumulated radiation and performance degradation of transistors. Following this idea, a simple delay chain is used as sensing part, providing configurable sensitivity that allows to use this device for a wide range of radiation doses. Radiation mitigation techniques have been used to harden the remaining sensor blocks. The sensor interface allows its easy integration in other on-chip monitoring infrastructures.

Extensive experimental tests have been carried out to fully characterize the proposed sensor. In the irradiation tests biased DUTs have shown a response that matches well their expected behavior with radiation. On the other hand, we have seen how unbiased sensors were almost immune to TID effects. Finally, charge redistribution has been also observed after radiation test what supports the possibility of implementing dynamic recovery systems.

## Acknowledgment

The authors wish to thank C. Benito, E. Pun and D. González from Arquimea for their support and expertise when designing the test chips. Special thanks also go to S. Ibarmia and S. Esteve for their valuable help in defining the irradiation tests.

## References

[1] Holmes-Siedle, A. (1974). The space-charge dosimeter: General principles of a new method of radiation detection. Nuclear Instruments and Methods, 121(1), 169-179.

[2] G. Sarrabayrouse, D. Buchdahl, V. Polischuk, S. Siskos, Stacked-MOS ionizing radiation dosimeters: potentials and limitations, Radiation Physics and Chemistry, Volume 71, Issues 34, OctoberNovember 2004, Pages 737-739.

[3] Osuna CG, Ituero P, Lpez-Vallejo M. A Self-Timed Multipurpose Delay Sensor for Field Programmable Gate Arrays (FPGAs). Sensors. 2014; 14(1):129-143.

[4] Ituero, P., Lopez-Vallejo, M., Marcos, M. A. S. and Osuna, C. G. (2012). Light-weight on-chip monitoring network for dynamic adaptation and calibration. Sensors Journal, IEEE, 12(6), 1736-1745.

[5] Barnaby, H.J., "Total-Ionizing-Dose Effects in Modern CMOS Technologies," Nuclear Science, IEEE Transactions on , vol.53, no.6, pp.3103,3121, Dec. 2006.

[6] Giraldo, A., Paccagnella, A. and Minzoni, A. (2000). Aspect ratio calculation in n-channel MOSFETs with a gate-enclosed layout. Solid-State Electronics, 44(6), 981-989.

[7] Shaneyfelt, M.R.; Schwank, J.R.; Dodd, P.E.; Felix, J.A, "Total Ionizing Dose and Single Event Effects Hardness Assurance Qualification Issues for Microelectronics," Nuclear Science, IEEE Transactions on , vol.55, no.4, pp.1926,1946, Aug. 2008.