Energy-Based switches losses model for the optimization of PwrSoC buck converter

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***Abstract*— Current trends in automotive industry impose as main drivers the improvement of the efficiency and the miniaturization of the electronic systems. New technologies for passives enable the integration of inductor based power converter together with the load in a single chip. Due to the complexity of the system and various constraints, multi-variable optimization needs to be employed. This study presents an energy-based piece-wise linear model for switches losses estimation for 40 nm automotive approved semiconductor technology used for implementation of PwrSoC buck converter system. The model, based on discrete number of calculations performed with Spice simulations, is presented in detail in this study and it is validated experimentally.**

Keywords—Switching losses; Energy based model; PwrSoC system

I. INTRODUCTION

Current trends in automotive industry [1] show significant increase of car electronics, shifting the functionality form mechanical to electrical systems. According to this study, during the period 1993-2008, vehicle production has increased by 44%, while the automotive electronic content has grown by 155% and the semiconductor content by 325%. These growing trends impose efficiency and miniaturization as main drivers for power supply system due to the mass and CO_2 reduction. On the other hand, different studies of the trends in power electronics [2]-[6] show that significant effort is invested in integration and miniaturization of the power system. Special effort is given to the implementation of the passives [7]-[11] and improvement of the semiconductor design and models for losses estimation [12]-[16].

Having in mind these trends, the work presented in this paper is part of a project that proposes a fully integrated solution for an automotive power supply chain from the battery to the microcontroller. The system, presented in Fig. 1, is composed of the power converter and a load. The power converter can be implemented as a single stage solution or multistage, adapting the semiconductor technology depending on the selected solution. In order to optimize the power converter a multi-variable optimization needs to be employed. Further, to reduce the computational effort of the optimization, analytical models, implemented in the algorithm, need to have small computational cost and to have relatively good accuracy. Independently of the topology considered as the possible solution, losses estimation of the passives as well of the power switches is crucial part of the algorithm.

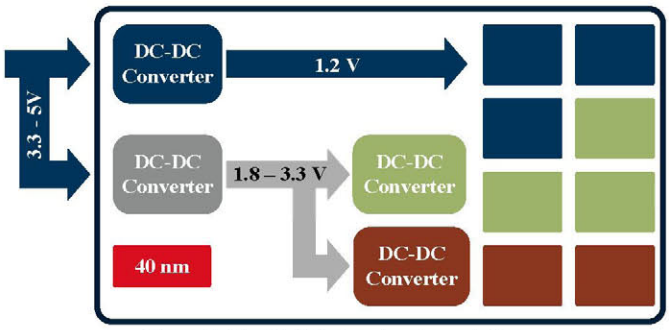

Figure 1: PwrSoC System implementation.

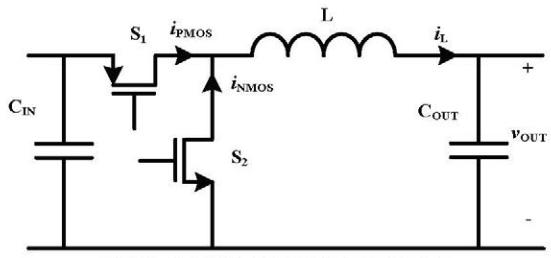

Figure 2: Single Phase Buck converter.

In this paper, the energy-based analytical model for switches losses estimation is presented. The model is based on discrete number of accurate calculations performed with Spice simulations for each losses component of the switch. Using those calculations, interpolated piece-wise linear functions are constructed allowing the estimation of the losses for all points which are belonging to the input domain of the model. In the first part of the paper, the analysis of power-switch losses components is presented on a buck converter example followed by the second part where the methods how to measure them are presented. The third part is dedicated to Energy-based model. Finally, the fourth part shows the validation of the model on the single-phase buck converter with lossless passives in various operation conditions.

II. BUCK CONCVERTER SWITCHING LOSSES

For the buck converter, shown in Fig. 2, where the high-side switch is implemented with PMOS and the low-side with NMOS, corresponding current waveforms in CCM are presented in Fig. 3. The losses of this switching structure can be divided in conduction losses and switching losses. The conduction losses are proportional to the on-resistance and the square value of the RMS currents. Assuming that for a given application and semiconductor technology, an input voltage, V_{IN}, and minimal lengths of both PMOS and NMOS are

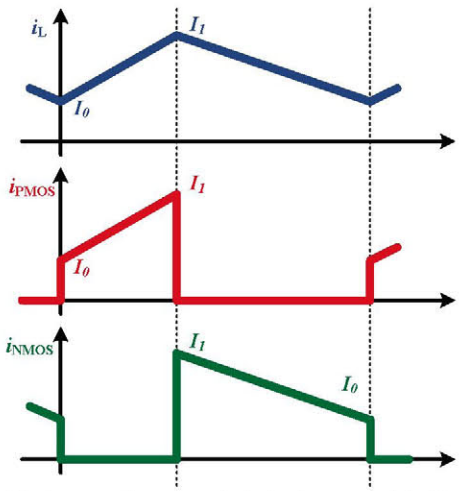

Figure 3: Buck converter currents: inductor current i_L (blue), PMOS current i_{PMOS} (red) and NMOS current i_{NMOS} (green)

selected, the on-resistances depend on the widths of the MOSFETs (w_P and w_N), applied gate-to-source voltages (V_{GSP} and V_{GSN}) and the average currents during the conduction time which are equal, for the case of CCM, to the average inductor current i_L. Having this into account, the conduction losses can be calculated using equations presented in Table I, where R_{PMOS} and R_{NMOS} are on-resistance calculation functions of PMOS and NMOS, respectively, and $I_{PmosRMS}$ and $I_{NmosRMS}$ are PMOS and NMOS RMS currents.

Further, switching losses can be calculated by firstly estimating the energy loss. For the PMOS switch, since it is operating with hard switching, the switching losses can be divided into driving, turn-on and turn-off losses. The turn-on energy loss occurs at the beginning of the cycle and it depends on instantaneous inductor current I_0, the width of the PMOS w_P and input voltage. As stated before, since the input voltage is fixed, it can be omitted into the model, thus degrading the dependence to only two variables (w_P and I_0). Similarly, the turn-off energy loss, which occurs at the end of the on-time, also depends on instantaneous inductor current I_1 and the width of the PMOS w_P, assuming that the input voltage has been incorporated into the model. The final component of the PMOS switching losses is the driving loss which is occurring at the beginning of the cycle. The driving energy loss can be estimated as the product of the charge needed to turn-on the device and the driving voltage. Once again, the needed charge is depending on the width w_P, instantaneous current I_0 and the driving voltage V_{GSP}.

On the other hand, since the low-side NMOS is operating with ZVS, the switching losses can be divided into the driving loss, the body-diode conduction losses and the reverse-recovery of the body-diode. Similarly as for the PMOS, the driving energy loss, which is occurring at time instance DT_{SW}, can be calculated as a product of the charge and the driving voltage V_{GSN}. The charge is dependent on the width w_N, instantaneous current I_1 and the driving voltage V_{GSN}. The energy losses of the body-diode conduction are occurring at the beginning of the cycle as well at the time instance DT_{SW}, and they can be calculated as a product of the voltage drop of the diode, instantaneous currents (I_0 and I_1) and the duration of the dead times (t_{dead_N2P} and t_{dead_P2N}). The voltage drop is

TABLE I. CALCULATION OF SEMICONDUCTOR LOSSES

Losses component	Time instance	Equation
P_{PMOS_Cond}	-	$R_{PMOS}(w_P, V_{GSP}, I_L) \cdot I_{PmosRMS}^2$
$P_{PMOS\_turn\_on}$	0, (T_{SW})	$E_{PMOSturn\text{-}on}(w_P, I_0) \cdot f_{SW}$
$P_{PMOS\_turn\_off}$	DT_{SW}	$E_{PMOSturn\text{-}off}(w_P, I_1) \cdot f_{SW}$
P_{PMOS_gate}	0, (T_{SW})	$Q_{PMOS}(V_{GSP}, w_P, I_0) \cdot V_{GSP} \cdot f_{SW}$
P_{NMOS_Cond}	-	$R_{NMOS}(w_N, V_{GSN}, I_L) \cdot I_{NmosRMS}^2$
P_{NMOS_gate}	DT_{SW}	$Q_{NMOS}(V_{GSN}, w_N, I_1) \cdot V_{GSN} \cdot f_{SW}$
$P_{NMOS\_rev\_rec}$	0, (T_{SW})	$E_{Nrev\text{-}rec}(w_N, I_0) \cdot f_{SW}$
P_{Ndiode_N2P}	0, (T_{SW})	$I_0 \cdot V_{D\text{-}NMOS}(w_N, I_0) \cdot f_{SW} \cdot t_{dead\_N2P}$
P_{Ndiode_P2N}	DT_{SW}	$I_1 \cdot V_{D\text{-}NMOS}(w_N, I_1) \cdot f_{SW} \cdot t_{dead\_P2N}$

proportional to the corresponding currents and the width of NMOS. Characterizing all the functions of the model, the total losses can be calculated using equations presented in Table I.

III. ENERGY LOSSES CALCULATIONS

As mentioned before, the energy-based model, presented in this paper, is built using discrete number of calculations for each energy loss component obtained from Cadence® software. The computations are performed by sweeping the variables of the measured function (w and I and v_{GS}, if needed). In Fig. 4 circuits which are used to characterize MOSFETs are presented. The circuit in Fig. 4a) is used to compute on-resistance of the PMOS. The sweeps of the MOSFET width w_P[n], load current I_{LOAD}[k] and gate to source voltage v_{GS}[m], are performed. Finally, by measuring source to drain voltage drop v_{SD}, the on resistance is calculated and the dependence R_{PMOS} (w_P[n], V_{GS}[m], I_{LOAD}[k]) is obtained. Similarly, the circuit in Fig. 4b) is used to obtain the on-resistance of the NMOS, obtaining R_{NMOS} (w_N[n], V_{GS}[m], I_{LOAD}[k]). The circuit in Fig. 4c) is used to measure NMOS body-diode voltage drop. The sweep of the MOSFET width w_N[n] and load current I_{LOAD}[k] is performed, while the gate is connected to the source via small resistance R_G, which is emulating driver output resistance. Finally, the dependence $V_{D\text{-}NMOS}$ (w_N[n], I_{LOAD}[k]) is obtained.

Using circuits from Fig. 4a-c the static characteristics are obtained. On the other hand, the circuits from Fig. 4d-f are used to obtain the dynamic characteristics. To perform the Spice calculations, the driver is modeled as current source injecting a constant current during the transient. The circuit in Fig. 4d) is used to calculate both turn-on and turn-off energy loss and gate charge. The turn-on energy loss calculation and gate-charge calculation are presented in Fig. 5 for the load current of 280 mA, PMOS width of 8mm and 5 V input voltage V_{IN}. A single switch action is performed. Initially, the PMOS is turned-off and the ideal diode is carrying the load current while the PMOS is blocking the input voltage. At the time instant t_0, driver current saturates to maximal value I_{DR} (80mA for presented case) and gate-to-source voltage v_{GS} starts to decrease. When the PMOS current i_{SD} reaches the load current, source-to-drain voltage v_{SD} starts to reduce up to the voltage drop defined with the product of on resistance and the load current at moment t_1. On the other hand, gate to source

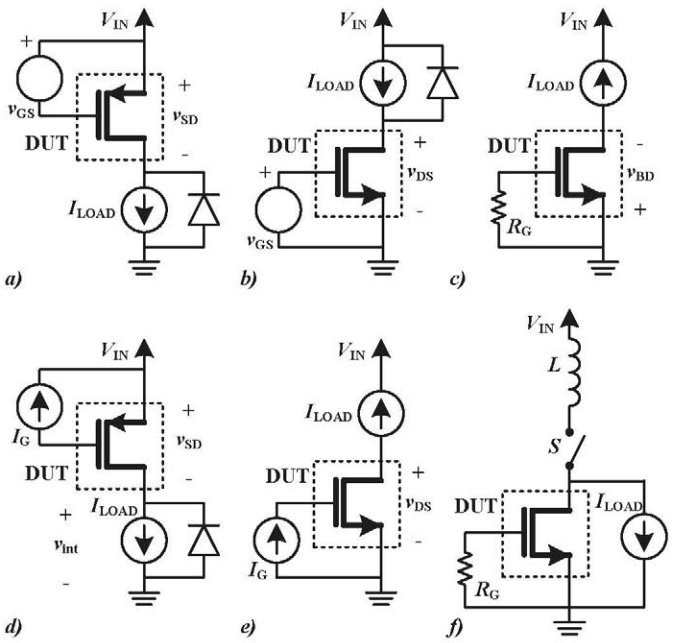

Figure 4: Circuits for characterizing MOSFETs: *a*) PMOS on resistance, R_{PMOS} (w_P, V_{GSP} , I_{LOAD}), *b*) NMOS on resistance, R_{NMOS} (w_N, V_{GSN} , I_{LOAD}), *c*) NMOS body-diode voltage drop, $V_{D\,NMOS}$ (w_N, I_{LOAD}), *d*) PMOS turn-on, $E_{PMOSturn\text{-}on}$(w_P, I_{LOAD}), and turn-off, $E_{PMOSturn\text{-}off}$(w_P, I_{LOAD}), energy loss and driving gate charge, Q_{PMOS}(V_{GSP}, w_P, I_{LOAD}), *e*) NMOS driving gate charge, Q_{NMOS}(V_{GSN}, w_N, I_{LOAD}), and *f*) NMOS body-diode reverse recovery energy loss, $E_{Nrev\text{-}rec}$(w_N, I_{LOAD}).

voltage continues to decrease up to the targeted value V_{GSP} which it reaches at time instance t_2. The product of the PMOS current i_{SD} and source-to-drain voltage v_{SD} is instantaneous power loss p_{SD}. Integrating the power loss p_{SD} from t_0 to t_1, turn-on energy loss is calculated for a given PMOS width and instantaneous current and $E_{PMOSturn\text{-}on}(w_P[n], I_{LOAD}[k])$ energy dependence is obtained. Similarly, integrating the gate current i_G from 0 to t2, the gate charge $Q_{PMOS}(V_{GS}[m], w_P[n], I_{LOAD}[k])$ dependence is obtained for the same PMOS width and the load current I_{LOAD} and driving voltage V_{GSP}. In a similar manner, using the same circuit, the turn-off energy characteristic $E_{PMOSturn\text{-}off}(w_P[n], I_{LOAD}[k])$ is calculated. Further, using the circuit in Fig. 4e), the NMOS gate-charge dependence is obtained. Initially, the NMOS is turned off and the body-diode carries the entire load current. Once again, the gate current is saturated at it maximal value I_G at moment t_0 and the gate to source voltage starts to increase. Since the NMOS is turned-on with small drain to source voltage (determined by body-diode voltage drop), it can be assumed that the switching is nearly lossless (ZVS is achieved). When the gate to source voltage reaches targeted value V_{GSN} at t_2, the transient is finished and the gate charge is calculated by integrating the gate current from t_0 up to t_2. Finally, the gate-charge dependence $Q_{NMOS}(V_{GSN}[m], w_N[n], I_{LOAD}[k])$ is obtained. The circuit in Fig. 4f) is used to calculate reverse-recovery energy loss of the NMOS body diode. Once again, the NMOS is turned-off since the gate is connected to the source via small resistance R_G. Initially, all the current is carried by the body-diode. At time t_0 the ideal switch is turned-on, imposing positive voltage at the drain, thus turning-off the body diode. The inductance L is used to limit the slew-rate of the body-diode current and it

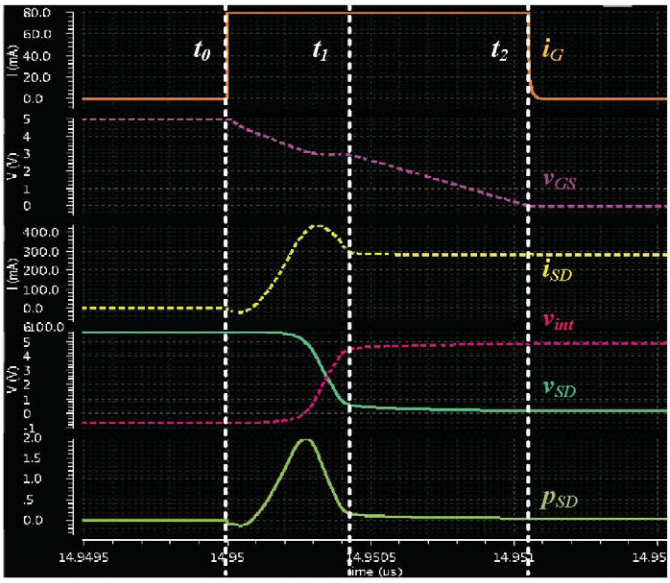

Figure 5: Spice simulation – PMOS turn-on energy loss and gate charge calculation: gate current i_G (orange, solid), PMOS gate to source voltage v_{GS} (violet, dotted), PMOS source to drain current i_{SD} (yellow, dotted), intermediate voltage v_{int} (red, dotted), PMOS source to drain voltage v_{SD} (dark green, solid) and PMOS source to drain power loss p_{SD} (light green, solid).

should be selected based on the slew-rate of the PMOS source to drain current from simulations performed with the circuit from Fig. 4d). When inductor current reaches load current at t_1, the body-diode enters in reverse recovery mode, creating energy loss. The transient is finished at t_2 when the diode current returns to zero. Integrating the product of the body-diode current and the voltage from t_0 to t_2, the reverse-recovery energy dependence $E_{Nrev\text{-}rec}(w_N[n], I_{LOAD}[k])$ is obtained.

IV. Energy-Based Model

As shown in chapter II, in order to calculate the losses of the switching structure it is necessary to model nine functions, which are presented in Table I. Most of the functions are defined with two input variables (the width w and the current I) and they are based on a finite number of calculation. In the case that the dependence Y is defined with three variables (e.g. R_{NMOS} (w_N, V_{GS}, I)), the gate to source voltage is declared as parameter and interpolation is performed, once again with the width w and current I. In order to perform interpolation between those Spice calculations, a model has been derived using piece-wise linear planes providing continuity of the estimation. The generation of the model is presented in Fig. 6. The interpolation is crucial for the usage of the model in order to obtain continues dependence while maintaining the derivative tendencies.

In general, the obtained results can be defined as Y(w[i], I[j]), where Y is the calculated value (energy, charge or resistance) and w[i] and I[j] represent input variables of the modeling function. Both of the input variables are arrays where i and j are indexes of the corresponding array, and they can have values from 1 to N+1 and 1 to M+1, respectively. Therefore, in the rest of the paper the series w[i] and I[j] will be noted as w_i and I_j, while Y(w[i], I[j]) will be noted as $Y_{i,j}$.

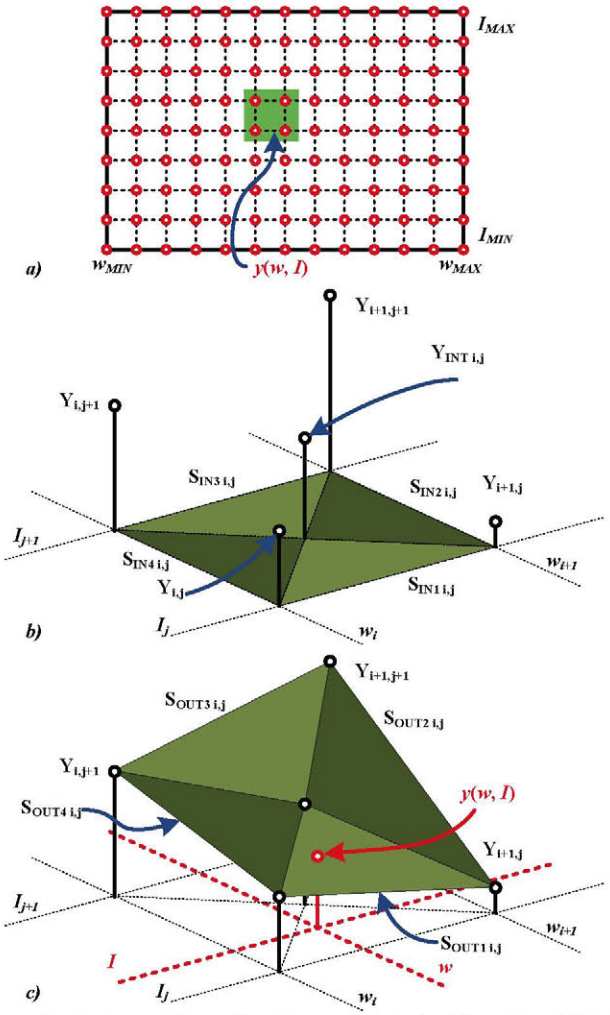

Figure 5: Basic modeling cell: a) Input plain defined by *w*[i] and *I*[j]; b) interpolation between four input points, input sub-domains, intermediate point $Y_{INT\ i,j}$; and c) the output plains and calculation of *y*(*w*,*I*)

As mentioned above, in order to interpolate the output plane, for each four values of the output, $Y_{i,j}$, $Y_{i+1,j}$, $Y_{i,j+1}$ and $Y_{i+1,j+1}$, with their corresponding input coordinates, (w_i, I_j), (w_{i+1}, I_j), (w_i, I_{j+1}) and (w_{i+1}, I_{j+1}), firstly, additional point $Y_{INTi,j}$ has been added as presented in Fig. 6b). The additional point value is defined by

$$Y_{INT\ i,j} = \frac{Y_{i,j} + Y_{i+1,j} + Y_{i,j+1} + Y_{i+1,j+1}}{4}, \quad (1)$$

while its input coordinates ($w_{INT\ i}$, $I_{INT\ j}$) are

$$w_{INT\ i} = \frac{w_i + w_{i+1}}{2}$$
$$I_{INT\ j} = \frac{I_{2j} + I_{j+1}}{2}. \quad (2)$$

Using additional point $Y_{INTi,j}$, the output plain has been interpolated using four linear plains defined by the additional and two extreme points, while the input domain has been equally divided in to its corresponding sub domains. In other words, the input sub-planes are defined by

$$\begin{aligned} S_{IN1i,j} &: (w_i, I_j), (w_{i+1}, I_j), (w_{INT\ i}, I_{INT\ j}) \\ S_{IN2i,j} &: (w_{i+1}, I_j), (w_{i+1}, I_{j+1}), (w_{INT\ i}, I_{INT\ j}) \\ S_{IN3i,j} &: (w_{i+1}, I_{j+1}), (w_i, I_{j+1}), (w_{INT\ i}, I_{INT\ j}) \\ S_{IN4i,j} &: (w_i, I_{j+1}), (w_i, I_j), (w_{INT\ i}, I_{INT\ j}) \end{aligned}, \quad (3)$$

and the input sub domains are related with theirs corresponding output planes

$$\begin{aligned} S_{IN1i,j} &\rightarrow S_{OUT1i,j} : Y_{i,j}, Y_{i+1,j}, Y_{INT\ i,j} \\ S_{IN2i,j} &\rightarrow S_{OUT2i,j} : Y_{i+1,j}, Y_{i+1,j+1}, Y_{INT\ i,j} \\ S_{IN3i,j} &\rightarrow S_{OUT3i,j} : Y_{i+1,j+1}, Y_{i,j+1}, Y_{INT\ i,j} \\ S_{IN4i,j} &\rightarrow S_{OUT4i,j} : Y_{i,j+1}, Y_{i,j}, Y_{INT\ i,j} \end{aligned}. \quad (4)$$

As mentioned, the output planes are linear functions of the input sub-domains, thus, for each point (*w*, *I*) of the corresponding input sub-domain, its output plain is defined by

$$\begin{aligned} (w,I) \in S_{IN1i,j} &\Rightarrow y_1(w,I) = a_{1i,j} w + b_{1i,j} I + c_{1i,j} \\ (w,I) \in S_{IN2i,j} &\Rightarrow y_2(w,I) = a_{2i,j} w + b_{2i,j} I + c_{2i,j} \\ (w,I) \in S_{IN3i,j} &\Rightarrow y_3(w,I) = a_{3i,j} w + b_{3i,j} I + c_{3i,j} \\ (w,I) \in S_{IN4i,j} &\Rightarrow y_4(w,I) = a_{4i,j} w + b_{4i,j} I + c_{4i,j} \end{aligned}, \quad (5)$$

where $a_{k\ i,j}$, $b_{k\ i,j}$ and $c_{k\ i,j}$ (k=1, 2, 3, 4) are constants obtained solving systems

$$\begin{aligned} a_{1i,j} w_i + b_{1i,j} I_j + c_{1i,j} &= Y_{i,j} \\ a_{1i,j} w_{i+1} + b_{1i,j} I_j + c_{1i,j} &= Y_{i+1,j} \\ a_{1i,j} w_{INT\ i} + b_{1i,j} I_{INT\ j} + c_{1i,j} &= Y_{INT\ i,j} \end{aligned}$$

$$\begin{aligned} a_{2i,j} w_{i+1} + b_{2i,j} I_j + c_{2i,j} &= Y_{i+1,j} \\ a_{2i,j} w_{i+1} + b_{2i,j} I_{j+1} + c_{2i,j} &= Y_{i+1,j+1} \\ a_{2i,j} w_{INT\ i} + b_{2i,j} I_{INT\ j} + c_{2i,j} &= Y_{INT\ i,j} \end{aligned}$$

$$\begin{aligned} a_{3i,j} w_{i+1} + b_{3i,j} I_{j+1} + c_{3i,j} &= Y_{i+1,j+1} \\ a_{3i,j} w_i + b_{3i,j} I_{j+1} + c_{3i,j} &= Y_{i,j+1} \\ a_{3i,j} w_{INT\ i} + b_{3i,j} I_{INT\ j} + c_{3i,j} &= Y_{INT\ i,j} \end{aligned} \quad (6)$$

$$\begin{aligned} a_{4i,j} w_i + b_{4i,j} I_{j+1} + c_{4i,j} &= Y_{i,j+1} \\ a_{4i,j} w_i + b_{4i,j} I_j + c_{4i,j} &= Y_{i,j} \\ a_{4i,j} w_{INT\ i} + b_{4i,j} I_{INT\ j} + c_{4i,jb} &= Y_{INT\ i,j} \end{aligned}$$

In order to calculate the output for input variables *w* and *I*, a three step procedure needs to be followed to use the model:

1. Find series indexes *i* and *j* which satisfy

$$\begin{aligned} w_i \le w < w_{i+1} \\ I_j \le I < I_{i+1} \end{aligned} \quad (7)$$

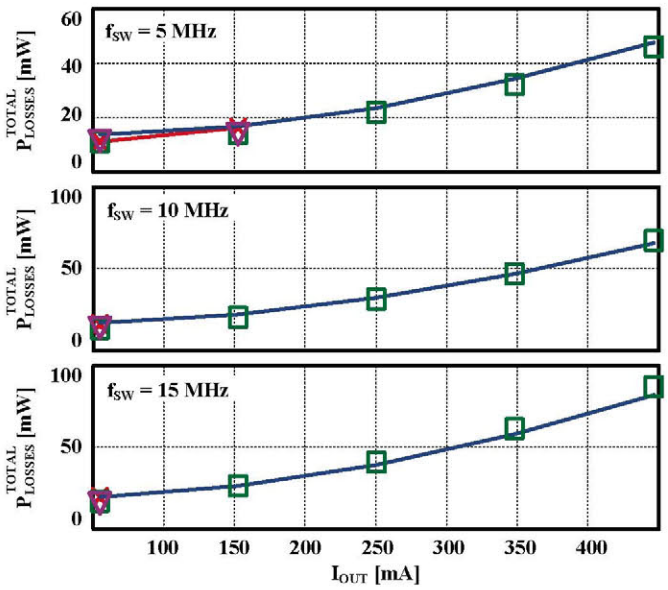

Figure 6: Total losses: Estimation of CCM (blue solid line) and DCM (red solid, x marker), Spice calculations CCM (green, square) and DCM (violet, triangle)

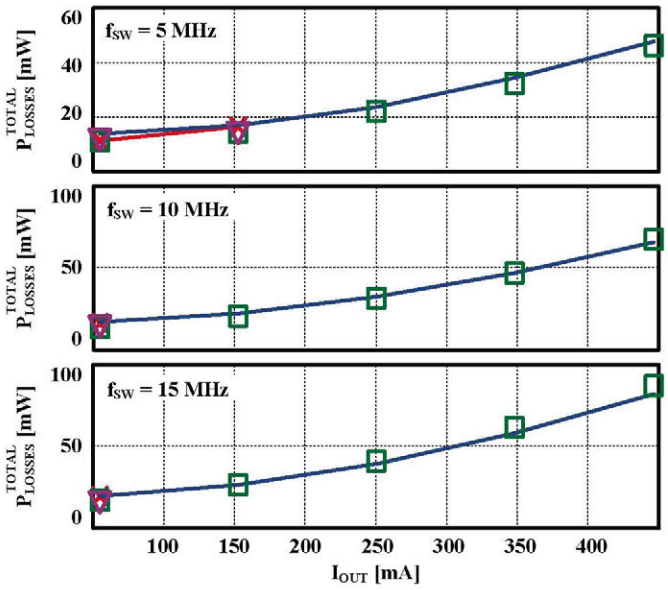

Figure 7: PMOS source to drain losses: Estimation of CCM (blue solid line) and DCM (red solid, x marker), Spice calculations CCM (green, square) and DCM (violet, triangle)

2. Determine the sub-domain in the input plain

$$(w, I) \in S_{INk\,i,j}, (k \in [1,4]) \tag{8}$$

3. Load corresponding coefficients $a_{k\,i,j}$, $b_{k\,i,j}$ and $c_{k\,i,j}$ from a look-up table and calculate the output using (5)

V. Results and Discussion

In this chapter, the validation of the model is presented. The model has been developed for an input voltage of 5 V, maximal driver current of 80 mA, driving voltage from 3V to 5V with a step of 0.5V, MOSFETs currents from 0 to 800mA

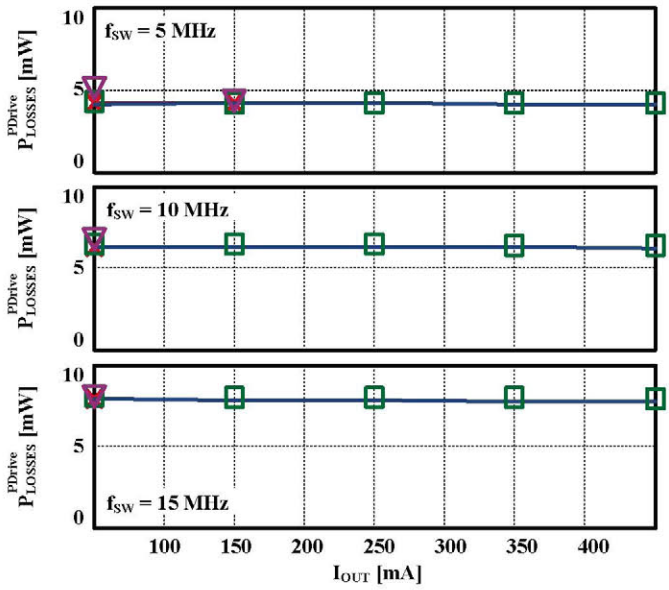

Figure 8: PMOS gate driving losses: Estimation of CCM (blue solid line) and DCM (red solid, x marker), Spice calculations CCM (green, square) and DCM (violet, triangle)

with a 100mA step, and MOSFETs widths from 2 mm up to 30mm with a step of 2 mm. The model is applied to calculate buck converter power losses using Cadence software as the reference simulation. The buck is converting 5 V to 1.2 V, the driving voltages are 5 V and it is designed with lossless output filter composed of 465 nH inductor and 800 nF output capacitor. The Spice calculations have been performed for three scenarios: in the first one the converter is switching at 5 MHz while the widths of both PMOS and NMOS are 16 mm; in the second, the converter is switching at 10 MHz while the widths of both PMOS and NMOS are 12 mm; and in the third the converter is switching at 15 MHz while the widths of both PMOS and NMOS are 10 mm.

The comparisons of the Spice calculations with the model estimation are presented in Fig. 6-10. In all figures, the losses calculated by the model in CCM operation are shown with the solid blue lined, while in DCM operation are presented with solid red lined with x marker. The Spice calculations are presented with green square marker for CCM operation and violet triangle for DCM operation. In Fig. 6 comparison of total losses of the converter are presented. It can be seen that the model predictions are in good agreement with obtained Spice calculations for both CCM and DCM operation. In Fig. 7 the drain to source PMOS losses (without the driving losses) are presented for all three scenarios, while the Fig. 8 shows PMOS driving losses. One again the Spice calculations are in good agreement with the estimations. Fig. 9 and Fig. 10 present the drain to source NMOS losses (without the driving losses) and NMOS driving losses are presented for all three scenarios respectively. Although the model predicts NMOS driving losses with relatively high accuracy, an error is present in NMOS drain to source losses due to the sensitivity of the model on estimated dead times (t_{dead_N2P} and t_{dead_P2N}). In addition, it is assumed that NMOS is switching with ZVS, which is not the case since prior to the switching, NMOS is blocking the body-diode voltage. As the switching frequency

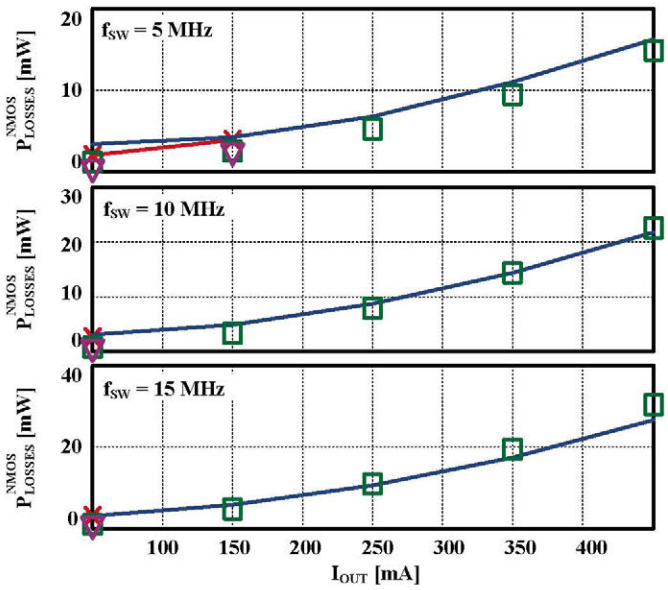

Figure 9: NMOS source to drain losses: Estimation of CCM (blue solid line) and DCM (red solid, x marker), Spice calculations CCM (green, square) and DCM (violet, triangle)

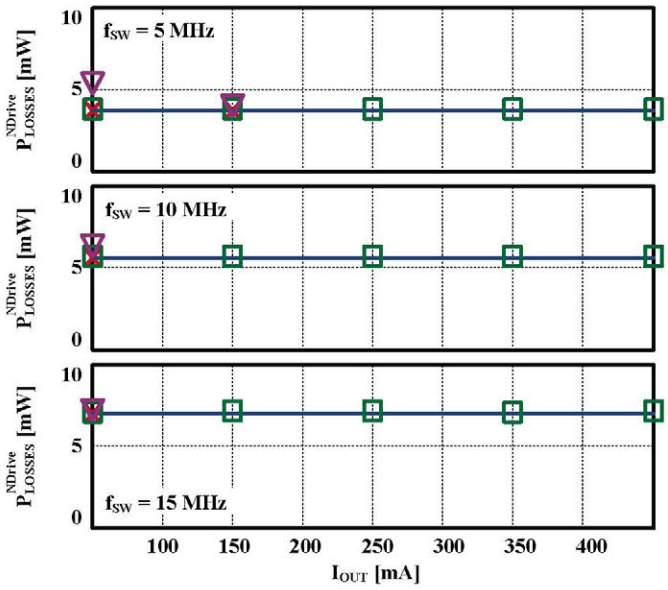

Figure 10: NMOS gate driving losses: Estimation of CCM (blue solid line) and DCM (red solid, x marker), Spice calculations CCM (green, square) and DCM (violet, triangle)

is increasing, those losses components have bigger influence on the error.

In the Table II statistical parameters are shown. It can be seen that maximal absolute error in total power loss estimation is 5.06 mW for the output power range from 60 mW to 600 mW and that standard deviation is 2.1 mW. The relative errors are normalized to the output power, giving the maximal relative error of 4.43%, while the relative standard deviation of the error is 1.89%. Regarding the losses components, PMOS losses are estimated with relatively high accuracy, obtaining for drain to source losses maximal error of 1.06 mW (1.4% relative) and standard deviation of 0.58 mW (0.5% relative), while driving losses have maximal error of 1.16 mW (1.94% relative) and standard deviation of 0.36 mW (0.54% relative). As shown previously, NMOS losses are exhibiting bigger error: for NMOS drain to source losses, maximal error is 3.87 mW (3.54%) and the standard deviation is 1.76 mW (1.87%), while for NMOS driving losses, the maximal error is 1.83 mW (3.06%) and standard deviation is 0.51 mW (0.81%).

TABLE II. ERRORS OF THE MODEL

	err_{AVR} [mW]	err_{MAX} [mW]	σ [mW]
P_{TOTAL}	1.7415	5.0624	2.1233
$P_{PMOStotal}$	0.4926	1.0661	0.5808
$P_{PMOSdrv}$	0.2485	1.1638	0.3561
$P_{NMOStotal}$	1.5711	3.8663	1.7554
$P_{NMOSdrv}$	0.2763	1.8347	0.5072
	err_{AVR}^{REL} [%]	err_{MAX}^{REL} [%]	σ^{REL} [%]
P_{TOTAL}	1.2524	4.4331	1.8998
$P_{PMOStotal}$	0.3603	1.4011	0.5074
$P_{PMOSdrv}$	0.2681	1.9397	0.5423
$P_{NMOStotal}$	1.33	3.5414	1.8655
$P_{NMOSdrv}$	0.3421	3.0578	0.8126

TABLE III. LOSSES BREAKDOWN FOR 5MHZ 250 MA

	Estimated [mW]	**Cadence** [mW]	**error** [mW]
P_{PMOS_Cond}	5.7		
$P_{PMOS\_turn\_on}$	0.19		
$P_{PMOS\_turn\_off}$	2.92		
P_{PMOS_total}	8.81	8.708	0.102
P_{PMOS_gate}	4.2	4.271	-0.071
P_{NMOS_Cond}	4.91		
$P_{NMOS\_rev\_rec}$	1.42		
P_{Ndiode_P2N}	1.45		
P_{Ndiode_N2P}	0.11		
P_{NMOS_total}	7.89	5.23	2.66
P_{PMOS_gate}	3.72	3.79	-0.07
$P_{LOSSESTotal}$	24.62	21.55	3.07

Table III shows breakdown of the losses for 5 MHz converter at 250 mA of output current, while Fig.11 shows the waveforms of the MOSFETs currents, inductor currents and NMOS drain-to-source voltage. Once again it can be seen that the model is predicting total losses with the small error of 3.07 mW at 300 mW of output power. Also it can be seen that the PMOS losses are estimated with small error: 102 μW for drain to source component and 71 μW for driving losses. Similarly, NMOS driving losses are estimated with 70 μW error. The main part of the total error originates for NMOS drain to source an error which is 2.66 mW or 86% of the total error.

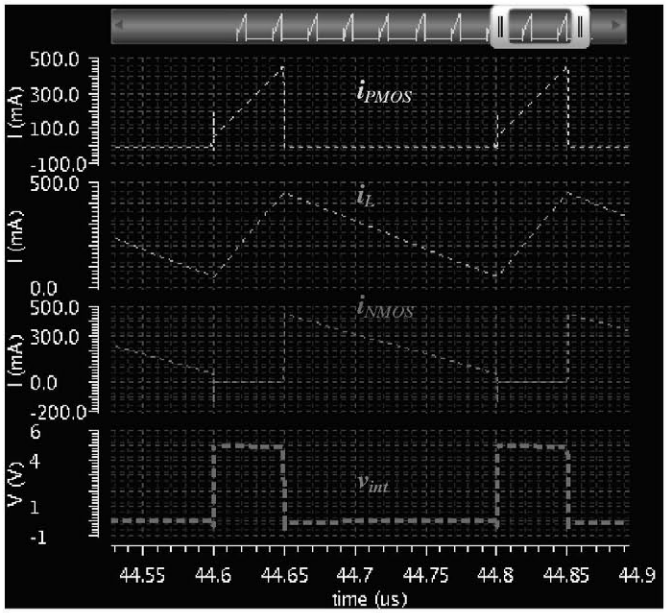

Figure 11: Buck converter waveforms: PMOS current (yellow), the inductor current (light blue), NMOS current (pink) and NMOS drain-to-source voltage (blue)

VI. CONCLUSIONS

In this study, the energy-based analytical model for power switch loss estimation is presented. The model is based on discrete number of calculations performed on Spice simulations for each loss component of the switch. The model takes into account all the losses contributions, allowing better optimization of the inductor based power converter of the PwrSoC system. As presented, the model is validated on a Buck converter with lossless output filter using Spice simulations for three scenarios. The calculated losses are in relatively good agreement with measured results, achieving maximal absolute error in the total power calculation of 5 mW while the average error and the standard deviation are 1.74 mW and 2.12 mW for the output power range from 60 mW up to 600 mW.

REFERENCES

[1] R. Ploss, A. Mueller and P. Leteinturier,"Solving automotive challenges with Electronics," in *IEEE International Symposium on VLSI Technology, Systems and Applications*, 2008. VLSI-TSA 2008, April 2008, pp. 1-2

[2] S. Musunuri, P. L. Chapman, Zou Jun, and Liu Chang, "Design issues for monolithic DC-DC converters," *IEEE Trans. Power Electron.*, vol. 20, no. 3, pp. 639–649, May 2005.

[3] T. Karnik, P. Hazucha, G. Schrom, F. Paillet, and D. Gardner, "Highfrequency DC-DC conversion: Fact or fiction," in *Proc. IEEE Int. Symp. Circuits Syst.*, Greece, May 2006, pp. 245–248.

[4] F. C. Lee and Q. Li, "High-Frequency Integrated Point-of-Load Converters: Overview", *IEEE Trans. Power Ele*ctron., vol. 28, no. 9, pp. 4127–4136, Sep. 2013.

[5] F. Waldron, R. Foley, J. Slowey, A. N. Alderman, B. C. Narveson and S. C. O'Mathuna, "Technology Roadmapping for Power Supply in Package (PSiP) and Power Supply on Chip (PwrSoC)", *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4137–4145, Sep. 2013.

[6] S. C. O'Mathuna, "Power supply on chip: Has the ship come in?" *plenary session presented at the 24th Annu. IEEE Applied Power Electronics Conf.*

[7] S. C. O'Mathuna, T. O'Donnell, N. Wang, and K. Rinne, "Magnetics on silicon: An enabling technology for power supply on chip," *IEEE Trans. Power Electron.*, vol. 20, no. 3, pp. 585–592, May 2005.

[8] T. M. Andersen, C. M. Zingerli, F. Krismer, J. W. Kolar, N. Wang and C. O. Mathuna, "Modeling and Pareto Optimization of Microfabricated Inductors for Power Supply on Chip", *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4422–4430, Sep. 2013

[9] T. O'Donnell, N. Wang, M. Brunet, S. Roy, A. Connell, J. Power, C. O'Mathuna, and P. McCloskey, "Thin film micro-transformers for future power conversion," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2004, pp. 939–944.

[10] T. O'Donnell, N. Wang, R. Meere, F. Rhen, S. Roy, D. O'Sullivan, and C. O'Mathuna, "Microfabricated inductors for 20 MHz Dc-Dc converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2008, pp. 689–693.

[11] F. Roozeboom, A. L. A. M. Kemmeren, J. F. C. Verhoeven, F. C. van den Heuvel, J. Klootwijk, H. Kretschman, T. Fric, E. C. E. van Grunsven, S. Bardy, C. Bunel, F. Chevrie, D. LeCornec, S. Ledain, F. Murray, and P. Philippe, "Passive and heterogeneous integration towards a Si-based system-in-package concept," *Thin Solid Films*, vol. 504, pp. 391–396, May 2006.

[12] S. Musunuri and P. L. Chapman, "Design of low power monolithic DCDC buck converter with integrated inductor," in *Proc. IEEE 36th Power Electron. Spec. Conf.*, Recife, Brasil, Jun. 16, 2005, pp. 1773–1779.

[13] S. Abedinpour, B. Bakkaloglu, and S. Kiaei, "A 65 MHZ switching rate, two-stage interleaved synchronous buck converter with fully integrated output filter," presented at the *IEEE Int. Symp. on Circuits Syst.*, Greece, May 2006.

[14] J. Hannon, D. O'Sullivan, R. Foley, J. Griffiths, K.G. McCarthy, and M.G. Egan, "Design and optimization of a high current, high frequency monolithic buck converter," in *Proc. 23rd Annu. IEEE Applied Power Electronics Conf. Expo.*, Austin, TX, Feb. 24–28, 2008, pp. 1472–1476.

[15] J. Hannon, R. Foley, J. Griffiths, D. O'Sullivan, K. G. McCarthy, and M. G. Egan, "A 20 MHz 200–500 mA monolithic buck converter for RF applications," in Proc. 24th Annu. *IEEE Applied Power Electron. Conf. Expo.*, Washington, D.C., Feb. 15–19, 2009, pp. 503–508.

[16] D. Díaz, M. Vasić, O. García, J.A. Oliver, P. Alou, J.A. Cobos, "Hybrid behavioral-analytical loss model for a high frequency and low load DC-DC buck converter," in *Proc. Energy Conversion Congress and Exposition (ECCE)*, 2012 IEEE, Sept., 2012, pp. 4288 - 4294.