Analysis of the effect of modulation delays on the size of the output capacitor

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Keywords

<<Converter Control>>, <<Pulse Width Modulation (PWM)>>, <<Integrated Circuit (IC)>>.

Abstract

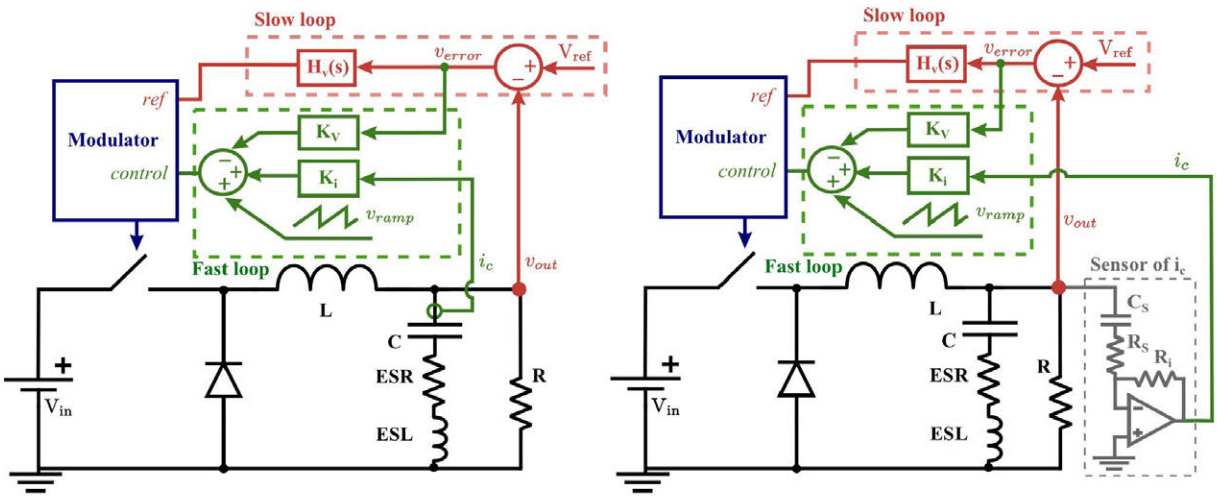
Constant frequency (PWM), constant on-time (COT) and constant off-time modulations exhibit inherent delays where the controller is unable to respond instantaneously. These delays can increase the required size of the output capacitor to meet dynamic requirements in applications with high demanding load such as the supply of microprocessors. This paper analyzes the minimum required output filter (output inductor and output capacitor) to meet a given specification and quantifies the effect that different modulations have in the minimum size of the output capacitor. The paper also shows a novel technique to mitigate the delays of the modulations by means of synchronizing the load step with the clock of the modulation. This technique is applicable to most of controllers as it only acts on the modulator

Introduction

Controls of power converters can be modulated in several ways such as constant frequency, constant on-time, constant off-time and hysteretic modulation.

Constant frequency modulation, also known as Pulse Width modulation (PWM), is the most widely applied. It forces a constant switching frequency and modulates the width of the duty cycle. On the other hand, constant on-time modulation (COT) is becoming more and more popular in the industry in applications with high demanding loads such as in Point of Load converters (PoL) [1, 2] thanks to its allegedly better dynamic performance and efficiency [3]. This modulation forces a constant on-time and modulates the off-time of the duty cycle. Hysteretic modulation is another increasingly used modulation for fast dynamic response [4, 5]. As opposed to the aforementioned, the hysteretic modulation does not have any time restrictions and modulates both the on-time and the off-time of the duty cycle.

Besides considerations of efficiency, the choice of the modulation is not trivial because it can have a significant impact in the worst-case voltage deviation under a load transient. If constant frequency, constant on-time or constant off-time are used, then, there might be instances where the control reacts to a disturbance with a delay. For example, if a loading transient occurs when the converter is in the off-time with constant switching frequency modulation, then the control needs to wait till the beginning of the next period to command an on-time because the modulation forces a constant period. The effect of this inherent delay of the modulation can be very dominant in the total voltage deviation and even shift the worst-case load transient from the unloading to the loading in applications with small duty cycle [6].



(a) Conceptual scheme (b) Implementation of capacitor current sensor

Figure 1: Control scheme of V^2I_c.

Therefore, the delays of the modulation affect the worst-case voltage deviation and, consequently, the minimum required size of the output capacitor to comply with dynamic requirements.

This paper studies the effect that different modulations have on the size of the output capacitor. It also shows a novel technique called "**C**lock **P**ulse **S**ynchronization" based on the capacitor current ($CPSI_c$) in order to counteract the limitations of the modulator [6].

The paper is structured as follows. The first section exemplifies the problematic with the control V^2I_c control modulated with constant switching frequency. The second section explains the effect in the deviation of the output voltage of the inherent delays of the modulator. The third section explains the proposed technique to overcome the limitations of the modulation and minimize the voltage deviation under load transients. The fourth section shows the experimental validation of the proposed technique and the last section summarizes the contributions of the article. The simulation results of the article are obtained from the program Simplis.

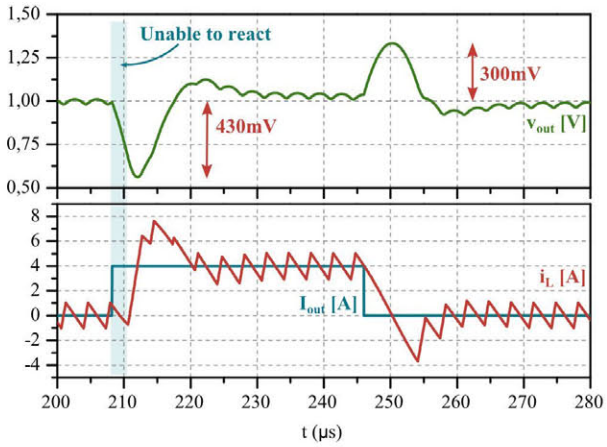
Exemplification of the delay in constant frequency modulation in a V^2I_c control

V^2I_c (fig.1a), proposed in [7], is a ripple-based control that presents a very fast dynamic response under load perturbations and reference voltage steps [8, 9]. It is composed by a slow loop, where the output voltage is regulated with a linear controller, and a fast loop, composed by the error of the output voltage and the current through the output capacitor. An optional artificial compensating ramp can be added in the fast loop in order to stabilize the converter.

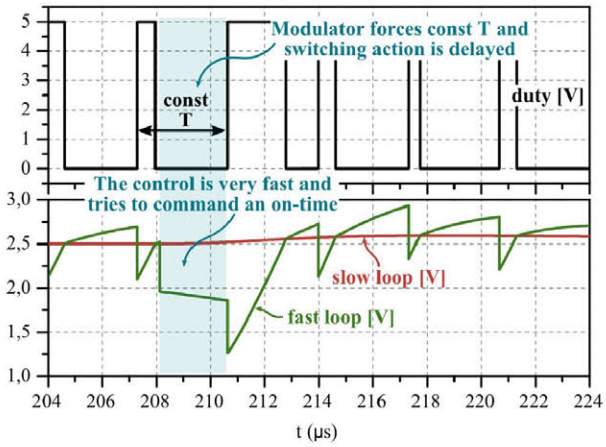
As the current through the output capacitor is the difference between the current through the inductor and the output current, the control exhibits inherently a feedforward of the load current. Whenever the load changes, this disturbance is reproduced in the current through the output capacitor which produces an almost instantaneous change in the control signal and in the duty cycle. This way, the control presents a very fast response under load perturbations. The error of the output voltage is also added in the fast loop and, consequently, a step in the reference voltage causes an instantaneous reaction in the control signal. Therefore, V^2I_c can be used in applications with reference voltage tracking such as in microprocessors with dynamic voltage scaling.

The current through the output capacitor is estimated with a trans-impedance amplifier [10] (fig.1b) in order not to increase the impedance of the capacitor. The current sensor is designed so that it behaves like an impedance proportional to the impedance of the output capacitor and, as a result, the measured current is proportional to the current through the output capacitor. Notice that the actual implementation of V^2I_c only needs to sense the output voltage.

The V^2I_c control is chosen to exemplify the problematic of the constant switching frequency modulation because it can achieve almost optimal responses under load disturbances. Therefore, the effect that the delay of the modulation has on the voltage deviation is more dominant. For the constant frequency modulation, if a positive load transient occurs during the off-time, the control is unable to react immediately because the on-time is synchronized with the clock and it cannot begin until the next period. This causes



(a) Output voltage deviation under a loading and an unloading transient.



(b) Control signals of the loading transient of (a). The slow loop signal and the fast loop signal that create the switching action are shown.

Figure 2: Load transient response of V^2I_c control with constant frequency modulation.

an additional drop of the output voltage that does not depend on the dynamic behavior of the control. For the constant on-time modulation, an additional overshoot of the output voltage, that is independent of the control, occurs if a negative load transient occurs during the constant on-time.

Fig.2 shows the worst-case load transients for positive load step and negative load step of a constant frequency V^2I_c peak control. First, notice that, for the unloading transient, the control commands a lengthy off-time so the deviation of the output voltage is the absolute minimum overshoot achievable for this power stage and it is $300mV$. On the other hand, when the positive load step occurs at the beginning of the off-state and the control is unable to react until the end of the period. When a new period starts, the control commands a lengthy on-time to recover from the drop of the output voltage. The drop of the output voltage for this loading transient is $430mV$. Fig.2b shows, for the delayed load transient response of fig.2a, the fast and the slow signals of the control that generate the switching action (in fig.1a, the slow loop and fast loop signals correspond to the *ref* and the *control* signals that enter the modulator, respectively). Notice that the fast loop signal immediately drops below the slow loop signal when the load disturbance occurs so that control is trying to command an on-time just after the perturbation. But the switching action is delayed until the end of the period because the modulator is forcing a constant switching frequency.

Fig.2 shows that V^2I_c control performs excellent and achieves the absolute minimum voltage deviation for the power stage and modulation. However, the larger drop is due to the constraint of the modulation, where the control is not able to command the power stage.

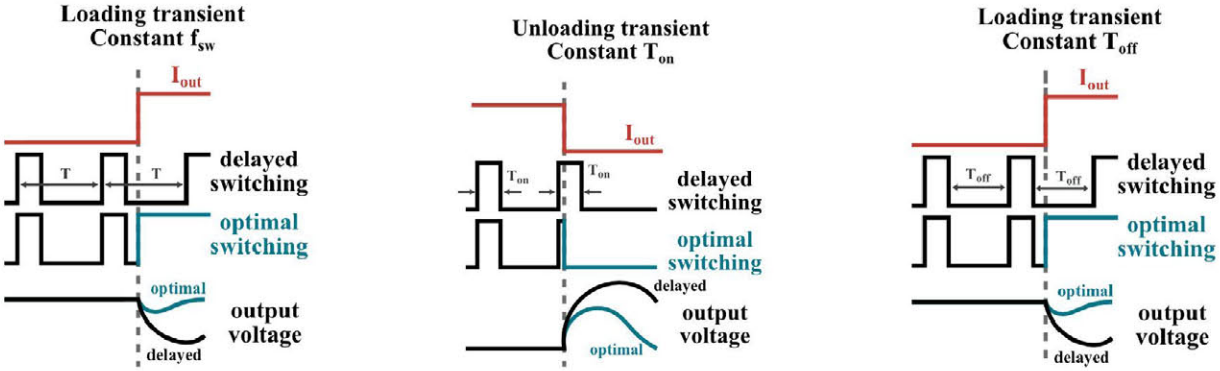
As a consequence of this inherent delay, the effectiveness of very fast controls, such as V^2I_c, is hindered by the delay of the modulation as this deviation of the output voltage is independent of the dynamic behavior of the control.

Effect in the size of the output capacitor of the inherent delays in the switching action of the modulators

Even an ideal instantaneous control cannot prevent a certain deviation of the output voltage under a load transient. For a Buck converter, the minimum deviation of the output voltage, $\triangle v_{o,load}^{min}$, is given by the equation (1).

$$\triangle v_{o,load}^{min} = \frac{1}{2C} \cdot \left((C \cdot ESR)^2 m_i + \frac{\triangle i_o^2}{m_i} \right) \tag{1}$$

where m_i is the slope of the inductor current and correspond to the positive slope for the case of the loading transient, $m_1 = (V_{in} - v_o)/L$, and the negative slope for the case of the unloading transient, $m_2 = v_o/L$. The other parameters are the load current step, $\triangle i_o$, the input voltage, V_{in}, the output voltage, v_o, the output filter inductor, L, and the output capacitor, C.



(a) Delayed switching action of constant frequency modulation.

(b) Delayed switching action of constant on-time modulation.

(c) Delayed switching action of constant off-time modulation.

Figure 3: Conceptual scheme of the delayed switching actions of different modulation techniques and comparison with the optimal switching action.

By analyzing the topology and equation (1), it is well-known [11]–[12] that the deviation of the output voltage under unloading transients is greater than under loading transients for Buck converters operating with a small duty cycle.

But these equations are derived assuming that the control is able to react instantaneously after the load transient. However, if constant on-time, constant off-time or constant switching frequency modulations are used, then, there are intrinsic delays that limit the effectiveness of the control. This is because there is an additional voltage deviation that is independent on how fast the control is.

Fig.3 illustrates these delays and compares the response of the modulation with the optimal response:

- In the case of constant frequency modulation (fig. 3a), this would be the case if a positive load step occurs during the off-state begins, as the control is not able to react until the end of the period. In order to overcome this problem, the clock needs to be synchronized with the load disturbance so that an on-time can occur just after the perturbation.
- In the case of constant T_{on} modulations (fig. 3b), the control is not able to react until the end of the constant on-time if a negative load step occurs during the on-state. In order to overcome this problem, the generation of the constant on-time needs to be reset so that an off-time can occur just after the perturbation.
- In the case of constant T_{off} modulations (fig. 3c), the control is not able to react until the end of the constant off-time if a positive load step occurs during the off-state. In order to overcome this problem, the generation of the constant off-time needs to be reset so that an on-time can occur just after the perturbation.
- On the other hand, it is important to point out that ideal hysteretic modulations, which modulate with variable switching frequency, do not exhibit this problem as these modulations do not have time restrictions.

Without considering the ESR and the ESL of the output capacitor, the additional drop of the output voltage due to a time delay is:

$$\triangle V_{delay} = \frac{1}{C}\left(\frac{1}{2}m_i \cdot t_d^2 - \frac{1}{2}\triangle i_L t_d + \triangle i_o t_d\right) \tag{2}$$

where t_d is the time delay, $\triangle i_L$ is the ripple of the inductor current in steady-state.

In constant frequency and constant off-time modulations, the worst-case is if the control is unable to respond during the whole off-time. Then, $t_d = T_{off} = (1-d)T$ and the additional drop of the output voltage is:

$$\triangle V_{delay} = \frac{1}{C}\left(\frac{1}{2}\frac{\triangle i_L}{(1-d)T}(1-d)^2T^2 - \frac{1}{2}\triangle i_L(1-d)T + \triangle i_o(1-d)T\right) = \frac{1}{C}\triangle i_o(1-d)T \tag{3}$$

Table I: Minimum voltage deviation for a loading transient, $\triangle v_{o,loading}^{min}$, and an unloading transient, $\triangle v_{o,unloading}^{min}$, for different modulations. The equations do not consider the ESR of the output capacitor.

Modulation	$\triangle \mathbf{v}_{\mathbf{o,loading}}^{\mathbf{min}}$	$\triangle \mathbf{v}_{\mathbf{o,unloading}}^{\mathbf{min}}$
Constant switching frequency (PWM)	$\frac{1}{C}\cdot\left(\triangle i_o(1-d)T+\frac{\triangle i_o^2}{2(V_{in}-v_o)}L\right)$	$\frac{1}{C}\cdot\frac{\triangle i_o^2}{2v_o}L$
Constant on-time (COT)	$\frac{1}{C}\cdot\frac{\triangle i_o^2}{2(V_{in}-v_o)}L$	$\frac{1}{C}\cdot\left(\triangle i_o dT+\frac{\triangle i_o^2}{2v_o}L\right)$
Constant off-time	$\frac{1}{C}\cdot\left(\triangle i_o(1-d)T+\frac{\triangle i_o^2}{2(V_{in}-v_o)}L\right)$	$\frac{1}{C}\cdot\frac{\triangle i_o^2}{2v_o}L$
Hysteretic / Without delay	$\frac{1}{C}\cdot\frac{\triangle i_o^2}{2(V_{in}-v_o)}L$	$\frac{1}{C}\cdot\frac{\triangle i_o^2}{2v_o}L$

In constant on-time modulation, the worst-case is if the control is unable to respond during the whole on-time. Then, $t_d = T_{on} = dT$ and the additional drop of the output voltage is:

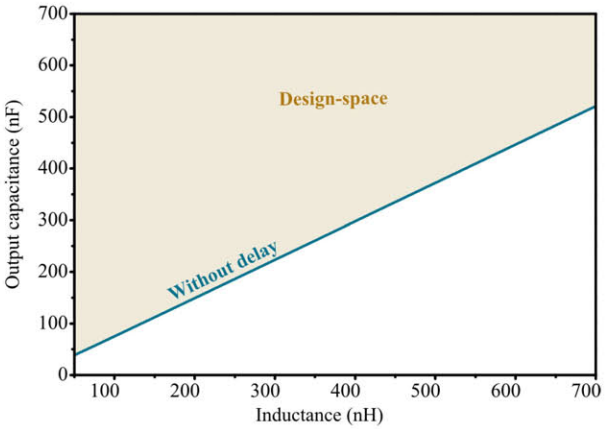
$$\triangle V_{delay} = \frac{1}{C}\left(\frac{1}{2}\frac{\triangle i_L}{dT}d^2T^2 - \frac{1}{2}\triangle i_L dT + \triangle i_o dT\right) = \frac{1}{C}\triangle i_o dT \tag{4}$$

Notice that, in both cases, the worst-case additional drop of the output voltage due to the delay does not depend on the inductor of the power stage.

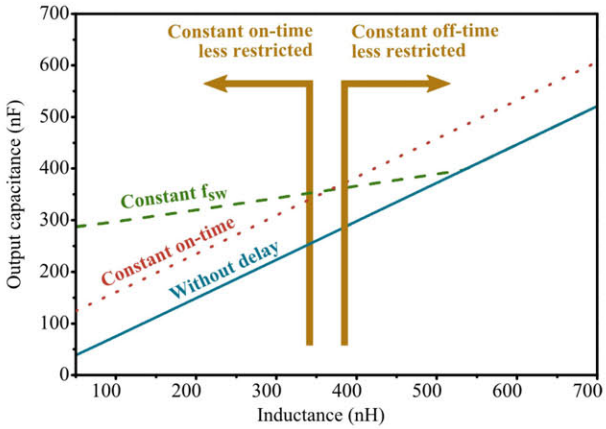
Table I shows the minimum voltage deviation for a loading transient and an unloading transient for different modulations taking into account the additional voltage drop due to the delay of the modulations.

Now, by studying table I, for small duty cycles and constant frequency modulation, the worst-case deviation of the output voltage could occur under the loading transient. In order to better study how the delays can affect the size of the output capacitor, figures 4 and 5 show the design space for the sizing of the inductor and the output capacitor. The parameters of the converter are $f_{sw} = 10\,\text{MHz}$, $V_{in} = 5V$, $v_{out} = 1.2V$, $i_{out} = 0A \sim 1A$, $L = 100nH$. The maximum allowed static ripple of the output voltage is $v_{out} \pm 30mV$ and the maximum allowed voltage deviation during a transient is $v_{out} \pm 100mV$.: .

- Figure 4a shows the design space for a switching frequency of 10 MHz and supposing that the modulation does not have a delay in the response. The upper orange area represents the L-C combination that can be designed in order to comply with the dynamic requirements for a load transient.
- Figure 4b shows the same graphic but superposing the design space for constant switching frequency and constant on-time modulations. Several important conclusions can be drawn from this figure:
  - By examining the design space for constant switching frequency modulation (green dotted line), notice that above 500nH of inductance, the design space matches the one for the modulation without delay. This is because, below $L = 500nH$, the worst-case voltage deviation is the loading transient (which exhibits the delay) and , above $L = 500nH$, the worst-case voltage deviation is the unloading transient. Therefore, the delay of constant switching frequency modulation does not affect the worst-case voltage deviation in the case of larger values of inductance.
  - On the other hand, the design space of the constant on-time is parallel to the one of the modulation without delay. This is because the additional voltage deviation caused by the delay adds up to the already larger voltage deviation which is the unloading transient in the case of applications of small duty cycle. Consequently, as opposed to constant switching frequency modulations, the delay of constant on-time modulation always increases the worst-case voltage deviation for these applications.
  - Lastly, notice also that around $L = 400nH$, the design spaces of the constant switching frequency and constant on-time modulations intersect. As a result, lower values of the inductance benefit constant on-time while greater values of inductance benefit constant switching frequency.
- Figures 5a and 5b show the design space of different modulations for switching frequencies of 5MHz and 20MHz, respectively. It can be seen that, obviously, lower switching frequencies incr

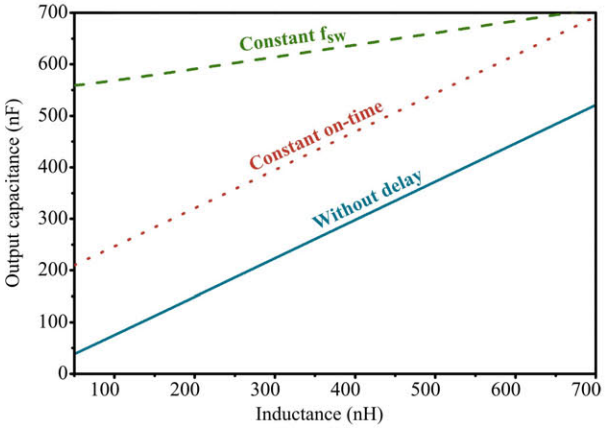


(a) Design space for a switching frequency of 10 MHz and a modulation without delay.

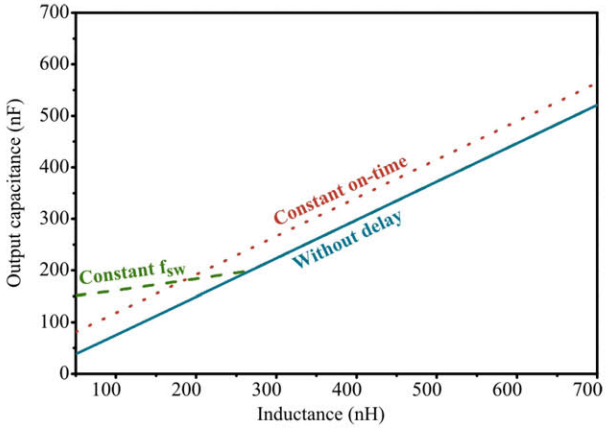


(b) Design space for a switching frequency of 10 MHz and for different modulations.

Figure 4: Conceptual scheme of the delayed switching actions of different modulation techniques and comparison with the optimal switching action for 10MHz.



(a) Design space for a switching frequency of 5 MHz and for different modulations.



(b) Design space for a switching frequency of 20 MHz and for different modulations.

Figure 5: Conceptual scheme of the delayed switching actions of different modulation techniques and comparison with the optimal switching action for 5MHz and 20MHz.

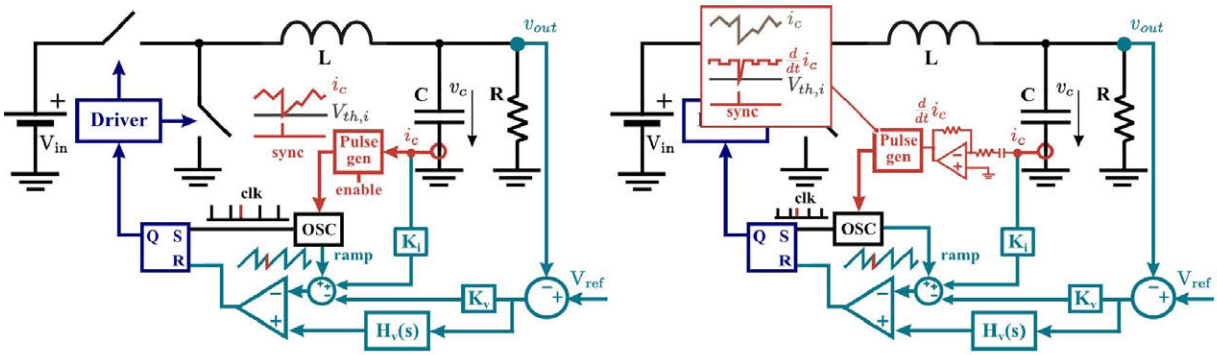
eases the delay of these modulations and, therefore, increases the minimum required output capacitor. Furthermore, by comparing the design spaces of constant switching frequency and constant on-time modulations, it is concluded that constant on-time can be preferable for lower switching frequencies because it exhibits less voltage deviation while constant switching frequency can be preferable for higher switching frequencies.

Clock Pulse Synchronization based on the capacitor current ($\mathbf{CPSI_c}$)

[6] proposes a novel technique called **C**lock **P**ulse **S**ynchronization" based on the capacitor current ($\mathrm{CPSI_c}$) that significantly reduces the delay in constant switching frequency modulation. Figure 6 shows the proposed technique applied to a V^2I_c control.

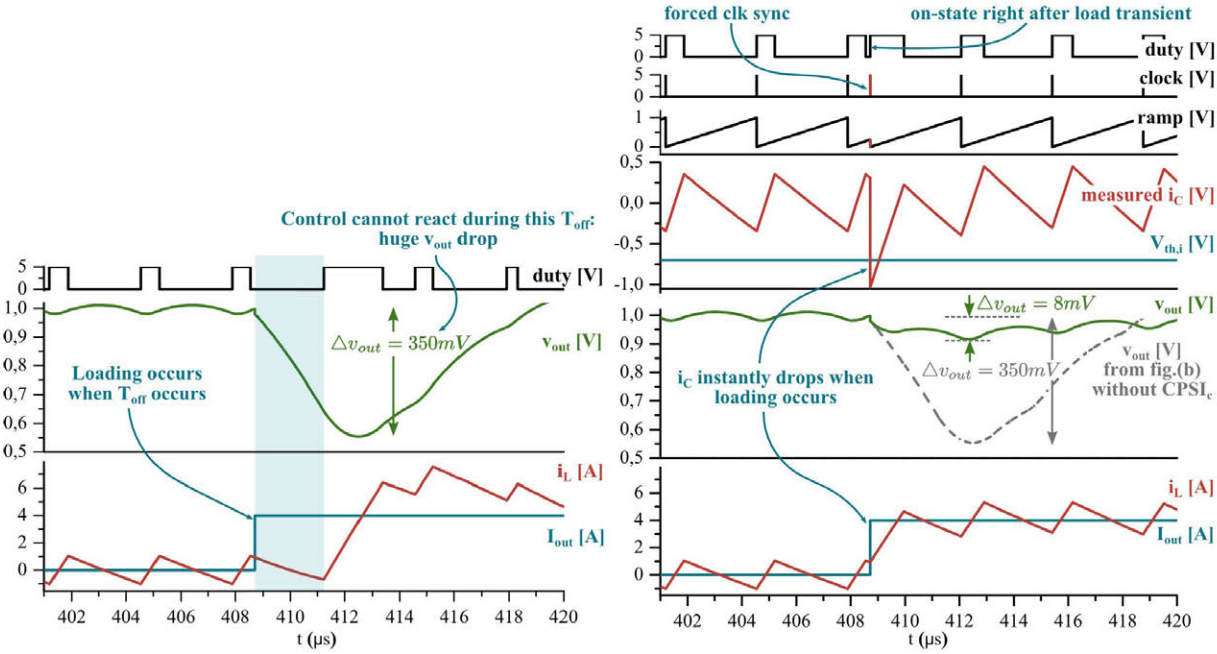
The proposed technique predicts sudden change in the load current by means of monitoring the capacitor current (figure 6a) or the derivative of the capacitor current (figure 6b). When, a positive step occurs, the change is seen on the capacitor current and the oscillator is forced to be synchronized. In this way, an on-time is allowed to occur even if the controller has not end the period set by the clock.

Fig.7.a shows a loading transient response of a constant frequency control without $\mathrm{CPSI_c}$. The parameters of the converter are as follows: $f_{sw} = 300kHz, V_{in} = 5V, v_{out} = 1V, i_o = 4A, L = 1.3\mu H, C = 30\mu F, ESR =$



(a) Using the capacitor current (b) Using the derivative of the capacitor current

Figure 6: Proposed Clock Pulse Synchronization technique (in red) on a V^2I_c control.



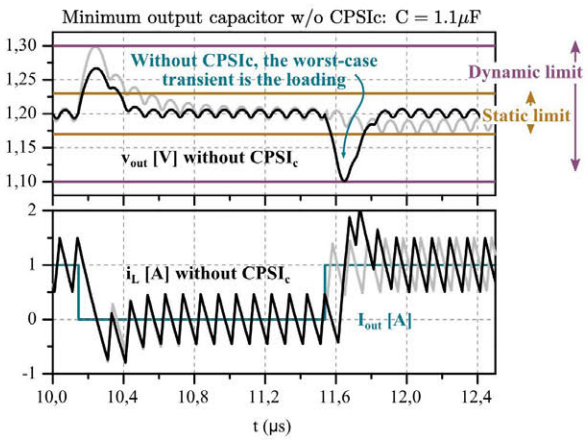
(a) Loading transient response without including CPSI$_c$ in the control. (b) Loading transient response including CPSI$_c$ in the control.

Figure 7: Loading transient response of the same converter modulated with constant switching frequency without including (a) and including CPSI$_c$ (b).

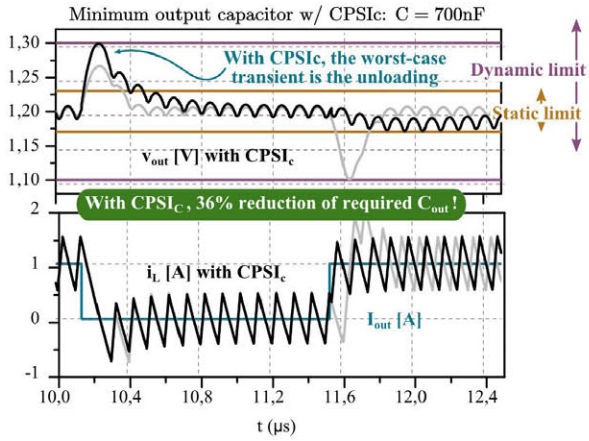
$4.4m\Omega$, $ESL = 650pH$, $K_i = 0.13\Omega$, $K_v = 1$, $V_{ramp}^{pk-pk} = 0.6V$, $H_v(s) = 38400/s$. The control is designed for an inductance of $L = 1.3\mu H$. When the loading occurs at the off-time, the control cannot react till the end of the period and, consequently, the drop of the output voltage is very large ($\triangle v_{out} = 350mV$). Fig.7.b shows the very same control and the same loading transient response but including the proposed CPSI$_c$. When the loading occurs, the current through the output capacitor instantly drops which triggers a pulse that resets the clock of the control and the next on-time begins right after the load transient. In the figure, $V_{th,i}$ is the threshold voltage of the measurement of the current through the output capacitor to trigger the clock synchronization. With CPSI$_c$, the control is able to react without delay and the drop of the output voltage is dramatically reduced (98% of reduction). Notice that CPSI$_c$ only changes during one period the switching frequency. When the clock is synchronized, the converter returns to switch at the nominal frequency.

Improvement in the load transient response for constant frequency modulation

By analyzing the table I and figures 4 and 5, it can be concluded that:



(a) Without including $CPSI_c$, the minimum required output capacitance is $1.1\mu F$ (highlighted in black). The response including $CPSI_c$ and C=$700nF$ is in the background in grey.



(b) Including $CPSI_c$, the minimum required output capacitance is $700nF$ (highlighted in black). The response without including $CPSI_c$ and C=$1.1\mu F$ is in the background in grey.

Figure 8: Comparison of the minimum required output capacitance to comply with requirements without including and including $CPSI_c$. The load steps are from full load (1 A) to no load (0 A) and vice versa.

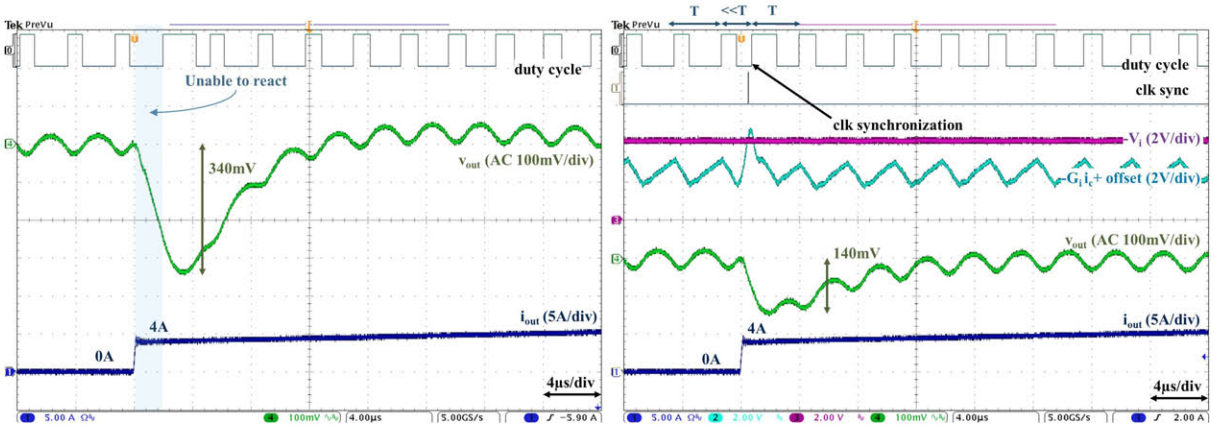
- the capacitance of the output capacitor affects the same way to the contributions of both deviations of the output voltage: due to the load disturbance and the additional drop due to the delay in the response.
- the lower the inductance, the lower the voltage deviation due to load disturbances. But the additional voltage drop due to the delay in the response remains the same independently of the inductance.

Therefore, converters with low inductance are greater benefited from using $CPSI_c$ because, for these cases, the additional drop of the output voltage due to the delay is dominant. This is very interesting for the case of high-frequency integrated converters. These converters have a low inductance for integration purposes. Fig.8 shows a comparison of the minimum required output capacitor needed to comply with the requirements of a specific high-frequency converter. The parameters of the converter are the same as in figures 4 and 5. Fig.8a shows the unloading and the loading transient of V^2I_c control without including $CPSI_c$. When $C = 1.1\mu F$, the output voltage just reaches the lower dynamic limit under the loading, so this is the minimum required output capacitance. Fig.8b shows the unloading and the loading transient of V^2I_c control including $CPSI_c$. Now, when $C = 700nF$, the output voltage just reaches the upper dynamic limit under the unloading. This means that, when $CPSI_c$ is included in the control, the required output capacitance can be reduced by a 36%, in this specific example.

Experimental validation

This section documents the experimental validation of $CPSI_c$ on a $300kHz$ Buck converter with V^2I_c control. The nominal parameters of the Buck converter are the same as in figure 7. The PWM controller UC3823 [13] is used to modulate the V^2I_c control with constant frequency. This PWM controller allows the external synchronization of the clock signal.

Fig.9 shows the experimental validation of $CPSI_c$. When a positive load step from 0A to 4A occurs in the off-time, the drop of the output voltage is 340mV (fig.9.a). When the same load transient occurs at the same instant of the off-time but including $CPSI_c$, the drop of the output voltage is 140mV (fig.9.b), achieving a 58% reduction. Notice that the measurement of the current through the output capacitor (in light blue in fig.9.b) is inverted as the implemented current sensor inverts the measurement. Notice that the reduction of the drop of the output voltage is not as dramatic as previously shown in simulations. This is because there is still a certain delay in the response due to the implementation of $CPSI_c$ with discrete components. For example, notice that there is some delay between the pulse that synchronizes the clock and the actual synchronization of the clock. This delay would be reduced if $CPSI_c$ is integrated in the PWM controller. Anyway, in order to reduce the required size of the output capacitor, it is not needed to completely eliminate the additional voltage drop due to the delay. It is enough to reduce it sufficiently so that the worst-case voltage deviation becomes the one caused by the unloading transient.



(a) Load step 0A to 4A without including CPSI_c in the control.

(b) Load step 0A to 4A including CPSI_c in the control.

Figure 9: Experimental validation of CPSI_c on a 300kHz Buck converter with V^2I_c control. Output voltage in green, output current in blue, measurement of the current through the output capacitor in light blue, comparator signal in purple, synchronization pulse (lower digital signal) and duty cycle (upper digital signal) in black.

Summary and conclusions

This paper has presented a throughout analysis of the effect that delays of constant frequency and constant on-time modulations have on the minimum required size of the output capacitor. The analysis can help designers to better understand the most appropriate modulator for their specific application. For example, it has been explained that the delay of constant frequency modulation increases the voltage deviation under a loading transient whereas the constant on-time modulation increases the voltage deviation under an unloading transient. As in small duty cycle applications, the worst-case transient is the unloading, the delay of constant frequency modulation may not affect at all the minimum required output capacitance. On the other hand, the delay of the constant on-time always increases the required capacitance for these applications.

The paper has also shown and validated a technique to improve the dynamic response of controls with constant frequency modulation that is extensible to other modulations and can be implemented in a wide variety of controllers. By using the proposed technique, the delay of constant frequency modulation can be mitigated enough so that it does not affect the minimum required size of the output capacitor.

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