An optimization algorithm to design fast and robust analog controls for Buck converters

Jorge Cortés, Vladimir Šviković, Pedro Alou, Jesús A. Oliver and José A. Cobos

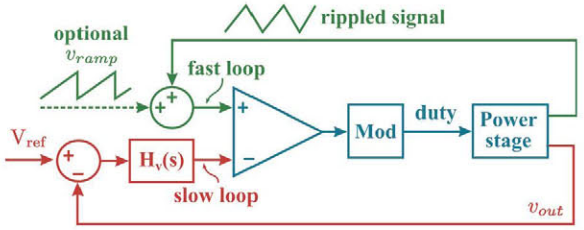
***Abstract*—Ripple-based controls are popular to achieve a fast dynamic response, but the design of these controls assuring robustness is not easy due to its intrinsic nonlinear nature. These techniques often rely on sensing networks heavily dependent on parasitic elements to estimate the inductor current or the capacitor current. Consequently, a modeling technique that takes into account these sensors and parasitic elements is needed. This paper proposes an optimization algorithm to design a wide variety of controls that can take into account the parasitic elements and tolerances of the converter. The proposed algorithm can be used to design very fast controls that are also robust in a real-world implementation. This algorithm is verified on a 300kHz Buck converter with Voltage mode and a 1.3MHz Buck converter with V^2I_c control.**

***Index Terms*—control of DC/DC converters, fast, robustness, voltage mode, v2, v2ic, optimization.**

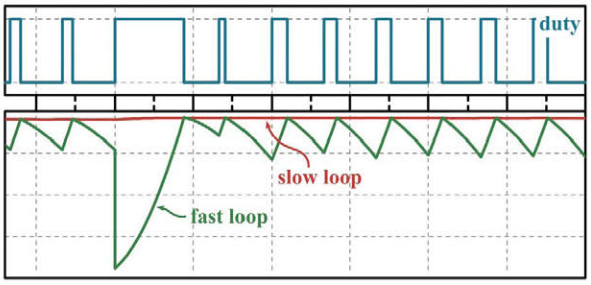
I. Introduction

Point-of-Load DC/DC converters need to withstand severe load perturbations and, to minimize the voltage deviation under these transients, the control of the converter needs to be very fast. The design of very fast controls can be problematic because the higher the bandwidth, the higher the effects of the parasitic elements and the lower the robustness. In order to ensure a robust design, practitioners must consider not only the operation region of the converter but also the possible tolerances of the passive elements.

Ripple-based controls, like V^2 [1], are popular in Point-of-Load applications for their capability to achieve a fast response. These controls use rippled information of the power stage as the triangular waveform for the modulator (fig.1a). They are composed by a fast loop, composed by the rippled signals and an optional external ramp, and a slow loop, composed typically by a type-I controller with low bandwidth that regulates tightly the output voltage in steady state. Consequently, when there is a perturbation that causes a change in the rippled signal, the duty cycle can change immediately and the control reacts very fast (fig.1b). However, the design of a fast and robust ripple-based control is not easy. These



(a) Scheme of a ripple-based control



(b) Slow and fast signals of a ripple-based control

Fig. 1: Conceptual explanation of ripple-based controls.

controls are prone to sub-harmonic oscillations so external ramp compensation might be required. Since the external ramp typically damps the dynamic response, a trade-off between fastness and robustness is needed when selecting the amplitude of the ramp.

Furthermore, some ripple-based controls sense the inductor current [2, 3] or the capacitor current [4, 5, 6] by introducing a lossless network that matches the time constant of a passive element, including parasitic elements. For example, for a good sense of the capacitor current the time constants of a real capacitor (including capacitance, series-resistance and series-inductance) need to be matched [7]. In order to design a robust control, the effect of distorted measurements due to a not ideal matching need to be also taken into consideration.

As seen above, the operation region, tolerances of the passives, parasitic elements, the sensing network and possible appearances of sub-harmonic oscillations must be regarded for a robust design of the control. In order to achieve this task, a modeling technique and a stability analysis that include all these considerations is needed. The Describing Function technique is a useful modeling technique [8], it can be used to model current mode and ripple-based controls as a transfer

function [8, 9] or as an equivalent circuit model [10, 11, 6]. Since it is accurate up to half the switching frequency, it can be used to predict sub-harmonic oscillations. Consequently, the Describing Function technique provides a very good understanding of the system. However, it may not be an appropriate technique when modeling a converter including all the relevant parasitic elements or the sensing network. Therefore, the effect of the distortion in the measurement due to a non ideal sensing may not be analyzed with this technique. Furthermore, [12] shows that, under certain conditions, the accuracy of the model based on the Describing Function decreases and needs to be used with caution.

This paper proposes an optimization algorithm that uses a very accurate numerical modeling technique and stability analysis, that takes into account tolerances of passives, parasitic elements and distorted measurements [12]. This way, the algorithm is capable of designing a very fast control while being very robust. The proposed algorithm can be applied to a wide variety of controls such as voltage mode, current mode and ripple-based controls and to different modulation techniques such as PWM (constant switching frequency) and constant on-time.

II. Review of V^2, V^2I_L and V^2I_c controls

V^2 [1] is a ripple-based control that uses the output voltage as the signal to modulate the duty cycle. If the ESR of the output capacitor is large, as it is the case for OS-CON capacitors, the output voltage ripple is dominated by the ripple across the ESR. This voltage is $v_{Rc} = i_c \cdot R_c$, where i_c is the capacitor current and R_c is the ESR of the output capacitor. Therefore, if the ESR is large, the output voltage has information about the capacitor current and, consequently, about the output current and can react very fast under load steps [13].

However, if low-ESR capacitor are used such as ceramic capacitors, sub-harmonic oscillations can appear in V^2 control (fig.2). In these cases, it is needed to add compensation to stabilize the control.

This compensation can be done means of adding a ramp, but this can damp the response of the control. A better strategy is to compensate with a triangular signal that has information about the converter. The most popular way to achieve this is to compensate with the inductor current [2, 3]. This control is called in the industry V^2 with inductor current ramp compensation but we will call it V^2I_L for simplicity. The sense of the inductor current is commonly done by means of a R-C network that matches the impedance of the inductor: $L/R_L = R_iC_i$, where L is the inductance, R_L is the ESR of the inductor and R_i and C_i are the resistance and capacitance of the R-C network (fig.3). V^2I_L control is already popular in the industry with chips available to build the controller [14, 15].

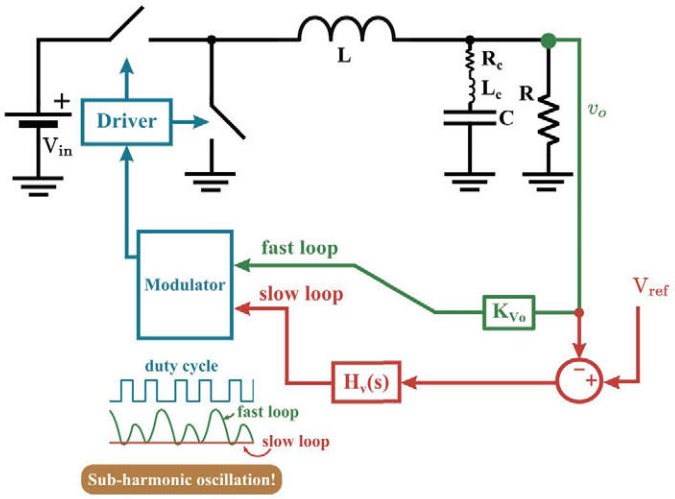


Fig. 2: Sub-harmonic oscillation in V^2 control when the ESR of the output capacitor is not dominant.

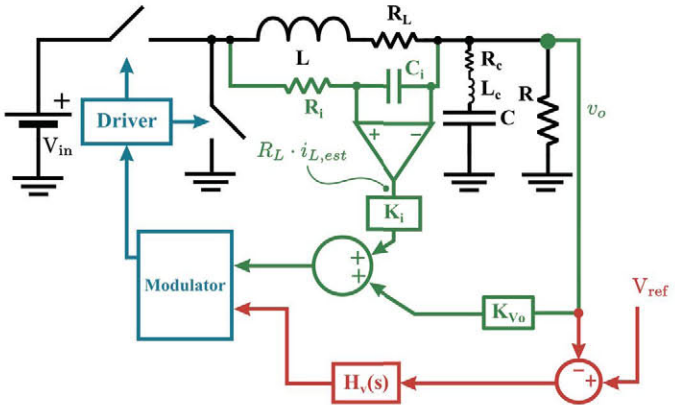


Fig. 3: Control scheme of V^2I_L [2, 3].

Nonetheless, the inductor current does not have information about the output current and, if low-ESR caps are used, the control does not exhibit a feedforward of the output current. This can limit its dynamic response under a load step. On the other hand, if the capacitor current is used to compensate the V^2 control, then the control will exhibit a feedforward of the

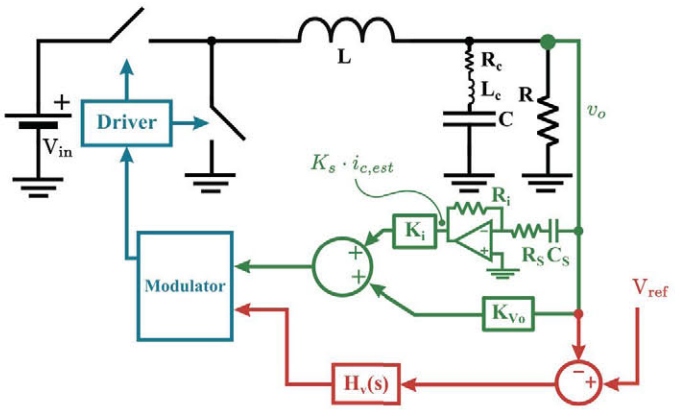


Fig. 4: Control scheme of V^2I_c [5, 6].

$$
\begin{aligned}
i) \quad & \frac{dx(t)}{dt} = \begin{cases} A_0 x(t) + B_0 u, & \text{if state 0} \\ \quad \ldots \\ A_n x(t) + B_n u, & \text{if state n} \end{cases} \\
& h_0(x(t), t) = 0 \\
ii) \quad & \quad \ldots \\
& h_m(x(t), t) = 0
\end{aligned}
\xrightarrow{\text{ref.[12]}} \quad x(t) = f(x_0, u) \tag{1}
$$

output current and, consequently, it can react very fast under load steps [13]. This control, that uses both the output voltage and the capacitor current as the modulator signal, is called V^2I_c [5, 6]. Fig.4 shows the scheme of the V^2I_c control. The sensing of the capacitor current is done by means of a transimpedance amplifier that is designed to behave like an impedance proportional to the impedance of the output capacitor, including the ESR and the ESL of the capacitor. Notice that, in the implementation of V^2I_c, only the output voltage is sensed.

III. Modeling and Stability Analysis

This section explains the techniques to model and evaluate the stability that will be later used in the optimization algorithm. It also shows the complete schemes of the Buck converter and controls that will be modeled. The optimization algorithm can optimize the dynamic response of a wide variety of controls but the following ones are selected to illustrate the possibilities:

- Voltage mode with constant frequency modulation because it is the most widely used control.
- V^2I_L with constant on-time modulation because it has gathered a lot of attention from the industry and it is being increasingly used.
- V^2I_c with constant frequency modulation for its capability of achieving an almost optimal dynamic response.

A. Methodology

This subsection explains the methodology to model the whole converter (with the power stage and the control included) and to evaluate its stability. [12] presents the description of the methodology applied to V^2 and V^2I_c control. The modeling of the converter is a time-domain model derived from the piecewise-smooth model of the system (1):

where $i)$ is the piecewise state space model of the converter, $ii)$ are the switching conditions to commutate the state, x is a vector containing the state variables and u is a vector containing the input variables. It is important to point out that x does not only contain the state variables of the power stage but also the state variables of the control. The stability analysis is based on Floquet theory which uses the piecewise-smooth model of (1). As this paper is focused on explaining the optimization algorithm and its results, please refer to [12] for further information about the modeling and stability analysis.

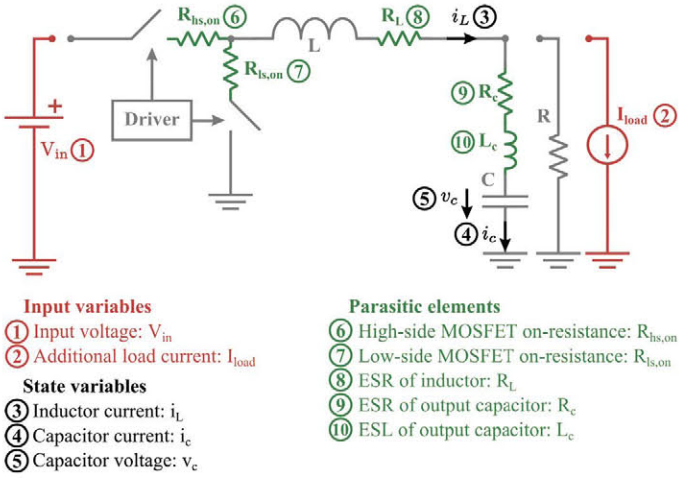


Fig. 5: Scheme of a Buck converter with parasitic elements.

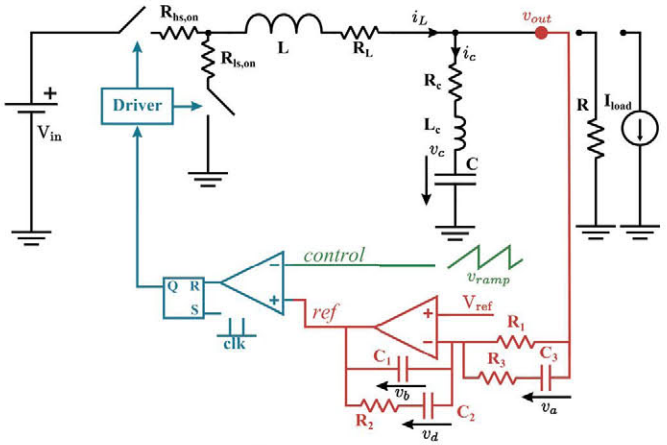
B. Power stage and control

This subsection explains the elements that are considered in the modeling of the power stage and the control. Fig.5 shows the power stage of a synchronous Buck converter with all the considered input variables, state variables and parasitic elements.

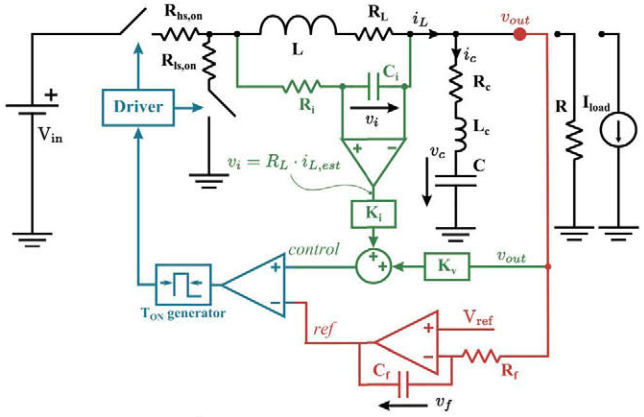
The input variables are the input voltage, V_{in}, and an additional load current, I_{load}. The state variables are the inductor current, i_L, the capacitor current, i_c, and the capacitor voltage, v_c. The considered parasitic elements are the on-resistances of the MOSFETs, $R_{hs,on}$ and $R_{ls,on}$, the series-resistance of the inductor, R_L, and the series-resistance and series-inductance of the output capacitor, R_c and L_c.

Since V^2I_L and V^2I_c use the parasitic elements of the inductor and the output capacitor, respectively, their inclusion in the modeling is crucial to evaluate the influence of an incorrect estimation of them.

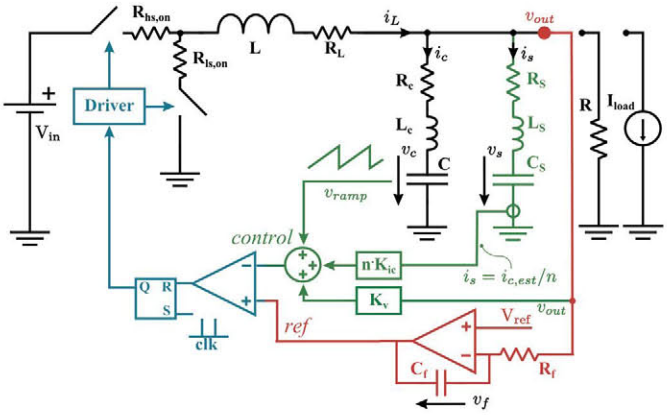
Fig.6a–6c show the complete schemes of the converters with different controls as they are modeled. Fig.6a represents the model of the converter controlled with voltage mode, fig.6b with V^2I_L control and fig.6c with V^2I_c control. Notice that the sensing networks have been included in the modeling. In the case, of V^2I_c, the trans-impedance amplifier has been changed to an equivalent RLC network with an impedance n times proportional to the impedance of the output capacitor for analysis purposes. The input variable of the controls is the reference voltage, V_{ref}. The state variables are specific for each control. In voltage mode, the state variables of the



(a) Voltage mode control



(b) V^2I_L control with constant on-time.



(c) V^2I_c control with constant switching frequency.

Fig. 6: Schemes of the controls as they are modeled.

control are v_a, v_b and v_d, which are the capacitor voltages of the type-III linear controller. In V^2I_L, the state variables are the capacitor voltage of the type-I linear controller, v_f, and the capacitor voltage of the sensing network of the inductor current, v_i. In V^2I_c, the state variables are the capacitor voltage of the type-I linear controller, v_f, and the capacitor voltage and capacitor current of the sensing network of the current through the output capacitor, v_s and i_s.

C. Comparison with Simplis simulation

This subsection validates at simulation level the models that are used in the optimization algorithm. Fig.7 shows the transient response of the modeled controls under a load disturbance obtained from the derived model and from the Simplis simulation. Specifically, fig.7a shows the validation of the model of Voltage mode, 7b shows the validation of the model of V^2I_L and 7c shows the validation of the model of V^2I_c. The parameters of each control are:

- Voltage mode (fig.6a): $V_{in} = 5V$, $v_{out} = 1V$, $f_{sw} = 1.29MHz$, $L = 150nH$, $R_L = 2m\Omega$, $C = 150\mu F$, $R_c = 1m\Omega$, $L_c = 400pH$, $R_{hs,on} = 30m\Omega$, $R_{ls,on} = 12m\Omega$, $R_1 = 1.54k\Omega$, $R_2 = 3.3k\Omega$, $R_3 = 50\Omega$, $C_1 = 75pF$, $C_2 = 2.1nF$, $C_3 = 2.2nF$.
- V^2I_L (fig.6b): $V_{in} = 5V$, $v_{out} = 1.2V$, $T_{on} = 61ns$, $L = 100nH$, $R_L = 10m\Omega$, $C = 4\mu F$, $R_c = 4.86m\Omega$, $L_c = 100pH$, $R_{hs,on} = 20m\Omega$, $R_{ls,on} = 10m\Omega$, $R_i = 10k\Omega$, $C_i = 1nF$, $K_i = 10.718$, $K_v = 1.61$, $R_f = 1k\Omega$, $C_f = 4.28nF$.
- V^2I_c (fig.6c): $V_{in} = 5V$, $v_{out} = 1.2V$, $f_{sw} = 300kHz$, $L = 1.3\mu H$, $R_L = 2m\Omega$, $C = 30\mu F$, $R_c = 4.4m\Omega$, $L_c = 100pH$, $R_{hs,on} = 50m\Omega$, $R_{ls,on} = 50m\Omega$, $C_s = 30nF$, $R_s = 4.4\Omega$, $L_s = 100nH$, $K_i \cdot n = 0.129$, $K_v = 1$, $R_f = 1.2k\Omega$, $C_f = 22nF$, $V_{ramp,pp} = 0.6V$.

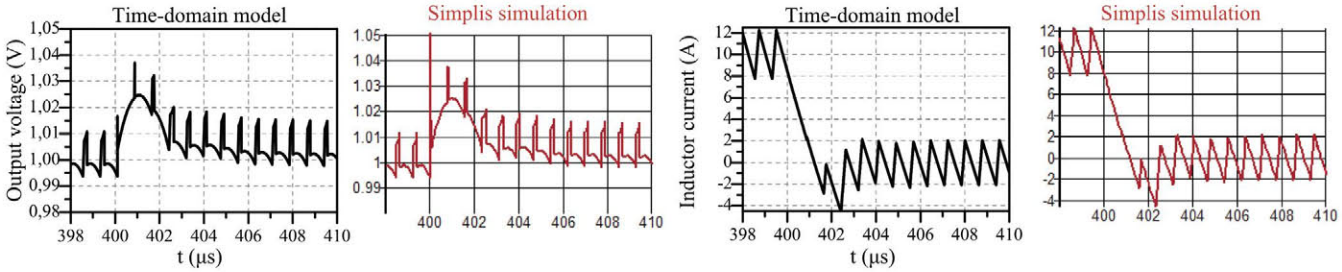
The reason for different power stages and conditions is to validate that the model behaves well under several cases. For example, V^2I_L is modulated with constant on-time while the others are modulates with constant switching frequency. Also, Voltage mode control is tested with high switching frequency to see the effect of the ESL on the output voltage. They all show a very good agreement and, consequently, the models are valid.

IV. Optimization Algorithm

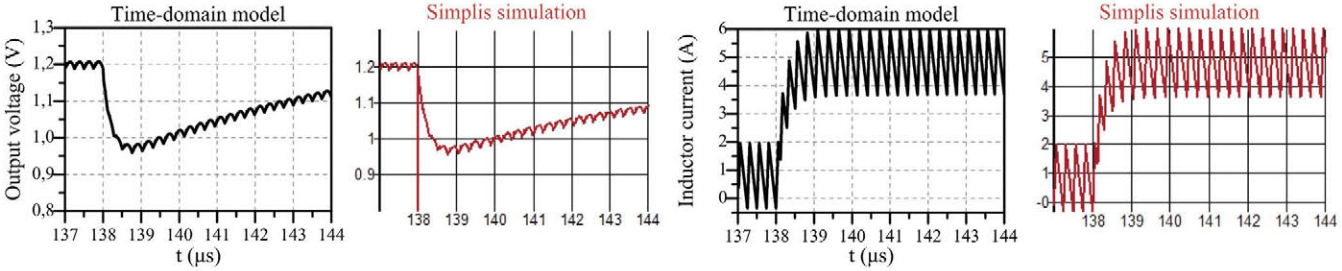
This section explains the proposed optimization algorithm to design fast and robust controls. Fig.8a shows the conceptual scheme of the proposed algorithm: by using an accurate stability analysis and modeling, the algorithm optimizes the transient response of the control taking into account static and dynamic constraints specified by the user. Fig.8b is a visual example of the tolerances and constraints that can be defined in the algorithm.

The flow of the algorithm is as follows:

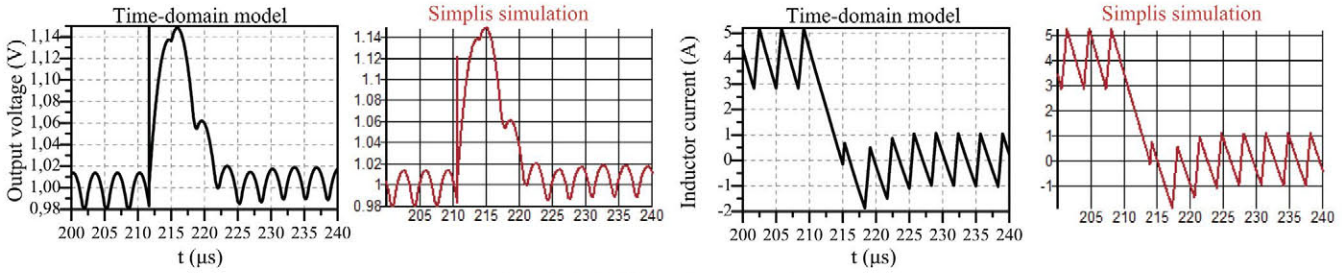
1) assuring stability: for every set of control parameters (gains and capacitors and resistors of linear controllers) that is evaluated, first, the stability is analyzed over the whole operating region and regarding tolerances of the components of the converter. If the converter is not stable in any of the cases, then that set of control parameters is rejected.
2) assuring dynamic requirements: if the converter is stable in all cases, the dynamic behavior under user-defined



(a) Load step $10A \rightarrow 0A$ of Voltage mode control with constant frequency modulation.



(b) Load step $0A \rightarrow 4A$ of V^2I_L control with constant on-time modulation.



(c) Load step $4A \rightarrow 0A$ of V^2I_c with constant frequency modulation.

Fig. 7: Comparison of proposed time-domain models with Simplis simulation.

perturbations is computed. The value of the output voltage and the inductor current is monitored and, if a dynamic constraint (maximum overcurrent, maximum overvoltage,...) is violated, the algorithm rejects that set of parameters.

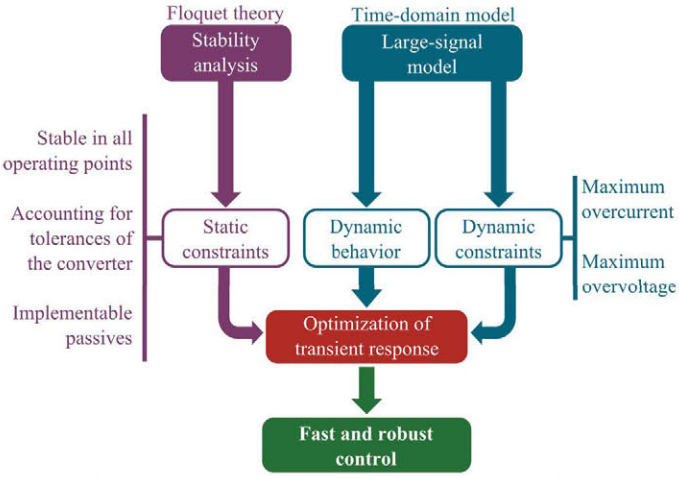
3) calculation of objective function: if the set of control parameters complies with the static and dynamic requirements, the algorithm calculates the objective function as a measurement of how well that set of parameters performs. The algorithm uses by default the weighted quadratic errors of the output voltage under the user-defined perturbations as the objective function to minimize, but the user can create another objective function if needed.
4) optimization of parameters: the algorithm tries to find the set of control parameters that minimizes the objective function while complying with the static and dynamic constraints. This search is done because of simplicity with a coordinate descent algorithm, although other techniques as gradient descent can be used.

This way, the final design of the optimization algorithm is fast, because the error of the output voltage is minimized under perturbations, and robust, because the design complies with the specific static and dynamic requirements of the converter, accounting for tolerances, parasitic elements and distorted measurements.

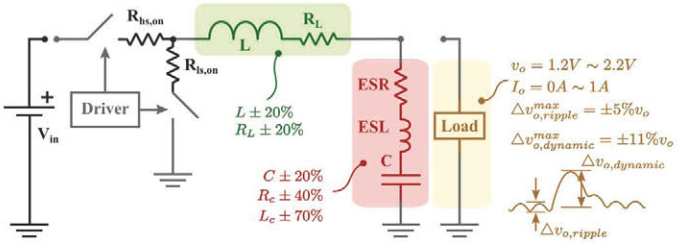
A. Comparison of different designs of Voltage mode control

In order to show the benefits of using the proposed optimization algorithm, this subsection compares a design of Voltage mode obtained from the proposed optimization algorithm with the design guidelines proposed by International Rectifier in [16] and Intersil in [17]. Of course, these design guidelines are meant to be general and fine tuning of the parameters is expected afterwards to achieve the best results. Still, this comparison can illustrate what can be achieved with the proposed optimization algorithm.

Fig.9 shows the comparison of the dynamic response of the three designs under a load step (fig.9a) and a reference voltage step (fig.9b). The power stage is the same as the one in fig.7a. The optimized design is shown in black, the design based in International Rectifier's guidelines is shown in grey and the design based in Intersil's guidelines is shown in

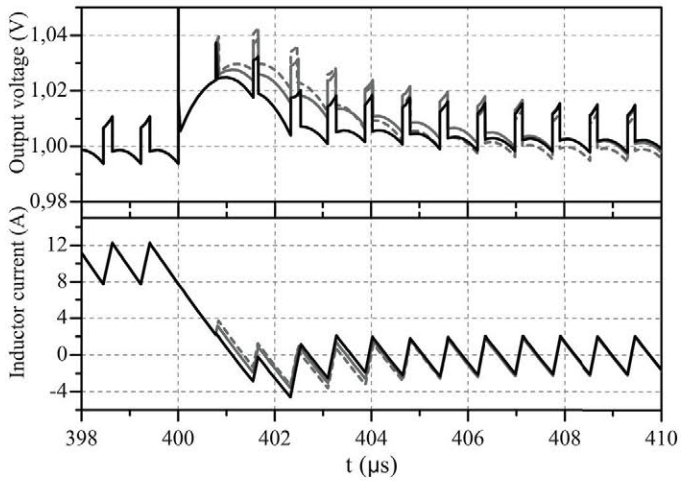


(a) Conceptual scheme of proposed optimization algorithm

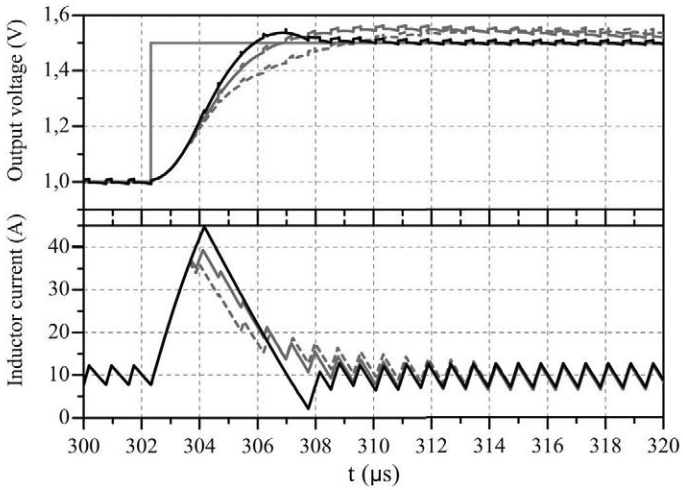


(b) Example of tolerances and constraints that can be defined by the user in the proposed optimization algorithm

Fig. 8: Scheme of optimization algorithm and example of a setup of constraints.



(a) Load step $10A \rightarrow 0A$



(b) Voltage reference voltage step $1V \rightarrow 1.5V$

Fig. 9: Comparison of the dynamic response of the three designs of Voltage mode under a load step (a) and voltage reference step (b). The design obtained from the optimization is shown in black, the design based in [16] is in grey and the design based in [17] is shown in dotted grey.

dotted grey. The comparison shows that the design optimized with the proposed algorithm is faster than the other designs. Specifically, notice that it achieves the minimum possible deviation of the output voltage for the power stage under the load step, saturating the duty cycle to zero. Furthermore, it achieves an almost time-optimal response under the reference voltage step with a transient response very similar to the Minimum-time control [18, 19].

V. Experimental validation

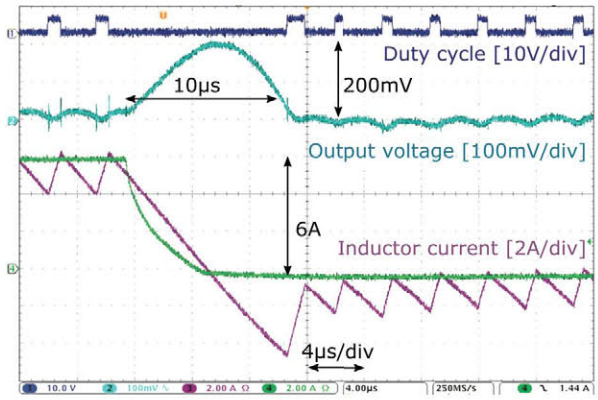
This section validates the designs of Voltage mode and $V^2 I_c$ controls optimized with the proposed algorithm in order to prove that they are fast and can be implemented in practice. It is divided in two subsections that explain separately each design.

A. Validation of optimized design of Voltage mode control

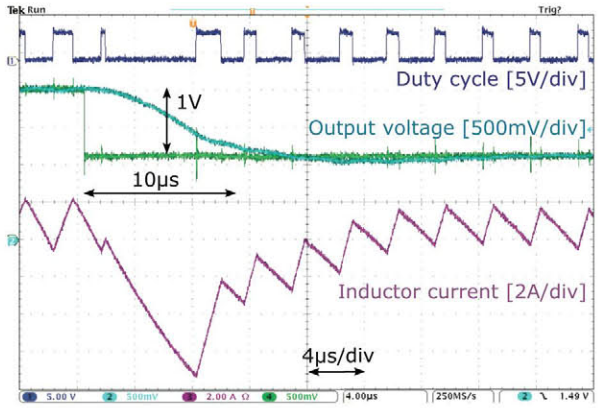
The power stage to be controlled is as follows (fig.6a): $V_{in} = 5V$, $v_{out} = 1V$, $f_{sw} = 300kHz$, $L = 1.3\mu H$, $R_L = 1.5m\Omega$, $C = 40\mu F$, $R_c = 4m\Omega$, $L_c = 600pH$, $R_{hs,on} = 30m\Omega$, $R_{ls,on} = 14.2m\Omega$. The optimization algorithm is setup with the following conditions:

- The control is optimized for load disturbances and voltage reference steps.
- The converter needs to be stable over the whole operation region and accounting for tolerances of the passive elements. The operation region is as follows: the output voltage can vary from 1V to 4V and the output current can vary from 0A to 10A. Only the tolerance of the ESL of the output capacitor is taken into account, which is $L_c \pm 70\%$ (accounting for the tolerances of the ESL because of the layout).
- Only capacitance values greater than $10pF$ in the linear controller is allowed so that the design is implementable in practice.

The obtained optimized controller has the following parameters (fig.6a): $R_1 = 300\Omega$, $R_2 = 130\Omega$, $R_3 = 12\Omega$, $C_1 = 570pF$, $C_2 = 100nF$, $C_3 = 22nF$. Fig.10 shows the experimental transient responses of the designed Voltage mode control in a prototype under a load step (fig.10a) and under a reference voltage step (fig.10b). Notice that, in the case of the load disturbance, the response of the control is almost time-

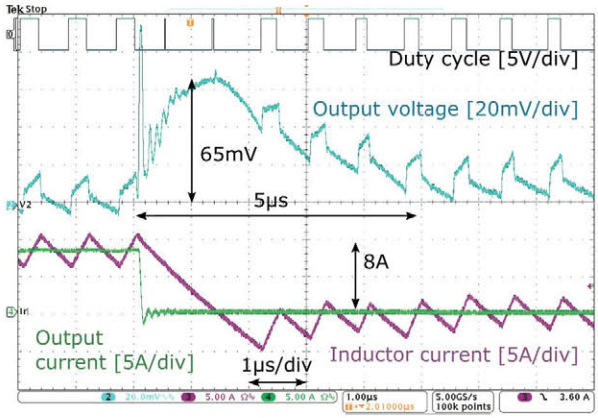


(a) Optimized Voltage mode. Load step $6A \rightarrow 0A$.

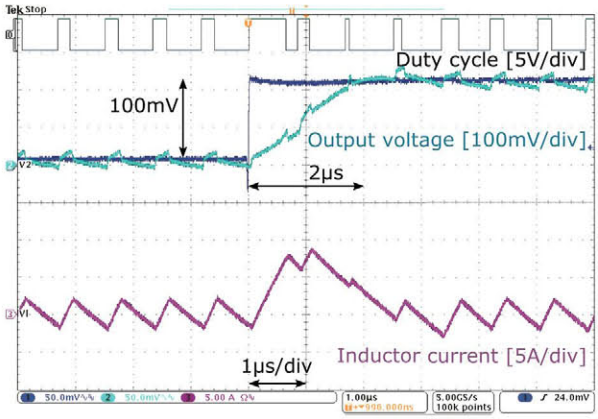


(b) Optimized Voltage mode. Reference voltage step $2V \rightarrow 1V$.

Fig. 10: Transient response of the optimized design of Voltage mode control under a load step (a) and a reference voltage step (b).



(a) Optimized V^2I_c. Load step $8A \rightarrow 0A$.



(b) Optimized V^2I_c. Reference voltage step $1.5V \rightarrow 1.6V$.

Fig. 11: Transient response of the optimized design of V^2I_c control under a load step (a) and a reference voltage step (b).

optimal, achieving a very similar transient response as charge-balance controls [20]. The response of the converter under voltage step is equally fast. Consequently, it has been validated that the design of a Voltage mode control with the proposed optimization algorithm is very fast and implementable.

B. Validation of optimized design of V^2I_c control

The power stage to be controlled is as follows (fig.6c): $V_{in} = 5V$, $v_{out} = 1.5V$, $f_{sw} = 1.29MHz$, $L = 150nH$, $R_L = 2m\Omega$, $C = 150\mu F$, $R_c = 1m\Omega$, $L_c = 1nH$, $R_{hs,on} = 30m\Omega$, $R_{ls,on} = 12m\Omega$, $C_s = 150nF$, $R_s = 1\Omega$, $L_s = 1\mu H$. The optimization algorithm is setup with the following conditions:

- The control is optimized for load disturbances and voltage reference steps.
- The converter needs to be stable over the whole operation region and accounting for tolerances of the passive elements. The operation region is as follows: the output voltage can vary from 0.5V to 2V and the output current can vary from 0A to 15A. The converter needs to be stable also under the following variations of parameters: $C \pm 20\%$, $L \pm 20\%$, $R_c \pm 20\%$, $L_c \pm 70\%$. Notice that, variations in the output capacitor from the nominal values (C, R_c, L_c) would distort the current measurement. Consequently, by taking into account these tolerances, the control will be robust under not-ideal sensing.
- Only capacitance values greater than $10pF$ in the linear controller is allowed so that the design is implementable in practice.

The obtained optimized controller has the following parameters (fig.6c): $K_i \cdot n = 0.0184$, $K_v = 2.33$, $R_f = 1.6k\Omega$, $C_f = 47nF$, $V_{ramp,pp} = 0.49V$. Fig.11 shows the experimental transient responses of the designed V^2I_c control in a prototype under a load step (fig.10a) and under a reference voltage step (fig.11b). Notice that, in the case of the load disturbance, the response of the control achieves the minimum voltage deviation for the power stage. The response of the converter under voltage step is also fast. Consequently, it has been validated that the design of a V^2I_c control with the proposed optimization algorithm is very fast and implementable.

VI. Summary

This paper has proposed an optimization algorithm to design fast and robust controls. It has been validated in simulations and in an experimental prototype that the designs are very fast, close to time-optimal response. Furthermore, their robustness is assured by means of a very accurate stability analysis. The

algorithm can take into account a lot of information such as operation region, tolerances of components, parasitic elements and sensing networks. The algorithm can be applied to voltage mode, current mode and ripple-based controls and different modulation techniques such as constant frequency or constant on-time modulations.

APPENDIX A
PIECE-WISE MODELS OF CONTROLS

This appendix contains the detailed expression of the piece-wise models of the Buck converter controlled with type-III Voltage mode, V^2I_L and V^2I_c. The models are of the form:

$$\frac{dx(t)}{dt} = \begin{cases} A_0 x(t) + B_0 u, & \text{if state is 0} \\ A_1 x(t) + B_1 u, & \text{if state is 1} \end{cases} \tag{2}$$

where u are the input variables, x are the state variables, the state 0 is when the low-side MOSFET is conducting and the state 1 is when the high-side MOSFET is conducting.

A. Piece-wise model of type-III Voltage mode with constant frequency

Figure 6a shows the scheme of the model of Voltage mode. The state variables are

$$x(t) = \left(v_c(t),\ i_L(t),\ i_c(t),\ v_a(t),\ v_b(t)\ v_d(t)\right)^T, \tag{3}$$

and the input variables are

$$u = (V_{in},\ V_{ref},\ I_{load})^T. \tag{4}$$

The matrices are

$$A_0 = \begin{pmatrix} 0 & 0 & 1/C \\ 0 & \dfrac{R_{ls,on} + R_L + R}{-L} & R/L \\ -1/L_c & R/L_c & -(R+R_c)/L_c \\ 0 & R/(R_3C_3) & -R/(R_3C_3) \\ 0 & \dfrac{R}{R_1C_1} + \dfrac{R}{R_3C1} & \dfrac{-R}{R_1C_1} + \dfrac{-R}{R_3C_1} \\ 0 & 0 & 0 \end{pmatrix}$$

$$\begin{pmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ -1/(R_3C_3) & 0 & 0 \\ -1/(R_3C_1) & -1/(R_2C_1) & 1/(R_2C_1) \\ 0 & 1/(R_2C_2) & -1/(R_2C_2) \end{pmatrix}; \tag{5}$$

$$A_1 = \begin{pmatrix} 0 & 0 & 1/C \\ 0 & \dfrac{R_{hs,on} + R_L + R}{-L} & R/L \\ -1/L_c & R/L_c & -(R+R_c)/L_c \\ 0 & R/(R_3C_3) & -R/(R_3C_3) \\ 0 & \dfrac{R}{R_1C_1} + \dfrac{R}{R_3C1} & \dfrac{-R}{R_1C_1} + \dfrac{-R}{R_3C_1} \\ 0 & 0 & 0 \end{pmatrix}$$

$$\begin{pmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ -1/(R_3C_3) & 0 & 0 \\ -1/(R_3C_1) & -1/(R_2C_1) & 1/(R_2C_1) \\ 0 & 1/(R_2C_2) & -1/(R_2C_2) \end{pmatrix}; \tag{6}$$

$$B_0 = \begin{pmatrix} 0 & 0 & 0 \\ 0 & 0 & R/L \\ 0 & 0 & -R/L_c \\ 0 & -1/(R_3C_3) & -R/(R_3C_3) \\ 0 & \dfrac{-1}{R_1C_1} + \dfrac{-1}{R_3C_1} & \dfrac{-R}{R_1C_1} + \dfrac{-1}{R_3C_1} \end{pmatrix}; \tag{7}$$

$$B_1 = \begin{pmatrix} 0 & 0 & 0 \\ 1/L & 0 & R/L \\ 0 & 0 & -R/L_c \\ 0 & -1/(R_3C_3) & -R/(R_3C_3) \\ 0 & \dfrac{-1}{R_1C_1} + \dfrac{-1}{R_3C_1} & \dfrac{-R}{R_1C_1} + \dfrac{-1}{R_3C_1} \end{pmatrix}. \tag{8}$$

The switching conditions to switch from ON to OFF and from OFF to ON are, respectively:

$$h_{10}(x,t) = Kx(t) + Gu + m_{ramp}t \tag{9}$$

$$h_{01}(t) = t - T \tag{10}$$

where

$$K = (0,\ 0,\ 0,\ 0,\ 1,\ 0) \tag{11}$$

$$G = (0,\ 0,\ 0) \tag{12}$$

B. Piece-wise model of V^2I_L with constant on-time

Figure 6b shows the scheme of the model of V^2I_L. The state variables are

$$x(t) = \left(v_c(t),\ i_L(t),\ i_c(t),\ v_i(t),\ v_f(t)\right)^T, \tag{13}$$

and the input variables are

$$u = (V_{in},\ V_{ref},\ I_{load})^T; \quad K_p = 1/(R_fC_f). \tag{14}$$

The matrices are

$$A_0 = \begin{pmatrix} 0 & 0 & 1/C \\ 0 & \dfrac{R_{ls,on} + R_L + R}{-L} & R/L \\ -1/L_c & R/L_c & -(R+R_c)/L_c \\ 0 & -(R_{ls,on}+R)/(R_iC_i) & R/(R_iC_i) \\ 0 & -K_pR & K_pR \end{pmatrix}$$

$$\begin{pmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ -1/(R_iC_i) & 0 \\ K_pR & 0 \end{pmatrix}; \tag{15}$$

$$A_1 = \begin{pmatrix} 0 & 0 & 1/C \\ 0 & \frac{R_{hs,on}+R_L+R}{-L} & R/L \\ -1/L_c & R/L_c & -(R+R_c)/L_c \\ 0 & -(R_{hs,on}+R)/(R_iC_i) & R/(R_iC_i) \\ 0 & -K_pR & K_pR \end{pmatrix}$$

$$\begin{pmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ -1/(R_iC_i) & 0 \\ K_pR & 0 \end{pmatrix}; \quad (16)$$

$$B_0 = \begin{pmatrix} 0 & 0 & 0 \\ 0 & 0 & R/L \\ 0 & 0 & -R/L_c \\ 0 & 0 & R/(R_iC_i) \\ 0 & K_p & K_pR \end{pmatrix}; \quad (17)$$

$$B_1 = \begin{pmatrix} 0 & 0 & 0 \\ 1/L & 0 & R/L \\ 0 & 0 & -R/L_c \\ 1/(R_iC_i) & 0 & R/(R_iC_i) \\ 0 & K_p & K_pR \end{pmatrix}. \quad (18)$$

The switching conditions to switch from ON to OFF and from OFF to ON are, respectively:

$$h_{10}(x,t) = t - T_{on} \quad (19)$$

$$h_{01}(x,t) = Kx(t) + Gu \quad (20)$$

where

$$K = (0,\ K_vR,\ -K_vR,\ K_i,\ -1) \quad (21)$$

$$G = (0,\ 0,\ -K_vR). \quad (22)$$

C. Piece-wise model of V^2I_c with constant frequency

Figure 6c shows the scheme of the model of V^2I_c. The state variables are

$$x(t) = \big(v_c(t),\ v_s(t),\ i_L(t),\ i_c(t),\ i_s(t)\ v_f(t)\big)^T, \quad (23)$$

and the input variables are

$$u = (V_{in},\ V_{ref},\ I_{load})^T; \quad K_p = 1/(R_fC_f). \quad (24)$$

The matrices are

$$A_0 = \begin{pmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & \frac{R_{ls,on}+R_L+R}{-L} \\ -1/L_c & 0 & R/L_c \\ 0 & -1/L_s & R/L_s \\ 0 & 0 & -K_pR \end{pmatrix}$$

$$\begin{pmatrix} 1/C & 0 & 0 \\ 0 & 1/C_s & 0 \\ R/L & R/L & 0 \\ -(R+R_c)/L_c & -R/L_c & 0 \\ -R/L_s & -(R+R_s)/L_s & 0 \\ K_pR & K_pR & 0 \end{pmatrix} \quad (25)$$

$$A_1 = \begin{pmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & \frac{R_{hs,on}+R_L+R}{-L} \\ -1/L_c & 0 & R/L_c \\ 0 & -1/L_s & R/L_s \\ 0 & 0 & -K_pR \end{pmatrix}$$

$$\begin{pmatrix} 1/C & 0 & 0 \\ 0 & 1/C_s & 0 \\ R/L & R/L & 0 \\ -(R+R_c)/L_c & -R/L_c & 0 \\ -R/L_s & -(R+R_s)/L_s & 0 \\ K_pR & K_pR & 0 \end{pmatrix} \quad (26)$$

$$B_0 = \begin{pmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & R/L \\ 0 & 0 & -R/L_c \\ 0 & 0 & -R/L_s \\ 0 & K_p & K_pR \end{pmatrix} B_1 = \begin{pmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 1/L & 0 & R/L \\ 0 & 0 & -R/L_c \\ 0 & 0 & -R/L_s \\ 0 & K_p & K_pR \end{pmatrix} \quad (27)$$

The switching conditions to switch from ON to OFF and from OFF to ON are, respectively:

$$h_{10}(x,t) = Kx(t) + Gu + m_{ramp}t \quad (28)$$

$$h_{01}(t) = t - T \quad (29)$$

where

$$K = (0,\ 0,\ K_vR,\ -K_vR,\ nK_i - K_vR,\ -1) \quad (30)$$

$$G = (0,\ -1,\ -K_vR) \quad (31)$$

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