Using pMOS Pass-Gates to Boost SRAM Performance by Exploiting Strain Effects in Sub-20-nm FinFET Technologies

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Abstract—**Strained fin is one of the techniques used to improve the devices as their size keeps reducing in new nanoscale nodes. In this paper, we use a predictive technology of 14 nm where pMOS mobility is significantly improved when those devices are built on top of long, uncut fins, while nMOS devices present the opposite behavior due to the combination of strains. We explore the possibility of boosting circuit performance in repetitive structures where long uncut fins can be exploited to increase fin strain impact. In particular, pMOS pass-gates are used in 6T complementary SRAM cells (CSRAM) with reinforced pull-ups. Those cells are simulated under process variability and compared to the regular SRAM. We show that when layout dependent effects are considered the CSRAM design provides 10% to 40% faster access time while keeping the same area, power, and stability than a regular 6T SRAM cell. The conclusions also apply to 8T SRAM cells. The CSRAM cell also presents increased reliability in technologies whose nMOS devices have more mismatch than pMOS transistors.**

Index Terms—**Complementary SRAM, fin-shaped field-effect-transistor (FinFET), mismatch, pass-gate, SiGe stressor, static random access memory (SRAM), tensile stress, variability.**

I. Introduction

FINFET technology has allowed the success of device scaling following Moore's law deep in the nanoscale regime. However, there are many technological challenges of FinFET manufacturing to achieve satisfactory devices in terms of speed, power, and variation tolerance. Strain technology has been a key enabler for improving device performance in the past decade [1]. In incoming CMOS FinFET nodes, fin strain compresses or stretches the fins that form the transistor; this increases the mobility of the charge carriers making the devices faster. However, the particular effects of strained technology have only recently started to be considered at circuit level [2].

Another important challenge related to nanoscale technology is the need for mapping technology advances to circuit models. In this sense, more efforts must be applied to the development of predictive MOSFET models that play a critical role for early stage design technology co-optimization and circuit design research [3]. We can find that circuits designed with devices beyond the 20-nm node can present unexpected results or behaviors far away from the conventional design. Thus, designers should open their mind and look for proposals that break the traditional rules. This is what we do in this study, we explore the design of SRAM cells with pMOS as pass transistors.

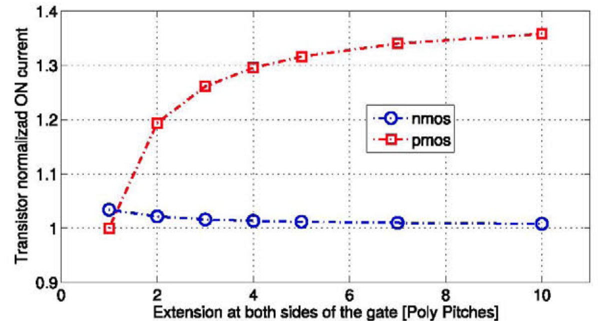


Fig. 1. Different effect of tensile STI strain on pMOS and nMOS devices mobility, depending on fin length.

In particular, we focus on designing SRAM cells using the same predictive FinFET technology as in [4] corresponding to the 14-nm node. In this technology, source and drain SiGe compressive stressors combined with tensile shallow-trench isolation (STI) [5] of 1-GPa tensile stress are employed. As shown in Fig. 1, for pMOS, the mobility enhancement from stressor increases as the fin is lengthened, due to lateral relaxation of SiGe stressors. On the other hand, tensile STI stress increases while the fin length is reduced. As a result, it boosts nMOS mobility for a shorter fin length, but at the same time it degrades pMOS mobility. A study on how strain affects differently nMOS and pMOS transistors was already done in [2], the authors show that applying stressors only to one of the devices, leaving the other fins unstressed, leads to SRAM cells with an enhanced read stability compared to having both or none of the devices strained.

In standard cell design, in order to reduce cell placement complexity, strain and other layout dependent effects (LDEs) are preferred to remain low or have a constant effect, similar for both transistor types [4], [6]. This way, the performance of a logic gate does not depend on which gate is placed next to it. This is not the case in SRAM cells, where the surrounding cells are always known, this is true even for the cells at the boundaries of the array. Therefore, we can take advantage of LDEs in an SRAM array to maximize the performance of the memory.

The regular layout of SRAM arrays makes them a good candidate to achieve long uncut fins that maximize the effects of stress in pMOS. Many transistors are built over the same fin, such as the pass-gate and pull-down in a regular 6T SRAM cell. In addition, surrounding cells are symmetrical sharing the connections at the edges of the cells, this allows fins to go across different cells without being cut, even across the whole SRAM array.

Unfortunately, SRAMs that occupy large areas of nowadays SoCs [7] are particularly affected by local device mismatch, which reduces their reliability. Variability is expected to keep increasing as the size of the devices gets reduced, even if FinFET technology reduces the device mismatch, it is still a major design concern [8], [9]. Thus, the design of SRAM cells has to take care of mismatch and must ensure both read stability and write ability, still presenting good speed and power metrics.

In this study, we bridge the gap between technology advances and circuit design by introducing the complementary SRAM (CSRAM) cell. This cell uses pMOS transistors for the pass-gates obtaining long fins in the pull-up pass-gate path, besides, the fin that builds the pull-down is now cut. This maximizes the benefits of stress for all the three devices. We apply this new design to both 6T and 8T cells tuned to maximize stability when different variability scenarios are considered.

The use of pMOS pass-gates does not bring any physical challenge since the layout of the whole array remains the same than a regular SRAM cell for all the contacts, metal layers, fin sizes, device gates, and active areas. Only the device types are exchanged: nMOS transistors in regular SRAM become pMOS transistors, and transistors that were of pMOS type in regular cells now become nMOS transistors. Particularly, the size of the cells remains exactly the same.

The structure of this paper is as follows. In the next section, we introduce the CSRAM cell, presenting the main differences with respect to regular SRAM cells in its design and functionality. Then, we explain the methodology that has been carried out to compare regular and CSRAM cells under variability, analyzing 6T and 8T cells. Finally, the speed, stability, and mismatch results are presented and some conclusions are drawn.

II. CSRAM Cell Overview

Knowing that pMOS transistors are improved if the length of their fin is increased and that the opposite happens to nMOS devices, we want to find an SRAM cell design whose pMOS transistors are built on long fins and nMOS transistors on short fins. As shown in Fig. 2, a regular SRAM cell presents just the opposite characteristic (long nMOS fins and short pMOS fins). Therefore, a way to achieve a significant improvement in a tensile strained FinFET technology is to use the complementary cell exchanging nMOS and pMOS devices. We will apply this approach to both 6T and 8T SRAM cells.

The idea of designing SRAM cells with pMOS transistors in pass-gates is not new, pMOS pass-gates were used in [10] to ease the data write operation. Razavipour *et al.* [11] proposed a cell with pMOS pass-gates in order to reduce the overall gate leakage currents and, thus, the static power dissipated by

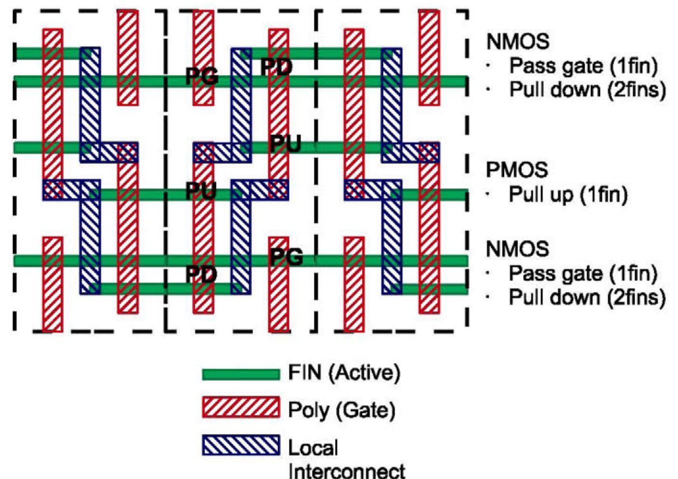


Fig. 2. Layout of three regular 112 FinFET SRAM cells, the pull-up fin is cut, as well as one of the fins of the pull-down. The pass-gate as well as the second fin of the pull-down extend all across the memory array.

the memory. However, to the best of our knowledge, this is the first time that pMOS pass-gates are used to take advantage of the different effects that strain has on pMOS and nMOS FinFET devices.

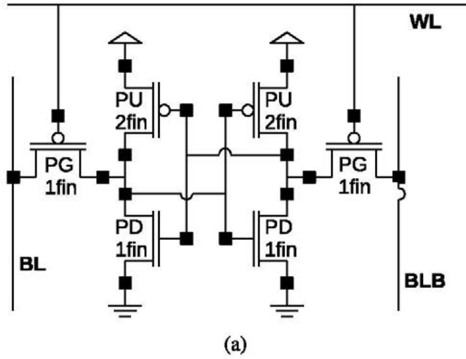
A. Complementary Cell Design

By exchanging pMOS and nMOS devices in the cell layout, the transistor next to the pass-gate is now the pull-up, and the pass-gate is now a pMOS device, both transistors are built with the same fin. In addition, thanks to the symmetry of an SRAM cell, this same fin is extended even more in the neighbouring cells to the right and left and it is only cut at the bounds of the SRAM array. Moreover, what used to be the pull-up becomes now the pull-down and consists on a short fin, which improves the transistor in the case of an nMOS device.

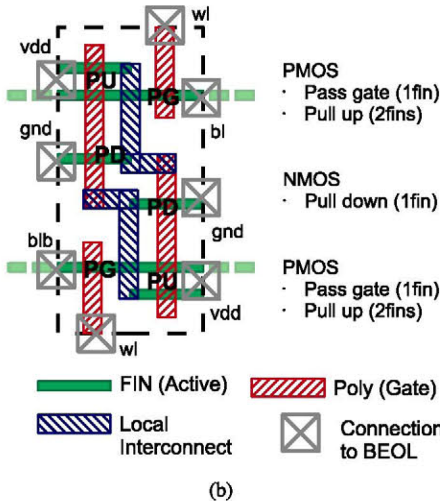
The whole layout of the SRAM array remains the same as only the type of transistor has been changed but not its size or position, as shown in Fig. 3. Also the metal layers and connections remain the same, with the difference that the lines carrying V_{dd} and ground have been exchanged. As the same layout is used, there is no area penalty with respect to the regular cell. The active power of the memory array is due to the charge and discharge of the word-line and bit-line large capacitances. These capacitances are due to the metal lines, that remain unchanged, and so it does the active power.

With this configuration, we make sure that the fins in the nMOS pull-down are always cut leading always to an improved device in our target strained technology, meanwhile at least one fin of the pull-up and pass-gate remains uncut. More generally, the device with fewer fins from pull-up and pass-gate sets the number of uncut fins by both devices, if one of the transistors has more fins than the other (usually the strong pull-down, the pull-up in our case), these fins are cut.

In the case of an 8T SRAM cell, all the previous premises can be directly applied as the 8T cell reuses the layout of a 6T cell. In addition, we exchange the two transistors added for the

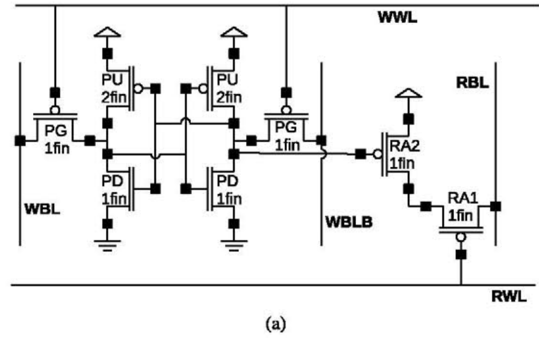


(a)

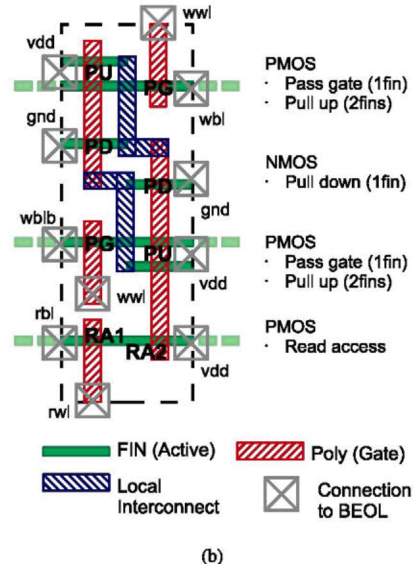


(b)

Fig. 3. 6T 112 CSRAM cell schematic and layout. The layout includes connections to back end of line but the metal layers are skipped for improved visibility. Uncut fins are extended with dashed lines. (a) Schematic (b) Layout.



(a)



(b)

Fig. 4. 8T CSRAM cell with 112 core and 1-fin decoupled read circuitry schematic and layout, the decoupled read circuitry at the bottom of the layout is made out of a long fin. (a) Schematic (b) Layout.

decoupled read circuitry from nMOS to pMOS devices, this will provide faster devices as they are made out of the same fin. The schematic showing the pMOS read access transistors of an 8T SRAM cell and its layout are shown in Fig. 4. Two fins are used in the pull-up of the 8T cell to ease the comparison with the 6T cell, even though the simulations for the 8T cell will use a different topology (see Section III).

B. Complementary Cell Operation

Using a complementary cell not only consists on using a pMOS pass-gate, also the pull-up and pull-down transistor roles are switched. While a regular SRAM cell has a weak pMOS pull-up and a strong nMOS pull-down, in a CSRAM cell the pull-up has now the role the pull-down used to have, and thus, we need a strong pull-up. In the same way, in the CSRAM the pull-down is a weak nMOS transistor.

The consequences are that all the periphery signals must be changed now. During a read process, the bit-lines are not precharged to V_{dd} but discharged to ground before leaving them floating. Then the word-line, charged to V_{dd} in idle mode, is discharged to ground. This activates the pMOS pass-gates and the bit-line next to the cell that stores a '1' will be charged through the pull-up pass-gate path.

The write access is more similar to a regular SRAM cell. One of the bit-lines is set to V_{dd} while the other is set to ground. The write starts when the word-line is discharged to ground. While the main write process in a regular SRAM cell is performed by the bit-line that is tied to ground, overtaking the effect of the weak pull-up, in the CSRAM it is done by the bit-line charged to V_{dd}, overtaking the weak pull-down.

Fig. 5 shows the operation of a CSRAM cell. First, a write operation is performed by pulling up the corresponding bit-line while the word line is pulled down. The same bit is then read by pulling down the word-line again, while the bit-lines initially discharged are left floating. The cell charges one of the bit-lines making a differential voltage appear which will be detected by the sense amplifier.

We can see that the signals are opposite with respect to those of a regular SRAM cell, thus, any strategy to improve SRAM speed or reliability [12] will also be applicable to the complementary cell design, including V_{dd} tuning, word-line boosting (the same effect will be obtained driving the word-line below zero during read and write), or negative bit-line voltages (the equivalent for CSRAM consists on driving the selected bit-line above the nominal supply voltage during write).

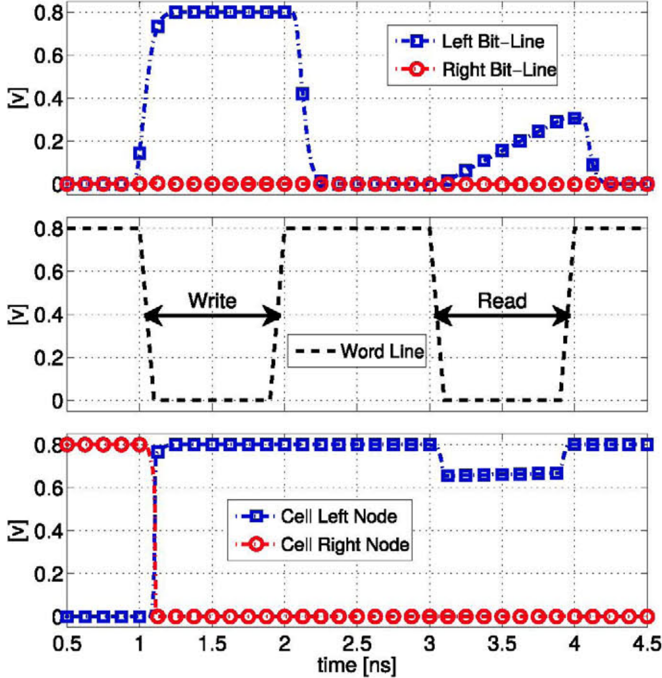


Fig. 5. Simulation of CSRAM operations.

In the case of an 8T SRAM cell, the write process is the same. However, the read process starts by setting the read word-line to ground which will result on charging the read bit-line depending on the data stored in the cell.

III. Methodology

In this study, we analyze two kinds of cell design: 6T cells and 8T cells. Each design can be implemented with different transistor sizes which in FinFET technology is defined by the number of fins the transistor has. We call *topology* the combination of different fin numbers for each transistor in the SRAM cell. The topology determines the area of the cell, that is, every 6T cell having a 123 topology will have the same area, regardless to whether transistors are pMOS or nMOS, or to which voltage we tune their threshold voltage.

Three numbers define the topology, for example 123 means one-fin pull-ups, two-fin pass-gates and three-fin pull-downs in the case of a normal cell, the order is pull-down, pass-gate, pull-up in the case of CSRAM cell. This is done to keep the role the transistor has in the cell as explained in Section II-B.

For this work three different 6T SRAM cell topologies have been analyzed: 111, 112, and 123. For each topology both regular SRAM cells and their corresponding CSRAM cells are simulated. Given that the conclusions were the same for the three topologies, we have only considered the one fin per transistor topology for the 8T cell.

A. Work Flow

For a given topology, different cell performance and stability tradeoffs can be made by tuning the threshold voltage of the transistors (Vt). Also the gate length (Lg) can be slightly changed while keeping the poly-pitch constant and, thus, not altering the area. For the 8T topology, we also allow to tune the gate length and threshold voltage of the two transistors in the read path, in addition to the other transistors already used in the 6T topology that are still present.

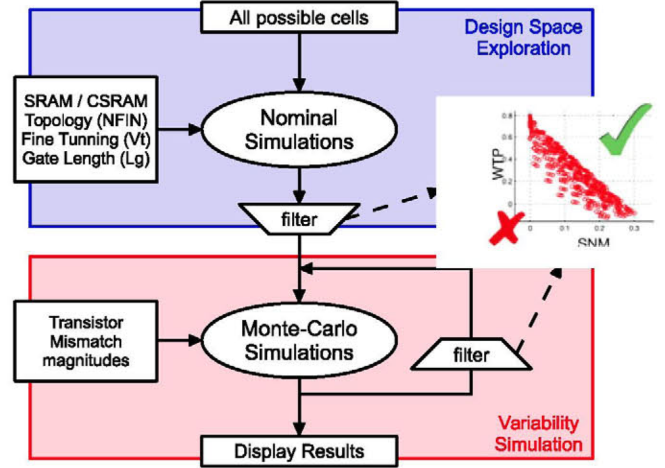


Fig. 6. Validation Work flow.

As summarized in Fig. 6, the process starts by the *design space exploration* phase (blue on top of the figure). This step consists of simulating the nominal performance and stability metrics of all possible combinations of Vt and Lg for a given topology. This allows us to discard cells that will not match a given threshold of performance. This is represented as a filter in the figure.

All the cells that are not discarded in the previous phase go then through the *variability simulation* phase (red at bottom of Fig. 6). Monte-Carlo simulations are carried out to obtain the final results under threshold voltage and drain–source current mismatch.

Optionally, the variability simulation step can be repeated, simulating the most interesting cells according to the last results and discarding the rest. Since less cells are now simulated, we can increase the number of Monte–Carlo points that are simulated.

B. Technology Assumptions

We have used for this study the predictive compact model for 14-nm FinFET technology from [4]. The impact of the different strains is modeled by altering the mobility of charge carriers in the BSIM-CMG model cards of the transistors, depending on the fin extension at the sides of the transistor gate. This is carried out according to TCAD simulations. The device has a fin height of 30 nm, a fin width of 10 nm, and a nominal gate length of 20 nm. The nominal power supply is 0.8 volts.

Transistors made out of several fins are treated as one-fin transistors in parallel applying the strain effect to each individual fin depending on whether it is cut or not. The physical dimensions of the design are the same in regular SRAM and CSRAM cells,

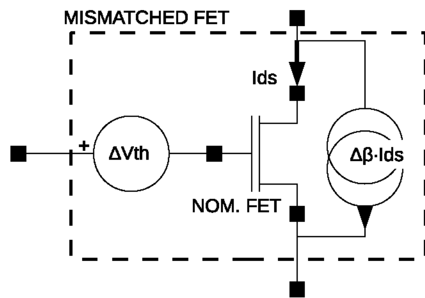


Fig. 7. Voltage and current sources used in the two-injectors method to model threshold voltage and drain-source current variability respectively.

and so are the metal layers. As a consequence, the parasitics and the capacitive load of the bit-lines are the same in both designs for a same number of fins. This allows us to compare the speed of the cells through the current they are able to sink from the bit-lines, without knowing the absolute figures of the capacitance.

As in FinFET, the threshold voltage of the transistor is tuned by modifying the gate work-function [13], we assume that the Vt of each transistor in the cell can be individually set.

Since the technology is predictive, there is no variability information in the compact model. Thus we model the variability following the two-injector method [14], inserting voltage and current source generators as shown in Fig. 7. The first injector models the variability in the threshold voltage through the parameter AVt, which is dependent on the fabrication process. The parameter AVt links the area of the transistor gate to the standard deviation of the mismatch of its threshold voltage following the formula $\sigma Vt = \mathrm{AVt}/\sqrt{\mathrm{Area}}$. In the case of a FinFET transistor, the area of a one-fin transistor is calculated using a width equal to twice the fin height plus the fin thickness [15] so that $\mathrm{FinFET_{Area}} = N_{\mathrm{FIN}} \times L \times (2 \cdot H_{\mathrm{FIN}} + T_{\mathrm{FIN}})$. The other mismatch parameter modeled is the drain-source current, and it is derived through the correlation it has to the threshold voltage mismatch in previous technology nodes.

Since the purpose of this work is to compare two different SRAM cell designs, the actual value used for AVt does not affect the conclusions as long as the same value is used for both simulations. Nevertheless, we used an AVt of $1.2\ \mathrm{mV} \cdot \mu\mathrm{m}$ that seems to be a realistic value according to the literature [16].

In a first experiment, the same AVt is used for both nMOS an pMOS transistors so that the comparison between regular and CSRAM is unbiased. In addition, to compare the sensitivity of regular and CSRAM cells to a different magnitude of mismatch [17], [18] in the nMOS and pMOS devices, some cells were simulated again. These new simulations included mismatch spreads scaled differently for the two transistor types, proving the different effects on cell yield that mismatches of pMOS and nMOS devices have.

C. Simulated Metrics

Following the proposed methodology, only the cells that presented an optimal nominal read stability and write ability tradeoff were simulated under variability. The results of the stability metrics under variability can be used to predict the yield of a cell. A cell will fail if it presents a value below a given threshold for either read or write static noise margin. A failure probability is calculated knowing the spreads and correlations of these two metrics, assuming they fit a two-dimensional Gaussian distribution [19]. The failure probability of the individual cells will determine the yield of a whole SRAM array. An SRAM array fails if one or more than one of its cells fails. We do not need to simulate the full array, but only a single cell; however, this cell takes into account the fin extensions that would propagate in adjacent cells if the cell were included in a full array.

The speed of an SRAM array is limited by the read operation, as it is a small cell charging or discharging the large capacitance of the bit-line. Other factors such as the charge and discharge of the word-line, or the charge and discharge of the bit-lines during a write access are carried out by the periphery, and thus, are less affected by variability. The charge or discharge of the bit-line during a read operation will depend on the amount of current that the cell can sink or deliver through the pass-gate, and the size of the capacitance that has to be switched. The later parameter is unknown until the memory size is set. Nevertheless it does not matter if the cell is a regular SRAM cell or a CSRAM, given that they have the same topology and have been built using the same technology, the capacitances of the bit-lines will be the same in both regular and complementary designs. As a consequence, we take the read current as a parameter to measure the speed of the cells. However, no comparisons can be done between two different topologies, since cells with different number of fins will add a different load to the bit-line and word-line, in addition to the different size of the cell across different topologies.

The metric used to show the speed of a cell under variability is the mean value of the read current minus six standard deviations (6σ), which is enough to ensure the yield of the memory will not be limited by its speed. Similar results are obtained with a less restrictive metric.

IV. Results

A. Stability and Speed Results for 6T CSRAM

We carried out Monte–Carlo simulations of 6T cells for 111, 112, and 123 topologies. The read and write static noise margins, represented as mean over standard deviation ratio of all the cells for each topology are shown on the left plot of Fig. 8(a)–(c). This metric is better than the nominal or mean values of the metrics as it takes into account both the mean and standard deviation. The greater these metrics are the better the yield the cell will have. Also the best cells will be located at the point where both ratios are similar ($x = y$ diagonal), otherwise either read stability or write ability failures will dominate, reducing the overall yield.

A line joins all the results in the optimal Pareto front of the two metrics. Regarding stability there is no clear advantage of one cell over the other, except for the 111 cell, which presents better metrics for the CSRAM cell.

The plot on the right of Fig. 8(a)–(c) shows the one-cell failure probability of all simulated cells against the speed of the cells, as well as the optimal Pareto front of the two metrics. We can see that thanks to the increased mobility that the continuous

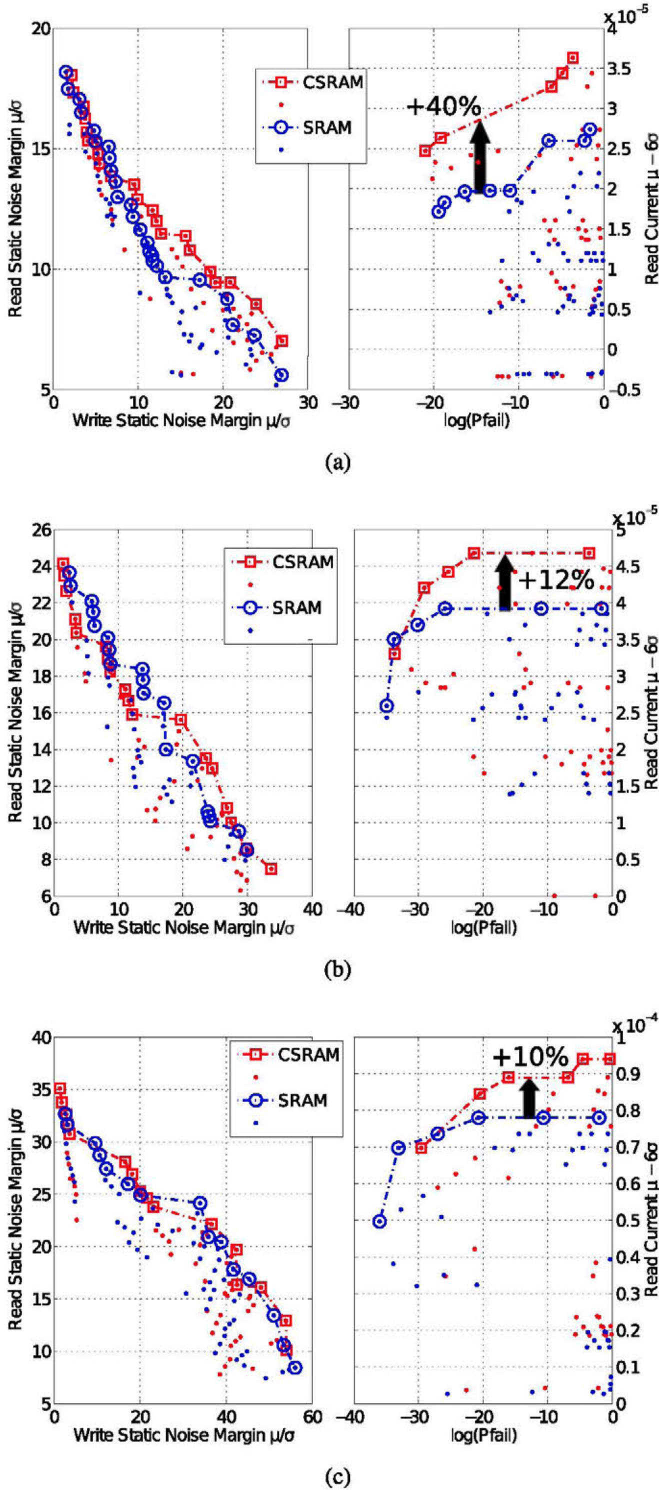


Fig. 8. Read and Write stability metrics (left) and Failure probability versus read current (right) of a 111 (a), 112 (b), and 123 (c) SRAM cell compared to a complementary cell.

fin brings to the transistors in the pass-gate pull-up path, the CSRAM cells are faster for a same yield.

The speed improvement turns to be higher in the 111 topology, as the number of fins is the same in the two transistors of the read path, all the fins are uncut, and thus, their speed is improved.

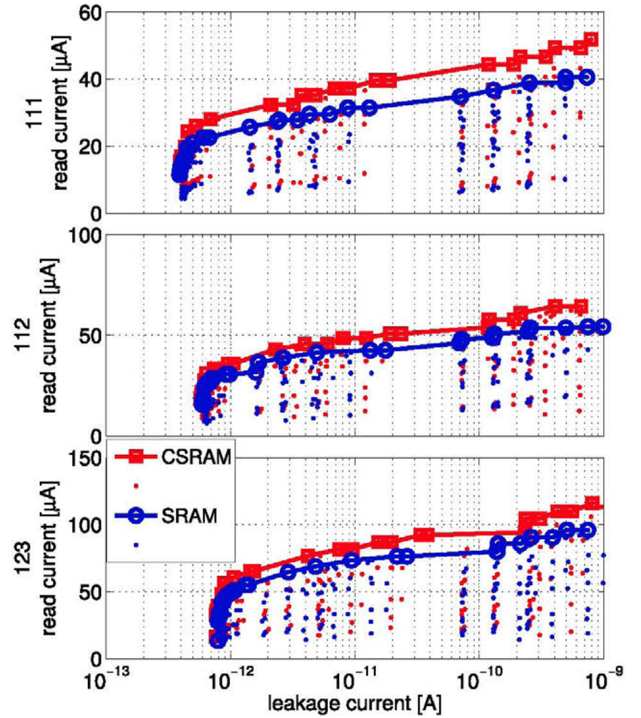


Fig. 9. Comparison of leakage versus read currents of CSRAM and regular SRAM, for the three cell topologies considered.

On the other hand, only the fins shared by both the pass-gate and the pull-up get uncut in the 112 and 123 configurations, leaving a fin in the pull-up cut, and thus, showing a lower speed improvement than for the 111 configuration.

As explained before, the active power consumption is due to the charge and discharge of the bit-lines and word-lines. Since those tracks are built in the same technology and have the same dimensions for a same cell topology, their capacitive load is the same and so it is the active power consumption. Fig. 9 compares the leakage current against the read current of CSRAM and regular SRAM, for the three cell topologies considered. It can be seen that for a given leakage current, the CSRAM presents a higher read current, thus, the speed improvement of the CSRAM cell is not obtained at the expense of an increase of the leakage power.

B. Complementary 8T Cell

Unlike 6T SRAM cell, where an enhancement in read or write static noise margin is always achieved at the expense of the other parameter, a read operation introduces almost no disturbance in the 8T SRAM cell thanks to the decoupled read circuitry. This can be clearly seen in the plot on the left of Fig. 10 as both metrics can be improved almost independently.

The differentiated read circuitry also allows us to achieve the desired read current without modifying the six transistors that hold the data and the write operation. This is shown on the right plot of Fig. 10, the 8T SRAM cell shows a flatter speed behavior for the range of failure probabilities, for both regular and complementary cells. As happened with 6T CSRAM cells,

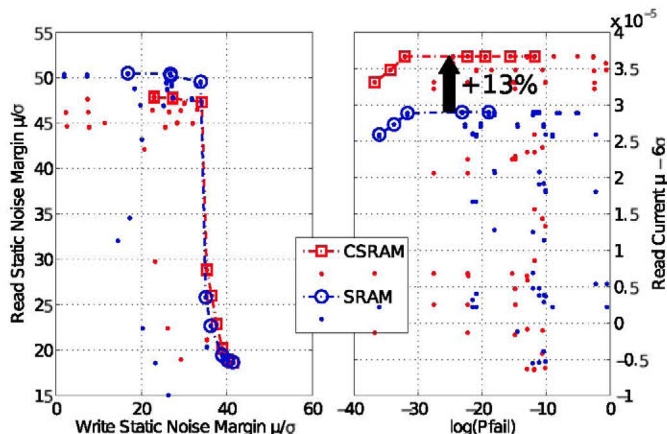


Fig. 10. Read and Write stability metrics (left) and Failure probability versus read current (right) of a 8T SRAM cell compared to a complementary cell.

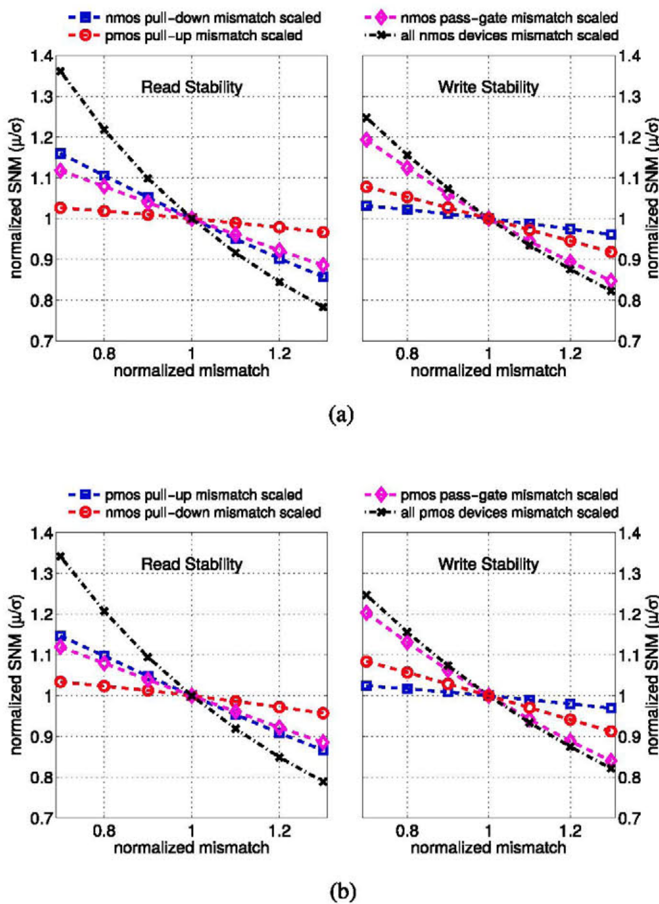


Fig. 11. Sensitivity of the cell read (left) and write (right) stabilities to the magnitude of the mismatch on different transistors for regular SRAM (a) and CSRAM (b).

8T CSRAM cells also show a faster read speed for a same target yield.

C. Biased Mismatch Dependence

For the previously exposed results, we have assumed that the fabrication process has an AVt factor of 1.2 mV · μm equal for both nMOS and pMOS transistors. This is not always true due to the different materials involved in the fabrication of the two devices, they can present different mismatch factors that differently affect the yield of the memory, depending on the kind of device that is used for each transistor in the SRAM cell. Fig. 11(a) and (b) shows the effect of mismatches of different magnitudes for pMOS and nMOS devices.

We can see in Fig. 11(b) for regular SRAM cells that a change in nMOS variability translates into a higher change in stability than the same change in pMOS variability. Both nMOS pull-down and pass-gate devices contribute to this sensitivity in the case of read stability while for the write stability this is mainly due to the pass-gate.

When CSRAM cells are considered [see Fig. 11(b)], the stability presents a higher sensitivity to the variability of pMOS devices. Again the pass-gate is the major contributor during read, while both pMOS pull-up and pass-gate contribute during write operation.

The results shown in Fig. 11(a) and (b) were obtained for cells using 111 topology. 112 and 123 topologies led to the same conclusions.

During a write access, the pass-gate is the most sensitive device as it has to overtake the weak pull-up in the case of a regular cell, or the weak pull-down in the case of a complementary cell. During a read access, the two transistors of the same type that make the current sink are the ones that limit the sensitivity: the nMOS pass-gate pull-down path in the case of a regular cell, or the pMOS pass-gate pull-up path in the case of a complementary cell. Weak pull-up or pull-down play a minor role during read access, and thus, stability is less sensitive to their mismatch.

As expected, cells are more sensitive to the mismatch of the dominant type of transistor they are made of. This goes with the transistors that are more involved in the write and read operations, that limit the yield of the cell.

This means that in addition to a faster operation, CSRAM cells are more suitable for technologies that present a greater mismatch magnitude in the nMOS device than in the pMOS device, as in the case of the FinFETs presented in [17] or some of the devices in [18].

V. Conclusion

In this paper, we have analyzed the possibility of using CSRAM cells to take advantage of the enhanced pMOS devices that tensile stress provides in FinFET technology. Since the benefits of strain increase as the fin is extended in the source and drain sides, the proposed CSRAM cell allows the same fin to be used in the pass-gate and pull-up and to be extended across neighbouring cells all along the SRAM array. This CSRAM cell has the same physical layout than a regular cell and as a consequence it does not entail any penalty in area nor manufacturing.

Results of Monte–Carlo simulations under mismatch have shown that CSRAM cells provide an increased read speed of at least 10% and up to 40% in some cases compared to an equivalent regular SRAM cell with the same area and for a same yield target. These results can be extended to 8T SRAM cells.

CSRAM cells have also shown to be less sensitive to nMOS mismatch than to pMOS mismatch, as opposed to regular SRAM cells that are more sensitive to nMOS mismatch. CSRAM cells will therefore throw a better yield in technologies where nMOS mismatch is more important than pMOS mismatch which appears to be the case of many FinFET based technologies in the literature.

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