DCIS XXVIII

November 27-29, 2013

Donostia- San Sebastian

28th Conference on Design of Circuits and Integrated Systems (DCIS 2013)

session 7A. Special Session. Variability and Reliability
room: Zarautz
chairs: -

09:00 – 10:20

A great challenge for future information technologies is building reliable systems on top of unreliable components. Parameters of modern and future technology devices are affected by severe levels of process variability and devices will degrade and even fail during the normal lifetime of the chip due to aging mechanisms. These extreme levels of variability are caused by the high device miniaturization and the random placement of individual atoms. Variability is considered a "red brick" by the International Technology Roadmap for Semiconductors. The session is devoted to this topic presenting research experiences from the Spanish Network on Variability called **VARIABLES**.

Variables network overview
A. Rubio / M. López Vallejo
Modeling sub-threshold slope and DIBL mismatch of sub-22nm FinFet
Pablo Royer and Marisa López-Vallejo
Time-dependent variability of CMOS differential amplifier performance evaluated with RELAB, a tool for circuit reliability simulation
J. Martin-Martinez, M. Moras, R. Rodriguez, M. Nafria, E. Roca, F. Fernández
Experimental analysis of SER variability in CMOS nanometer SRAMs
Gabriel Torrens, Sebastià Bota, Jaume Segura
Fault-tolerance techniques for variation-aware design
Luis Entrena
CHAOS-BASED DIGITAL LOGIC IMMUNE TO NOISE AND RADIATION
Vicenç Canals, Antoni Morro and Josep L Rosselló
A new tuning approach for OTA-C filters aimed at compensating PVT variations
J. Font, E. Isern, M. Roca, R. Picos and E. García-Moreno
Partial design-based compensation of process variations in LNAs
Jorge González, Juan C. Cruz, Diego Vázquez, Adoración Rueda
CMOS Retina Sensibility Improvement by Enhancing Mismatch Inmunity
Teresa Serrano, Bernabé Linares
Impact of Variability and Aging in the N-MR Fault Tolerant architecture
Antonio Rubio

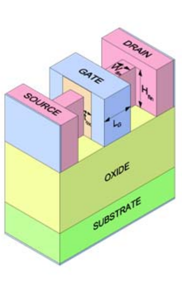
Modeling sub-threshold slope and DIBL mismatch of sub-22nm FinFet

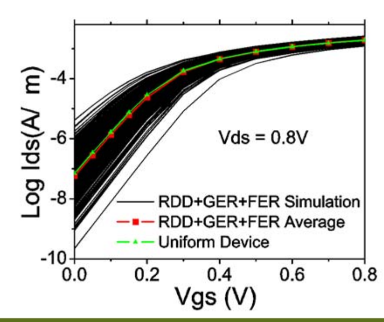
Pablo Royer, Marisa López Vallejo

DCIS 2014

Introduction

- New sources of mismatch in sub-22nm:
  - Fin edge roughness induce important **sub-threshold slope** variations
  - Fin and gate edge roughness also introduce important **DIBL** variability



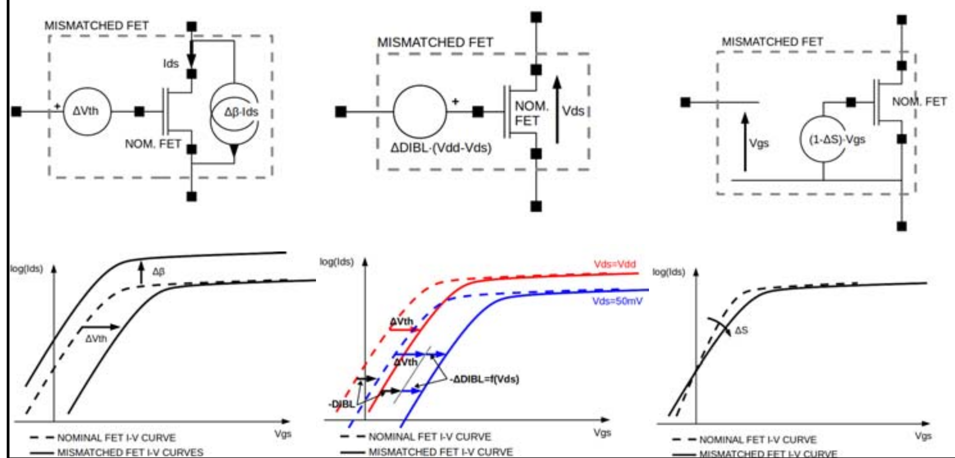


Approaches

- Statistical compact model: “real” variations for commercial devices
- Injectors modeling: less accurate, but
  - We can vary electrical parameters rather than physical parameters of model card
  - Can be used before the statistical compact model is available
- Play a key role when working with predictive technologies

New injectors

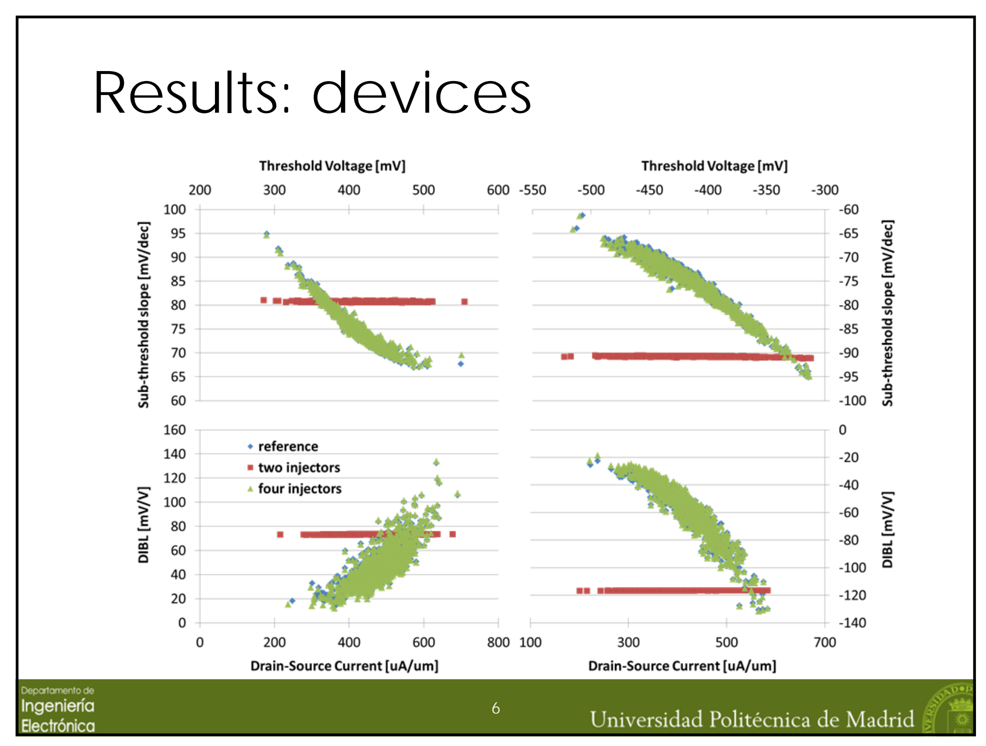
- We reproduce **at circuit level** the new sources of variability not considered in traditional threshold voltage and drain-source current injectors

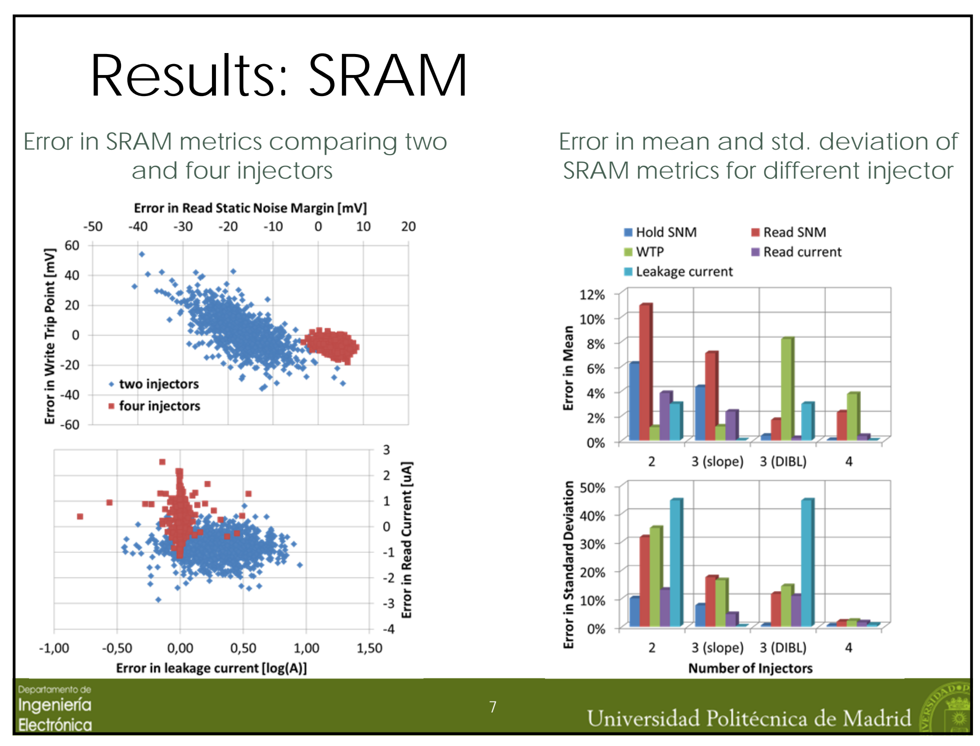


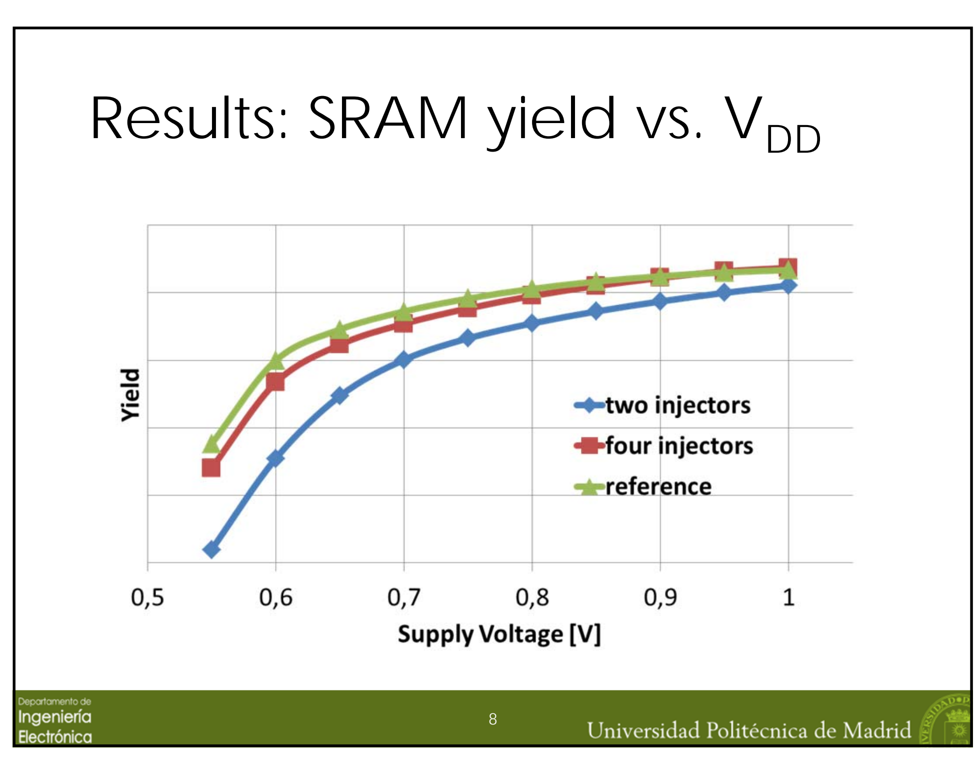
Benchmark

- 1000 N and P **10nm FinFET** devices obtained by the atomistic simulator Garand, University of Glasgow
- The sources of variability considered were:
  - Fin edge roughness (FER)
  - Gate edge roughness (GER)
  - Random dopant fluctuation (RDD)
- Validation: one to one comparison
  - Devices: figures of merits of transistor (I_{on}, I_{off}, DIBL, SSL, V_{th})
  - 6T SRAM cell: R&W stability, speed and power metrics
  - SRAM Array: yield

Results: devices




Results: SRAM
Error in SRAM metrics comparing two and four injectors
Error in mean and std. deviation of SRAM metrics for different injector
Error in Read Static Noise Margin [mV]
Error in Write Trip Point [mV]
two injectors
four injectors
Error in Read Current [uA]
Error in leakage current [log(A)]
Hold SNM
Read SNM
WTP
Read current
Leakage current
Error in Mean
Error in Standard Deviation
Number of Injectors
Departamento de Ingeniería Electrónica
7
Universidad Politécnica de Madrid


Results: SRAM yield vs. V_{DD}
Yield
two injectors
four injectors
reference
Supply Voltage [V]
Departamento de Ingeniería Electrónica
8
Universidad Politécnica de Madrid

Conclusions

- Injector-based variability modeling can work fo beyond 22nm technologies
  - New effects must be considered: DIBL and Subthreshold slope
- Approach validated through benchnarking