

# A Low-Area Reference-Free Power Supply Sensor

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**Abstract**—Power supply unpredictable fluctuations jeopardize the functioning of several types of current electronic systems. This work presents a power supply sensor based on a voltage divider followed by buffer-comparator cells employing just MOSFET transistors and provides a digital output. The divider outputs are designed to change more slowly than the thresholds of the comparators, in this way the sensor is able to detect voltage droops. The sensor is implemented in a 65nm technology node occupying an area of  $2700 \mu\text{m}^2$  and displaying a power consumption of  $50 \mu\text{W}$ . It is designed to work with no voltage reference and with no clock and aiming to obtain a fast response.

**Index Terms**—Power supply sensor, voltage sensor, reference-free, CMOS, analog-to-digital converter.

## I. INTRODUCTION

Power supply in current technologies has ceased to be considered a robust and trustable signal due to several instability sources. Glitches in the system that may affect the power grids,  $V_{DD}$  drops, voltage noise or the lack of a power supply are some examples of the problems that must be addressed. There have been several design-time approaches to minimize the impact of the fluctuations. However, power supply must be always monitored to flag a signal when certain security margins are surpassed. In the event that the supply voltage is too far above the operating range, or too low, an output of the power supply monitor can be used to deactivate the voltage supply itself or disable the powered circuits so that unreliable circuit operation does not occur.

Power voltage,  $V_{DD}$ , instabilities are most likely to appear in mobile or portable systems or in sensor networks that realize ubiquitous computing, where a battery or harvester is a need. In RFID systems the power is obtained by an external electromagnetic field, the RF signal. The low energy field is harvested and stored on a capacitor, which provides enough power for the RFID system. However, the stability of the signal is affected by environmental factors and if the source is moved or stopped. In any of these cases, a voltage sensor is needed to prevent malfunction. RFID systems have strict demands of area and power consumption; therefore any monitoring infrastructure must suppose a small overhead.

Also, nanometer technologies have exacerbated the problem of voltage droops in processor systems. For example, as seen on [1] the voltage-noise affects the system performance — for a 2.53 GHz Pentium 4 microprocessor using a 130 nm technology the power supply noise reduces clock frequency by 6.7%. In [2] it is shown that in the Power6 microprocessor for

high activity states, there is a 17% delay change due to power supply noise, which equates to a 200 mV droop at 1.1 V.

In processor systems, since power supply over/under shoots travel from where the current draw is highest to other parts of the integrated circuit, a control system tracking supply voltage droops will only need to allocate supply voltage monitors close to the circuits most responsible for dynamic current draw. Thus, relatively few power supply monitors are needed. However, compared to other circuit issues, such as temperature, supply voltage fluctuations have a much shorter time constant and they also demand much quicker actions. Due to all this, much care must be taken in the design of power supply sensors to reduce the response time [3].

Previous works in the literature have dealt with the problem of designing a  $V_{DD}$  sensor through several approaches. Some of them are based on analog cells, usually a comparator like in the work of Chun-Pong [4] which consists on a bandgap reference, a comparator and a resistor divider where the reference needed for the comparator is provided by the bandgap reference cell. Although the bandgap comparator is said to be insensitive to process variations, temperature and supply voltage, it uses some resistors and bipolar transistors which are especially sensitive to these issues. Also, it only senses one voltage level set by the voltage resistor, if a wide range of outputs is desired, the sensor should be adapted and replicated.

Other architectures have been proposed, like the one based on a differential stage, called mode selector [5] or the one based on the charging time of a capacitor, who is termed as Power On Reset [6]. Developing the latter, two more architectures are presented in [7]. All of these sensors only detect a established voltage level and they flag out a signal when it is reached.

In [8], the authors proposed a reference-free on-chip voltage sensor that is based on the different behavior (in terms of latency) of two circuits under the same voltage, through a voltage range. This sensor uses a clock to measure that difference and to generate the start/stop signal for the sensor. The main advantage of this work is the lack of a voltage reference however it has the drawback of needing a clock.

In this work we present a  $V_{DD}$  sensor structure that works without the need of both a power reference and a clock signal. The sensor has a resistor-like voltage divider where the voltage to be measured is split into different voltage values, each one is connected to the input of a cell called buffer comparator —the sensing stage in figure 2. When the input of the buffer comparator is over the inversion point of the cell,

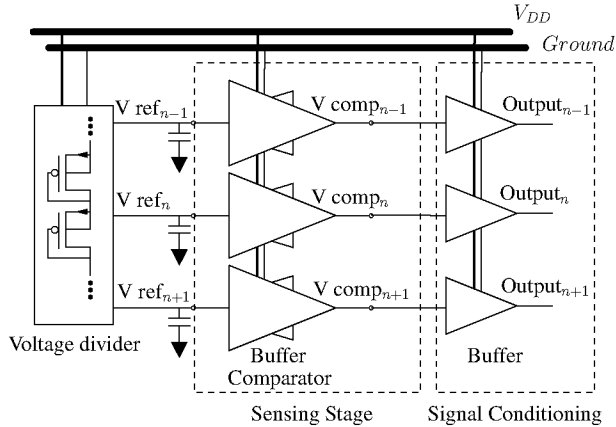


Fig. 1. Schematic of the voltage sensor.

the output goes up ( $V_{DD}$ ), and when the input is under the inversion point, the output goes down ( $Ground$ ), providing a thermometer code at the output. If the power supply varies, the threshold of the comparators is updated faster than the internal voltages of the divider due to the input parasitic capacitances of the comparator. This produces transitory changes at the output thermometer code which are proved to effectively detect voltage drops.

The main contribution of this work is the introduction of a novel  $V_{DD}$  sensor structure that does not need any clock or voltage reference apart for the one that it intends to monitor. A 65-nm implementation is characterized by the following features:

- The sensor is capable of measuring voltage drops in a short range of time  $\sim 5 ns$  delay time ( $V_{DD}$  steps were performed; from 1.2V to 0.9V aiming to reproduce a real power supply drop).
- The structure can be integrated in any standard CMOS circuit; it is just made of regular MOSFET devices.
- The output of the sensor is fully digital.
- The sensor displays an accuracy of 85 mV.
- Layout area: 2700  $\mu m^2$ .
- 50  $\mu W$  power consumption under repeated  $V_{DD}$  drops and recovers.
- Dynamic range, 1.7V - 0.8V.

The paper is organized as follows. Section II describes the design of the sensor, the building blocks and the complete sensor model. In section III we show the behavior of the system and characterize it. Finally, in section IV we discuss the results and draw some conclusions and future work.

## II. PROPOSED CIRCUIT

The voltage sensor proposed in this paper has four different blocks: a voltage divider, a sensing stage made of buffer-comparator cells, a signal conditioning stage and the control stage. In this section we will explain how these different blocks work. A schematic of the circuit is shown on figure 1.

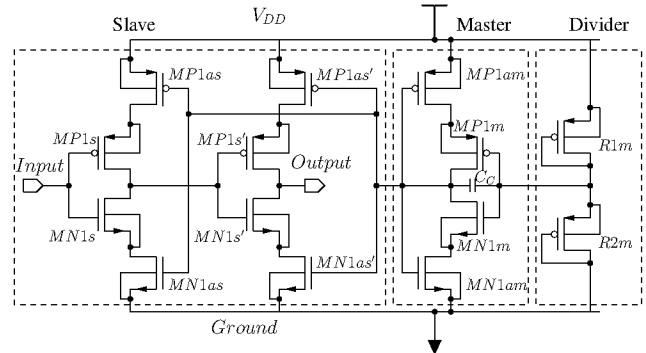


Fig. 2. Schematic of the Buffer-Comparator.

### A. Voltage Divider

The first stage of the sensor is a voltage divider made of series connected PMOS transistors. The usage of PMOS transistors is because they can be biased in such way that there is no body effect; the n-well of each transistor is connected to their source avoiding resistance discrepancies between the different transistors induced by this effect. The output voltage in each drain depends linearly on the number of transistors. The current circulating from  $V_{DD}$  to  $GND$  through the divider, dependent on the sizing of the transistors, will be responsible of the (dis)charge time of the intermediate nodes, thus in order to minimize the static power consumption and to extend the voltage retention it is interesting that the PMOS transistors are as resistive as possible.

### B. Buffer Comparator

The buffer comparator is the main cell of the sensor, as it provides a voltage-dependent output. The cell is used in various previous works in the literature, for example [9] and was presented originally in [10], where it was proved to be temperature and process invariant. The inverter cell presented in those works has been modified to work as a buffer, just by adding an inverter stage. This buffer comparator cell is divided into three parts as follows: A  $V_{DD}/2$  voltage divider, a master stage and a slave stage. A schematic of this cell is shown in figure 2.

The voltage divider is a two PMOS series connected transistors. The output voltage of this cell is going to be  $V_{DD}(t)/2$  no matter if  $V_{DD}(t)$  suffers variations. The master stage is an inverter that acts as a master switch which is fed by the fixed voltage divider. The second inverter is the slave switch.

How this comparator stage is tolerant to temperature and process variations is explained in detail in [9] and [10]. The main idea is to have the master switch in a state where its input is always below its threshold voltage. This is achieved with the  $V_{DD}/2$  voltage divider. If due to process or temperature variations, the threshold of the inverter (the slave stage) varies, the master stage leads to a variation of the PMOS or the NMOS resistances, pulling up or down the threshold of the inverter to compensate the variation.

### C. Signal Conditioning and Control Stage

These stages manage the digital output and interface of the sensor. Signal conditioning employs a standard buffer cell in order to have a CMOS logic value out of the sensor. This buffer is made with two minimum size inverters to achieve a high speed and small area. The control stage comprises the combinational logic that demultiplexes the thermometer code so that the output is binary quantization code of the measured voltage.

### D. Working Principle

Let us now explain a complete analytical model of the sensor. In the final architecture, the analog part of the sensor is shown in figure 1. A buffer-comparator cell is connected to each output of the voltage divider. Finally the digital signals are produced at the conditioning stage.

To understand how the sensor works, we can start from a static point of operation. At  $1.2V$ , the upper half of the comparators is high, logic "1", and the rest—the lower half—are down, logic "0". Employing the nomenclature of figure 1, this start point is where  $\text{Output}_{n-1} = 1$ ,  $\text{Output}_n = 1$  and  $\text{Output}_{n+1} = 0$ . From an analytical perspective, the voltage divider has a voltage  $V$  in each output  $n$  (count from  $n$  to ground) given by the following equation:

$$V_n = \frac{n}{m} \cdot V_{DD} \quad (1)$$

where  $m$  is the total number of PMOS resistors, all those resistors are equal. And if the threshold of the comparators is  $V_{DD}/2$ , the thermometer code changes from "0" to "1" when:

$$\frac{n}{m} \cdot V_{DD} > \frac{V_{DD}}{2} \Rightarrow n = \lceil \frac{m}{2} \rceil \quad (2)$$

When  $V_{DD}$  varies, the threshold voltage will follow the fluctuation much faster than the intermediate voltages at the divider due to the high output resistances of the PMOS transistors and the parasitic capacitances at the input of the buffer-comparator. From an analytical perspective, if there is a change in the power supply from  $V_{DD}$  to  $V_{DD} \pm \Delta V$ , with  $\Delta V > 0$ , and supposing an instantaneous response in the inverting threshold and no variation in the divider voltages, the new change in the thermometer code is produced at:

$$\frac{n}{m} \cdot V_{DD} > \frac{V_{DD} \pm \Delta V}{2} \Rightarrow n = \lceil \frac{m}{2} (1 \pm \frac{\Delta V}{V_{DD}}) \rceil \quad (3)$$

To illustrate this concept, figure 3 shows an example of a transient simulation of the sensor.  $V_{DD}$  is a sine wave from  $1.8V$  to  $0.6V$ , (red line on top of the figure), the thick line (in orange) is the comparator inversion point, the rest of the lines are some selected outputs of the voltage divider. As shown, these lines display lag a little behind  $V_{DD}$  and cross the inversion point at different  $V_{DD}$  values. When they are over it, the corresponding sensor outputs are high. Those who are under the inversion point are low. If  $V_{DD}$  varies, the outputs of the sensor change accordingly.

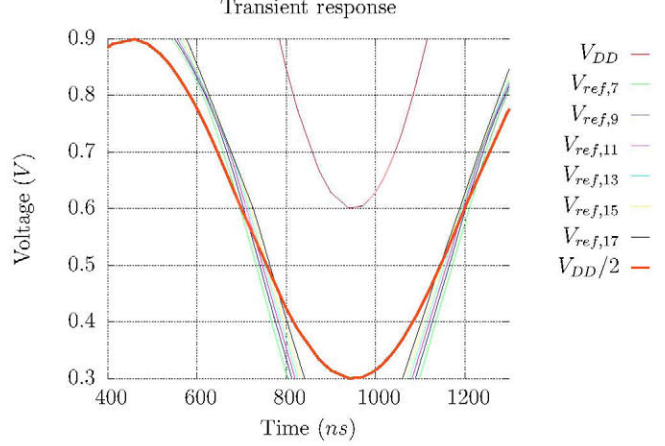


Fig. 3. Transient simulation of the sensor.

If the variation in  $V_{DD}$  is too slow, all the parasitic capacitors at the input of the comparators reach their final stable values  $n/m \cdot (V_{DD} \pm \Delta V)$  and the thermometer code returns to the original state no matter what the value of  $\Delta V$  is. An external control system is in charge of detecting the variations in  $V_{DD}$  registering any change in the output code. Ideally, the changes in the output code must be registered as soon as possible as the voltages in the divider will also evolve with  $V_{DD}$ . The fastest variation that the sensor is able to track is bounded by the buffer delay, while the slowest variation is limited by the RC constant governing the (dis)charge time of the parasitic capacitances. The sizing of the divider and the comparators are fundamental to control these delays.

Concerning the accuracy of the sensor, if we again suppose an instantaneous threshold change and no variation in the intermediate divider voltages, we can establish a relationship between  $m$ , the number of PMOS transistors in the divider, and  $\Delta V_{min}$ , the minimum  $V_{DD}$  variation that we can track. Let focus on the case when the power signal goes from a stable value of  $V_{DD}$  to  $V_{DD} + \Delta V_{min}$  which can be easily extended to any arbitrary initial condition. Imposing  $m$  to be an odd number, which optimizes the comparison at the middle of the interval, the thermometer code will change to ones at:

$$n = \lceil \frac{m}{2} \rceil = \frac{m+1}{2} \quad (4)$$

The accuracy of the sensor will be given by the minimum  $\Delta V_{min}$  that makes the  $n$ th bit change from "1" to "0":

$$\frac{m+1}{2} V_{DD} < \frac{V_{DD} + \Delta V_{min}}{2} \Rightarrow \Delta V_{min} > \frac{V_{DD}}{m} \quad (5)$$

There are several factors that degrade this expression of the accuracy such as the transient behaviors of the divider voltages, threshold variations in the comparators, the delay of the buffers and process and temperature variations. Note that the number of comparators can be significantly smaller than the stages in the divider depending on the system needs as

TABLE I  
BUFFER STAGE ANALYZED PARAMETERS. STANDARD SIMULATION.

Parameter	Simulated
Inversion point	0.615 V
Delay up	32.81 ps
Delay down	37.76 ps
Static current	2.06 $\mu A$
Dynamic current	2.33 $\mu A$

TABLE II  
BUFFER STAGE ANALYZED PARAMETERS. MONTE CARLO SIMULATION.

Parameter	Monte Carlo simulation values	
	Mean Value	Standard deviation
Inversion point	0.6165 V	0.0208 V
Delay up	34.86 ps	7.70 ps
Delay down	37.75 ps	2.07 ps
Static current	2.0649 $\mu A$	0.4782 $\mu A$
Dynamic current	2.3407 $\mu A$	0.4302 $\mu A$

probably just the central voltages will be needed; furthermore and adaptive not equally spaced scheme could be used for particular purposes.

### III. EXPERIMENTAL RESULTS AND COMPARISON

To test the correct behavior of the system we have designed a sensor and laid it out in a 1.2V TSMC 65nm CMOS process. The simulations and layouts have been carried out in the Cadence<sup>TM</sup> environment. The area of the sensor is 2700  $\mu m^2$ . All the characterization results come from post place-and-route Monte Carlo simulations taking a distribution of 100 test circuits —representing different technology corners and mismatch variations— to estimate the effects of fabrication uncertainties. The vendor, TSMC<sup>TM</sup>, provides with a description of the probability distribution for each parameter of the transistor model and mismatch variations. The sensor has 23 outputs that are able to measure a range of voltages from 0.8 V to 1.7 V achieving an accuracy of 0.85 mV.

The correct functioning of the buffer-comparator stage is fundamental for the design and some simulations are made in order to characterize it. The simulations show a good behavior of the cell both in standard and Monte Carlo simulations.

In a first experiment, we target the response time of the sensor focusing on the buffer-comparator. Figures 4(a) and 4(b) show the Monte Carlo simulation results for the buffer-comparator delay when the output changes to logic “1” and to logic “0”, respectively. Table I provides a summary of the buffer-comparator characterization.

Concerning the speed and power characterization of the complete sensor model, several transient simulations were carried out. First, in order to analyze the static power consumption, we started with a stable 1.2 V power supply. Then, a set of known  $V_{DD}(t)$  sine waves with varying frequencies were introduced. Finally, we simulated  $V_{DD}(t)$  drops based on expected real system fluctuations. Due to the stochastic behavior of the  $V_{DD}(t)$  variation in a system, we can simulate different kinds of drops in terms of intensity and speed and analyze the power consumption and the delay for each one.

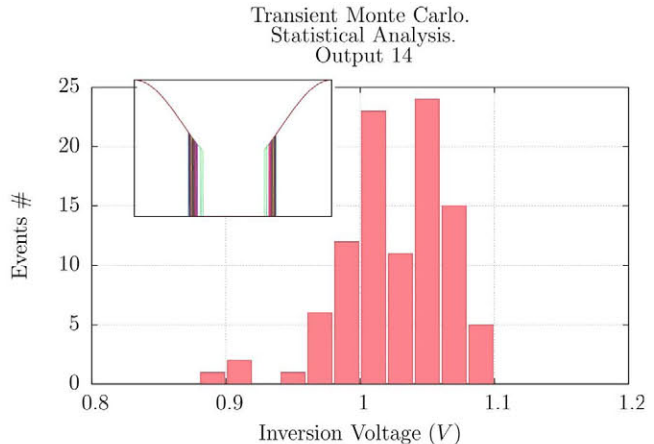


Fig. 6. Monte Carlo simulation and results for output-14.

Those simulations show an average delay of 5 ns when the voltage drops from 1.2 V to 0.9 V. With the same simulation —voltage drops— we have measured a power consumption of 50  $\mu W$ .

Focusing now on the accuracy, from the Monte Carlo simulations we can extract that the outputs of the sensor are highly dependent on both process variations and the sizing of the buffer-comparator. Figure 6 serves as an example to explain this, it shows the results for output-14. The smaller graph is a superposition of the transient simulations, it displays how the point where the output goes to 0 V —the threshold of the comparator— changes due to process variations. The bigger graph shows the distribution of the threshold.

In order to reduce this effect, the sizing of the buffer-comparator was specially tailored and optimized. The transfer function of the sensor without any calibration is shown in figure 7. After a full calibration we obtained an accuracy of 0.085 V. This calibration takes into account 100 Monte Carlo simulations for each one of the outputs. The error distribution histogram is in figure 8.

As far as the calibration process is concerned, it is interesting to mention that current on-chip DVFS systems under static conditions provide very robust and stable power supply values that could be used to automatically calibrate the sensor without the need of any external aid.

Table III summarizes the main characteristics of the proposed sensor and compares it with relevant works from the recent literature. As shown, this work overcomes previous ones in terms of area without the need of an external reference of any kind; furthermore it supposes a good compromise between speed, accuracy and power consumption and provides with digitized output.

### IV. CONCLUSION

Power supply over/under shoots or vanishing are serious issues that affect several types of current electronic circuits such as high-end processors or RFID systems. This work has presented a novel structure to monitor variations in the

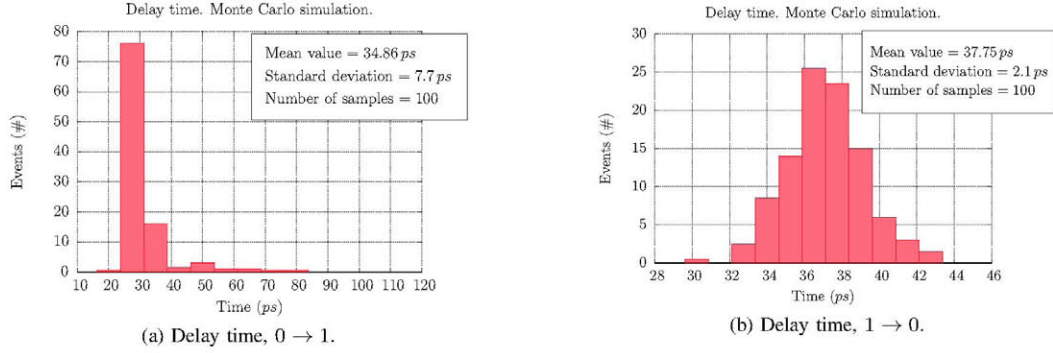


Fig. 4. Monte Carlo Buffer-Comparator Simulation Results.

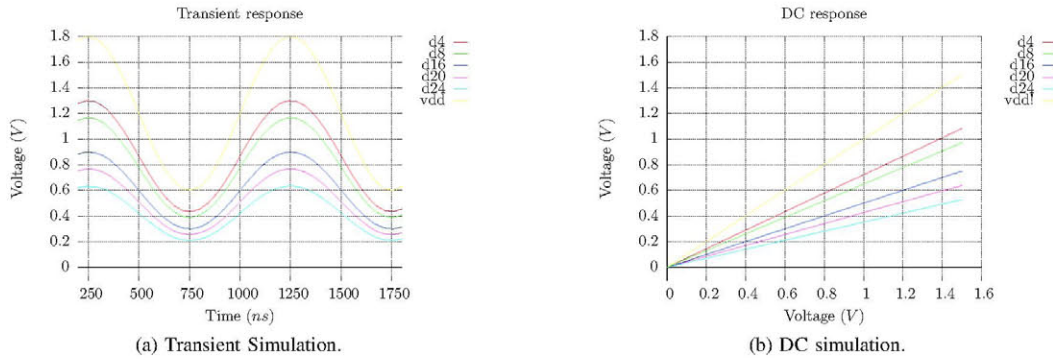


Fig. 5. Monte Carlo Voltage Divider Simulation Results.

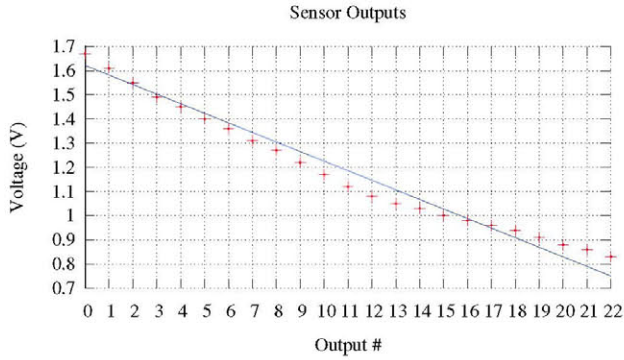


Fig. 7. Proposed sensor transfer function.

TABLE III  
COMPARISON WITH OTHER WORKS

	Present	Morales-Ramos [7]	Shang [8]
Delay	5 ns	-	1.85 ns - 872 ns
Power	50 $\mu$ W	0.28 $\mu$ W	778 - 338 $\mu$ W
Accuracy	85 mV	Single Threshold	50 mV-10 mV
Area	2700 $\mu$ m <sup>2</sup>	24950 $\mu$ m <sup>2</sup>	-
Reference	No	No	No
Clock	No	No	Yes
Technology	65 nm	0.35 $\mu$ m	90 nm

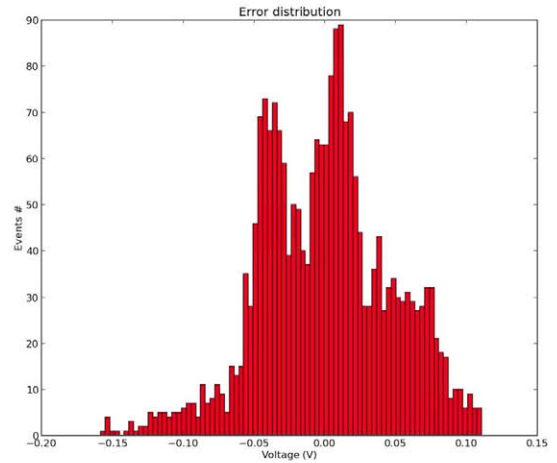


Fig. 8. Error distribution of the proposed power supply sensor.

power supply network. The sensor is designed to work with no voltage reference and no clock and intended to have a wide range of operation. Additionally it provides a digital output. The sensor has been laid out and simulated targeting the TSMC 65 nm node, taking an area of 2700  $\mu$ m<sup>2</sup>. The response time, when a simulated  $V_{DD}$  drop from 1.2 V to 0.9 V is about

5 ns with a maximum power consumption of  $50 \mu W$ . When compared to other previous works in the literature, the sensor presents a much reduced area and a very good compromise in terms of power, accuracy and speed.

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