Hybrid analysis of nonlinear circuits: DAE models with indices zero and one

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Abstract

We extend in this paper some previous results concerning the differential-algebraic index of hybrid models of electrical and electronic circuits. Specifically, we present a comprehensive index characterization which holds without passivity requirements, in contrast to previous approaches, and which applies to nonlinear circuits composed of uncoupled, one-port devices. The index conditions, which are stated in terms of the forest-structure of certain digraph minors, do not depend on the specific tree chosen in the formulation of the hybrid equations. Additionally, we show how to include memristors in hybrid circuit models; in this direction, we extend the index analysis to circuits including active memristors, which have been recently used in the design of nonlinear oscillators and chaotic circuits. We also discuss the extension of these results to circuits with controlled sources, making our framework of interest in the analysis of circuits with transistors, amplifiers and other multiterminal devices.

Keywords: differential-algebraic equation, index, electrical circuit, hybrid analysis, memristor.

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1 Introduction

Differential-algebraic equations (DAEs), also known as singular, semistate or descriptor systems, have played a significant role in circuit analysis, power systems and controls in the last three decades. From the seminal works in the 1970s and 1980s (cf. the 1971 paper of Gear [26], the papers of Luenberger in the late 1970s [45, 46], the "Pitman books" of Campbell [11, 12], the 1981 paper of Newcomb [51], and the 1986 and 1989 special issues of *Circuits, Systems, and Signal Processing* [41, 42]), DAEs have played an increasingly significant role as a modelling and analysis tool within these fields. Recent applications are reported in [2, 4, 21, 35, 37, 44, 47, 55, 56, 57, 67, 70, 71, 72].

In this context, the index characterization of differential-algebraic models of electrical and electronic circuits is a central problem in circuit simulation [23, 27, 28, 59, 68]. This is due to the fact that the index has a critical impact in the numerical techniques to be used in the simulation of circuit dynamics. The index is also relevant with regard to other analytical aspects, related e.g. to the non-degeneracy of the circuit, the state formulation problem or different qualitative issues [15, 24, 31, 65]. The reader is referred to [8, 29, 40, 39, 54, 59] for detailed introductions to the different index notions in DAE theory.

Much research in this direction has been focused on the characterization of the index of nodal models [22, 23, 59, 68]. This has been mainly motivated by the use of nodal techniques such as Modified Nodal Analysis (MNA) in circuit simulators, notably in SPICE and its commercial variants [27, 28, 55]. Under passivity assumptions, the index of nodal models is known to be not greater than two, according to the results in [23, 68].

By contrast, recent research has been focused on so-called *hybrid models*, whose origin can be traced back to [38] (cf. also [3, 7, 13, 30, 64]). The recent use of a differential-algebraic formalism to accommodate hybrid models has made it possible to show that their index does not exceed one in passive contexts [35, 36, 67], in contrast to MNA and other nodal techniques, for which certain configurations yield index two systems. This result, which reflects an index reduction implicit in the formulation of the model, is of great interest from the computational point of view, since index two DAEs are known to be more involved and to pose more difficulties than lower index problems, specially when they do not admit a Hessenberg form.

However, the working setting of [35, 36, 67] assumes that the circuit devices are strictly locally passive; this means that the incremental circuit matrices are positive definite everywhere. This excludes, for instance, the nonlinear resistors arising in Van der Pol's type nonlinear oscillators or in Chua's circuit, just to name some very relevant examples; the presence of a locally active resistor supports the oscillatory or chaotic behavior (respectively) of such circuits. Additionally, many modern circuit devices such as tunnel diodes or Josephson junctions do not meet the passivity requirement at certain operating regions [17]. For these reasons it is important to extend the index analysis to non-passive contexts: this defines the first goal of the present paper. Actually, we will arrive at a virtually complete characterization of the index of hybrid models of circuits composed of one-port (two-terminal) devices, as far as no coupling effects are displayed (cf. Theorems 1 and 2 in Section 4; it is

worth mentioning that, by contrast, the index analysis of passive problems carried out in [35, 36, 67] accommodates coupled devices). We will also discuss how to extend our results to circuits with multiterminals and controlled sources, so that they can be used in circuits with transistors, amplifiers, etc. (cf. Example 3 in Section 6).

Our second goal is to extend the formulation and the analysis of hybrid models to memristive circuits. The memory-resistor or *memristor* is an electronic device defined by a nonlinear relation between the charge and the flux, and its existence was predicted by Leon Chua in 1971 for symmetry reasons [14]. The report in 2008 of a nanoscale device with a memristive characteristic [66] had a great impact in electrical and electronic engineering and made the memristor and related devices a topic of active research (cf. [18, 19, 33, 34, 48, 53, 60, 61, 63] and references therein), which has been further motivated by the announcement of HP that commercial memory chips based on the memristor will be released in 2013 [1]. Including memristors in the study of analytical and numerical features of nonlinear circuits seems therefore to be important from both a theoretical and a practical perspective. Note that the index characterization here obtained will be of particular interest in the design of nonlinear oscillators and chaotic circuits including active memristors (cf. [5, 33, 50]).

Our analysis will make a systematic use of the notion of a *normal tree*. The origin of this concept can be found in Bryant's work on the state formulation problem [10] and has been revisited since then in connection to different aspects of circuit analysis [36, 58, 62, 67]. Although the original notion of a normal tree is oriented to circuits with three types of devices (capacitors, resistors and inductors), the concept can be naturally extended to digraphs with an arbitrary number of branches' types.

We will explore several basic features of normal trees in Section 2, which also includes some background material on digraph matrices. Section 3 presents a detailed derivation of the hybrid equations, whereas the index analysis for hybrid models of classical circuits (namely, circuits without memristors) is carried out in Section 4. The results are extended to circuits with memristors in Section 5. Section 6 discusses several examples, including a memristor oscillator, and suggests how our approach can be extended to problems with controlled sources, enlarging the scope to transistor-based circuits. Finally, concluding remarks are compiled in Section 7.

2 Digraph matrices and normal trees

For the sake of readability in the derivation of the hybrid model in Section 3 and in the index analyses of Sections 4 and 5, we compile here the definition and some properties of the loop and cutset matrices of a given digraph, including the so-called fundamental ones constructed from a given tree or forest, together with some elementary remarks about normal trees. The reader is referred to [6, 20, 25, 43] for further details.

2.1 Loop and cutset matrices

Consider a directed graph $\mathcal{G}$ with m branches, n nodes and k connected components. Chosen an orientation in every loop, the *loop matrix* $\tilde{B}$ is defined as (b_{ij}), where

$$b_{ij} = \begin{cases} 1 & \text{if branch } j \text{ is in loop } i \text{ with the same orientation} \\ -1 & \text{if branch } j \text{ is in loop } i \text{ with the opposite orientation} \\ 0 & \text{if branch } j \text{ is not in loop } i. \end{cases}$$

The rank of this matrix can be shown to equal $m - n + k$. A *reduced loop matrix* B is any $((m - n + k) \times m)$-submatrix of $\tilde{B}$ with full row rank. With terminological abuse, we will often refer to B simply as the *loop matrix*.

A set of branches in a given digraph is a *cutset* if its removal increases the number of connected components of the digraph, and it is minimal with respect to this property, that is, the removal of any proper subset does not change the number of components. The removal of a cutset can be shown to split a connected component in two, and the orientation of the cutset is defined by directing it from one of these components towards the other. The cutset matrix $\tilde{Q} = (q_{ij})$ is then defined by

$$q_{ij} = \begin{cases} 1 & \text{if branch } j \text{ is in cutset } i \text{ with the same orientation} \\ -1 & \text{if branch } j \text{ is in cutset } i \text{ with the opposite orientation} \\ 0 & \text{if branch } j \text{ is not in cutset } i. \end{cases}$$

The rank of $\tilde{Q}$ can be proved to be $n - k$, and any set of $n - k$ linearly independent rows of $\tilde{Q}$ defines a *reduced cutset matrix* $Q \in \mathbb{R}^{(n-k)\times m}$.

2.2 Fundamental matrices

In a connected digraph, the choice of a spanning tree confers the loop and cutset matrices introduced above a special structure. This is a consequence of a widely-used property in circuit theory, according to which every cotree branch (or link) defines a unique loop together with some tree branches (twigs), and every twig defines a unique cutset together with some links. This way, the so-called *fundamental* matrices take the form

$$B = (K \quad I), \quad Q = (I \quad -K^T). \tag{1}$$

The appearance of the same submatrix K in both B and Q (reading as $-K^T$ within the latter) follows from Tellegen's identity $BQ^T = 0$, which expresses the orthogonality of the so-called *cycle* and *cut* spaces. The same form holds for this matrices in non-connected digraphs once a (spanning) *forest* has been chosen. A spanning forest is defined by the choice of a minimal set of trees spanning every connected component of the digraph. Note that throughout the paper trees (in connected digraphs) and forests (in general) will be often understood to be spanning ones (that is, to include all nodes) without explicit mention.

Lemma 1. *Consider the pair of fundamental matrices depicted in (1). A full-row submatrix of Q (resp. of B) is non-singular if and only if its columns correspond to the branches of a forest (resp. a coforest). In this case, the determinants of these submatrices equal ± 1.*

We will also make use of Kirchhoff's matrix tree theorem, stated in Lemma 2 below for the products QQ^T and BB^T (provided that Q and B are fundamental matrices). This result can be easily derived from Lemma 1 and the Cauchy-Binet formula [32].

Lemma 2. *Let B, Q stand for fundamental loop and cutset matrices of a digraph $\mathcal{G}$. Then the determinants $\det BB^T$ and $\det QQ^T$ equal the total number of forests in $\mathcal{G}$.*

2.3 Normal trees

In our analysis we will address problems in which the branches of $\mathcal{G}$ are divided into p disjoint classes or *types*. We will number these types from 1 to p. When applied to circuit analysis, these types will correspond to branches with a different electrical nature. This taxonomy of branches makes it possible to define a special class of spanning trees, namely, the so-called *normal trees*, whose origin can be found in Bryant's work [10].

Given a digraph with p different types of branches, a normal tree is a spanning tree which verifies the following: it includes as many branches of type 1 as possible; among the ones satisfying the previous condition, it includes as many branches of type 2 as possible; among these, it includes as many branches of type 3 as possible, and so on, up to type p.

By construction, the fundamental loop defined in a normal tree by a link of type i includes only branches of types $j \leq i$ and, similarly, the cutset defined by a twig of type i is formed by branches of type $j \geq i$: the proof of this claim can be traced back at least to [9]. Within the corresponding loop and cutset matrices (1), this confers the block K the structure

$$\begin{pmatrix} K_{11} & 0 & 0 & \dots & 0 & 0 \\ K_{21} & K_{22} & 0 & \dots & 0 & 0 \\ K_{31} & K_{32} & K_{33} & \dots & 0 & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\ K_{(p-1)1} & K_{(p-1)2} & K_{(p-1)3} & \dots & K_{(p-1)(p-1)} & 0 \\ K_{p1} & K_{p2} & K_{p3} & \dots & K_{p(p-1)} & K_{pp} \end{pmatrix}. \tag{2}$$

3 Hybrid analysis

For the sake of simplicity, for the moment we will focus the discussion on possibly nonlinear circuits including only uncoupled, one-port (two-terminal) capacitors, voltage- and current-controlled resistors, and inductors. Independent sources can be included in a straightforward manner (cf. subsection 4.6). With more technical difficulties, some controlled sources may also be included in the analysis, along the lines of [36]. Memristors will be considered in Section 5. Without loss of generality we will assume that the circuit is connected.

Hybrid circuit models, as formulated in [35, 36, 67], are based on the choice of a so-called *normal reference tree*. In our setting, such a tree is just a normal tree in a digraph with four types of branches, in which the hierarchy is defined by choosing capacitors as type 1 devices (devices with the highest priority, that is, to be included as twigs as far as possible), then voltage-controlled resistors (type 2), current-controlled resistors (type 3), and finally inductors (type 4, with the lowest priority). Find in subsection 5.2 an extension of this notion

to circuits with memristors. This hierarchy implies that the fundamental loop defined by a link capacitor will only include other capacitors, and the one defined by a link voltage-controlled resistor will only have capacitors and/or voltage-controlled resistors; analogously, the fundamental cutset defined by an inductor will just include other inductors, and the one defined by a twig current-controlled resistor will only be formed by inductors and current-controlled resistors. These properties are the key to the formulation of the hybrid model, which will be expressed in terms of the voltages of twig capacitors and voltage-controlled resistors and the currents of link inductors and current-controlled resistors.

We will derive such models as a reduction of the system

$$\begin{aligned} C(v_c)v_c' &= i_c && \text{(3a)}\\ L(i_l)i_l' &= v_l && \text{(3b)}\\ 0 &= i_g - h(v_g) && \text{(3c)}\\ 0 &= v_r - f(i_r) && \text{(3d)}\\ 0 &= Bv && \text{(3e)}\\ 0 &= Qi, && \text{(3f)} \end{aligned}$$

where we express Kirchhoff laws using the loop and cutset matrices B, Q introduced in Section 2. The subscripts c, g, r and l correspond to capacitors, voltage-controlled resistors, current-controlled resistors and inductors, respectively. Capacitors (resp. inductors) are said to be uncoupled when C (resp. L) is diagonal and the i-th diagonal entry depends only on the voltage (resp. the current) of the i-th capacitor (resp. inductor). The maps h and f are C^1 and describe the characteristics of voltage-controlled and current-controlled resistors, respectively; we will denote by $G(v_g) = h'(v_g)$ and $R(i_r) = f'(i_r)$ the incremental conductance and resistance matrices (we will often omit the label "incremental" for these and for the capacitance and inductance matrices $C(v_c)$, $L(i_l)$ without explicit mention). Voltage-controlled (resp. current-controlled) resistors are uncoupled when the i-th component of h (resp. f) only depends on the voltage (resp. the current) of the i-th voltage-controlled (resp. current-controlled) resistor.

By using the normal tree referred to above, (3e) and (3f) read as

$$\begin{pmatrix} v_{c_{co}} \\ v_{g_{co}} \\ v_{r_{co}} \\ v_{l_{co}} \end{pmatrix} = - \begin{pmatrix} K_{11} & 0 & 0 & 0 \\ K_{21} & K_{22} & 0 & 0 \\ K_{31} & K_{32} & K_{33} & 0 \\ K_{41} & K_{42} & K_{43} & K_{44} \end{pmatrix} \begin{pmatrix} v_{c_{tr}} \\ v_{g_{tr}} \\ v_{r_{tr}} \\ v_{l_{tr}} \end{pmatrix}$$

and

$$\begin{pmatrix} i_{c_{tr}} \\ i_{g_{tr}} \\ i_{r_{tr}} \\ i_{l_{tr}} \end{pmatrix} = \begin{pmatrix} K_{11}^T & K_{21}^T & K_{31}^T & K_{41}^T \\ 0 & K_{22}^T & K_{32}^T & K_{42}^T \\ 0 & 0 & K_{33}^T & K_{43}^T \\ 0 & 0 & 0 & K_{44}^T \end{pmatrix} \begin{pmatrix} i_{c_{co}} \\ i_{g_{co}} \\ i_{r_{co}} \\ i_{l_{co}} \end{pmatrix},$$

respectively; the subscripts $_{tr}$ and $_{co}$ specify tree and cotree elements. For later use, these relations can be explicitly written as

$$\begin{aligned} v_{c_{co}} &= -K_{11}v_{c_{tr}} && \text{(4a)}\\ v_{g_{co}} &= -K_{21}v_{c_{tr}} - K_{22}v_{g_{tr}} && \text{(4b)}\\ v_{r_{co}} &= -K_{31}v_{c_{tr}} - K_{32}v_{g_{tr}} - K_{33}v_{r_{tr}} && \text{(4c)}\\ v_{l_{co}} &= -K_{41}v_{c_{tr}} - K_{42}v_{g_{tr}} - K_{43}v_{r_{tr}} - K_{44}v_{l_{tr}} && \text{(4d)} \end{aligned}$$

and

$$\begin{aligned} i_{c_{tr}} &= K_{11}^T i_{c_{co}} + K_{21}^T i_{g_{co}} + K_{31}^T i_{r_{co}} + K_{41}^T i_{l_{co}} && \text{(5a)}\\ i_{g_{tr}} &= K_{22}^T i_{g_{co}} + K_{32}^T i_{r_{co}} + K_{42}^T i_{l_{co}} && \text{(5b)}\\ i_{r_{tr}} &= K_{33}^T i_{r_{co}} + K_{43}^T i_{l_{co}} && \text{(5c)}\\ i_{l_{tr}} &= K_{44}^T i_{l_{co}}. && \text{(5d)} \end{aligned}$$

The steps which make it possible to derive the hybrid model, that is, to express the circuit equations just in terms of $v_{c_{tr}}$, $v_{g_{tr}}$, $i_{r_{co}}$ and $i_{l_{co}}$, are the following.

1. Recast (5a) by means of (3a) and (3c) as

$$C_{tr}(v_{c_{tr}})v'_{c_{tr}} = K_{11}^T C_{co}(v_{c_{co}})v'_{c_{co}} + K_{21}^T h_{co}(v_{g_{co}}) + K_{31}^T i_{r_{co}} + K_{41}^T i_{l_{co}}$$

and further, using (4a) and (4b), as

$$(C_{tr}(v_{c_{tr}}) + K_{11}^T C_{co}(-K_{11}v_{c_{tr}})K_{11})v'_{c_{tr}} = K_{21}^T h_{co}(-K_{21}v_{c_{tr}} - K_{22}v_{g_{tr}}) + K_{31}^T i_{r_{co}} + K_{41}^T i_{l_{co}}. \quad (6)$$

2. Analogously, (4d) can be rewritten, using (3b) and (3d), as

$$L_{co}(i_{l_{co}})i'_{l_{co}} = -K_{41}v_{c_{tr}} - K_{42}v_{g_{tr}} - K_{43}f_{tr}(i_{r_{tr}}) - K_{44}L_{tr}(i_{l_{tr}})i'_{l_{tr}}$$

which, via (5c) and (5d), reads as

$$(L_{co}(i_{l_{co}}) + K_{44}L_{tr}(K_{44}^T i_{l_{co}})K_{44}^T)i'_{l_{co}} = -K_{41}v_{c_{tr}} - K_{42}v_{g_{tr}} - K_{43}f_{tr}(K_{33}^T i_{r_{co}} + K_{43}^T i_{l_{co}}). \quad (7)$$

At this point, it is worth emphasizing that the elimination of $v_{c_{co}}$ and $i_{l_{tr}}$ carried out in steps 1 and 2 above is a key feature in the formulation of hybrid models. The elimination of these variables will prevent the index of these models from exceeding one.

3. In turn, (5b) leads, via (3c), to

$$h_{tr}(v_{g_{tr}}) = K_{22}^T h_{co}(v_{g_{co}}) + K_{32}^T i_{r_{co}} + K_{42}^T i_{l_{co}}$$

and, using (4b), to

$$h_{tr}(v_{g_{tr}}) = K_{22}^T h_{co}(-K_{21}v_{c_{tr}} - K_{22}v_{g_{tr}}) + K_{32}^T i_{r_{co}} + K_{42}^T i_{l_{co}}. \quad (8)$$

4. Finally, we will rewrite (4c) by means of (3d) as

$$f_{co}(i_{r_{co}}) = -K_{31}v_{c_{tr}} - K_{32}v_{g_{tr}} - K_{33}f_{tr}(i_{r_{tr}})$$

and in turn, via (5c), as

$$f_{co}(i_{r_{co}}) = -K_{31}v_{c_{tr}} - K_{32}v_{g_{tr}} - K_{33}f_{tr}(K_{33}^T i_{r_{co}} + K_{43}^T i_{l_{co}}). \tag{9}$$

Altogether, (6), (7), (8) and (9) yield the hybrid model

$$\begin{aligned}
(C_{tr}(v_{c_{tr}}) + K_{11}^T C_{co}(-K_{11}v_{c_{tr}})K_{11})v'_{c_{tr}} &= K_{21}^T h_{co}(-K_{21}v_{c_{tr}} - K_{22}v_{g_{tr}}) + K_{31}^T i_{r_{co}} + K_{41}^T i_{l_{co}} && \text{(10a)}\\
(L_{co}(i_{l_{co}}) + K_{44}L_{tr}(K_{44}^T i_{l_{co}})K_{44}^T)i'_{l_{co}} &= -K_{41}v_{c_{tr}} - K_{42}v_{g_{tr}} - K_{43}f_{tr}(K_{33}^T i_{r_{co}} + K_{43}^T i_{l_{co}}) && \text{(10b)}\\
h_{tr}(v_{g_{tr}}) &= K_{22}^T h_{co}(-K_{21}v_{c_{tr}} - K_{22}v_{g_{tr}}) + K_{32}^T i_{r_{co}} + K_{42}^T i_{l_{co}} && \text{(10c)}\\
f_{co}(i_{r_{co}}) &= -K_{31}v_{c_{tr}} - K_{32}v_{g_{tr}} - K_{33}f_{tr}(K_{33}^T i_{r_{co}} + K_{43}^T i_{l_{co}}). && \text{(10d)}
\end{aligned}$$

This is a differential-algebraic equation (DAE; cf. [8, 29, 40, 39, 54, 59]) of the form

$$\begin{aligned}
M(x)x' &= F_1(x,y) && \text{(11a)}\\
0 &= F_2(x,y), && \text{(11b)}
\end{aligned}$$

where $x = (v_{c_{tr}}, i_{l_{co}})$, $y = (v_{g_{tr}}, i_{r_{co}})$, and

$$M = \begin{pmatrix} C_{tr}(v_{c_{tr}}) + K_{11}^T C_{co}(-K_{11}v_{c_{tr}})K_{11} & 0 \\ 0 & L_{co}(i_{l_{co}}) + K_{44}L_{tr}(K_{44}^T i_{l_{co}})K_{44}^T \end{pmatrix},$$

whereas F_1 captures the right-hand side of (10a) and (10b), and F_2 comprises the algebraic restrictions defined by (10c) and (10d). The index of this DAE is addressed in Section 4 below.

4 Index characterization of hybrid models of non-passive circuits

For the reasons detailed in the Introduction it is important to characterize the index of differential-algebraic models of electrical and electronic circuits. In this Section we address the index of the hybrid model (10) without passivity restrictions, extending the results of [35, 36, 67], which only hold for passive problems. We will provide a description of the different index conditions in terms of the digraph topology and, specifically, in terms of the forests of certain digraph minors; these conditions will turn out to be independent of the normal tree chosen in the formulation of the hybrid model. Our index analysis will also be the key for the characterization of the set of non-degenerate points (cf. subsection 6.2).

Our results extend the approach introduced in [22] for nodal models (previous results regarding nodal analysis of passive circuits were obtained in [23, 68]); note that this extension is highly non-trivial for several reasons. Indeed, in the present framework we accommodate

both voltage-controlled and current-controlled resistors (in contrast to [22], which only handles voltage-controlled resistors) and also topologically degenerate configurations (VC-loops and IL-cutsets, which are precluded in [22]). Additionally, from a mathematical point of view, the form of the matrices J and J_1 arising in the proof of Theorem 2 below, as well as the (say) non-symmetric form of the factorization DEF of J_1, makes the analysis substantially more difficult than the one in [22]. These difficulties may be understood as a result of the use of the matrices B and Q (vs. the incidence matrix A in nodal models), which on the other hand make it possible to characterize models with degenerate configurations, beyond the scope of [22].

It is also worth indicating that Example 3 in Section 6 suggests that our index characterization can be extended to problems with controlled sources and multiports; this way, the scope of our framework potentially includes circuits with transistors, amplifiers, etc. A general analysis in this context is in the scope of future research.

4.1 The index of a DAE

Different index notions have arisen in DAE theory in the last decades. These include the differentiation, geometric, perturbation, strangeness and tractability indices; cf. [8, 29, 40, 39, 54, 59]. All these concepts generalize the notion of the *nilpotency index* of a matrix pencil, and support different approaches to the analysis and the numerical simulation of DAEs. Moreover, at least for so-called quasilinear DAEs (which include those of the form (11) as a particular case), these notions are invariant with respect to contact equivalence (cf. Theorem 3.3 in [59]). This implies that a diffeomorphic change of coordinates does not affect the index and, in this sense, makes this notion independent of the problem description.

In the settings which arise in this paper (index zero and index one systems of the form (11)), the different index notions amount to the same conditions. For the sake of completeness, we will present below the main ideas supporting the differentiation index concept [8], which is possibly the most widely used in DAE theory. Note also that in the index zero and index one cases considered in this paper, there is no explicit dependence of the solutions on the derivatives of the input (in non-autonomous problems), contrary to what happens in higher index problems.

The DAE (11) is said to be index zero if neither the algebraic variables y nor the explicit restrictions (11b) are present, and the matrix $M(x)$ in (11a) is non-singular. In this context, the problem can be obviously recast as the explicit ODE $x' = (M(x))^{-1}F_1(x)$. Provided that there is an explicit restriction (11b) and that $M(x)$ in (11a) is non-singular, the DAE (11) is said to be index one if the matrix of partial derivatives $F_{2y}(x, y)$ is invertible. This can be understood in a global sense, or locally around a given (x^*, y^*) satisfying (11b). Differentiation of (11b) readily gives an *underlying ODE*

$$x' = (M(x))^{-1}F_1(x, y) \tag{12a}$$
$$y' = -(F_{2y})^{-1}(x, y)F_{2x}(x, y)(M(x))^{-1}F_1(x, y), \tag{12b}$$

for which $F_2 = 0$ is an invariant comprising the solutions of the DAE. The fact that one

differentiation step is enough to reach an underlying explicit ODE explains the meaning of the "differentiation index one" expression.

4.2 A graph-theoretic property involving normal trees

Consider a digraph $\mathcal{G}$ with p different types of branches. For $i = 1, \ldots, p$ we will denote by $\mathcal{G}_i$ the digraph minor obtained after short-circuiting (contracting) all branches of types $j < i$ and open-circuiting (removing) all branches of types $j > i$.

Proposition 1. *With the notation of (2),* $(K_{ii} \;\; I)$ *and* $(I \;\; -K_{ii}^T)$ *are reduced loop/cutset matrices of the minor* $\mathcal{G}_i$*.*

Proof. Let us first note that open-circuiting branches of types $j > i$ does not affect the fundamental loops defined by the links of type i, since they involve branches of types $j \leq i$. Additionally, short-circuiting branches of types $j < i$ transforms the fundamental loops defined by the links of type i into loops of the minor $\mathcal{G}_i$. This means that all the rows of $(K_{ii} \;\; I)$ correspond to (linearly independent) loops of $\mathcal{G}_i$.

Analogously, short-circuiting branches of types $j < i$ is irrelevant with respect to the cutsets defined by the twigs of type i, because these cutsets only include branches of types $j \geq i$. And, in turn, open-circuiting branches of types $j > i$ transforms the original cutsets defined by twigs of type i into cutsets of $\mathcal{G}_i$. Therefore, all the rows of $(I \;\; -K_{ii}^T)$ describe (linearly independent) cutsets of $\mathcal{G}_i$.

Altogether, the number of loops and cutsets specified by the rows of $(K_{ii} \;\; I)$ and $(I \;\; -K_{ii}^T)$, respectively, equals the total number of branches of $\mathcal{G}_i$. Hence, the ranks of the loop and cutset matrices of $\mathcal{G}_i$ cannot exceed those of $(K_{ii} \;\; I)$ and $(I \;\; -K_{ii}^T)$. This shows that these are actually reduced loop and cutset matrices of $\mathcal{G}_i$ and the proof is complete. □

4.3 On the resistor-acyclic condition

According to the discussion in subsection 4.1, for the hybrid model (10) to be index zero (that is, for it to amount to an explicit ODE without the need for any differentiations), an obvious requirement is the absence of the algebraic restrictions (10c)-(10d). According to the derivation of the model presented above, this will happen if all voltage-controlled resistors are located in the cotree and every current-controlled one is in the tree. Recall that the construction of the hybrid model is based on choosing a tree with as many twig voltage-controlled resistors as possible (having previously maximized the number of twig capacitors) and as many link current-controlled resistors as possible (after having maximized the number of link inductors). This means that the algebraic restrictions are absent if and only if there is no chance to have voltage-controlled resistors in the tree or current-controlled ones in the cotree.

The situation described above is characterized in [36, 67] by means of the so-called *resistor-acyclic condition*, according to which every voltage-controlled resistor defines a loop together with some capacitors, and every current-controlled resistor defines a cutset together with some inductors. The equivalence between this condition and the requirement explained

above is due to the fact that capacitors and inductors have a higher priority than resistors as twig and links, respectively: the resistor-acyclic condition precludes choosing voltage-controlled resistors as twigs and current-controlled resistors as links.

We present in Proposition 2 below an alternative formulation of this condition. Within this statement, by a GRL-cutset we mean a cutset defined by voltage-controlled resistors and/or current-controlled ones and/or inductors (GR-, GL-, RL-, G-, R- and L-cutsets being particular instances; with the same criterion, R- and L-cutsets are particular instances of an RL-cutset, etc.). Analogously, a CGR-loop is a loop defined by capacitors and/or voltage-controlled resistors and/or current-controlled ones.

Proposition 2. *A circuit composed of capacitors, voltage- and current-controlled resistors and inductors satisfies the resistor-acyclic condition if and only if the circuit displays neither GRL-cutsets (except for RL-cutsets) nor CGR-loops (except for CG-loops).*

Proof. The claim is based on the colored branch theorem [69] (which is actually a corollary of a more general result proved by Minty: cf. Theorem 3.1 in [49]), according to which, in a three-color graph with just one blue branch, this branch either forms a loop exclusively with green branches or a cutset exclusively with red branches, but not both.

According to this result, the requirement that every voltage-controlled resistor defines a loop together with some capacitors is equivalent to the absence of cutsets defined by (one or more) voltage-controlled resistors together with (possibly) some current-controlled ones and (possibly) some inductors; indeed, fix a voltage-controlled resistor and paint it in blue, paint the capacitors in green and the remaining voltage-controlled resistors as well as the current-controlled ones and the inductors in red; this voltage-controlled resistor cannot enter any GRL-cutset, and this reasoning applies to each voltage-controlled resistor. Analogously every current-controlled resistor defining a cutset jointly with some inductors precludes the existence of loops defined by (one or more) current-controlled resistors together with (possibly) some capacitors and (possibly) some voltage-controlled resistors. □

4.4 Index zero conditions

The remarks in subsection 4.3 make the analysis of index zero models (under the resistor-acyclic condition) amount to the study of the non-singularity of the leading matrix

$$M = \begin{pmatrix} M_1 & 0 \\ 0 & M_2 \end{pmatrix} = \begin{pmatrix} C_{tr}(v_{c_{tr}}) + K_{11}^T C_{co}(-K_{11} v_{c_{tr}}) K_{11} & 0 \\ 0 & L_{co}(i_{l_{co}}) + K_{44} L_{tr}(K_{44}^T i_{l_{co}}) K_{44}^T \end{pmatrix}.$$

In the absence of reactive coupling (cf. the Remark at the end of this subsection), the non-singularity of M_1 and M_2 can be addressed in a non-passive context using the digraph minors $\mathcal{G}_i$ arising in Proposition 1. Specifically, $\mathcal{G}_c$ will be the minor obtained after open-circuiting all elements except for capacitors, and $\mathcal{G}_l$ will stand for the minor resulting from short-circuiting all devices except for inductors. These two minors will be the key objects arising in Theorem 1 below. Additionally, in the proof of this result we will denote by τ_1 and τ_4 the number of tree capacitors and cotree inductors in a normal tree (recall that the original circuit is assumed to be connected).

Theorem 1. *Assume that a given circuit does not display capacitive or inductive coupling. Then the hybrid model (10) is index zero if and only if the following requirements hold.*

- *The resistor-acyclic condition is met.*
- *The sum of capacitance products in the forests of $\mathcal{G}_c$ does not vanish.*
- *The sum of inductance products in the coforests of $\mathcal{G}_l$ does not vanish.*

Proof. The need for the resistor-acyclic condition is clear from the remarks discussed in subsection 4.3 (cf. [36, 67]).

The matrix M_1 arising above can be factorized as

$$M_1 = \begin{pmatrix} I & -K_{11}^T \end{pmatrix} \begin{pmatrix} C_{tr} & 0 \\ 0 & C_{co} \end{pmatrix} \begin{pmatrix} I \\ -K_{11} \end{pmatrix}.$$

Denote

$$D = \begin{pmatrix} I & -K_{11}^T \end{pmatrix}, \; E = \begin{pmatrix} C_{tr} & 0 \\ 0 & C_{co} \end{pmatrix}, \; F = \begin{pmatrix} I \\ -K_{11} \end{pmatrix}.$$

According to Proposition 1, D is a cutset matrix for the minor $\mathcal{G}_c$ defined above. By means of the Cauchy-Binet formula [32] we may write

$$\det M_1 = \sum_{\alpha,\beta} \det D^{\omega,\alpha} \det E^{\alpha,\beta} \det F^{\beta,\omega},$$

where the notation $D^{\omega,\alpha}$, $E^{\alpha,\beta}$, $F^{\beta,\omega}$ is used to mean certain submatrices of D, E, F: specifically, α and β are index sets which select τ_1 columns and rows of D and F, respectively; $\omega = \{1, \ldots, \tau_1\}$ specifies *all* rows/columns of these matrices, and $E^{\alpha,\beta}$ is the submatrix of E defined by the rows indexed by α and the columns indexed by β.

Since E is diagonal (because of the absence of capacitive coupling effects), we have $\det E^{\alpha,\beta} \neq 0$ only if $\alpha = \beta$. We also have $D = F^T$, and then $\det D^{\omega,\alpha} = \det F^{\alpha,\omega}$. Additionally, $\det D^{\omega,\alpha}$ is known to be non-vanishing if and only if the set of indices α specifies a forest, and in this case $\det D^{\omega,\alpha} = \pm 1$ (cf. Lemma 1).

In light of these remarks, we get

$$\det M_1 = \sum_{\alpha \in \mathcal{T}_c} \det D^{\omega,\alpha} \det E^{\alpha,\alpha} \det F^{\alpha,\omega} = \sum_{\alpha \in \mathcal{T}_c} (\det D^{\omega,\alpha})^2 \prod_{i \in \alpha} C_i = \sum_{\alpha \in \mathcal{T}_c} \prod_{i \in \alpha} C_i, \tag{13}$$

where $\mathcal{T}_c$ stands for the family of index sets that specify a forest of $\mathcal{G}_c$, and C_i is the i-th capacitance. From (13) it is clear that M_1 is non-singular if and only if the sum of capacitance products in the forests of $\mathcal{G}_c$ does not vanish.

The dual case arises in the matrix

$$M_2 = \begin{pmatrix} K_{44} & I \end{pmatrix} \begin{pmatrix} L_{tr} & 0 \\ 0 & L_{co} \end{pmatrix} \begin{pmatrix} K_{44}^T \\ I \end{pmatrix}.$$

The factorization reads

$$D = \begin{pmatrix} K_{44} & I \end{pmatrix}, \; E = \begin{pmatrix} L_{tr} & 0 \\ 0 & L_{co} \end{pmatrix}, \; F = \begin{pmatrix} K_{44}^T \\ I \end{pmatrix},$$

and now $D = \begin{pmatrix} K_{44} & I \end{pmatrix}$ is a loop matrix for the minor $\mathcal{G}_l$ (cf. Proposition 1). Proceeding as above we may derive

$$\det M_2 = \sum_{\alpha} \det D^{\omega,\alpha} \det E^{\alpha,\alpha} \det F^{\alpha,\omega} = \sum_{\alpha} (\det D^{\omega,\alpha})^2 \prod_{i \in \alpha} L_i,$$

where α now stands for sets of τ_4 indices; L_i is the i-th inductance. Additionally, $\det D^{\omega,\alpha}$ does not vanish if and only if α specifies a coforest, and in this case $\det D^{\omega,\alpha} = \pm 1$ since D is a fundamental matrix (see Lemma 1). Hence

$$\det M_2 = \sum_{\alpha \in \mathcal{C}_l} \prod_{i \in \alpha} L_i,$$

where $\mathcal{C}_l$ denotes the family of indices specifying coforests of $\mathcal{G}_l$. Again, this makes it clear that M_2 is non-singular if and only if the sum of inductance products in the coforests of $\mathcal{G}_l$ does not vanish. This completes the proof of Theorem 1. □

Remark. In particular, if the capacitors and inductors are strictly locally passive, then the incremental capacitances and inductances are positive and the sums arising above are always positive (and hence non-zero). In this sense, Theorem 1 above is an extension of the results in [35, 36, 67] to the non-passive setting, holding for problems without reactive coupling.

4.5 Index one conditions

The discussion of index one conditions for the hybrid model (10) without passivity requirements will be based on the digraph minor $\mathcal{G}_r$, obtained after short-circuiting capacitors and open-circuiting inductors. We will assume the leading matrix of the hybrid equations to be non-singular via the conditions arising in Theorem 1.

Theorem 2. *Assume that a given uncoupled circuit does not meet the resistor-acyclic condition, and that the sums of capacitance and inductance products arising in Theorem 1 do not vanish.*

Then the hybrid model (10) is index one if and only if the sum of products of the conductances of voltage-controlled twig resistors and the resistances of current-controlled link resistors, extended over the forests of $\mathcal{G}_r$, does not vanish.

Proof. In this working setting, the index one condition relies on the non-singularity of the matrix of partial derivatives of the algebraic restrictions (10c) and (10d) with respect to the algebraic variables $v_{g_{tr}}$ and $i_{r_{co}}$. This matrix is

$$J = \begin{pmatrix} G_{tr} + K_{22}^T G_{co} K_{22} & -K_{32}^T \\ K_{32} & R_{co} + K_{33} R_{tr} K_{33}^T \end{pmatrix}. \tag{14}$$

The key idea to tackle the non-singularity of this matrix is to look at it as the Schur complement [32, 59] of the middle identity block in

$$J_1 = \begin{pmatrix} G_{tr} & 0 & -K_{22}^T G_{co} & -K_{32}^T \\ 0 & I & 0 & -K_{33}^T \\ K_{22} & 0 & I & 0 \\ K_{32} & K_{33} R_{tr} & 0 & R_{co} \end{pmatrix},$$

and to factorize J_1 as the product DEF with

$$D = \begin{pmatrix} I & 0 & -K_{22}^T & -K_{32}^T & 0 & 0 & 0 & 0 \\ 0 & I & 0 & -K_{33}^T & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & K_{22} & 0 & I & 0 \\ 0 & 0 & 0 & 0 & K_{32} & K_{33} & 0 & I \end{pmatrix},$$

$$E = \begin{pmatrix} G_{tr} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & I & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & G_{co} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & I & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & I & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & R_{tr} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & I & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & R_{co} \end{pmatrix}, \quad F = \begin{pmatrix} I & 0 & 0 & 0 \\ 0 & I & 0 & 0 \\ 0 & 0 & I & 0 \\ 0 & 0 & 0 & I \\ I & 0 & 0 & 0 \\ 0 & I & 0 & 0 \\ 0 & 0 & I & 0 \\ 0 & 0 & 0 & I \end{pmatrix}.$$

Note that the submatrices

$$D_1 = \begin{pmatrix} I & 0 & -K_{22}^T & -K_{32}^T \\ 0 & I & 0 & -K_{33}^T \end{pmatrix}, \quad D_2 = \begin{pmatrix} K_{22} & 0 & I & 0 \\ K_{32} & K_{33} & 0 & I \end{pmatrix}$$

of D are, by construction, reduced cutset and loop matrices of the minor $\mathcal{G}_r$.

The properties enumerated below, together with the diagonal form of E, will make it feasible to simplify the Cauchy-Binet expansion of the factorization $J_1 = DEF$.

1. Only sets of columns corresponding to forests (resp. coforests) of $\mathcal{G}_r$ yield non-vanishing determinants in the corresponding submatrices of D_1 (resp. of D_2).

2. Moreover, the structure of F is easily checked to imply that only when the forest arising from D_1 and the coforest associated with D_2 are complementary to each other, the corresponding determinant of $F^{\alpha,\omega}$ (cf. (15) below) does not vanish, since otherwise this submatrix would have (at least) two identical rows.

Items 1 and 2 above make it possible to write the Cauchy-Binet expansion as

$$\det J_1 = \sum_{\alpha \in \mathcal{T}_{gr}} \det D^{\omega,\alpha} \det E^{\alpha,\alpha} \det F^{\alpha,\omega}, \tag{15}$$

where $\mathcal{T}_{gr}$ is the family of sets of indices which can be written as $\alpha = \alpha_1 \cup \alpha_2$, the former corresponding to a forest of $\mathcal{G}_r$ and the latter specifying the associated coforest. Notice that each forest (resp. coforest) of $\mathcal{G}_r$ yields a non-singular submatrix of D_1 (resp. of D_2).

3. In the context defined by items 1 and 2 above, the identity

$$\det D^{\omega,\alpha} \det F^{\alpha,\omega} = 1 \tag{16}$$

holds, as detailed in what follows. Consider the product

$$H = DF = \begin{pmatrix} I & 0 & -K_{22}^T & -K_{32}^T \\ 0 & I & 0 & -K_{33}^T \\ K_{22} & 0 & I & 0 \\ K_{32} & K_{33} & 0 & I \end{pmatrix}$$

and denote, for notational simplicity,

$$\tilde{K} = \begin{pmatrix} K_{22} & 0 \\ K_{32} & K_{33} \end{pmatrix}.$$

By means of the identity

$$\begin{pmatrix} I & \tilde{K}^T \\ 0 & I \end{pmatrix} \begin{pmatrix} I & -\tilde{K}^T \\ \tilde{K} & I \end{pmatrix} = \begin{pmatrix} I + \tilde{K}^T\tilde{K} & 0 \\ \tilde{K} & I \end{pmatrix}$$

it is easy to check that $\det H = \det(I + \tilde{K}^T\tilde{K})$. The latter matrix equals the product $(I \quad -\tilde{K}^T)(I \quad -\tilde{K}^T)^T$ and, since $(I \quad -\tilde{K}^T)$ is a fundamental cutset matrix for the minor $\mathcal{G}_r$, according to Lemma 2 this determinant, and hence $\det H$, equals the total number of (spanning) forests in this minor.

On the other hand, reasoning as in item 2, the Cauchy-Binet formula applied to the product $H = DF$ yields

$$\det H = \sum_{\alpha \in \mathcal{T}_{gr}} \det D^{\omega,\alpha} \det F^{\alpha,\omega}, \tag{17}$$

with index sets $\alpha \in \mathcal{T}_{gr}$ as above. Both $\det D^{\omega,\alpha}$ and $\det F^{\alpha,\omega}$ are ± 1, and for the sum in (17) to equal the total number of forests, it must be $\det D^{\omega,\alpha} \det F^{\alpha,\omega} = 1$ for all the index sets α which make both determinants non-null. This way the identity (16) is proved.

Because of the properties 1, 2 and 3 above, the Cauchy-Binet expansion of $J_1 = DEF$ amounts to a sum of products of certain diagonal entries of E, namely, the ones signaled by α_1 from the first four blocks G_{tr}, I, G_{co}, I, together with those specified by α_2 from the last four blocks I, R_{tr}, I, R_{co}. Since α_1 and α_2 must correspond to a forest and its coforest, the non-vanishing terms in the sum are therefore defined by the products of the conductances of voltage-controlled resistors in forests of $\mathcal{G}_r$ and the resistances of current-controlled resistors in the corresponding coforests. The proof of Theorem 2 is then complete. □

Again, the index one results of [35, 36, 67] for passive circuits may be derived in uncoupled cases from Theorem 2 above, since strictly locally passive resistors have positive conductances and resistances and therefore all products arising in Theorem 2 are positive.

Note that points in the semistate space where some of the sum of products arising in Theorems 1 and 2 vanish lead to singularities of the model, possibly yielding impasse phenomena [15, 54, 59]; cf. subsections 6.2 and 6.3 in this regard. The detailed analysis of such singularities in terms of the electrical features of the circuit is an open problem.

4.6 Sources

Independent voltage and current sources can be added without difficulties in well-posed configurations (i.e. not including loops of voltage sources or cutsets of current sources). In this context, normal trees include all voltage sources and no current sources, the hierarchy of other devices remaining the same. The minor $\mathcal{G}_c$ must in this case be replaced by the one obtained after short-circuiting voltage sources and open-circuiting all other devices (except for capacitors), and analogously the minor $\mathcal{G}_l$ now results from short-circuiting all elements except for inductors and current sources, and open-circuiting current sources. Similarly, the minor $\mathcal{G}_r$ must now be constructed by short-circuiting voltage sources and capacitors, and open-circuiting current sources and inductors.

The resistor-acyclic condition must be restated as to require that every voltage-controlled resistor defines a loop together with some capacitors and/or voltage sources, and every current-controlled resistor defines a cutset together with some inductors and/or current sources. The statement in Proposition 2 must be reformulated as the absence of GRLI-cutsets (except for RLI-cutsets) and VCGR-loops (except for VCG-loops). The remaining conditions arising in the index analysis remain the same in problems with independent sources. Note that, in the formulation of the circuit equations, the derivatives of the excitation terms coming from voltage sources within VC-loops and current sources within IL-cutsets will appear explicitly in the model (cf. Section 6).

5 Circuits with memristors

5.1 The memristor

A *charge-controlled memristor* [14] is a nonlinear device governed by a flux-charge characteristic of the form

$$\varphi = \phi(q). \tag{18}$$

By means of the electromagnetic relations $\varphi'(t) = v(t)$, $q'(t) = i(t)$, from (18) we get the voltage-current characteristic

$$v = M(q)i$$

where

$$M(q) = \phi'(q)$$

is the so-called incremental *memristance*.

The device behaves as a resistor in which the resistance depends on $q(t) = \int_{-\infty}^{t} i(\tau)d\tau$, keeping track of the device history. For this reason Chua called this circuit element a *memory-resistor* or *memristor*. As indicated in Section 1, the memristor and related devices have been the object of much recent attention: see [1, 18, 19, 33, 34, 48, 53, 60, 61, 66] and references therein.

The dual case is defined by a *flux-controlled* memristor, which has a characteristic of the form

$$q = \sigma(\varphi),$$

with incremental *memductance*

$$W(\varphi) = \sigma'(\varphi).$$

A memristor is *strictly locally passive* if $M(q) > 0$ or $W(\varphi) > 0$ for all q or φ, respectively.

As in Section 4, our goal in the analysis carried out below is to get an index characterization holding without the need to require memristors (or other circuit elements) to be passive. This way, the results here obtained will be of interest in the analysis of nonlinear oscillators and chaotic circuits including active memristors [5, 33, 50].

5.2 Hybrid model

The derivation of the hybrid equations for memristive circuits parallelizes the one detailed in Section 3 for classical circuits (i.e. circuits without memristors), and therefore most details will be omitted. Again, in a first step we avoid including sources in order to simplify the notation, especially concerning the matrices arising below. We will use the subscripts m and w to refer to charge-controlled and flux-controlled memristors, respectively.

A normal tree will now be defined by a hierarchy of circuit elements in which capacitors (type 1 devices) are the ones preferred as twigs, and then voltage-controlled resistors and flux-controlled memristors (type 2), current-controlled resistors and charge-controlled memristors (type 3), and inductors (type 4). We will simplify a bit the form of the equations by priorizing (additionally) voltage-controlled resistors over flux-controlled memristors, and current-controlled resistors over charge-controlled memristors, although the analysis could also be performed without these distinctions. In this direction, reverting the priority between voltage-controlled resistors and flux-controlled memristors, and/or the one between current-controlled resistors and charge-controlled memristors, would lead to a model with similar complexity.

With the device hierarchy specified above, the matrix K takes the form

$$\begin{pmatrix} K_{11} & 0 & 0 & 0 & 0 & 0 \\ K_{21} & K_{22} & 0 & 0 & 0 & 0 \\ K_{31} & K_{32} & K_{33} & 0 & 0 & 0 \\ K_{41} & K_{42} & K_{43} & K_{44} & 0 & 0 \\ K_{51} & K_{52} & K_{53} & K_{54} & K_{55} & 0 \\ K_{61} & K_{62} & K_{63} & K_{64} & K_{65} & K_{66} \end{pmatrix}.$$

The hybrid model is defined by the differential equations for the reactive elements, which now can be checked to read as

$$\begin{aligned} [C_{tr}(v_{c_{tr}}) + K_{11}^T C_{co}(-K_{11}v_{c_{tr}})K_{11}]v'_{c_{tr}} &= K_{21}^T h_{co}(-K_{21}v_{c_{tr}} - K_{22}v_{g_{tr}}) + \\ &+ K_{31}^T W(\varphi_{w_{co}})(-K_{31}v_{c_{tr}} - K_{32}v_{g_{tr}} - K_{33}v_{w_{tr}}) + K_{41}^T i_{r_{co}} + K_{51}^T i_{m_{co}} + K_{61}^T i_{l_{co}} \end{aligned} \tag{19a}$$

$$\begin{aligned} [L_{co}(i_{l_{co}}) + K_{66}L_{tr}(K_{66}^T i_{l_{co}})K_{66}^T]i'_{l_{co}} &= -K_{61}v_{c_{tr}} - K_{62}v_{g_{tr}} - K_{63}v_{w_{tr}} - \\ &- K_{64}f_{tr}(K_{44}^T i_{r_{co}} + K_{54}^T i_{m_{co}} + K_{64}^T i_{l_{co}}) - K_{65}M_{tr}(q_{m_{tr}})(K_{55}^T i_{m_{co}} + K_{65}^T i_{l_{co}}) \end{aligned} \tag{19b}$$

and the ones for the memristive devices

$$\begin{aligned}
\varphi'_{w_{tr}} &= v_{w_{tr}} && \text{(20a)}\\
\varphi'_{w_{co}} &= -K_{31}v_{c_{tr}} - K_{32}v_{g_{tr}} - K_{33}v_{w_{tr}} && \text{(20b)}\\
q'_{m_{tr}} &= K_{55}^T i_{m_{co}} + K_{65}^T i_{l_{co}} && \text{(20c)}\\
q'_{m_{co}} &= i_{m_{co}}, && \text{(20d)}
\end{aligned}$$

together with the algebraic restrictions, which take the form

$$\begin{aligned}
&h_{tr}(v_{g_{tr}}) = K_{22}^T h_{co}(-K_{21}v_{c_{tr}} - K_{22}v_{g_{tr}}) + \\
&\quad + K_{32}^T W_{co}(\varphi_{w_{co}})(-K_{31}v_{c_{tr}} - K_{32}v_{g_{tr}} - K_{33}v_{w_{tr}}) + K_{42}^T i_{r_{co}} + K_{52}^T i_{m_{co}} + K_{62}^T i_{l_{co}} && \text{(21a)}\\
&[W_{tr}(\varphi_{w_{tr}}) + K_{33}^T W_{co}(\varphi_{w_{co}})K_{33}]v_{w_{tr}} = \\
&\qquad = K_{33}^T W_{co}(\varphi_{w_{co}})(-K_{31}v_{c_{tr}} - K_{32}v_{g_{tr}}) + K_{43}^T i_{r_{co}} + K_{53}^T i_{m_{co}} + K_{63}^T i_{l_{co}} && \text{(21b)}\\
&f_{co}(i_{r_{co}}) = -K_{41}v_{c_{tr}} - K_{42}v_{g_{tr}} - K_{43}v_{w_{tr}} - K_{44}f_{tr}(K_{44}^T i_{r_{co}} + K_{54}^T i_{m_{co}} + K_{64}^T i_{l_{co}}) && \text{(21c)}\\
&[M_{co}(q_{m_{co}}) + K_{55}M_{tr}(q_{m_{tr}})K_{55}^T]i_{m_{co}} = -K_{51}v_{c_{tr}} - K_{52}v_{g_{tr}} - K_{53}v_{w_{tr}} - \\
&\qquad - K_{54}f_{tr}(K_{44}^T i_{r_{co}} + K_{54}^T i_{m_{co}} + K_{64}^T i_{l_{co}}) - K_{55}M_{tr}(q_{m_{tr}})K_{65}^T i_{l_{co}}. && \text{(21d)}
\end{aligned}$$

The differential variables are defined by the vector $(v_{c_{tr}}, i_{l_{co}}, \varphi_{w_{tr}}, \varphi_{w_{co}}, q_{m_{tr}}, q_{m_{co}})$ and the algebraic ones by $(v_{g_{tr}}, v_{w_{tr}}, i_{r_{co}}, i_{m_{co}})$.

5.3 The index of memristive circuits

The (mem)resistor-acyclic condition. The resistor-acyclic condition must now be restated as follows: every voltage-controlled resistor, but also every flux-controlled memristor, defines a loop together with some capacitors, and every current-controlled resistor or charge-controlled memristor defines a cutset together with some inductors. This rules out choosing voltage-controlled resistors or flux-controlled memristors as twigs, and current-controlled resistors or charge-controlled memristors as links. This is a straightforward extension of the condition arising in the classical setting; we give it a different name only for the sake of terminological consistency. We leave it to the reader to formulate the analog of Proposition 2 in the memristive context.

The characterization of index zero problems follows exactly Theorem 1, now in terms of the (mem)resistor-acyclic condition and the digraph minors $\mathcal{G}_c$ (which is now defined by open-circuiting all resistors, memristors and inductors) and $\mathcal{G}_l$ (now being defined by short-circuiting all capacitors, resistors and memristors). The attention will be therefore focused on the index one context: we provide below a characterization of index one hybrid models in the memristive context, in terms of the digraph minor obtained after short-circuiting capacitors and open-circuiting inductors (to be denoted by $\mathcal{G}_{rm}$; note that this minor now includes resistors and memristors).

Theorem 3. *Assume that a given uncoupled circuit does not meet the (mem)resistor-acyclic condition and that the sums of capacitance and inductance products arising in Theorem 1 (now being computed over $\mathcal{G}_c$ and $\mathcal{G}_l$ as defined above) do not vanish.*

Then the hybrid model defined by the equations (19), (20) and (21) is index one if and only if the sum of products of the conductances of voltage-controlled twig resistors, the memductances of flux-controlled twig memristors, the memristances of charge-controlled link memristors and the resistances of current-controlled link resistors, extended over the forests of $\mathcal{G}_{rm}$, does not vanish.

Proof. Recall that the model defined by (19), (20) and (21) has $v_{c_{tr}}$, $i_{l_{co}}$, $\varphi_{w_{tr}}$, $\varphi_{w_{co}}$, $q_{m_{tr}}$ and $q_{m_{co}}$ as differential variables, and $v_{g_{tr}}$, $v_{w_{tr}}$, $i_{r_{co}}$ and $i_{m_{co}}$ as algebraic ones. The index one condition now relies on the non-singularity of the matrix of partial derivatives of the algebraic restrictions (21) with respect to $v_{g_{tr}}$, $v_{w_{tr}}$, $i_{r_{co}}$ and $i_{m_{co}}$, namely

$$\begin{pmatrix} G_{tr}+K_{22}^T G_{co} K_{22}+K_{32}^T W_{co} K_{32} & K_{32}^T W_{co} K_{33} & -K_{42}^T & -K_{52}^T \\ K_{33}^T W_{co} K_{32} & W_{tr}+K_{33}^T W_{co} K_{33} & -K_{43}^T & -K_{53}^T \\ K_{42} & K_{43} & R_{co}+K_{44} R_{tr} K_{44}^T & K_{44} R_{tr} K_{54}^T \\ K_{52} & K_{53} & K_{54} R_{tr} K_{44}^T & M_{co}+K_{55} M_{tr} K_{55}^T+K_{54} R_{tr} K_{54}^T \end{pmatrix}.$$

Let us denote

$$Y_{tr}=\begin{pmatrix} G_{tr} & 0 \\ 0 & W_{tr} \end{pmatrix},\ Y_{co}=\begin{pmatrix} G_{co} & 0 \\ 0 & W_{co} \end{pmatrix},\ Z_{tr}=\begin{pmatrix} R_{tr} & 0 \\ 0 & M_{tr} \end{pmatrix},\ Z_{co}=\begin{pmatrix} R_{co} & 0 \\ 0 & M_{co} \end{pmatrix},$$

and

$$\tilde{K}=\begin{pmatrix} K_{22} & 0 \\ K_{32} & K_{33} \end{pmatrix},\ \hat{K}=\begin{pmatrix} K_{42} & K_{43} \\ K_{52} & K_{53} \end{pmatrix},\ \bar{K}=\begin{pmatrix} K_{44} & 0 \\ K_{54} & K_{55} \end{pmatrix}.$$

Then the matrix above reads as

$$\begin{pmatrix} Y_{tr}+\tilde{K}^T Y_{co} \tilde{K} & -\hat{K}^T \\ \hat{K} & Z_{co}+\bar{K} R_{tr} \bar{K}^T \end{pmatrix}$$

and this shows that it has exactly the structure depicted in (14). Therefore the proof of Theorem 2 applies here by grouping together voltage-controlled resistors and flux-controlled memristors, on the one hand, and current-controlled resistors and charge-controlled memristors, on the other. □

Sources. Without the need for additional details, it should be clear that independent voltage and current sources can be included in the analysis as long as loops of voltage sources and cutsets of current sources are avoided. The capacitive minor is again obtained after short-circuiting voltage sources and open-circuiting all other devices (except for capacitors), and the inductive minor results from short-circuiting all elements except for inductors and current sources, and open-circuiting the latter. The definition of the resistive-memristive minor and the restatement of the (mem)resistor-acyclic condition also proceed as in the classical setting.

6 Examples

6.1 Example 1

We begin with a simple example aimed at illustrating the notions and ideas introduced above and, specially, at showing how to compute the index conditions in terms of the (co)forests

of the different digraph minors. The example is defined by the circuit depicted in Figure 1.

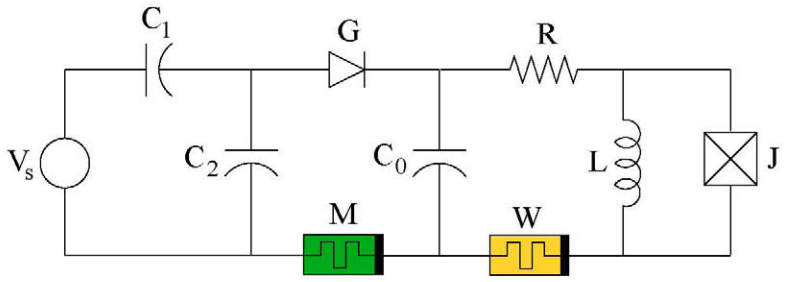

Figure 1: Memristive circuit.

The circuit includes a voltage source V_s, three linear capacitors (with capacitances C_0, C_1, C_2), a linear inductor with inductance L, a linear current-controlled resistor with resistance R, and four nonlinear devices: a diode (which will be treated as a nonlinear voltage-controlled resistor governed by a relation of the form $i_g = h(v_g)$, with incremental conductance $G = h'$), a charge-controlled memristor with memristance M, a flux-controlled memristor with memductance W, and a Josephson junction (labelled as J). The latter (cf. [17]) can be seen as a nonlinear inductor governed by a current-flux relation of the form $i_j = I_0 \sin(k_0 \varphi_J)$ for certain constants I_0, k_0; we will denote its incremental inductance by L_J. This inductance becomes negative at certain operating regions; the same may happen with the incremental conductance G of the diode if it displays tunneling effects. The non-passive setting considered in previous Sections is therefore of interest in the index analysis of hybrid models for this circuit. Note also that the VC-loop defined by the voltage source together with the capacitors C_1 and C_2 would confer the Modified Nodal Analysis (MNA) model for this circuit an index two structure [23, 68], at least under passivity requirements.

We will formulate the hybrid equations in terms of the normal tree depicted in Figure 2. It is worth remarking that the circuit only has another normal tree, obtained after replacing the capacitor C_1 by C_2. Certainly, the index conditions arising in the analysis will not depend on the choice of one or another.

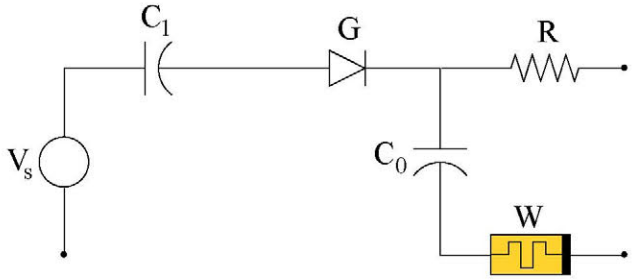

Figure 2: Normal tree.

With this choice, and letting v_0 and v_1 stand for the voltage drops in the capacitors C_0

and C_1, the hybrid equations can be checked to read as

$$\begin{aligned}
C_0 v_0' &= -i_m - i_l - i_J && \text{(22a)}\\
(C_1 + C_2) v_1' &= C_2 v_s'(t) - i_m && \text{(22b)}\\
L i_l' &= v_0 + v_w - R(i_l + i_J) && \text{(22c)}\\
L_J(i_J) i_J' &= v_0 + v_w - R(i_l + i_J) && \text{(22d)}\\
\varphi_w' &= v_w && \text{(22e)}\\
q_m' &= i_m && \text{(22f)}\\
0 &= h(v_g) + i_m && \text{(22g)}\\
0 &= i_l + i_J + W(\varphi_w) v_w && \text{(22h)}\\
0 &= M(q_m) i_m + v_s(t) - v_0 - v_1 - v_g. && \text{(22i)}
\end{aligned}$$

This system is formulated in terms of the twig capacitor voltages v_0, v_1, the link inductor currents i_l, i_J, the flux and the charge of flux-controlled and charge-controlled memristors, respectively (namely, φ_w and q_m), the voltage of voltage-controlled twig resistors and flux-controlled twig memristors (in this case, v_g and v_w) and the current of current-controlled link resistors and charge-controlled link memristors (which in this case amount to i_m).

In light of the model (22), it is easy to check that the leading matrix (cf. (22a)-(22f)) is non-singular if and only if

$$C_0 \neq 0 \neq C_1 + C_2, \; L \neq 0 \neq L_J, \tag{23}$$

and that the index one condition arising from (22g)-(22i) is

$$W(GM + 1) \neq 0. \tag{24}$$

Our goal is to show that the conditions (23)-(24) can be obtained in graph-theoretic terms, just by examining the (mem)resistor-acyclic condition and the trees of the digraphs $\mathcal{G}_c$, $\mathcal{G}_l$, $\mathcal{G}_{rm}$ introduced in Section 5. A simple check shows that the (mem)resistor-acyclic condition does not hold; actually, only R satisfies the requirement arising in this condition, because of the cutset defined by this resistor together with L and J.

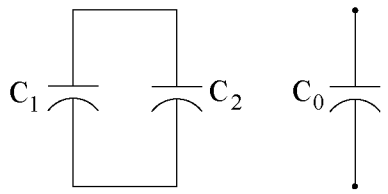

Figure 3: The $\mathcal{G}_c$ minor.

The minor $\mathcal{G}_c$ for this example is depicted in Figure 3. From this Figure it is obvious that $\mathcal{G}_c$ has two forests, defined by C_0, C_1 and by C_0, C_2, respectively. The corresponding

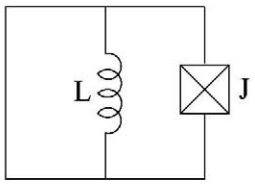

Figure 4: The $\mathcal{G}_l$ minor.

sum of products is therefore $C_0C_1 + C_0C_2 = C_0(C_1 + C_2)$, and this explains the conditions $C_0 \neq 0 \neq C_1 + C_2$ in (23).

Figure 4 displays the $\mathcal{G}_l$ minor. Now there is a unique forest (which is a singleton), and therefore a unique coforest comprising the inductor and the Josephson junction. The product of inductances in this unique coforest is LL_J and this is responsible for the non-vanishing requirement on both inductances in (23).

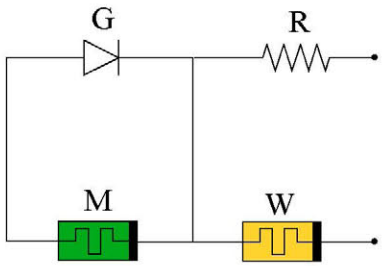

Figure 5: The $\mathcal{G}_{rm}$ minor.

Finally, the $\mathcal{G}_{rm}$ minor is displayed in Figure 5. This connected minor has two forests (trees), defined by G, R, W and by M, R, W. Now the products involve the conductances of voltage-controlled twig resistors, the memductances of flux-controlled twig memristors, the memristances of charge-controlled link memristors and the resistances of current-controlled link resistors; this means that the first tree yields the product GWM, whereas only W arises in the second. This leads to the requirement $W(GM + 1) \neq 0$ in (24).

Certainly, in this example the derivation of the model (22) and the computations leading to (23)-(24) are easy to perform by hand, but the scope of our results also includes in practice complex circuits in which such computations are not feasible; note additionally that the approach applies even without computing the model. This way, the framework here presented not only displays a theoretical interest but is also useful for practical purposes in actual circuit analysis, e.g. for monitoring index conditions in circuit simulation.

6.2 Non-degeneracy

It is important to understand the meaning of the conditions (23)-(24) within Example 1. These conditions restrict the values of the variables i_J, φ_w, v_g and q_m for which the model (22) is non-degenerate; singularities and impasse phenomena would arise at values of these

variables making the aforementioned conditions fail. Should C_0, C_1, C_2 and/or L be nonlinear, the same applies to the variables v_0, v_1 and/or i_l.

This can be addressed in greater generality, in terms of the DAE model (10). Denote $x = (v_{c_{tr}}, i_{l_{co}})$, $y = (v_{g_{tr}}, i_{r_{co}})$. A set of values for (x, y) is said to be *non-degenerate* if a unique solution of (10) emanates from it. From an analytical point of view, the importance of the index one notion relies on the fact that it characterizes the set of non-degenerate points. The non-degeneracy condition fails at so-called *singular points*, where impasse phenomena are displayed [15, 16]. Specifically, (x^*, y^*) is said to be a *forward impasse point* if there exists a $\delta > 0$ and two distinct solutions in $C^1((-\delta, 0), \Omega) \cap C^0((-\delta, 0], \Omega)$ with initial point $x(0) = x^*$, $y(0) = y^*$, whose derivatives blow up at $t = 0$. A *backward impasse point* is defined analogously, just requiring the solutions to be defined in $C^1((0, \delta), \Omega) \cap C^0([0, \delta), \Omega)$. Singularities may also arise in an index zero setting, and analogous remarks apply to the model defined by (19), (20) and (21) for circuits with memristors.

The non-degeneracy notion, together with that of an impasse point, will be illustrated by means of the memristor oscillator considered in Example 2 below.

6.3 Example 2

Consider the circuit displayed in Figure 6(a), defined by a series connection of a charge-controlled memristor with memristance $M(q_m)$, a linear inductor and a linear capacitor. Memristor oscillators of this type have been considered in [33].

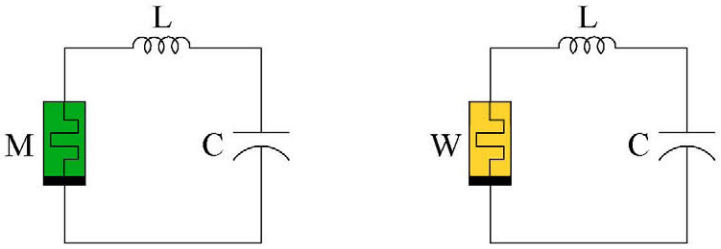

Figure 6: (a) MLC oscillator. (b) Replacing M by a flux-controlled memristor.

Because of the cutset defined by the charge-controlled memristor and the inductor, the (mem)resistor-acyclic condition holds. For non-vanishing C, L, and any value of M, the circuit is non-degenerate: this means that there is no restriction on the values of q_m, i_l and v_c for which a unique solution is well-defined. In particular, no concern arises at the values of q_m for which $M(q_m)$ may vanish.

However, qualitative changes may be displayed at points where $M(q_m)$ vanishes. Note that the circuit is governed by the hybrid equations

$$q_m' = i_l \tag{25a}$$

$$Li_l' = -M(q_m)i_l - v_c \tag{25b}$$

$$Cv_c' = i_l. \tag{25c}$$

In particular, it is worth noticing the invariant $q_m - Cv_c$; indeed, the identity $q_m' - Cv_c' = i_l - i_l = 0$ implies that $q_m - Cv_c$ remains constant along trajectories. We may then consider

$\mu = q_m - Cv_c$ a parameter and rewrite (25) just in terms of q_m and i_l. Fixing $L = C = 1$ for the sake of simplicity, we arrive at

$$\begin{aligned} q_m' &= i_l && \text{(26a)} \\ i_l' &= -M(q_m)i_l - q_m + \mu. && \text{(26b)} \end{aligned}$$

Equilibria of (26) are given by $i_l = 0$, $q_m = \mu$, and the eigenvalues of the linearization at equilibrium are easily checked to be

$$\lambda = \frac{-M(\mu) \pm \sqrt{M(\mu)^2 - 4}}{2}.$$

If μ undergoes a value where the memristance M vanishes, eventually becoming negative (this modelling a locally active device), the real part of the eigenvalues become positive and the equilibrium point experiences a stability change. In particular, when a *supercritical* Hopf bifurcation occurs [52], this stability loss conveys the birth of a nonlinear limit cycle, making the circuit oscillate. This is the case e.g. if we take $M(q_m) = q_m - q_m^3$: for small negative values of μ, the memristance $M(\mu)$ becomes negative and an attracting periodic trajectory shows up. In Figure 7 (q_m and i_l in abscissae and ordinates, respectively) we plot such periodic solutions for the parameter values $\mu = -0.1$ and $\mu = -0.5$; note that in both cases the periodic solution encircles the equilibrium located at $q_m = \mu$, $i_l = 0$.

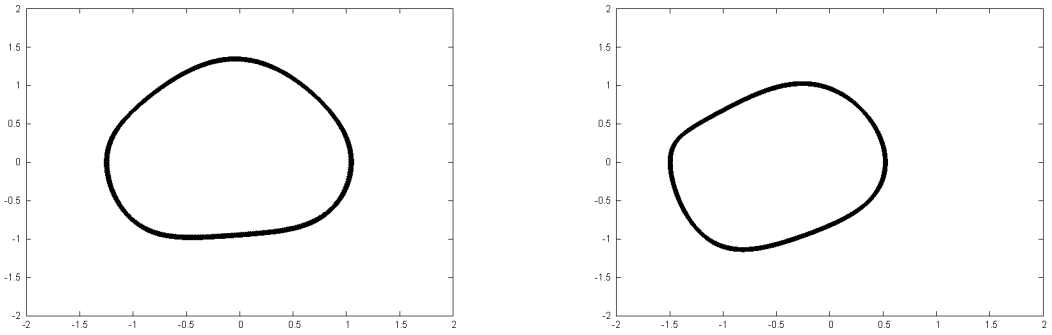

Figure 7: Nonlinear oscillations: (a) $\mu = -0.1$ (b) $\mu = -0.5$.

Things are different if the charge-controlled memristor is replaced by a flux-controlled one, as depicted in Figure 6(b). Now the (mem)resistor-acyclic condition does not hold and the hybrid equations do not amount to an explicit ODE such as (25). Instead, the model now reads as the semiexplicit DAE

$$\begin{aligned} \varphi_w' &= v_w && \text{(27a)} \\ Li_l' &= -v_c - v_w && \text{(27b)} \\ Cv_c' &= i_l && \text{(27c)} \\ 0 &= i_l - W(\varphi_w)v_w. && \text{(27d)} \end{aligned}$$

This DAE is easily seen to be index one if and only if $W(\varphi_w)$ does not vanish. Values of φ_w for which $W(\varphi_w) = 0$ are degenerate and lead to singularities. Computer simulations

actually show, with $W(\varphi_w) = \varphi_w$, that the hyperplane $\varphi_w = 0$ is composed of impasse points; in particular, a pair of trajectories collapse with infinite speed at forward impasse points located on the region $i_l < 0$.

Note, incidentally, that the $\mathcal{G}_{rm}$ minor amounts in this circuit to a single twig defined by the memristor and, in a flux-controlled setting, it must be $W \neq 0$ for the problem to be non-degenerate, according to Theorem 3. By contrast, Theorem 3 imposes no restriction on the value of M for the circuit in Figure 6(a) because in that case the memristor is a charge-controlled one. As detailed above, if $M = 0$ then the dynamics undergoes a Hopf bifurcation, but the circuit keeps on being non-degenerate (and, accordingly, no impasse phenomenon is displayed) even if M vanishes.

6.4 Example 3

The results of Sections 4 and 5 are based on the assumption that the circuit elements are uncoupled one-ports. In the presence of coupling effects, controlled sources and/or multiports the analysis is more cumbersome; some results based on so-called *balanced trees* were obtained for nodal models of topologically non-degenerate circuits with controlled sources in [62]. We discuss below an example involving a bipolar junction transistor, which is usually modelled as a three-terminal (or two-port) with controlled sources, in order to motivate further study aiming to extend the results based on balanced trees to our present context.

Consider the common-emitter amplifier shown in Figure 8, where the *pnp* transistor acts as an amplifier for an input voltage v_i, the circuit displaying also a parasitic input resistance R_i, a coupling capacitor C, a bias resistor R_b, a load resistor R_L and a DC source V_{cc}.

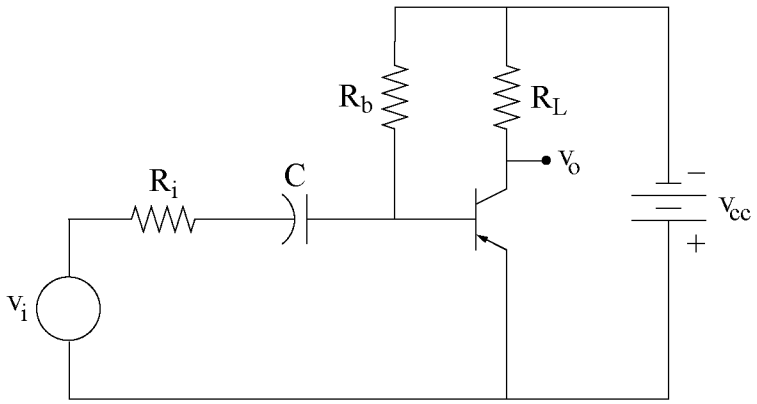

Figure 8: A *pnp* transistor amplifier.

In Figure 9 we replace the transistor by the well-known Ebers-Moll model, where

$$\begin{aligned} i_{EB} &= i_1 - \alpha_R i_2 = I_{ES}(e^{v_{EB}/v_T} - 1) - \alpha_R I_{CS}(e^{v_{CB}/v_T} - 1) \\ i_{CB} &= -\alpha_F i_1 + i_2 = -\alpha_F I_{ES}(e^{v_{EB}/v_T} - 1) + I_{CS}(e^{v_{CB}/v_T} - 1). \end{aligned}$$

Here I_{ES} and I_{CS} are the reverse saturation currents in the emitter and the collector diodes, α_F and α_R are the forward and reverse current transfer rations, and v_T is the thermal voltage.

Note that the current sources may also be understood to be nonlinear, voltage-controlled ones, the base-emitter and the base-collector sources being controlled by the collector-base and the emitter-base voltages, respectively; this point of view will be useful later since it provides a (coupled) conductance description of all four branches in the model, namely

$$\begin{aligned} i_{EB} &= g_1(v_{EB}) - g_3(v_{CB}) \\ i_{CB} &= -g_4(v_{EB}) + g_2(v_{CB}), \end{aligned}$$

with $g_3(v_{CB}) = \alpha_R g_2(v_{CB})$ and $g_4(v_{EB}) = \alpha_F g_1(v_{EB})$.

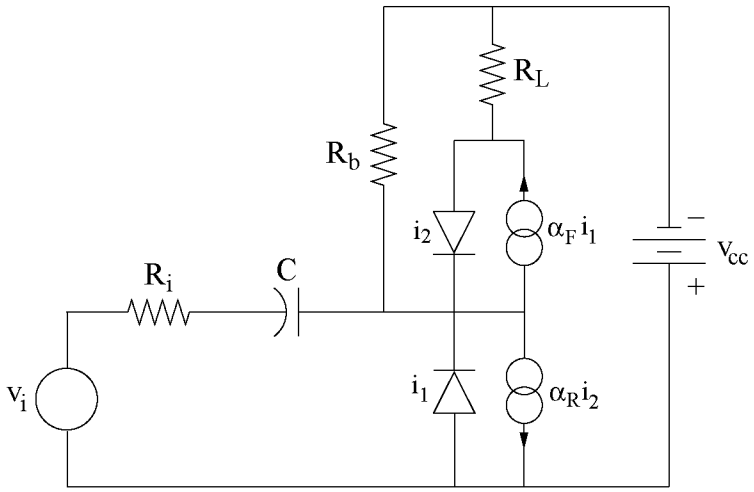

Figure 9: Equivalent circuit.

Omitting some details for the sake of brevity, the hybrid equations can be written for this circuit as

$$\begin{aligned} v_c' &= i_{R_i} && \text{(28a)} \\ 0 &= g_1(v_{EB}) - g_3(v_{CB}) - i_{R_L} - i_{R_b} + i_{R_i} && \text{(28b)} \\ 0 &= g_2(v_{CB}) - g_4(v_{EB}) + i_{R_L} && \text{(28c)} \\ 0 &= v_i(t) - v_c - R_i i_{R_i} + v_{EB} && \text{(28d)} \\ 0 &= -v_{cc} + R_b i_{R_b} + v_{EB} && \text{(28e)} \\ 0 &= -v_{cc} + R_L i_{R_L} + v_{EB} - v_{CB}. && \text{(28f)} \end{aligned}$$

This model is written in terms of the capacitor voltage v_c, the resistors' currents i_{R_i}, i_{R_b} and i_{R_L}, and the emitter-base and collector-base voltages v_{EB}, v_{CB}. Some simple computations show that the index one condition for the model (28), relying on the non-singularity of the matrix of partial derivatives of (28b)-(28f) w.r.t. the algebraic variables v_{EB}, v_{CB}, i_{R_i}, i_{R_b} and i_{R_L}, reads as

$$R_i + R_b + G_2 R_b R_L + G_2 R_i R_L + (G_1 + G_2 - G_3 - G_4) R_i R_b + (G_1 G_2 - G_3 G_4) R_i R_b R_L \neq 0. \quad (29)$$

Notably, this is again a sum of twig conductance and link resistance products. The different terms arising in this sum can be checked to correspond to certain spanning trees of the resistive minor depicted in Figure 10, where we label each device with its incremental conductance or resistance; note that in the controlled sources, each one of the conductances G_3 and G_4 depend on the voltage drop across the other junction. Specifically, the terms arising in (29) correspond to the products of twig conductances and link resistances in the spanning trees defined by the pairs R_b-R_L, R_i-R_L, G_2-R_i, G_2-R_b, G_1-R_L, G_2-R_L, G_3-R_L, G_4-R_L, G_1-G_2 and G_3-G_4, depicted in Figure 11.

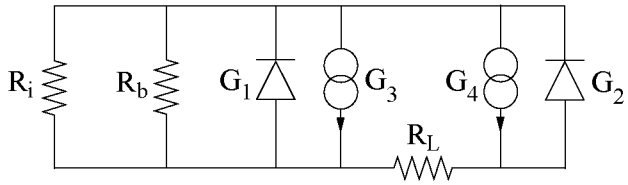

Figure 10: Resistive minor.

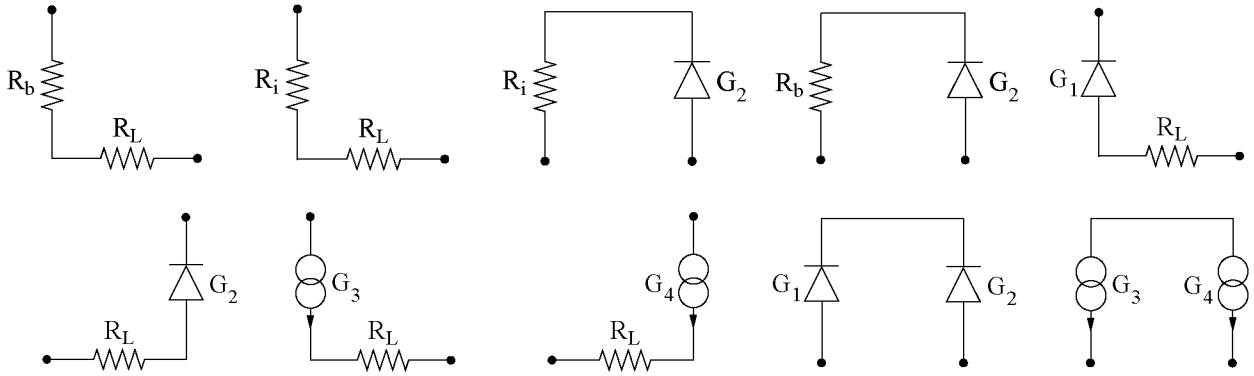

Figure 11: Balanced trees.

These trees are actually the *balanced* ones, in the terminology of [62]. A balanced tree is a spanning tree which (a) does not contain simultaneously a controlled source and its controlling branch, and (b) is such that the replacement of all controlled sources in the tree by their controlling branches still results in a tree. The first requirement rules out the pairs G_1-G_4 and G_2-G_3, and the second one precludes the pairs G_4-R_i and G_4-R_b (note that neither G_1-R_i nor G_1-R_b define a tree). One can check that the signature of the trees G_3-R_L, G_4-R_L and G_3-G_4 as defined in [62] is -1, and this is responsible for the "$-$" sign in the terms $G_3R_iR_b$, $G_4R_iR_b$ and $G_3G_4R_iR_bR_L$ within (29).

This example suggests that the results of [62] can be extended to the general context of hybrid models of circuits with controlled sources and multiports in the broader framework here considered, that is, including (in contrast to [62]) topologically degenerate configurations and both current-controlled and voltage-controlled resistors, as well as memristors. A general index analysis in this setting is in the scope of future research.

7 Concluding remarks

Hybrid circuit models, originally due to Kron [38], have been recently framed in a differential-algebraic setting [35, 36, 67]. Within a passive context, the DAE index of such models are proved in the aforementioned references to be not greater than one. In this paper we have extended the index analysis to the non-passive context, providing accurate index conditions in terms of the forests of certain digraph minors. The elimination of certain variables in the formulation of the model guarantees that also in the non-passive context the index is generically not greater than one. This provides a key computational advantage over Modified Nodal Analysis (MNA), supporting SPICE and other circuit simulators, for which certain circuit configurations are known to lead to index two models, thus requiring a more sophisticated numerical treatment.

The conditions arising in our analysis provide an exact description of the sets of index zero and index one points, and lead to an accurate description of the manifold of singularities where the index is not defined, yielding degenerate points where impasse phenomena are expected. The hybrid models and the index characterization have been extended to the context of memristive circuits. In both the classical and the memristive context, the results are of interest in the design of nonlinear oscillators and chaotic circuits, which are crucially based on the use of active devices. In particular, a memristor oscillator example has been used to illustrate different notions and results.

Our analysis virtually provides a complete index characterization of hybrid models of lumped circuits with one-port devices, not displaying controlled sources or coupling effects. An example involving a bipolar junction transistor suggests that our results can be extended to problems with certain types of controlled sources. Other active devices might lead to higher index problems, as it happens in other approaches; this is a topic that requires further study. In this direction, a general analysis of circuits with controlled sources and coupling effects, possibly including multiport and multiterminal devices, as well as the extension of the results to distributed circuits and to systems with other mem-devices, define lines for future research.

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