Low-Power Vertical Cavity NAND Gate

A. Hurtado[1], A.P. Gonzalez-Marcos[2], J.A. Martin-Pereda[3]
Universidad Politécnica de Madrid.
c/ Ciudad Universitaria s/n -28040- Madrid (Spain)

ABSTRACT

The study of the Vertical-Cavity Semiconductor Optical Amplifiers (VCSOAs) for optical signal processing applications is increasing his interest. Due to their particular structure, the VCSOAs present some advantages when compared to their edge-emitting counterparts including low manufacturing costs, high coupling efficiency to optical fibers and the ease to fabricate 2-D arrays of this kind of devices. As a consequence, all-optical logic gates based on VCSOAs may be very promising devices for their use in optical computing and optical switching in communications. Moreover, since all the boolean logic functions can be implemented by combining NAND logic gates, the development of a Vertical-Cavity NAND gate would be of particular interest. In this paper, the characteristics of the dispersive optical bistability appearing on a VCSOA operated in reflection are studied. A progressive increment of the number of layers compounding the top Distributed Bragg Reflector (DBR) of the VCSOA results on a change on the shape of the appearing bistability from an S-shape to a clockwise bistable loop. This resulting clockwise bistability has high on-off contrast ratio and input power requirements one order of magnitude lower than those needed for edge-emitting devices. Based on these results, an all-optical vertical-cavity NAND gate with high on-off contrast ratio and an input power for operation of only 10μW will be reported in this paper.

Keywords: Vertical-Cavity Semiconductor Optical Amplifier (VCSOA), Optical Bistability, Logic Gate, Optical Logic, optical computing

1. INTRODUCTION

The Optical Bistability (OB) in Semiconductor Laser Amplifiers (SLAs) has been widely studied in the recent past, due to the potential practical applications that this kind of devices could perform in the fields of optical computing and optical communications (for a review see [1]). Recently, the study of OB in Vertical-Cavity Semiconductor Optical Amplifiers (VCSOAs) has attracted the attention [2-4]. The VCSOA consists on a vertical resonant cavity formed by placing an active region between two Distributed Bragg Reflectors (DBRs). As a consequence of its particular vertical structure the VCSOA has a very small active region and therefore the top and bottom DBR should have high reflectivity values in order to be able to obtain a considerable amount of power at its output, but also because of the small length of the cavity, the VCSOA has single mode operation. These devices introduce additional advantages to those exhibited by their edge-emitting counterparts [2-5]. Among others, the benefits of using VCSOAs are: low cost manufacturing, single-mode operation, high-fibre coupling efficiency, mode-partitioning noise suppression and the capability to produce 2-D arrays of these devices for parallel processing applications.

Sánchez et al.[3][4] have recently studied the reflective optical bistability in VCSOAs. Their results demonstrated anticlockwise optical bistability and differential-gain occurring with an input power requirement reduced to only a few μWatts. They have also demonstrated, making use of the differential-gain characteristic, a low switching power vertical cavity AND gate, with optical gain and high on-off contrast ratio[6]. Nevertheless, all the results obtained by Sánchez et al[4] were limited to the observation of anticlockwise transitions for bistability and differential-gain, and consequently, only non-inverting logic could be developed, restricting the operability of the device to the implementation of AND and OR logic gates. Particularly interesting would be the capability to produce an all-optical vertical NAND gate. The fact that by the combination of NAND gates it is possible to implement all the rest of the boolean logic functions, added to

[1] ahurtado@tfo.upm.es
[2] agonmar@tfo.upm.es
[3] jamp@tfo.upm.es

Photonic Materials, Devices, and Applications, edited by
Gonçal Badenes, Derek Abbott, Ali Serpengüzel, Proc. of SPIE Vol. 5840
(SPIE, Bellingham, WA, 2005) · 0277-786X/05/$15 · doi: 10.1117/12.608468

the possibility to fabricate arrays of VCSOAs, may open new possible applications of this kind of devices in the fields of optical parallel signal processing or optical interconnecting.

In a previous work[2], the authors have studied theoretically the reflective optical bistability in a VCSOA using the model proposed by Adams[ref] for the study of the optical bistability in Fabry-Perot Semiconductor Laser Amplifiers (FPSLAs). In that work, apart from the classical anticlockwise bistable loop, the occurrence of two other forms of bistability in the reflective I/O Power characteristic of the VCSOA (the X-shape and the clockwise bistability) were predicted theoretically for the first time. Moreover, it was also reported that a progressive increment of the number of periods compounding the top DBR of the VCSOA, that acts as an interface of the power coming in and out of the device, results on a change of the assessed form of bistability from the typical anticlockwise to the clockwise bistable loop. Particularly important is the fact that the increase of the top DBR period number makes the clockwise bistability to appear for input power requirements one order of magnitude lower than those needed in the edge-emitting devices. This clockwise bistable loop, as it switches from a 'high' to a 'low' output state with associated hysteresis might be used for the development of inverting logic optical gates, including the capability to perform the XOR, the NOR and the NAND logic functions.

In this work an all-optical low power vertical-cavity NAND gate with a VCSOA working in reflection is predicted theoretically. The predicted NAND gate mechanism is based in the change in the characteristics and shapes of the optical bistability and differential gain produced by the addition of new periods in the VCSOA top Distributed Bragg Reflector (DBR). For this NAND gate low input power requirements reduced to optical power levels of only 8μW and an acceptable on-off contrast ratio of 5:1.

In section 2 the theoretical model used for the modeling of the reflective optical bistability in a VCSOA is introduced briefly. In section 3 the details and main parameters of the VCSOA used in the modeling are reported. The main results of the reflective optical bistability in a VCSOA are presented in section 4. The evolution of the optical bistability in the VCSOA as a function of the initial phase detuning, applied bias current and top DBR period number will be discussed also in Section 4. In Section 5 the predicted low-power Vertical-Cavity NAND gate is described and discussed. Finally, the conclusions of the work are included in Section 6.

2. THEORY

For the modeling of VCSOAs the Fabry-Perot approach [6] is used. In this approach the top and the bottom DBRs are replaced by highly reflectivity mirrors that are separated by an effective cavity length conforming a Fabry-Perot cavity. This effective cavity length includes the penetration of the optical field into the mirrors. The reflectivity of the top and bottom DBRs is given by[6]:

$$R_{DBR} = \left(\frac{1 - qp^{2m-1}a}{1 + qp^{2m-1}a} \right)^2 \tag{1}$$

where m is the number of periods that compound the Distributed Bragg Reflectors (DBRs) in each case. The variables p, q and a are respectively the low-to-high refractive index ratio of the two DBR layers, at the first and at the last DBR interface.

For the occurrence of optical bistability, the signal to be injected into the VCSOA must be slightly detuned to the long-wavelength side of the resonant peak of the VCSOA[3][4]. This fact allows the wavelength dependence of the DBR reflectivity to be ignored, since the reflection bandwidth of a typical DBR is very large compared to the difference between the wavelength of the external injected signal and the resonance wavelength of the VCSOA. As a consequence of the distributed reflectivity provided by the DBRs, the effective cavity length, L_c is larger than the distance of the cavity formed between the two DBRs, L_i, and it has to include both phase penetration depths into the top (L_{pt}) and the bottom (L_{pb}) DBRs in the form: $L_c = L_{pt} + L_i + L_{pb}$. To calculate both phase penetration depths into the DBRs the following expression is applied [6]:

$$L_p = \frac{\lambda_c}{4n_c} x \frac{q}{1-p} x \frac{\left(1-a^2p^{2m-1}\right)\left(1-p^{2m}\right)}{1-q^2a^2p^{4m-2}} \tag{2}$$

being n_c the averaged refractive index of the cavity formed between the two highly reflective mirrors, and λ_c is the operating wavelength. Once the VCSOA can be treated as a Fabry-Perot amplifier the study of the reflective bistability in the VCSOA is developed making use of the model proposed by Adams [7], commonly used for the study of the optical bistability in Fabry-Perot Laser Amplifiers. The model works under two basic assumptions: the spontaneous emission is neglected as it is much lower than the external injected optical power, and the optical intensity is considered to be uniform along the cavity. The model also neglects the transversal optical mode structure. The equations relating the injected, reflected and averaged internal power are given by[4][7]:

$$I_{av} = \frac{\left(1-R_t\right)\left(1+R_b e^{gL_c}\right)\left(e^{gL_c}-1\right)}{\left(1-\sqrt{R_tR_b}\,e^{gL_c}\right)^2 + 4\sqrt{R_tR_b}\,e^{gL_c}\sin^2\phi} \frac{P_{in}}{P_x g L_c} \tag{3}$$

$$P_R = \frac{\left(\sqrt{R_t}-\sqrt{R_b}\,e^{gL_c}\right)^2 + 4\sqrt{R_tR_b}\,e^{gL_c}\sin^2\phi}{\left(1-R_t\right)\left(1+R_b e^{gL_c}\right)\left(e^{gL_c}-1\right)} I_{av} P_y g L_c \tag{4}$$

where R_t and R_b are the top and bottom DBR reflectivity, L_c is the effective length of the VCSOA, g is the gain per unit length and ϕ is the single-pass phase change. P_x and P_y are scaling parameters and their values have been taken from the literature[4]. In the steady-state, the net gain coefficient and the relative phase change are expressed by:

$$gL_c = \frac{\Gamma g_0 L_c}{1+(I_{av}/I_s)} - \alpha_i L_c \tag{5}$$

$$\Phi = \Phi_0 + \frac{\Gamma g_0 L_c b}{2}\left(\frac{I_{av}/I_s}{1+I_{av}/I_s}\right) \tag{6}$$

where Φ_0 is the initial phase detuning, b is the material linewidth enhancement factor, α_i is the internal loss coefficient, I_s is the saturation intensity, g_0 is the unsaturated gain coefficient expressed by $g_0=a(n-n_0)$ where a is the linear material gain coefficient, n_0 is the transparency carrier density and n is the carrier density without external optical injection and finally, the confinement factor Γ relates the volumes of the active region and the effective cavity, $\Gamma=L_a/L_c$.

3. MODELED VCSOA

The parameters used for the modeling of the VCSOA are all included in Table 1. Applying equation (1) the reflectivity of the top and the bottom DBR are respectively equal to $R_t=0.9955$ and R_b=0.9993. The top and bottom penetrations depths are calculated with equation (2) and are respectively: $L_{pt}=0.3794\mu m$ and $L_{pb}=0.3808\mu m$, that added to the length of the cavity existing between the two DBRs, leads to an effective cavity length of $L_c=1.56\mu m$. The approximation carried out taking account the effective cavity length and the highly reflective mirrors leads to a Fabry-Perot model of the VCSOA, and therefore a threshold condition can be applied, giving an expression for the threshold gain[8]:

$$g_{th} = \frac{1}{\Gamma L_c}\ln\left(\frac{1}{\sqrt{R_tR_b}}\right) + \frac{\alpha_i}{\Gamma} \tag{7}$$

and as the threshold gain is also a function of the carrier density at threshold in the form: $g_{th}=a(n_{th}-n_0)$, being n_{th} the carrier density at threshold, the threshold current for the VCSOA is given by[8]:

$$I_{th} = q\left(\frac{n_{th}}{\eta_i}\right)\left(\frac{\Gamma L_c Area}{\tau}\right) \tag{8}$$

where q is the electron charge, η_i is the internal quantum efficiency and τ is the recombination time. In this case, having substituted in the equations (7) and (8) the parameters of the modeled device listed in Table 1, the VCSOA has a calculated threshold current of 7.33mA.

Table 1. Parameter used for the modeling of the VCSOA

VCSOA Parameter	Value
Wavelength (nm), λ	853.33
Cavity Length (μm), L_i	$3\cdot\lambda/n_c$
Cavity refractive index, n_c	3.2
Top DBR periods	16[1] & 22[2]
Bottom DBR periods	25
DBR high/low refractive indexes, (μ_h/μ_l)	3.45/2.89
Substrate refractive index (μ_s)	3.45
Active region area (μm^2)	$\pi\cdot 10^2$
Confinement Factor, Γ	0.1
Internal Quantum Efficiency, η_i	1
Linear Material Gain Coeff. (cm^2), a	$2.7\cdot 10^{-16}$
Linewidth Enhancement Factor, b	2.7
Linear Recombination Coeff. (1/s), A	$1\cdot 10^8$
Bimolecular Recomb. Coeff. (m^3/s), B	10^{-16}
Auger Recombination Coeff. (m^6/s), C	$5\cdot 10^{-42}$
Transparency Carrier Density ($1/m^3$), n_0	$1.5\cdot 10^{24}$
Fixed Internal Loss (1/m), α	1,000
P_x	200,000
P_y	260,000

[1]Used for the study of the Reflective Optical Bistability in a VCSOA
[2]Used for the modeling of the Vertical-Cavity NAND Gate.

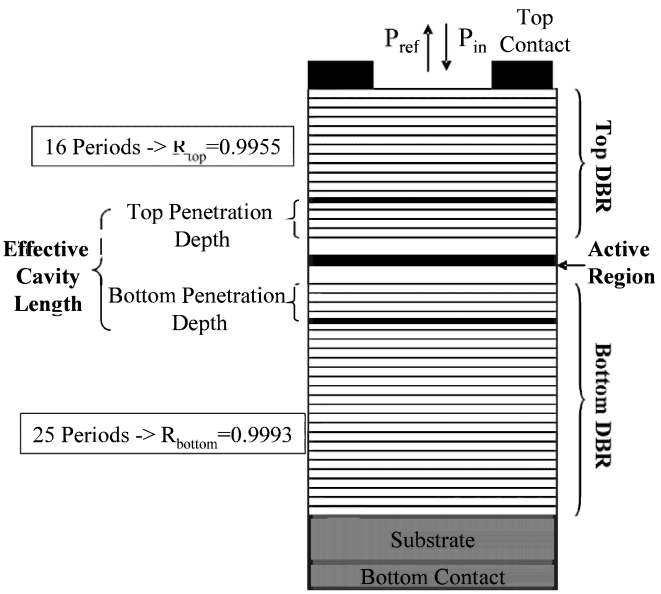

Fig. 1. Structure of a VCSOA.

4. RESULTS OF THE REFLECTIVE OPTICAL BISTABILITY IN THE VCSOA

The graphical representations of figs. 4-6 show the evolution of the bistable behavior of a VCSOA operated in reflection as a function of main device and system parameters, including the bias current, the initial phase detuning and the top DBR periods number. The parameters used for the modeling of the VCSOA are listed in Table 1. The results are here presented briefly, for a complete study of the reflective optical bistability in a VCSOA see [2].

Fig. 2 shows the calculated reflected versus input optical power characteristic of the VCSOA as a function of the applied bias current. The evolution of the bistable behavior of the VCSOA is reported for six different levels of bias current (from 99.5% to 97% of the threshold level) keeping constant the initial phase detuning at a value of $-5\cdot10^{-4}\pi$, where π represents the separation between adjacent longitudinal modes. In all cases anticlockwise bistable transitions appear for input power requirements of some μwatts in the I/O power characteristics of the VCSOA operated in reflection. Higher input power requirements for the assessment of bistability, narrower hysteresis cycles and lower on-off contrast ratio between output states are obtained when the applied bias current to the VCSOA is reduced.

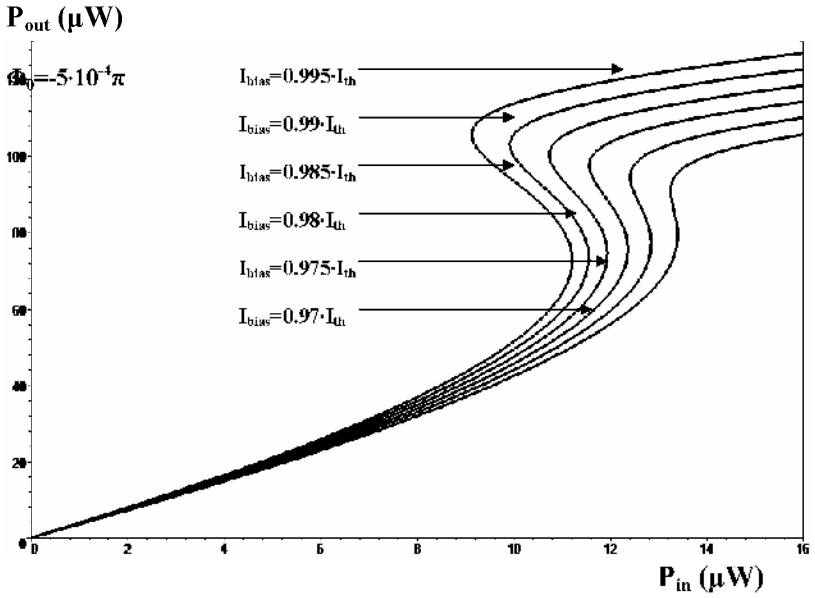

Fig. 2. Reflected versus Input Power to the VCSOA for fixed initial phase detuning equal to $-5\cdot10^{-4}\pi$ and different applied bias currents as indicated.

Another critical parameter in the study of the reflective optical bistability in a VCSOA is the initial phase detuning, directly related to the initial frequency (wavelength) separation between the resonant peak of the VCSOA and the frequency of the external injected signal. Fig. 3 shows the I/O power characteristics of the VCSOA operated in reflection for different values of the initial phase detuning, as indicated, keeping constant in all cases the applied bias current, which is equal to the 99% of the threshold level. Fig. 3 shows the evolution in the shape of the reflective optical bistability in a VCSOA as the initial phase detuning is incremented. As the detuning is increased the bistability changes from the classical anticlockwise bistable loop to the clockwise bistable loop, with the intermediate X-shape or butterfly bistable loop. Once a clockwise bistable transition is obtain, it might be possible to develop inverting logic, including NAND and NOR logic gates [10]. Anyway, the NAND logic gates that could be develop in this situation will have a small on-off contrast ratio and higher input power requirements for operation[11], around 150μW, compared to those reported for the development of an Vertical-Cavity AND logic gate[5].

Fig. 4 shows the evolution of the reflected versus input power characteristic of the VCSOA at fixed bias current (99.5% of the threshold value) and frequency detuning of $-3\text{x}10^{-4}\pi$, as the number of periods conforming the top DBR is

increased from 16 to 22. The evolution from the anticlockwise to the clockwise bistable loop can be clearly seen. The reason explaining this behavior relies on the delicate balance existing between the reflected, internal averaged and transmitted intensity [2]. It is remarkable the fact that the modification on the structure of the VCSOA, reduces in more than one order of magnitude the input power needed to achieve clockwise bistable transitions compared to that needed by a lower top DBR reflectivity VCSOA (see fig. 3) and compared to the input power requirements needed also in in-plane devices[8]. It is also very important to point that the assessed clockwise bistable transitions are characterized, as seen in fig. 4, by a high on-off contrast ratio and low input power requirements. These features are ideal for the development of inverting logic elements, including NAND logic gates.

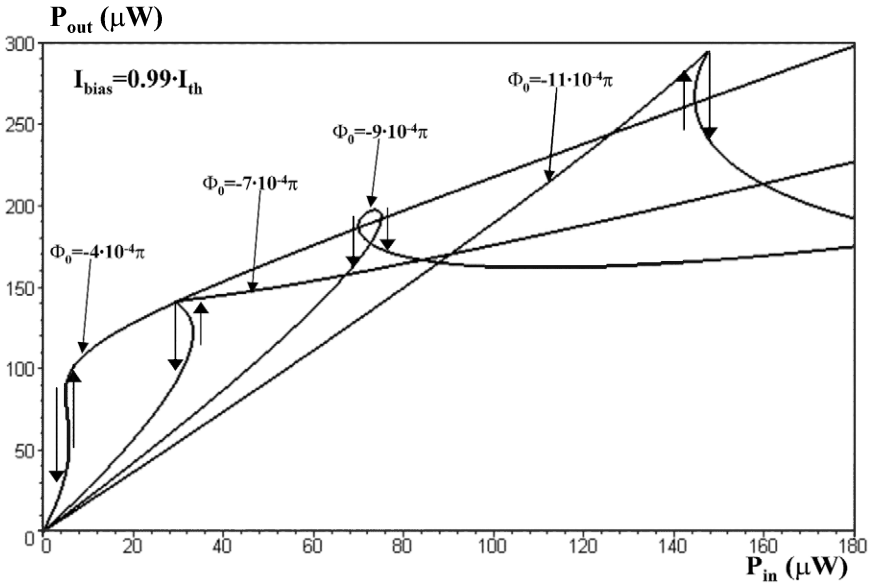

Fig. 3. Reflected versus Input Power to the VCSOA for several initial phase detuning, Φ_0, with constant applied bias current equal to the 99% of value at threshold.

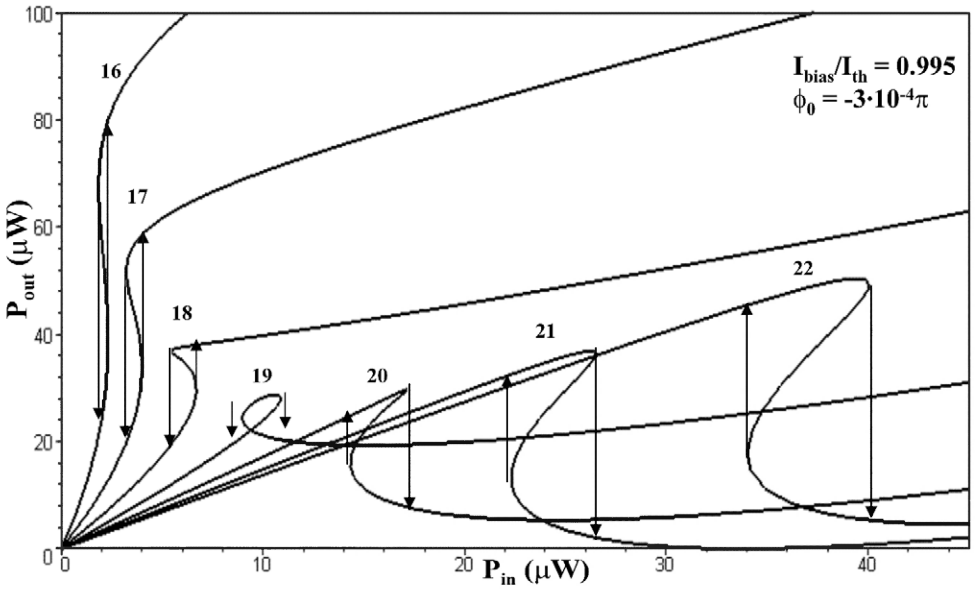

Fig. 4. Reflected versus Input Power to the VCSOA for different number of periods conforming the top DBR (as indicated) and fixed values of initial phase detuning, $-3\cdot10^{-4}\pi$, and bias current $0.99\cdot I_{th}$.

5. VERTICAL-CAVITY NAND GATE

Once the clockwise switching transition with low input power requirements and high on-off contrast ratio has been obtained, it is possible to produce a NAND gate using a VCSOA. For that purpose a VCSOA whose parameters are listed in table 1 has been modelled. The top DBR of the VCSOA is configured with 22 periods, what leads to a reflectivity value of the top DBR of 0.9994. Reducing now the initial frequency detuning existing between the external signal frequency and the resonant frequency mode of the VCSOA to only $-1.5\text{x}10^{-4}\pi$ (4.5Ghz) and the applied bias current to the 98% of the threshold value, the input power needed for switching is considerably lowered. At the same time, the optical bistability is not anymore observable, appearing now in the I/O power relation what we call *differential-loss*, as it is the opposite phenomenon to the *differential-gain* reported by Sánchez et al[4][5]. In this particular case of OB, the associated hysteresis cycle disappears, appearing now an abruptly decaying nonlinear function. Fig. 5. shows the resulting I/O power characteristic which is going to be the transfer function of the vertical-cavity NAND gate reported in this work.

Fig. 5. shows that the reported *differential-loss* characteristic occurs for an approximated input power of only 7μW. Distinguishing in the graphical representation of fig. 4, a threshold level, delimiting the logic levels of the '1' and '0' bits to be considered at the output of the modelled gate and selecting a proper set of values for the signals involved in the logical processing, namely, two optical digital data signals and an optical bias signal, it is possible to develop a NAND gate with the reported transfer function, as it is shown in fig. 5. Concretely in this work, the bias power signal has a amplitude of 4μW and the '1' bit of the optical data signals is configured with a power of only 2μW. For these working conditions the on-off contrast ratio is found to be higher than 5:1. Another potential advantage associated with the use of a VCSOA is the high-frequency performance [5]. Westlake et al[12] reported that the maximum speed of optical bistability in in-plane semiconductor laser amplifiers operated below threshold is limited by the recombination time. Recently, Wen et al[5] have suggested that, due to small size of the active region of the VCSOA and its quantum well structure, the VCSOA will have a better high-frequency response.

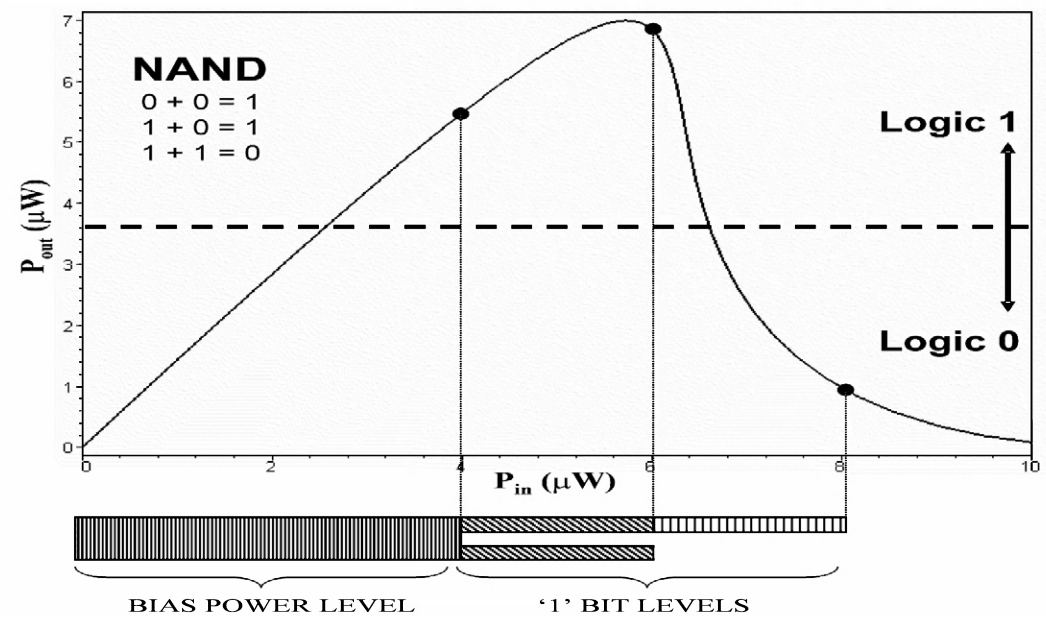

Fig. 5. Vertical Cavity NAND gate I/O Power Characteristic and working mechanism

Consequently an all-optical vertical-cavity NAND gate with very low input requirements, high on-off contrast and high frequency response is reported in this work. The assessment of an optical vertical-cavity NAND logic gate is of particular interest for many reasons. First of all as by combinations of NAND logic gates, the whole set of logic

functions could be obtained. Also the capability to fabricate 2-D arrays of this kind of devices could increase significantly the total achievable processing speed and could be useful for optical signal processing applications in the field of optical computing and optical interconnect applications in optical telecommunication networks. For future works, the application of VCSOAs to previously reported optical logic processing structures should be consider [13][14].

6. CONCLUSIONS

The addition of new periods on the top DBR of a VCSOA modifies the characteristics of the optical bistability and differential-gain appearing in the reflective mode of operation from an anticlockwise to a clockwise switching mechanism. This feature has been used to model, for the first time to our knowledge, a vertical cavity NAND gate with a total power requirement of only 8μW, an on-off contrast ratio equal to 5:1 and high-frequency performance. The assessment of a vertical cavity NAND gate is of particular interest, as the rest of the logic functions can be implemented from the combination of NAND gates, and for the possibility to manufacture 2-D arrays of this kind of devices. These two features could make VCSOAs very attractive for parallel optical signal processing or optical interconnecting applications either for optical computing or optical telecommunication networks.

ACKNOWLEDGEMENTS

This work was partly supported by CICYT, grant TIC2003-04309, and CAM "Comunidad Autónoma de Madrid", grant FPI- Formación Personal Investigador.

REFERENCES

1. H. Kawaguchi, *Bistabilities and Nonlinearities in Laser Diodes*, Norwood:MA, 1994.
2. A. Hurtado, A. Gonzalez-Marcos, J.A. Martin-Pereda, 'Modeling Reflective Bistability in a Vertical-Cavity Semiconductor Optical Amplifier (VCSOA)', in the IEEE Journal of Quantum Electronics, Vol. 41, No. 3, pp. 376-383. March 2005.
3. M. D. Sánchez, P. Wen, M. Gross and S. Esener, "Nonlinear Gain in Vertical-Cavity Semiconductor Optical Amplifiers", in IEEE Photonics Technology Letters, Vol. 15, No 4, pp. 507-509. April 2003.
4. P. Wen, M. D. Sánchez, M. Gross and S. Esener, "Observation of bistability in a Vertical-Cavity Semiconductor Optical Amplifier (VCSOA)", in Optics Express, Vol. 10, No. 22, pp. 1273-1278. November 2002.
5. P. Wen, M. D. Sánchez, M. Gross and S. Esener, "Vertical-cavity optical AND gate", in Optics Communications, 219, pp. 383-387. (2003).
6. J. Piprek, S. Björling, and J.E. Bowers, "Design and Analysis of Vertical- Cavity Semiconductor Optical Amplifiers", in IEEE Journal of Quantum Electronics, Vol. 37, No. 1, pp. 127-134. January 2001.
7. M. J. Adams, H. J. Wetlake, M. J. O'Mahony, and I. D. Henning, "A comparison of Active and Passive Optical Bistability in Semiconductors" in IEEE J. Quantum Electron., Vol. 21, No. 9, pp. 1498-1504, September 1985.
8. P. Pakdeevanich and M. J. Adams, "Measurements and Modeling of Reflective Bistability in 1.55μm Laser Diode Amplifiers", in IEEE Journal of Quantum Electronics, Vol. 35, No. 12, pp. 1894-1903. December 1999.
9. G. P. Agrawal, *Semiconductor Lasers, Past, Present, and Future,* Woodbury, NY: AIP Press, 1995. pp. 145-180.
10. J. E. Midwinter, "Light' Electronics, Myth or Reality?", in IEE Proceedings, Vol. 132, Pt. J., No. 6, pp. 371-383. December 1985.
11. A. Hurtado, A. González-Marcos, J.A. Martín-Pereda "All-Optical Vertical-Cavity Logic Gates" in *Optoinformatics'04. Abstracts of the Internacional Topical Meeting '2004*, pp. 19-21. Saint-Petersburg, 18-21 October 2004. ISBN: 5-7577-0157-7.
12. H. J. Westlake, M. J. Adams, and M. J. O'Mahony, "Assesment of Switching Speed of Optical Bistability in Semiconductor Laser Amplifiers", in Electronics Letters, Vol. 22, No. 10, pp. 541-543. 8th May 1986.
13. A. González-Marcos and J. A. Martín-Pereda, "Method to analyze the influence of hysteresis in optical arithmetic units", in Optical Engineering, Vol. 40 No. 11, pp. 2371-2385. November 2001.
14. A. Hurtado-Villavieja and A. Gonzalez-Marcos, "An all-optical programmable logic gate with 1550nm laser diode amplifiers", in *EOS Topical Meeting Optics in Computing 2004*, pp. 5-6. Engelberg (Switzerland), 21-23 April 2004. ISBN: 3-00-013069-1.