# Minimum Time Control for Multiphase Buck Converter: Analysis and Application

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***Abstract*—The combination of minimum time control and multiphase converter is a favorable option for DC-DC converters in applications where output voltage variation is required, such as RF amplifiers and dynamic voltage scaling in microprocessors, due to their advantage of fast dynamic response. In this paper, an improved minimum time control approach for multiphase buck converter that is based on charge balance technique, aiming at fast output voltage transition is presented. Compared with the traditional method, the proposed control takes into account the phase delay and current ripple in each phase. Therefore, by investigating the behavior of multiphase converter during voltage transition, it resolves the problem of current unbalance after the transient, which can lead to long settling time of the output voltage. The restriction of this control is that the output voltage that the converter can provide is related to the number of the phases, because only the duty cycles at which the multiphase converter has total ripple cancellation are used in this approach. The model of the proposed control is introduced, and the design constraints of the buck converter's filter for this control are discussed. In order to prove the concept, a four phase buck converter is implemented and the experimental results that validate the proposed control method are presented. The application of this control to RF envelope tracking is also presented in this paper.**

***Index Terms*—Minimum time control, multiphase converter, voltage variation, charge balance, envelope amplifer.**

## I. Introduction

Analog linear control is the classic control in power converters. However, the demands for power supplies with very fast dynamic response in modern electronic applications require complex control algorithms [1]. For example, in power supplies for microprocessors, dynamic voltage scaling (DVS) technique is applied in order to reduce the energy consumption. The supply voltage is dynamically adjusted to the workload conditions. The voltage transition has to be fast enough to comply with performance requirements [2]. Fast voltage variation is also required in power amplifiers (PA), because energy efficiency can be dramatically improved by supplying PA with a voltage proportional to the signal's envelope [3]. Traditional analog linear control needs high bandwidth to achieve fast dynamic response, which means high switching frequency and, consequently, high switching losses. Nevertheless, the minimum time control technique, as a non-linear control, can provide change of the output voltage beyond the limitation of the bandwidth [4].

Minimum time control (or time-optimal control) is theoretically from optimal control for switched systems [5], [6], which has been used to achieve fast transient responses for load steps and fast output voltage variations.

For fast load transient responses, in [1], minimum time control is derived from a piecewise linear model and implemented as a pre-calculated solution in a look-up table [2]. But it requires an accurate model of the actual converter. In [7]–[11], the controllers use the observed current and voltage to calculate the transition time. In these solutions the current of the output capacitor is estimated or observed in order to calculate the charge change during the transition. Therefore, minimum time control can be calibrated to compensate that charge change of the output capacitor by calculating the on-off times dynamically in every transition. Comparing with the pre-calculated solution, the solution with the observer can be implemented without preliminary knowledge of the converter.

For the output voltage variations, the control principle is similar to load transients. However, in the load transients the output voltage always remains the same after the transition, while in the output voltage variation, both output voltage and current may change after the transition, like in DVS systems [2]. The aim of the output voltage variation is to change the system from a stable initial state to a stable target state within a defined time. In both states, the average inductor current is equal to the load current. Therefore, at the end of the transient, the output voltage has to be equal to the voltage of the target state, and the average inductor current has to be equal to the current of the target state as well.

If the transient time in the minimum time control is similar to, or even lower than the switching period of the converter, the steady state ripple in the output voltage is comparable to the voltage change during transient, which is not acceptable in the most applications. Increasing the switching frequency can reduce the ripple, but there is a limitation to the frequency rise, which are the switching losses. One solution to overcome this problem is to use a multiphase interleaved converter to reduce the filtering requirements without increasing the switching frequency [12], because the multiphase converter increases the effective switching frequency by N, being N is the number of phases [13].

In this paper, we present a minimum time control on a multiphase buck converter, which can improve the performance of the converter's output voltage transition. Section II describes the principle of minimum time control and the reason why we need to change the traditional minimum time control method for fast output voltage variations in multiphase applications. Section III and IV propose a model to apply the minimum time control in the multiphase buck converter. Section V addresses the filter design of converter for a specific slew rate of the output voltage which is one of critical specifications in some

applications. Section VI includes the experimental results and compares the performance of the traditional model and the proposed model. Section VII presents an application example of the proposed control technique.

## II. Minimum Time Control for Buck Converter

The minimum time control is derived from Pontryagin's Principle. For a single phase buck converter, if the system is driven from one initial state ($V_C$ and $I_L$ before transition) to a target state ($V_C$ and $I_L$ after transition) in the shortest possible time, the control during the transition consists of two intervals: on-time (main switch on) and off-time (main switch off). For the step-up transition (in our case, we focus on voltage transition), it is from on-time to off-time and from off-time to on-time for the step-down transition. Using phase-plane trajectory from the geometric control surface, the length of the on-time and off-time can be obtained to achieve minimum time transition [14], [15]. However, some approximations can be done in order to get analytical expressions for minimum control in most of applications, which lead to the charge balance method [16] described by observing Fig. 1. It shows a buck converter's approximated output capacitor voltage and inductor current during step-up voltage transition. The inductor current exceeds load current in the transition time. The charge (green part) is accumulated on the output capacitor, which is needed to achieve the required output voltage variation.

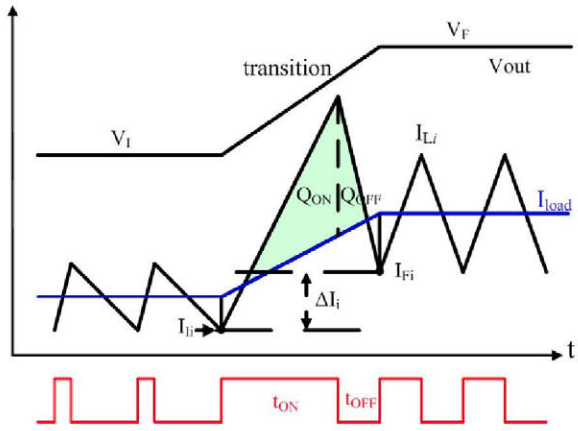



Fig. 1: Waveforms in a voltage transition with resistive load.

As aforementioned, a multiphase interleaved converter has some advantages over the single phase version such as reduced ripple, dynamic response, etc. Many applications nowadays employ a multiphase converter instead of a single phase. For a N phase buck converter, there are N+1 state variable and N switching events are needed to perform a minimum time transient. One switching event per phase is analysed in this paper. However, in most of the works, the multiphase buck converter is considered as an equivalent single buck converter, in which the equivalent inductor value is L/N (inductor value of each phase divided by the number of phases) [2], [17], [18]. This equivalent model is valid for linear control analysis, but problematic for minimum time control analysis. In the equivalent model, phase shifting among phases is neglected, and the minimum time control law is calculated with an equivalent single phase buck converter. Therefore, all the phases would have the same control signals during the transition, as shown in Fig. 2. A phase current unbalance would occur after the transition, which would result in output voltage overshoot and a second order oscillation. The reason for current unbalance can be explained by the phase shift: every phase has different "initial phase current" due to this phase shift. In both initial state and target state, periodic phase currents have fixed phase delay, but applying the same transition control signals in all the phases cannot produce the appropriate phase currents between two states. In order to solve this problem, we propose that the different minimum time control signals (on-time and off-time) referring to the phase delay are needed to achieve phase current balance, which cannot be obtained by the equivalent inductor model. The model based on the charge balance method is presented in the next section.

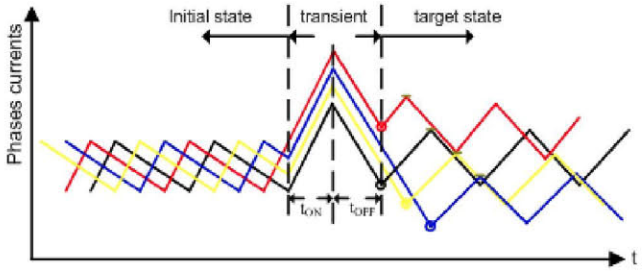



Fig. 2: Inductor current waveforms show unbalance after voltage transition caused by phase shifting.

## III. Proposed Minimum Time Control in a Multiphase Buck Converter

### A. Timing calculation

The multiphase buck converter using the interleaving technique has advantages regarding filter reduction and dynamic response. A multiphase interleaved buck converter has current ripple reduction for all duty cycles [19]. Additionally, it has several discrete duty cycles at which the converter shows complete ripple cancellation. Therefore, the output capacitor can be smaller which results in improved dynamic response of the converter. The multiphase buck converter has been widely used in applications like microprocessor power supplies and automotive power systems due to these advantages. In order to calculate the on and off times of the minimum time control, this paper presents a pre-calculated solution based on the charge balance method.

Using Kirchhoff's current law, the currents can always be expressed as (see Fig. 3):

$$\sum_{i=1}^{N} i_{Li} = i_c + i_{load} \tag{1}$$

Considering that the current through inductor during on-time and off-time of the transition should compensate the charge provided to the load and the charge needed for the voltage change, it is possible to analyze the charge flow during the transition. During the transient time, from initial voltage

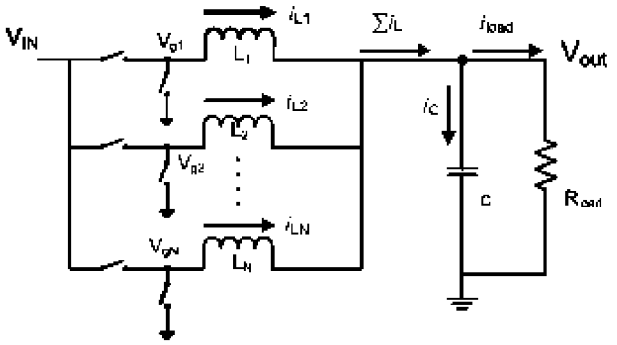



Fig. 3: Power stage of multiphase buck converter.

($V_1$) to the target voltage ($V_2$), the charge change at the output capacitor is

$$\triangle Q_C = C(V_2 - V_1) = C \cdot \triangle V = \int_{t_1(V_C=V_1)}^{t_2(V_C=V_2)} i_C \cdot dt \quad (2)$$

And during the transient time, the load receives the charge:

$$Q_{LOAD} = \int_{t_1(V_C=V_1)}^{t_2(V_C=V_2)} i_{load} \cdot dt \quad (3)$$

which comes from the converter's inductor. Therefore, the charge balance can be represented by

$$\sum_{i=1}^{N} Q_{Li} = \triangle Q_C + Q_{LOAD} \quad (4)$$

where $Q_{Li}$ is the charge provided by each phase of the multiphase converter. The system in Fig. 3 can be defined with state variables, the inductor currents $i_{Li}$ and the voltage of output capacitor $v_c$ by:

$$\begin{cases} \dfrac{di_{Li}}{dt} = \dfrac{V_{gi} - V_{out}}{L_i} \\ \dfrac{dV_c}{dt} = \dfrac{\sum_{i=1}^{N} i_{Li} - i_{load}}{C}, \end{cases} \quad V_{gi} = \begin{cases} V_{in}, & \text{phase i is on} \\ 0, & \text{phase i is off} \end{cases} \quad (5)$$

With this model and charge balance method, the minimum time problem can be numerically solved with a mathematic tool. However, it is possible to simplify the problem and derive analytical solutions, if the following conditions are applied.

- The filter (L, C) is ideal.
- Assume that the output voltage changes linearly during the transition.

The filter's parasitic parameters are not involved in this model, because their effects can be eliminated during the transition in the interleaved multiphase buck converter [4]. Therefore, the ideal filter assumption is considered to simplify the calculation. Being a fast transition, the output voltage is approximately linear, which makes the second assumption acceptable. Therefore, the voltage during the transition can be expressed as:

$$V_{out}(t) = V_1 + \frac{\triangle V}{\triangle t} \cdot t \quad (6)$$

Where $V_1$ is the buck's initial output voltage before the transient starts, $\triangle t$ is the duration of the transient and $\triangle V$ is the voltage difference of the target and initial voltage. With the assumption of linear voltage change, if it is a step-up transition, the instantaneous current in each phase can be calculated by (7) from (5) and (6).

Therefore, the charge provided by each phase is represented by (8)

$$Q_{Li} = \int_0^{\triangle t} i_{Li} \cdot dt = -\frac{V_{in}}{2L} t_{ON,i}^2 - \frac{V_1}{2L} \triangle t^2 + \frac{V_{in} t_{ON,i} \triangle t}{L} + I_i \triangle t - \frac{\triangle V \triangle t^2}{6L} \quad (8)$$

where $I_i$ is the $i^{th}$ inductor's initial current at the beginning of the transient, $t_{ON,i}$ is the interval time when the main switch of the $i^{th}$ phase is turned on and L is the value of the inductor in each phase. With (4) and (8), one equation with $t_{ON,i}$ and $\triangle t$ can be found. In order to get the solution for them, other relations between $t_{ON,i}$ and $\triangle t$ are required. According to the second assumption again, for each phase:

$$L \triangle I_i = V_{in} t_{ON,i} - V_1 \triangle t - \frac{1}{2} \triangle V \triangle t \quad (9)$$

where $\triangle I_i$ is the current difference of the phase current after and before the transient (Fig. 2). Equation (9) leads to:

$$t_{ON,i} = K \cdot \triangle t + \frac{L \cdot \triangle I_i}{V_{in}}, \quad K = \frac{V_1 + \frac{V_2}{2}}{V_{in}} \quad (10)$$

$$t_{ON,i}^2 = K^2 \triangle t^2 + \frac{L^2 \triangle I_i^2}{V_{in}^2} + \frac{2KL}{V_{in}} \triangle t \triangle I_i \quad (11)$$

From (10) it can be seen that the "on time" of each phase can be presented using the total transition time and the information regarding the system (inductance, input voltage, initial and final voltage level). Having in mind that the "off time" is easily obtained by subtracting the "on time" ($t_on, i$) from the transition time ($\triangle t$) it can be concluded that knowing the $\triangle t$ is sufficient to know the duration of the switching event for each phase. Therefore in the continuation of the calculus, the transition time $\triangle t$ is calculated for two types of load (current source and resistive load).

**Current source load**: As mentioned before, the sum of $\triangle I_i$ is related with the load current of initial and target states. We can first consider that the load is a variable current source

$$i_{Li}(t) = \begin{cases} -\dfrac{\triangle V}{2 \cdot L_i \cdot \triangle t} \cdot t^2 + \dfrac{V_{in} - V_1}{L_i} \cdot + I_1, \text{when} 0 < t < t_{ON,i} \\ -\dfrac{\triangle V}{2 \cdot L_i \cdot \triangle t} \cdot t^2 - \dfrac{V_1}{L_i} \cdot t + \dfrac{V_{in}}{Li} + I_1, \text{when} t_{ON,i} < t < \triangle t \end{cases} \quad (7)$$

(later we will discuss resistive load), which is the case of a real application [15]. However, if the transition is sufficiently fast (even can be shorter than one switching period of the converter), the load current will be, approximately, constant during the transient time. Therefore, the load current during the transient is assumed to be constant, and hence:

$$\sum_{i=1}^{N} \triangle I_i = 0 \tag{12}$$

Combining equations (10)-(12), it can be obtained:

$$\sum_{i=1}^{N} t_{ON,i} = nK \triangle t \tag{13}$$

$$\sum_{i=1}^{N} t_{ON,i}^2 = nK^2 \triangle t^2 + \frac{L^2}{V_{in}^2} \sum_{i=1}^{N} \triangle I_i^2 \tag{14}$$

Since the parameters of the converter and the state voltage ($V_1$, $V2$) are known,$\sum_{i=1}^{N} \triangle I_i^2$ can be calculated. Equation (4), (8), (13) and (14) yield an intermediate equation:

$$\begin{aligned} C \triangle V + I_{load} \cdot \triangle t = \triangle t^2 (&-\frac{V_{in}}{2L} nK^2 + \frac{V_{in}}{L} nK \\ &- \frac{V_1}{2L} n - \frac{\triangle V}{6L} n) \\ &- \frac{L}{2V_{in}} \sum_{i=1}^{N} \triangle I_i^2 + \sum_{i=1}^{N} I_i \cdot \triangle t \end{aligned} \tag{15}$$

where n is the phase number. Combining (4) and (8) with (15), the on and off time for each phase can be obtained. However, equation (15) indicates that the transition time is related with the load current (the second term on the left side of (15)) and the sum of the phase currents (the second term on the right side of (15)). The sum of the phase currents is equal to the sum of the load current and capacitor current (due to the voltage ripple). Nevertheless, if the converter is always in the "node" duty cycles (D=i/n, i=1, 2 ... n, n is the number of phase), it has total current and voltage ripple cancellation. It means the current of the output capacitor in (1) will always be zero and the load current always equals the current in the phases. Therefore, it can be written:

$$I_{load} \cdot \triangle t = \sum_{i=1}^{N} I_i \cdot \triangle t \tag{16}$$

and (15) can be simplified by:

$$\triangle t = \sqrt{\frac{(C \triangle V + \frac{L}{2V_{in}} \sum_{i=1}^{N} \triangle I_i^2)}{(-\frac{V_{in}}{2L} nK^2 + \frac{V_{in}}{L} nK - \frac{V_1}{2L} n - \frac{\triangle V}{6L} n)}} \tag{17}$$

Now the on and off times can be analytically solved. It is important to notice that the transition time $\triangle t$ is the same for all the phases, while the ON and OFF time for each phase is different. Another important conclusion is that the transition time does not depend on the value of the load current. Nevertheless, it depends on the difference of the phase current before and after the transient (the last term of (17)), but it can be calculated as it will be shown later. In the case when the "node" duty cycles are used, the output voltage has discrete levels that depend on the number of converter's phase. Additionally, these duty cycles also give a favorable advantage to output capacitor design, because there is no ripple on the output capacitor. It means small capacitor can be used without suffering from the ripple, which is also demanded by fast output voltage change. Equation (8) is for the calculation of charge from each phase. In the step-down transition case, it is changed by:

$$Q_{Li} = \frac{V_{in}}{2L} t_{ON,i}^2 - \frac{V_1}{2L} \triangle t^2 + I_i \triangle t - \frac{\triangle V \triangle t^2}{6L} \tag{18}$$

And the equation to calculate $\triangle t$ should be:

$$\triangle t = \sqrt{\frac{(C \triangle V - \frac{L}{2V_{in}} \sum_{i=1}^{N} \triangle I_i^2)}{(\frac{V_{in}}{2L} nK^2 - \frac{V_1}{2L} n - \frac{\triangle V}{6L} n)}} \tag{19}$$

The "on-time" of each phase ($t_{ON,i}$) is calculated by substituting (19) into (10), while the "off-time" is obtained by subtracting $t_{ON,i}$ from $\triangle t$.

**Resistive load**: For a resistive load, the difference is the charge to the load during the transition. Taking that into account, the equation for $\triangle t$ is modified to be:

$$\begin{aligned} C \triangle V = \triangle t^2 (&-\frac{V_{in}}{2L} nK^2 + \frac{V_{in}}{L} nK - \frac{V_1}{2L} n - \frac{\triangle V}{6L} n) \\ &+ \triangle t (\frac{V_1}{R} - (1-K) \cdot \sum_{i=1}^{N} \triangle I_i - \frac{V_1 + V_2}{2R}) \\ &- \frac{L}{2V_{in}} \sum_{i=1}^{N} I_i^2 \quad \text{(step-up)} \end{aligned} \tag{20}$$

$$\begin{aligned} C \triangle V = \triangle t^2 (&\frac{V_{in}}{2L} nK^2 - \frac{V_1}{2L} n - \frac{\triangle V}{6L} n) \\ &+ \triangle t (\frac{V_1}{R} - (1-K) \cdot \sum_{i=1}^{N} \triangle I_i - \frac{V_1 + V_2}{2R}) \\ &+ \frac{L}{2V_{in}} \sum_{i=1}^{N} I_i^2 \quad \text{(step-down)} \end{aligned} \tag{21}$$

First, $\triangle t$ is obtained by resolving (20) or (21). Then, the calculation of "on-time" and "off-time" is the same as the current source load. From (8) and (15), it can be found that $\triangle I_i$ in the moment when the transient starts have to be known to calculate $\triangle t$. However, if the transient is synchronized with PWM duty cycle, $\triangle I_i$ can be calculated using input voltage, duty cycle, inductance and information about the phase shifting. One of the synchronizing ways is to start the transient at the end of PWM cycle of one phase (rising or falling edge). At this moment, all the phases enter the minimum time control and each phase will have different on-time and off-time (equation (13) and (14)), but the same transition time. Then the minimum time control ends at the beginning of PWM cycle of that phase (rising or falling edge)

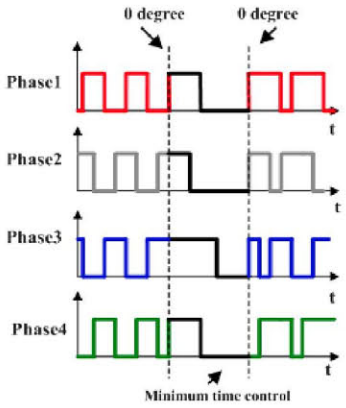



Fig. 4: Control signal for output voltage transition from $0.5V_{in}$ to $0.75V_{in}$.

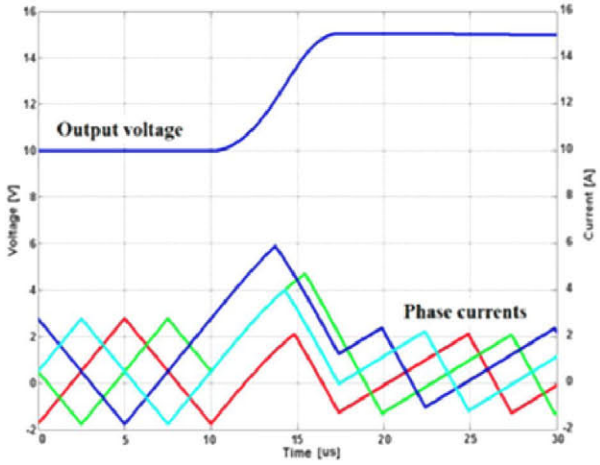
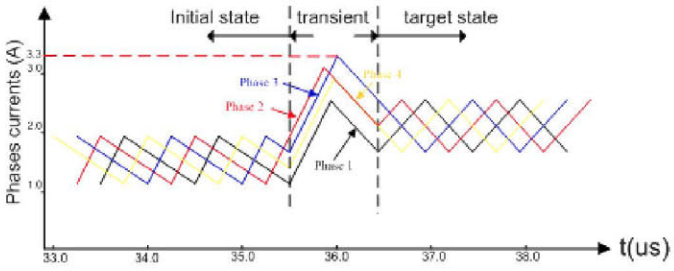


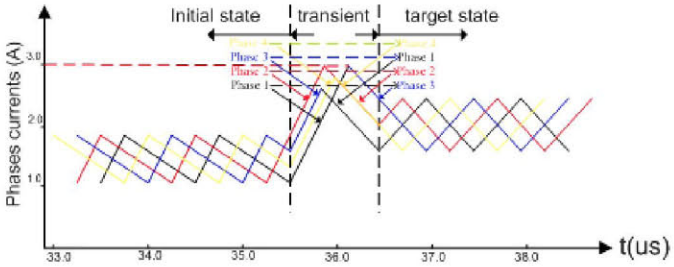

Fig. 5: Simulation waveforms in the voltage transition from $0.5V_{in}$ to $0.75V_{in}$.

and keeps the corresponding phase delay for the rest phases. Fig. 4 shows a control example of 4-phase buck converter when the transition is from $0.5V_{in}$ to $0.75V_{in}$. Therefore, $\triangle I_i$ for each phase can be exactly calculated. Additionally, the factor that affects the transient time will be the sum of $\triangle I_i$, not the current of each phase itself, which indicates that a good inductor currents balance is not needed in this model. Another important conclusion that can be obtained from these equations is that the minimum time control calculation does not depend on the load current value, which is important for the pre-calculation method. Fig. 5 shows the simulated output voltage and phase currents during the transient using MATLAB with the control signals shown in Fig. 4.

One additional advantage that can be obtained with the proposed control is that the phase order can be rearranged after the transition. This can bring some benefits from the point of view of the peak inductor current. The calculation shows that $t_{ON,i}$ and $\triangle t$ depend on the filter (L, C), input voltage ($V_{in}$), initial state voltage ($V_1$), target state voltage ($V_2$) and current difference between two states ($\triangle I_i$). All the parameters are fixed by applications except $\triangle I_i$. As it is explained, the previous analysis takes for granted that there is the same reference phase (it is called the first phase) in




(a) The phases correspondence is maintained after voltage transition




(b) The phases correspondence is optimized after voltage transition

Fig. 6: Phase current waveforms in a voltage transition showing the peak inductor current.

both initial and target states, and all other phases are also fixed (do not change their phase delay referring to the first phase). Therefore, the earlier calculation for $\triangle I_i$ is based on this method (see Fig. 6(a)). However, the phases order after the transition can be rearranged. For example, the reference phase (first phase) of the initial state can change to the second phase (with i/n phase shifting) in the target state, and any other phase can also be changed. The important thing is that it has to keep phase-to-phase correspondence. Then $\triangle I_i$ is changed by the new correspondence (see Fig. 6(b)). Table I shows $\triangle I_i$ for two different phase combinations. Through phase rearrangement, this control can obtain lower peak current in the inductor but it is penalized by a longer transition time.

### *B. Filter design constraint*

The inductor limits the slew rate of the current through the output capacitor, and the output capacitance value determines the charge that has to be delivered during the transient time to change the output voltage. Therefore, the output filer (L, C) limits the response time of the buck converter to change the output voltage. And this transient time has to be lower than the required tracking time of the system. The transient time that the converter can accomplish to change from one state to another one can be calculated with filter values. However, the design way is usually inversed. The maximum transient time of the converter that can be accepted is determined by applications. For the given maximum signal slope, there are many possibilities for the filter parameters (L, C). The constraint condition (22) can be obtained from the equations in section III.

TABLE I: Comparison between original phase correspondence and selected one

| Initial phase | Original phase correspondence | | | | | reorder phase | selected phase correspondence | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | $\triangle I(A)$ | $\sum(\triangle I_i)^2$ | $t_on(ns)$ | $\triangle t(ns)$ | $I_{peak}(A)$ | | $\triangle I(A)$ | $\sum(\triangle I_i)^2$ | $t_on(ns)$ | $\triangle t(ns)$ | $I_{peak}(A)$ |
| $1^{st}$ | -0.188 | 0.703 | 218 | 666 | 2.975 | $3^{rd}$ | 1.313 | 2.8125 | 484 | 707 | 2.742 |
| $2^{nd}$ | -0.563 | | 156 | | | $2^{nd}$ | -0.563 | | 171 | | |
| $3^{rd}$ | 0.563 | | 343 | | | $1^{st}$ | -0.938 | | 109 | | |
| $4^{th}$ | 0.188 | | 281 | | | $4^{th}$ | 0.188 | | 296 | | |

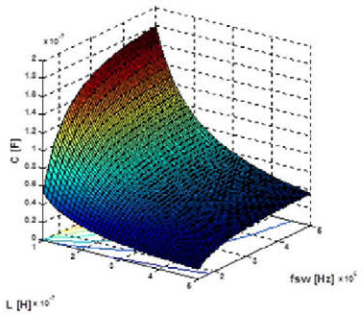



Fig. 7: Filter design example to track envelope with the maximum slope $50V/\mu s$.

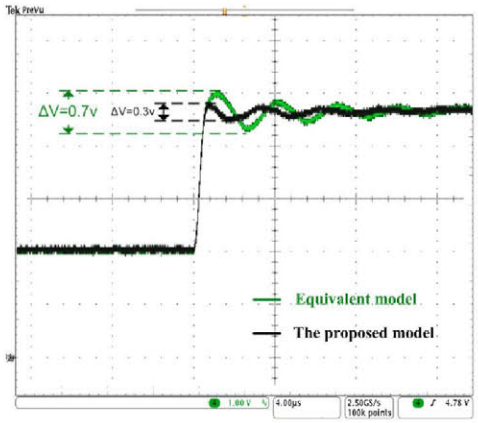



Fig. 9: Comparison of voltage transition performance between the equivalent model and proposed model.

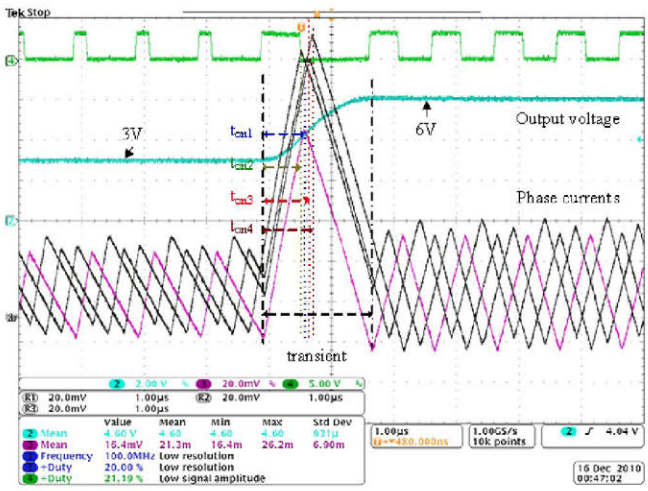
$$C < \frac{\triangle V}{6Lm^2}(6V_{in} \cdot N \cdot K - 3N \cdot V_1 - N \cdot \triangle V - 3N \cdot K^2 \cdot V_{in}) - \frac{L}{2V_{in} \triangle V} \sum_{i=1}^{N} \triangle I_i^2 \quad (22)$$

In (22), m is the maximal slew rate which the multiphase buck converter can achieve and N is the number of phases. Fig. 7 shows the constraint of the filter to track the envelope with a slope lower than $50V/\mu s$. The combinations of L, C and $f_{sw}$ on the surface are the minimum requirement in order to track this envelope. The switching frequency, $f_{sw}$ is used to calculate the current ripple in order to obtain $\triangle I_i$ in the equations. Additionally, to design for very fast output voltage transient, a high ratio between L and C is needed to charge the output capacitor fast. And it makes inductor size large. On the other hand, the good regulation under the load current change requires a low ratio between L and C. It reduces the size of inductor, but increases the inductor current ripple and output voltage ripple. Therefore, the transient speed and regulation tradeoff is needed for a specific design.

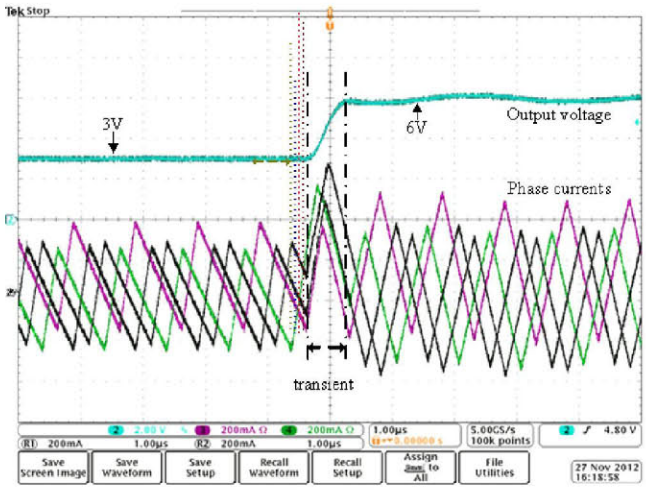
## IV. Experimental results

The minimum time control is validated in a four-phase buck prototype with a current source load. Fig. 8 shows the voltage step-up and step-down transitions with two different output filters, corresponding to different transition times, which shows a output voltage change from 3V to 6V (25% duty cycle to 50%) and from 9V to 6V (75% duty cycle to 50%). The input voltage is 12V and the switching frequency is 1MHz. The transition with filter L=$6.8\mu H$ and C=$1\mu F$, lasts for $1.7\mu s$ and $1.4\mu s$ transition time from 3V to 6V and from 9V to 6V respectively; the other one with the filter L=$4.5\mu H$ and C=220nF, lasts for $0.65\mu s$ and $0.58\mu s$ respectively (less than a switching cycle). It is important to notice that there is not voltage oscillation after the transient. Fig. 8 shows that there is slight phase currents unbalance, but it doesn't affect the minimum time control, which corresponds with theoretical predictions. (Fig. 8 (a) and (c) only show one and two control signals respectively due to clarity of the figures) In fact, the experimental result for the voltage transition always involves some oscillations, due to inaccurate LC model, finite resolution of FPGA clock and the assumption regarding the linear voltage change during the transition. Nevertheless, this control shows exact consideration on current ripple for the minimum time control, which is better than the one of the equivalent buck converter. Therefore, the performance of the proposed minimum time control is compared with the one based on the equivalent buck [8] in Fig. 9. The performance of the multiphase buck converter based on equivalent buck model has more oscillations and longer settling time than the proposed control ($0.7V_{pk-pk}$ vs $0.3V_{pk-pk}$ and $7\mu s$ vs $2\mu s$). This difference can be explained from the performance of phase currents in Fig. 10(a) and (b) . As mentioned in the last section, the equivalent inductor model can not include the phase shifting information for the transition, which leads to the current unbalance after the transient. On the other hand, the proposed control shows good match of the phase current as the calculation predicts. The importance of the current balance after transient is that it prepares the converter for the next transition faster.

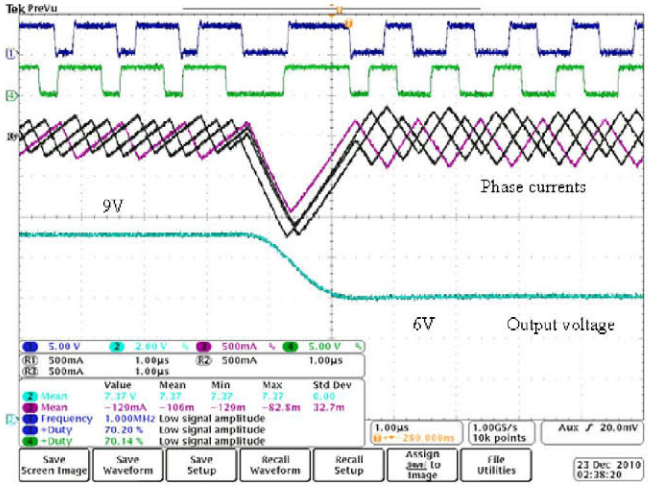
The control strategy is implemented in an FPGA (Fig. 11). Four counter modules are used in the program to generate the PWM signal. With different initial counter value, four PWM counters can work in an interleaved way. There is a process in the program to synchronize the transient with one of the PWM signals by counters. At the end of the transient time, the new



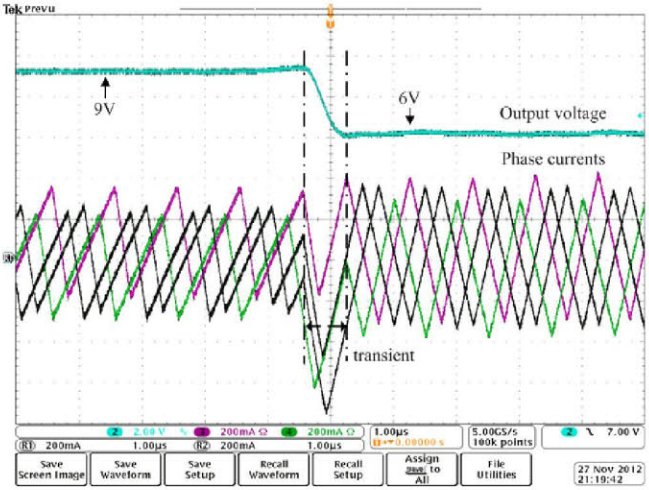

(a) Output voltage step from 3V to 6V, 1MHz (2V/div) and Phase currents (200mA/div), L=6.8$\mu H$, C=1$\mu F$




(b) Output voltage step from 3V to 6V, 1MHz (2V/div) and Phase currents (200mA/div), L=4.5$\mu H$, C=220nF

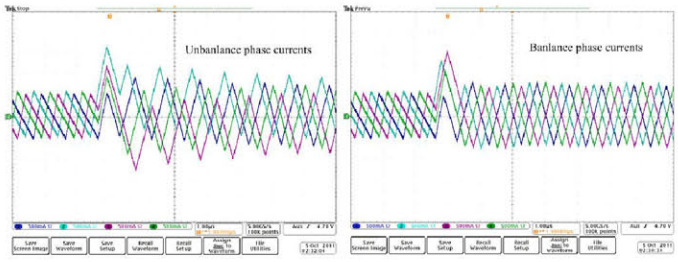



(c) Output voltage step from 9V to 6V, 1MHz (2V/div) and Phase currents (500mA/div), L=6.8$\mu H$, C=1$\mu F$




(d) Output voltage step from 9V to 6V, 1MHz (2V/div) and Phase currents (200mA/div), L=4.5$\mu H$, C=220nF

Fig. 8: Voltage transient with different filters.




(a) Phase current waveforms of control with the equivalent inductor model (b) Phase current waveforms of the proposed control

Fig. 10: Phase current waveforms of the equivalent inductor model and the proposed control in voltage variation.

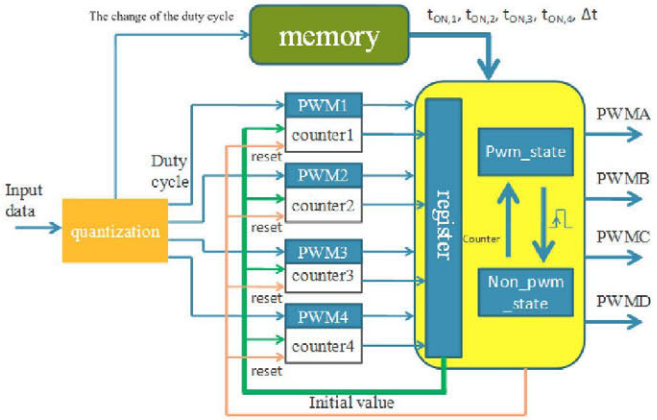



Fig. 11: The control scheme in the FPGA.

initial value has to be given to the counter. The required on-time and off-time in the transient are in the look-up table of the program. The control has been tested in open-loop.

Table II shows the comparison of the on-time and off-time between the calculation and the experiment. The considered transition is from an output voltage $0.25V_{in}$ to $0.5V_{in}$. The

TABLE II: Comparison of interval time from $0.25V_{in}$ to $0.5V_{in}$

| phase | L=6.8$\mu H$ C=1$\mu F$ | | | | L=4.5$\mu H$ C=220nF | | | |
|---|---|---|---|---|---|---|---|---|
| | calculation | | experiment | | calculation | | experiment | |
| | $t_{ON}[\mu s]$ | $t_{OFF}[\mu s]$ | $t_{ON}[\mu s]$ | $t_{OFF}[\mu s]$ | $t_{ON}[ns]$ | $t_{OFF}[ns]$ | $t_{ON}[ns]$ | $t_{OFF}[ns]$ |
| $1^{st}$ | 2.5 | 5.02 | 2.5 | 4.18 | 230 | 467 | 210 | 470 |
| $2^{nd}$ | 1.88 | 5.64 | 1.82 | 4.86 | 168 | 529 | 150 | 530 |
| $3^{rd}$ | 3.76 | 3.76 | 3.98 | 2.7 | 355 | 342 | 340 | 340 |
| $4^{th}$ | 3.13 | 4.39 | 3.15 | 3.53 | 293 | 404 | 270 | 410 |

smaller filter shows shorter transition time, and the experimental results show smaller deviation from the calculation. It is due to the aforementioned assumption that the output voltage changes linearly during the transition time, which produces an inherent error (the maximal deviation in this example is 28%). When the transition time is short, the output voltage during the transition is closer to the linear one.

## V. Application of RF amplifier

One application of the proposed method is the envelope amplifier for RF power amplifiers (using Envelope Elimination and Restoration, EER (Fig. 12) or envelope tracking technique) [20], [21]. The envelope amplifier is a DC-DC converter whose output voltage is proportional to the RF envelope. One of the solutions for this converter is to use a multilevel converter in series with a linear regulator (Fig. 13). The linear regulator has excellent dynamic behavior that is good for envelope amplifier but suffer from low efficiency. However, if the linear regulator's supply voltage can be modulated by the multilevel converter according to the required instantaneous output voltage, the voltage drop across the power transistor of linear regulator is significantly reduced resulting in reduced power losses [22]. The multilevel converters' output voltage has discrete levels to roughly track the envelope, seen in Fig. 14. There are several proposals for this multilevel converter in the state of art [22], [23], but all these methods use complex circuits such as isolated converter cells and multi-output transformer. Our proposal presents a medium complexity and high performance solution using the multiphase buck converter with minimum time control as an alternate of multilevel converter.

The number of the produced voltage levels is equal to the number of the phases and the multiphase converter has to operate in the nodes in order to guarantee ripple cancellation. Fig. 16 shows the prototype of an envelope amplifier, which is used to validate our concept. The D-A converter provides the envelope reference generated by FPGA for the linear regulator. The experimental result of this prototype with 500kHz 64QAM envelope reference is shown in Fig. 15. As in the multilevel converter in [19], the proposed control also allows the multiphase buck converter change from one output voltage level to any other level (such as directly from $0.25V_{in}$ to $V_{in}$), which is favorable for this envelope amplifier because the digital envelope information can be known in advance. The average output power is around 3W and the peak output power is 12.1W. With the proposed control, around 60% average efficiency is obtained. The oscillation of the multiphase buck converter output voltage can be observed, which is at the resonant frequency of the output filter. However, it is not a penalty since there is a linear regulator. Increasing the margin between the supply voltage and the output voltage of the linear regulator, the oscillation can be avoided.

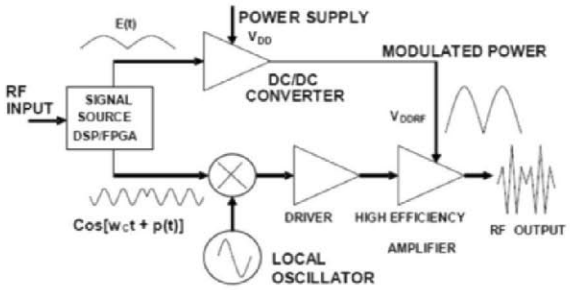



Fig. 12: Simplified block diagram of EER technique.

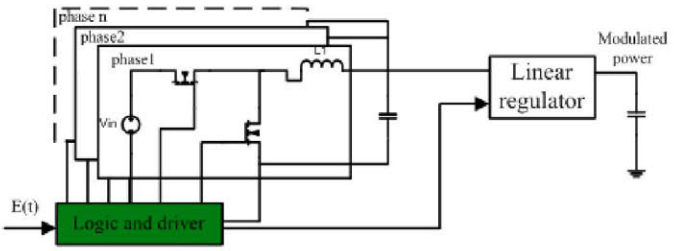



Fig. 13: The envelope amplifier using multiphase buck converter in series with a linear regulator.

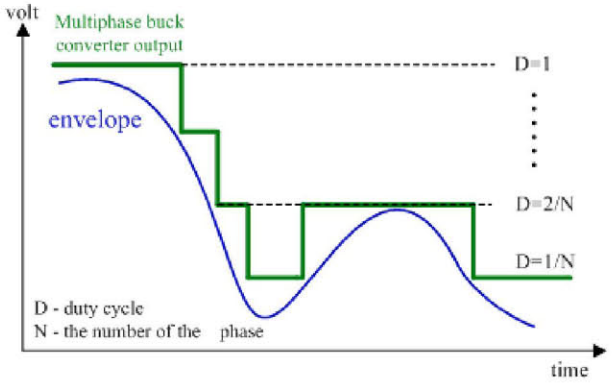



Fig. 14: Time diagrams of the envelope amplifier.

## VI. Conclusions

This research is motivated by the fast dynamic voltage transition demanded by some applications. An improved minimum time control is applied to a multiphase buck converter, obtaining improved voltage transition performance, which can also be applied in other power topologies. The objective of minimum time control in this case is to change the converter's output voltage from an initial state to a target state as fast as

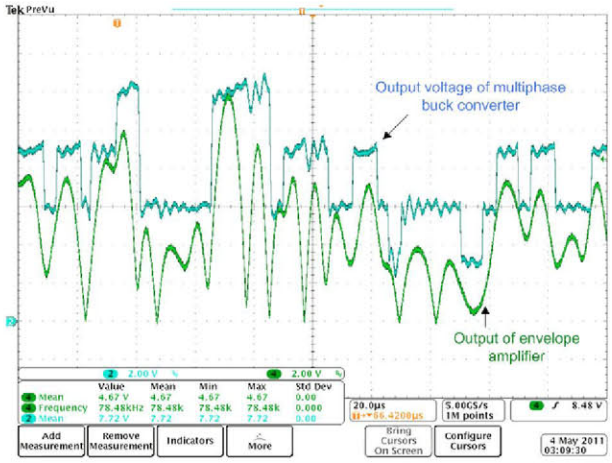



Fig. 15: The envelope amplifier performance with 64QAM.

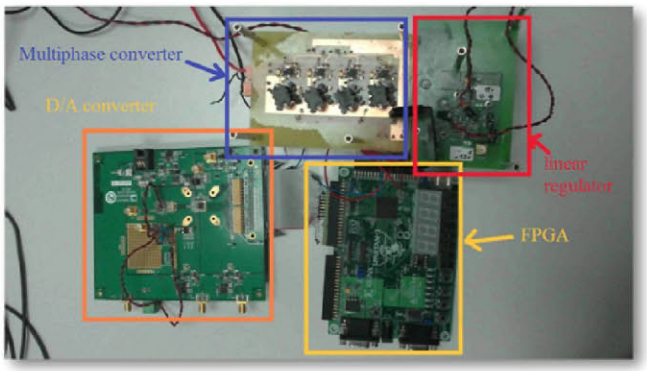



Fig. 16: The envelope amplifier prototype.

possible, avoiding large oscillations after the transition. Our approach is to take the different initial and target transient state of the phases into account, which is caused by phase shifting. This paper presented a model to calculate the transient parameters based on the charge balance principle. The different on and off times in the transition for each phase is originally proposed in this model, which contributes to keep the balance of phase currents after the transition. This improvement results in smaller oscillation and shorter settling time, compared with the equivalent inductor model. This model is applied in open loop with all the parameters stored in the look-up table to validate the mathematical analysis. The filter (L, C) constraint to achieve the maximum slew rate of RF envelope is also analyzed. According to this improved minimum time control, there are only discrete voltage levels corresponding to the number of phases and the input voltage. Digital control makes this complex control practical with FPGA. However, very short transient time in this control requires very high resolution of the controller, which is a challenge for the hardware. The concept is validated in a four phase buck converter. It shows the reduction of oscillation and settling time after the voltage transition, compared with the equivalent inductor model. This converter is also tested for an RF application, showing the feasibility to track a 500kHz 64QAM envelope. The efficiency of the envelope amplifier is as high as 60%.

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